THERMAL DESIGNS, MODELS AND OPTIMIZATION FOR THREE-DIMENSIONAL INTEGRATED CIRCUITS

BY

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DISSERTATION

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ABSTRACT

Three-dimensional integrated circuits (3D ICs), a novel packaging technology, are heavily studied to enable improved performance with denser packaging and reduced interconnects. Despite numerous advantages, thermal management is the biggest bottleneck to expanding the applications of this device stacking technology. In addition to implementing the thermal-aware designs of existing methodologies, it is necessary to implement new features to dissipate heat efficiently.

This work presents two main aspects of thermal designs: on-chip level and package level. First, we propose a novel thermal-aware physical design on chip between devices. We aim to mitigate localized hotspots to ensure the functionality by adding thermal fin geometry to existing thermal through-silicon via (TTSV). We analyze design requirements of thermal fin for single TTSV as well as TTSV cluster designs with the goal of maximizing heat dissipation while minimizing the interference with routing and area consumption. An analytical model of the three-dimensional system and thermal resistance circuit is built for accurate and runtime-efficient thermal analysis.

In terms of high-performance computing systems in 3D ICs, thermal bottlenecks are much more challenging with merely on-chip design solutions. Inter-tier liquid cooling microchannel layers have been introduced into 3D ICs as an integrated cooling mechanism to tackle the thermal degradation. Many existing research works optimize microchannel designs based on runtime-intensive numerical methods or inaccurate thermo-fluid models. Hence, we propose an accurate but compact closed-form model of tapered microchannel to capture the relationship between the channel geometry and heat transfer performance. To improve the accuracy, our correlations are based on the developing flow model and derived from numerical simulation data on a subset of multiple channel parameters. Our model achieves 57 % less error in Nusselt number and 45 % less error in pressure drop for channels with inlet

width 100-400 µm compared to a commonly used approximate model on fully developed flow.

Next, we present the correlations for diverging channels as well as complete correlations that extend to any linearly tapering channel models, that include diverging shape, uniformly rectangular shape and converging shape. The complete models provide the flexibility to analyze and optimize any arbitrary geometry based on the piecewise linear channel wall assumption.

Finally, we demonstrate the optimized channel designs using the derived correlations. Tapered channel models provided the flexibility to incorporate any arbitrary shapes and explore the advanced geometries during the optimization. The microchannel is divided into small segments in axial direction from inlet to outlet and piecewise optimized. The simulated annealing method is applied in our optimization, and channel width at one randomly chosen segment interface is altered to evaluate the design at each iteration. The objective is to minimize the overall thermal resistance while pressure drop is maintained less than a threshold value and channel widths have minimum and maximum boundaries. We compare the designs with the optimization based on fully developed flow models and verify the channel performance through numerical simulations.

To guarantee optimality, accurate analysis is crucial. Our proposed models have significantly improved the accuracy by applying the appropriate flow assumption. However, many opportunities exist to increase the design flexibility and the accuracy. Fluid conditions, such as coolant material and varying volumetric flow rate, can also be part of the optimization parameters to expand the design scope. Moreover, physical phenomena, such as reduced friction on the channel walls or a vortex created on abrupt angle changes, can be considered to improve the accuracy in the closed-form models.

To my Romeo, for his love and memory.

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LIST OF ABBREVIATIONS

2D IC	Two-Dimensional Integrated Circuits
3D IC	Three-Dimensional Integrated Circuits
CFD	Computational Fluid Dynamics
FEM	Finite Element Method
FVM	Finite Volume Method
ILD	Inter-Layer Dielectric
SA	Simulated Annealing
SIMPLE	Semi-Implicit-Method for Pressure-Linked-Equations
SOI	Silicon-On-Insulator
TSV	Through-Silicon Via
TTSV	Thermal Through-Silicon Via

NOMENCLATURE

$\dot{V}$	Volumetric flow rate	[m^3/s]
ν	Kinematic viscosity	[m^2/s]
ρ	Density	[kg/m^3]
A	Cross-sectional area	[μm^2]
A_{wet}	Wetted surface area	[μm^2]
AR	Aspect ratio	
d	Distance between objects	[μm]
D_h	Hydraulic diameter	[μm]
dz	Section length	[μm]
f	Fanning friction factor	
f_D	Darcy friction factor	
f_i	Volume fraction of the layer i	
H	Height	[μm]
h	Convection coefficient or heat transfer coefficient	[W/m^2-K]
h_{avg}	Average heat transfer coefficient	[W/m^2-K]
I	Electrical current	[A]
k	Thermal conductivity	[W/m-K]

k_{eff}	Effective thermal conductivity	[W/m-K]
L	Length	[µm]
$L_{fd,h}$	Hydrodynamic entrance length	[µm]
$L_{fd,t}$	Thermal entrance length	[µm]
L_{fin}	Thermal fin length	[µm]
N	Number of sections	
Nu	Nusselt number	
Nu_z	Local Nusselt number in position z	
P	Pressure	[Pa]
p	Perimeter	[µm]
Pr	Prantdl number	
Q	Heat flux	[W/cm^2]
Q	Heat rate	[W]
R	Electrical resistance	[Ω]
$R_{th,cond}$	Conductive thermal resistance	[K/W]
$R_{th,conv}$	Convective thermal resistance	[K/W]
$R_{th,eq}$	Equivalent thermal resistance	[K/W]
R_{th}	Thermal resistance	[K/W]
Re	Reynolds number	
T	Temperature	[K or °C]
t	Thickness	[µm]
T_b	Bulk temperature	[K]
T_w	Channel wall temperature	[K]

u	Velocity	[m/s]
V	Electrical voltage	[V]
w	Width	[µm]
w_{in}	Channel inlet width	[µm]
w_{out}	Channel outlet width	[µm]
z	Length-wise position in channel	

CHAPTER 1

INTRODUCTION

Moore's law has been the golden rule for the electronic industry for more than 50 years since 1965. It is the observation that the number of transistors in an integrated circuit (IC) doubles every 18 months to two years [1]. As semiconductor technology scales, highly integrated circuits face various bottlenecks in two-dimensional integrated circuits (2D IC) manufacturing technology and can no longer scale in accordance with Moore's law [2]. Limited by the nature of physics, the future of Moore's law is diminishing and numerous scientists and engineers have been developing technologies to prolong the trend or even achieve advanced improvement. Vertical, or three-dimensional (3D), integration is a promising manufacturing technology to realize denser packaging and increased performance with reduced interconnect lengths. However, the thermal challenge is exacerbated on 3D integration implementations due to the low thermally conductive adhesive layer between device tiers and denser packaging that causes an increase in power density, and thus might further result in malfunction.

1.1 Three-Dimensional Integrated Circuits

More than a decade ago, three-dimensional integrated circuits (3D ICs) were introduced as a promising breakthrough to overcome the physical bottleneck of denser packaging previously achieved from transistor miniaturization for "more than Moore" [3]. The 3D IC is realized by adding a third dimension to the two-dimensional devices. Two or more conventional 2D ICs are vertically stacked on one another (die-to-die, die-to-wafer, or wafer-to-wafer [4]) with electrically insulated bonding layer in between as shown in Figure 1.1. To complete the electric connections between the stacked device tiers, through-silicon vias (TSV) are inserted as routing. The structure resembles the struc-

ture of a multistory building, where each device layer is considered as a floor. It has become an attractive field of research to mitigate several problems. Stacked ICs reduce interconnect lengths mainly due to the usage of electronic TSVs. This leads to less wire delay and reduction in Joule heating. Not only can it achieve higher transistor densities and shorter interconnect lengths on a given footprint, but it is also a new paradigm for heterogeneous integration, such as central processing unit (CPU) and memory or digital and analog components on a single chip [5].

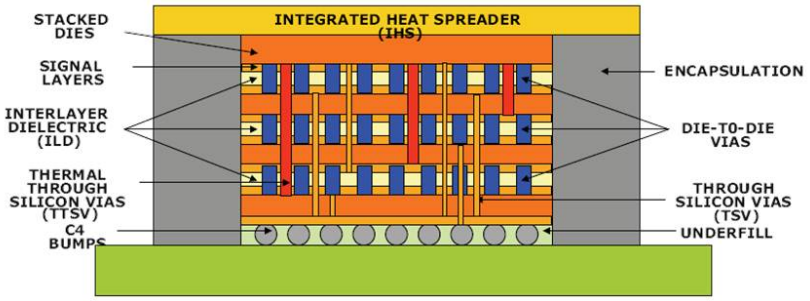


Figure 1.1: Three-dimensional integrated circuit diagram [6].

Recently, a 3D stacked memory chip was officially announced [7] and mass production is imminent [8]. However, 3D IC also comes with some problems as well as exacerbated issues. Inserting TSVs leads to the increase in footprint and decrease in chip reliability due to manufacturing difficulties and stress to the neighboring features. Moreover, higher active transistor count per cooling area and increased vertical thermal resistances in bonding layer due to multiple silicon-on-insulator (SOI) layers and inter-layer dielectrics (ILD) increases on-chip operating temperature. Thus, high-performance multi-processors or heterogeneous device integrations still face thermal bottlenecks due to high heat density.

Heat dissipation has been the most critical barrier to advancing core-to-memory or core-to-core stacking, which has higher power density compared to memory-to-memory stacking. Remaining unresolved, the thermal issue will act as a limiting factor on the number of device layers to be stacked, and in an extreme case, it can further result in malfunction even on two device layers.

1.2 Thermal Challenges and Designs

First, we evaluate the temperature variations of four-devices stacked IC from the international technology roadmap for semiconductors from 2002 [9]. Average temperature at each device layer from bottom to top is measured as 30 °C, 100 °C, 135 K and 150 K. We can observe how temperature rises as the device layer goes up, farther from the air cooled heat sink. Increased temperature will not guarantee the functionalities of the upper devices and will limit the number of device layers to be stacked. Efficient vertical heat dissipation paths are sorely needed to fully utilize the benefits of 3D IC.

To solve the thermal problems of the 3D IC structure, there have been many research works on different aspects of the design. We can divide the cooling methodology in two main scopes: 1) on-chip level and 2) package level [10]. On-chip thermal design on an actual device layer is necessary to reduce the elevated heat generation of localized regions with high power density, also known as hotspots, down to an operational range in close proximity. In package level cooling techniques, air cooling at the heat sink, liquid cooling with various geometry heat exchangers [11] are being studied.

1.2.1 On-Chip Thermal Designs

Thermal-aware designs from the high-level system to the physical level implementations have been studied to alleviate the aggravated thermal issues while coping with existing chip designs. Dynamic thermal management techniques on 2D high-performance core designs or data centers include fetch throttling [12], task and thread scheduling [13], [14], [15], and dynamic voltage and frequency scaling [16]. These works can also be applied to 3D stacked designs to study the effect on the temperature profile. However, this approach often sacrifices performance to reduce the hotspots.

Contrary to the system-level techniques, physical design approaches have to consider a new factor for 3D IC packaging, the TSVs, which serve as electric connections through multiple device tiers [17]. Research works include thermal-aware placement for hotspot reduction [18], heat dissipation through TSV routing [19], thermal wires [20], dummy TSV insertion [21] and so on.

Previous research works on physical design approaches include the insertion of thermal TSV (TTSV) in reserved space depending on the density and

thermal dissipation effectiveness [22], heat pipe insertion to minimize the temperature gradient on the horizontal plane [23], thermal driven floorplanning [24] and placement [25]. TTSVs are electronically isolated from other components of the chip, which are inserted solely to act as vertical heat dissipating paths from each device layer to the heat sink. Numerous research works have planned to insert TTSVs on different physical design stages; these include partitioning [26], placement [22], floorplanning [27], routing [28], [20] and so on. From analytical studies to experimental results, the TSV manufacturing process is found to stress surrounding features on the chip; therefore the number of TSVs needs to be minimized for maximum process reliability. In our work, a new design of thermal vias with fin-like geometries is studied primarily for the usage in 3D ICs [29]. Our thermal-aware design structures are easily manufacturable, less stressful to neighboring devices and interconnects, more reliable and thermally effective. Furthermore, there is a high possibility to decrease the number of TTSVs inserted for similar or better heat dissipating effectiveness. The potential benefits of the design are higher yield, improved performance and commercialization of 3D IC devices.

1.2.2 Package Thermal Designs

The aforementioned works are mostly based on conductive heat transfer resolved in solids within chips. Conductive thermal management designs in combination with conventional air cooling based heat sinks are often insufficient to keep the chip in operational and reliable range for high performance applications [30]. The heat flux upper limit with air cooling methods for most applications is around $100\,\mathrm{W/cm^2}$. The 3D multi-chip modules that dissipate more than $300\,\mathrm{W/cm^2}$ at the die are beyond the capability of most conventional air cooling solutions [31]. Major heat transfer blockages in 3D IC, that create localized, trapped heat, or hotspots, result mainly from the bonding layer between the device stacks. The bonding layer is composed of very low thermally conductive ILD to isolate the unnecessary electric connections between device tiers. Hence, it is crucial to introduce additional cooling mechanism for thermally isolated device layers that are distant from the heat sinks.

Due to the scale limitation of on-chip thermal solutions, package level

designs are considered to possess greater potential for 3D IC applications. Engineers have been exploring more effective ways of cooling by pumping liquid coolants directly onto the chips, rather than circulating air around them or using backside cold plating. The inter-tier liquid cooling micrometer-scale channel, or microchannel, illustrated in Figure 1.2, layer has been gaining attention as an integrated cooling mechanism to tackle thermal degradation in 3D ICs [32], [33]. The use of liquid coolant, commonly water, has become an attractive option due to higher convective heat transfer coefficient compared to air cooling. The heat transfer coefficient of water h_{water} = 50-3000 W/m^2-K is higher than air h_{air} = 0.5-1000 W/m^2-K for natural convection, and becomes even more effective in forced convection, h_{water} = 50-10 000 W/m^2-K versus h_{air} = 10-1000 W/m^2-K. A single-phase loop in the liquid cooling system consists of a miniaturized pump and heat exchanger (e.g. cold plate or microchannels). Conventional board-level liquid cooling heat exchangers are not suitable for chip-level implementations due to bulky modules. Therefore, there has been interest in compact microchannel heat exchangers that could directly be etched on the back of the silicon dies [34], [35].

The majority of the research on microchannel design optimizations is based on runtime expensive numerical simulations, oversimplified thermo-fluidic models or correlations with incorrect assumptions. Numerical models are typically unsuitable for optimization considering intensive computing. Ap-

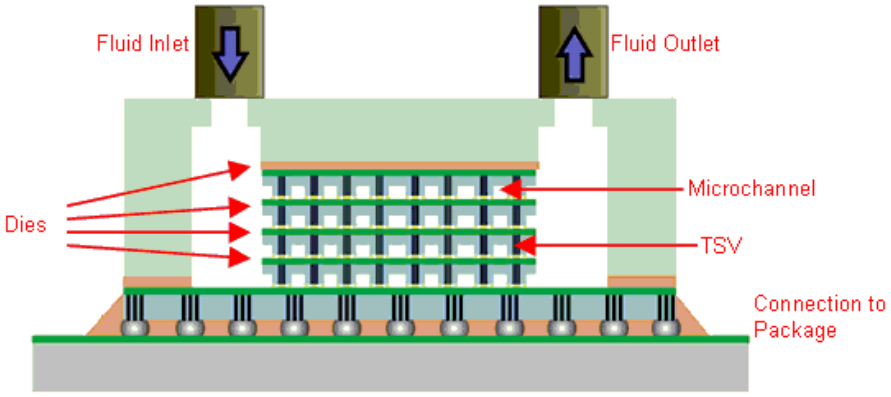


Figure 1.2: Liquid-cooling microchannel scheme on 3D IC packaging [36].

proximate models or correlations with improper assumptions pose a fundamental limitation to accurately derive the relationships between the channel parameters and the thermal performance. Applying a fully developed flow model on a short channel that presents developing flow will cause large discrepancy. In microchannel optimization, inaccuracy on the base channel model will significantly affect the optimality and quality of the resulting design.

1.3 Dissertation Organization

The remainder of this dissertation is organized as follows.

Chapter 2 presents our proposed thermal design of thermal via-fin structure [29]. We study the design criteria for thermal fin to be effective in thermal performance and analyze the improvements for various designs. Thermal via cluster design with and without the insertion of thermal fin is studied and proves the potential of minimizing the area with this new design component.

In Chapter 3, we derive accurate thermo-fluid correlations of the microchannel to capture the relationship between the channel physical parameters and the thermal performance [37]. The correlations are based on developing flow model to properly establish the parametric study at the entrance region of the channel. In microchannel design optimization, the flow behavior at the entrance region will be prolonged when microchannel dimensions vary across the flow direction. Therefore, correlations based on developing flow model will serve as a solid foundation for finding the optimal microchannel design. Tapered channel was chosen for the design flexibility in the microchannel optimization. To verify the accuracy of our model, we have made comparison with commonly used fully developed flow-based correlations and reliable numerical simulation.

Chapter 4 applies the same technique to derive the thermo-fluid correlations of diverging shape microchannels. Then, we merge the correlations to fully analyze any linear-walled channels with single correlation for each thermal performance and cooling power consumption. The resulting correlations provide the foundation for the microchannel design optimization.

In Chapter 5, we perform microchannel geometric optimization based on the derived tapered channel models [38]. The microchannel is divided into

small sections and optimized piecewise linearly at each section. An iterative simulated annealing optimization technique is applied for multi-section channels. Our model finds the channel inlet width and tapering angle to maximize the thermal performance subject to cooling energy and manufacturing constraints. This work determines the optimal tapering angle of the microchannel at each location.

Finally, we highlight the proposed works and summarize the impact in Chapter 6. Based on what we have observed, we propose potential future works. Thermo-fluid models can be improved in accuracy and flexibility by adding more design parameters and analyzing more complicated physical phenomena. In addition, microchannel design can be extended to non-straight channels, such as branching out in forks, merging multiple streams into single channel and so on. The multistream analysis will be helpful to design grid-like microchannel structures.

CHAPTER 2

THERMAL THROUGH-SILICON VIA WITH THERMAL FIN DESIGN

2.1 Introduction

Greater than 50 % of dynamic power consumption in current IC chips is contributed by interconnect networks; the lengths of which do not generally scale down with each technology node [39]. 3D IC, a novel packaging technology, is heavily studied to realize the improved performance with denser packaging and reduced wirelength. Despite numerous advantages, thermal management is the biggest bottleneck to realize the device-stacking technology.

In this chapter, we propose a thermal-aware physical design for 3D IC [29]. We aim to mitigate localized hotspots to ensure functionality by adding thermal fin geometry to existing thermal through-silicon via (TTSV). We analyze various ways to insert thermal fin for single TTSV as well as TTSV cluster designs with the goal of maximizing heat dissipation while minimizing the interference with routing and area consumption. A global analysis of a 3D system is developed and a thermal resistance circuit is built for an accurate and runtime-efficient thermal analysis of a complete 3D IC.

We design thermal vias with laterally elongated fins in the device layer to minimize the maximum temperature of the chip as in Figure 2.1 and also decrease the number of TTSVs to improve the reliability. This structure not only eases the manufacturing but also simplifies the routing strategies. In addition, we use the advantage of reserved space for the TTSV cluster region placed in close proximity to hotspots to insert fins. Finite element method (FEM) simulations and analytical models are shown to verify the presented geometries.

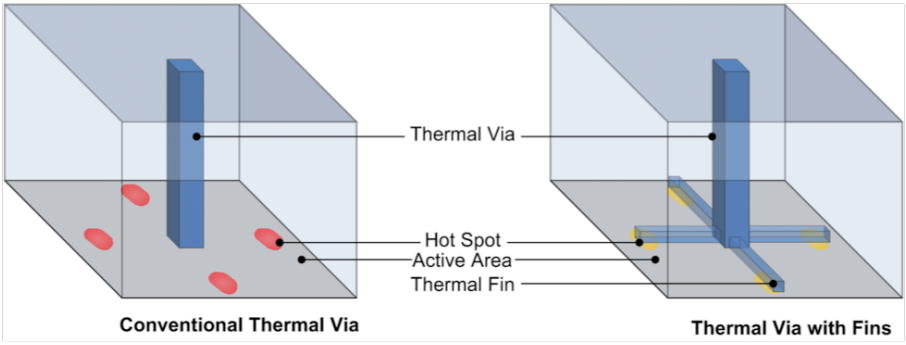


Figure 2.1: 3D view of thermal via-fin structure.

2.2 Analytical Model

2.2.1 Thermal Fin Geometry

To successfully dissipate heat from hotspots on a chip to guarantee the proper functionality, bundles of TTSVs are typically deployed. In our design, we will take advantage of the space between TTSVs inside the TTSV cluster region to insert additional thermally conductive fin geometry extending from interior TTSVs to the boundary. By utilizing the space in between the TTSVs, no extra space is consumed. The fins can be placed in the whitespace between the TTSVs in close proximity to the hotspots which construct heat dissipating paths to maximize their effectiveness. In addition, they do not penetrate the ILD layer, where the metal interconnects lie, hence the adverse effects to the interconnect routing are minimal.

Heat flux to TTSV is inversely proportional to the distance from hotspots. Moreover, within the via cluster, TTSVs closer to the hotspot might act as lateral heat blockage to further TTSVs [40]. Thermal fin structure enables TTSVs outside the efficient heat dissipation region to be more effective as heat conduits.

However, there is a requirement for the fin structures to be more effective in heat transfer than conventional structure without fins. Figure 2.2 illustrates simple top view of two TTSVs and a single thermal fin extending towards the hotspot from further TTSV, labeled $TTSV_2$. There can be two major heat dissipation paths through $TTSV_2$ from the hotspot, heat flux through

thermal fin denoted as Q_1" and the other path through $TTSV_1$ to $TTSV_2$ represented as Q_2". The heat flux Q_1" has to be greater than Q_2" in order for the thermal fin to be more effective than the TTSV without fin structure.

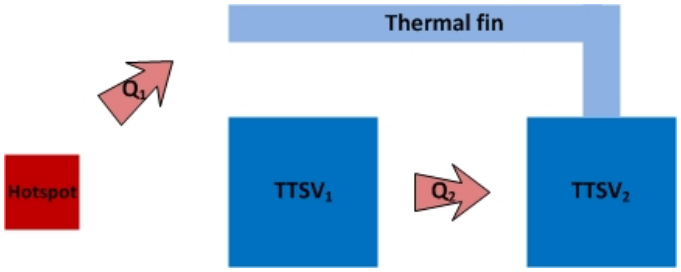


Figure 2.2: TTSV and thermal fin with two heat paths (top view).

From Figure 2.2, we set three assumptions for simplicity:

- Length of the thermal fin can be assumed as $L_{fin} \approx \frac{3}{2} w_{via} + d_{via}$, where w_{via} is the width of the thermal via (TTSV) and d_{via} is the distance between the vias.
- Minimum pitch between the fin and nearest TTSV is assumed to be the same as TTSV pitch, $d_p. \approx d_{via}$
- Temperature is horizontally isothermal in two-dimensional TTSV plane; temperature difference in the horizontal surface area is not considered in the resistive model.

Integrating the assumptions listed above, we can find the appropriate condition for the thermal fin to be effective for heat dissipation using the terms specified in the Table 2.1.

Table 2.1: Symbols in the Analytical Model

Symbols	Description
A_i	cross-sectional area of structure (i.e. via, fin, hotspot)
k_i	thermal conductivity of the material (i.e. ILD, copper)
w_i	width of the geometry
t_i	thickness of the geometry
d_i	distance between any neighboring structures (i.e. via-to-via, fin-to-via)

As a result, the cross-sectional area necessary for the fin to be an effective thermal conduit is derived as below,

Theorem: Cross-sectional area A_{fin} of the effective thermal fin should be,

$$A_{fin} > \frac{A_{via}A_{HS}(k_{ILD}(L_{fin}+d_{via})+k_{cu}\sqrt{d_{HS}^2+d_{via}^2})}{k_{cu}(d_{via}A_{HS}+d_{HS}A_{via})} \tag{2.1}$$

$$A_i = w_i t_i \qquad \textit{for i=fin, via, hotspot(HS)}$$

2.2.2 Heat Transfer Model of ILD

Thermal management is key to the success of a given multi-chip design. Our proposed thermal-aware structural design is based on the assumption that additional TTSVs are inserted to prevent thermal exacerbation. For comprehensive understanding of the design, a modified analytical heat transfer model of the design is necessary. Heat is dissipated mainly through a high thermally conductive substrate in 2D IC design, which is vertical direction (one-directional heat flow); however, in 3D IC, active layers are embedded in the ILD regions [41] such that the ILD thermal resistance should be considered as well. Low-k materials are widely adopted as new ILDs, and this porous material has an even lower thermal conductivity than silicon dioxide, SiO_2. Im et al. [42] listed the thermal conductivity of ILD $k_{ILD} = 0.3\,\mathrm{W/m\text{-}K}$. As Figure 2.3 shows, by assuming metal wire with width w and length L, aligned with each other with the pitch p, the volume fraction of the wire f_{wire} will be $f_{wire} \approx w/p$ and the volume fraction of the via f_{via} will be $f_{via} = f_{wire} * w/L$. The effective thermal conductivity will be $k_{i,eff} = f_i k_m + (1-f_i)k_{ILD}$, where f_i will be either f_{via} or f_{wire} on each layer i, and k_m is the thermal conductivity of the interconnect metal, which is usually $k_{cu} = 401\,\mathrm{W/m\text{-}K}$ for copper, Cu. The equivalent thermal resistance $R_{th,eq}$ will be

$$\begin{aligned} R_{th,eq,ILD} &= R_{th,eq,via} + R_{th,eq,wire} \\ &= \sum \frac{t_{via}}{k_{i,eff,via}} + \sum \frac{t_{wire}}{k_{i,eff,wire}} \end{aligned} \tag{2.2}$$

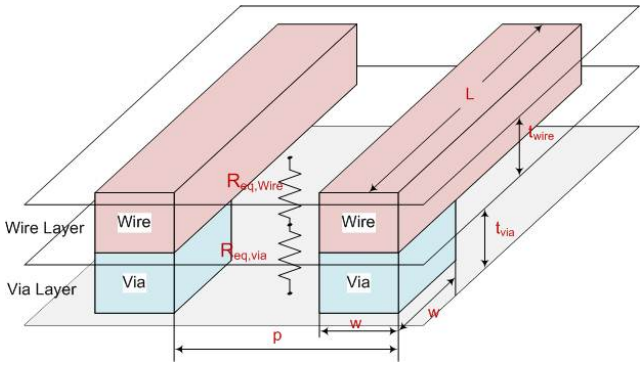


Figure 2.3: TSV and wire layers with the lumped thermal resistance model.

2.2.3 3D Thermal Resistance Circuits

There are some similarities between the electric circuit model and heat transfer equations [43]. Hotspot where heat is generated is modeled as the current source and the thermal resistance is similar to the electric resistance. Temperature on each position is analogous to the voltage and ambient temperature is represented as ground in the circuit (sometimes, it can also be represented as the DC voltage source). We developed an analytical 3D resistive network heat transfer model as shown in Figure 2.4, to be able to simulate our proposed design as well as conventional TTSV structures. Our thermal design has lateral structures on each device tier and 3D heat flow should be considered in the model; 2D heat flow is analyzed on the horizontal device plane. The 3D analytical model will provide more accurate understanding compared to the previous analytical models which only consider one-dimensional heat flow on the device plane [44]. Furthermore, the simulation can be extended to larger benchmark applications with reduced runtime as compared to the commercially available FEM tools or commonly used finite difference method.

Similar to Section 2.2.2, each thermal resistance between the nodes (geometries) of the circuit is expressed with the dimension parameters, characteristics of the structure, $R_{th} = t/(kA)$, where t is the thickness, k is the thermal conductivity and A is the cross-sectional area of the structure.

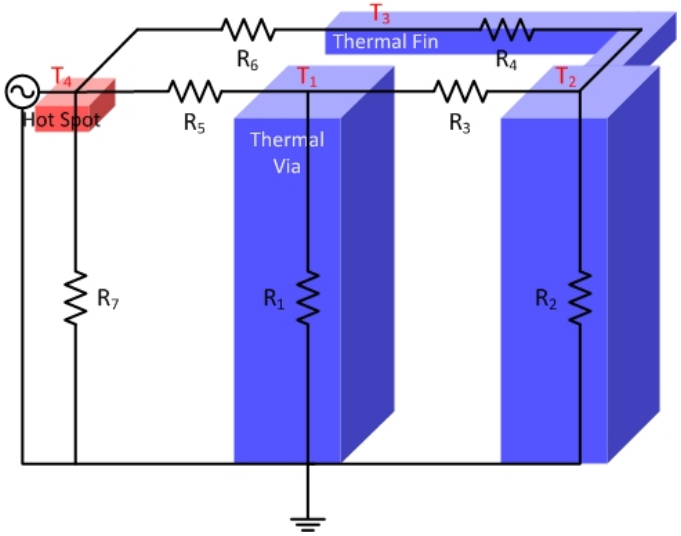


Figure 2.4: Three-dimensional thermal resistance model for TTSV-Fin structure.

$$
\begin{aligned}
R_{th,1} &= R_{th,2} = \frac{t_{via}}{k_{cu} w_{via}^2} \\
R_{th,3} &= \frac{d_{via}}{k_{ILD} w_{via} t_{via}} \\
R_{th,4} &= \frac{L_{fin} + d_p}{k_{cu} w_{fin} t_{fin}} \\
R_{th,5} &= \frac{d_{HS}}{k_{ILD} w_{HS} t_{HS}} \\
R_{th,6} &= \frac{\sqrt{d_{HS}^2 + d_p^2}}{k_{ILD} w_{fin} t_{fin}} \\
R_{th,7} &= \frac{t_{via} - t_{HS}}{k_{ILD} w_{HS}^2}
\end{aligned}
\tag{2.3}
$$

In the resistive model, heat generating sources are modeled as current sources and temperature is analogous to the voltage at each node of the circuit. Thermal resistances are expressed as regular resistors and heat transfer in Equation (2.4), $R_{th} = \triangle T/Q$ is expressed similarly to Ohm's law, $R = V/I$. Setting the resistance equations of the given circuit is done based on Kirchhoff's current law. Note that Q is heat rate, which equals to the product of the heat flux and the area, $Q = Q"A$.

$$R_{th}Q = \triangle T \tag{2.4}$$

$$\begin{aligned}
\frac{T_4 - T_1}{R_{th,5}} - \frac{T_1 - T_2}{R_{th,3}} - \frac{T_1}{R_{th,1}} &= 0 \\
\frac{T_1 - T_2}{R_{th,3}} + \frac{T_3 - T_2}{R_{th,4}} - \frac{T_2}{R_{th,2}} &= 0 \\
\frac{T_4 - T_3}{R_{th,6}} - \frac{T_3 - T_2}{R_{th,4}} &= 0 \\
Q - \frac{T_4 - T_3}{R_{th,6}} - \frac{T_4 - T_1}{R_{th,5}} - \frac{T_4}{R_{th,7}} &= 0
\end{aligned} \tag{2.5}$$

Table 2.2 lists the parameter values that can be applied into this TTSV and fin structure. These parameters also fulfill the requirement for the effective thermal fin in Equation (2.1).

Table 2.2: TTSV, Thermal Fin Structure Parameters

Parameters	Values	Parameters	Values
t_{fin}	5 µm	t_{HS}	2 µm
w_{fin}	5 µm	w_{HS}	10 µm
t_{via}	100 µm	d_{via}	5 µm
w_{via}	20 µm	d_{HS}	50 µm
k_{ILD}	1.4 W/m-K	k_{cu}	401 W/m-K

2.3 Experimental Results

2.3.1 2D Simulation

Steady-state thermal FEM simulations using ANSYS Workbench are used to verify the analytical results. The first set of the simulations model is the 2D heat spreading through the active region with a thin-film silicon layer (0.1 µm thickness) on top of a silicon dioxide layer (0.9 µm thickness), a copper via with fin (1 µm thickness), as shown in Figure 2.5. The copper via is fixed

at a temperature of 30 °C, a 100 µm^2 hotspot with a heat flux of 500 W/cm^2 is placed in the thin-film silicon region, and all other surfaces are adiabatic. The temperature distribution of the 2D model is shown in Figure 2.6. FEM results confirm that thermal fins reduce the maximum temperature of the hotspot (Figure 2.6-a $\sim$ 2.6-f), as compared to the geometry without a thermal fin (Figure 2.6-g). As predicted, hotspot placement is crucial; ideally, the hotspot should be adjacent to the fin, and the effective fin length should be less than 50 µm. A wider fin width (10 µm in Figure 2.6-d vs. 4 µm in Figure 2.6-e) is more effective, but comes at a tradeoff of additional chip area.

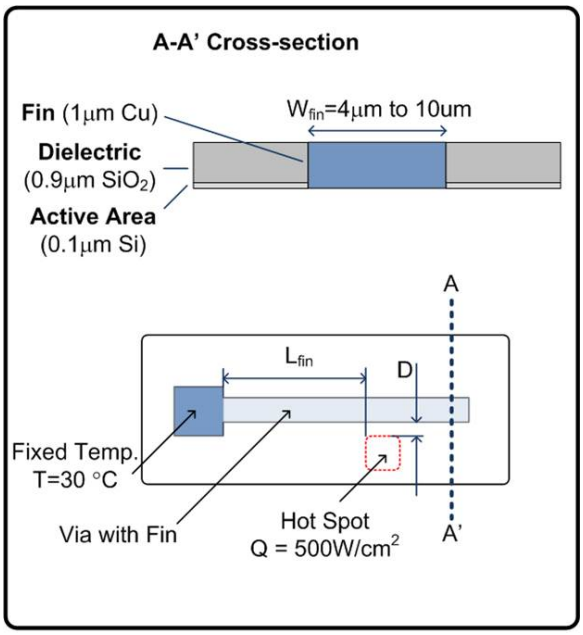


Figure 2.5: Two-dimensional simulation model.

2.3.2 3D Simulation on Thermal Via Cluster

One study has shown that TTSVs can also act as lateral heat blockage to the vias further from the hotspot [40]. For heat to be dissipated from the hotspot, the distance between TTSV and the hotspot affects the amount of total heat dissipation. In 3D simulation, the locations of the hotspot for all models were fixed but we varied the number of TTSVs in the cluster

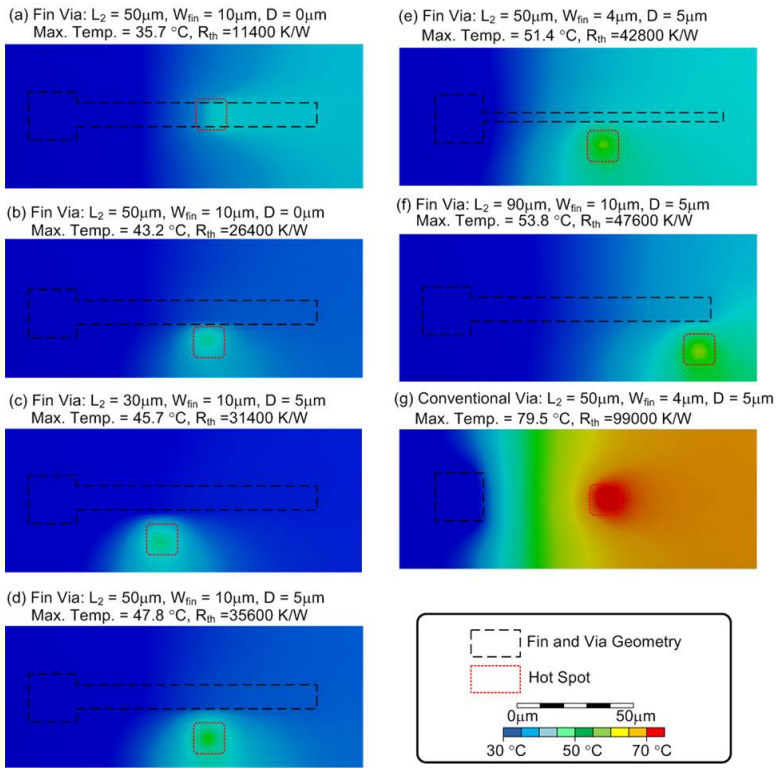


Figure 2.6: Two-dimensional simulation of TTSV and fin.

for the difference in the distance between the closest via and the hotspot. In addition, the largest area via cluster example is compared with full via insertion and selective elimination of inner TTSVs. The simulation result shows that overall reduction in maximum temperature depends heavily on the distance and the number of vias inserted (which also can be interpreted as the size of the cluster). Furthermore, although more vias are inserted inside the cluster, inner TTSVs are not as effective as the closer vias on the boundary of the thermal via cluster. The simulation results are shown in Figure 2.7 and Table 2.3.

2.3.3 Fin Stretched Inside TSV Cluster

From the analytical studies, the dimension of the fin is a key parameter in heat dissipation efficiency. Both width and depth of the fin structure will affect the performance, but in this work, we will fix the depth of the fin

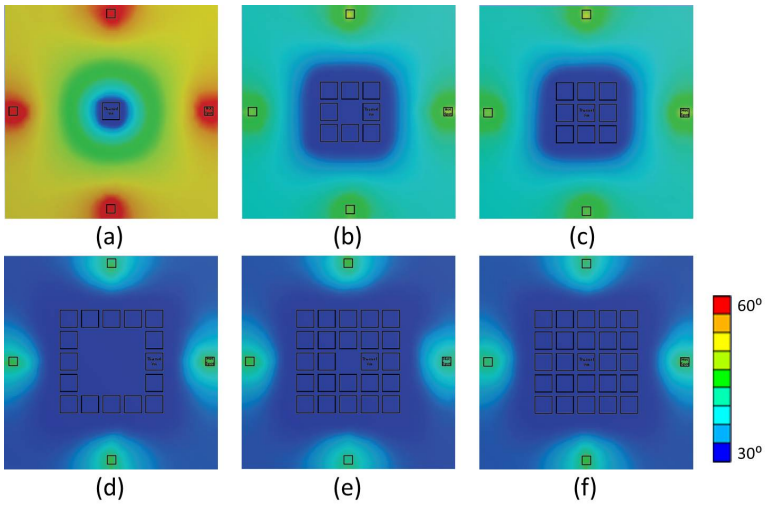


Figure 2.7: FEM simulation on different number of TTSVs (minimum distance to the hotspot: 50 µm, TTSV width: 20 µm, hotspot width: 10 µm) (a) Single TTSV, (b) 8 TTSVs, (c) 9 TTSVs, (d) 16 TTSVs, (e) 24 TTSVs, (f) 25 TTSVs.

Table 2.3: Simulation Result of TTSV Cluster Model

# of TTSVs	1	8	9	16	24	25
T_{max}[°C]	59.61	46.95	47.24	41.85	41.44	42.11
$Improvement$[%]	Ref.	42.76	41.77	59.98	61.36	59.10

and mainly focus on the width variance. There will be a trade-off with the area consumption on the device surface and the enhanced heat dissipation from the fin width widening. To optimize for both fin width and thermal performance, Figure 2.8 shows the simulation result of four via clusters with the fin extended from further vias varying in width from 0.5 µm to 3 µm. The other parameters for the structures are $w_{via} = 10\,\mu m$, $d_{via} = 20\,\mu m$, $A_{HS} = 300\,\mu m^2$, $d_{HS} = 5\,\mu m$.

The effect of the fin structure is simulated on the simplest model under the conditions described in previous sections. Figure 2.9 shows the comparison between single via and two vias structures and with or without the fin structure by varying the distance of the hotspot. In the single via case,

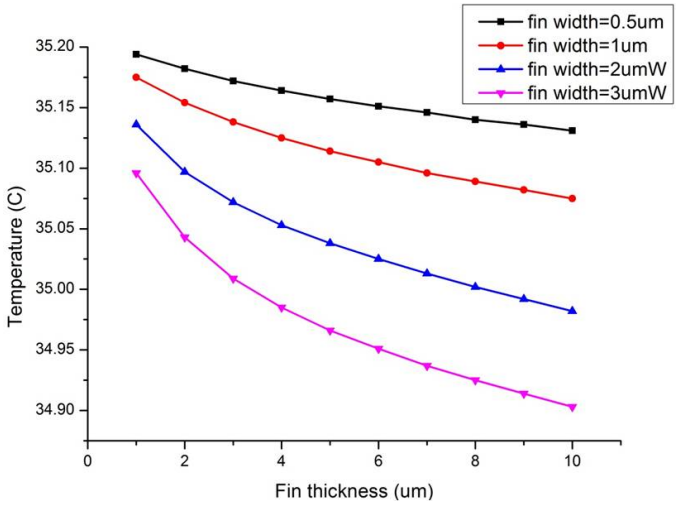


Figure 2.8: Simulation results of thermal fin width variation.

the distance between the hotspot and the TTSV via was reduced by adding the fin structure stretching toward the hotspot. However, for multiple vias, the fin was extended until it meets the boundary of the TTSV cluster. In Figure 2.9, we have fitted the curve for the data points we have collected. Based on Fourier's law, $\triangle T = T_{HS} - T_{via} = Qd/(kA)$, k and Q are constant values but area A is the function of the distance d as the heat diffusion path is no longer linear as the distance increases. For simplicity, assume that A is a second-order polynomial function of d. Hence, the temperature was inversely proportional to the distance and the coefficient and intercept values were obtained accordingly.

The fin structure helps to construct an efficient heat dissipation path toward the hotspot from farther TTSVs. By inserting fin structures, the heat flowing through the fin path can exceed the heat flux through the closer via. Figure 2.10 illustrates the comparison between three, six and nine vias with and without fin structure from a 3 x 3 square via cluster. Three vias are the closest column of the cluster, six vias are two closer columns and nine vias are the whole via cluster. We can observe from the simulation result that the temperature difference between six and nine vias is almost negligible compared to three vias. The result can be interpreted to mean that the last farthest column was not contributing at all. To efficiently utilize the last col-

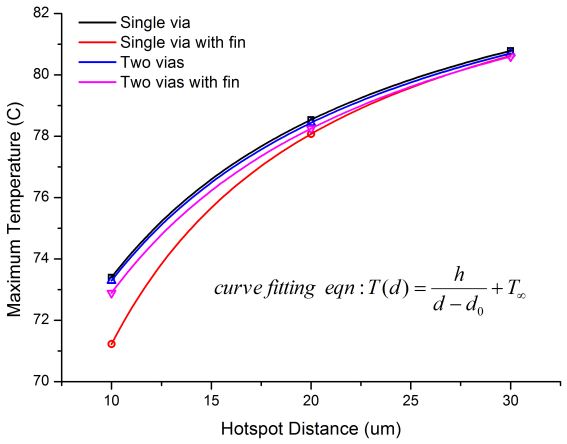
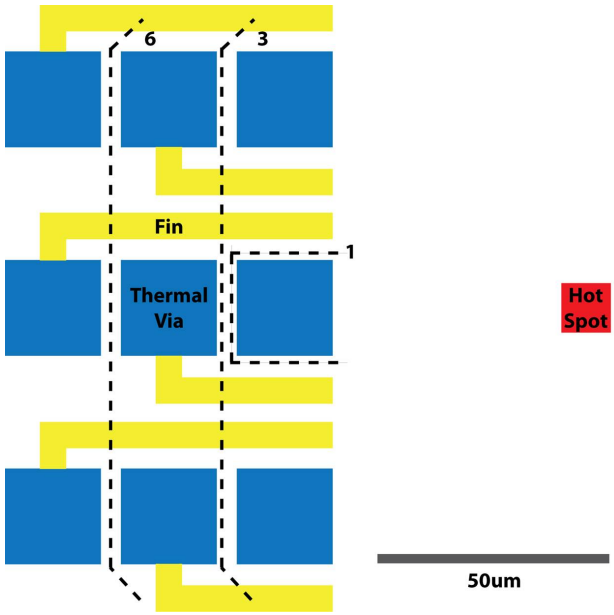


Figure 2.9: FEM simulations on single TTSV, two TTSVs with and without fin.

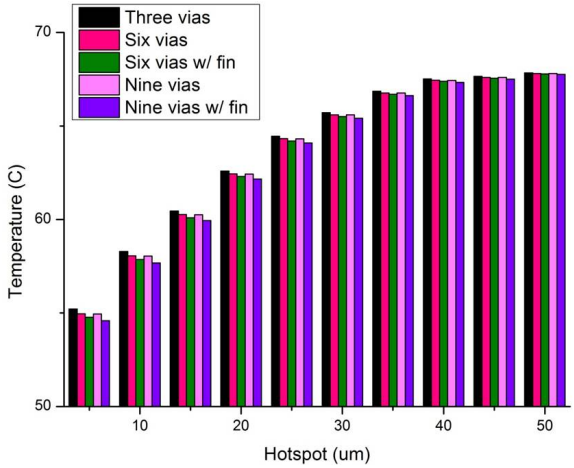
umn, thermal fins are inserted. There is approximately 2.5 % improvement in temperature distribution for the 5 µm away hotspot with $w_{fin} = 1\,\mu m$, $t_{fin} = 2\,\mu m$, $A_{HS} = 900\,\mu m^2$, and $w_{via} = 10\,\mu m$. We can also observe that six vias with fin is lower in temperature compared to the nine vias without the fin. This result shows the potential in decreasing the number of TTSVs inserted for similar or even better thermal performance. It allows less area consumption as well as lower stress to the neighboring devices. However, the effect is diminished as the hotspot is farther away. We can conclude that with the fins inserted inside the cluster, the effect is maximized as the cluster is closer to the hotspot. Table 2.4 shows the maximum temperature values and the percentage improvement of each structure with respect to single via structure.

Table 2.4: Simulation Result of TTSV and Thermal Fin Cluster Model

# of TTSV+Fin	1	3	6	6+Fin	9	9+Fin
T_{max}[°C]	58.985	55.218	54.961	54.776	54.951	54.587
$Improvement$[%]	Ref.	12.996	13.883	14.521	13.917	15.173



(a) Nine TTSV-thermal fin model (red: hotspot, blue: TTSV, yellow: thermal fin).



(b) Simulation results of TTSV cluster model with hotspot distance variation.

Figure 2.10: TTSV cluster model and simulation results.

2.4 Conclusion

Analytical and FEM models show that a conventional TTSV design is effective only when the hotspot is near the TTSV. A via with fin-like geometries adds flexibility to the design such that hotspots farther away from the TTSV can be cooled effectively without additional fabrication or routing constraints.

This work presents a new design of TTSV with fin-like geometries to enhance cooling in 3D ICs. Fin-like geometries reduce the number of TTSVs needed for 3D IC cooling, which relaxes the fabrication and routing constraints on the design. The distance of the hotspot from the fin was found to play a crucial role in the combined equivalent thermal resistance. The usage of fins is recommended if the hotspot can be reached from the via in less than 10 µm. Otherwise, additional complexity in manufacturing processes and stricter routing constraints due to the extra fins will outweigh the small efficiency gains. New structures and designs of TTSVs to reduce the thermal management issues in 3D ICs were found to merit further exploration.

CHAPTER 3

ACCURATE MODELS FOR TAPERED MICROCHANNEL HEAT SINKS

3.1 Introduction

The majority of existing thermal-aware designs on 3D ICs are based on conductive heat transfer resolved in solids within a chip. Conductive thermal management designs only in combination with conventional air cooling based heat sinks are often insufficient to keep the chip in operational and reliable temperature range for high-performance applications [30]. The upper limit of the heat flux with air cooling methods for most applications is around $Q" = 100\,\mathrm{W/cm^2}$. 3D multi-chip modules that dissipate more than $Q" = 300\,\mathrm{W/cm^2}$ at the die are beyond the capability of most conventional air cooling solutions [31]. In addition to the fact that heat sink is attached to only one of the device layers, major heat transfer blockages in 3D IC that create localized, trapped heat, or hotspots, result mainly from the bonding layer between the device stacks. Bonding layer is composed with very low thermally conductive ILD to isolate the unnecessary electric connections between device tiers. Hence, it is crucial to introduce an additional cooling mechanism for thermally isolated device layers that are distant from the heat sinks.

Packaging level designs can introduce larger scale solutions for effective performance. The use of liquid coolant has become an attractive option due to higher convective heat transfer coefficient compared to the traditional air cooling method. By pumping the liquid coolant directly onto the chips, we can achieve a higher heat transfer rate. Compact microchannel heat exchangers that could directly be etched on the back of the silicon dies [34], [35] are studied which also have the benefit of being placed between the device layers. Hence, the inter-tier liquid cooling microchannel layer has been gaining attention as an integrated cooling mechanism to tackle thermal

degradation in 3D ICs [32], [33].

Pumping power is the cost to pay for effective microchannels, often resulting in prohibitive expense. Designing microchannel with a well-balanced trade-off between thermal performance and the cooling power is important. Flow conditions as well as channel design will dominantly define the performance. To reduce the complexity and achieve more accurate relationship, we focus on channel design and leave the fluid condition in the future extension.

Traditional approaches to novel microchannel designs are usually inherited from the intuition of the engineer and verified through numerical simulations or empirical data. Then, some of the earlier optimization works were proposed, but they are either based on numerical simulations or oversimplified thermo-fluidic models. Numerical models are typically unsuitable for optimization considering intensive computing and long runtime. Approximate models or compact correlations used in the optimization are often based on improper assumptions and pose a fundamental limitation to accurately derive the relationships between the channel parameters and the thermal performance. For example, many of the previous works claim that fully developed flow models within microchannel have good agreement with the numerical solution and the corresponding experimental data [45]. However, applying a fully developed flow model to analyze short or arbitrary channels that presents developing flow characteristics will cause large discrepancy. Inaccuracy on the base channel model will significantly affect the optimality and quality of the resulting microchannel design.

In this chapter, we derive thermo-fluid correlations of the microchannel to accurately capture the relationship between the channel physical parameters and the thermo-fluid performance [37]. Thermal correlations are based on developing flow model to properly establish the parametric study at the entrance region of the channel as well as varying channel shapes. In the microchannel, the flow behavior at the entrance region will be prolonged when microchannel dimensions vary across the flow direction. Therefore, correlation based on developing flow model will serve as a solid foundation for finding the optimal microchannel design. Assuming the channel is symmetrical in length-wise axis, arbitrary shapes can be considered as piecewise linear channel; therefore, a tapered channel was chosen in our model. It provides more flexibility and accuracy than a rectangular channel with constant width. To verify the accuracy of our models, we have compared them with

commonly used fully developed flow based correlations and reliable numerical simulation.

3.2 Related Works

The concept of liquid cooling microchannel integrated to electronics was introduced by Tuckerman and Pease [11]. Kishimoto and Ohsaki [46] numerically simulated non-monotonic relationship of thermal resistance and channel width. They also fabricated board level via hole channels and tested the cooling performance. Working with popular 28-nanometer field-programmable gate array devices made by Altera Corporation, Sarvey et al. have demonstrated a monolithically cooled chip using microfluidic passages that could operate at temperatures more than 60 percent below those of similar air cooled chips with heat sink or cooling fans [47].

From the early 1990s until now, numerous studies on the heat transfer performance of various channel geometries have been of great interest. Hoopman [48] and Peng and Peterson [49] studied the influence of the geometry on heat transfer performance of rectangular microchannels and optimal geometry design under fixed height and total cross-section area. Harley and Bau [50] and Qu et al. [51] studied heat transfer of micrometer-scale rectangular and trapezoidal channels in silicon wafers. Rahman [52] investigated heat transfer performance of parallel and serpentine microchannels in silicon wafers. Lee et al. [53] studied heat transfer of various channel widths with constant aspect ratio and Foli et al. [54] explored optimal cross-section geometry based on constant cross-section area. Kuo et al. [55] assessed the effect of channel geometry on heat transfer for fully developed flow and found the optimal channel width decreased with increasing pumping power. Most of the designs studied and analyzed even with very unique and complicated cross-sectional shapes had a uniform shape and area along the fluid flow direction.

One of the challenges in single-phase liquid cooling is the increased thermal gradient due to absorbed sensible heat which leads to performance degradation. To achieve more uniform heat distribution, Sabry et al. [56] proposed to alter the channel width along the traveling direction of the fluid. Channel design in Sabry's work [56], [57] has a relatively wider inlet based on

fixed incoming coolant temperature and narrower outlet due to increased temperature from absorbed heat. This work assumes a piecewise constant channel and is based on rectangular channel approximate model for fully developed flow. All channels at the inlet start with the developing flow and there is a distinct difference in velocity and thermal profiles between developing and fully developed regions. Thus, applying a fully developed flow model to analyze a developing region is fundamentally incorrect. Especially for non-uniform channels, flow will be more perturbed and fluctuated, and likely to remain developing both hydrodynamically and thermally. Although it is reasonable to conclude that the tapered channel geometry contributes to thermal gradient reduction, it is uncertain whether the design is optimal when the microchannel design is optimized based on a fully developed flow model.

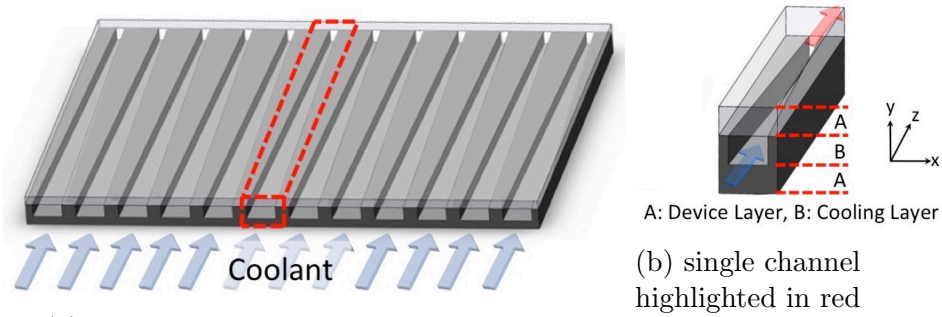
Hung and Yan [58] studied similar tapered channel but using finite volume based numerical analysis. The results provide insight into the performance with parameter variation. However, numerical approach is very compute-intensive and inappropriate for further optimization. Moreover, this model is based on a single-sided heat source, which is inapplicable for inter-tier cooling stacked between device layers in 3D IC. Thus, it is crucial to establish a compact model for fast microchannel design optimization that incorporates 3D IC applications.

In this work, we propose a compact and accurate closed-form model of the tapered channel for microchannel design optimization. The presented model is of fundamental importance in channel design study and can improve the accuracy with proper flow assumption and computation speed compared to the numerical approach in optimizing the design of various microchannels.

3.3 Fundamentals of Heat Transfer

Three-dimensional chips are composed of multiple vertically stacked device layers. To effectively dissipate heat from the device layers further to air cooled heat sinks, liquid cooling microchannel layers are fabricated in between the tiers. Figure 3.1 depicts a 3D view of two device tiers with a single microchannel layer.

In this section, we start by introducing the parameters of the tapered mi-



(a) cooling layer multiple tapered channel.

(b) single channel highlighted in red dashed box from (a).

Figure 3.1: 3D stacked device layers with inter-tier liquid cooling microchannel layer. Tapered channels are etched at the bottom of the device layer. Top device layer is presented transparent for clear cooling layer illustration. Note that figure is not to scale.

crochannel dimensions, followed by the metric used to determine the thermal efficiency of liquid cooling heat exchangers. Then, appropriate heat transfer models for tapered microchannel design and analysis are proposed and further improved with parameter fitting.

3.3.1 Microchannel Geometry

In heat and mass transfer community, various channel geometries, such as circular, triangular, rectangular, trapezoidal, and wavy channels, are modeled and simulated for the past few decades. Considering practical manufacturing simplicity and the cost, rectangular cross-sectional microchannel has been applied in electronic design implementations. To provide a solid base model of the channel geometry, a straight channel is considered in this work rather than a channel that bends or branches out. Applying a single channel model to multiple channels will be a straightforward expansion. Moreover, complicated structures such as grid, mesh or tree can be developed upon the base channel model but are outside the scope of this work.

An increased thermal gradient across a chip has been the rising challenge in liquid cooling designs. Tapering channel with a large inlet and a small outlet has been proposed to reduce the temperature gradient [56]. The top view of the tapered rectangular channel is portrayed in Figure 3.2.

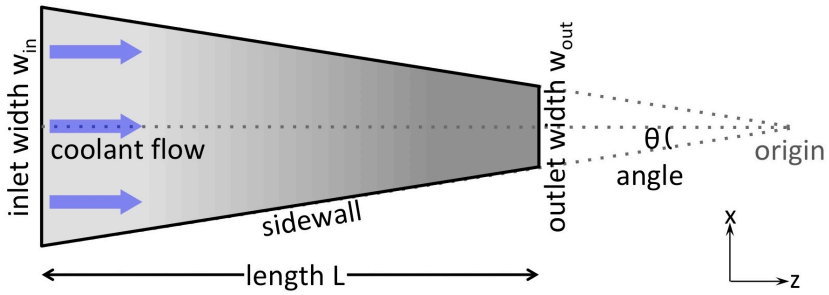


Figure 3.2: Tapered channel with inlet width w_{in}, outlet width w_{out}, length L, and half angle θ (top view).

Given the channel inlet width w_{in}, outlet width w_{out} and length L, the channel angle θ will be expressed as Equation (4.1). Opposed to a tapered channel, a channel with a uniform cross-section from inlet to outlet is denoted as uniform channel in the remaining of the work.

$$\theta = arctan\left(\frac{w_{in} - w_{out}}{2L}\right) \tag{3.1}$$

Sabry et al. [56] have proposed design-time technique to optimize channel width at a given location to minimize the thermal gradient using channel width modulation. Given uniform heat flux across the chip, the optimized channel design has nearly a linear-tapered rectangular channel. The top view of a single channel is a rough trapezoid.

3.3.2 Thermal Resistance

Within the microchannel cooling systems, conduction and convection are primary modes of heat transfer. To evaluate the thermal effectiveness of the design, thermal resistance is considered. Objectives for most of the thermal optimization are based on the temperature. However, there hardly exists an analytical closed-form model of temperature for a given design. To replace the metric, we focus on the temperature gradient instead of the temperature. Overall temperature drop $\triangle T$ is the product of thermal resistance R_{th} and heat rate Q, $\triangle T = QR_{th}$. The compact closed-form relationship makes temperature gradient a good design metric. Total thermal resistance R_{th} is

the summation of resistance from conductive $R_{th,cond}$ and convective $R_{th,conv}$ heat transfer as Equation (3.2), and each term is dependent on the material property, physical dimensions as well as the hydrodynamic conditions in the fluid region. Heat transfers to all directions but more heat flows where there is higher temperature drop. In device layers, heat will mainly dissipate from hotspots to the inter-tier microchannel layer, y-axis direction. Equivalent thermal circuit will consist of pairs of series vertical conductive resistance and horizontal convective resistance connected in parallel along the channel length. Note that each thermal resistance is two-dimensional, but the overall thermal circuit becomes three-dimensional.

$$R_{th} = R_{th,cond} + R_{th,conv} = \frac{d}{kA_c} + \frac{1}{hA} \tag{3.2}$$

In IC design, we formulate the conductive resistance only in solid: silicon device layers and walls surrounding the microchannels where the majority of the conduction occurs. Conductive thermal resistance is defined by distance d, thermal conductivity k and the cross-sectional area in solid A. Convective thermal resistance is defined in the liquid region: microchannel layer. Convective thermal resistance is inversely proportional to the product of the convective coefficient h and wetted area A_{wet}. Overall $R_{th,conv}$ can be considered as parallel connections of each local cross-sectional convective thermal resistance $R_{th,conv,i}$ at location i as in Equation (3.3). In a tapered channel, both h and A_{wet} vary across the channel length and local values are represented as h_i and $A_{wet,i}$ respectively. For each section, $A_{wet,i}$ is computed with local perimeter p_i and the length segment dz. In a lumped model, average convective coefficient h_{avg} is the mean of the local convective coefficient h_i as in Equation (3.4). The total wetted area A_{wet} is the product of wetted perimeter p_{wet} and the channel length L. For each section, local perimeter is computed with local channel width w_i, channel height H and the length segment dz.

$$R_{th,conv} = \left(\int_i \frac{1}{R_{th,conv,i}} \right)^{-1} = \frac{1}{\sum_i h_i A_{wet,i}} = \frac{1}{\sum_i h_i p_{wet,i} dz} \tag{3.3}$$

$$h_{avg} = \frac{1}{L} \sum_i h_i dz \tag{3.4}$$

$$A_{wet} = P_{wet}L = \sum_i 2(w_i + H)dz \tag{3.5}$$

3.3.3 Convective Heat Transfer

Heat dissipated in liquid cooling microchannels is based on forced convection. Convective heat transfer coefficient h, one of the factors to determine $R_{th,conv}$, depends on numerous parameters, such as coolant properties, fluid velocity, and channel dimensions, and yet there does not exist any closed-form analytical model. Thus we rely on the empirical or numerical correlations. Similar to the overall thermal resistance, temperature difference is computed by the product of the heat rate Q and the convective thermal resistance $R_{th,conv}$. Using this relationship, we can derive h as in Equation (3.6),

$$h = \frac{1}{R_{th,conv} * A_{wet}} = \frac{Q}{(T_w - T_b) * A_{wet}} = \frac{Q"}{T_w - T_b} \tag{3.6}$$

where Q" is the heat flux, T_w is the channel wall temperature and T_b is the bulk fluid temperature.

The efficiency ratio of the convection to conduction in fluid is defined as Nusselt number, $Nu = hD_h/k$, where k is the thermal conductivity and D_h is the hydraulic diameter. Non-circular channels are often formulated into circular-shaped channels using hydraulic diameter and computed using equation $D_h = 4A/P_{wet}$. The Nusselt number is used to compare the values from correlations with numerical results. Here, h is derived from exising empirical and numerical Nusselt number correlations on various case studies using the Equation (3.7).

$$h = \frac{Nuk}{D_h} \tag{3.7}$$

Shah and London [59] have studied Nusselt number approximate model on various channel geometries. Six-digit accuracy polynomial approximate model on rectangular channel in terms of aspect ratio, AR, for fully developed flow is shown in Equation (3.8). This model is valid when is $AR \leq 1$, hence AR is computed by height to width or width to height interchangeably.

$$Nu = 8.235(1 - 2.0421AR + 3.0853AR^2 - 2.4765AR^3 + 1.0578AR^4 - 0.1861AR^5) \tag{3.8}$$

Many recent works on microchannel design and optimization have adopted this approximate model [56], [60]. However, depending on the flow assumption and the channel geometry, this model in Equation (3.8) cannot fully capture the phenomenon and becomes inapplicable for accurate optimizations. This model is based on rectangular channel with fully developed flow. Based on commonly used microchannel dimensions in circuits, fully developed flow is reached in multiple folds (e.g. 5x-30x) in rectangular channel and non-negligible portion preserves developing flow toward the entrance region. Fully developed region is defined where flow velocity profile and normalized temperature gradient profile remain unchanged along the flow direction. In a uniform channel, fully developed hydrodynamic flow will be reached after length $L_{fd,h} \approx 0.05Re * D_h$ and fully developed thermal flow will be reached after length $L_{fd,t} \approx 0.05Re * Pr * D_h$ for laminar flow ($Re < 2300$), where Re is Reynolds number and Pr is Prandtl number. For example, a uniform rectangular channel of width $w = 100\,\mu m$, height $H = 100\,\mu m$, inlet flow velocity $u = 1\,m/s$ with water at $300\,K$ as coolant, hydrodynamic and thermal entrance lengths will be $L_{fd,h} = 560\,\mu m$ and $L_{fd,t} = 3300\,\mu m$ respectively.

However, in a tapered channel, normalized velocity profile continuously changes in the flow direction based on mass conservation law and therefore, fully developed flow will not be reached. Figure 3.3 shows the velocity profile comparison between uniform channel and tapered channel. In addition, piecewise channel optimization will vary the channel dimensions at each segmented section. The fluid dynamics and heat transfer in channel with varying cross-sectional shape differ from those in the uniform channel as the flow cannot reach the developed condition. Non-constant channel geometry will contribute to flow alterations and extend the length to reach the fully developed flow.

The local Nusselt number, Nu_z, correlation for developing flow in the entrance region for circular and non-circular channel developed by Shah and London [61] is shown in Equation (3.9).

$$Nu_z \approx 0.517(fRe)^{1/3}(z^*)^{-1/3} \tag{3.9}$$

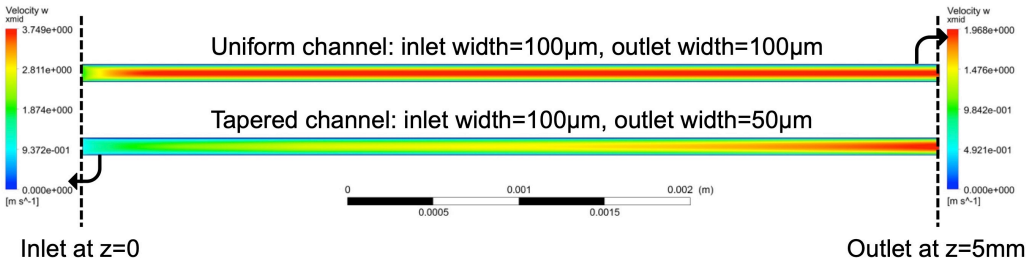


Figure 3.3: Velocity profile comparison of uniform channel and tapered channel at mid-plane in length-wise direction.

The Nusselt number is dependent on the Fanning friction factor f and position z. For simplification, some of the parameters are formulated into the variable z^*, where $z^* = z/(D_h * Re * Pr)$. In laminar flow, Fanning friction factor f is $16/Re$ which leads the term $f * Re$ constant as 16. This simplification is based on fully developed assumption, but we have verified that this exponent value has minimum effect in improving the accuracy through fitting, hence we have concluded this assumption is justified in our correlations. Pr is also a fixed constant for water at room temperature. As a result, the only remaining variables are D_h, Re and z.

3.4 Closed-Form Developing Flow Models

Figure 3.4 illustrates the procedure of the model derivation. To derive a closed-form model, we have first collected numerical simulation data of selected microchannel with various design parameters and extracted the values for the thermo-fluid performance analysis. Then, we have performed parameter fitting from the base model that we aim to improve the accuracy from. In our work, we have used the least-squares method in the parameter fitting. Finally, we have surface-fitted model parameters to create the correlations with the function of design variables. The surface fitting functions vary depending on the resulting function formula. This method is a commonly used approach and can be applied to other model derivations as well.

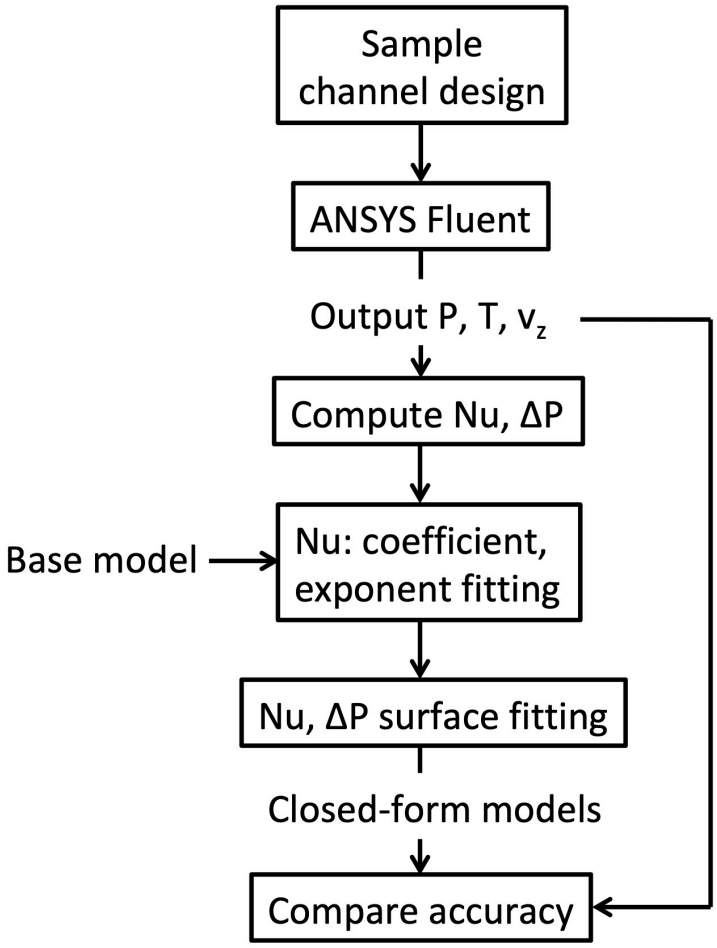


Figure 3.4: Flow chart of the model derivation.

3.4.1 Simulator

For numerical simulations, we used commercial computational fluid dynamics (CFD) solver, ANSYS Fluent v.18, in our experiments. The software uses the finite-volume method (FVM) with the support of the semi-implicit-method for pressure-linked-equations (SIMPLE) method. We applied rectilinear mesh with less than 0.1 maximum skewness, 0.1-0.5 million nodes depending on the channel size, 5 µm mesh element size and double precision simulation setting. The solutions converged within 100 iterations.

3.4.2 Parameters

Microchannel dimensions used in the experiment are shown in Table 3.1. Height and length of the channel are fixed to single values as they are mainly defined by the manufacturing technology and the chip footprint. Channel inlet and outlet widths are varied between the minimum and maximum range listed. The range is selected based on commonly used manufacturing dimensions listed in previous works [11], [56], [62], [63]. To ensure the converging tapered shape, channel outlet width is set less than or equal to the channel inlet width for each geometry. Tapering angle is computed using Equation (4.1). Table 3.2 lists the thermo-fluid conditions and the properties of materials used for the simulations. Water at room temperature is used as coolant and inlet flow velocity is set to 1 m/s. Adding fluid velocity into the optimization variable can be the future extension of this work.

First, we have compared the models of different flow conditions and analysis methods. Figure 3.5a compares four models: 1) Shah-London fully de-

Table 3.1: Microchannel Parameters

Definitions	Param.	Min	Max
Height	H	100 µm	
Length	L	0.5 mm	
Inlet width	w_{in}	100 µm	400 µm
Outlet width	w_{out}	10 µm	400 µm
Angle	θ	0°	19.8°

Table 3.2: Thermal and Fluid Properties

Definitions	Param.	Values
Silicon thermal conductivity	k_{si}	130 W/m-K
Water thermal conductivity at 300 K	k_{water}	0.613 W/m-K
Water kinematic viscosity	ν	1.004×10^{-6} m^2/s
Coolant inlet flow velocity	u	1 m/s
Coolant inlet temperature	T_{inlet}	300 K
Prandtl number for water at 300 K	Pr	5.83
Reynolds number	Re	99-159

veloped model for rectangular channel [59], 2) Sparrow-Starr fully developed model for tapered cylindrical channel [64], and 3) Shah-London developing flow model for general channel [61] compared with 4) FVM numerical simulation. Model comparison experimented on a single tapered channel with inlet width of 400 µm, outlet width 200 µm, length 500 µm with inlet flow velocity 1 m/s and heat flux 100 W/cm^2. Regardless of two different geometry approaches, rectangular versus tapered channel, both fully developed models showed large gaps between the local Nusselt number values as well as the Nusselt number gradients along the channel to the FVM result. On the contrary, developing flow model for circular and non-circular channels has a reasonably well-matching curve to the FVM result.

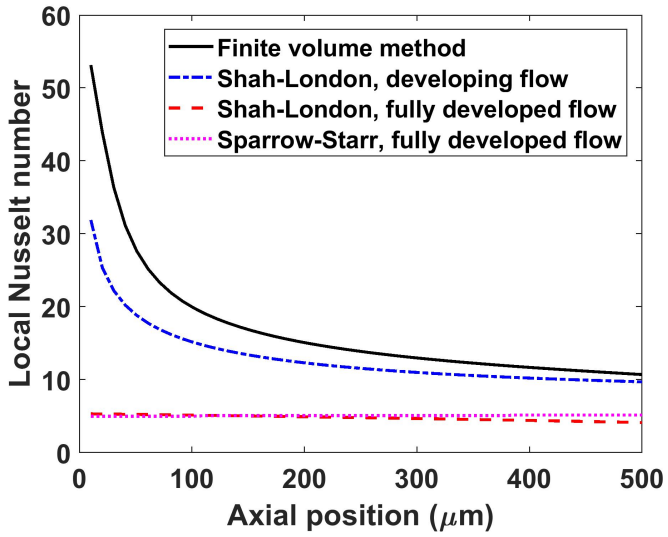
3.4.3 Constant Inlet Velocity

Nusselt Number

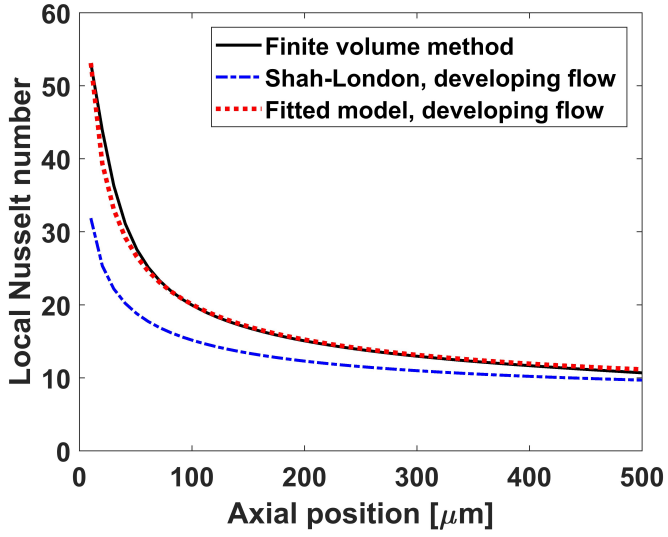
It is a widely used approach to derive a close-fitting Nusselt number or convective coefficient correlation from empirical data [65]. In this work, the model is built from numerical simulation data instead of the physical experimental results. Based on the Shah-London developing flow model with fixed constants for coefficient and exponents, we have further improved the model by fitting these parameters: 1) coefficient, denoted as α, and 2) exponent, denoted as β, in Equation (3.10) to the numerical results. Exponent of fRe remains unchanged as the term is constant in laminar flow.

$$Nu_{z,fitted} \approx \alpha(f \cdot Re)^{1/3}(z^*)^{\beta} \tag{3.10}$$

We have simulated 15 channel sizes: combination of three inlet widths and five tapering angles for each channel width. Flow velocity and heat flux are fixed to a single value for in-depth study of the channel geometry dimensions in our model. These values can also be varied to induce more comprehensive correlations, but this is beyond the scope of this work. Each (α, β) value pair is determined by the least squares method for all datasets. Figure 3.5b exhibits the improvement of our fitted correlation from Shah-London general channel developing flow model, matching closer to the FVM result on the same tapered channel used in Figure 3.5a.



(a) Numerical simulation, fully developed and developing flow correlations comparison.



(b) Numerical simulation, general channel developing flow and fitted developing flow model comparison.

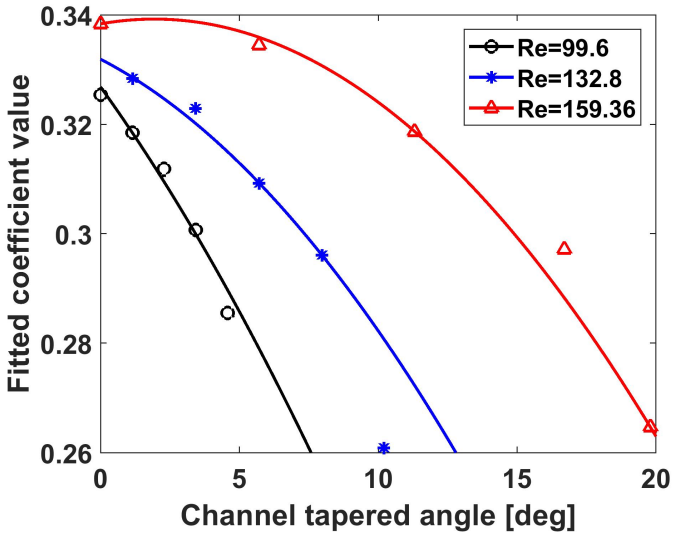
Figure 3.5: Local Nusselt number comparisons on tapered channel with inlet width 400 µm, outlet width 200 µm, length 500 µm, inlet flow velocity 1 m/s, heat flux 100 W/cm^2.

Next, fitted (α, β) pair values for selected channel geometries are extended to derive the 3D correlations of the parameters as a function of two variables: 1) tapered angle θ and 2) Reynolds number Re, using polynomial least squares surface fit. The Reynolds number is a representative indicator of the flow condition, defined by volumetric flow rate $\dot{V}$, hydraulic diameter D_h and kinematic viscosity ν, $Re = \dot{V}D_h/\nu = uAD_h/\nu$. Volumetric flow rate $\dot{V}$ is expanded to the product of flow velocity u and cross-sectional area A. We fixed flow velocity and channel height, thus inlet width is the only variable for determining the Reynolds number. Therefore, equivalently, fitting parameters can be expressed as a function of channel tapering angle θ and the inlet width w_{in}. The 3D correlations were within 95 % accuracy compared to the individually fitted parameters of each geometry. Then, we have determined the function of the surface fitting. In the case of the local Nusselt number, polynomial-22 function formula was used. Finally, we have 3D fitted the model parameters in terms of microchannel design variables using least absolute residuals method. The fitting algorithm applied depends on the target function formula and can be altered for the highest accuracy. The results of the 3D surface fitted curves for coefficient and exponent value are illustrated in the Figure 3.6a and 3.6b respectively. The resulting correlations for α and β in terms of θ and Re are shown in Equations (3.11) and (3.12). These fitted functions are combined to the Equation (3.10) to compute the convective coefficient in developing flow for tapered rectangular channel.

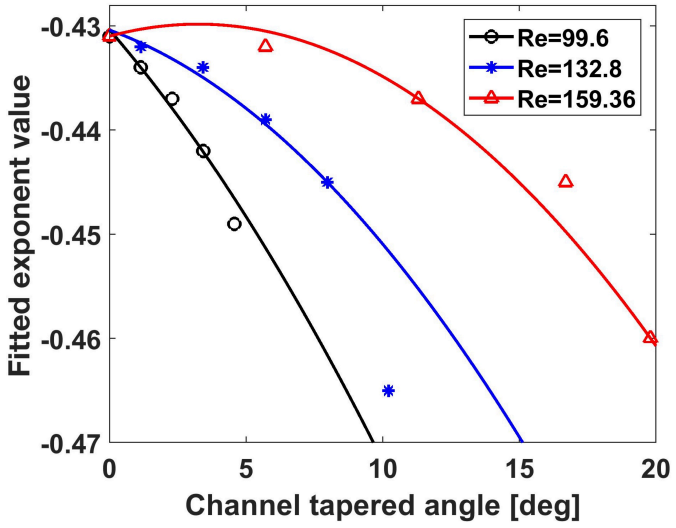
$$\begin{aligned}\alpha(\theta, Re) = {} & 0.3317 - 0.02029\theta - 0.0001991Re \\ & - 0.0002337\theta^2 + 0.000133\theta Re + 1.513 * 10^{-6} Re^2\end{aligned} \tag{3.11}$$

$$\begin{aligned}\beta(\theta, Re) = {} & -0.435 - 0.009296\theta + 8.235 * 10^{-5} Re \\ & - 0.0001101\theta^2 + 6.282 * 10^{-5}\theta Re - 3.586 * 10^{-7} Re^2\end{aligned} \tag{3.12}$$

For qualitative and quantitative analysis between the models, mean error values on the local Nusselt number for simulated set of channels are compared in Figure 3.7. Each model is compared with respect to FVM. Average error percentage of Shah-London and Sparrow-Starr fully developed correlations are 62 % and 72 % respectively and the Shah-London developing flow model tremendously dropped down to 14 %. Our fitted model further improved up to 4 % error. Deviation is bigger on channels with a larger tapered angle, but



(a) Coefficient curves.



(b) Exponent curves.

Figure 3.6: 3D surface fitted parameters of developing flow Nusselt number models for converging tapered channel on various tapering angles and Reynolds numbers.

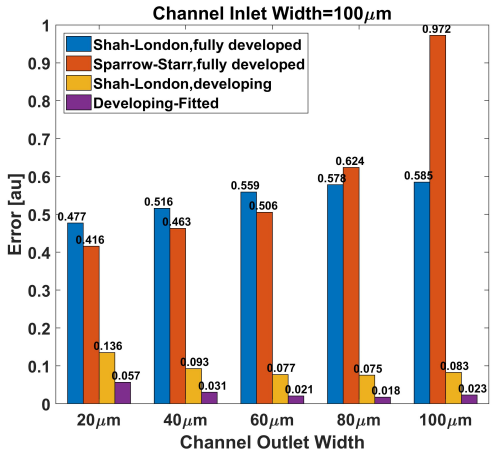
the difference is 1-3.5 %.

Furthermore, the Sparrow-Starr model is based on a tapered cylindrical model, which incorporates the effect of the slanted channel wall. However, this model is inapplicable for uniform channels with 0° angle. Rightmost bars from Figure 3.7a and 3.7c show uniform channels with the same inlet and outlet widths. Both Shah-London and Sparrow-Starr fully developed flow models were comparable between tapered channels, but the error rose significantly on the uniform channel and exhibited 97 % error from the FVM. On the other hand, our model is reliably accurate throughout all channel wall angles.

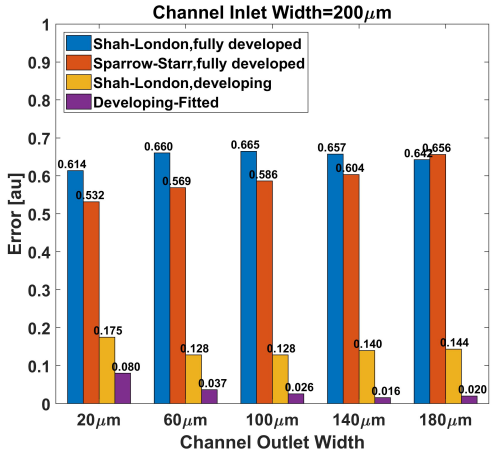
Referring to Figure 3.5, the discrepancy of analytical models to FVM is larger near the entrance region of the channel. The observation indicates that the fully developed assumption will lead to more unreliable result for channels which are significantly shorter than entry length. Channel geometry design with piecewise optimization will dissect the channel into small sections and apply the heat transfer model to each channel sections. In this design optimization, every channel section will carry large error, eventually accumulate throughout the entire channel and exacerbate the effect. Moreover, channel dimensions can alter between the sections and cause the flow to fluctuate. As a result, fully developed flow will never be reached in the extreme case.

Pressure Drop

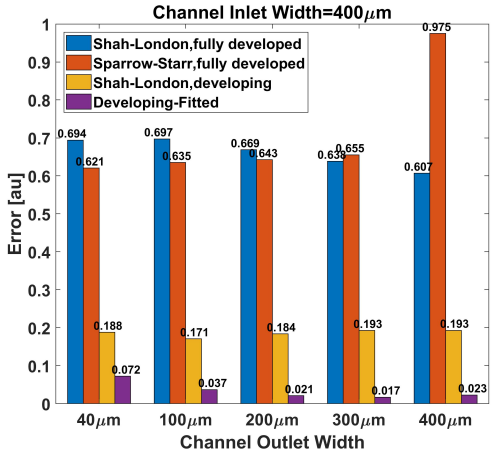
Cooling efficiency in microchannel comes at a price which can be mainly quantified by the pressure drop. Given microchannel design and the flow rate, pressure drop is determined. Darcy-Weisbach analytical pressure model for general channel in laminar flow is shown in Equation (3.13), where f_D is Darcy friction factor, four times the Fanning friction factor f from Equation (3.9), ρ is the density of the fluid, and u_{mean} is the mean flow velocity. Although it is a commonly used model in rectangular channels, there are discrepancies with numerical results on tapered channel design. Correlations for friction factor used in pressure formula for rectangular channels are derived in numerous works [66], [67]; however, the pressure model for tapered channel is not heavily studied.



(a) Tapered channel with inlet=100 µm.



(b) Tapered channel with inlet=200 µm.



(c) Tapered channel with inlet=400 µm.

Figure 3.7: Nusselt number error comparisons on various models: Shah-London (fully developed flow), Sparrow-Starr (fully developed flow), Shah-London (developing flow) and our fitted developing flow model.

$$\triangle P_{dw} = f_D L \frac{\rho u_{mean}^2}{2D_h} \tag{3.13}$$

Similar to the Nusselt number correlation parameter fitting, the pressure model is obtained from numerical results as Equation (3.14), and fitted curves are demonstrated in Figure 3.8. We have 3D surface fitted using the non-linear least squares method based on the Levenberg-Marquardt algorithm. Accuracy of surface fitting was maintained a minimum of 95 %. The pressure fitted model is valid for the range where the angle does not exceed to fully close the channel outlet. For example, given channel inlet width $w_{in} = 200\,\mu m$ and length $L = 500\,\mu m$, the maximum angle to preserve the open-ended channel is 11.3°.

$$\triangle P(\theta, Re) = \frac{795.335 + 38.9285\theta - 11.8544Re + 0.0685Re^2}{1 - 0.0278\theta - 0.0185Re + 0.0001Re^2} \tag{3.14}$$

As the tapering angle reaches the maximum angle, pressure drop will be extremely high, almost infinite. Beyond this angle, outlet width will fall below 0. Valid pressure drop cannot be computed at this angle and becomes singularity point in our fitted model. Fitted pressure curve demonstrated 1.58 % error to the FVM numerical result while Darcy-Weisbach model showed 46.92 % error, on average, on the same set of channels in Figure 3.8.

3.5 Conclusion

We have proposed an accurate closed-form model for tapered channel based on the developing flow model. Tapered channel designs will fluctuate the coolant flow, extend the developing flow region and possibly never reach fully developed state. Nevertheless, widely used correlations for optimizations were based on the fully developed flow models. Compared to the fully developed flow based thermo-fluid models, our derived correlations have reduced error by 57 % in Nusselt number, and by 45 % in pressure drop for channels with inlet width 100-400 µm compared to FVM simulation values. The model can conveniently be extended and applied to other channel sizes while maintaining the accuracy. As the model captures the relationship of fitting parameters in terms of the channel geometric dimensions, it can be

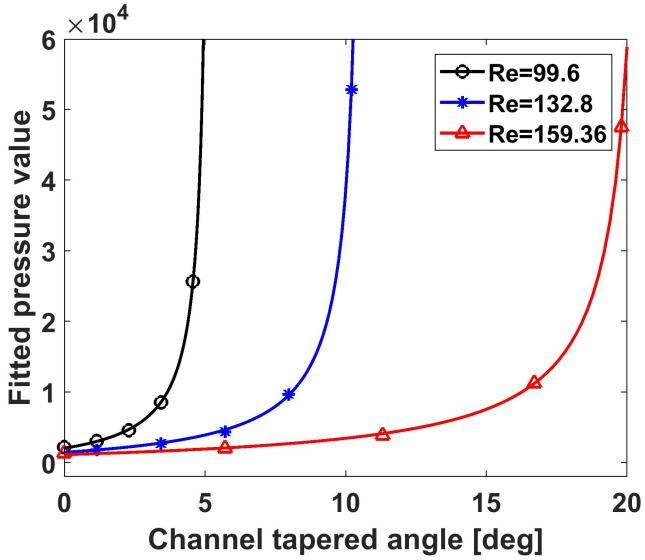


Figure 3.8: Pressure fitted curves of converging tapering channel on various tapering angles and Reynolds numbers.

applied for the accurate microchannel design optimizations.

CHAPTER 4

COMPLETE MODELS FOR LINEARLY TAPERED MICROCHANNELS

4.1 Introduction

In this chapter, we extend previously presented thermo-fluid correlations of the microchannel with any linearly angled wall for complete representation of the relationship between the channel parameters and the thermo-fluid performance. Similarly, thermal correlations are based on the developing flow model for varying channel shapes. In the microchannel, the flow behavior at the entrance region will be prolonged when microchannel dimensions vary across the flow direction. Therefore, correlation based on developing flow model will serve as a solid foundation for finding the optimal microchannel design. Assuming the channel is symmetrical in the length-wise axis, arbitrary shapes can be considered as a piece-wise linear channel, therefore, tapered channel was chosen in our model. It provides more flexibility and accuracy than a rectangular channel with constant width. To verify the accuracy of our models, we have compared with commonly used fully developed flow-based correlations and reliable numerical simulation.

4.2 Complete Microchannel Models

In this section, we start by introducing the parameters of the tapered microchannel dimensions, followed by the metric used to determine the thermal efficiency of liquid cooling heat exchangers. Then, appropriate heat transfer model for tapered microchannel design and analysis are proposed and further improved with parameter fitting.

4.2.1 Microchannel Geometry

Diverging channel is illustrated in Figure 4.1. Given the channel inlet width w_{in}, outlet width w_{out} and length L, the channel angle θ will be expressed as Equation (4.1). Opposed to tapered channel, channel with uniform cross-section from inlet to outlet is denoted as uniform channel in the remainder of the work.

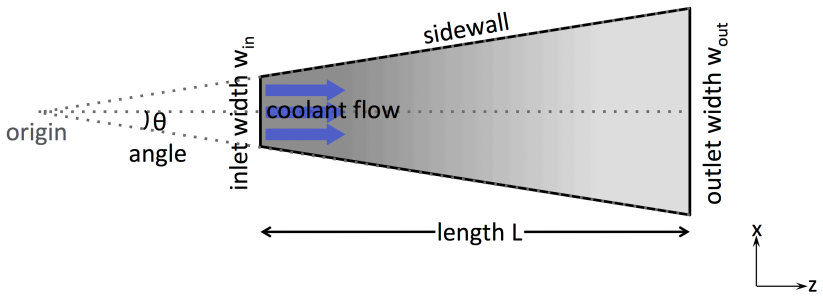


Figure 4.1: Diverging channel with inlet width w_{in}, outlet width w_{out}, length L, and half angle θ (top view).

$$\theta = arctan\left(\frac{w_{in} - w_{out}}{2L}\right) \tag{4.1}$$

4.2.2 Complete Model Derivation

To derive extended closed-form models, we have collected numerical simulation data of diverging shape channels, converging shape channels and uniformly straight channel. Then, we have performed parameter fitting from the base model, surface fitted to create improved correlations following the same procedure illustrated in Figure 3.4. The derived correlations are defined as functions of the microchannel design parameters and other fixed thermo-fluid parameters.

4.2.3 Simulator

To obtain numerical analysis data, we used the commercial CFD solver, ANSYS Fluent v.18. The software uses FVM with the support of the SIMPLE.

We applied rectilinear mesh with less than 0.1 maximum skewness, 0.1-0.5 million nodes depending on the channel size, 5 µm mesh element size and double-precision simulation setting. The solutions converged within 100 iterations.

4.2.4 Parameters

Microchannel dimensions for diverging shape used in the experiment are shown in Table 4.1. Height and length of the channel are fixed to single values as they are mainly defined by the manufacturing technology and the chip footprint. Channel inlet and outlet widths are varied between the minimum and maximum range listed. To ensure the converging tapered shape, channel outlet width is set less than or equal to the channel inlet width for each geometry. Tapering angle is computed using Equation (4.1). We used the same thermo-fluid conditions and properties of materials used in the converging channel simulations. Water at room temperature is used as coolant and inlet flow velocity is set to 1 m/s. Adding fluid velocity into the optimization variable can be the future extension of this work.

First, we have compared the models of different flow conditions and analysis methods. Figure 3.5a compares four models: 1) Shah-London fully developed model for rectangular channel [59], 2) Sparrow-Starr fully developed model for tapered cylindrical channel [64], and 3) Shah-London developing flow model for general channel compared with 4) FVM numerical simulation. Model comparison was experimented on a single tapered channel with inlet width of 400 µm, outlet width 200 µm, length 500 µm with inlet flow velocity

Table 4.1: Microchannel Parameters

Definitions	Param.	Min	Max
Height	H	100 µm	
Length	L	0.5 mm	
Inlet width	w_{in}	100 µm	400 µm
Outlet width	w_{out}	100 µm	600 µm
Angle	θ	$-84°$	$0°$

1 m/s and heat flux 100 W/cm^2. Regardless of two different geometry approaches, rectangular versus tapered channel, both fully developed models showed big gaps between the local Nusselt number values as well as the Nusselt number gradients along the channel to the FVM result. On the contrary, developing flow model for circular and non-circular channels has reasonably well-matching curve to the FVM result.

4.2.5 Correlations on Diverging Microchannel

The coefficient and the exponent of Nu number on diverging channels are shown in Equation 4.2 and Equation 4.3. Similar to the converging channel, these derived functions replace α and β in Equation 3.10 to complete the local Nu number correlation. Developing flow built by Shah-London has shown 15.4 % error compared to the numerical results and our model has improved to 3.94 % error in Nusselt number. Pressure drop correlation is derived in similar fashion.

Error rates on pressure values are 89.69 %, 24.82 % and 26.26 % on the channels with inlet width 100 µm, 200 µm and 400 µm respectively on Darcy-Weisbach pressure model. Our correlation has shown 3.04 %, 1.01 % and 0.68 % on the channels with inlet width 100 µm, 200 µm and 400 µm respectively.

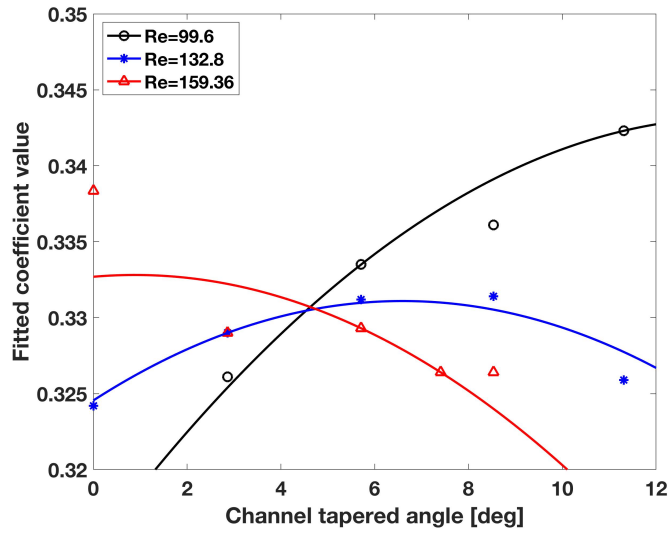
$$\begin{aligned}\alpha(\theta, Re) &= 0.2884 + 0.01058\theta + 0.0002438Re \\ &\quad - 0.0001506\theta^2 - 6.474 * 10^{-5}\theta Re + 2.148 * 10^{-7}Re^2\end{aligned} \tag{4.2}$$

$$\begin{aligned}\beta(\theta, Re) &= -0.4656 + 0.00448\theta + 0.000395Re \\ &\quad - 7.649 * 10^{-5}\theta^2 - 2.652 * 10^{-5}\theta Re - 1.181 * 10^{-6}Re^2\end{aligned} \tag{4.3}$$

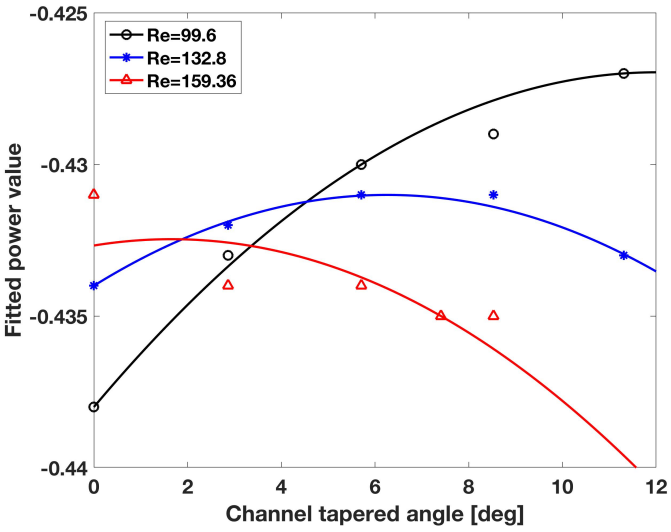
$$\triangle P(\theta, Re) = \frac{1412 - 10.28\theta - 21.21Re + 0.1125Re^2}{1 + 0.04096\theta - 0.0184Re + 0.0001029Re^2} \tag{4.4}$$

4.2.6 Correlations on Constant Inlet Velocity

However, microchannel dimensions commonly used in electronics result in non-negligible entrance length with developing flow before the fluid reaches fully developed flow. Moreover, fluid in a microchannel with varying shapes

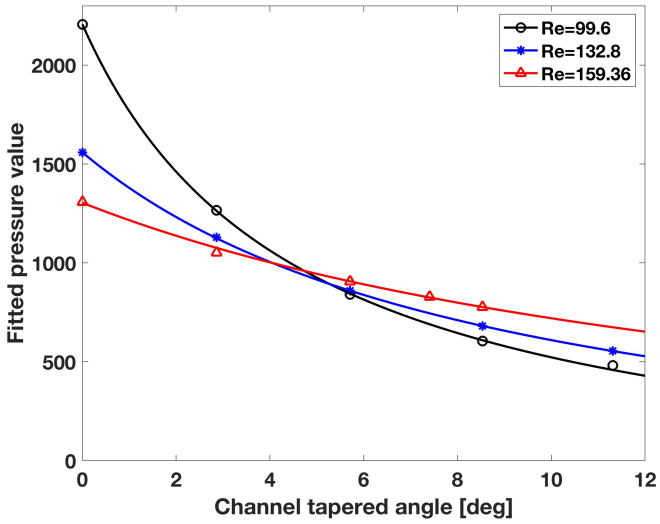


(a) Coefficient curves



(b) Exponent curves

Figure 4.2: 3D surface fitted parameters of developing flow model for diverging shape channel on various tapering angles and Reynolds numbers. (cont.)



(c) Pressure curves

Figure 4.2: 3D surface fitted parameters of developing flow model for diverging shape channel on various tapering angles and Reynolds numbers.

along the coolant flow direction will never reach the fully developed state.

For accurate channel width variation modeling, smooth channel wall transitions as well as faster design convergence, we have considered linearly tapered channel as our base microchannel design. Tapered channel can be mainly divided into converging and diverging shapes as Figure 4.1. The converging channel will contribute to thermal performance improvement, especially temperature gradient reduction by narrowing the outlet where coolant temperature is risen with absorbed heat. The diverging channel will reduce the pressure drop by relaxing the cross-sectional area of the channel.

Channel optimization based on either the converging or diverging channel model will limit the resulting channel in monotonic converging or diverging shape or may lead to inaccurate analysis for channels with other geometries. Assume a straight channel is divided into multiple sections length-wise and optimized per-section using the converging channel model. Every segment of monotonically converging channel will have relatively wide inlet and narrow outlet. On the segment boundaries, outlet width of the current segment $w_{out,i}$ is greater than or equal to the inlet width of the following segment $w_{in,i+1}$, $w_{in,i+1} \leq w_{out,i}$. Although each segment conserves converging shape,

if the inlet of the following segment is wider than the outlet of the current segment, the converging channel model will introduce error in the analysis. For a higher degree of design freedom in the optimization, a model for a generalized channel is required.

Similar to the approach in the converging channel designs, we have further fitted the parameters to model the local Nusselt number of any tapered channel including converging and diverging shapes as in Equations (4.5) and (4.6). Figure 4.3 depicts the fitted curves of the complete channel. Converging channel is represented with positive tapering angle and diverging channel is represented with a negative tapering angle. Either the tapered channel model converges at deg 0, which is the uniformly straight channel with constant width. The derived pressure model for complete channels is shown in Equation (4.7).

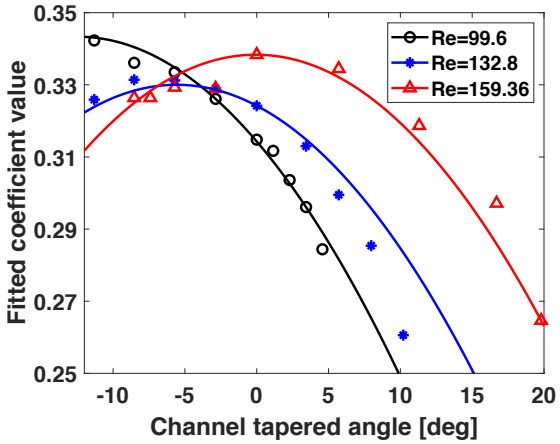
$$\begin{aligned}\alpha(\theta, Re) &= 0.3365 - 0.01238\theta - 0.0006135Re \\ &\quad - 0.0001868\theta^2 + 7.753 * 10^{-5}\theta Re + 3.923 * 10^{-6}Re^2\end{aligned} \tag{4.5}$$

$$\begin{aligned}\beta(\theta, Re) &= -0.4517 - 0.005169\theta + 0.0001498Re \\ &\quad - 7.265 * 10^{-5}\theta^2 + 3.227 * 10^{-5}\theta Re - 1.26 * 10^{-7}Re^2\end{aligned} \tag{4.6}$$

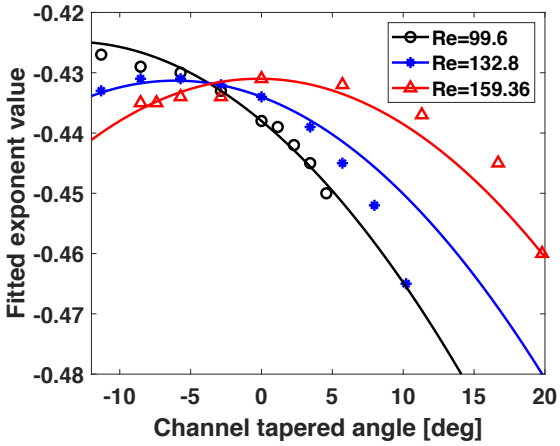
$$\triangle P(\theta, Re) = \frac{1142 - 24.21\theta - 18.24Re + 0.1018Re^2}{1 - 0.0281\theta - 0.01851Re + 9.978 * 10^{-5}Re^2} \tag{4.7}$$

4.3 Conclusion

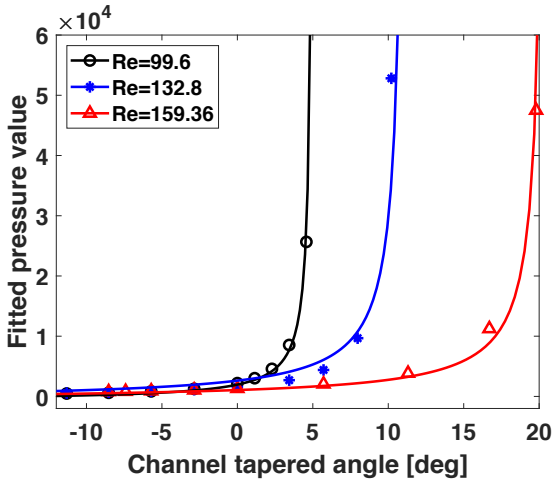
We have presented accurate and complete closed-form models for any tapered channel based on the developing flow model. Tapered channel designs will fluctuate the coolant flow, extend the developing flow region and possibly never reach the fully developed state. Nevertheless, widely used correlations for optimizations were based on the fully developed flow models. For diverging microchannels, compared to the Shah-London developing flow model, our Nu number correlation has 11 % less error. For pressure drop, we have 45 % less error than the Darcy-Weisbach model for channels with inlet width 100-400 µm to FVM simulation values. As the models capture the relationship of fitting parameters in terms of the channel geometric dimensions, they can be applied for accurate microchannel design optimizations.



(a) Coefficient curves



(b) Exponent curves



(c) Pressure curves

Figure 4.3: 3D surface fitted parameters of developing flow model for any tapered channel on various tapering angles and Reynolds numbers.

CHAPTER 5

LIQUID COOLING MICROCHANNEL OPTIMIZATION

5.1 Introduction

To attain the feasibility of liquid cooling technique in compact chip packaging, it is crucial to design low power and highly efficient microchannels. Similar to other physical designs, microchannels require more power to obtain high thermal performance, and well-balanced tradeoff is necessary.

The majority of research works on channel design optimization are based on runtime expensive numerical simulations, oversimplified thermo-fluidic models or correlations with incorrect assumptions. Numerical models are typically unsuitable for optimization considering intensive computing. Approximate models or correlations with improper assumptions pose a fundamental limitation to accurately derive the relationships between the channel parameters and the thermal performance. Applying a fully developed flow model on a short channel that presents developing flow will cause large discrepancy. In microchannel optimization, inaccuracy on the base channel model will significantly affect the optimality and quality of the resulting design.

If empirical data is unavailable, numerical methods are typically adopted to perform accurate analysis of complex thermo-fluid physics of the microchannel. However, numerical method limit the design optimization domain due to compute-intensiveness. On the other hand, the majority of the existing channel correlations for fast analysis are based on fully developed flow, which does not apply for the cases with varying channel shapes.

In this chapter, we optimized the microchannel with balanced thermal performance and coolant pumping power based on our correlations presented in Chapter 3 and validated with numerical simulations [38]. Our model controls channel inlet width and tapering angle to maximize the thermal perfor-

mance subject to cooling energy and manufacturing constraints. The results demonstrate significantly improved estimation of overall thermal resistance and provide reliable optimized microchannel design.

5.2 Related Works

Microchannel design optimization using channel width modulation has been introduced by Sabry et al. [57]. Microchannel width is varied for each section while maintaining constant width for each section, resulting in piece-wise rectangular microchannel. Another microchannel optimization on grid-like network design has been studied Chen et al. [60]. These works, like other similar optimizations, are based on a rectangular channel in a fully developed flow model, which does not accommodate the flow fluctuation between the sections and friction across channel wall from abrupt wall changes.

In our work, we perform microchannel optimization on developing flow models derived in Chapter 4. One example of optimized microchannels based on given thermal map of the chip is illustrated in Figure 5.1. The channel shapes can vary depending on the location on the chip, the amount of heat generated by the neighboring components and the performance of neighboring microchannels. We run the same experiment with fully developed models and compare the resulting designs. Then, we use the commercial numerical solver to check which design performs better with given objectives to verify the importance of applying the appropriate analysis model.

5.3 Constant Inlet Volumetric Flow Rate

Previous correlations are based on constant coolant inlet velocity. The models are beneficial for optimizing a single channel as an entire piece. However, when microchannel is divided into multiple sections in length-wise direction, we can no longer apply the same model for accurate analysis. The fluid velocity condition for the inlet that is controlled by the pump will be different from the remaining sections if the width changes, resulting in varying mean velocity. Consider the two-section microchannels illustrated in Figure 5.2. As the channel widths w_i are varied along the axial direction, the coolant

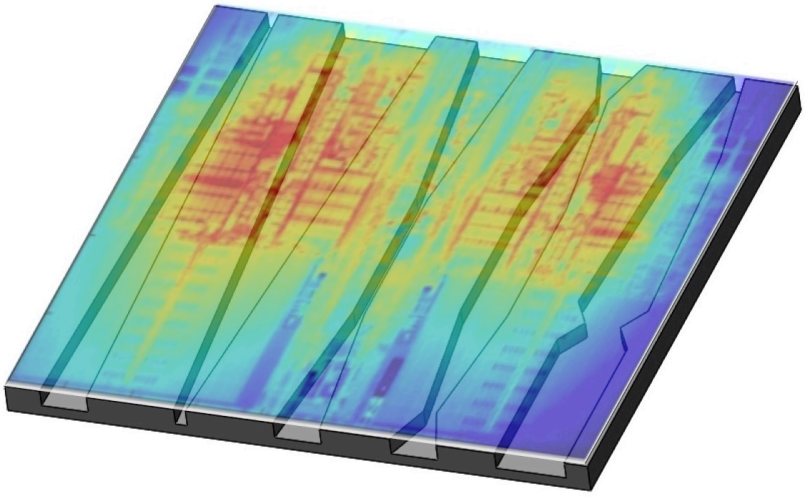
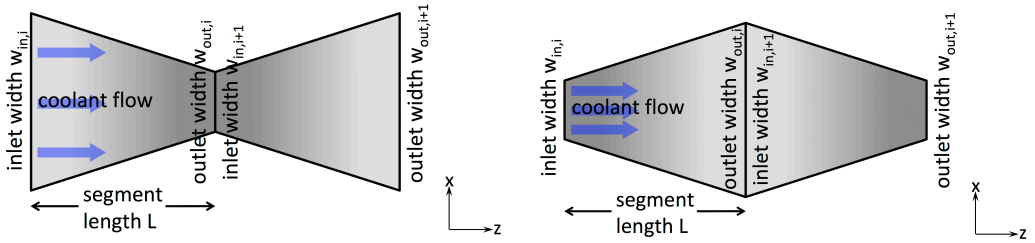


Figure 5.1: An example of arbitrary microchannel design on given thermal map of the chip.

velocity will change accordingly based on equation $u = \dot{V}/A = \dot{V}/(w_i H)$. It leads to different Reynolds numbers and pressure drop values. On the other hand, due to the mass conservation law, volumetric flow rate will be conserved throughout the channel from inlet to outlet. Figure 5.3 shows how the velocity and cross-sectional area change but the volumetric flow rate remains constant in diverging-converging channel in Figure 5.2b.



(a) Converging-diverging channel

(b) Diverging-converging channel

Figure 5.2: Examples of two-section channels.

To be more specific, when the channel inlet widths are increased, Re has increased on constant velocity, but decreased on constant volumetric flow rate assumption. Therefore, for length-wise channel optimization, we derived

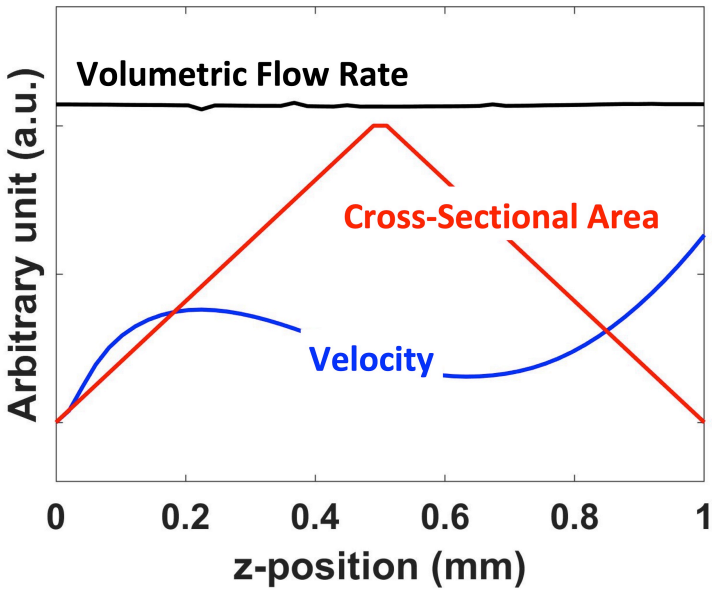


Figure 5.3: Velocity, cross-sectional area and volumetric flow rate profiles on diverging-converging channel.

the correlations based on fixed volumetric flow rate. We applied the same approach as before, varied inlet velocity based on cross-sectional area of the inlet between the designs. All linearly tapering channels, i.e. converging, diverging and straight channels, are considered in the models.

Using the thermo-fluid properties listed in Table 5.1, we have fitted parameters using least squares method with average error of 95 %. For the complete Nu number correlation of any tapering channel on constant volumetric flow, we have achieved 4.22 % error while original developing flor model shows 18.07 %.

$$\begin{aligned}\alpha(\theta, Re) = {} & 0.1446 - 0.001179\theta - 0.001138Re \\ & - 6.603 * 10^{-5}\theta^2 - 2.271 * 10^{-5}\theta Re + 2.829 * 10^{-5}Re^2\end{aligned} \tag{5.1}$$

$$\begin{aligned}\beta(\theta, Re) = {} & -0.4681 - 0.0015140\theta + 0.0008248Re \\ & - 9.804 * 10^{-5}\theta^2 - 3.37 * 10^{-6}\theta Re + 1.137 * 10^{-5}Re^2\end{aligned} \tag{5.2}$$

$$\triangle P(\theta, Re) = \frac{0.1566 + 10.14\theta + 9.175Re - 0.079Re^2}{1 - 0.010820\theta - 0.02022Re + 0.0001079Re^2} \tag{5.3}$$

Table 5.1: Thermal and Fluid Properties

Definitions	Param.	Values
Silicon thermal conductivity	k_{si}	$130\,\mathrm{W/m\text{-}K}$
Water thermal conductivity at 300 K	k_{water}	$0.613\,\mathrm{W/m\text{-}K}$
Water kinematic viscosity	ν	$1.004 \times 10^{-6}\,\mathrm{m^2/s}$
Coolant volumetric flow rate	Q	$1 \times 10^{-8}\,\mathrm{m^3/s}$
Coolant inlet temperature	T_{inlet}	300 K
Prandtl number for water at 300 K	Pr	5.83
Reynolds number	Re	39-99

5.4 Microchannel Optimization

An optimized channel can result in not only monotonically converging, straight or diverging shape but also wavy or any other random geometry. Based on both converging and diverging tapered channel models on constant volumetric flow velocity, we optimized the microchannel to minimize the thermal resistance with channel width and pressure constraints. Any other assumptions and boundary conditions fixed on our problem are listed below.

Assumptions

- Uniform heat flux, Q", on channel walls (from the power source of the circuit)
- Laminar coolant flow, $Re < 2300$
- Volumetric flow rate, $\dot{V}$, is set to $1 \times 10^{-8}\,\mathrm{m^3/s}$ at inlet
- Constant coolant temperature through inlet, T_{inlet}
- Pressure is set to 0 at the outlet, P_{outlet}
- Single-phase incompressible coolant in liquid state
- Gravity and radiation heat transfer is neglected
- Viscosity dissipation is negligible
- Steady-state on symmetric model
- Continuity, momentum, energy equations are solved subject to no-slip boundary condition

5.4.1 Optimization Problem

Given a specified channel length and heap map of the device, our goal is to maximize the thermal performance with the cooling power and manufacturing constraints as in Equation (5.4). Two design variables, channel width and tapering angle, are varied with very fine granularity, hence considered as continuous variable. Regarding a straight channel from one chip boundary to another, the footprint defined by the device will determine the channel length. Depending on each section length, the number of sections will vary with the chip size. Within a given chip, the section granularity can also be controlled depending on the designer, but it also should consider the manufacturability of the channel and should be defined by the resolution of the fabrication technology of interest. In our experiment, we have fixed the section length to 500 µm that has been used to derive the correlations on more smooth angle variations and has better aspect ratio with the maximum and minimum widths. In addition, we fixed the channel height as it is typically determined from the etching process.

Constant heat flux instead of constant temperature on the channel wall is used in the analysis to closely mimic the behavior of the electronics. Assuming static operation mode in the circuit, heat generated by each component will be constant, equivalent to fixed value current source in electric circuit representation. Microchannel wall temperature depends on the relative cooling performance of the channel compared to the device layer and thermal resistance will vary in the optimization process. Optimization parameters used in this experiment are listed in Table 5.2.

$$\begin{aligned} f(w) &= min(R_{th,conv}) = min(\frac{1}{hA_{wet}}) \\ &s.t.\ \triangle P \leq P_{th} \\ &w_{min} \leq w_i \leq w_{max} \end{aligned} \tag{5.4}$$

5.4.2 Simulated Annealing

Simulated annealing is a stochastic optimization method based on the physical process of annealing. It is a robust technique commonly used in the electronic design automation to find near-optimal solution. We have applied

Table 5.2: Optimization Parameters

Parameters	Values
Number of sections	4, 10, 20, 100
Channel length	2mm, 5mm, 1cm, 5cm
Section length	500 µm
Width granularity	3 µm
Maximum width	400 µm
Minimum width	100 µm
Heat flux	100 W/cm^2
Threshold pressure	P_{max}, $0.9P_{max}$, $0.8P_{max}$, $0.7P_{max}$

this technique in our channel optimization. Microchannel is dissected to N sections from inlet to outlet with the same section length L/N, where L is the channel length. At every section interface i including the inlet and outlet, width value w_i is set between given minimum w_{min} and maximum w_{max} constraints. Between iterations, one of the sections will be randomly selected to alter the width by a small amount δ to evaluate the new solution. If the new solution is better than the old solution in terms of the cost, we update the solution. Otherwise, we accept the new solution with the acceptance probability. As the algorithm proceeds, we accept worse solution less and less and converge to the final optimized solution. Pseudocode of the simulated annealing implementation is written in Algorithm 1. It is well known that the quality of the solution depends heavily on the initial annealing temperature. The method to find the ideal initial temperature is implemented from this work [68].

For easier illustration, Figure 5.4 shows the flow of the simulated annealing optimization technique.

Algorithm 1: Microchannel Optimization using Simulated Annealing

```
Find an ideal initial annealing temperature;
Set an acceptance probability;
Initialize current_solution;
Compute the cost of current_solution;
while !stop criterion do
    Find a new_solution;
    Calculate the cost of new_solution;
    if (new_cost − current_cost) ≤ 0 then
        current_state = new_state;
    else
        if acceptance probability then
            Accept solution;
            current_solution = new_solution;
        else
            Reject solution;
    Decrease the temperature;
```

5.5 Experimental Results

5.5.1 Simulator

Similar to Chapter 3, we used commercial CFD solver, ANSYS Fluent v19, for numerical simulation. We applied rectilinear mesh of 10 µm mesh size with less than 0.1 maximum skewness for single tapering angle designs, 0.65 for multi-angle designs and double-precision simulation setting. The solutions converged within two hundred iterations. For runtime comparison, we ran our experiments on Intel Xeon processor 8-core at 3.7 GHz with 64 GB memory.

5.5.2 Optimized Channels

We obtained optimal channel designs on various pressure constraints and channel lengths. The minimum and maximum widths are set to 100 µm, 400 µm respectively. To explore how the channel shape changes, we performed experiments on simple 2 mm channel with four sections. Pressure drop constraints were varied from no constraint, 9000 Pa to 3000 Pa at every

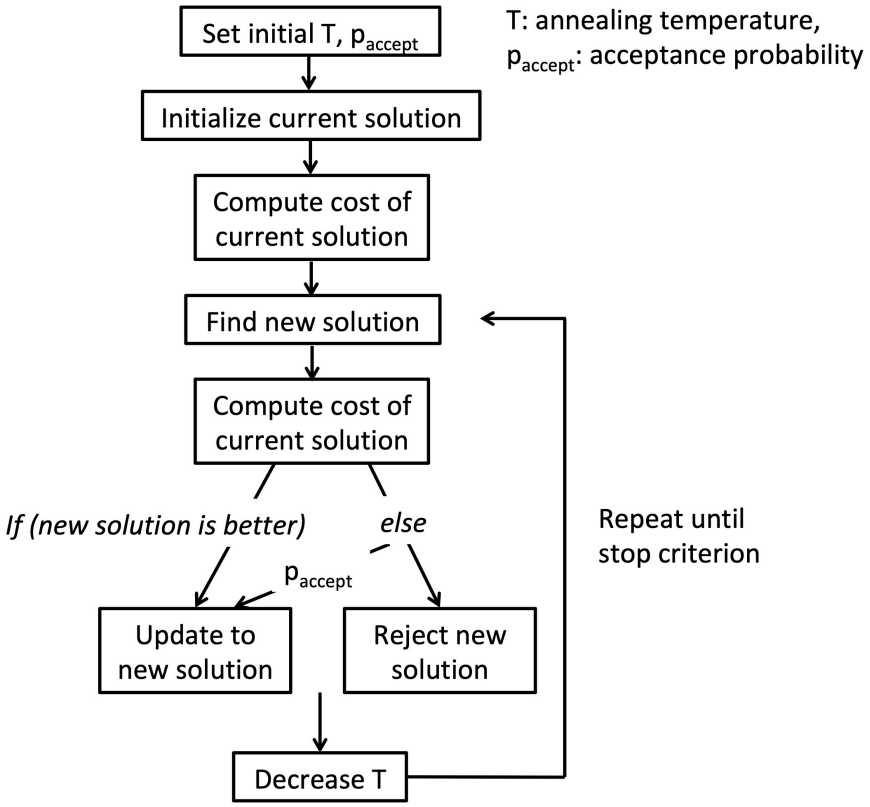


Figure 5.4: Flow chart of simulated annealing method.

1000 Pa granularity and the minimum value 2800 Pa. No pressure drop constraint is equivalent to setting the pressured drop higher than the maximum pressure value, P_{max}, which is the pressure value when the channel is uniform at minimum width. First, we have ran the simulated annealing optimization based on constant inlet velocity flow models. Regardless of the varying pressure drop constraint, the outcome channel results as in Figure 5.5. In other words, this channel was providing the highest thermal performance while minimizing the pressure drop. However, the analysis is counter-intuitive. The experimental result shows that it is crucial to use a proper models for thermo-fluid analysis in order to find the optimal channel design.

Then, we repeated the optimization engine based on constant volumetric flow rate models. Results are shown in Figure 5.6.

It is a very interesting observation how the channel shape changes along

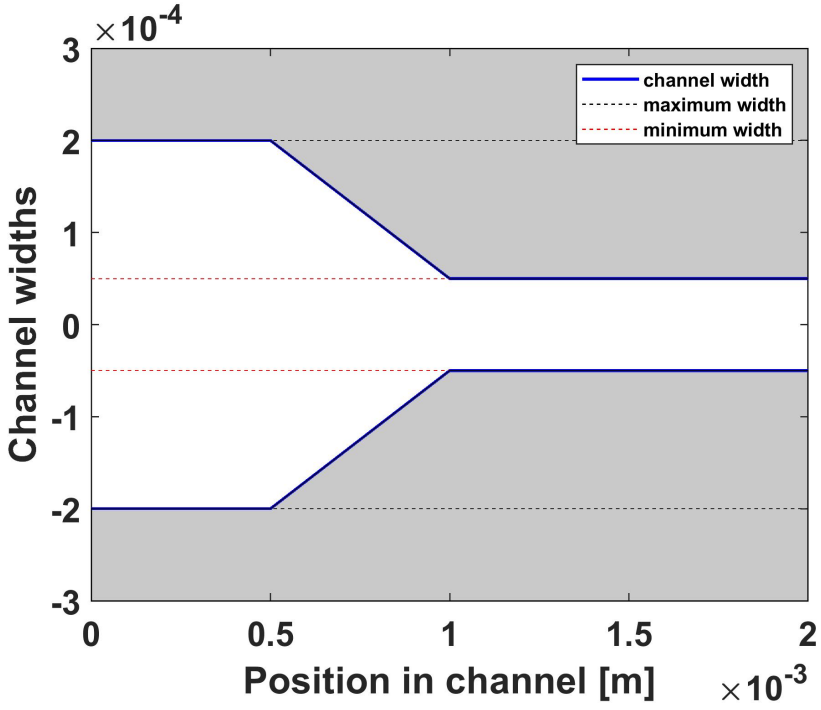
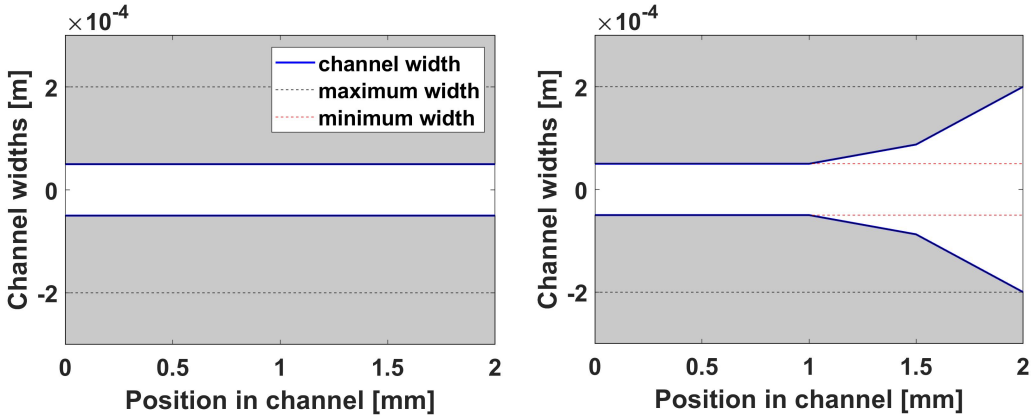


Figure 5.5: Optimized channel on constant inlet velocity flow models

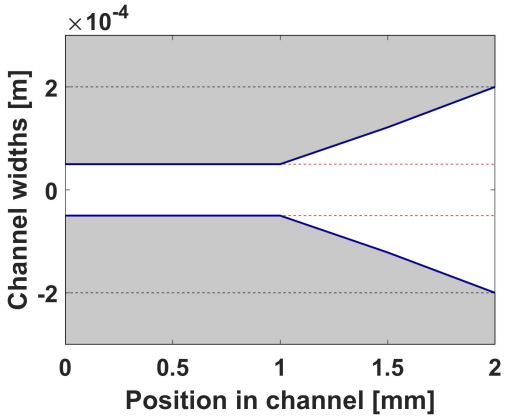
with the constraints. When a pressure threshold is set to a very large value, i.e. no pressure constraint, the channel results in straight uniform channel with minimum width. Thermal performance is maximum with high coolant velocity, hence the best thermal performance is guaranteed. As the threshold pressure decreases from the maximum value, the outlet starts to get wider to relax the pressure. The inlet is kept at narrow width to preserve the thermal performance. Then, under tighter constraint, the inlet also gets widened but the midsection is preserved to be narrow, resulting in hourglass shape. Existing analytical studies on microchannel design have suggested that wavy shape offers the benefit of balanced pressure drop release and enhanced thermal performance. Our result shows a similar tendency, but not necessarily regularly repetitive converging and diverging shape. Finally, under the tightest pressure constraint, the channel reaches fully maximum width in rectangular shape. As predicted, increased flow velocity leads to improved heat transfer performance and slanted wall contributes to flow perturbation, which leads to enhanced thermal efficiency.

For optimal design comparison, we have run the same optimization al-

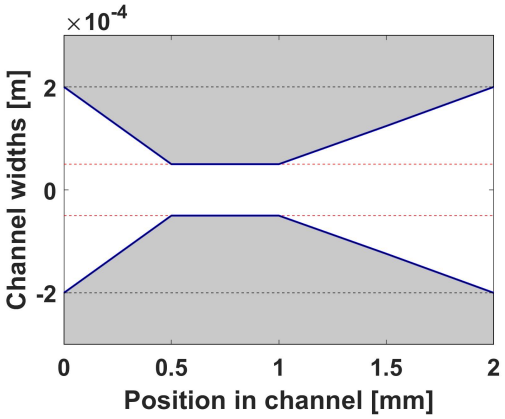


(a) No pressure constraint or $P_{th} = \inf$

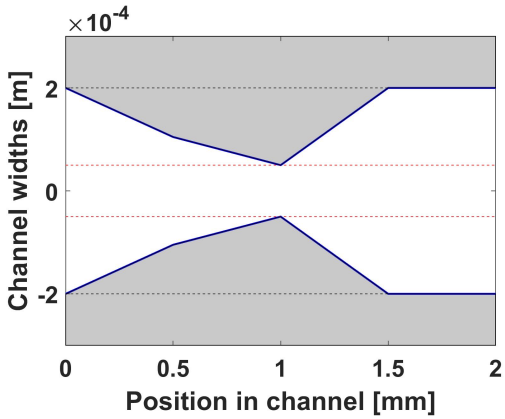
(b) $P_{th} = 9000\,\text{Pa}$



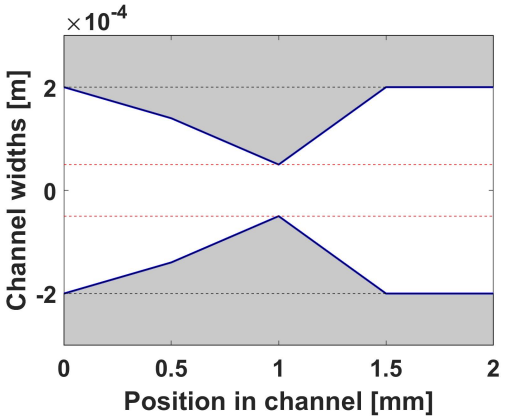
(c) $P_{th} = 8000\,\text{Pa}$



(d) $P_{th} = 7000\,\text{Pa}$

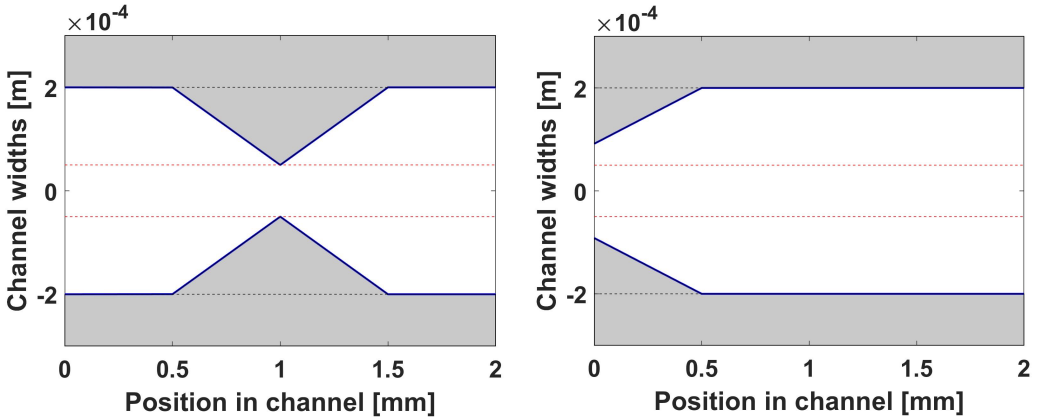


(e) $P_{th} = 6000\,\text{Pa}$



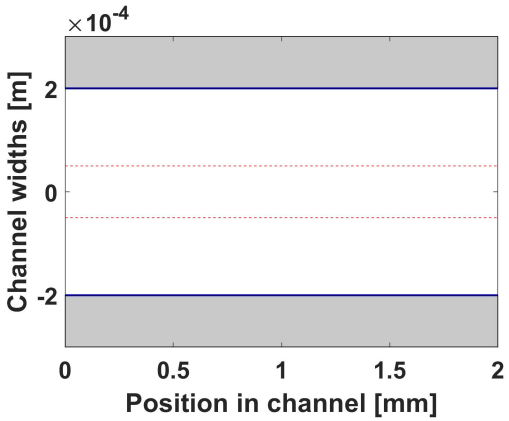
(f) $P_{th} = 5000\,\text{Pa}$

Figure 5.6: Optimized four-section channels with various pressure drop constraints using derived developing flow models. (Continued on next page.)



(g) $P_{th} = 4000\,\mathrm{Pa}$

(h) $P_{th} = 3000\,\mathrm{Pa}$



(i) $P_{th} = 2800\,\mathrm{Pa}$

Figure 5.6: (Continued) Optimized four-section channels with various pressure drop constraints using derived developing flow models.

gorithm based on Shah-London fully developed flow Nusselt number model and Darcy-Weisbach pressure drop model. Obtained channels shown in Figure 5.7 are different from the ones above with developing flow models. Note that the threshold pressure values vary by an order of magnitude due to the flow assumption. Under no pressure constraint, the resulting channel was a straight shape with maximum width defined. As threshold pressure has reduced, inlet has been narrowed down, which is the opposite behavior of the optimization result based on developing flow. Pressure was maintained below the constraint by keeping the outlet region at maximum width. For accurate comparison, we further verified the channel performance through

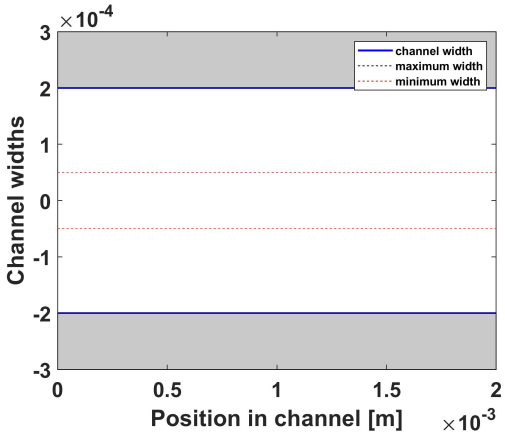
numerical simulation and the result is captured in Table 5.3.

Table 5.3: Thermal Resistance and Pressure Drop Comparison

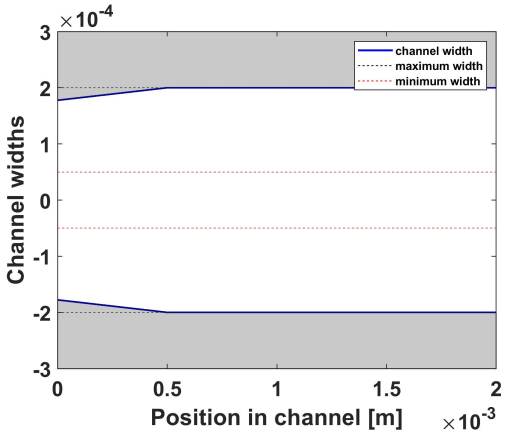
# of sec	P_{th} [Pa]	R_{th} [K/W]	Actual $\triangle P$ [Pa]
4	∞	338.34	9227
	9000	367.19	9000
	8000	376.34	8000
	7000	401.21	7000
	6000	444.89	6000
	5000	457.59	5000
	4000	471.74	4000
	3000	479.38	3000
	2800	480.63	2800

To evaluate the thermal performance of optimized channels, we ran numerical simulations on the resulting four-section channels under various pressure constraints. Temperature maps of five different microchannels are displayed in Figure 5.8. Optimization based on developing flow model, Figure 5.8a shows the thermal map of the channel with no pressure constraint. The maximum temperature of the straight channel with the minimum width is $T_{max} = 346.8\,\mathrm{K}$, the lowest among the channels, i.e. the best thermal performance. It is expected to result in the best performing design when there is no cost to be sacrificed. Then, the channels are displayed in the order as the pressure drop constraint becomes tighter. The maximum temperatures from Figure 5.8b through Figures 5.8e are $T_{max} = 389.9\,\mathrm{K}, 410.4\,\mathrm{K}, 396\,\mathrm{K}$ and $397.3\,\mathrm{K}$ respectively. The channel in Figure 5.8c shows the highest maximum temperature of all, which displays one drawback of our correlations. From the converging and diverging channel shape, the temperatures on the corners and wall boundaries in diverging sections are the most elevated. This result is due to the dead zone created in the spot with laminar flow, i.e. low Reynolds number. The model can be extended to capture the existence of this dead zone, which we have listed as potential future work in Chapter 6.

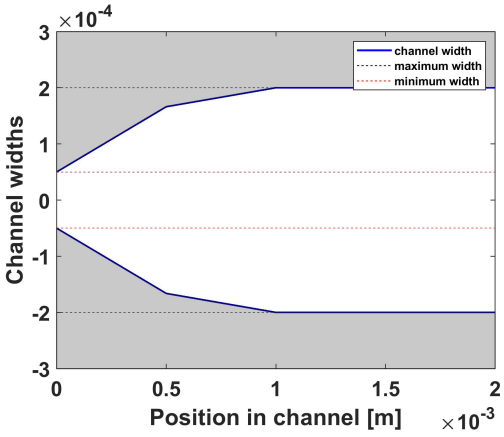
On the other hand, the channel shapes resulting from fully developed flow model based optimization are listed in Figure 5.8e, 5.8d. In contrast to the developing flow based optimization, microchannel design with no pressure



(a) No pressure constraint



(b) $P_{th} = 100\,\mathrm{Pa}$



(c) $P_{th} = 70\,\mathrm{Pa}$

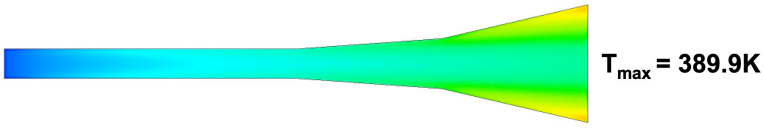
Figure 5.7: Optimized four-section channels with various pressure drop constraints using fully developed flow models.

constraint has resulted in worse design than the retrained pressure drop. This numerical result verifies that the optimization based on incorrect model is counter-intuitive and outputs non-optimal designs.

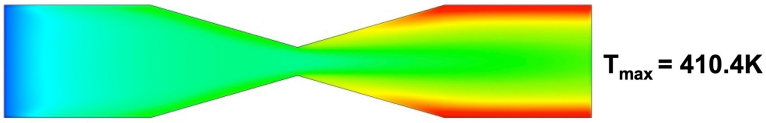
5.5.3 Runtime Comparison

In Table 5.4, we compare the runtime of single optimization run with single FVM run for computing the performance of the channel. We counted the number of designs computed in the optimization and then multiplied

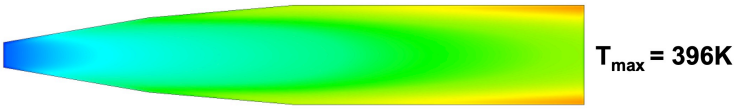
(a) Straight channel with minimum width on *no* P_{th}



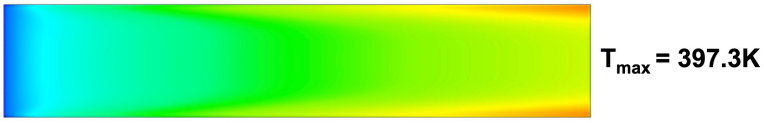
(b) Straight to diverging channel on $P_{th} = 9000\,\text{Pa}$



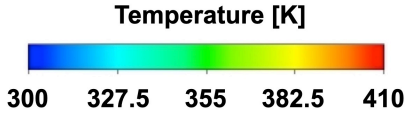
(c) Converging to diverging channel on $P_{th} = 4000\,\text{Pa}$



(d) Diverging to straight channel on $P_{th} = 3000\,\text{Pa}$ on developing flow model or $P_{th} = 70$ on fully developed flow model



(e) Straight channel with maximum width on $P_{th} = 2800$ for developing flow model or $P_{th} = \text{inf}$ on fully developed model



(f) Temperature bar

Figure 5.8: Temperature map of the four-section optimized channels on various pressure constraints. All thermal maps are illustrated based on the same temperature bar displayed in (f).

with single FVM run to find the projected runtime for numerical method based optimization. Our correlations based optimization ran slightly above 10 seconds for four-section microchannels and it did not show any variation between the pressure constraints, i.e. O(1) runtime for given number of sections or O(N) for N sections. One FVM run of the same channel takes a few seconds and it results in hundreds of hours for the same amount of design comparison. Also, by comparing the four-section channel example under $P_{th} = 9000\,\text{Pa}$ and $P_{th} = 4000\,\text{Pa}$, we can observe that depending on the pressure constraint, the number of nodes/elements in mesh will differ due to the design size complexity. Therefore, we can conclude that the runtime can vary depending on the pressure constraint and the resulting channel geometries, i.e. O(M) for mesh size M. Note that M is largely dependent on N as well. In this comparison, we have considered the numerical simulation only for a given design, however, the overall runtime will increase if mesh generation of the design and communication interface with the commercial software are included.

Table 5.4: Runtime Comparison of Single Optimization Run on Our Model and FVM

# sect	P_{th}	1-Op [sec]	# iter.	mesh size	1-FVM [sec]	Proj.Run [hr]
4	∞	10.458	448414	24079	0.734	91.427
	9000	10.771	450002	36839	2.835	354.376
	4000	10.484	439654	91553	7.303	891.887
	2800	10.111	422239	88847	2.268	266.01

5.6 Conclusion

To the best of our knowledge, this is the first microchannel optimization work based on developing flow model. Existing work was based on fully developed flow models, which become inaccurate when the channel shape changes to non-uniform geometry. We found that, because of the varying cross-sectional area, the constant velocity model does not maintain accuracy. Based on mass conservation law, we have derived constant volumetric flow rate based

correlations to use in multi-sectional optimization. Unlike constant velocity cases, as the inlet width increases, Reynolds number has decreased in this relationship.

We have applied simulated annealing technique in our optimization. Simulated annealing is a well-known robust optimization method very commonly used in the electronic design automation field and provides close to optimal solution. For comparison, we have performed the optimization on 1) our closed-form developing flow, constant velocity correlations, 2) our closed-form developing flow, constant volumetric flow rate correlations, and 3) Shah-London fully developed flow correlation with Darcy-Weisbach pressure drop correlation. Then, we compared it with the FVM result to verify the accuracy. Results show that the optimization channel geometries are completely different from the base flow model as the pressure drop constraint changes. Temperature map from FVM shows that the thermal performance is better with relaxed pressure drop constraint in developing flow case; however, it presents the opposite behavior on fully developed flow assumption, which is counter-intuitive. Finally, we compared the runtime of the closed-form correlations based optimization with numerical simulation. It takes a few seconds to compute four-section channel design in multi-core parallel computation; however, considering the number of designs analyzed during the optimization, it will take more than a few days, or even a month, on complex geometry.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Significance of Work

Thermal issues constitute a critical barrier to the development of 3D IC packaging technology. To overcome the exacerbated thermal challenges, we have studied two different thermal designs, set up the analytical models, optimized the design parameters and compared the performance through numerical simulation.

In Chapter 2, we presented a new design of TTSV with fin-like geometries to enhance on-chip cooling in 3D ICs. Fin-like geometries reduce the number of TTSVs needed for similar cooling performance, which relaxes the fabrication and routing constraints on the design. The distance of the hotspot from the fin was found to play a crucial role in the combined equivalent thermal resistance. The usage of the fin is recommended if the hotspot can be reached from the via in less than 10 µm. Otherwise, additional complexity in manufacturing processes and stricter routing constraints due to the extra fins will outweigh the small efficiency gains. New structures and designs of TTSVs to reduce the thermal management issues in 3D ICs were found to be a reasonable area to explore further.

In Chapter 3, we proposed an accurate closed-form model for a liquid cooling tapered microchannel based on the developing flow model. Tapered channel designs will fluctuate the coolant flow, extend the developing flow region and possibly never reach the fully developed state. Nevertheless, widely used correlations were based on fully developed flow models. Compared to the fully developed flow-based thermo-fluid models, our derived correlations have reduced error by 57 % in Nusselt number and by 45 % in pressure drop for channels with an inlet width 100-400 µm compared to FVM simulation values.

Our thermal closed-form analytics models capture the relationship of the design parameters in terms of the geometric dimensions. The models can be applied for the accurate design optimizations on various environmental conditions.

6.2 Potential Future Work

6.2.1 4D or Above Microchannel Correlations

While we have greatly improved the accuracy by implementing a developing flow model, there still exist various physics we did not consider, such as non-uniform incoming velocity profile and the vortex between section interfaces with varying tapering angles as shown in Figure 6.1. On the contrary, flow with low Reynolds number will create dead zone in a channel shaped like that in Figure 6.2. The dead zones will not contribute to thermal efficiency, and in fact it will waste the space. In the case of channel with longer section lengths, the channel will provide a high heat transfer rate while increasing the pressure drop. From the simulation result, the overall pressure drop was higher by one order of magnitude for a 2 mm channel with varying sections from 400 µm at the inlet to 100 µm at the outlet in funnel fashion. One can create base models with two section pairs with a combination of converging, diverging and straight to create convex, concave, or arbitrary shapes to incorporate an effect on the changing interfaces. Then, the correlation can be added as a weighted value with the coefficient being the number of specific transitions in the channel design.

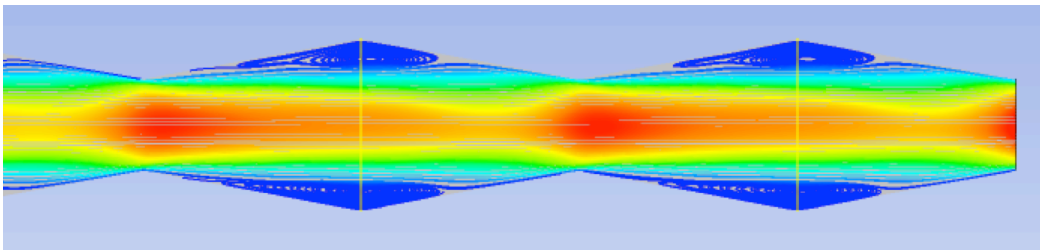


Figure 6.1: Creation of vortex on curved channel corner with high Reynolds number [69].

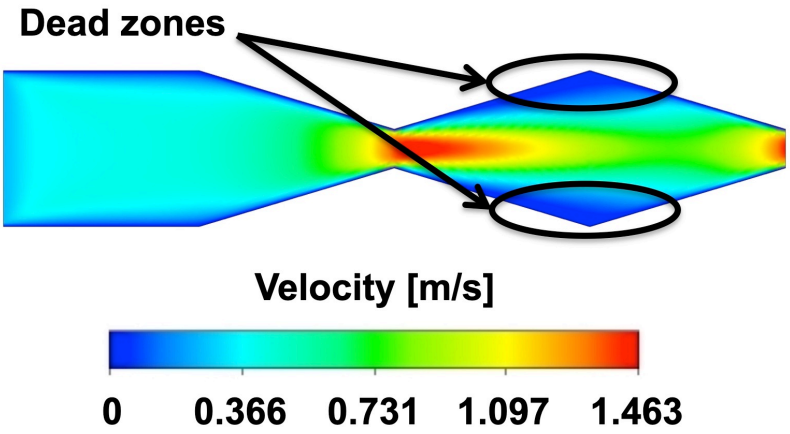


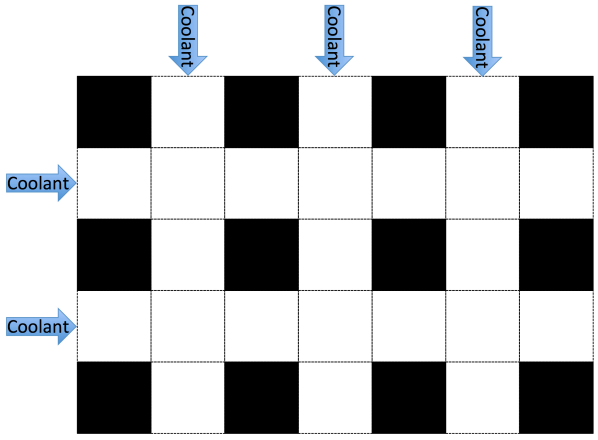
Figure 6.2: Creation of dead zone on curved channel corner on low Reynolds number.

6.2.2 Microchannel Network

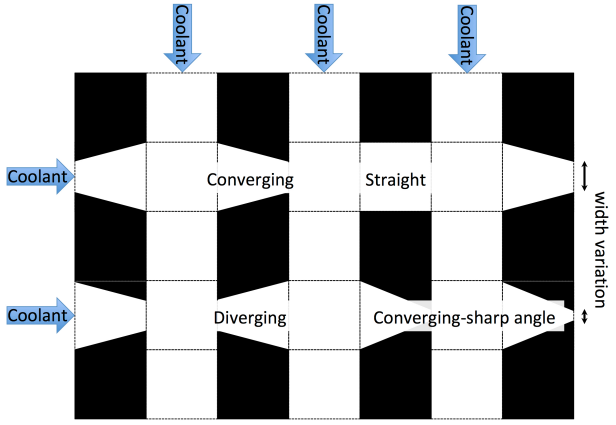
Depending on the chips with multiple hotspots, uniform channels throughout all locations of the chip may be very inefficient. Some locations may require more effective heat transfer whereas some locations may not. Microchannels placed on non-hotspots can potentially trade off the heat transfer efficiency and reduce the pressure drop to save cooling power. Moreover, straight microchannels have been facing challenges with large thermal gradient which affects the circuit performance.

With regard to the necessary design factors, we can apply our models into more complicated channel geometry optimizations. One of the high-performance cooling designs is a microchannel network in a full grid, both horizontal and vertical connections. The distance between the neighboring intersecting points will be the pitch, and can also be defined as segment length. Optimization algorithm can iteratively traverse every horizontal and vertical segment and alter the design to meet the specific needs of that location. A design example is shown in Figure 6.3. A grid with uniform width microchannel is shown in Figure 6.3a. Inlets are fixed to the left and top boundaries in this example. In future work, one can plan to fix the location of inlets and outlets and exclude them from the optimization parameters. Previous work has studied the arrangement of inlets and outlets [70] but this

is beyond our focus on optimizing the channel shape. Figure 6.3b shows an example of how each section can result in altered shape. There are three main geometries: 1) straight, 2) tapered converging and 3) tapered diverging. Furthermore, the tapering angle can be precisely controlled for each converging and diverging channel to maximize the objective while meeting the constraints.



(a) Microchannel network grid



(b) Example of optimized microchannel network

Figure 6.3: Microchannel network with uniform width and tapered wall comparison.

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