DEVELOPMENT OF AN OPTICAL NOR GATE TRANSISTOR LASER INTEGRATED CIRCUIT

BY

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DISSERTATION

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ABSTRACT

The transistor laser combines the intrinsic switching property of a bipolar transistor and the coherent light output of a laser in a single device, making it uniquely suited for electro-optical integration. Furthermore, with the addition of waveguide structures, a transistor laser integrated circuit is well suited for monolithic logic processing using on-chip optical interconnects. Although there are still many challenges to overcome both on the device level and the integration level, a transistor laser integrated circuit can be an attractive alternative to conventional electrical integrated circuits based on complementary metal-oxide-semiconductor (CMOS) technology. The subject of this work is the design, process development, and fabrication of a transistor laser integrated circuit in the form of an optical NOR gate to demonstrate optical logic processing using the transistor laser. This work begins with a brief introduction to optical logic processing and why the transistor laser is ideal for this application. Details of the development of a high-speed GaAs photodiode are given to supplement the original transistor laser process with a vertically illuminated optical receiver. The development of the transistor laser optical NOR gate is described, including the design and operating principle as well as the two rounds of fabrication. The methods used to characterize the optical NOR gate are reported, followed by a discussion of the results. Finally, the work is summarized and future improvements to the current process as well as next generation transistor laser integrated circuit concepts are proposed.

To my family

ACKNOWLEDGMENTS

I would like to thank my advisor, Professor Milton Feng, for the opportunity to work in the High-speed Integrated Circuits (HSIC) group and for his continuous support and guidance throughout my graduate school career. I would also like to thank the Pao Family Fellowship for their support. I am grateful for the mentoring from former HSIC students, Dr. Huiming Xu, who taught me semiconductor device fabrication techniques when working on the InP double heterojunction bipolar transistor (DHBT), and Dr. Eric Iverson, who recruited me and taught me about microwave measurements and small-signal modeling. I am also thankful for all the help and support from current and former HSIC group members Dr. Rohan Bambery, Dr. Mong-Kai Wu, Dr. Fei Tan, Dr. Curtis Wang, Yu-Ting Peng, Hsiao-Lun Wang, Dufei Wu, and Wenning Fu. I have relied heavily on their thoughtful suggestions, discussions, and assistance over the years. Special thanks go to HSIC members Dr. Xin Yu for his processing input and contributions in the back-end processing of the optical NOR gate as well as Junyi Qiu for his help in the characterization of the optical NOR gate and simulation of transistor laser integrated circuits. I would like to thank the staff at the Micro and Nanotechnology Laboratory who have helped me greatly through my Ph.D. career, especially Dr. Edmond Chow, Ken Tarman, and Clay Childers. Last but most importantly, I would like to thank my family for their never-ending love, support, and encouragement. I would not be the person I am today if not for them.

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1. INTRODUCTION

1.1 Optical Logic Processing and Current Technology

Since its invention by Bardeen and Brattain [1], the transistor has become the backbone of nearly all electronic devices. Specifically, silicon CMOS technology [2] in the form of an electrical integrated circuit (IC) is the fundamental building block of all electronics and logic processors. Until 2003, conventional gate scaling of CMOS has allowed the doubling of the transistor count in an IC every two years in accordance with Moore's Law, resulting in a steady increase in IC speed, efficiency, and cost reduction. Going to sub-40 nm gate lengths, additional innovations such as high-K gate dielectrics [3] and FinFETs [4] were required due to the device performance degradation that comes with further CMOS scaling. Although scaling in this non-traditional manner has allowed CMOS technology to largely follow Moore's prediction up until 2017, it is accompanied with increasing wafer cost due to increased process complexity [5].

Another disadvantage for CMOS technology in terms of data rate scaling comes from the use of metal interconnects. As the operating frequency of circuits get higher, the conventional metal electrical interconnect experiences major problems in terms of loss, crosstalk, and reflections [6]. This problem is well known and is the main reason why optical interconnects in the form of optical fiber links are used in applications where very long distance or high-speed data transmission is necessary. In computing applications, optical interconnects have been constrained to the board-to-board or rack-to-rack level in high-performance computers (HPCs) and data centers. On-chip optical interconnects have

been demonstrated commercially, but mostly in long-haul applications in large-scale photonic integrated circuits (PICs) such as by Infinera [7, 8].

The prospect of on-chip optical interconnects for logic processing applications is currently hindered by the fact that in all current logic processing applications, the optical interconnect is composed of discrete transmitter and receiver modules. Extra resources are required to interface with the logic processor, which is usually implemented on a separate chip. In order to bridge the gap between current PICs and CMOS ICs, a device that can directly process optical signals efficiently is required. Previous attempts to realize such a device include logic gates based on optical interference phenomena in waveguides using microring resonators, semiconductor optical amplifiers (SOAs), electro-absorption modulators (EAMs), and Mach-Zender modulators [9, 10]. The major disadvantage of these devices is their large size, which limits their integration potential. Semiconductor-based optical logic gates have also been demonstrated. A laser-photothyristor implementation [11, 12] achieved monolithic logic operation, but has extremely slow switching speed, typically in the MHz range. This fundamental limitation is due to the saturated nature of the p-n-p-n switch, which accumulates a large amount of charge in the base and can take a long time to turn off. Another demonstration is a cascadable laser logic device [13] which uses a diode laser grown on a phototransistor, creating a p-i-n-p-n structure. The cascadable laser logic device suffers from a very complex layer structure, resulting in extremely complex device fabrication that is not suitable for large-scale integration.

1.2 Transistor Laser Fundamentals

The transistor laser, invented by Feng and Holonyak [14, 15], is based on an n-p-n heterojunction bipolar transistor (HBT) with a quantum well in the base and an optical cavity for transistor base stimulated recombination process and coherent light output. Unlike a diode laser which traps carriers in the quantum well (QW) active region, the transistor laser has a tilted charge distribution due to the HBT-like operation. A comparison of the charge distribution is shown in Fig. 1. Carriers that are slow to recombine, instead of waiting in the QW like in a diode laser, get swept by the electric field towards the collector. Without the carrier "pile-up" effect, the recombination lifetime of the transistor laser is in the picosecond range compared to the nanosecond range for the diode laser. The short recombination lifetime enables high optical modulation bandwidth [16]. Using base current modulation, transistor laser devices have

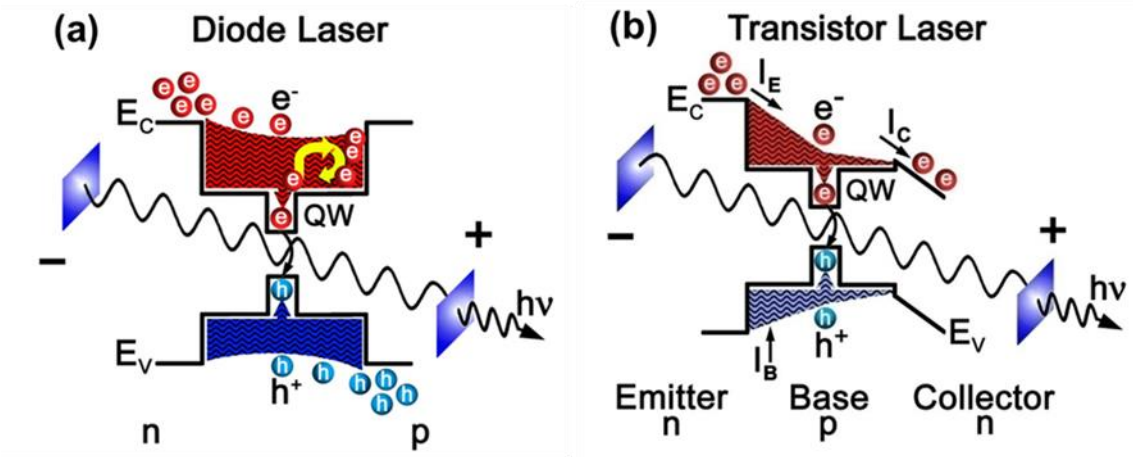


Figure 1. Charge distribution in (a) a diode laser and (b) a transistor laser. The tilted charge profile in a transistor laser causes a short recombination lifetime in the base, enabling high-speed modulation.

demonstrated simultaneous electrical and optical output at 20 and 40 Gb/s [17].

1.3 Tunneling Modulation of the Transistor Laser

A unique characteristic of the transistor laser is the dependence of the light output on base-collector junction reverse bias. This phenomenon gives the transistor laser two distinct advantages. First, it enables pure voltage modulation of the light output, which is not possible in a diode laser. Second, collector voltage modulation potentially holds the key to extend the bandwidth of the transistor laser even more, since it is based on a very fast tunneling process.

To understand the mechanism behind the tunneling modulation of a transistor laser, it is helpful to consider the excess carrier distribution in the base of a transistor laser shown in Fig. 2 [18]. Electron injection from the emitter forms the emitter current I_{En} with a triangular tilted charge distribution Δn_1 and Δp_1 due to the boundary condition set by the base quantum well and the base-collector junction. Electrons that recombine inside the base form the primary base recombination current I_{r1}, and electrons that diffuse to the base-collector junction will then drift towards the collector and form the primary base transport current I_{t1}. Meanwhile, electrons in the base tunnel towards the collector assisted by photons inside the cavity, called intra-cavity photon-assisted tunneling (ICPAT). The tunneling electrons form the tunneling current I_{ICPAT} and leave an excess hole concentration Δp_2 in the base. The charge is compensated by the electron concentration Δn_2 through dielectric relaxation with an approximated time constant of 4.9 fs. Diffusion of Δn_2 near the base-collector junction forms the secondary base transport

current I_{t2}, and diffusion near the quantum well forms the secondary stimulated base recombination current I_{r2}.

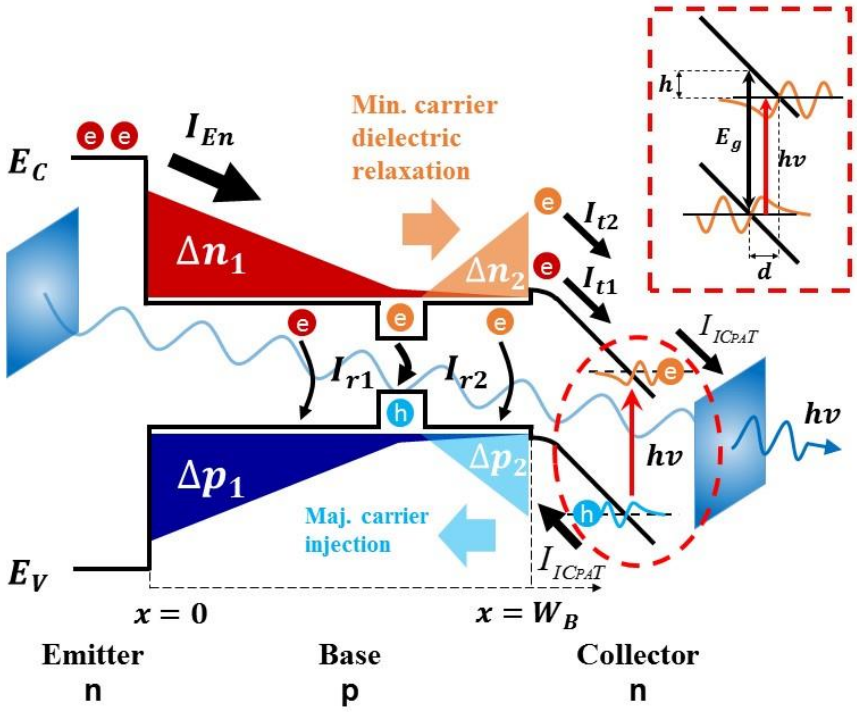


Figure 2. Excess carrier distribution in the base of a transistor laser with ICPAT [18].

A typical L-I-V curve for a transistor laser with ICPAT is shown in Fig. 3. When the device is biased with I_B above the lasing threshold, high collector-emitter bias voltage leads to increased tunneling probability, resulting in reduced light output with simultaneously increased collector current. This direct voltage dependence, along with the conventional base current modulation of the transistor laser, adds a degree of freedom in the design of an electro-optical or all-optical integrated circuit. Moreover, the non-parasitic limit of the collector voltage modulation is dictated by the tunneling process and

dielectric relaxation, both faster than the recombination lifetime limit of base current modulation. So far, collector modulation has shown error-free operation at 13.5 Gb/s [19].

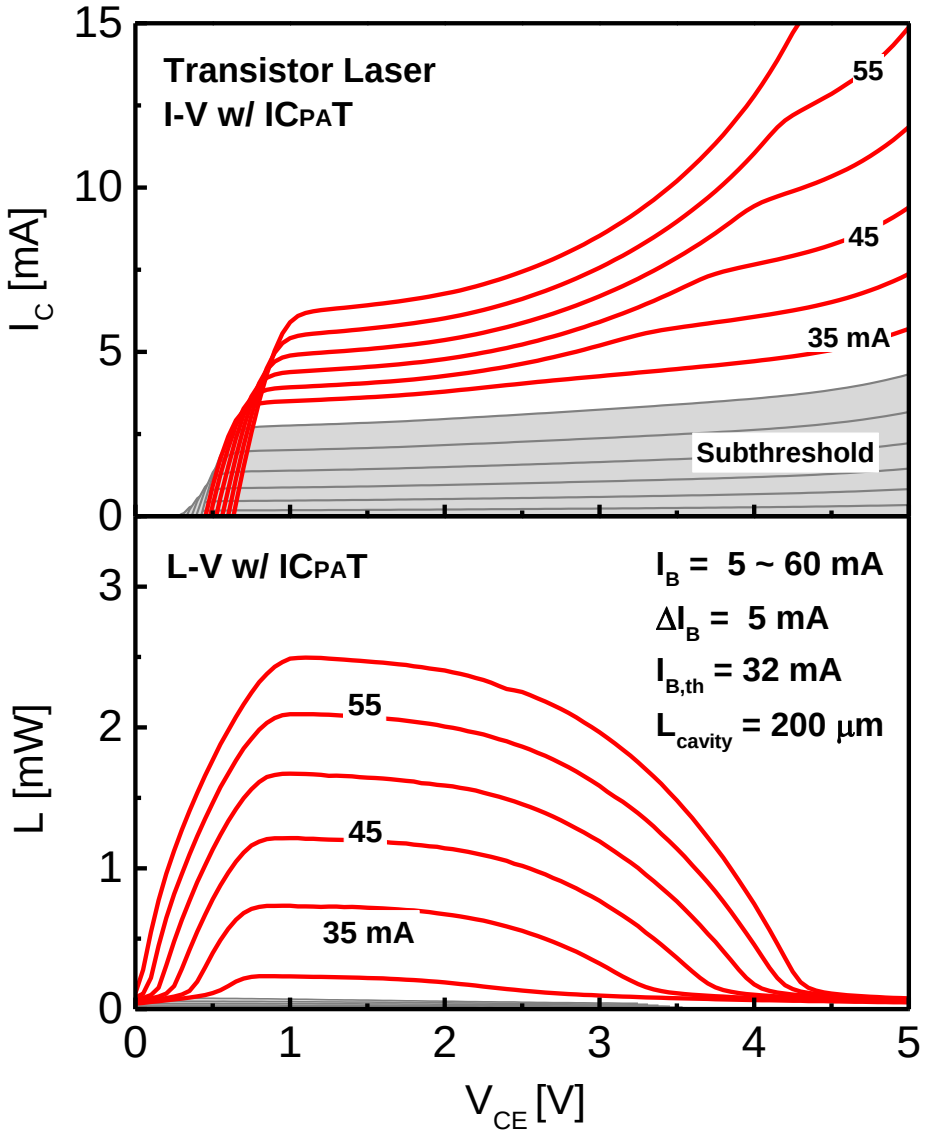
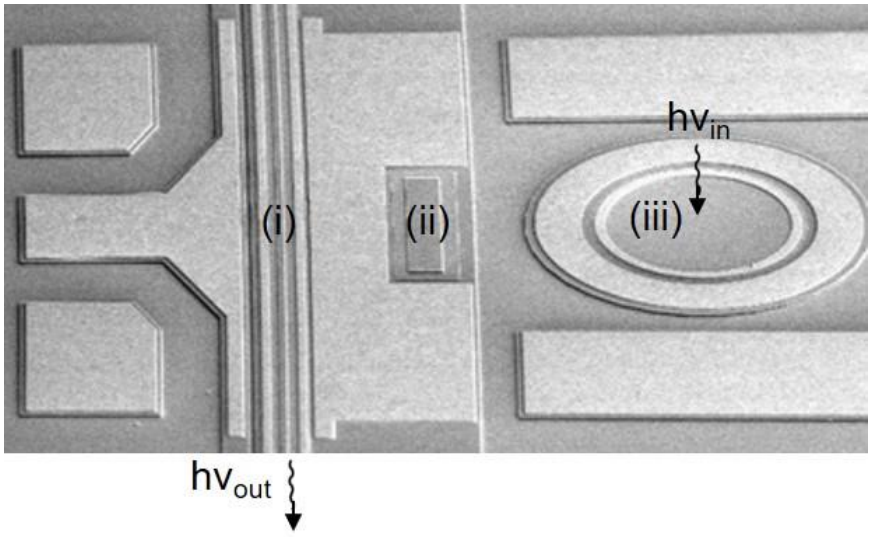


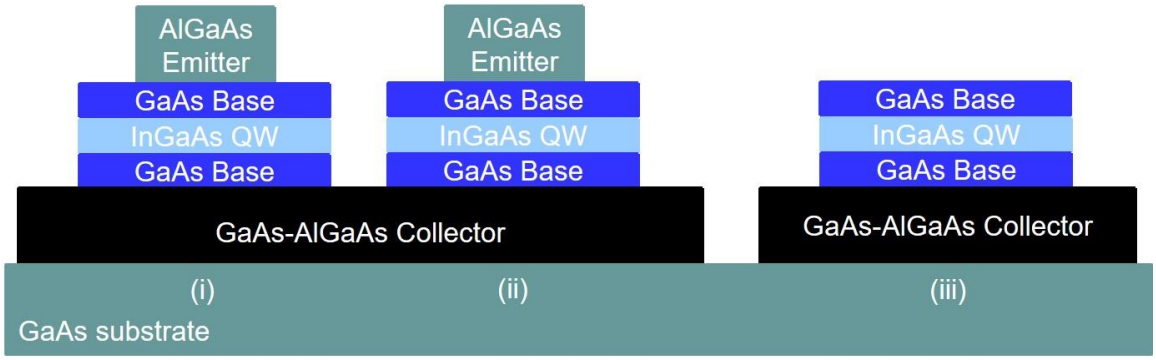
Figure 3. Typical L-I-V curves of a transistor laser with ICPAT. Above threshold, the transistor laser shows reduced light output and increased collector current at high collector bias.

1.4 Transistor Laser Integrated Circuit for Optical Logic Processing

The use of the transistor laser for optical logic processing has been previously proposed [20]. Compared to transistor ICs technologies such as CMOS or BiCMOS, the transistor laser possesses two innate advantages for electro-optical integration. First, unlike a diode laser, the transistor laser light output can be modulated without an external driver, which greatly reduces the complexity of the transmitter circuitry. Second, the epitaxial layer structure readily contains both an optical transmitter as well as regular transistor since the transistor laser can be operated as a normal HBT. An optical receiver can be implemented using an additional intrinsic layer or using the base-collector junction of the transistor laser. An example of a transistor laser integrated circuit is illustrated in Fig. 4. Passive elements such as optical waveguides can also be defined using more advanced techniques to allow for a purely monolithic PIC.



(a)



(b)

Figure 4. Top view (a) and cross-section diagram (b) of a transistor laser integrated circuit containing a transistor laser with an optical cavity and cleaved facets (i), and HBT without an optical cavity (ii) and a vertical PIN photodiode (iii).

Using voltage modulation of the light output, an all-optical logic device gate on the transistor laser can potentially be more efficient than a conventional CMOS logic gate. The delay for a typical CMOS logic gate can be expressed as follows [21]:

$$\tau_{MOS} \sim \frac{C_g V_{dd}}{K(V_{dd} - V_t)^a}$$

where C_g is the gate capacitance and V_{dd} is the supply voltage. K, V_t, and a are CMOS process-dependent parameters. The power dissipation can be expressed below, assuming maximum clock rate equal to the inverse of the delay:

$$P_{MOS} = C_g \times {V_{dd}}^2 \times clock\ rate \sim \frac{C_g {V_{dd}}^2}{\tau_{MOS}}$$

The energy-delay product (EDP) for the CMOS logic gate can be approximated as:

$$E_{MOS} \times \tau_{MOS} = (P_{MOS} \times \tau_{MOS}) \times \tau_{MOS} \sim \frac{{C_g}^2 {V_{dd}}^3}{K(V_{dd} - V_t)^a}$$

Assuming K, Vt, and a are uncontrollable processing parameters, smaller gate capacitance and supply voltage are required for lower EDP. Reducing gate capacitance and supply voltage can typically only be done by scaling the area of the MOS transistor or by introducing processing changes.

In the case for a transistor laser optical NOR gate, the delay can be expressed as:

$$\tau_{TL} = \frac{C_{TL2} \Delta V}{I_{C2}}$$

C_{TL2} is the capacitance and I_{C2} is the collector current for the output TL. ΔV is the voltage swing required to turn off the light output of the TL. K, V_t,

The power dissipation can be expressed as follows:

$$P_{TL2} = I_{B2}V_{B2} + I_{C2}V_{C2}$$

I_{B2}, I_{C2} and V_{B2}, V_{C2} are the base and collector currents and voltages, respectively. The EDP can be expressed as follows:

$$E_{TL} \times \tau_{TL} = (P_{TL2} \times \tau_{TL}) \times \tau_{TL} = (I_{B2}V_{B2} + I_{C2}V_{C2}) \frac{{C_{TL2}}^2 \Delta V^2}{{I_{C2}}^2}$$

and can be rewritten in terms of the TL electrical gain β:

$$E_{TL} \times \tau_{TL} = \left(\frac{V_{B2}}{\beta} + V_{C2}\right) \frac{{C_{TL2}}^2 \Delta V^2}{I_{C2}}$$

We see that the EDP can be decreased with an increase in I_{C2} and β and using a small voltage swing ΔV. Therefore, the scaling potential for the transistor laser optical NOR gate is limited not only to the scaling of the device. Additionally, the transistor laser process can also integrate electrical functions based on an analog bipolar process, making it ideal for mixed-signal applications.

2. DEVELOPMENT OF HIGH-SPEED PIN PHOTODIODE

2.1 Introduction

In order to form an optical logic gate using the transistor laser, a photoreceiver first needs to be implemented. The transistor laser epitaxial structures in previously reported work [17, 19] do not inherently contain a photoreceiver, but the depletion region in the base-collector junction can act as a PIN photodiode. Due to the epitaxial constraints in the photosensitive region, a vertically illuminated photodiode structure is likely to be required to avoid light coupling issues. In order to define the fabrication and testing methodology, a high-speed GaAs PIN photodiode was designed, fabricated, and characterized. The specific design goal of the PIN photodiode is to function in conjunction with a high-speed oxide confined vertical cavity surface-emitting laser (VCSEL) [22, 23] in an optical fiber link with data rates up to 50 Gb/s. Therefore, the target design bandwidth is 25 GHz with maximum responsivity. Two types of photodiodes were fabricated. Photodiode A is a conventional PIN photodiode with a 0.75 μm thick intrinsic region, while photodiode B is similar to photodiode A but with a 15-pair AlGaAs distributed Bragg reflector (DBR) mirror to enhance light absorption.

2.2 High-speed GaAs Photodiode Design

Figure 5 shows a typical PIN photodiode operated in reverse bias, creating a constant electric field in the intrinsic region which acts as a light absorption layer. When light is

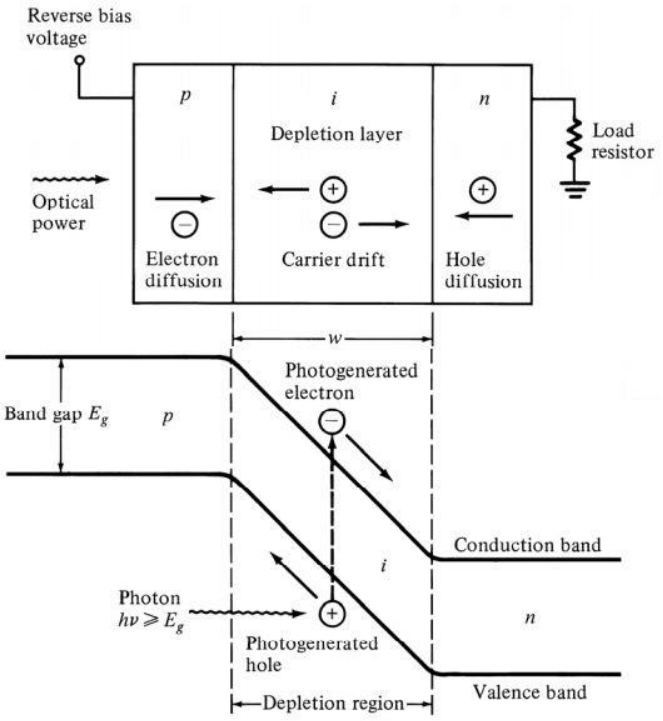


Figure 5. Diagram of a typical PIN photodiode operating in reverse bias.

incident on the photodiode, carriers are optically generated in the intrinsic region and swept towards the contacts by the electric field, generating a photocurrent. There are two main limiting factors to the high-speed operation of the photodiode: RC charging delay and transit time. The RC-limited bandwidth of a PIN photodiode can be expressed as follows:

$$f_{-3dB,RC} = \frac{1}{2\pi(R_S + R_L)(C_P + C_j)}$$

R_S is the series resistance of the photodiode, R_L is the load resistance, C_P is the parasitic pad capacitance, and $C_j = \frac{\epsilon A}{T}$ is the junction capacitance of the photodiode with area A and intrinsic region thickness T. The transit time is defined as the delay before an

optically generated carrier is collected at the contacts and forms the photocurrent. The transit-limited bandwidth of a photodiode was calculated by Lucovsky et al. [24]:

$$f_{-3dB,transit} = \frac{0.45T}{v_{sat}}$$

T is the intrinsic region thickness and is v_{sat} is the average carrier saturation velocity.

From the two delay components, it can be concluded that the critical parameter for high-speed PIN photodiode design is the thickness of the intrinsic region. Following the method in [25, 26], the two bandwidths can be combined into a total bandwidth. Plotting the constant bandwidth contours against the device dimensions creates the design curve shown in Fig. 6. For a given diode mesa diameter, a specific intrinsic region thickness results in a maximized bandwidth, following a "line of optimum bandwidth." For 50 Gb/s operation, f_{-3dB} of approximately 25 GHz is required. Following the design curves, the optimum photodiode dimensions are $T = 0.75\ \mu m$ and aperture diameter $R = 20\ \mu m$.

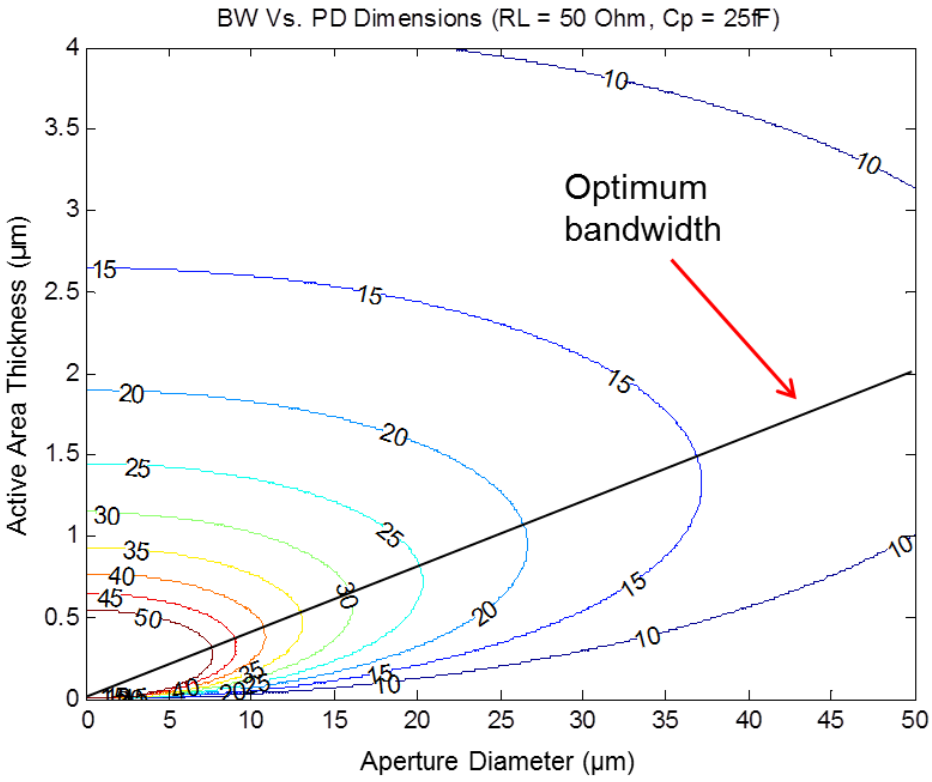


Figure 6. 3-dB bandwidth contours of a PIN photodiode plotted against active area thickness and aperture diameter [25].

The intrinsic region thickness requirement $T = 0.75\ \mu m$ for the 25 GHz design goal poses a challenge because it only allows about 45% of light to be absorbed in the intrinsic region, resulting in low responsivity. If a receiver with better performance is desired, a commonly used technique is to integrate a high-gain transimpedance amplifier (TIA) to boost the overall responsivity. In this work, we attempted to boost the internal responsivity of the photodiode by adding a reflective bottom AlGaAs DBR mirror. The mirror reflects incoming light back towards the intrinsic region, effectively extending the thickness of the absorption layer. Two assumptions are made: first, subsequent reflections on the top AlGaAs-air interface and the bottom intrinsic GaAs-DBR interface are ignored

due to the exponential decay of light intensity as it travels through the absorption region. Second, any delay terms associated with photogenerated carriers from the secondary (reflected) are taken into account in the derivation of photodiode transit time [24] as the 1.5 μm "effective" thickness of the intrinsic region is still much larger than the photon wavelength.

2.3 High-speed PIN Photodiode with 25 GHz Bandwidth

This section explains the fabrication process development and characterization of a PIN photodiode with 25 GHz −3dB bandwidth [27, 28]. The epitaxial wafers are grown by MOCVD and consist of a bottom n-type GaAs contact, a 0.75 μm undoped GaAs absorption region, and an $Al_{0.2}Ga_{0.8}As$ p-type contact layer. Photodiode B includes a 15-pair AlGaAs DBR mirror below the absorption region. The $Al_{0.2}Ga_{0.8}As$ layer also acts as a large-bandgap optical window, allowing most of the incoming light to penetrate and reach the intrinsic absorption region. With the GaAs absorption region and the $Al_{0.2}Ga_{0.8}As$ optical window, the photodiodes are sensitive to light between 700 nm and 870 nm wavelengths.

The device structure consists of a circular mesa to define the photodiode area, and the fabrication process is very similar to a high-speed oxide confined VCSEL [22, 23]. First, a ring Ti/Pt/Au p-type contact is deposited on the top $Al_{0.2}Ga_{0.8}As$ layer, followed by plasma-enhanced chemical vapor deposition (PECVD) SiNx deposition on the whole wafer surface. A dry etch mask for the device mesa is defined by optical lithography and etched using CF_4 RIE. The device mesa is then etched using BCl_3 in an Oxford ICP-RIE.

The etch recipe is very carefully tuned to get a smooth vertical sidewall with minimal etch foot. The amount of overetch into the n-type GaAs layer potentially increases the dark current of the photodiode as the vertical sidewall is subjected to more dry etching [27]. However, spatial non-uniformity of the etch rate means that a certain degree of overetch is required to ensure that all devices on the wafer have good n-type contact. Next, a AuGe/Ni/Au contact is deposited on the n-GaAs and alloyed at 380 °C to form the bottom n-type contact. Since some of the devices are designed to function in arrays, each device is isolated using a second round of dry etch with a PECVD SiNx mask. In order to lay down contact pads without causing a short, the devices are then planarized using bencozyclobutane (BCB) and then etched back using SF_6 / O_2 RIE to expose the aperture and p-type contact. A via is defined using optical lithography with a reflow process to attain a gradual slope, then opened using SF_6 / O_2 RIE. Ti/Au contact pads are deposited followed by deposition of a SiNx anti-reflective coating. A cross-sectional sketch and top view of the completed photodiode are shown in Fig. 7.

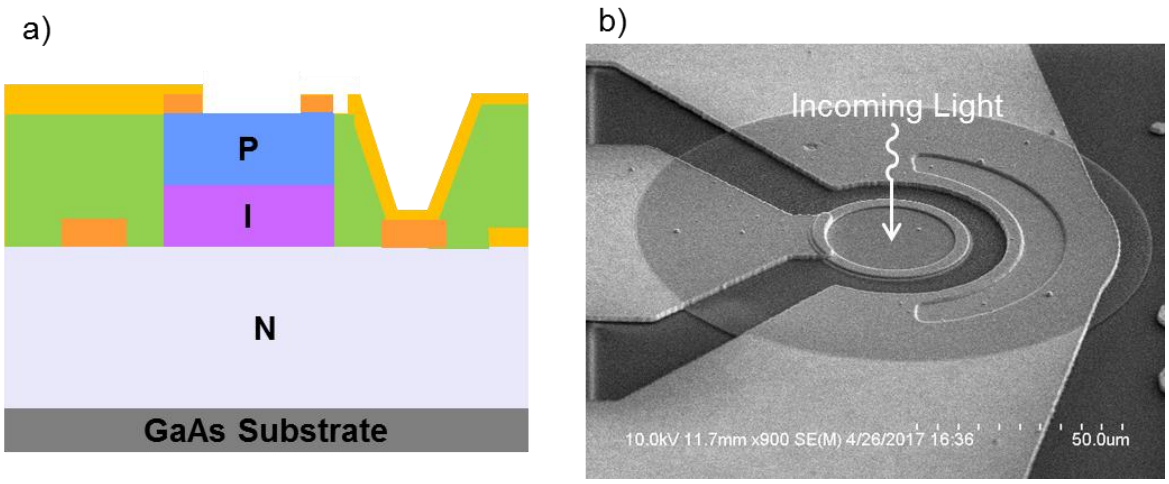


Figure 7. (a) Cross-sectional view of photodiode A and (b) top view of a completed photodiode.

The PIN photodiodes are characterized using three metrics: dark current, responsivity, and bandwidth. The dark current is defined as the measured current when the diode is reverse biased with no optical input. The measurement is done with a DC probe station with tungsten probes inside a dark box to block incoming light. An Agilent E5270B with E5287A stimulus and measurement units (SMUs) is used to measure the I-V curve. Photodiodes A and B show similar dark current values of around 0.1 nA at 4 V reverse bias. A typical dark current plot showing data from 1 × 4 arrays of photodiodes is shown in Fig. 8.

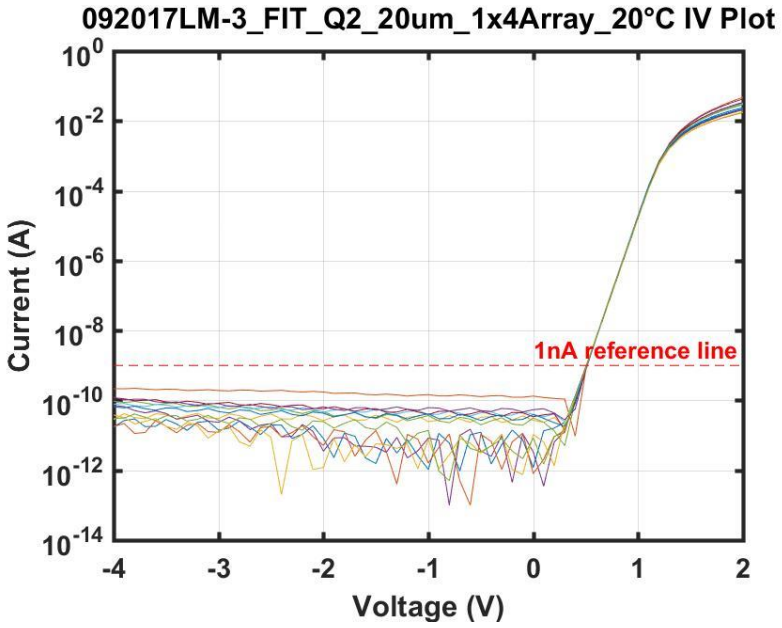


Figure 8. Plot of photodiode dark current measured from 1 × 4 arrays.

The equipment setup to measure the responsivity and bandwidth is shown in Fig. 9. An oxide confined VCSEL fabricated at the University of Illinois with known −3dB bandwidth > 25 GHz from [22, 23] driven by an Agilent 4142 power supply is used as the optical light source. The light is coupled to the PIN photodiode using a set of lightwave probes and optical fiber. The responsivity is defined as the ratio of photogenerated current in the PIN photodiode (in units of amps) over the incoming light (in units of watts). Since the light source is an on-wafer VCSEL driven by a power supply, the L-I relationship of the light source must first be established using an external calibration photodiode. Using the L-I curve (light output vs. VCSEL drive current in units of W/A), the raw measurement response of the PIN photodiode (photodiode response current vs. VCSEL drive current in A/A) can be converted into responsivity

(units of A/W). Figure 10 shows the responsivity data for the fabricated photodiodes, including theoretical limits for the responsivity for 850 nm light absorption in GaAs. The responsivity is lower for smaller mesa photodiodes due to incomplete coupling of the optical signal from the lightwave probe. It is shown that for a 30 µm mesa dimension, photodiode B has approximately 0.15 A/W more responsivity over photodiode A. However, as the responsivity becomes limited by the mesa diameter, the increase in responsivity becomes limited.

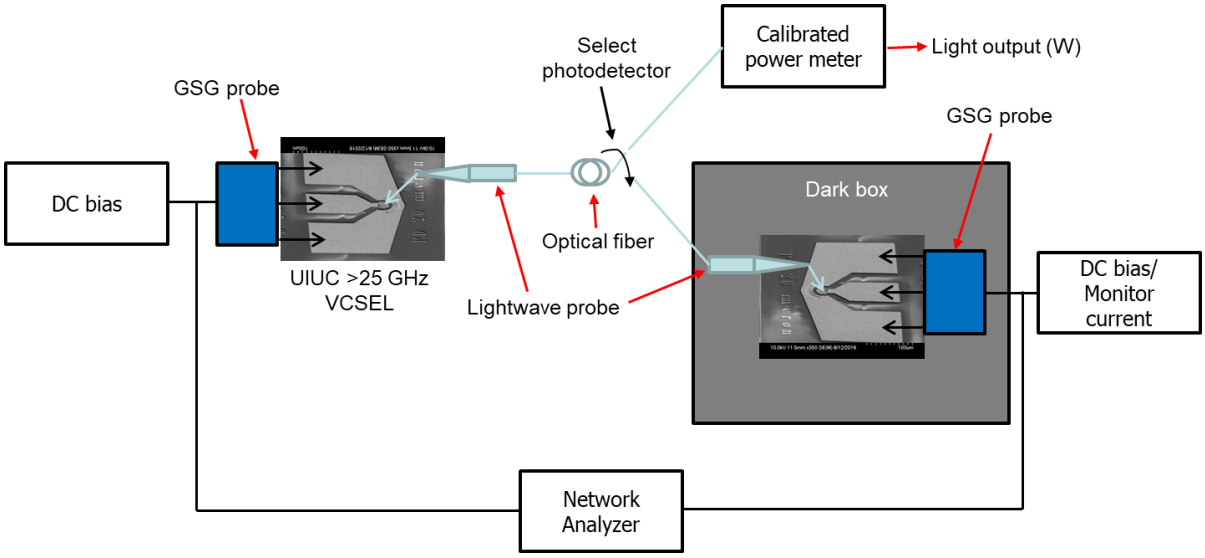


Figure 9. Measurement setup to characterize the responsivity and bandwidth of the PIN photodiodes.

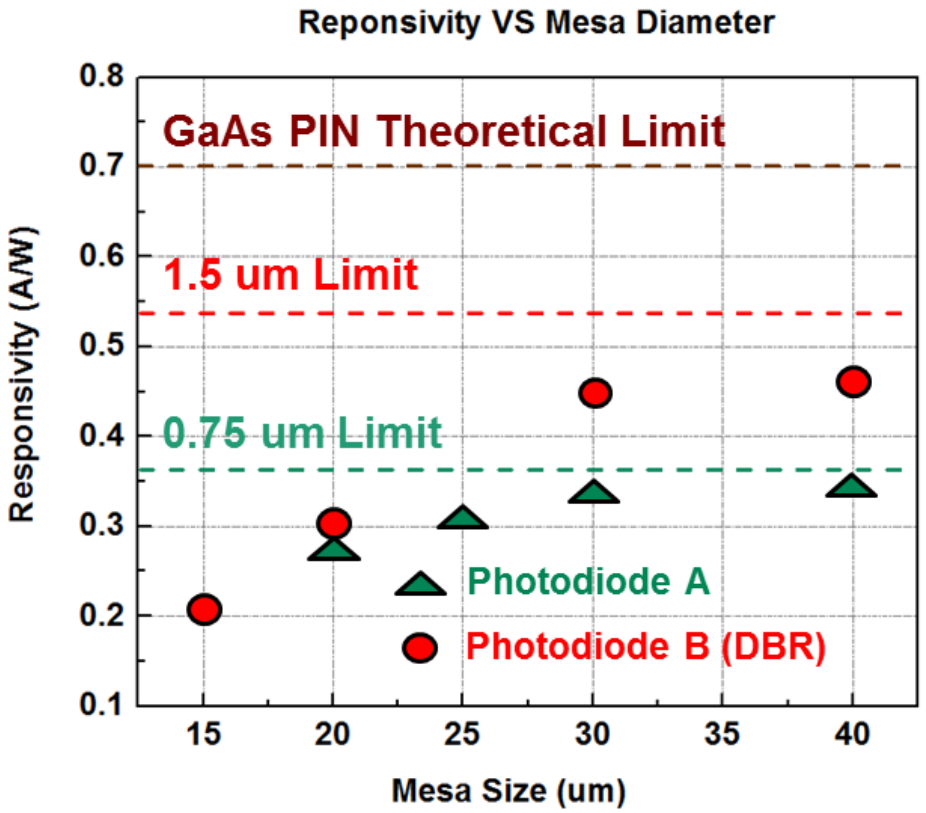


Figure 10. Responsivity data of photodiode A (green) and photodiode B (red) for various device mesa sizes. The theoretical responsivity limits based on 850 nm light absorption in GaAs for full and partial absorption of incident light (1.5 μm and 0.75 μm thickness) are included.

To measure the −3dB bandwidth of the photodiode, the same VCSEL-optical-fiber-photodiode optical link is used. This time, an Agilent N4527A PNA-X is used in conjunction with the power supply to modulate the VCSEL and receive the small-signal response from the photodiode. The measured S_{21} directly represents the bandwidth response of the whole optical link in arbitrary units. First, an optical link measurement is done using a calibrated photodiode with a known bandwidth response. Subtracting the photodiode response from the overall response gives the bandwidth response of the VCSEL as shown in the blue curve in Fig. 11. Switching the optical path to a 20 μm PIN

photodiode and measuring S_{21} gives the frequency response of the VCSEL–fiber–PIN photodiode as shown in the red curve in Fig. 11. The VCSEL response shows a −3dB bandwidth of 27 GHz while the optical link response shows a −3dB bandwidth of 25 GHz.

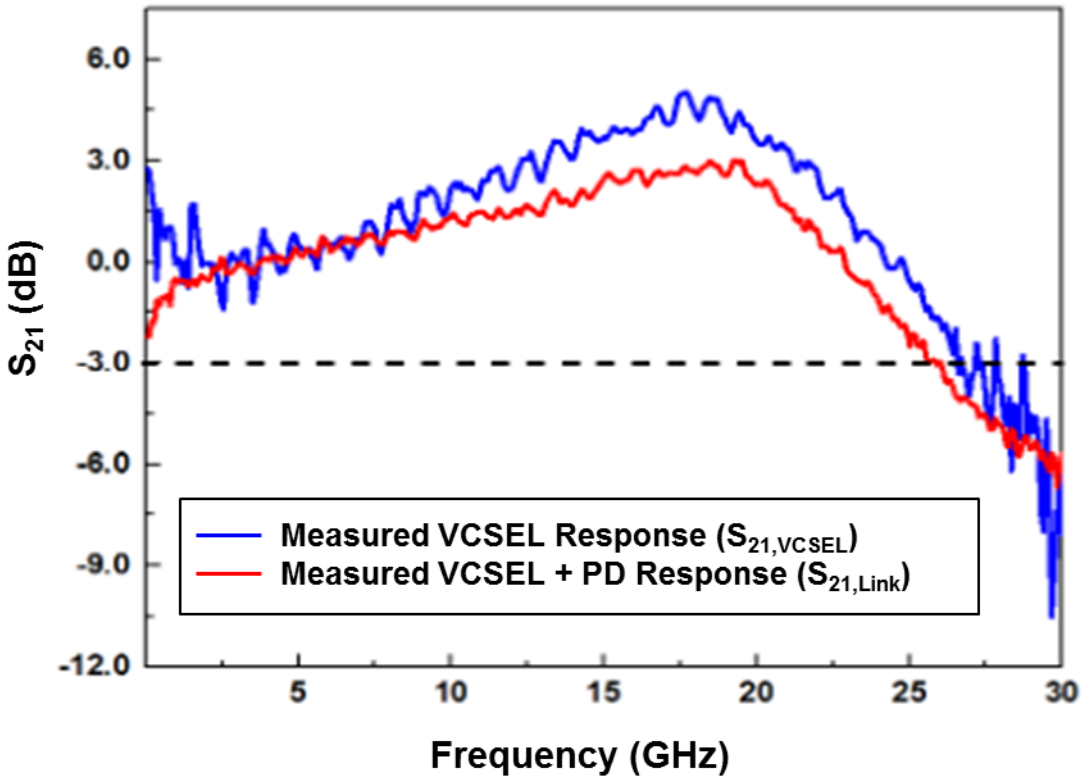
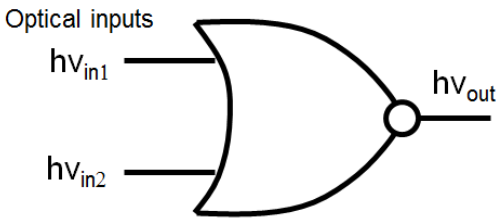


Figure 11. Frequency response curves taken from direct modulated S-parameter measurements. The VCSEL response (blue) is taken using a calibrated high-speed photodiode with the photodiode response calibrated out. The VCSEL + 20 μm PIN photodiode optical link response (red) shows slightly lower −3dB bandwidth.

3. DEVELOPMENT OF TRANSISTOR LASER OPTICAL NOR GATE

3.1 Design and Switching Mechanism

In order to demonstrate the logic processing functionality of a transistor laser integrated circuit, a NOR gate structure has been selected. A logic gate representation for the transistor laser optical NOR gate and the accompanying logic table are shown in Fig. 12. The NOR gate is a universal logic gate, meaning that with manipulation of Boolean algebra, any logic function can be realized using the NOR gate as a building block. This allows for more highly integrated designs incorporating the original NOR gate for future work. The transistor laser circuit that realizes this functionality is shown in Fig. 13.



hv$_{in1}$	hv$_{in2}$	hv$_{out}$
0	0	1
1	0	0
0	1	0
1	1	0

Figure 12. Logic gate representation and logic table of the transistor laser optical NOR gate.

The circuit consists of three transistor lasers divided into two branches, sharing a constant voltage supply V and resistor R. The right branch contains TL2, which acts as a normal transistor laser biased in forward active mode with a fixed base-emitter voltage to set the base current above threshold with constant collector voltage and collector current

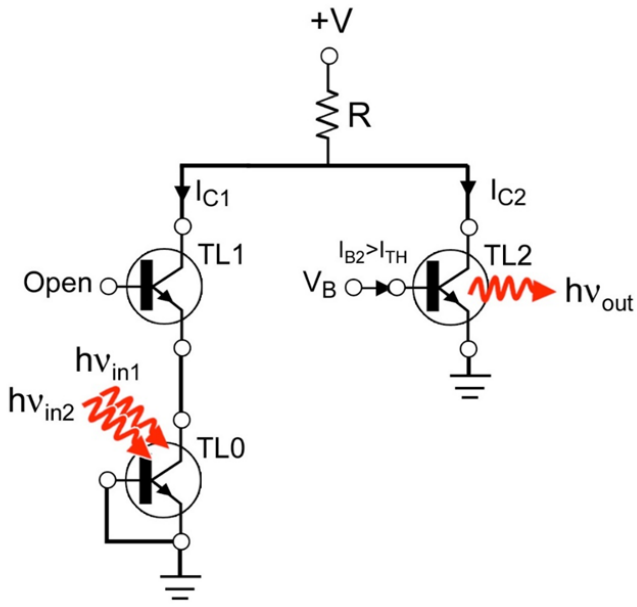


Figure 13. Circuit diagram for the transistor laser optical NOR gate. TL2 acts as a regular transistor laser, TL1 acts as an active load, and TL0 acts as a photodiode.

I_{C2}. The left branch provides the control structure to regulate the shared collector node voltage to switch the output of TL2. TL0 acts as a photodiode with its collector tied to the emitter of TL1, which acts as an active load.

The functionality of the optical NOR gate is explained as follows. In a logic "1" case, no optical input is applied to TL0. This causes no current to conduct on the left branch (I_{C1} = 0) and the right branch operates as a conventionally biased transistor laser. In a logic "0" case, a nominal optical input is applied to TL0. The resulting photocurrent sets the collector current I_{C1} of the left branch, inducing a nonzero collector-emitter voltage on TL1. The induced voltage causes the total voltage on the combined node to rise, increasing the collector-emitter bias of TL2. Due to the dependence of transistor light output on the base-collector voltage through ICPAT, the increase in collector voltage will

lead to a light output reduction in TL2. Illustrations for logic “1” and logic “0” operations based on the I-V characteristics of a tunnel junction transistor laser is shown in Figs. 14 and 15, respectively.

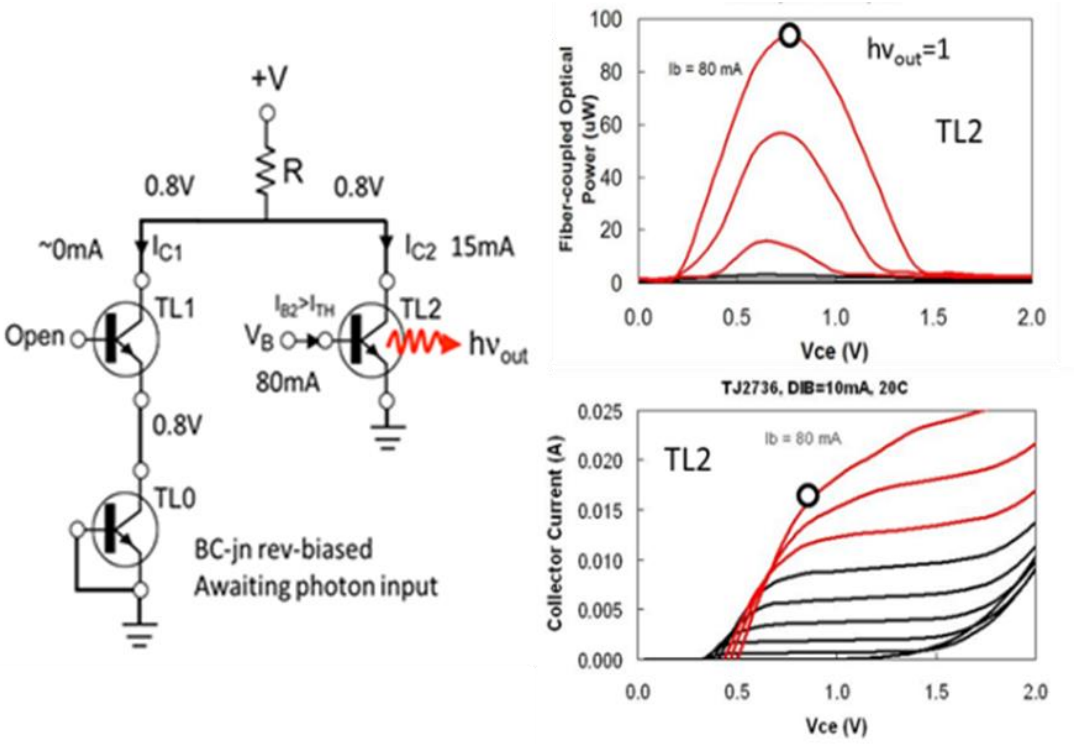


Figure 14. Logic “1” operation for the transistor laser optical NOR gate. With no optical input to the photodiode TL0, no current flows in the left branch and TL2 operates as normal.

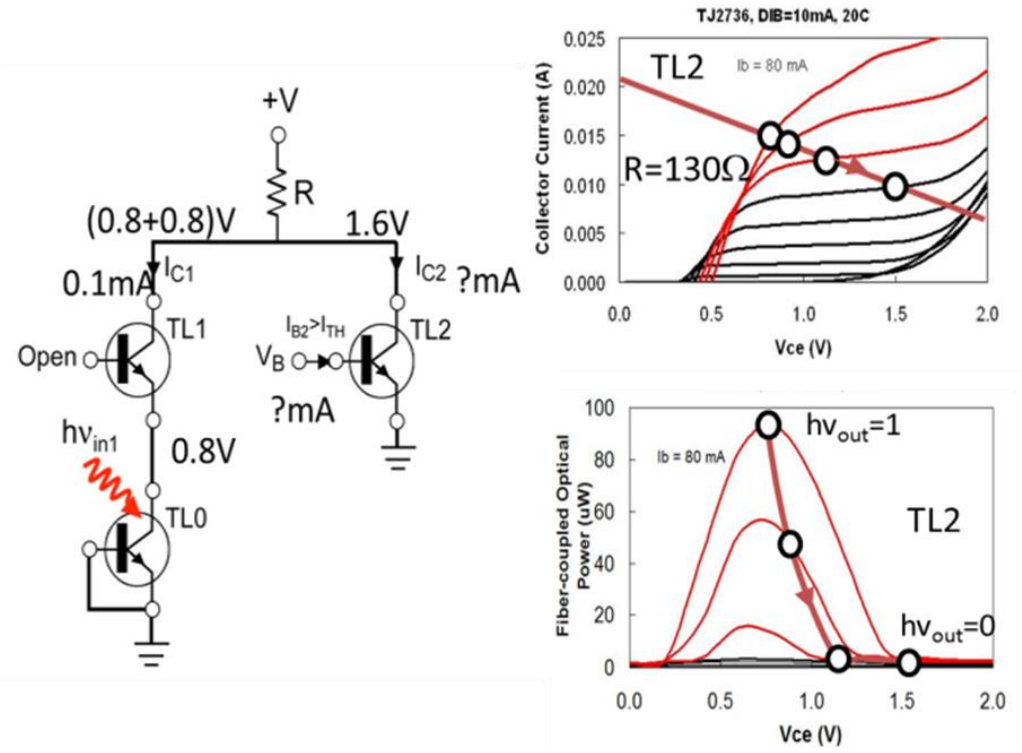


Figure 15. Logic "0" operation for the transistor laser optical NOR gate. When an optical input is present on TL0, the resulting photocurrent induces a collector-emitter bias on TL1, which increases the collector-emitter bias on TL2, thus turning off the light output (illustrated by red arrow).

The illustrations in Figs. 14 and 15 assume the case of a single continuous light input that allows the output transistor laser to completely turn off its light output. In digital applications, the input signal is bound between two "0" and "1" states. In addition, depending on specific transistor laser epitaxial structure and circuit design, it may not be possible to completely switch off the light output of the logic gate. In this case, the light output will fluctuate between determined output "0" and "1" states. In the case of the optical NOR gate, one of the benefits of this structure is multi-input logic operation in a relatively simple structure, especially compared to a similar NAND structure, which

would require a series cascade of photoreceivers, resulting in complicated interconnects. The drawback to the NOR structure for this circuit is the fact that considering all possible input combinations, for a two-input NOR gate, the light output will have three stable states, as shown in the simulated logic diagram in Fig. 16. Since the light output is further diminished with higher photocurrent, a logic "0" threshold needs to be defined for the single input case.

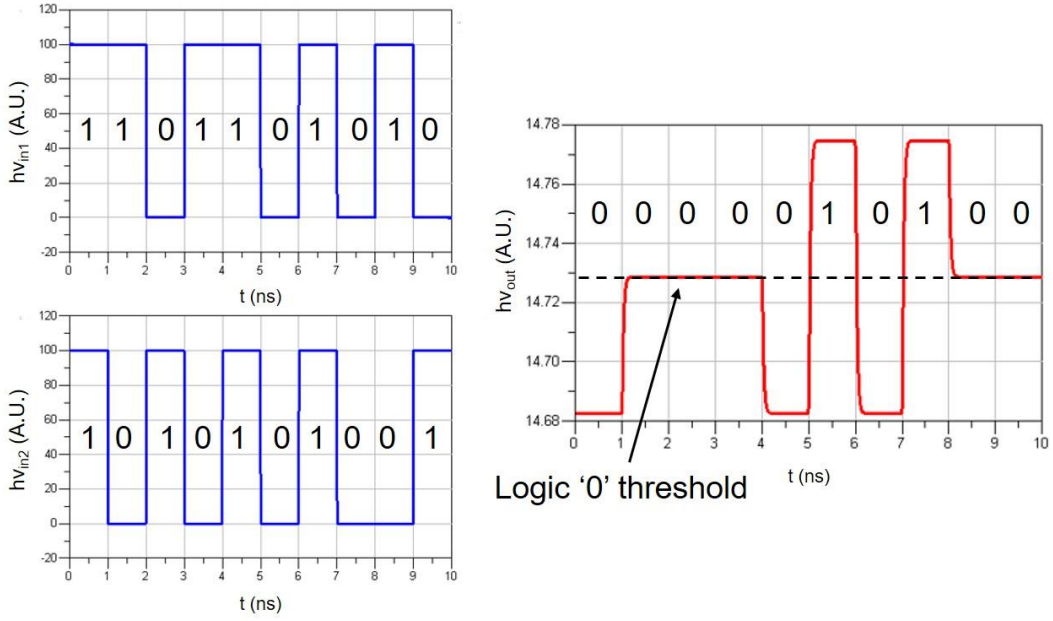


Figure 16. Simulated logic diagram for the optical NOR gate with two discrete inputs. With two "1" inputs, the output is diminished further and requires a set threshold for the logic "0" level.

Next, the design considerations for each circuit component are described. The first design parameter is the emitter dimensions of TL2. In order to provide a robust multimode laser output with a large tolerance to processing deviations, the emitter was set to a stripe of 5 × 400 μm. The base-emitter bias is kept constant to maintain the base current above the lasing threshold.

The next design step is to approximate the operation of TL0. For the epitaxial structure used in the fabrication process, the light absorption region in the base-collector junction is a 60 nm lightly doped GaAs layer. Following the exponential rule for light absorption, only about 5% of incoming light will be absorbed. Since the photodiode described in section 2.2 absorbs around 45% of incoming light, we can estimate the responsivity for the photodiode to be around 0.04 A/W. Assuming a nominal light input of 2 to 3 mW (which is easily attainable in our measurement setup), we can approximate the resulting photocurrent, and therefore I_{C1} is on the order of 80 to 120 μA.

The dimensions of TL1 are set by: 1) the current through the left branch I_{C1} and 2) the voltage swing required to turn off the output of TL2. Since TL2 in this process is a transistor laser without a tunneling junction, a high voltage bias is required to turn off the light output. Previous measurement data from a similar transistor laser process are used to estimate the zero-bias leakage current for TL1 (I_C vs. V_{CE} with $I_B = 0$). An emitter dimension of 20 × 100 μm for TL1 is used in this design in order to provide sufficient voltage swing for TL2.

Finally, the external voltage supply V and resistor R are parameters to be tuned during the measurement process. The two parameters combine together to set a collector-emitter bias and collector current for TL2 to maintain normal operation. The specific values will also set the load line for TL2, which determines the specific "off" state voltage of the transistor laser, as shown in Fig. 15.

The device layout implementation of the optical NOR gate is done in Agilent ADS and shown in Fig. 17 along with a cross-sectional view and the original circuit diagram.

A regular transistor laser shown in Fig. 18 for comparison. The layout for TL2 is similar to a normal transistor laser [17, 19] but with a slight modification. The ground-signal-ground (GSG) pad on the collector side of TL2 is replaced with a shared collector pad with TL1, which is a facet-less normal HBT with no base contact since it is operated in the open-base configuration. TL0 is implemented as a photodiode similar to that in section 2.2 with minor modifications to conform to the TL process flow. Additionally, a metal pad connects the emitter of TL1 to the collector (n-contact) of TL0. The aperture diameter of TL0 is set to be 100 µm for easy light coupling with a lightwave probe. The bandwidth of the TL0 photodiode is expected to be limited to the MHz range due to its large capacitance, so high-speed performance will not be a concern in this first iteration design.

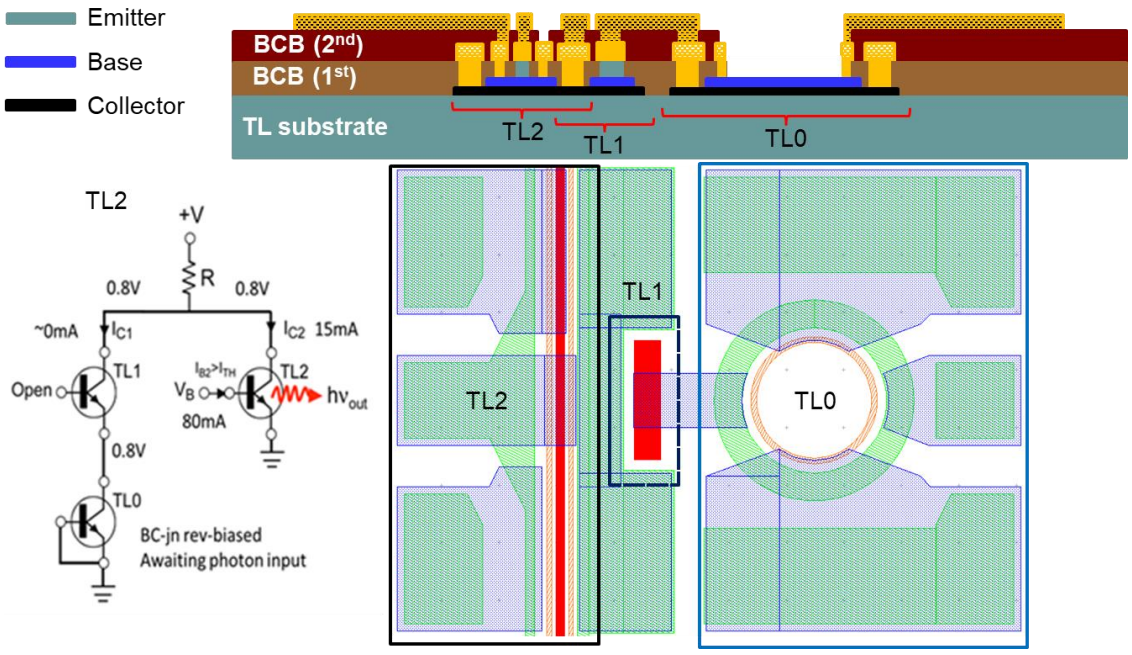


Figure 17. Cross-section and layout view of the transistor laser optical NOR gate.

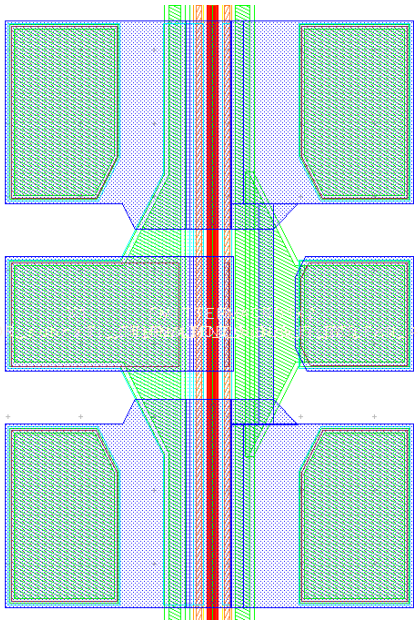


Figure 18. Layout for a regular 5 × 400 µm transistor laser.

3.2 First Round Process Development

The material structure and initial fabrication process used in the optical NOR gate is similar to previously reported work [17, 19]. The epitaxial wafer was grown using metal-organic chemical vapor deposition (MOCVD) on a semi-insulating (SI) GaAs substrate. It contains a high-bandgap n-type AlGaAs emitter and a p-type GaAs base, forming a heterojunction that prevents hole back-injection towards the emitter. Additionally, the base contains an InGaAs quantum well that acts as a carrier trap for the radiative recombination process. The collector is low-doped n-type GaAs followed by a highly doped n-GaAs subcollector on which the collector contacts are placed. Under the subcollector is an AlGaAs optical confinement layer to constrain the optical field between the emitter and collector.

The fabrication process for the optical NOR gate starts with the definition of a PECVD SiNx on the wafer followed by photoresist patterning and etching by CF_4 RIE to form an etching mask. Then, emitter etch was performed using a wet etch mixture of H_3PO_4 and H_2O_2. The exposed emitter facet sidewalls were then passivated using wet oxidation in a 425 °C furnace. The SiNx mask was then removed using CF_4 RIE. Next, Ti/Pt/Au was deposited using e-beam evaporation to form base contacts. The thickness of the Ti/Pt/Au contact was controlled to be the same height as the emitter mesa. Base-collector wet etch was performed using a solution of $H_2SO_4 : H_2O_2 : H_2O$, stopping at an InGaP etch stop right before the highly doped GaAs subcollector. AuGe/Ni/Au contacts were then deposited on the subcollector to form collector contacts that were the same height as the emitter mesa and the base contacts. Next, the devices were isolated by etching down to the GaAs substrate using BCl_3 ICP RIE with a PECVD SiNx mask.

After isolation, the height difference from the GaAs substrate to the emitter surface was around 2.5 μm. Planarization is performed using BCB followed by an SF_6/O_2 etchback to simultaneously expose the emitter surface, the base contact, and the collector contact. Next, AuGe/Ni/Au was deposited on the exposed emitter surface to form emitter contacts followed by annealing to form ohmic contacts to the emitter and collector. Afterwards, the first Ti/Au metal contact layer (Metal 1) was deposited on top of the base and collector contacts to ensure the base, collector, and emitter contacts were the same height. A second planarization step was then performed using benzocyclobutane (BCB). Since the top metal contact (Metal 2) required simultaneous overlap on the base and collector contacts, exposing the Metal 1 pads using uniform BCB etchback would have

caused metal shorts. Instead, BCB vias were opened on the Metal 1 pads where required prior to Metal 2 deposition. The via patterns were defined by optical lithography using AZ9245 photoresist followed by a reflow bake to attain a sloped profile on the via openings. The sloped profile was transferred to the BCB during the SF_6/O_2 RIE via etch. The gradual transition is necessary to prevent the Metal 2 contact pads from breaking at the transition between the planar BCB surface and the Metal 1 surface. The final step was Ti/Au Metal 2 deposition to form contact pads for testing. A scanning electron microscope (SEM) picture of the completed device before planarization is shown in Fig. 19.

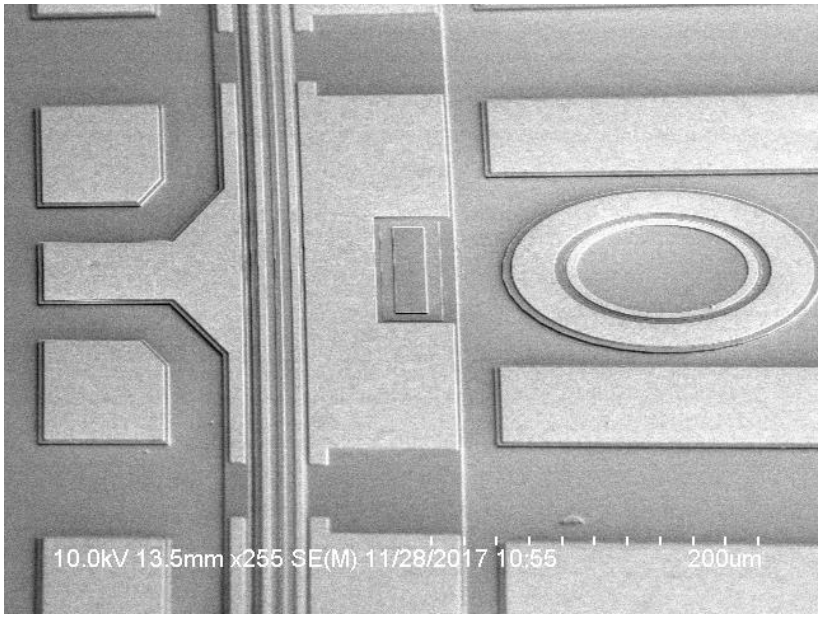


Figure 19. SEM of a transistor laser optical NOR gate before planarization.

In the first device fabrication round, two major problems were encountered which prevented the completion of a finished optical NOR gate. First, the tight, long stripe

between the collector mesa near the base metal contacts was very difficult to isolate. The stripe is 3 μm wide and runs the whole length of the wafer. An SEM picture of the device from Fig. 19 enlarged to show the 3 μm stripe is shown in Fig. 20. Initially, isolation was done by wet etch using a $H_2SO_4 : H_2O_2 : H_2O$ solution. Using various concentrations to etch the ~2 μm isolation etch depth, it proved difficult to control the etch rate. The result was non-uniform etch depths across the wafer when measured using a surface profiler. Consequently, the first fabricated device lot presented base-collector shorts on every device. It is suspected that the long and narrow nature of the collector mesa isolation stripe makes it difficult for the etchant to penetrate, causing the etch rate to be much slower in the 3 μm isolation gap region. To further isolate the problem, SF_6/O_2 etching is done on a fully processed wafer in order to remove the BCB planarization layer. During the etch, Metal 2 contact pads act as a mask to protect the underlying BCB. When SEM pictures of the devices are taken at a tilted angle (Fig. 21), the BCB thickness between overlapping metal layers can be measured. Using this process, the BCB coverage was estimated to be 1 to 1.2 μm for optical NOR gate transistor lasers and 0.6 to 0.8 μm for stand-alone transistor lasers. Based on previous experimental results, at least 0.7 μm BCB isolation is required between two overlapping metal layers to prevent leakage. Since the transistor laser in Fig. 21 shows isolation in excess of 1 μm and still suffers from a base to collector short, a semiconductor short is the likely mechanism.

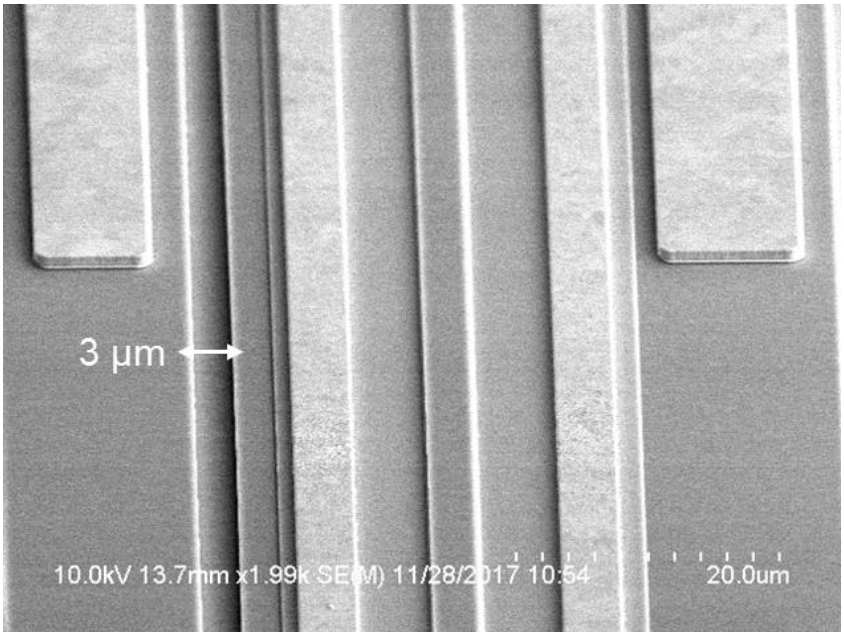


Figure 20. SEM of a transistor laser optical NOR gate before planarization, showing the 3 µm gap between isolated collector mesas on the base side. The long, narrow nature of the gap makes it difficult to etch.

In the second attempted fabrication lot, the semiconductor short problem was addressed by switching to a dry etch using BCL_3 ICP RIE. The dry etch was favored because of two reasons. First, the dry etching rate is more controllable and the extent of the etch can be monitored using a built-in laser reflectometer. Second, it is suspected that the directional nature of the RIE will be able to penetrate the narrow collector mesa stripe better than the wet etch. The devices were isolated using this method to a 0.2 µm overetch depth of the SI GaAs substrate. The overetch depth was specified to limit the height discrepancy of the device, which can potentially make the second planarization and via process more difficult. Process control monitor (PCM) collector mesas with 3 µm gap were measured and showed adequate isolation. Right before the second planarization,

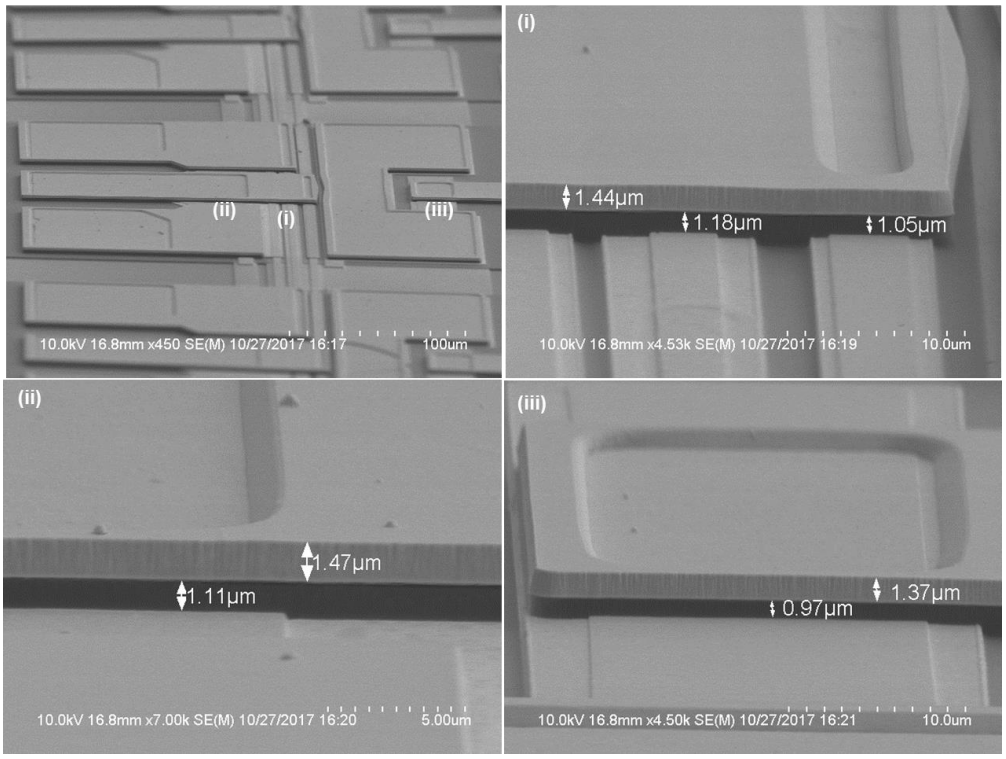


Figure 21. Tilted angle SEM pictures of a transistor laser with the BCB etched away to reveal the isolation depth. The metal overlap regions are isolated by ~1 µm BCB to prevent metal shorts. The SEM pictures reveal that the base-collector short of the device is due to a semiconductor short instead of a metal short.

The devices showed a varying degree of isolation in the narrow gap. Some devices showed good isolation with leakage currents limited to several nA, while other devices had very high leakage currents up to the µA range. Interestingly, the low leakage devices were constrained to two columns of devices in one wafer while the remaining columns showed high leakage. It is suspected that using the dry etch still suffers from reduced etch rates in the 3 µm gap regions, but the etch uniformity was better across the wafer. In addition, the interconnection of base contact metals of adjacent devices prior to cleaving

could present a path of low resistance, indicating that a device in a high-leakage column could show low leakage base-collector leakage once cleaved.

The second major problem that was encountered is base-emitter short caused by overexposure of the base metal and emitter mesa during the first planarization and etchback steps. After the first planarization, the BCB coverage on top of the metal pads is non-uniform following the size discrepancy of the individual patterns on the device. As a result, when etchback is performed, the emitter mesa and base metal stripes are exposed first, followed by the collector metal pads, and the photodiode aperture p and n contacts last. Since the goal of the etchback is to expose all metal pads for Metal 1 deposition, the stripe regions end up overexposed. As illustrated in Fig. 22, when emitter metal is deposited on an overexposed stripe, there is not enough BCB isolation between the emitter metal and the base surface to prevent a base-emitter short. Moreover, since the stand-alone transistor lasers have a much smaller footprint compared to the optical NOR gate transistor lasers, their emitter and base stripes are usually covered by the thinnest BCB, meaning they will likely always be overexposed. Because of these two major problems, the device processing was halted and further process modifications were made.

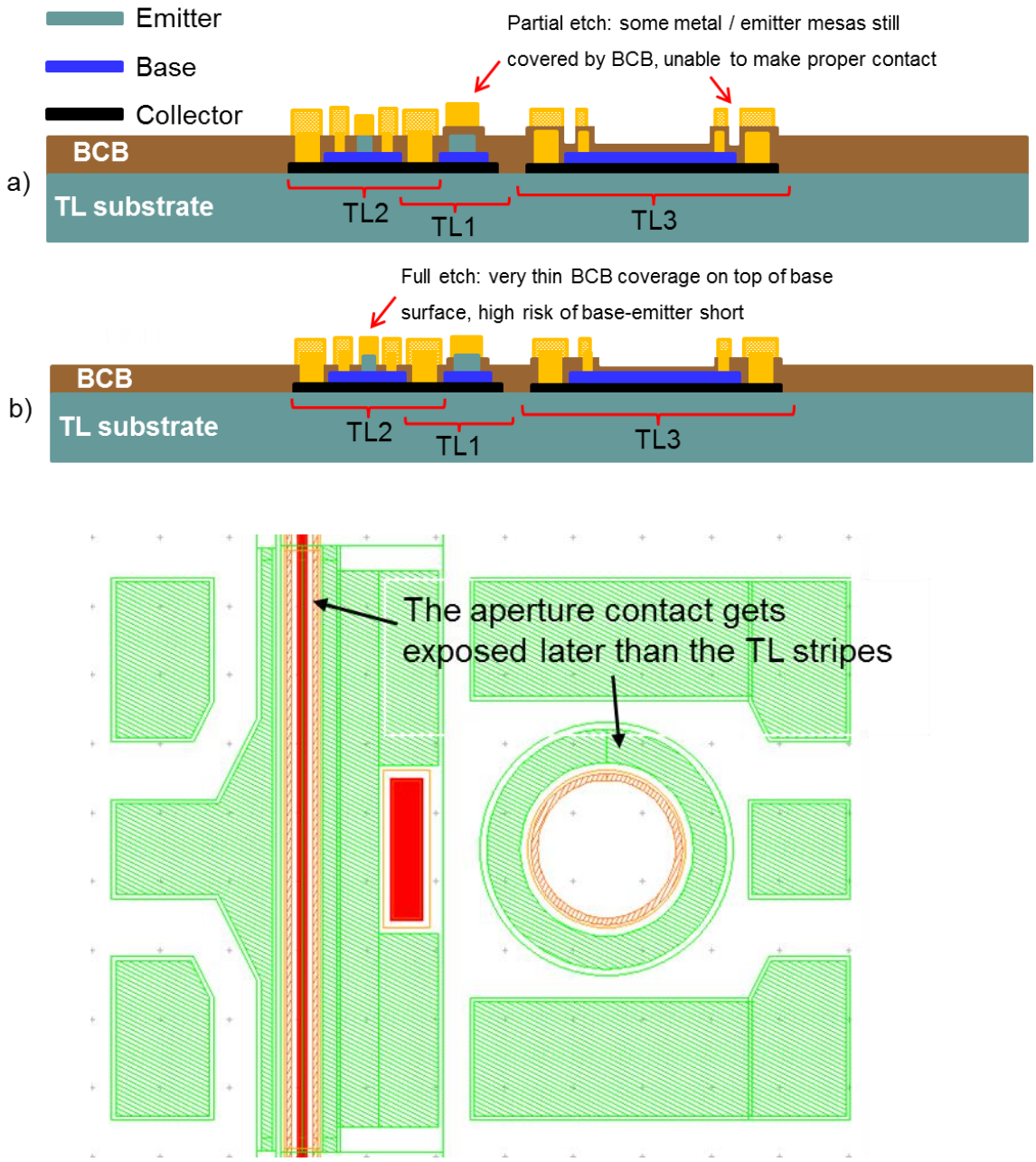


Figure 22. Cross-sectional (top) and layout view (bottom) illustrating the problem with uneven BCB planarization in (a) a partial etchback case resulting in underexposed features and (b) full etchback case resulting in very thin BCB coverage on top of the base surface.

3.3 Second Round Process Development

In the second round of process development, two important changes were implemented. First, the isolation dry etch was done to a deeper overetch in order to eliminate the semiconductor base-to-collector short. Second, in order to ensure even exposure of the metal pads, a via process (first via) was added to expose metal pads or features only where the emitter metal or Metal 1 need to be deposited while maintaining BCB coverage in critical areas. The first via process was also split between two masks to account for different etching rates between wide and narrow vias. The fabrication process flow for the second fabrication round is shown in Fig. 23, and a sketch of the first via process and photomask are shown in Fig. 24.

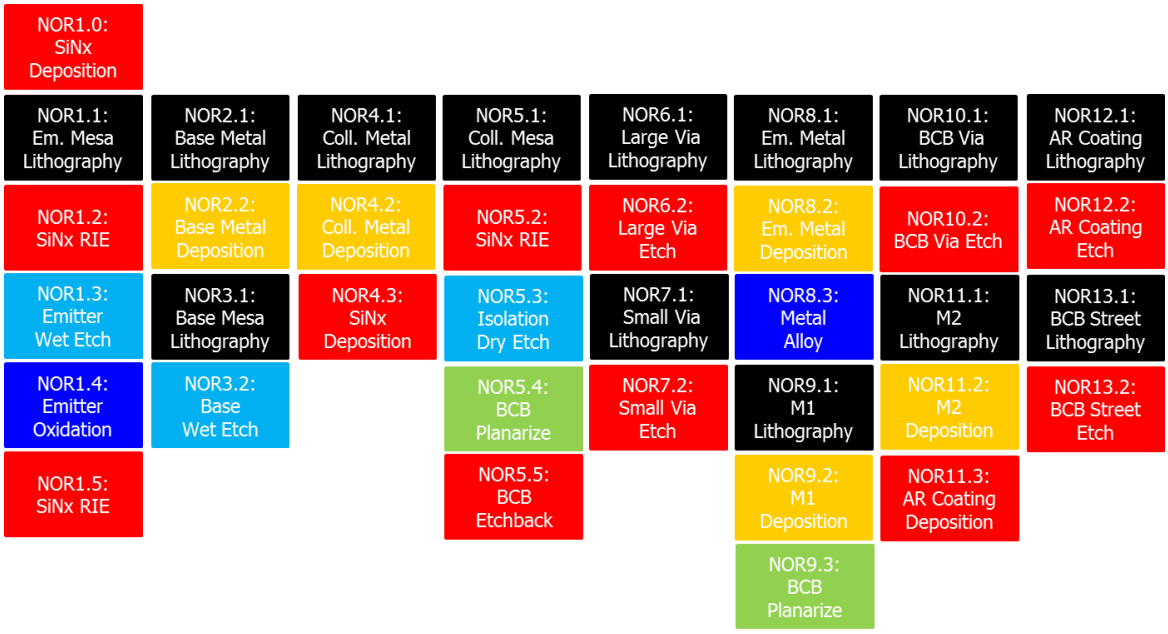


Figure 23. Process flow for the second fabrication round of the transistor laser optical NOR gate.

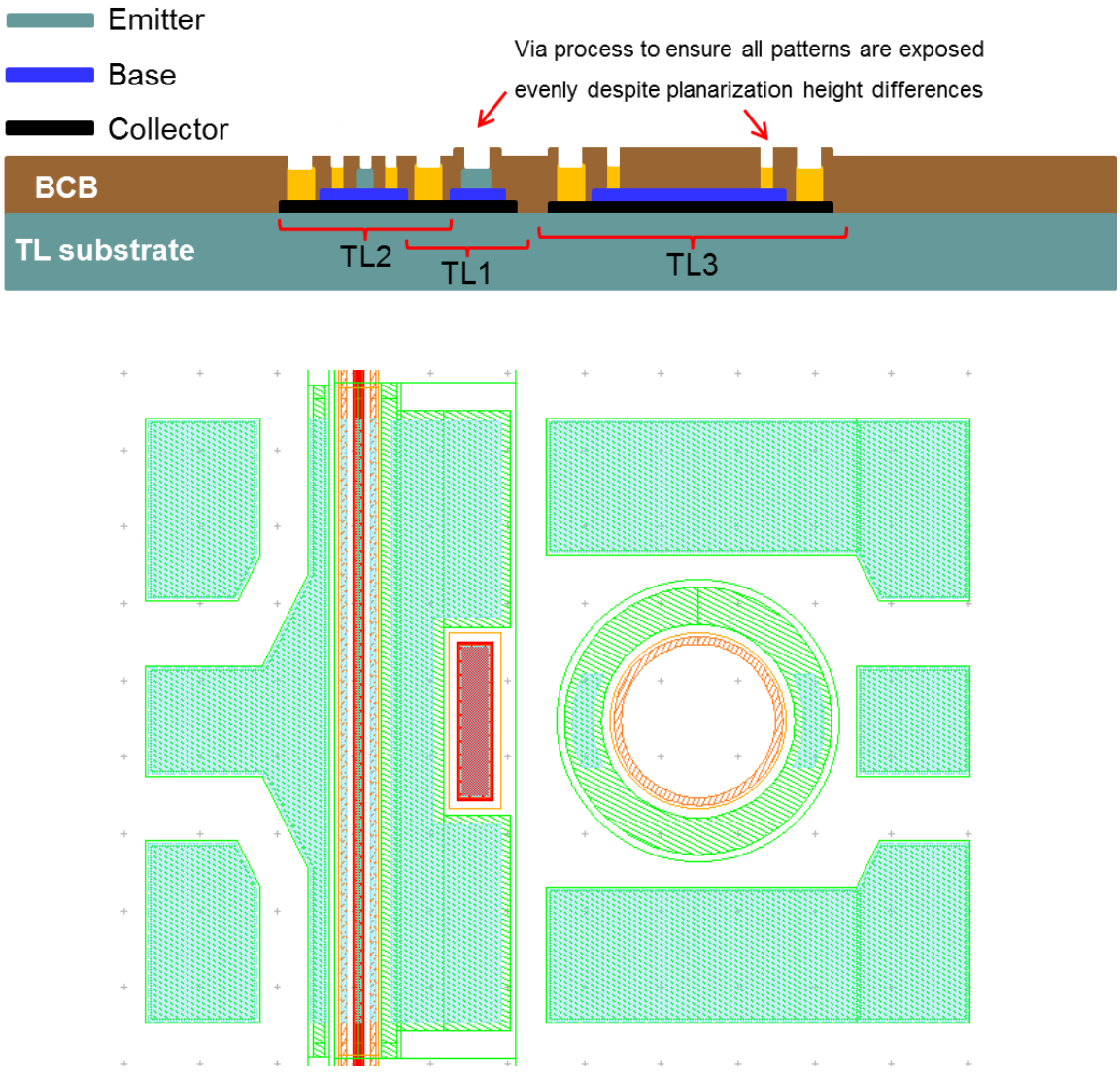


Figure 24. Cross-sectional (top) and layout view (bottom) of the first via process to solve the uneven BCB planarization / etchback issue.

The fabrication process went exactly the same as the first round until the isolation dry etch step, where the overetch was increased from 0.2 µm to 0.5 µm. First planarization was done with a minimum target BCB coverage of 1.5 µm, with some samples requiring additional uniform etchback steps. Then the wide and narrow first vias

were defined using separate photoresist reflow masks. After the first via processes, the emitter metal was deposited over the emitter stripe followed by annealing in a 350 °C dry N_2 furnace in order to form ohmic contacts to the emitter and the collector. After the Metal 1 had been deposited to planarize contact heights between the emitter, base, collector, and photodiode contact pads, the second BCB planarization was performed, followed by the second via process. Finally, the Metal 2 probing pads were deposited. The sequence between the first and second planarization and via steps is illustrated in Fig. 25. After the core device fabrication processes were complete, the BCB in the regions between discrete devices was etched away using a photoresist mask, forming a cleaving "street" to ensure uniform cleavage. The wafers were lapped down to 150 μm, using photoresist to protect the top surface. Then, using a scribe and break method, the wafers were split into sections and the laser facets were formed.

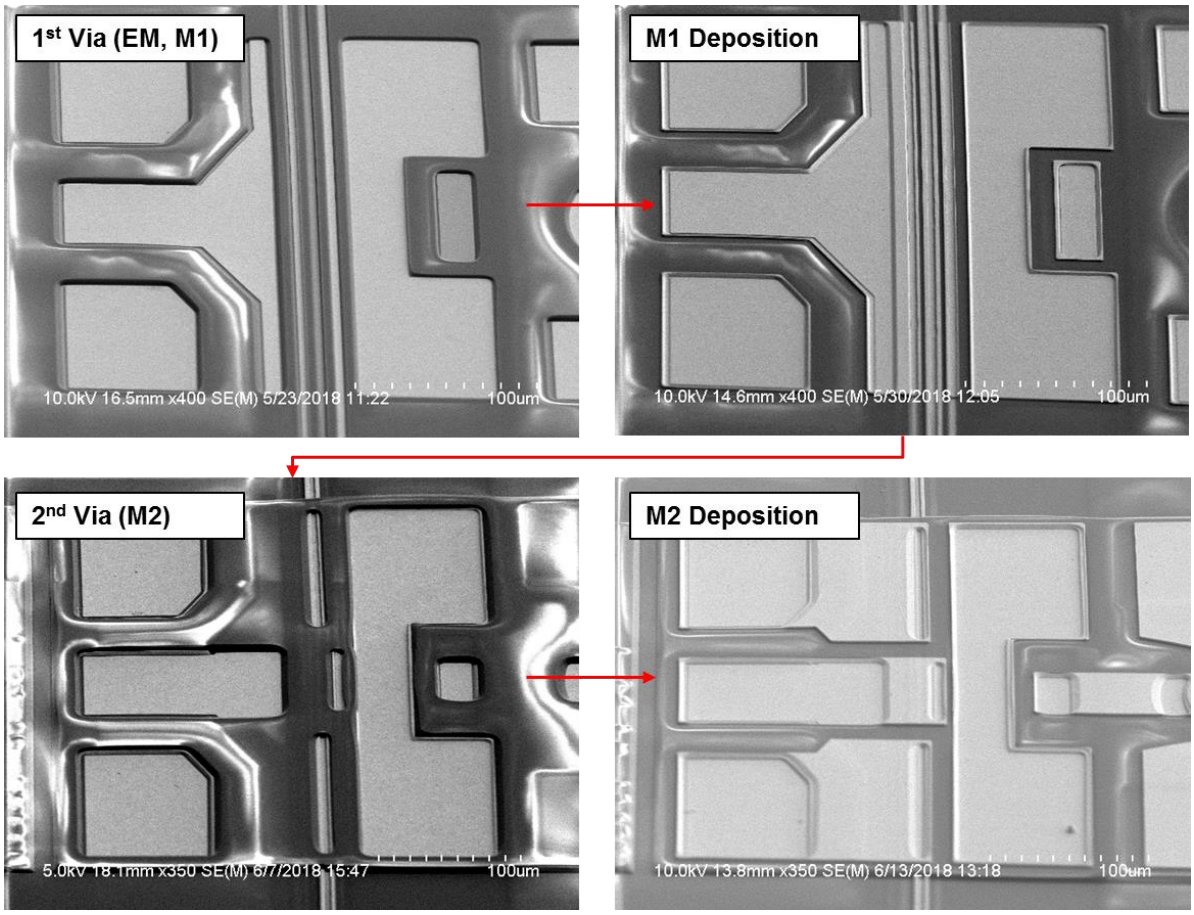


Figure 25. SEM of the revised process flow including first and second via processes.

4. CHARACTERIZATION OF TRANSISTOR LASER OPTICAL NOR GATE

4.1 Measurement Setup

The characterization of the transistor laser optical NOR gate was performed in the measurement station shown in Fig. 26. The station consists of a sample stage with a microscope, a HP 4142 power supply with stimulus and measurement units (SMUs), a large-area photodiode in an integrating sphere, a 850 nm VCSEL module, a fiber probe, GSG probes, and DC probes. The base-emitter voltage bias of the transistor laser is provided through a GSG probe. A DC probe connected to a constant DC power supply through a variable load resistor supplies the collector voltage. The DC power supply and the load resistor both set the load line operation of the transistor laser. The light input

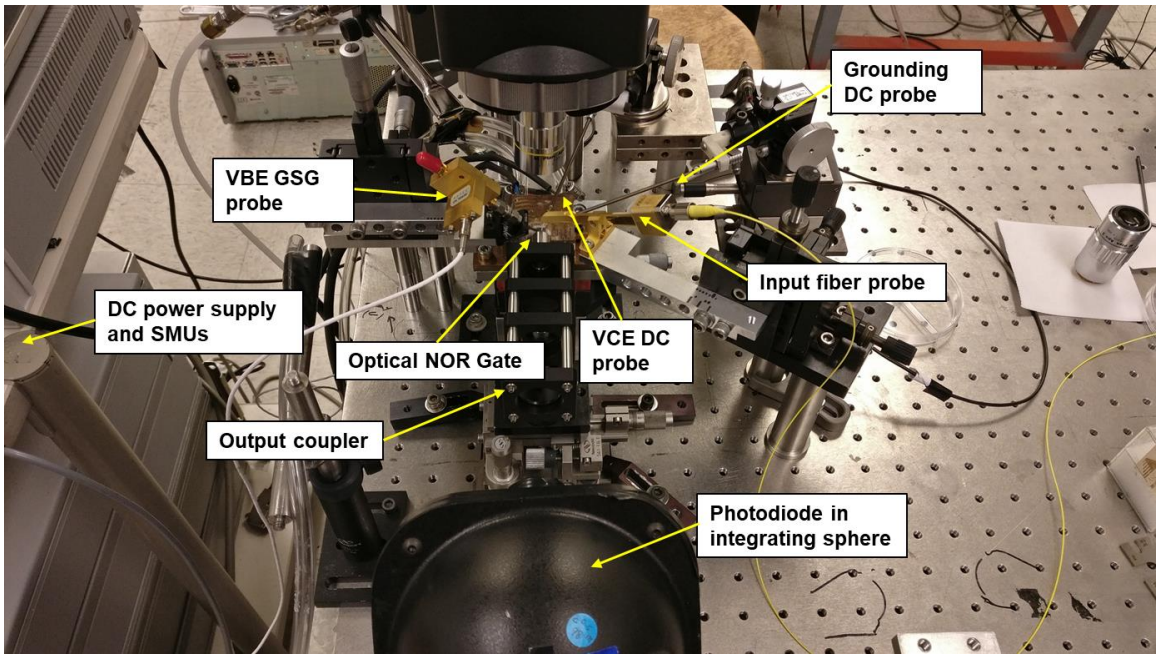


Figure 26. Measurement station to characterize the transistor laser optical NOR gate.

source is a packaged 850 nm VCSEL which is coupled to the optical NOR photodiode through a fiber probe similar to that in section 2.3. A DC probe grounds the n-contacts of the photodiode. Finally, light output from the transistor laser facet is free-space coupled into a large-area photodiode in an integrating sphere. An optical microscope picture of the fabricated optical NOR gate with the probing arrangement is shown in Fig. 27.

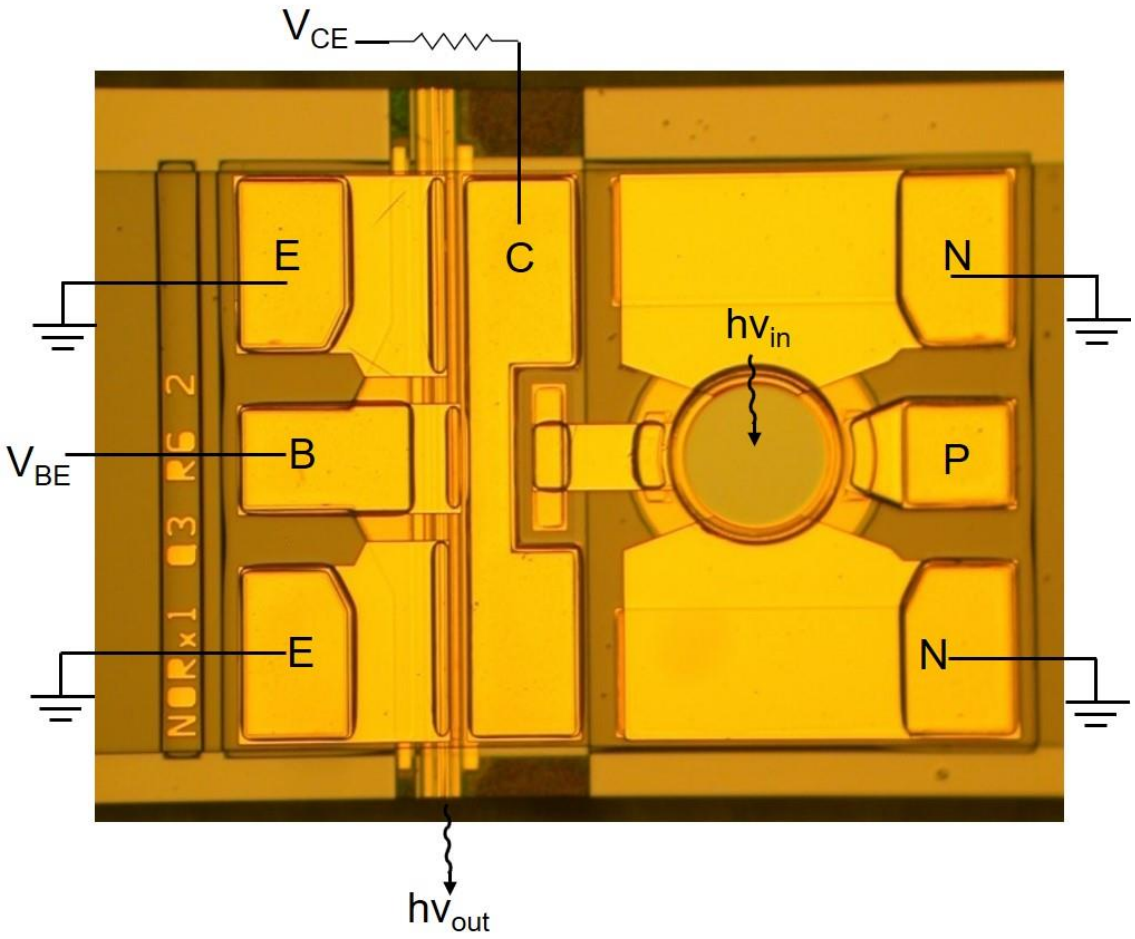


Figure 27. Optical microscope picture of the finished optical NOR gate with the measurement probing arrangement overlaid.

4.2 Discrete Component Characterization

Before testing the logic functionality, the individual components of the NOR gate are characterized. First, the responsivity of the TL0 photodiode is measured using the 850 nm packaged VCSEL. As in section 2.3, the VCSEL light output vs. current characteristics were first calibrated using a power meter. The average responsivity of the optical NOR gate photodiode was found to be 0.0346 A/W, as shown in Fig. 28. The low responsivity is caused by limited light absorption in the base-collector junction of the transistor laser material, which only contains a 60 nm thick region of depleted GaAs.

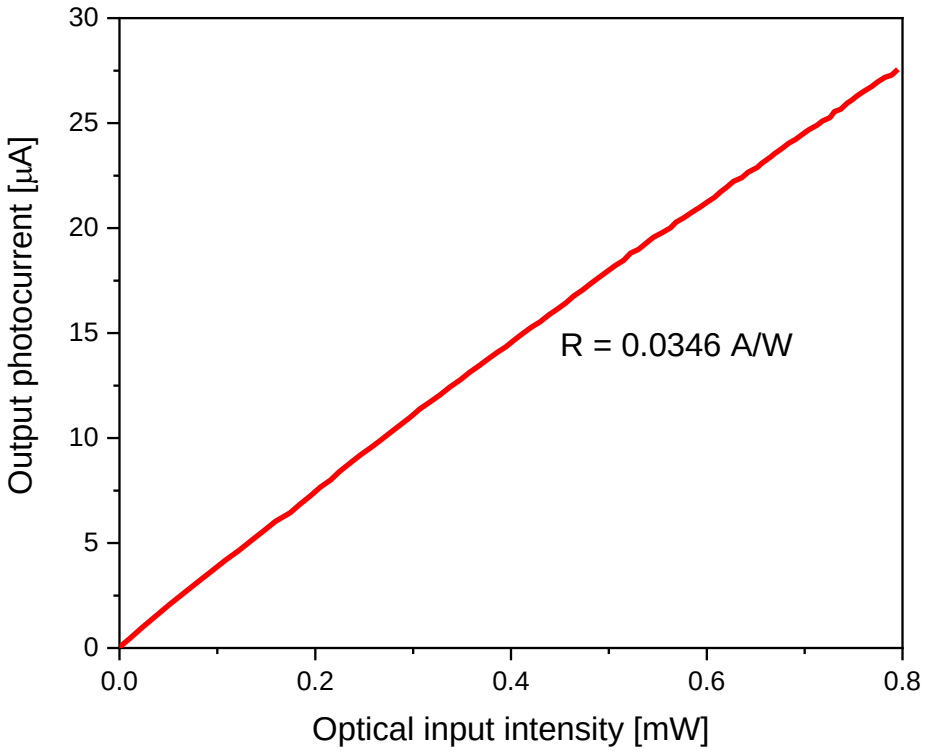


Figure 28. Responsivity of the TL0 photodiode measured using a 850 nm VCSEL.

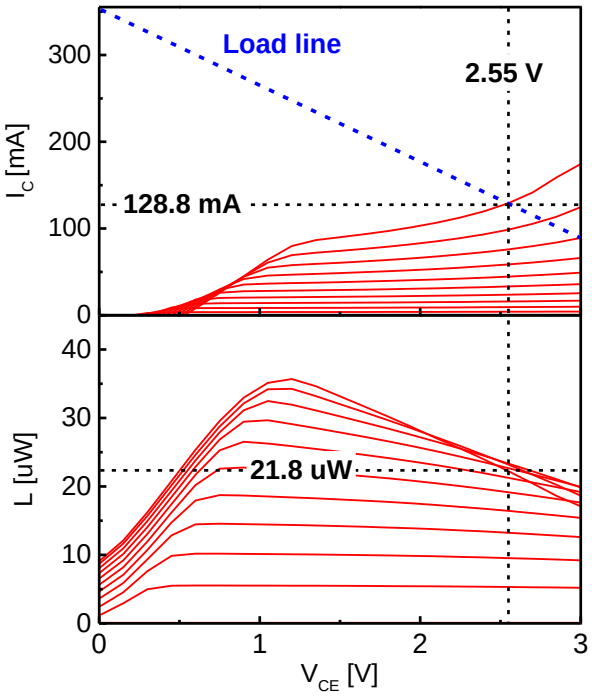


Figure 29. L-I-V curves of TL2 showing light-emitting transistor behavior. The blue line indicates the load line set by the voltage supply (V = 4 V) and the load resistor (R = 11.3 Ω).

The L-I-V curves of the output transistor laser TL2 biased at a maximum base current of 50 mA (ΔIB = 5 mA) is shown in Fig. 29. The collector current exhibits relatively large electrical gain compared to a typical transistor laser without showing gain compression which signals the transition from spontaneous to stimulated light emission. The measured light output of the transistor laser is very weak due to the spontaneous nature of the light emission, which is similar to that from a light-emitting transistor (LET). It is suspected that the transistor laser suffers from a prohibitively high lasing threshold caused by poor heat conduction or added resistance from the double via process. Because the structure of the transistor laser is designed for light collection from

the cleaved facet, only a very small amount of light can be collected using the free-space coupling method.

4.3 Demonstration of Logic Functionality

The logic function of the optical NOR gate was characterized as follows. First, TL2 was biased at a base current of 50 mA to maximize optical output. The voltage supply was set at 4 V with a load resistor R of 11.3 Ω, yielding a TL2 collector-emitter voltage of 2.3 V, which correctly places TL2 in the tunneling modulation region. Simultaneously, the VCSEL light output was coupled to the TL0 aperture and switched on and off to provide a square wave input optical signal. The generated photocurrent shifted the operation of TL2 along the load line as indicated by the blue line in Fig. 29. Note that in this case the NOR gate acts as an inverter, but testing for the NOR functionality can be done by coupling two different light sources into the fiber or by using a multi-level input signal. The optical logic timing diagram for the optical NOR gate is shown in Fig. 30. It shows a logic “1” threshold of 21.85 μW and a logic “0” threshold of 21.75 μW, respectively.

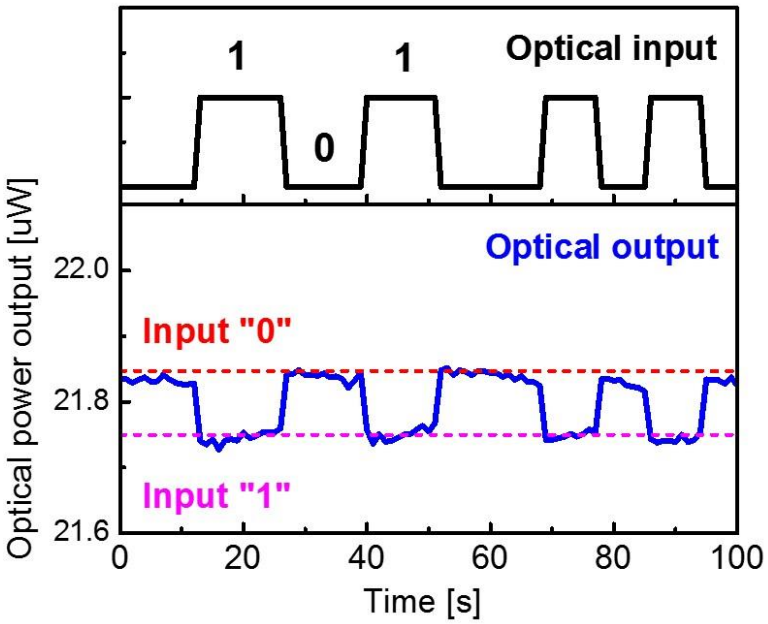


Figure 30. Logic timing diagram for the optical NOR gate for a single input case.

5. CONCLUSIONS AND FUTURE WORK

5.1 Summary

The transistor laser exhibits unique transistor operation with high-speed and integration potential enhanced by the tunneling modulation from the electron-photon interaction inside the base laser cavity. The development process to take a single transistor laser device into an integrated circuit was described. First, a vertical photodiode structure and methodology were developed and then integrated into the transistor laser. Based on ICPAT, the functioning mechanism and the design of the transistor laser optical NOR gate circuit were described. Through layout design changes and extensive process development, the optical NOR gate device were fabricated. During characterization, it was found that the optical NOR gate transistor laser exhibits spontaneous emission and was unable to reach the lasing threshold due to reasons addressed in the next section. Regardless, since the tunneling modulation properties were still present, logic processing functionality was demonstrated in the case of a single optical input. To this date, this work is the first demonstration of a transistor laser integrated circuit and optical logic processing using the transistor laser.

5.2 First Generation Transistor Laser Integrated Circuit Process Improvements

As described in sections 3.2 and 3.3, the conversion from the original single-device transistor laser process was not straightforward. Particularly, when introducing integrated devices with different-sized isolation mesas, BCB planarization non-uniformity was a lingering issue. Although the use of the double via process was mostly successful in eliminating base-to-emitter shorts in optical NOR gate transistor lasers, the resulting devices could not reach lasing operation. In addition, all of the discrete transistor laser devices were shorted due to insufficient BCB coverage despite the double vias. This means that even after the second fabrication round, the process is not yet robust and some improvements can be proposed.

To reach the lasing threshold, the round-trip gain in the optical cavity must be larger than the total loss in the system. Since the epitaxial structure in the optical NOR gate is similar to that in previously demonstrated work, it is safe to assume that any additional loss in the system can be attributed to processing changes made in the integration process. One such change is the incorporation of a via when depositing the emitter metal on the emitter mesa to prevent a base-to-emitter short due to insufficient BCB isolation. SEM pictures were taken to analyze the emitter contact after cleaving. As shown in Fig. 31 (b), the emitter metal breaks off in the middle due to a very sharp via slope, with the metal not thick enough to compensate. As a result, the effective emitter metal area is reduced by about half and will result in increased emitter resistance. In

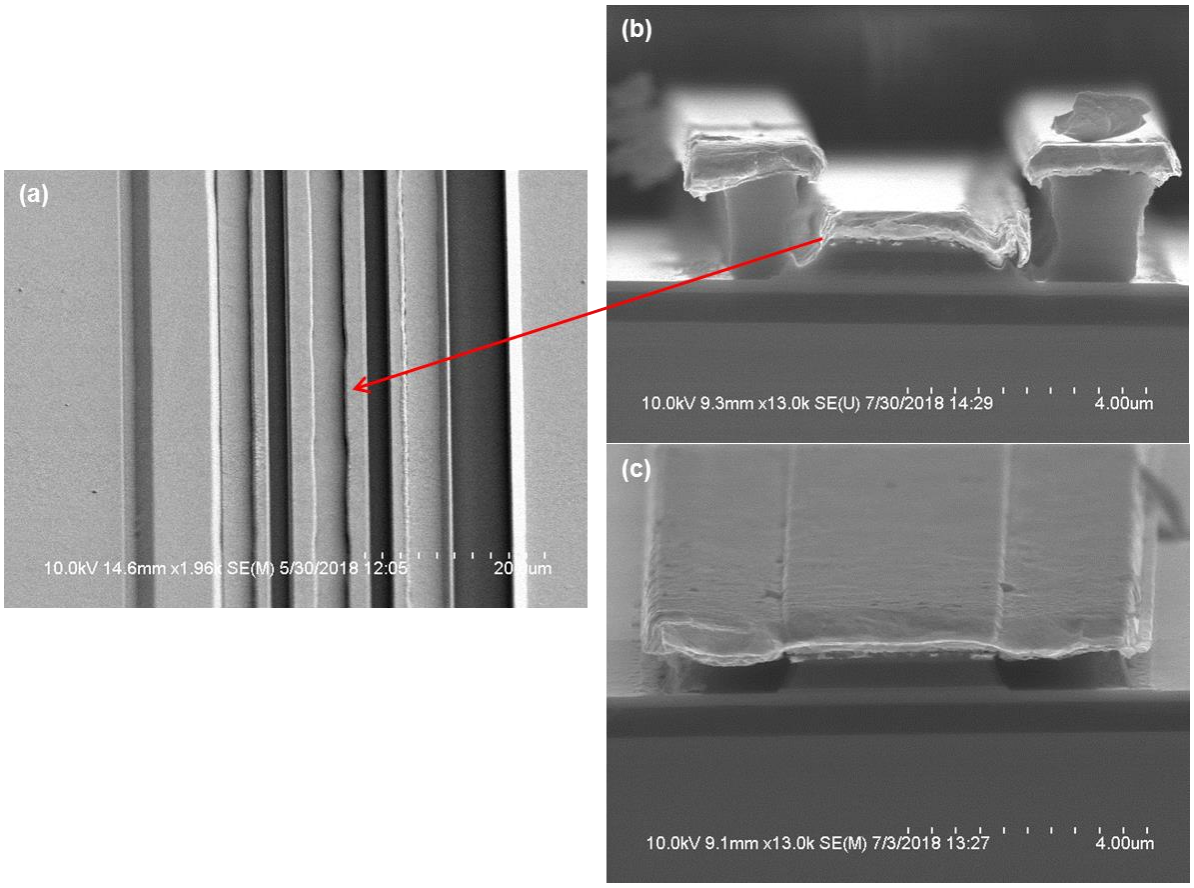


Figure 31. (a) SEM picture of the optical NOR gate transistor laser emitter stripe. (b) A zoomed-in, cross-sectional SEM picture of a section of the emitter stripe showing a metal break due to sharp via slope, increasing device resistance (c) Cross-sectional view of a similar emitter stripe in the original transistor laser process.

addition, the via opening process becomes extremely difficult. The via needs to have a very wide, gradual transition area while at the same time maintaining the maximum possible contact area with the emitter mesa without extending too far toward the base. When the via opening reduces the contact area with the emitter mesa, the emitter resistance will also be increased. In contrast, in the original process shown in Fig. 31 (c), the maximum contact area will always be guaranteed and only limited by the lateral overetch during emitter mesa wet etching.

In order to solve both the emitter contact issue and the uneven planarization between discrete and integrated transistor lasers, another mask change may be necessary. One possible approach is to increase the size of the emitter mesa so that it does not require a via process to deposit the emitter metal without causing a base-to-emitter short. Another possible process improvement, which can be implemented by slightly changing the lithography order, is to deposit the emitter and collector contacts simultaneously, then depositing the base metal on top of the base and the collector metal in order to planarize the contact heights. This way, the process eliminates two lithography and evaporation steps and allows metal deposition prior to BCB planarization. Figure 32 illustrates the proposed process changes. Lastly, it must be noted that it is inherently difficult to evenly planarize two differently sized devices on the same wafer using only a spin coating method. Therefore, another improvement that can be made is to either implement only optical NOR devices on a single wafer or to extend the mesa size of stand-alone transistor lasers in order to achieve even planarization.

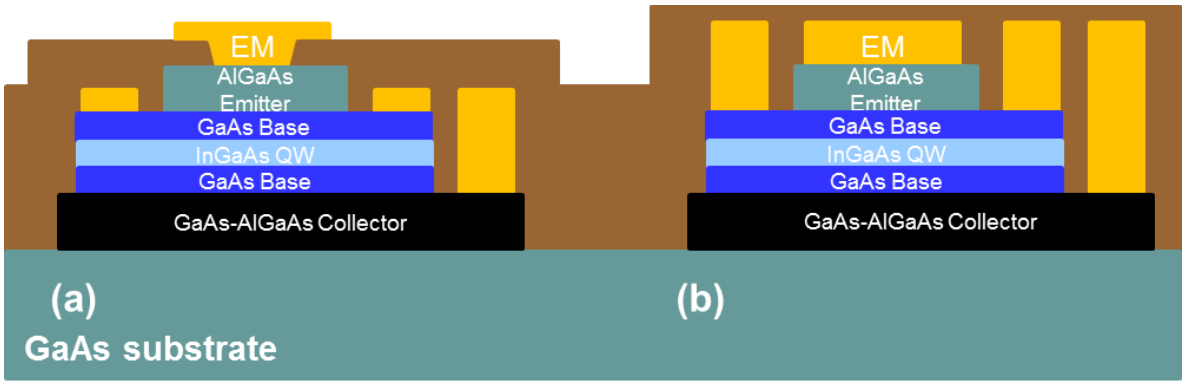


Figure 32. (a) Cross-sectional diagram of the current transistor laser structure. (b) Proposed cross-sectional diagram for the revised transistor laser optical NOR gate.

5.3 Second Generation Transistor Laser Integrated Circuit

The demonstrated optical NOR gate is the first step toward transistor laser integrated circuits. The unique transistor operation and tunneling modulation properties are not limited by the size of the device and should be well suited to aggressive scaling as long as the system can provide enough gain to sustain stimulated emission. Since tunneling modulation is an inherently fast process with THz-range bandwidth, a transistor laser-based device with well-controlled parasitic elements is an excellent candidate for future high-performance electro-optical applications.

To achieve a higher level of integration, several modifications can be made to the existing transistor laser technology. On the epitaxial side, incorporating a highly doped collector layer to achieve a sharper base-collector junction enhances ICPAT, resulting in a "tunnel junction" [29]. In a tunnel junction transistor laser (TJTL), light output dependence on the collector voltage is greatly increased. Figure 33 compares typical L-V curves of a regular transistor laser and a TJTL. Optical switching in a TJTL requires a lower voltage swing, which results in lower power consumption and enables smaller device dimensions to reduce parasitics. The addition of a larger dedicated intrinsic region or a buried photodiode region can ensure larger photocurrent and allow smaller area vertical photodiodes. In an ideal world, defining photodiodes and waveguides using selective area growth wimilar to those in [7,8] will be the ultimate solution for a transistor laser integrated circuit. In addition, optical facet definition by dry etching instead of cleaving can allow for monolithic optical transmit-receive operations.

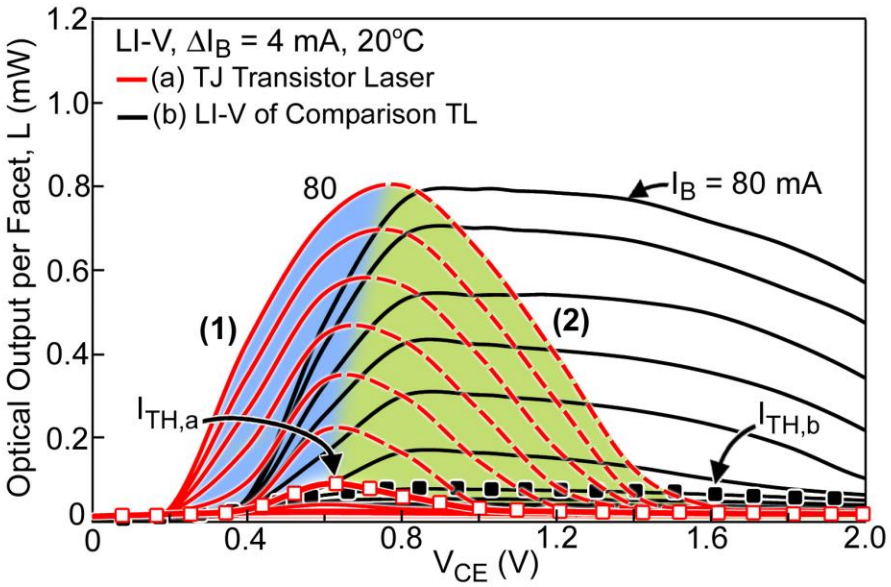


Figure 33. L-V curves of a tunnel junction transistor laser (red) and a regular transistor laser [29]. The tunnel junction enhances ICPAT in the base-collector junction, resulting in a stronger tunneling modulation, which requires a smaller voltage swing.

Using a black box model of a previously reported edge-emitting transistor laser with 200 µm cavity width [19], simulations were done in Keysight ADS to predict the potential performance of a transistor laser-based optical logic gate when it is not hindered by excessive parasitics [30]. The simulation assumes a scaled-down transistor laser junction capacitance of 200 fF and a reduced load resistance of 5 Ω. The photodiode capacitance is limited to 100 fF with an assumed photocurrent of 1 mA. Based on these parameters, the power consumption is estimated to be 26.6 mW. Figure 34 shows an eye diagram of the gate simulated at 40 Gb/s. Using the same parameters, different logic gate configurations were simulated using both base current and collector voltage modulation, as shown in Table 1.

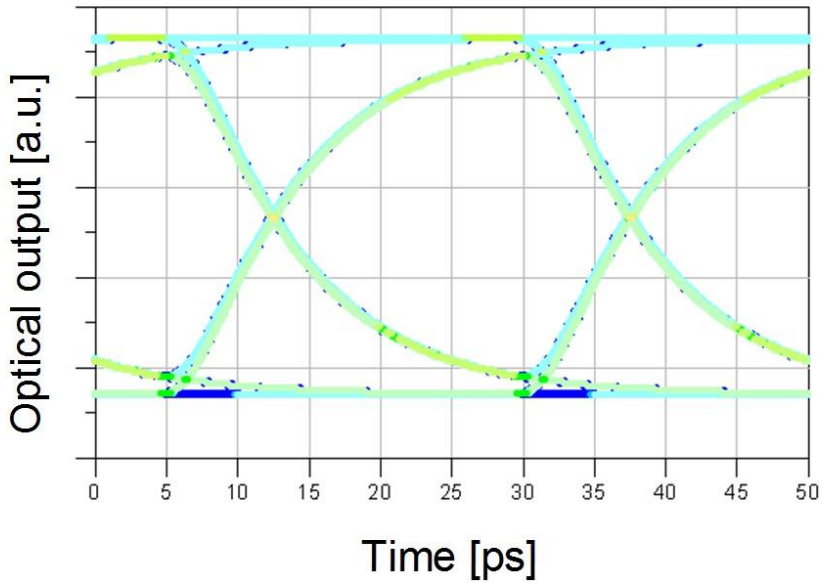


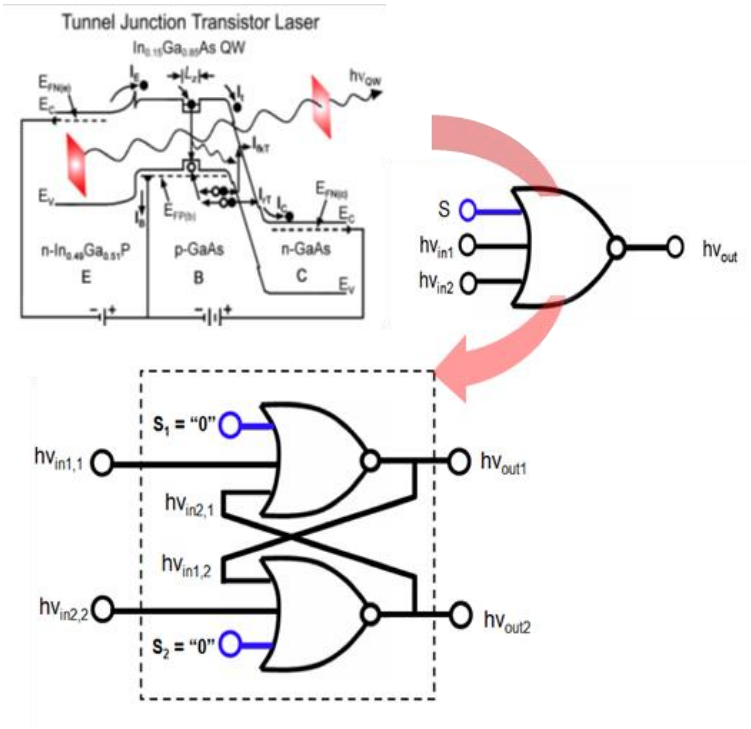
Figure 34. Simulated eye diagram for an optical NOR gate at 40 Gb/s operation assuming a junction capacitance of 200 fF, 1 mA photodiode current, 100fF photodiode capacitance, 5 Ω load resistance, and 2 V supply voltage [30].

Table 1. Simulated performance of transistor laser-based optical logic gates at 40 Gb/s data rate with different configurations and modulation schemes [30].

	Inverter	**NAND**	**AND**	**OR/NOR**
Delay [ps]	14.5	14.5	3.5	3.5
Rise / fall time [ps]	14.2 / 14.5	14.2 / 14.5	7.6 / 7.7	7.6 / 7.7
Jitter RMS [ps]	0.14	0.14	0.02	0.02
Power consumption [mW]	16.8	16.8	26.6	26.6
Modulation method	Base	Base	Collector	Collector

5.4 Optical Bistable Latch

While the optical NOR gate serves demonstration purposes, optical logic processing using the transistor laser can potentially be adopted in more involved computing applications with more complicated functions. The next step for transistor laser integration is to use the optical NOR gate as a building block to form multi-gate logic circuits. One of the simplest logic circuits that can be implemented using the integrated transistor laser optical NOR gate is the optical bistable latch shown in Fig. 35. The optical bistable latch consists of two optical NOR gates, each having three input ports. The output of each NOR gate is fed into the input of the other NOR gate, forming a cross-linked gate. The change of output state only happens when one of the inputs is a logic “1” and the other is a logic “0”, with a simultaneous logic “1” input being forbidden. The bistable latch is an important storage elements in digital logic applications.



$hv_{in1,1}$	$hv_{in1,2}$	hv_{out1}	hv_{out2}
0	0	No change	No change
0	1	0	1
1	0	1	0
1	1	Forbidden	Forbidden

Figure 35. Device diagram and logic table of an optical bistable latch using the transistor laser optical NOR gate.

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