Limitations of di/dt Technique in DC Line Protection

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Abstract

Protection issues are major challenges in realising multi-terminal (MT) HVDC systems. In this paper, the findings of an investigation carried out on a *di/dt* based protection technique with the view to ascertaining its suitability for the protection of DC lines are presented. Firstly the main issues regarding the protection of MT-HVDC system are explored and thereafter the *di/dt* protection technique is evaluated. Some of the limitations of *di/dt* protection technique were due to the effect of travelling waves and oscillations. These lead to errors in estimating the actual *di/dt* since the resulting fault current profile may attain its local maximum or minimum before or during the time window set for the measurement. This is particularly the case during directional comparison. Simulations have been carried out in PSCAD and the results presented show that the *di/dt* protection technique will not be a reliable method for the protection of DC lines, in particular for the protection of DC grid.

1 Introduction

The development of offshore wind farms with HVDC interconnections is attracting great attention across the globe since it is considered as one of the panaceas to current global energy challenge. Generally, for long distance power transmission, HVDC system is the preferred option due to its technical and economic advantages[1][2]. It is also envisaged that in the near future, a number of offshore and onshore converter stations will be interconnected to form a multi-terminal HVDC network (MT-HVDC); whereas protection issues remain a major challenge[3]–[6]. This is because protection algorithms for MT-HVDC system will have to operate faster than those used in conventional HVAC interconnections; typically less than 1*ms* from fault inception including the time delay in hardware in the loop[7]. This is due to the relatively low inductance in DC networks which usually results in a rapid rise in the fault current during short circuits[8], [9]. This current propagates extremely rapidly, thus reaching damaging levels in few milliseconds[4]. Therefore fault detection and fault clearance must be done as fast as possible to avoid a total system collapse. However, a major issue is selectivity; as only the faulty section should be isolated in the event of a fault. This constitutes a major challenge considering the complex nature of the proposed DC grid as well as the anticipated length of the transmission lines or cables. Also, the effects of the distributed nature of the line parameters, their frequency dependency and the associated travelling wave phenomenon poses a major challenge to developing suitable and reliable protection algorithms for the proposed DC grid.

Several DC line protection techniques including a method based on the rate of rise of fault current (or *di/dt*) have been proposed and are well documented in literature[2], [5], [8]–[14]. The rest of the paper is structured as follows. Section 2 gives a brief overview of the protection issues regarding the development of suitable protection algorithms for MT-HVDC network. In section 3 the *di/dt* protection technique is evaluated and thereafter the phenomenon of fault propagation along a transmission line is explained based on travelling wave theory. Section 4 presents the results of a full scale simulation based on *Modular Multi-level Converter (MMC)* HVDC model while section 5 concludes the paper with some recommendations for future studies.

2 Protection Issues

As indicated in [4], a major issue even with HVDC breakers in place is the rapid propagation of the fault current into the grid. In the conventional HVAC grid, a fault in one part of the network has a reduced impact on another part of the network due to the transformer reactances and other reactors present in the system; hence given the protection system has up to *60ms* to detect and clear the fault[4]. In contrast, the inductances in a HVDC only affect the rate of rise of the current and therefore have a lower impact on the propagation of the fault current [4]. This implies that a fault in a DC grid will be experienced almost at the same time in other parts of the network.

Generally, MT-HVDC are based on Voltage Source Converters (VSC) due to their advantages over the conventional thyristor based Line Commutated Converters (LCC) such as black start capability and the ability to independently control active and reactive power. Furthermore, the power flow in VSC - HVDC systems can be controlled without changing the voltage polarity thus allowing a common bus to be used to interconnect several VSCs as well as enabling the use of Cross Linked Polyethylene (XLPE) cables[11].These attractive features have made VSCs the most suitable option for MT-HVDC grid. However, VSCs have limited over current capabilities and as such cannot be exposed to large fault currents[9]. During DC side short circuit such as *pole to pole* faults, even if the IGBTs are blocked for self-protection, the free-wheel diodes create a path for the fault current which can result in

extremely high current if the fault is not cleared. A fault on the DC side will therefore result in a three phase fault on the AC side[10].

Traditional LCC based HVDC systems are fitted with a large DC side inductance and as such able to limit the rate of rise of the fault current during DC side short circuits. Also, as LCC HVDC is thyristor based, converter control is able to limit the fault currents during short circuit[14]. This is not the case for VSC-HVDC. The use of AC side circuit breakers as in two-terminal VSC-HVDC is not applicable to MT-HVDC as this will de-energised the entire grid[8], [11].

Recent trends in VSC technology led to the development of the Modular Multilevel Converter (MMC). MMC can either be of half bridge or full bridge type [5], [15]. The half-bridge type is not able to block fault current and is referred to as a *non-blocking* converter. It therefore requires DC side circuit breakers located at both ends of the line or cable. The full-bridge type is able to block fault current by converter control and is referred to as a *blocking* converter; and as such may not require DC side breakers[5]. The circuit arrangements of a MMC converter are shown in Figure 2.1.

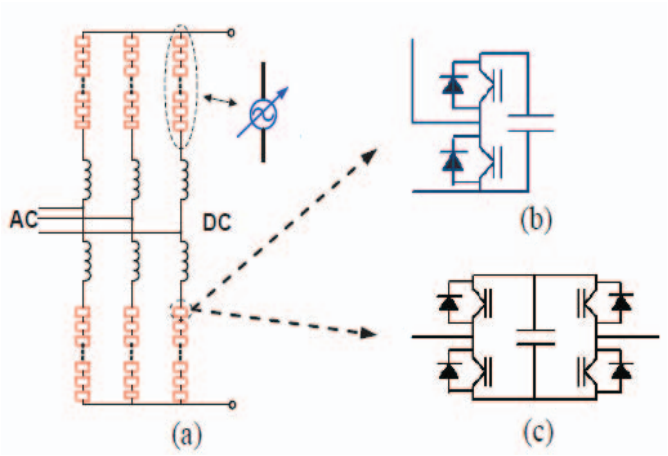


Fig. 2.1 MMC Converter [5]

(a)Topology (b) Half Bridge submodule (c)Full Bridge Submodule

The converter and earthing arrangement of the grid also have significant impact on the actual magnitude of the DC fault current.[4], [5], [10]. Generally, an MMC converter can either be a symmetrical or asymmetrical monopole configuration (Figure 2.2); with the former being the most economical and most widespread topology[5]

2.1 Pole to Ground and Pole to Pole faults

A pole to ground fault in a symmetrical monopole arrangement results in a significant shift in the healthy pole voltage [4], typically up to *2pu;* and the faulty pole voltage collapse suddenly to zero. Contribution from the AC side is small apart from the current flowing through the earthing resistor. However, the converter will experience a sudden high transient current owing the discharge of the energy store in the transmission system[5]. A pole to pole fault in a symmetrical monopole configuration will result in a high magnitude of fault currents which is driven by the converter [4], [5]. If the converter does not have the blocking capability, the fault current will rise to a value determined by the AC side reactance (transformer leakage reactance) or any other reactance within the circuit.

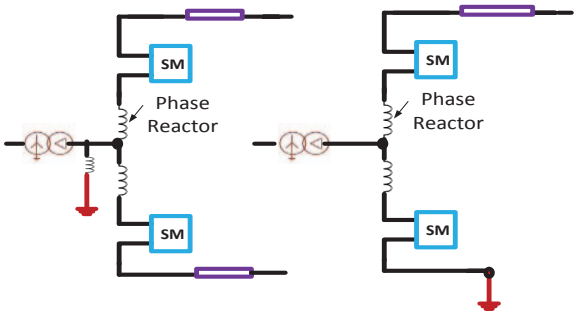


Fig. 2.2 MMC HVDC Configurations[4]
(a) Symmetrical monopole (b) Asymmetrical Monopole

Generally, the resulting magnitude of fault current in a pole to pole fault is larger compared to that of pole to ground, whereas the pole to ground faults are more common.

In all, the protection system for DC grid should possess the following attributes [7], [11].

- Able to discriminate between faults and normal load condition
- Must be insensitive to noise
- Must be transient based
- The primary protection should be a non-unit protection
- Must be capable of isolating only the faulty section in the event of a fault
- Has sufficiently fast DC breakers (for non-blocking converters)
- Offers a backup in the event of failure of the main protection.

This paper investigates the *di/dt* based DC line protection techniques with a view to ascertaining its suitability in DC grid protection.

3.0 The *di/dt* based Protection Systems

The rate of rise of current or *di/dt* based DC line protection systems use the initial rate of rise of fault current to determine whether or not a fault has occurred in a line. A DC line fault is detected by comparing the incremental DC current at the converter station with a predetermined threshold for a pre-set time duration.

As shown in Figure 3.1, prior to a DC line fault, the current, *i* is in steady state so that the *di/dt* is ideally zero. During DC

short circuit, the calculated *di/dt* is greater than the *setting value* which is usually determined after considering all operating conditions including overloads. Also, depending on the direction of fault with respect to the local relay, the calculated *di/dt* could be positive (for a forward directional fault) or negative (for a reverse directional fault).

However, and as will be observed later, this technique suffers some setbacks and as such, extreme care should be taken when deploying it as a primary protection for DC lines, in particular for the protection of MT-HVDC system; otherwise nuisance trips may result.

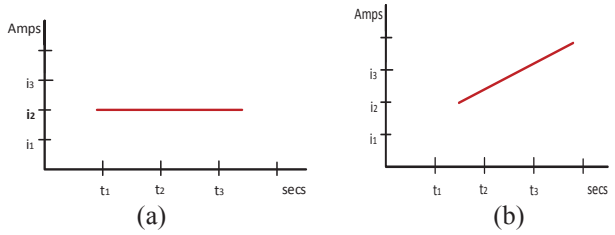


Fig. 3.1 *di/dt* Protection Technique by Sampling
(a)Pre-fault condition (b) Post-Fault Condition

$$\frac{di}{dt} \approx \frac{\Delta i}{\Delta t} \qquad (3.1)$$

$$\Delta i = i_3 - i_2 \; ; \quad \Delta t = t_3 - t_2$$

3.1 Limitations of *di/dt* Protection Technique

Fig. 3.2 shows a DC line supplying an arbitrary load of 100Ω. For clarity, the source is assumed to be ideal. The plots obtained following the application of a short circuit fault at *0.3secs* from the start of the simulation on the DC line for varying distances to the fault are shown in Figure 3.3. The parameters used are given in Table 3.1 and the Bergeron model was used to simulate the transmission line.

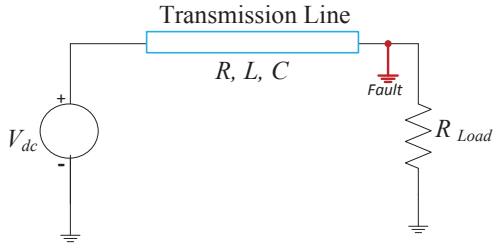


Fig. 3.2 Ideal DC Network

As shown in Figure 3.3, there are no appreciable differences in their initial *di/dt;* which shows that the distance to the fault cannot be established by the measurement of initial *di/dt* alone. However, the average *di/dt* or *"trend"* in *di/dt* as shown by the dotted line of Figure 3.3 which was obtained by regression analysis (Equation 3.1) varies with the fault distance and therefore may be suitable for locating the fault in the line under consideration.

Table 3.1 Parameter of Figure 3.2 [15]

DC Voltage , V_{dc}	*400kV*
Cable resistance, R	*10mΩ/km*
Cable Inductance, L	*0.16mH/km*
Cable Capacitance, C	*0.15μF/km*

$$di/dt_{(Trend)} \approx \frac{n\sum it - (\sum t)(\sum i)}{n\sum t^2 - (\sum t)^2} \qquad (3.1)$$

Where *n* is the number of data points

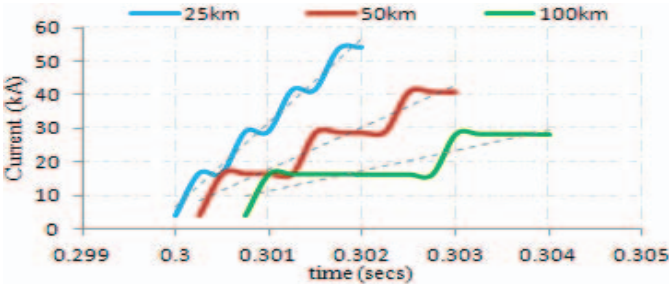


Fig. 3.3 Plots of current for varying Fault Distance

The initial *di/dt* is dependent on the magnitude of the *surge impedance*, due to which the initial *di/dt* is the same as the scenarios that the fault location is different. This phenomenon is caused by travelling wave propagation and is explained in the following section.

3.2 The Phenomenon of Travelling Wave

The notion of a gradual exponential rise of the current in inductive circuits during an abrupt change in the circuit conditions - such as switching or fault conditions does not actually hold in *true* transmission lines as travelling wave phenomenon must be considered[16].

When a short-circuit suddenly occurs in a transmission line, a wave of $-v_{dc}$ travels towards the source, reducing the line voltage to zero[16]. This wave is accompanied by a current wave of magnitude $+v_{dc}/Z_C$. Conventionally, it is assumed that the positive direction of current flow is from the source towards the transmission line. Generally, boundary conditions demand that at the short circuit, the voltage is zero and at the source, it is v_{dc}. When this wave reaches the source, a new wave of $+v_{dc}$ is reflected, and its associated current is $+v_{dc}/Z_C$. This reflected wave from the source again reaches the short circuit and the cycle continues. The time taken for the wave to travel from the fault to the source is referred to as the transit time, τ. This implies that the effect of the short circuit is not felt at the source until after τ seconds.

Based on this back and forth movement of the wave, the current at both the source and short circuit increases in discrete steps of $2v_{dc}/Z_C$ every 2τ seconds. This is illustrated in Figure 3.4.

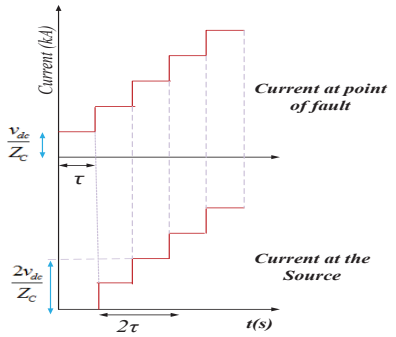


Fig. 3.4 Ideal Profile of Fault current during short circuit[16]

The average rate of rise of the current is therefore given as

$$\left|\frac{di}{dt}\right|_{(Average)} = \frac{2v_{dc}}{2Z_C\tau} \qquad (3.2)$$

$$Z_C = \sqrt{L/C}\ ;\ \tau = l_f/c;\ c = 1/\sqrt{LC}$$

Z_C=*Surge Impedance*

c=*Velocity of the wave*

l_f=*distance to fault*

Further simplification results in Equation 3.3.

$$\left|\frac{di}{dt}\right|_{(Average)} = \frac{v_{dc}}{l_f L} \qquad (3.3)$$

Generally, this is an ideal case as the effect of the resistive and dielectric losses will provide damping, and the current will attain steady state. Based on Equations 3.1 and 3.3, the distance to fault was estimated and the results (Table 3.2) show consistency in using both equations in estimating the distance to the fault.

Table 3.2 Calculated *di/dt* for varying Fault distances

Fault Distance (km)	*Trend in di/dt (kA/ms)*	
	Regression Analysis	$v_{dc}/l_f L$
25	26.7	25
50	13.3	12.5
100	0.67	0.62

4.0 Full Scale Simulation Studies Based on MMC-HVDC System

A similar study was carried out on a full scale MMC-HVDC system (Figure 4.1) and the transmission line was modelled by the frequency dependent distributed line Model provided by Manitoba HVDC Research Centre. The model parameters are given in Table 4.1 and Figure 4.2 respectively. All measurements are taken at the rectifier terminal, and all direction of faults are with respect to relay R_1; and from the positive pole. A positive pole to ground fault was assumed in this study.

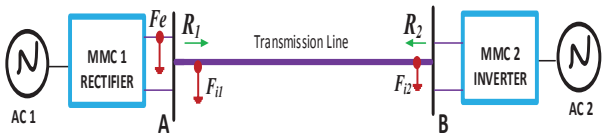


Fig. 4.1 Full Scale MMC-HVDC

Simulations were carried out and the fault applied at *2s* from the start of the simulation. Three arbitrary fault positions were considered - F_{i1}, F_{i2} and F_e. With respect to relay R_1, F_{i1}, and F_{i2} are forward faults whilst F_e is a reverse fault. F_{i1}, F_{i2} corresponds to *5%* (20km) and *95% (380km)* of the line length. These were selected in other to investigate the behaviour of both close-up and remote fault on the fault current profile. All fault distances are with respect to the rectifier terminal, where relay R_1 is located. Generally, the relay should operate for forward directional faults and restrain for reverse directional faults.

The plots of the fault current for the three different fault scenarios are shown in Figure 4.3

Table 4.1. The Model Parameters

Rated MVA of Converter	*1000MVA*
P-N Voltage, v_{dc}	*640kV*
Nominal voltage at Grid Side	$230kV_{(L\text{-}L),}$
Nominal Voltage at VSC Side	$370kV_{(L\text{-}L),}$
Leakage Reactance of Transformer	*0.15pu*
Arm Reactor	*50mH*
Sub-module Capacitor	*2800μF*
Height of all conductors	*13.2m*
Shunt Conductance	$1\times10^{-11}mho/m$
Outer radius of conductor	$3.8\times10^{-2}m$
Relative Permeability, μ_r	*1*
Length of Transmission Line	*400km*

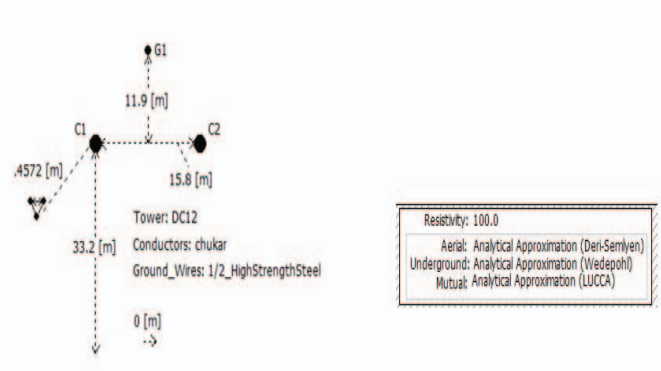
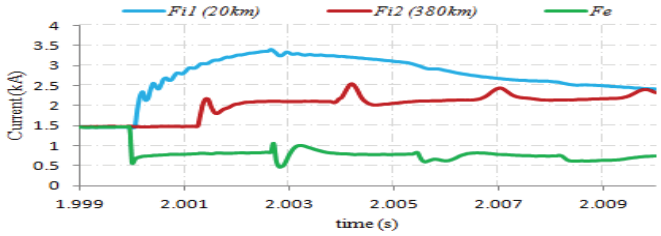


Fig. 4.2 Conductor Configuration



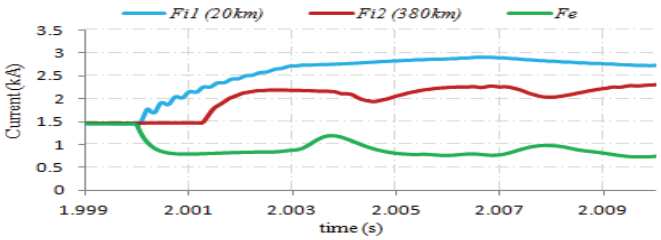
F_{i1}, F_{i2}: *Forward Directional Faults*
F_e: *Reverse Directional Fault*

Figure 4.3 Plots of Fault Current

As shown in Figure 4.3, their initial *di/dt* is consistent with those in the plots shown in Figure 3.3. Also, there are oscillations in the fault current profile which are due to the effect of the transmission line parameters. In practice, these effects can result in errors in extracting samples for the purpose of calculating the actual *di/dt.* This is because the measurement time window may coincide with the time when the fault current profile attains its local maximum/minimum; or when it appears to have a zero *di/dt* for a considerable length of time. Also, depending on the measurement period or fault distance, the calculated *di/dt* may vary between positive and negative values. This is independent of the actual direction of the fault.

A *100mH* DC smoothing reactor located at both ends of the line [10]; which is representative of a DC breaker located on the line ends (Figure 4.4) could limit the *di/dt* as shown in Figure 4.5, whereas the limitations explained above still persist. Generally, with respect to relay R_1, faults behind relay R_2 would be attenuated by inductor L_2 (Figure 4.4), whereas the time during which samples are taken still play a major role in the decision made by the relay.

Fig. 4.4 Full Scale MMC-HVDC with *di/dt* Limiting Inductor

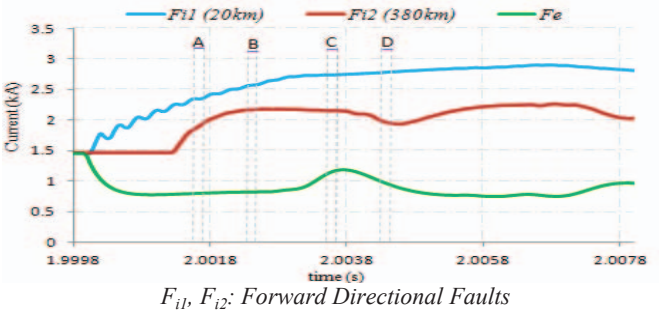


F_{i1}, F_{i2}: *Forward Directional Faults*
F_e: *Reverse Directional Fault*

Figure 4.5 Plots of Fault Current with *di/dt* DC inductors

Now, as the actual *di/dt* can either be positive for a forward directional faults (F_{i1}, and F_{i2} as shown) or negative for reverse directional faults (F_e as shown), nuisance trips may result. This is because any measurement taken during the time soon after the local maximum/minimum in the fault current profile will indicate a reverse or forward directional faults respectively. The converse is the case for measurements taken just before the local maximum/minimum. This actually may not be the case. This is illustrated in Figure 4.6.

The relay trip table based on Figure 4.6 is also shown in Table 4.2. An arbitrary window length has been chosen for ease of clarity.



F_{i1}, F_{i2}: *Forward Directional Faults*
F_e: *Reverse Directional Fault*

Fig. 4.6 Forward and Reverse Faults showing Measurement period

Table 4.2 Relay Trip table based on Figure 4.6

Measurement Window	*Sign of di/dt*						*Relay Decision*						*Status of Trip*		
	Calculated			*Actual*			*Calculated*			*Actual*			F_{i1}	F_{i2}	F_e
	F_{i1}	F_{i2}	F_e	F_{i1}	F_{i2}	F_e	F_{i1}	F_{i2}	F_e	F_{i1}	F_{i2}	F_e			
A	-	+	0	+	+	-	R	O	R	O	O	R	False	True	False[1]
B	-	0	0	+	+	-	R	R	R	O	O	R	False	False	False[1]
C	0	0	+	+	+	-	R	R	O	O	O	R	False	False	False
D	0	-	-	+	+	-	R	R	R	O	O	R	False	False	True

Actual di/dt is positive(+ve), negative (-ve) and zero for forward faults, reverse faults and normal operating condition respectively
O: Operate: R: Restrain

[1] With respect to relay R_1, the calculated *di/dt* must be negative for fault F_e. This was calculated to be '*zero*' hence regarded as a '*false*' trip..

5.0 Conclusions

This paper examined the *di/dt* protection technique with a view to ascertaining its suitability for the protection of DC grid. Some of the limitations of *di/dt* technique were found by using the travelling wave analysis to determine the fault current profile which demonstrated the oscillatory nature of the fault current. This leads to errors in estimating the actual *di/dt* since the profile may attain its local maximum/minimum before or during the time window set for the measurement. The initial *di/dt,* which is the same irrespective of the distance to the fault, is dependent on the magnitude of the surge impedance.

Furthermore, depending on the direction of the fault with respect to a local relay, the actual *di/dt* could be positive (for a forward directional fault) or negative (for a reverse directional fault). However, the calculated *di/dt* may give erroneous results since any measurement taken during the time soon after the local maximum or local minimum in the fault current profile will indicate a reverse or forward directional faults respectively; irrespective of the actual fault direction. This however, may not be the true case. Also, as the rate of rise is usually obtained by sampling the current at 96*kHz* and therefore due to the oscillations in the fault current profile, resulting from the distributed nature of the line parameters, the actual initial *di/dt* is not measureable in the time available.

The attenuation provided by the *di/dt* limiting inductor would in general, provide a good discriminant between *internal* and *external* faults, yet the time on the fault current profile when the samples are taken still plays a major role in the validity of the decision made by the relay, noting that the fault distance may vary.

From the forgoing, it can be seen that the *di/dt* based protection technique suffers some disadvantages and as such, extreme care should be taken when deploying it for the protection of DC lines, in particular for the protection of MT-HVDC system; otherwise nuisance trips may result. Protection philosophies based on the traditional distance protection philosophy applicable to HVAC systems as well as those based on travelling waves are possible research direction in this regard. These will be explored and the finding presented in the near future.

It is hopeful that this paper will contribute to the discussions involving the development of suitable protection algorithms for the proposed DC grids.

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