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Performance Analysis of a Three-to-Five Phase Dual Matrix Converter Based on Space Vector Pulse Width Modulation

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ABSTRACT In this paper, space vector pulse width modulation (SVPWM)-based algorithms for a five-phase open-end load fed from dual matrix converter (DMC) have been proposed. In the presented modulation methods, the reference output voltage vector is synthesized from two three-to-five phase matrix converters at both the ends of the load. Depending on the power-sharing of the two MCs, two proposed modulation methods are defined as equal reference sharing (ERS) and unequal reference sharing (URS). The performance of ERS and URS for the three-to-five phase DMC drive is compared. Performance comparison is based on the total harmonic distortion in the output voltages and the percentage of the voltage transferred from the source to the load, for the full linear modulation index (MI) range. Common mode voltage and zero sequence current in the load are also discussed. The efficiency of the ERS and URS is compared. It has been observed that the proposed ERS scheme offers better performance compared with URS for most of the MI values. The suggested modulation techniques are implemented in MATLAB/Simulink. The hardware setup is developed and control algorithm is implemented using dSPACE working in conjunction with the FPGA interface board for practical validation.

INDEX TERMS Dual matrix converter, modulation index, multiphase, open-end load, space vector pulse width modulation.

I. INTRODUCTION

The multiphase drive system is a viable alternative for high power industrial applications. Multiphase drive systems are accompanied with; improved fault tolerance, reduced torque pulsation, and reduced power converter switch rating. All AC machines require only two current components (namely d-q) for independent torque and flux control. An n-phase machine can continue to operate due to the presence of a rotating field in the post-fault operation as long as no more than (n-3) phases are faulted. Most power supply schemes, discussed in conjunction with both three-phase and multiphase machine drive systems, are of a so-called single-sided supply type. This means that the machine has an isolated neutral point and power converter feeds it from the available terminals. However, it is also possible to realize the machine supply system using different schemes. For example, the stator windings are fully opened from both the ends and two converters (rather than one) can be used to supply it from both sides.

This structure is known as open-end winding (OEW) machine fed from the dual converter. It has been under extensive investigation [1]–[3]. The OEW machine drive system offers numerous advantages over a conventional single-sided drive system. Some of them are: i) each of the converters is rated to one half of the total power, if both of them share the power equally, ii) there is a possibility for CMV reduction (for isolated dual supply system only) iii) fault tolerance is improved due to power converter supply redundancy [4], [5]., iv) multilevel output is achieved and the number of levels in the output voltage can be varied by changing the DC link voltage ratio (if inverters are used). Though, OEW drive can have some shortcomings, such as [6], [7]: zero sequence current might flow in the winding of the machine due to the zero sequence voltage. Moreover, a complex power converter is required which has more circuit gate drives and more power electronics devices, etc. A comparative study of the open-end topology has been done with equivalent

TABLE 1. Comparison of five-phase DMC with the same power rated existing topologies.

Parameters	Multilevel matrix converter	Single matrix converter	Dual matrix converter
Number of switches	45 H bridge cells, each cell contains 4 transistors and one capacitor	30 IGBTs	60 IGBTs
Power handling capability	High/Medium	Medium	High/medium
Voltage gain	$0 \leq V_o \leq 1 \times V_{in}$	$V_o \leq 0.7886 \times V_{in}$	$V_o \leq 1.5 \times V_{in}$
Fault tolerance	Good	Good	Better
Converter complexity	High	Medium	High
Clamping diodes	16	16	26
Switching losses	High	Medium	Medium
Efficiency	Low	High	High
Isolated Power supply	One	One	One/Two
Switching devices	Low voltage IGBTs	High voltage IGBTs	High voltage GBTs

existing converter topologies and results are organized in Table 1 [8]–[10].

Typically, two power supplies that have been considered with OEW topology are of either inverter [11]–[13] or an MC type [14]–[17]. The number of levels of the two supplying converters can be the same or different, with two isolated or non-isolated feeding sources. These combinations of supply systems are all available in the literature [11]–[17]. However, one should note that only a few works have been published in conjunction with multiphase OEW configuration, based on the DMC supply. Recently, three-to-five phase MC based OEW drive system is presented in [16]–[18], aiming to enhance the power transfer and generate sinusoidal output with reduced total harmonic distortion (THD).

Circulating currents have been observed in open-end load system because of the power semiconductor device voltage drops and the use of dead time operation between phase transitions [18]. In this paper, a five-phase open-end load configuration is obtained by connecting a simple three-to-five phase MC at each side of the load. Both the MCs were supplied from a common three-phase source. In such a configuration, it is essential to eliminate the CMV that is inevitably created by usual PWM control strategies [19], [20]. Some literature reported on these issues of circulating currents and CMV cancellation in the OEW fed by dual inverters [18]–[21], and by DMCs [22], [23]. However, the main focus of this paper is not the CMV and circulating currents, but to get the optimum condition for sharing the power of both MCs by controlling the reference voltage space vectors and analyze the system.

In this paper, a single-sided three-to-five phase MC is extended to dual three-to-five phase MC. To control the MC, an indirect approach is adopted in which MC is considered as a combination of a three-phase rectifier and five-phase inverter without the DC link capacitor. In the inverter stage, the reference voltage vectors are controlled on the basis of the power-sharing of the load. The power-sharing can be done in two ways, either it is divided equally or unequally between two MCs. Hence, they are named ERS and URS scheme. In the ERS scheme, both MCs are modulated with the same voltage reference. Whereas, in the URS scheme,

both of the MCs share the output voltage reference unequally. The pattern of reference sharing is explained in section III. The objective of the modulation is to find the condition for the maximum output voltage transferred to the load. In the DMC control schemes, the output voltage is obtained to 150% of the input voltage. The proposed SVPWM strategies choose the converter switching sequences by preferring the space vectors in the first *d-q* plane and eliminating the effects of the vectors in the *x-y* plane. The algorithm is tested with a five-phase open-ended R-L load. The performance of ERS and URS for three-to-five phase DMC is compared with each other. Simulation and experimental results are presented for the verification of the proposed schemes.

II. SVPWM CONTROL STRATEGY FOR THREE-TO-FIVE PHASE MATRIX CONVERTER

The output voltage v_o and the input current i_i are taken as reference quantities in the control of an MC. Since the input phase voltage vector e_i is imposed by the source voltages and is also known by measurements, the control of ϕ_i (displacement angle between voltage and current) can be achieved by controlling the phase angle α_i of the input current vector [24]. The input reference current angle from the d-axis of the input current space vector is α_i.

A. SPACE VECTOR PWM CONTROL OF INPUT CURRENT
The space vector diagram of the input currents, obtained from equation (1), is shown in Fig. 1.

$$\bar{i}_i = \frac{2}{3}\left(i_a + \kappa i_b + \kappa^2 i_c\right), \quad \kappa = e^{j\frac{2\pi}{3}} \quad (1)$$

There are nine possible switching combinations that generates nine different space vectors. These space vectors are spanned over six sectors (S1...S6). In Fig. 1(a), a, b and c indicate the input phases of the converter. Fig. 1(b) shows the sector S1 that span from $-30°$ to $30°$. The input reference current is determined by the two neighboring current vectors. Thus, input reference current in sector S1 can be decomposed along two adjacent space vectors i_γ and i_δ.
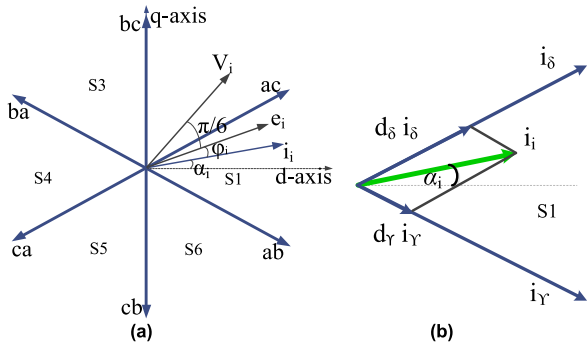
FIGURE 1. Three-to-five phase indirect matrix converter, (a) input current space vectors (b) generation of reference current for sector I.

The duty ratios of current space vectors of the rectifier stage can be expressed as:

$$d_\gamma = \frac{T_\gamma}{T_s} = m_r \times \sin\left(\frac{\pi}{3} - \alpha_i\right) \qquad (2)$$

$$d_\delta = \frac{T_\delta}{T_s} = m_r \times \sin(\alpha_i) \qquad (3)$$

$$d_0 = \frac{T_0}{T_s} = 1 - d_\gamma - d_\delta \qquad (4)$$

where T_s is the switching period, T_γ and T_δ are the time of operation, d_γ and d_δ are the duty ratio of current vectors I_γ and I_δ, respectively. The MI of the rectifier stage (m_r) is defined by equation (5). In equation (5), I_{dc} is the current of fictitious DC bus.

$$0 \le m_r = I_i/I_{dc} \le 1 \qquad (5)$$

B. SPACE VECTOR PWM CONTROL OF OUTPUT VOLTAGE

Output line voltage space vector is defined by:

$$\overline{V_o} = \frac{2}{5}(v_{AB} + \zeta v_{BC} + \zeta^2 v_{CD} + \zeta^3 v_{DE} + \zeta^4 v_{EA}) \qquad (6)$$

For the voltage in the d-q plane, $\zeta^\psi = e^{j\frac{2\pi\psi}{5}}$, $\psi \in 1, 2, 3, 4$, whereas for the x-y plane $\zeta^\psi = e^{j\frac{4\pi\psi}{5}}$. The space vectors V_{dq} and V_{xy} are shown in Fig. 2(a) and 2(b), respectively. There are 30 active and 2 zero vectors forming three concentric decagons. It can be divided into ten distinct equally spaced sectors named sector I to sector X. The outer decagon contains vectors called 'large' vectors; the medium decagon is formed by 'medium' vectors and the inner decagon is formed by 'small' vectors. The respective lengths of the output line voltages are $V_{large} = 0.763$p.u., $V_{medium} = 0.472$p.u., $V_{short} = 0.292$ p.u.. The reference voltage space vector V^* at an angle of α_o is shown in Fig. 2(c). The reference output voltage in sector I can be decomposed along the two adjacent space vectors. These are denoted by V' and V''.

Out of 6 voltage space vectors in sector I, two are small (V_1, V_2), two are medium (V_{11}, V_{12}) and two are large length vectors (V_{21}, V_{22}). Among these, two vectors (V_{11}, V_{21}) are selected along V' and (V_{12}, V_{22}) are selected along V'' for the synthesis of the reference output voltage.
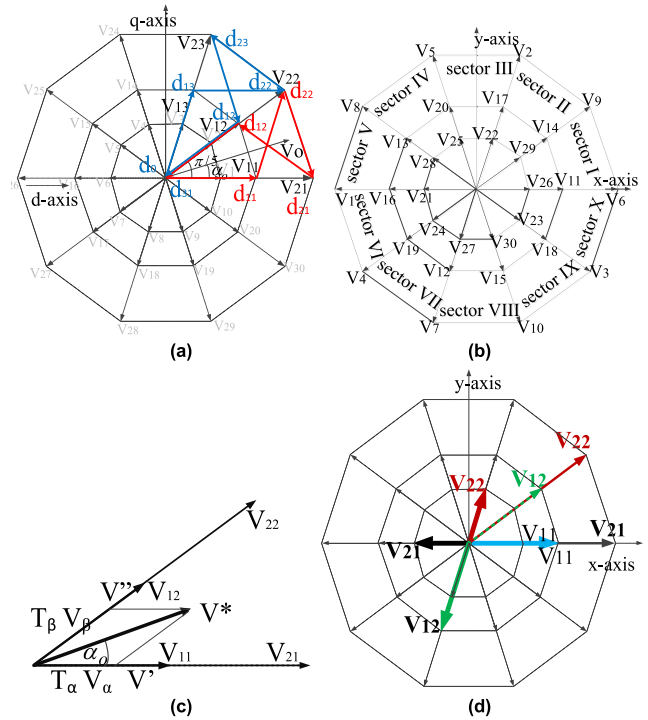

FIGURE 2. (a) Output voltage space vectors in the *d-q* plane, (b) Output voltage space vectors in the *x-y* plane, (c) Example of the reference voltage for sector I, (d) Minimization of *x-y* voltage components in sector I.

To achieve the minimum *x-y* effect in the output voltage, the selection of voltage vectors with their operation time is explained with the help of Fig. 2(d). The large vector with 0° angles is having a small length *x-y* component in the direction of 180°. Similarly, it is shown for all four active vectors. By proper adjustment of voltage × time ($V \times t$) application of vectors, the effect of the *x-y* component can be eliminated, i.e. a large vector which causes smaller *x-y* is operated for longer than the medium vector. The operation time is shared as $V_{21} \times t_{21} = V_{11} \times t_{11}$.

Assuming the time of application of a reference vector projected onto V' is T_α and onto V'' is T_β and the zero vector application time is T_0 (where the total switching period is T_s), one can write:

$$V^* \times T_s = V_\alpha \times T_\alpha + V_\beta \times T_\beta + V_0 \times T_0 \qquad (7)$$

In Cartesian form, it can be re-written as:

$$\begin{aligned}|V^*| &(\cos(\alpha_0) + j\sin(\alpha_0)) T_s \\ &= |V_\alpha| (\cos(0) + j\sin(0)) T_\alpha \\ &+ |V_\beta| \left(\cos\left(\frac{\pi}{5}\right) + j\sin\left(\frac{\pi}{5}\right)\right) T_\beta\end{aligned} \qquad (8)$$

By equating real and imaginary parts on the left and right-hand sides of the equation, and generalizing the equation for all sectors equations (9)-(11) can be obtained. In these equations, k is the sector number that can vary from 1 to 10.

$$T_\alpha = \frac{|V^*| \sin\left(k\frac{\pi}{5} - \alpha_0\right)}{|V_l| \sin\left(\frac{\pi}{5}\right)} T_s \qquad (9)$$

TABLE 2. Switching sequence and their commutations (blue circles) in a switching cycle in sector I.

Input Phase a,b,c	Output phases					Output line voltage				
	A	B	C	D	E	V_{AB}	V_{BC}	V_{CD}	V_{DE}	V_{EA}
b, b	b	b	b	b	b	0	0	0	0	0
a, b	a	b	b	b	b	V_{ab}	0	0	0	$-V_{ab}$
a, b	a	a	b	b	b	0	V_{ab}	0	0	$-V_{ab}$
a, b	a	a	b	b	a	0	V_{ab}	0	$-V_{ab}$	0
a, b	a	a	a	b	a	0	0	V_{ab}	0	$-V_{AB}$
a, a	a	a	a	a	a	0	0	0	0	0
a, c	a	a	a	c	a	0	0	$-V_{ca}$	V_{ca}	0
a, c	a	a	c	c	a	0	$-V_{ca}$	0	V_{ca}	0
a, c	a	a	c	c	c	0	$-V_{ca}$	0	0	V_{ca}
a, c	a	c	c	c	c	$-V_{ca}$	0	0	0	V_{ca}
c, c	c	c	c	c	c	0	0	0	0	0

$$T_\beta = \frac{|V^*| \sin\left(\alpha_0 - (k-1)\frac{\pi}{5}\right)}{|V_l| \sin\left(\frac{\pi}{5}\right)} T_s \qquad (10)$$

$$T_0 = T_s - T_\beta - T_\alpha \qquad (11)$$

To produce zero average voltage vectors in the *x-y* plane, the application time of the large and medium length voltage vectors are calculated from T_α, T_β and presented as $T_{\alpha L}$, $T_{\beta L}$.

$$\frac{T_{\alpha L}}{T_{\alpha M}} = \frac{T_{\beta L}}{T_{\beta M}} = \frac{V_L}{V_M} = x = 1.618 \qquad (12)$$

$$T_{\alpha L} = \frac{|V^*| \sin\left(k\frac{\pi}{5} - \alpha_0\right)}{|V_M| \sin\left(\frac{\pi}{5}\right)} \left(\frac{x}{1+x^2}\right) T_s \qquad (13)$$

$$T_{\beta L} = \frac{|V^*| \sin\left(\alpha_0 - (k-1)k\frac{\pi}{5}\right)}{|V_M| \sin\left(\frac{\pi}{5}\right)} \left(\frac{x}{1+x^2}\right) T_s \qquad (14)$$

$$T_{\alpha M} = \frac{|V^*| \sin\left(k\frac{\pi}{5} - \alpha_0\right)}{|V_L| \sin\left(\frac{\pi}{5}\right)} \left(\frac{x}{1+x^2}\right) T_s \qquad (15)$$

$$T_{\beta M} = \frac{|V^*| \sin\left(\alpha_0 - (k-1)k\frac{\pi}{5}\right)}{|V_L| \sin\left(\frac{\pi}{5}\right)} \left(\frac{x}{1+x^2}\right) T_s \qquad (16)$$

$$T_0 = T_s - T_{\beta L} - T_{\alpha L} - T_{\beta M} - T_{\alpha M} \qquad (17)$$

One possible switching pattern for sector I of the output voltage of the MC, with the switching commutations, is shown in Table 2, where the corresponding output line voltages are also shown. It is observed that total switching commutations in a switching cycle are 10, irrespective of sectors.

The dwell times of different space vectors used for the implementation of SVPWM is the same in both of the control techniques of the DMC. The only difference is that the voltage reference for MC2 is 180° shifted in phase from the MC1. Though, in the rectification stage, input current reference remains the same for both MCs.

III. SVPWM CONTROL STRATEGY FOR DUAL THREE-TO-FIVE PHASE MATRIX CONVERTER

The proposed control schemes are shown in Fig. 3. The reference voltage applied in the modulation is apportioned
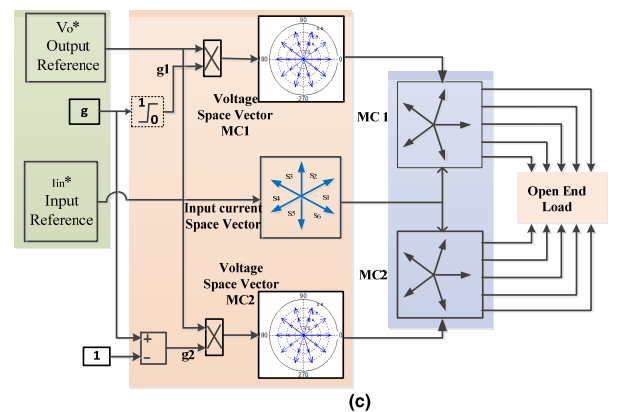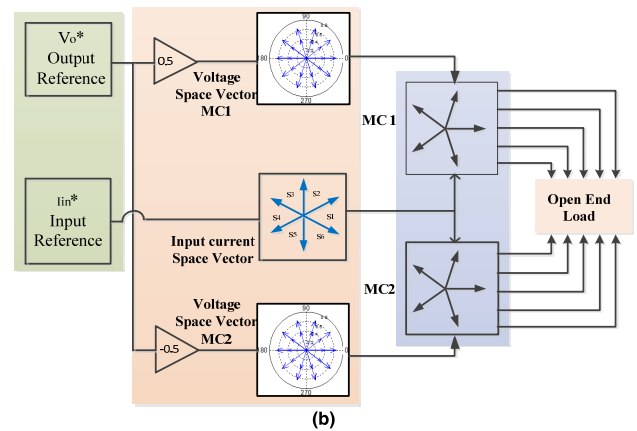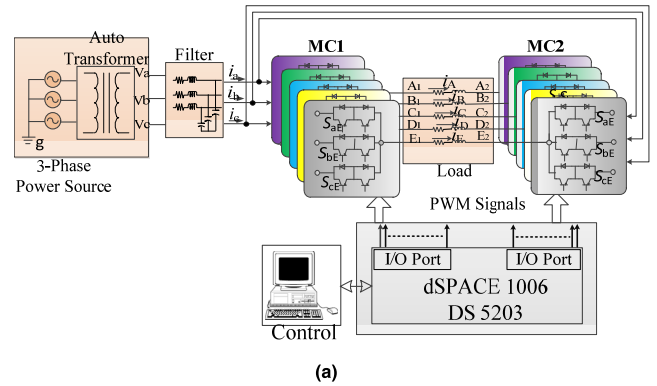
FIGURE 3. Topology and control for Dual Matrix Converter, (a) DMC fed five-phase open-end load, (b) ERS and (c) URS scheme.

according to the MI. These modulation concepts were introduced for voltage source inverter fed multiphase OEW drives topologies in [20]. With this modulation method, the load is supplied with a double of the maximum MI of a single MC. For a single three-to-five phase MC, it is calculated below in the equations (18)-(20).

The modulation of the rectifier stage (m_r) varies with the input current reference angle α_i in a sector. The voltage transfer to the output of the rectifier is given by (18) [26]. The maximum possible value of m_r is:

$$m_r = \frac{3}{2} \left.\frac{1}{\cos(\alpha_i)}\right|_{min} = 1.5 \qquad (18)$$

The maximum MI of the inverter stage m_{inv} can be calculated as [27]:

$$m_{inv} = \frac{\sin(\pi/5)(L + 0.618M)}{2\sin(\pi/10)\cos(\alpha_0)(1.618)}\bigg|_{max} = 0.5257 \quad (19)$$

where M and L are the medium and large length of the voltage space vector, α_o is the reference output voltage angle in a sector that varies from 0° to 36°. The factor 0.618 comes from the time of operation of M and L length vectors to cancel the x-y effect of voltage space vectors, i.e. due to the allocation of 61.8% more dwell time to a large space vector compared to a medium length space vector. Thus, a zero average voltage is produced in the x-y plane. The MI of MC is defined as a product of the modulation indices of the rectifier and the inverter stage and can be calculated as:

$$m_{3-5} = m_r \times m_{inv} = 1.5 \times 0.5257 = 0.7886 \quad (20)$$

The MI for the two modulators denoted as g_1 and g_2. If the maximum MI for each MC is assumed to be 1 (p.u.), then DMC will be able to operate up to MI value of 2 units. This would be the maximum possible value of total MI g. The reference output voltage vector can be synthesized in two different ways: i) reference voltage is divided equally between the two MCs to control the output voltage of the inverting stages – ERS scheme, ii) reference voltage is divided in such a way that up to the full linear modulation range of the first one i.e. up to 1 p.u. (maximum value of g_1), only MC1 is operated. If the MI of DMC exceeds this value (i.e. if $g > 1$), then the second matrix converter (MC2), becomes operational with the exceeding value of the MI ($g_2 = g - 1$). This is called URS scheme. Note that, there is no change or difference in the operation of the rectifier stage for both schemes. Values of g_1 and g_2 for ERS and URS control scheme can be mathematically defined as:

$$0 \leq g \leq 2 \rightarrow \begin{cases} g_1 = g/2 \\ g_2 = g/2 \end{cases} \quad \text{ERS} \quad (21)$$

$$0 \leq g \leq 1 \rightarrow \begin{cases} g_1 = g \\ g_2 = 0, \end{cases}$$

$$1 \leq g \leq 2 \rightarrow \begin{cases} g_1 = 1 \\ g_2 = g - 1 \end{cases} \quad \text{URS} \quad (22)$$

In Fig. 3, two MCs are denoted with indices 1 and 2. Legs of MCs are represented with their suffix 1 and 2 following the leg name A, B, C, D, and E.

Voltage space vectors of the inverter stage of the two MCs, in the d-q planes, are determined as:

$$V_{d1q1} = \frac{2}{5}\left(v_{A1} + \zeta v_{B1} + \zeta^2 v_{C1} + \zeta^3 v_{D1} + \zeta^4 v_{E1}\right)$$

$$V_{d2q2} = \frac{2}{5}\left(v_{A2} + \zeta v_{B2} + \zeta^2 v_{C2} + \zeta^3 v_{D2} + \zeta^4 v_{E2}\right) \quad (23)$$
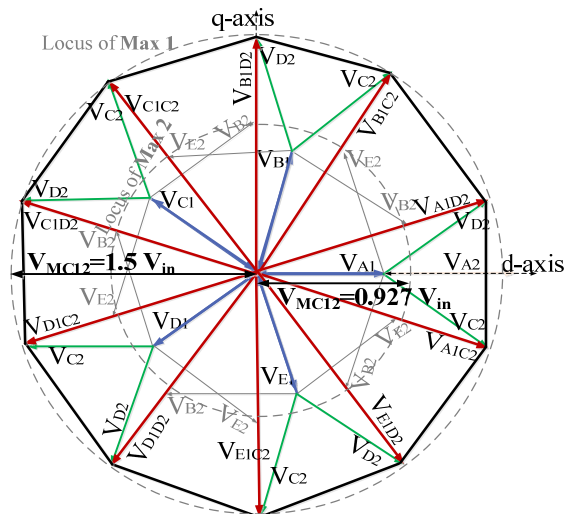

FIGURE 4. Synthesis of five-phase output voltage space vectors for the open-end load.

The dual-sided space vectors are obtained by using equation (24).

$$V_{dq} = \frac{2}{5}\left(v_{A1} + \zeta v_{B1} + \zeta^2 v_{C1} + \zeta^3 v_{D1} + \zeta^4 v_{E1}\right)$$
$$- \frac{2}{5}\left(v_{A2} + \zeta v_{B2} + \zeta^2 v_{C2} + \zeta^3 v_{D2} + \zeta^4 v_{E2}\right) \quad (24)$$

where $\zeta = e^{j\frac{2\pi}{5}}$.

The two sets of output voltage space vectors for MC1 and MC2 are shown in Fig. 4, in blue and green color, respectively. The obtained sets of space vectors are shown by red color. The generated voltages of MC1 and MC2, i.e. V_{A1} and V_{D2} results a DMC voltage vector V_{A1D2}. Both vectors are summed up and considering the maximum length of the individual space vectors for each MC. The resultant positions are shown in Fig. 4. The resulting output voltage vectors are shown in red color.

IV. COMMON MODE VOLTAGE AND ZERO SEQUENCE CURRENT IN THREE-TO-FIVE PHASE DUAL MATRIX CONVERTER
A. COMMON MODE VOLTAGE
In the case of DMC based open-end loads, the CMVs are generated at both of the load terminals [17]. The CMV at MC1, MC2, and DMC can be expressed as:

$$V_{CM1} = \frac{V_{A1} + V_{B1} + V_{C1} + V_{D1} + V_{E1}}{5} \quad (25)$$

$$V_{CM2} = \frac{V_{A2} + V_{B2} + V_{C2} + V_{D2} + V_{E2}}{5} \quad (26)$$

$$V_{CM} = V_{CM1} - V_{CM2} \quad (27)$$

In a single-sided supplied load, the CMV is defined as a voltage between the load neutral point and the ground of the source. In the case of an OEW, there is no common point at the load. Therefore, for measurement purpose, a very high shunt resistances are connected at the output of each MC

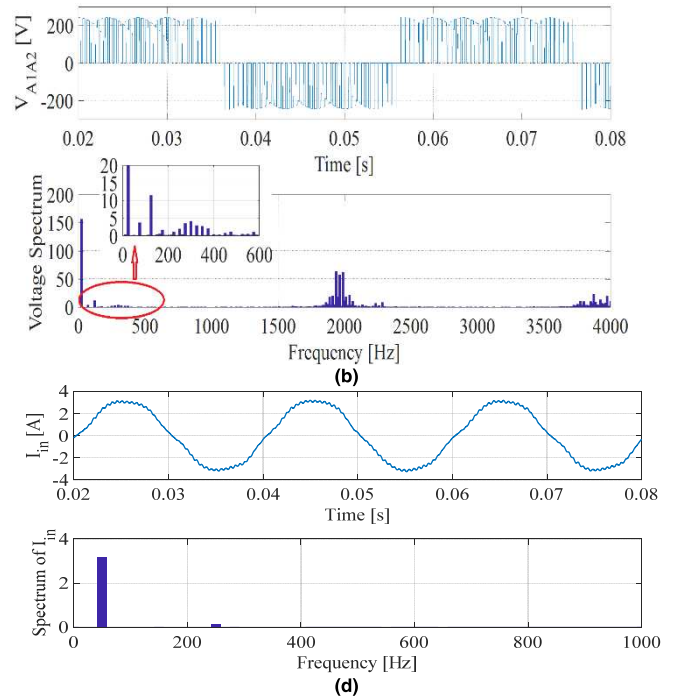**Equal Reference Sharing Scheme**
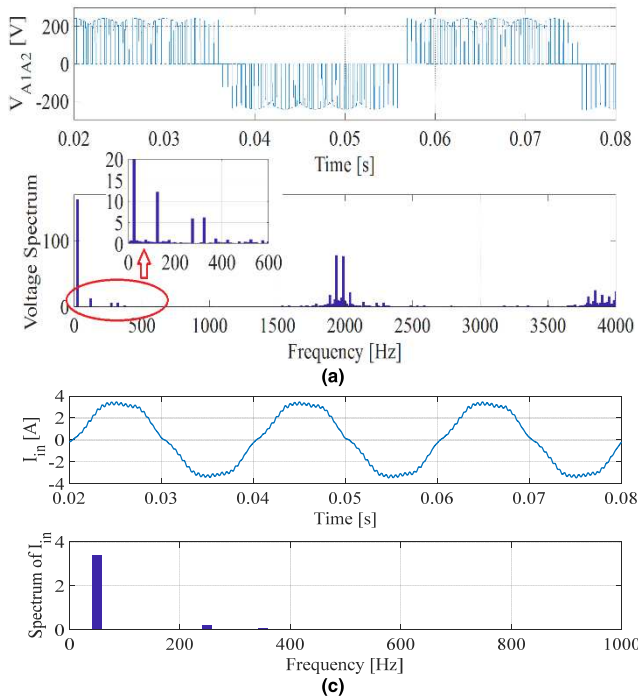
Unequal Reference Sharing Scheme

FIGURE 5. Simulation results for five-phase dual MC at $g = 1.4$. Output phase volatge (V_{A1A2}) with its spectrum for (a) ERS and (b) URS, and filtered source current with harmonic spectrum (c) ERS and (d) URS.

in star. The voltage between the created neutral points at MC1 and the ground of the source represents V_{CM1}. Similarly, the voltage V_{CM2} on MC2 can be measured. The difference between these two voltages gives the overall CMV [17].

B. ZERO SEQUENCE CURRENT IN THREE-TO-FIVE PHASE DMC

Due to a common source at both ends, inevitably a zero sequence current path will be developed from one side of the load terminal to the other [18]. The zero sequence current will flow through the closed path created by the open-end load and DMCs. The flow of this current can be measured by simply passing five-phase cables through a single current probe. As a result, the current measured is the sum of these five currents:

$$i_g = i_A + i_B + i_C + i_D + i_E = 5i_0 \qquad (28)$$

where, i_g is the ground current, i_0 is a zero sequence current and i_A, i_B, i_C, i_D, and i_E are five-phase load currents.

V. SIMULATION RESULTS

The modulation method is implemented as for indirect MCs. However, the rectifier and the inverter stage used space vectors can be combined in a simple way to control the direct MCs [25]. Hence, the six switching pulses for control of the rectifier switches and ten switching pulses for control of the inverter switches are mapped to control fifteen switches of the direct MC. Thus a direct MC output voltage is obtained only when the inverter leg 'A' upper switch and the rectifier

TABLE 3. Simulation parameters.

Source voltage	$V_{phase} = 100$ V rms
Load parameters (R-L)	$R = 75\ \Omega$, $L = 236$mH
Switching frequency	$f_s = 2$ kHz
Input frequency (f_{in})	f_{in}=50 Hz
Output frequency	f_{out}=25 Hz

leg 'a' upper switch are ON, or the inverter leg 'A' lower switch and the rectifier leg 'a' lower switch are ON. In this case, the input phase 'a' will be connected to the output 'A' of the MC. Similarly, inverter leg 'A' is applied AND/OR logic operation with the rectifier legs 'b' and 'c'. If similar conditions are fulfilled, the MC phase output will be directed to the input phase 'b' or 'c'. In this way, any of the three input phases can be linked to the output phase 'A' of the MC. Among three input phases, only one at a time will be passed to the output phase of the MC. The same strategy is followed for output phases 'B' 'C' 'D' and 'E'. In this way, in simulation as well as in the laboratory, direct MC is controlled using the indirect MC control approach.

A simple *R-L* load is considered to validate the control schemes for the DMCs. Simulation parameters are shown in Table 3. For both ERS and URS scheme the system is run at $g = 1.4$ per unit. For ERS scheme the reference voltages are generated with $g_1 = 0.7$ and $g_2 = 0.7$. The output voltage is double that of each MC output. For URS scheme, the same reference voltage is chosen. However, in this case,
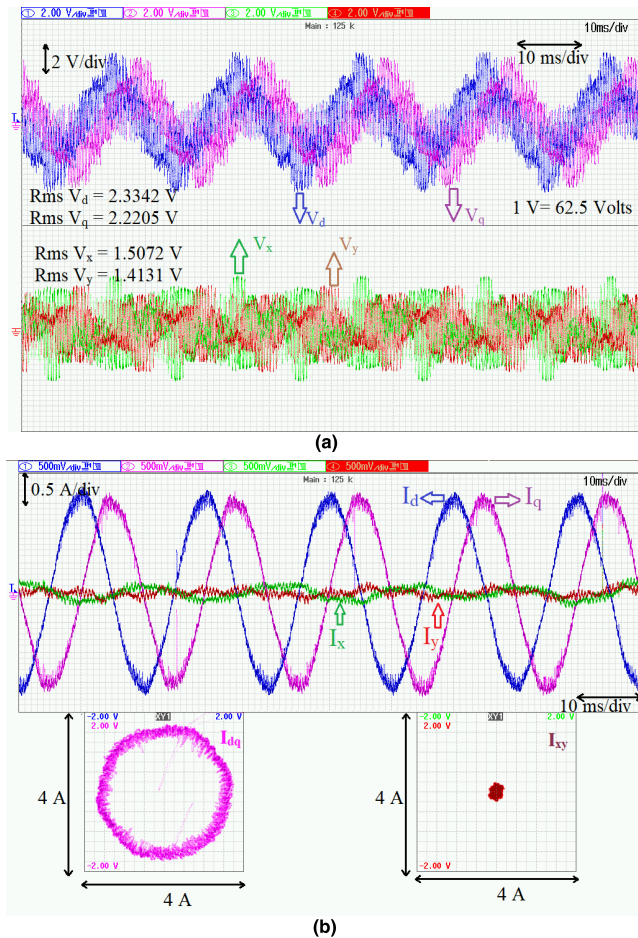
FIGURE 6. Three-to-five phase matrix converter. (a) V_{d-q} and V_{x-y} (b) I_{d-q} and I_{x-y}.

MC1 operates at its maximum limit (i.e. at 1.0), and the remaining value of g, i.e. 0.4, is used for g_2 to generate the reference voltage. Theoretically, the total voltage across the OEW should remain the same. However, it is different for both schemes. For ERS scheme, it is 115.3 V whereas, for URS scheme, it is 109.6 V. The simulation waveforms are shown in Fig. 5.

The effectiveness of the schemes is observed by the nature of the waveforms and the voltage transfer ratio. The phase voltage with its harmonic spectrum, for both modulation methods, is shown in Fig. 5(a) and 5(b). There are large switching harmonic components that appear as sidebands in the vicinity of the multiple of switching frequency. The input current is shown in Fig. 5(c) and 5(d), has very small low-order harmonics.

VI. EXPERIMENTAL RESULTS
For validation and testing a three-to-five phase DMC, the prototype is developed in the laboratory. The control code is developed in Simulink and built into dSPACE 1006, employed in combination with FPGA board DS 5203. A dead-band of 2 μs is implemented with a help of an external FPGA board programmed in VHDL.
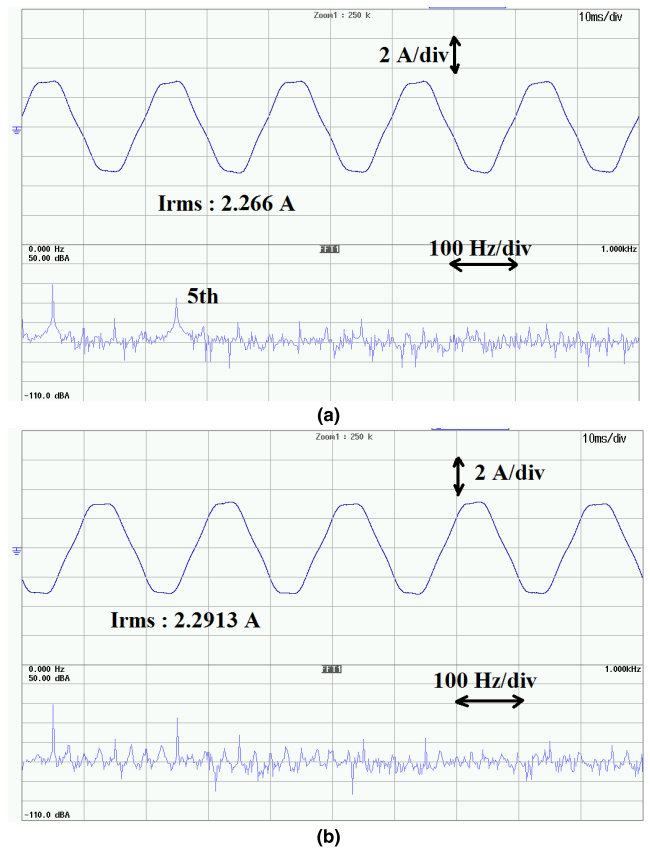
FIGURE 7. Experimental results for five-phase DMC source current with spectrum at $f = 25$ Hz and $g = 1.4$ [X-axis: 10ms/div, Y-axis: 2 A/div]. (a) ERS (b) URS.

Five-phase output voltage and currents in d-q and x-y planes are shown for three-to-five phase single-sided MC, in Fig. 6. Where the effect of x-y voltage is being eliminated in a sample time using the approach discussed in section IB. That is why current in the x-y plane is almost zero.

Fig. 7(a) and 7(b) show the input current waveforms, along with FFT spectra for an open-end R-L load at an input frequency of 50 Hz and total MI $g = 1.4$ units. It can be observed that the 5th harmonic are the most contributing to the THD expressed in the input current spectrum. The low pass filter with a cutoff frequency of 1600 Hz is applied.

Fig. 8(a) and 8(b) show the output voltage waveforms, along with FFT spectra at an operating frequency of 25 Hz and total MI $g = 1.4$ units. It can be observed that the 5th and 11th harmonic are the most contributing to the THD. 5th harmonics are due to the zero sequence component which causes a circulating current in the windings. ERS and URS scheme is operated under the same experimental conditions.

Theoretically, the overall voltage across the load should remain the same. However, in the practice, it is slightly different and for ERS $V_1 = 117.63$ V, while for URS $V_1 = 111.95$ V, i.e. the output voltage in case of URS is lower when compared with ERS case.

In Fig. 9(a) and 9(b), the balanced operation of DMC is shown through the load currents. Load phase current with its
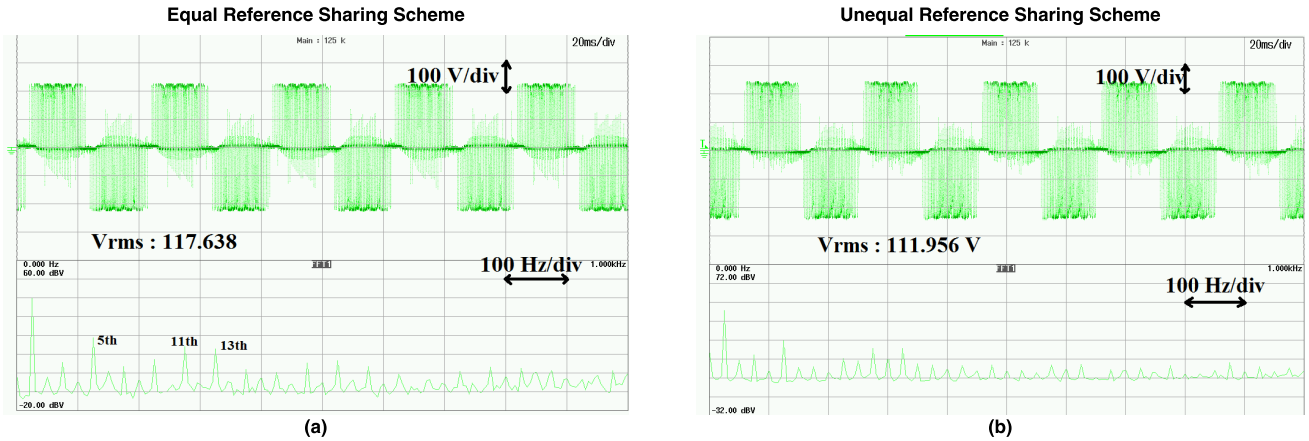
FIGURE 8. Experimental results for five-phase DMC following ERS and URS scheme at $f = 25$ Hz and $g = 1.4$. (a) and (b) Output phase volatge (V_{A1A2}) with spectrum.
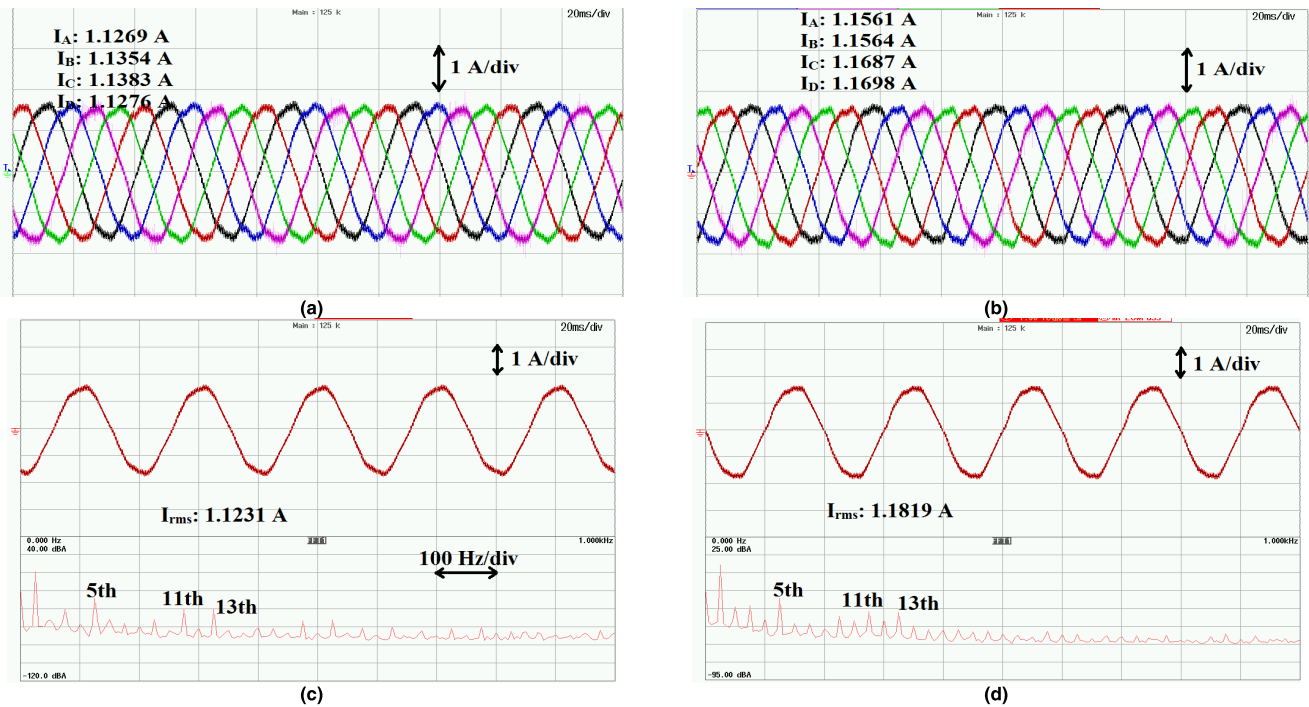

FIGURE 9. Experimental results for five-phase dual MC following ERS and URS scheme at $f = 25$ Hz and $g = 1.4$. (a) and (c) Balanced load currents [X-axis: 20ms/div, Y-axis: 1A/div] (c) and (d) Phase A load current with harmonic spectrum [X-axis: 20ms/div, Y-axis: 1A/div].

spectrum is shown in Fig. 9(c) and 9(d) for both proposed schemes.

CMV for both modulation schemes is measured with the use of star connected large resistors as explained in section IVA. The respective waveforms are shown in Fig. 10(a) and 10(b), where, V_{CM1}, V_{CM2}, and V_{CM} represents the CMV for MC1, MC2 and the difference between these two, respectively. It is observed that the peak value of the overall CMV and the number of levels are the same for both reference sharing schemes. It is seen that the peak value is 142 V, which is equal to the peak of the input phase voltage.

Zero sequence current is measured and presented in Fig. 10(c) and 10(d) for ERS and URS, respectively. It is

observed that in both modulation schemes, the zero sequence current is present. It is calculated by adding all line currents together. The current probe is giving the measured value in mV that is 10 mV/ 1A.

The measured value for ERS is 129.283 mV which corresponds to 129.283/100 A. Based on (29) this is equal to 5I0. Hence, I0 for ERS is 0.02586 A. Similarly, for URS I0 = 0.0264 A.

Note that the dead-time effect or any other nonlinear effects were not considered in the simulation. Some small differences between simulation and experimental can be observed in the current and voltage spectra. These are a consequence of the non-ideal nature of the experimental conditions
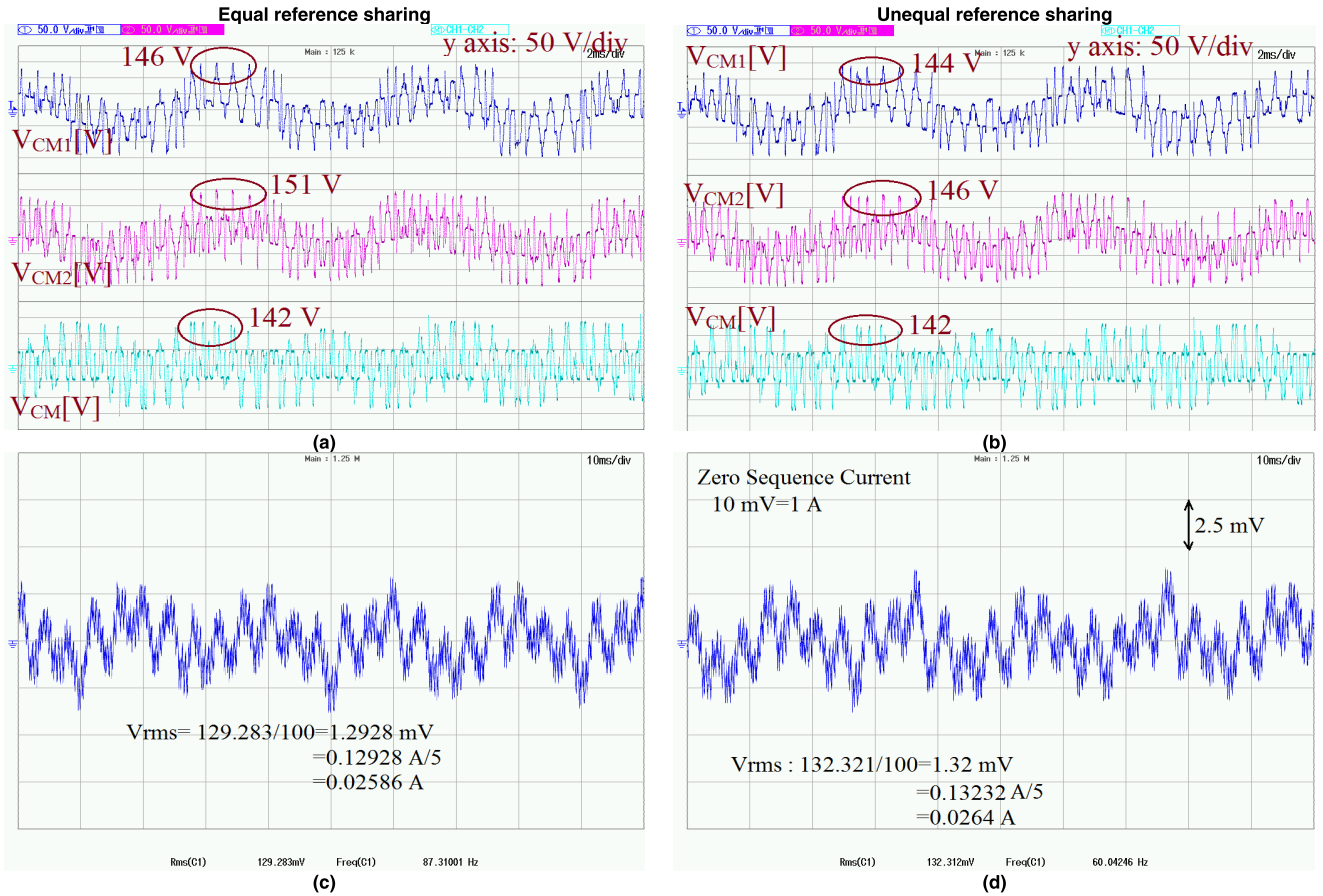
FIGURE 10. Five-phase open-end load fed from DMC and controlled by ERS and URS scheme at $f = 25$ Hz and $g = 1.4$. (a) and (b) Common mode voltage (c) and (d) Zero sequence current.

(dead-time effect etc.).Overall the experimental and simulation results agree well.

VII. PERFORMANCE ANALYSIS AND DISCUSSION

This section discusses the performance of the control techniques, based on the output voltage, THD and the converter efficiency at different modulation indices.

A. VOLTAGE TRANSFER TO THE LOAD

A generalized equation of the output voltage as a function of MI is derived. The generalized equation is a linear combination of known output function, and it is given as:

$$v_0 = \sum_{j=1}^{N} c_j v_j(g_1, g_2) \qquad (29)$$

where, v_0 is the output voltage from the DMC. The scaling coefficients c_j can be determined by the least square method while considering $v_j(g_1, g_2) \approx y_j$, where g_1 and g_2 are normalized modulation indices for MC1 and MC2, respectively. The number of samples is represented with j, and N is the total number of samples in the experiment. The error from the best-fitted equation in the ith sample is denoted as e_i. Error 'e'

can be described as:

$$e_i = y_i - v(g_1, g_2) \qquad (30)$$

The coefficient c_j is determined such that the second norms of (31), i.e. $\|e\|_2$ is minimized and the following expression is obtained:

$$\|e\|_2 = \|y - Bc\|_2$$

$$B = \begin{bmatrix} v_1(g_1^1, g_2^1) & v_2(g_1^1, g_2^1) & \cdots & v_n(g_1^1, g_2^1) \\ v_1(g_1^2, g_2^2) & v_2(g_1^2, g_2^2) & \cdots & v_n(g_1^2, g_2^2) \\ \vdots & \vdots & \cdots & \vdots \\ v_1(g_1^k, g_2^k) & v_2(g_1^k, g_2^k) & \cdots & v_n(g_1^k, g_2^k) \end{bmatrix}$$

$$c = \begin{bmatrix} c_1 \\ c_2 \\ \vdots \\ c_n \end{bmatrix} \quad and \quad y = \begin{bmatrix} y_1 \\ y_2 \\ \vdots \\ y_n \end{bmatrix} \qquad (31)$$

The coefficient of determination (R^2) which determines the accuracy is given by:

$$R^2 = 1 - \frac{\|e\|_2^2}{\sum_{i=1}^{n} (y_i - \bar{y})^2} \qquad (32)$$
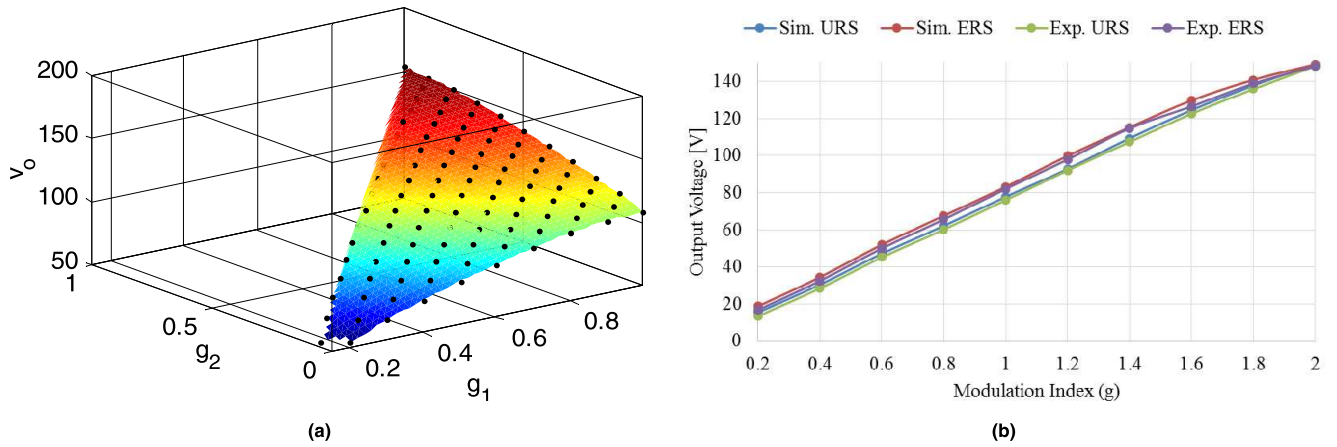
FIGURE 11. Dual matrix converter (a) Output voltage (V_0) calculated at different MI of MC1 and MC2 (b) Output voltage (V_0) transferred to the load.
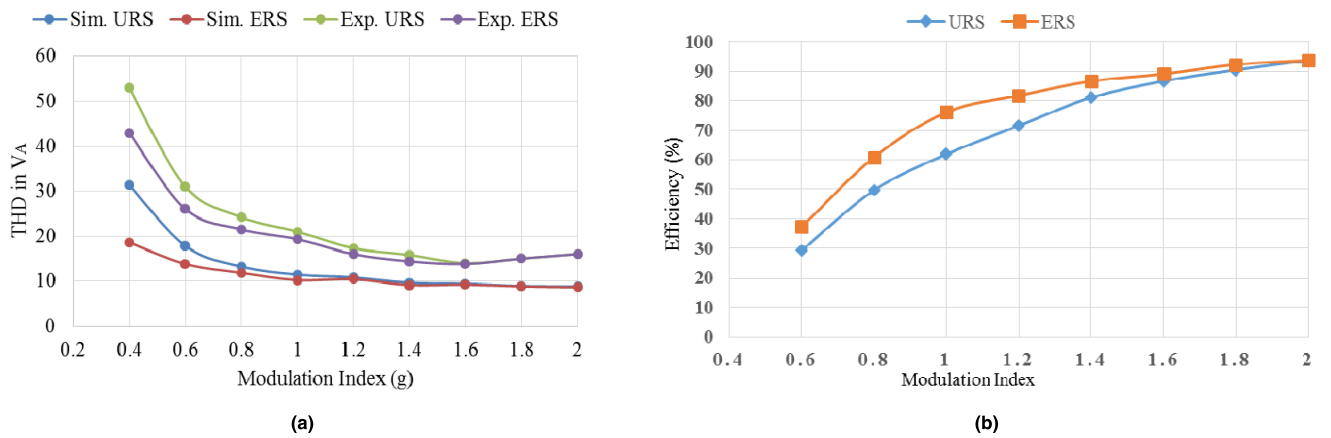

FIGURE 12. Dual matrix converter (a) THD in output voltage (b) Efficiency curve.

Subsequently going through the equations (29)-(32), the relationship between the output voltages with different modulation indices, can be given as:

$$v_o = 33.08 + 132.8g_1 + 94.06g_2 - 56.15g_1^2$$
$$- 26.23g_1g_2 - 22.48g_2^2 \qquad (33)$$

This equation represents the degree of accuracy, $R^2 = 0.9991$. Fig. 11(a) shows the output voltage as a function of modulation indices g_1, g_2 which is obtained within the defined limit (33). It is an indication of the voltage transfer for various combinations of g_1 and g_2. Fig. 11(b) represents the output voltage for DMC at different MI. The simulations and experiments produce practically the same values. It is observed from the Fig. 11(a) and 11(b) that the voltage transferred is higher in the case of ERS.

B. TOTAL HARMONIC DISTORTION IN OUTPUT VOLTAGE
The THD in the output voltage is mainly due to the switching frequency harmonics and its sidebands. Output voltage THD, for both ERS and URS scheme, is compared in Fig. 12(a). It is observed that ERS has significantly lower THD when compared to its counterpart. For example, at MI

of 1.2, ERS has 13.3% THD whereas URS has 16.2% THD. Note that the experimentally measured output voltage THD is slightly higher, which is a consequence of the dead-time and other non-idealities, which have not been considered in the simulation.

C. CONVERTER EFFICIENCY
For the efficiency calculation, the power at the three-phase input and at the five-phase output of the MC is calculated for the full MI range. The efficiency and the input and output powers are calculated as:

$$\eta_{conv} = \frac{P_{out}}{P_{in}}$$

$$P_{in} = \sum_{in=a,b,c}^{V_{in}I_{in}} \cos(\varphi_i)$$

$$P_{out} = \sum_{out=A...E}^{V_{out}I_{out}} \cos(\varphi_o) \qquad (34)$$

V_{in}, I_{in} and φ_i are input voltage, current and input power factor angle, respectively. The operation is maintained at

almost zero power factor angle. V_{out}, I_{out} and φ_o are output voltage across the open-end phase, current and output power factor angle, respectively. Fig. 12(b) shows the experimentally tested efficiency of the three-to-five phase DMC. It shows that ERS is more efficient as compared to the URS scheme. The reason behind this is the higher voltage transfer and lower harmonic losses in ERS.

VIII. CONCLUSION

In this paper, the output voltage of the DMC is controlled by two proposed SVPWM schemes. These two schemes are analyzed for a five-phase open-end load. A generalized equation for the DMC output voltage is derived in a linear range of MI. The performance of both the proposed schemes is compared with each other. Parameters considered for performance comparison are the THD in output voltage, voltage transferred from source to load and the efficiency of the MC. All these parameters were compared for a full linear range of MI. The result shows that THD in DMC controlled by ERS scheme is lower than URS scheme. In addition to this, higher voltages are transferred to the loads in the case of ERS. It is valid for a large range of MIs. The converter efficiency is slightly higher for ERS when compared to the URS scheme. Near to the maximum MI, both schemes are delivering the same voltage to the load that is nearly 150% of input phase voltage. Consequently, the ERS scheme is better than the URS scheme for open-end load system in full linear range of operation of DMC. The simulation and experimental results are in very close agreement.

ACKNOWLEDGMENT

REFERENCES

[1] M.-S. Kwak and S.-K. Sul, "Control of an open-winding machine in a grid-connected distributed generation system," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1259–1267, Apr./Aug. 2008.

[2] E. Levi, I. N. W. Satiawan, N. Bodo, and M. Jones, "A space-vector modulation scheme for multilevel open-end winding five-phase drives," *IEEE Trans. Energy Convers.*, vol. 27, no. 1, pp. 1–10, Mar. 2012.

[3] P. Srinivasan, B. L. Narasimharaju, and N. V. Srikanth, "Space-vector pulse width modulation scheme for open-end winding induction motor drive configuration," *IET Power Electron.*, vol. 8, no. 7, pp. 1083–1094, 2015.

[4] Q. T. An, M. H. Duan, L. Sun, and G. L. Wang, "SVPWM strategy of post-fault reconfigured dual inverter in open-end winding motor drive systems," *Electron. Lett.*, vol. 50, no. 17, pp. 1238–1240, Aug. 2014.

[5] A. Iqbal, K. Rahman, R. Al-Ammari, and H. Abu-Rub, "Post fault operation of a dual matrix converter fed open-end load," in *Proc. IEEE Int. Conf. Ind. Technol. (ICIT)*, Seville, Spain, Mar. 2015, pp. 1117–1122.

[6] Y. Wang, D. Panda, T. A. Lipo, and D. Pan, "Open-winding power conversion systems fed by half-controlled converters," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2427–2436, May 2013.

[7] A. Edpuganti and A. K. Rathore, "New optimal pulsewidth modulation for single DC-link dual-inverter fed open-end stator winding induction motor drive," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4386–4393, Aug. 2015.

[8] B. S. Umesh and K. Sivakumar, "Dual-inverter-fed pole-phase modulated nine-phase induction motor drive with improved performance," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5376–5383, Sep. 2016.

[9] K. K. Nallamekala and K. Sivakumar, "A fault-tolerant dual three-level inverter configuration for multipole induction motor drive with reduced torque ripple," *IEEE Trans. Ind. Electron.*, vol. 63, no. 3, pp. 1450–1457, Mar. 2016.

[10] Q. Jianglei, X. Lie, W. Lina, and H. Yannian, "Research on the modulation and control of multilevel matrix converter," in *J. Eng.*, vol. 2018, no. 13, pp. 614–621, 2018.

[11] M. Jones, I. N. W. Satiawan, N. Bodo, and E. Levi, "A dual five-phase space-vector modulation algorithm based on the decomposition method," *IEEE Trans. Ind. Appl.*, vol. 48, no. 6, pp. 2110–2120, Nov./Dec. 2012.

[12] S. Srinivas and V. T. Somasekhar, "Space-vector-based PWM switching strategies for a three-level dual-inverter-fed open-end winding induction motor drive and their comparative evaluation," *IET Electr. Power Appl.*, vol. 2, no. 1, pp. 19–31, 2008.

[13] A. D. Kiadehi, K. E. K. Drissi, and C. Pasquier, "Voltage THD reduction for dual-inverter fed open-end load with isolated DC sources," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2102–2111, Mar. 2017.

[14] R. K. Gupta, K. K. Mohapatra, A. Somani, and N. Mohan, "Direct-matrix-converter-based drive for a three-phase open-end-winding AC machine with advanced features," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4032–4042, Dec. 2010.

[15] J. Riedemann, J. C. Clare, P. W. Wheeler, R. Blasco-Gimenez, M. Rivera, and R. Peña, "Open-end winding induction machine fed by a dual-output indirect matrix converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4118–4128, Jul. 2016.

[16] S. M. Ahmed, H. Abu-Rub, Z. Salarti, M. Rivera, and O. Ellabban, "Generalized carrier based pulse width modulation technique for a three to n-phase dual matrix converter," in *Proc. 40th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Dallas, TX, USA, Oct./Nov. 2014, pp. 3298–3304.

[17] S. M. Ahmed, H. Abu-Rub, and Z. Salam, "Common-mode voltage elimination in a three-to-five-phase dual matrix converter feeding a five-phase open-end drive using space-vector modulation technique," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6051–6063, Oct. 2015.

[18] A. Somani, R. K. Gupta, K. K. Mohapatra, and N. Mohan, "On the causes of circulating currents in PWM drives with open-end winding AC machines," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3670–3678, Sep. 2013.

[19] A. Edpuganti and A. K. Rathore, "Optimal pulsewidth modulation for common-mode voltage elimination scheme of medium-voltage modular multilevel converter-fed open-end stator winding induction motor drives," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 848–856, Jan. 2017.

[20] N. Bodo, M. Jones, and E. Levi, "A space vector PWM with common-mode voltage elimination for open-end winding five-phase drives with a single DC supply," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2197–2207, May 2014.

[21] G. Mondal, K. Gopakumar, P. N. Tekwani, and E. Levi, "A reduced-switch-count five-level inverter with common-mode voltage elimination for an open-end winding induction motor drive," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2344–2351, Aug. 2007.

[22] Q.-H. Tran and H.-H. Lee, "A three-vector modulation strategy for indirect matrix converter fed open-end load to reduce common-mode voltage with improved output performance," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7904–7915, Oct. 2017.

[23] R. Baranwal, K. Basu, and N. Mohan, "Carrier-based implementation of SVPWM for dual two-level VSI and dual matrix converter with zero common-mode voltage," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1471–1487, Mar. 2015.

[24] A. Iqbal, S. K. Moin, and H. Abu-Rub, "Space vector PWM technique for a three-to-five-phase matrix converter," *IEEE Trans. Ind. Appl.*, vol. 48, no. 2, pp. 697–707, Mar./Apr. 2012.

[25] K. Rahman, A. Iqbal, N. Al-Emadi, and L. Ben-Brahim, "Common mode voltage reduction in a three-to-five phase matrix converter fed induction motor drive," *IET Power Electron.*, vol. 10, no. 7, pp. 817–825, Jun. 2017.

[26] D. Vincenti and H. Jin, "A three-phase regulated PWM rectifier with on-line feedforward input unbalance correction," *IEEE Trans. Ind. Electron.*, vol. 41, no. 5, pp. 526–532, Oct. 1994.

[27] A. Iqbal and S. Moinuddin, "Comprehensive relationship between carrier-based PWM and space vector PWM in a five-phase VSI," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2379–2390, Oct. 2009.

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