

## Development of High Power Amplifiers for Space and Ground-based Applications

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*Carlos Cilla*

# **Development of High Power Amplifiers for Space and Ground-based Applications**

PhD thesis, December 2012



PhD dissertation

# Development of High Power Amplifiers for Space and Ground-based Applications

by

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*Copenhagen, December 2012*

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# Abstract

The power amplifier used in the transmitter of a microwave system is a key issue, and it determines the system performance, cost, power consumption and reliability to a considerable extent. Traditionally, most of high power amplifiers used in military and commercial applications were tube-based amplifiers. They are efficient and provide very high power levels operating at low duty cycles. But they have a questionable long-term reliability, large footprints and they are not suitable for modern equipment with a decentralized transmitter, like a phase array system. Solid State Power Amplifier technology is the alternative to the tube-based amplifiers. Recently, there has been a renewed interest in this research field thanks, to a large extent, to the development of GaN semiconductor technology, that is already having an important impact on the wireless and radar market.

The scope of this PhD dissertation lies in the development of nonlinear design methodologies, manufacturing, and efficient testing of Solid State High Power Amplifier modules, with special focus on GaN state of the art technology. It is possible to identify two types of GaN Solid State High Power Amplifiers: the Hybrids and the Monolithic Microwave Integrated Circuits. The research work presented here focuses on practical realization and demonstration of these two types of amplifiers.

The design and experimental performance assessment of a 50 W Solid State C-band High Power Amplifier using European Monolithic Microwave Integrated Circuit GaN technology is discussed. The design will be used as a baseline for future developments of the next generation of the Sentinel satellite remote sensing radar T/R modules. The two-stage design features a  $6730 \times 3750 \mu\text{m}^2$  compact footprint. The overlapping between simulated intrinsic drain current and voltage waveforms is minimized, thus providing good power added efficiency. The design process encompasses a wide range of activities including technology assessment, small and large signal model validation using load pull measurements, nonlinear harmonic balance simulations, stability analysis, matching

network synthesis, evaluation of spreads and high power testing. The design has been fabricated at the United Monolithic Semiconductors foundry using their 0.25  $\mu\text{m}$  gate length GaN process, which currently is under final development.

Pulsed high power measurements provided excellent results. The maximum average power level measured under pulsed operation was 53 W at 4.74 GHz, and the maximum overall PAE measured was 55.8% at 4.9 GHz. The device presents a good bandwidth under large signal operation. At 1-2 dB compression point, in the frequency range from 4.85 GHz to 5.3 GHz, the output power is larger than 40 W (46.75 dBm  $\pm$  0.25 dB) with the gain ranging around 19 dB. This corresponds to a 0.5 dB bandwidth of 450MHz. PAE varies between 50%-54% along all this frequency range. These measurements present state of the art efficiency at C-band for these power levels achieved with a single chip. The results were in good agreement with the simulated values.

An efficient 100 W X-band hybrid high power amplifier using 0.25  $\mu\text{m}$  gate length GaN technology was successfully designed, assembled and tested. The goal of the project was to develop a high power amplifier for X-band frequencies with capabilities to replace the vacuum tubes used in the radar systems designed by Terma, the company co-funding the project. These radars are purely civilian systems used for applications like traffic surveillance within airports, coastal and air surveillance, environmental surveillance of sea surfaces and vessel traffic monitoring in harbors. The design process included technology evaluation, load pull and harmonic balance simulations, bondwire array and transition electromagnetic modelling, die attach, device fabrication and testing. Outstanding results were obtained for a single stage hybrid design using a power bar with 20 mm active area periphery. 94.5 W were measured under pulsed operation at 8.3 GHz and with a gain of around 7.6 dB. The maximum power added efficiency obtained was  $>60\%$ . This efficiency is higher than any other published for these power levels at X-band. Limited bandwidth was achieved. Along the 200 MHz band between 8.1 to 8.3 GHz, and at 1 dB compression point, the device was delivering power levels larger than 75 W, PAE  $>35\%$  and gain oscillating between 7.5  $\pm$  0.5 dB. Measurements were shifted down in frequency 1 GHz, but simulations predicted maximum power levels similar to the ones measured.

**Keywords:** Solid State High Power Amplifier, Gallium Nitrate Technology, Monolithic Microwave Integrated Circuit, Hybrid Integrated Circuit, Power Transistors, Nonlinear Microwave Design, Semiconductor Device Packaging, Wafer Bonding, Power Amplifier Testing, Transmitter, Ground-based Radar, Space-based Remote Sensing Systems.

# Resumé

I mikrobølgesystemers sendere er effektforstærkeren en nøglekomponent, som i vid udstrækning bestemmer systemets formåen, pris og effektforbrug. Traditionelt har mange effektforstærkere til militære og kommercielle anvendelser været baseret på elektronrør. De har høj virkningsgrad og kan levere meget høje effekter ved pulseret drift. Men deres forventede levetider er begrænsede, de fylder meget, og de er mindre velegnede til distribuerede anvendelser i moderne udstyr, f.eks. phase-array systemer. Halvleder effektforstærkerteknologi er her et alternativ til de elektronrørsbaserede effektforstærkere. Den seneste fornyede interesse i dette forskningsområde skyldes i høj grad udviklingen af GaN (gallium nitrid) halvleder teknologien, som allerede har gjort sig gældende på radio og radar markedet. Forskningsområdet for den foreliggende PhD afhandling er udvikling procedurer til design af ulineære halvleder effektforstærkere med tilhørende fremstillings- og afprøvningsmetoder, især med henblik på anvendelse af den nyeste "state of the art" teknologi. Det er her muligt at identificere to typer GaN effektforstærkere, den hybride og den monolitiske MMIC (Microwave Monolithic Integrated Circuit) forstærker. Der nærværende forskningsarbejde fokuserer på og demonstrerer praktisk opbygning af begge typer. Først diskuteres designet og den tilhørende eksperimentelle undersøgelse og vurdering af en 50 W halvleder C-bånds effektforstærker baseret på "European Monolithic Microwave Integrated Circuit" GaN teknologi. Dette design skal benyttes som en grundsten i den fremtidige udvikling af sender/modtager modulet til den næste generation af Sentinel satellit telemålings radarer. Det er et kompakt to trins design med et areal på kun  $6730 \times 3750 \mu\text{m}^2$ , som minimerer overlappningen mellem kurveformerne for de simulerede indre drain strømme og spændinger, hvorved der opnås en høj virkningsgrad. Designprocessen omfatter mange forskellige aktiviteter som valg af teknologi, verifikation af såvel småsignal som storsignal transistor modeller, herunder "load-pull" målinger, samt ulineær harmonisk balance simuleringer, stabilitets analyse, syntese af tilpasningskredsløb, analyser af parameterspredninger samt afprøvning under højeffekt betingelser. Forstærkeren blev

fremstillet hos United Monolithic Semiconductors, UMS, med deres 0,25  $\mu\text{m}$  gate GaN proces, der er i en afsluttende udviklingsfase. Målinger under pulserende drift viste meget fine resultater med en maksimal udgangseffekt på 53 W ved 4,74 GHz og en maksimal virkningsgrad på 55,8% (PAE, power added efficiency) ved 4,9 GHz. Forstærkeren havde en god storsignal båndbredde fra 4,85 GHz til 5,3 GHz med 1-2 dB kompression og en udgangseffekt over 40 W (46,75 dBm +/- 0,25 dB) med en forstærkning omkring 19 dB. Det svarer til en 0,5 dB båndbredde på 450 MHz. Virkningsgraden varierede fra 50% til 54% PAE og repræsenterer "state of the art" i C-bånd for en enkelt chip forstærker på dette effektniveau. Alle eksperimentelle data er i god overensstemmelse med tilsvarende simuleringer. Endvidere blev der konstrueret, opbygget og afprøvet en særdeles effektivt hybrid 100 W X-bånd effektforstærker, ligeledes baseret på 0,25  $\mu\text{m}$  gate GaN teknologi. Formålet med denne del af PhD arbejdet var udvikling af en X-bånd højeffektforstærker, med potentiale til at erstatte de elektronrørsforstærkere, der benyttes i radarsystemer fra Terma A/S, som medfinansierede projektet. Disse radarer er til rent civile anvendelse indenfor trafikovervågning i lufthavne, kystovervågning eller kontrol med skibstrafik i havne. Designprocessen omfattede her teknologivurdering, "load-pull" og harmonisk balance simuleringer, elektromagnetisk modellering af bondetrådsforbindelser, fastlodning af transistor chips samt design, montering og test af hybridkomponenter. Der blev opnået fremragende resultater for et enkelttrins hybrid forstærkerdesign med en "power-bar" chip på 20 mm periferi om det aktive areal. Bedste måling gav 94,5 W udgangseffekt under pulserende drift ved 8,3 GHz med en forstærkning på 7.6 dB og med en maksimal virkningsgrad  $> 60\%$  PAE. Dette resultat er bedre end andre publicerede X-bånds virkningsgrader ved tilsvarende effektniveauer. Forstærkerens båndbredde var begrænset til 200 MHz. Mellem 8,1 og 8,3 GHz var minimum udgangseffekten ved 1 dB kompression højere end 75 W, virkningsgraden over 35% PAE med forstærkningsvariationer +/- 0,5 dB omkring 7,5 dB. De opnåede effektniveauer svarede til de simulerede forventninger, men med en forskydning i frekvens til 1 GHz under de simulerede resultater.

# Preface

This thesis is submitted as a part of the requirements to achieve the Ph.D. degree at DTU Electrical Engineering, Technical University of Denmark. The PhD contract started in May 2009 and ended in August 2012. Between June 2010 and June 2011 I was at the European Space Research and Technology Centre (ESTEC) that is part of The European Space Agency (ESA). The work presented here has been financially supported by Terma A/S, The Technical University of Denmark and The European Space Agency. Initially Professor Viktor Krozer was the main PhD advisor until he left The Technical University of Denmark at the end of 2009. Professor Jens Vidkjær took then the role of main supervisor until the completion of the thesis.



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First of all, I would like to show my gratitude to my advisor Jens Vidkjær for sharing his knowledge with me, for his time to listen to all my progresses, and for giving me the freedom and responsibility to manage the project by myself. The experience has made me grow both as an engineer and as a person and I am convinced it will be a key asset to face future career challenges. Furthermore I convey my sincere thanks to Terma A/S for co-funding the project. I would also like to express my appreciation to my first advisor Viktor Krozer that unfortunately had to leave DTU right after starting my PhD. I would like to thank him for setting up the funding for the project and for all the work we shared during the years before I started the PhD. I also extend my sincere gratitude to Nicolas Le Gallou for giving me the opportunity to design a GaN MMIC HPA and for the fruitful technical discussions we had during my stay at ESA.

Moreover I highly appreciate the assistance of the technical staff that helped me with components fabrication during all this time: Bo Brændstrup from the electrical workshop at DTU Space, Martin Nielsen, Frank Persson and Jan Mortensen from the mechanical workshop at DTU Elektro, Jesper Hanberg from the Danish National Clean Room Danchip and Jos Castelein from the ESA Payload Division Laboratory.

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Carlos Cilla  
Copenhagen, December 2012.



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# List of Publications

The papers that I have written during the PhD time frame are listed below. Furthermore, two journal publications, based on the work presented in this dissertation, are under preparation.

- **40 W C-band GaN MMIC High Power Amplifier for Next Generation of Sentinel Satellites**, C.Cilla, N.Le Gallou, A.Chowdhary and J.Castelein, 6<sup>th</sup> Space Agency MOD Round Table Workshop on Wide Bandgap Semiconductors and Components, ESA 2012. (Appendix E p.130)
- **Bondwire Array Modeling for the Design of Hybrid High Power Amplifiers above C-band**, C.Cilla, S.Jonasson, J.Hanberg, Asia Pacific Microwave Conference 2012. (Appendix E p.137)
- **POLARIS: ESA's Airborne Ice Sounding Radar Front-End Design, Performance Assessment and First Results**, C. Cilla, V.Krozer, J.Vidkjær and J.Dall, International Microwave Symposium 2009. (Appendix E p.140)
- **High Power High Efficiency Amplifiers for P-Band in LDMOS, GaAs and GaN Technology**, V.Krozer, J.Vidkjær, D.Hadziabdic, C.Cilla Hernandez, N. Le Galou, European Space Agency Workshop on Advanced RF Sensors and Remote Sensing Instruments,ESA 2009. (Appendix E p.144)



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# Development of High Power Amplifiers for Space and Ground-based Applications

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# Chapter 1

## Introduction

### 1.1 Background and Motivation of the Research Topic

One of the key elements in an RF system is the high power amplifier (HPA). The interest in this technology has been renewed due to the fast development of the wireless market in the 90s and the steady but continuous progress of radar applications. Advanced radar systems have received considerable attention due to the increased demand in remote sensing and imaging applications both for terrestrial and space systems. Other application fields where high power amplifiers are used include military communications, electronic warfare systems, jammers, surveillance and reconnaissance systems, satellite communications, medical imaging, telecom basestations, broadcast infrastructure, Cable TV and green energy solutions. The power amplifier has a large impact in the system performance, cost, power consumption and reliability.

In the past, most of the high power amplifiers used in military and commercial applications were tube-based amplifiers, such as grid controlled tubes, magnetrons, klystrons, travelling-wave tubes and crossed field amplifiers. Solid State Power Amplifier (SSPA) technology is the alternative. If we compare the tubes versus solid state technology, the tubes are more efficient and they provide higher peak power levels operating at low duty cycles. On the other hand, the lower peak power levels of solid state amplifiers can be compensated through a modular approach and operating the devices with larger duty cycles or even at CW. Furthermore their power levels are continuously increasing as the new material technology matures. The efficiency of SSPAs is nowadays approaching the ones achieved by the tubes at frequencies under C-band. The tubes have larger mass and footprints that increase the size of the transmitters. Furthermore, higher operating voltage levels are required for the operation of tubes. Solid state technology is more reliable, presenting lower failure rates than the tubes. The solid state power amplifiers based on mature and well established semiconductor technologies are in general cheaper, but the tubes also have very competitive prices. Furthermore, the tubes are suitable for RF systems with a central transmitter, while solid state technology is suitable for

both systems with a central transmitter and also for modern phase array systems with a decentralized transmitter. SSPAs also present better linearity properties than the tubes.

This comparison concludes that even though the tubes are well established, SSPAs are a serious candidate to replace the tube-based amplifiers in the medium-term. Actually, nowadays, the use of SSPAs has already surpassed the use of amplifier tubes in applications using frequencies up to 4 GHz, and this tendency is expected to continue at higher frequencies in the upcoming years.

Solid State Power amplifiers have received much attention in the last years due to the fast development of Gallium Nitride (GaN) HEMT (Heterojunction Electron Mobility Transistor) technology. This material presents very interesting intrinsic properties for high power amplifier design. Power densities ten times larger than the ones achieved using Gallium Arsenide (GaAs) material have been demonstrated. This implies that a single GaN transistor can generate the same power level as many GaAs transistors placed in parallel. GaN technology has proven to be useful for the design of SSPAs, Low Noise Amplifiers and Switches, reducing the system size and enhancing transmission rates and target detection. In the medium-term it will also contribute to reduce system costs. The technology is on its way to the maturity and several designs have already been demonstrated in the literature. Reliability studies of GaN devices have been performed to achieve a fast commercialization process.

The development of SSPAs is a multi-faceted activity including linear and nonlinear device modelling, linear and nonlinear circuit design, device fabrication, technology development, packaging, measurement and testing. This PhD dissertation focuses on a subset of these research topics, with special focus on GaN state of the art technology. Research with immediate practical applications has always been pursued.

Two different design projects were successfully completed during this research project. The first one consisted of designing a single chip 50 W C-band GaN MMIC (Monolithic Microwave Integrated Circuit) to increase the transmitted power of the next generation of ESA Sentinel satellites. This solution is a good alternative to a larger design using four 11W GaAs transistors in parallel. The goal of the second project was to develop a 100W Hybrid amplifier for X-band frequencies with capabilities to replace the currently employed vacuum tubes at the Danish company Terma. During both projects, focus was placed on power amplifier design methodologies, manufacturing and efficient testing.

## 1.2 Thesis Overview

Chapter 1 gives an overview of the research topic and the goals targeted during the project.

Chapter 2 presents a brief overview of present and emerging HPA technologies for pulsed applications and accompanying modelling and design methodologies. The study

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overview will provide inputs to the design and implementation of solid state high power amplifiers.

Chapter 3 describes the design and experimental performance assessment of a 50 W C-band MMIC High Power Amplifier using 0.25  $\mu\text{m}$  gate length GaN technology.

Chapter 4 presents the design, assembly process and measurement campaign of 100W X-band hybrid high power amplifiers using 0.25  $\mu\text{m}$  discrete GaN power bars.

Chapter 5 provides the conclusions for this PhD dissertation.



# Chapter 2

## Study of Solid State High Power Amplifier Technologies

This chapter focuses on present and emerging Solid State High Power Amplifier technologies both at transistor level and circuit level. First, different semiconductor materials will be presented and compared, including state of the art GaN. Afterwards, the figures of merit for HPA design will be identified. A discussion on electro-thermal modelling of transistors will follow. Subsequently, circuit level technologies and design methodologies for HPA will briefly be presented. Finally, a comparison between power amplifier Monolithic Microwave Integrated Circuits and Hybrid solutions will be provided.

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### 2.1 HPA Technologies for Pulsed Applications at Transistor Level

The most well known semiconductor materials for SSPAs include: Silicon (Si), Silicon Germanium (SiGe), Gallium Arsenide (GaAs), Indium Phosphide (InP), Silicon Carbide (SiC) and Gallium Nitride (GaN). The material technology defines the limits of operation of the transistor. Several Figures of Merit (FOM) can be used to asses

the performance of RF semiconductor technologies. The Johnson FOM is the most common of them, and it provides the power-frequency limit for a given material. It can be written as follows:

$$JFOM = \frac{E_{cr} * V_{sat}}{2 * \pi} \quad (2.1)$$

Where  $E_{cr}$  is the material breakdown electric field and  $V_{sat}$  is the saturated electron velocity. Materials with higher JFOM are able to operate at higher frequencies and generate higher power levels. This is the case of the wide bandgap materials, like SiC and GaN, as it is shown in the table in Figure 2.1.

	Si	GaAs	4H-SiC	GaN	Diamond
$E_g$ (eV)	1.1	1.42	3.26	3.39	5.45
$n_i$ (cm <sup>-3</sup> )	1.5×10 <sup>10</sup>	1.5×10 <sup>6</sup>	8.2×10 <sup>-9</sup>	1.9×10 <sup>-10</sup>	1.6×10 <sup>-27</sup>
$\epsilon_r$	11.8	13.1	10	9.0	5.5
$\mu_n$ (cm <sup>2</sup> /Vs)	1350	8500	700	1200(Bulk) 2000(2DEG)	1900
$v_{sat}$ (10 <sup>7</sup> cm/s)	1.0	1.0	2.0	2.5	2.7
$E_{br}$ (MV/cm)	0.3	0.4	3.0	3.3	5.6
$\Theta$ (W/cm K)	1.5	0.43	3.3-4.5	1.3	20
$JM = \frac{E_{br}v_{sat}}{2\pi}$	1	2.7	20	27.5	50

Figure 2.1 – Table comparing different material properties from [1]

A brief discussion on the most important semiconductor materials is provided here.

### 1 Silicon (Si BJT, Si LDMOS, Si CMOS)

Silicon is very cheap, but by itself doesn't make very good high power amplifiers. Silicon BJTs (Bipolar Junction Transistors) and CMOS (Complementary Metal-Oxide-Semiconductor) transistors appeared in the 1950s and 1960s respectively, but they are not taken into consideration for power amplifier designs anymore because they cannot deliver high power or operate at high frequencies. Silicon LDMOS (Laterally double diffused Metal Oxide Semiconductor) is a technology that has been improved during the last years, and it is successfully used to generate high power levels at frequencies up to 4 GHz. The new generation of LDMOS devices can be operated at 50 V, achieving higher output power and using lower current levels.

### 2 Gallium Arsenide ( GaAs pHEMT, mHEMT, HBT, MESFET)

GaAs is a mature technology that was developed in the 1970s, and it has experienced an incredible growth in the last 15 years due to the wireless market. This technology will never be cheaper than silicon, due to initial material costs. The parts are more fragile than silicon, and the thermal dissipation is not optimal. Furthermore, this technology is limited in RF power due to the low drain



bias breakdown voltage. GaAs can not provide the power, linearity and efficiency required for the next generation of HPAs.

GaAs HBTs (Heterojunction Bipolar Transistor) operate vertically, in contrast to the horizontal operation of Field Effect Transistors (FETs). The fabrication process is cheaper than other GaAs processes, but it presents thermal problems, amongst others.

GaAs pHEMT (Pseudomorphic High Electron Mobility Transistor) was developed in the 1990s and it is used at up to 50 GHz. "Pseudomorphic" implies that the semiconductor is not just GaAs, but it also contains Aluminium or Indium (AlGaAs or InGaAs).

GaAs mHEMT (Metamorphic High Electron Mobility Transistor) performs at more than 100 GHz. "Metamorphic" implies that the lattice structure of GaAs is buffered using epitaxial layers to gradually transform the lattice constant so it matches with the one for InGaAs. InGaAs is normally grown on InP, which is expensive and fragile compared to GaAs.

GaAs MESFET (Metal Semiconductor Field Effect Transistor) technology is limited to Ku-band or lower frequencies and it may be abandoned soon, because it doesn't cost much more to fabricate pHEMT or mHEMT on GaAs, and these technologies offer higher performance.

### **3 Indium Phosphide (InP HEMT, HBT)**

Indium phosphide HEMT technology has the upper frequency record, being used to design Terahertz devices. Regarding the disadvantages, it is extremely fragile and expensive. Indium phosphide (InP) HBT has superior low voltage performance compared to GaAs HBT.

### **4 Silicon Germanium (SiGe HBT)**

SiGe HBT has been developed in the recent years, and it was originally predicted to beat GaAs. But this did not happen, since the technology performance in terms of noise figure and power is not as high as for GaAs. Designs up to 70GHz have been reported. If the upper frequency of SiGe is extended, the breakdown voltage is reduced to levels as low as 1 V. This means that the amplifiers are not really able to provide high power levels.

### **5 Silicon Carbide (SiC LDMOS, MESFET)**

SiC suffers from poor electron transport properties, which hinders its use in very high frequency amplifiers. It has also been limited by expensive substrate wafers, and it performs worse than GaN.

## 6 Gallium Nitride (GaN HEMT, HFET)

GaN development started in the late 1990s, and devices were first released into the market around 2005. The technology has progressed extraordinarily fast thanks to the upsurge of the wireless base station market. GaN material presents very interesting intrinsic properties for high power amplifier design, such as withstanding high voltage levels, wide bandgap, high power densities, high breakdown voltage and high current handling [1]. Substrates for GaN are either Silicon Carbide, Sapphire, or Silicon. SiC is an excellent heat-sink, having much higher thermal conductivity (400W/mK) than Silicon (140W/mK). If the GaN transistor is epitaxially grown on semi-insulating SiC substrates, the heat dissipation is notably improved which means lower temperature rise due to self-heating. But GaN on-silicon is cheaper than GaN on-silicon-carbide. When comparing GaN with other technologies it is important to highlight that:

- The JFOM is 15 times larger for GaN than GaAs.
- GaAs mobility of the carriers is much better, but the high electron saturation velocity of GaN HEMTs compensates for the relatively lower mobility.
- The breakdown voltage is around ten times larger than that of Si and GaAs.
- GaN has a record in power density, and devices with power density ten times larger than of GaAs have been demonstrated. The other technologies require larger area devices and larger currents to generate higher power levels. This implies higher parasitic capacitances and lower impedance levels, complicating the matching network designs and limiting the operating frequency and the bandwidth. The higher power densities up to 20 W/mm reported for GaN yields to a smaller die size and in principle more easily realized input and output matches. Normal power densities for reliable devices are around 5-7 W/mm.
- GaN can operate at higher channel temperature than GaAs, Si or SiGe.
- In contrast to SiC, GaN can form heterojunctions. This implies that GaN can be used to fabricate HEMTs, while SiC can only be used to fabricate MESFETs, which present worse performance.

GaN is becoming a well established semiconductor material that can be used in a broad range of circuits including power amplifiers, low noise amplifiers, switches and others. It contributes reducing the system size and enhancing transmission rates and radar target detection. Furthermore, the robustness of this technology has allowed to remove traditional components with device protection functions such as ferrite isolators or limiters.

Up to C-band, the competitors of GaN are mainly SiC and Si LDMOS. They have very competitive prices. At higher frequencies, SiC and Si LDMOS cannot be used, while GaAs can be used but with much lower power densities than GaN.

A lot of research has been conducted in the last years to reduce surface trapping effects through process improvements [2–6], and to improve the long-term reliability of the devices [7–11]. In spite of this rapid progress, much work still remains to be done for GaN devices. Among the research topics that have to be addressed we can highlight three:

- Research on thermal management and new packages. Thermal management of the devices has already been improved through wafer thinning [12–17]. Thinning the substrate effectively reduces the thermal resistance of the device and the via-hole inductance. Further improvements are required, and new carrier materials like Aluminum Diamond should be investigated.
- Push GaN higher in frequency. Results have already been published with GaN up to 500 GHz. One of the key issues towards achieving higher frequency with GaN is how to thinner the gate during fabrication. New E-beam fabrication techniques are being investigated.
- Research on efficiency enhancement at higher frequencies.

## 2.2 Identification of Figures-of-Merit for HPA Design

The most important parameters for the design of an HPA are described here:

- Bandwidth.
- Group delay.
- Gain. It can be traded for bandwidth.
- Saturated power and output peak pulsed power. It depends on the device periphery size. In mature technologies, the output power decreases following  $1/f^2$ .
- Maximum frequency of operation. It is determined by the material and the physical size of the transistor. In a FET transistor, the gate length determines the maximum possible frequency of operation, since the gate length is directly related to the channel length.
- Power Added Efficiency: This is the key in order to reduce size, weight and cost, and increase reliability through lower power dissipation. Efficiency can be traded for output power.
- Linearity. This is very important for applications using digital modulations like basestations, but it is not so critical in radar applications. Linearity can be traded for efficiency.
- Maximum current and voltage levels to operate within the Safe operating area (SOA).

## 2.3 Electro-Thermal Modelling of Transistors

Transistor non linear modeling has been addressed for many years, but the accuracy of the models has always been questionable. Therefore many people used to design power amplifiers based on experimental work. Nowadays, the transistor models are much more trustworthy, and there is an increasing tendency to use models as a valuable tool for designing power amplifiers. This allows a reduction in the number of trials needed to have a successful design. For a detailed discussion on this topic refer to [18] and [19]. It is possible to identify two kinds of models:

1. Physical models. These models are based on non linear partial differential equations and quantum-mechanics equations implemented in a simulator using finite-difference or finite-element methods. The main disadvantage of the method is that these equations have a huge computational cost, and the accuracy can be compromised depending on the numerical techniques used. This modeling technique is not useful for circuit design, but it is very practical during the transistor design stage.
2. Measurement-Based Equivalent Circuit Models in which the DC I-V and S-parameter measurements are used to build a network of equivalent circuit components. This is typically used for small-signal models. Large signal model can also be obtained using components that are dependent on the large-signal voltages. Mathematical function fitting techniques can be used after extracting the network model to obtain an equation model without physical meaning or to build a table-based model.

It is important to include memory effects in the models. They can be created by the transistor in itself or by the external circuitry. Two different types can be distinguished:

- Short-Term memory effects that have characteristic times close to the frequency of operation. They can be amongst others due to the charge stored in the transistor or the associated reactances. It is possible to perform measurements to include these effects in the model.
- Long-Term memory effects take place in a timescale much longer than the period of the RF signal. The sources of these effects inside the transistor are thermal gradients and charge trapping. The thermal effects consist of variations in the channel temperature due to previously amplified signals. Charge trapping effects occur due to imperfections in the semiconductor layers. GaAs and GaN FET transistors are affected by this problem.

There are several transistor parameters that vary with the temperature such as the threshold voltage, pinch-off, breakdown voltages and the mobility and saturation velocity of the charge carriers in the channel. It is difficult to guarantee isothermal

conditions in pulsed applications. Therefore, it is very important to generate coupled electro-thermal models by using parameters obtained from pulsed measurements at different base-plate temperatures.

## 2.4 Circuit Level Technologies and Design Methodologies for Efficient HPAs

Power amplifiers can be classified into two big groups:

- Amplifiers classified depending on the conduction angle determined by the DC bias point. They include class A, AB, B and C [20].
- Switching mode power amplifiers, including, among others, class E, D, F and inverse class F.

In HPA design the power efficiency is a key issue, since it relieves thermal dissipation problems, increases the reliability and reduces memory effects. In space applications, it is one of the most important parameters, since the available power from the satellite panels is limited. The efficiency is largely circuit-controlled, but it also depends on some device features.

Many HPAs for radar applications use class C operation. This gives a good efficiency for a single transistor stage, but normally, class-C has such a low gain that the efficiency advantage is lost when using additional stages.

Switching amplifiers are focused on improvement of power added efficiency by using two concepts:

- Avoiding the overlapping in time of voltage and current waveforms at the drain intrinsic reference plane.
- Controlling the harmonic loading conditions to increase the swing of the fundamental tone at the output. The control of the harmonics is implemented with parallel or series tuning.

Switching mode amplifiers have received much attention in the last years, especially since the introduction of GaN HEMTs. Class E ideal circuit model consists of an ideal switch, a parallel capacitor, a simple resonant circuit and a load [21–24]. The theoretical efficiency is 100%, because simultaneous high voltage and current are avoided across the transistor. In practice, the PAE is limited due to parasitic capacitances, resistances and package inductances. At lower frequencies, around 400 MHz, very high efficiencies exceeding 80% have been achieved [23], but, as the frequency is increased, the efficiency is reduced drastically, especially if high power is required. Class F or inverse Class F HPAs can generate greater power than class E. They use deep class AB biasing. The ideal class F HPA operates with square-wave drain voltage and half-sine shape current. In this way, DC-power is not dissipated in the circuit, since either current or voltage

is zero at any instant. The theoretical efficiency is 100%, and high efficiencies reaching 85% PAE at 2 GHz have been reported in [25]. The inverse class F amplifier has square-wave current and half-sinusoidal voltage outputs. Theoretically, it should present the same performance than the class F. In practice, the efficiency of the class F and inverse class F amplifiers is limited by the transistor drain to source capacitance, the losses in the channel due to the on-state resistance, the knee voltage and the losses in matching networks. GaN is a good candidate to be used in this type of amplifiers, since a high frequency of operation with respect to the fundamental is required in order to generate the higher order harmonics needed to shape the drain waveforms. For processes with lower  $f_t$  such as LDMOS, it is more difficult to shape the waveforms.

Series tuning is the preferred option for high efficiency amplifiers when there are very low impedance levels involved [21]. This means that the current entering the transistor is kept sinusoidal. This is in contrast to the classical class A, AB, B and C RF-power amplifier concepts, where parallel tuning forces sinusoidal voltages.

Other popular efficiency enhancement techniques that require more cumbersome hardware set ups include Doherty PAs, Push-pull HPAs and dynamic power supply approaches like envelop tracking [26–30].

- Doherty amplifiers allow increasing the efficiency while operating in back-off, but with a limited bandwidth [31–37]. The Doherty methods are often complex to be implemented, and in practice they seldom reach a total PAE above 50%.
- Push-pull PAs use two equal devices driven by out of phase signals. The technique improves the efficiency and the linearity, but the main disadvantage is the difficulty to fabricate balun transformers at high frequencies, used to combine both devices. At low frequencies impressive push-pull results have been demonstrated. A L-band GaN HEMT PA delivering 500 W pulsed power with 49% PAE is presented in [38]. A comparison between push-pull and Doherty amplifier performance can be found in [39].
- Envelop tracking technique consists of sampling the input power to dynamically adjust the drain or gate bias towards efficiency improvement. This technique is also known as drain modulation.

## 2.5 MMIC vs. Hybrid Power Amplifier Technology

It is possible to classify the Solid State High Power Amplifiers into Hybrids and MMICs. On the one hand, a Hybrid consist of a discrete semiconductor power bar, prematched structures like MOS capacitors, and external matching, combining and biasing networks built using another substrate material. Ceramic based substrates are suitable for high power applications. Often, the substrate used has a very high dielectric constant to allow miniaturization of the networks. Furthermore, the external substrates are usually much cheaper than the semiconductor material. Both the transistor dies and

the dielectric material pieces are mounted inside a package, and interconnected using bondwire arrays. On the other hand, an MMIC integrates the GaN transistor dies, the matching, combining and bias networks in the same piece of semiconductor material.

At frequencies below 6 GHz, it is typical to find Hybrid packaged transistor power bars. At frequencies above 6 GHz, MMIC solutions dominate the market, and it is challenging to find Hybrid solutions, since the package and bondwire parasitics become increasingly important at sizes comparable to the operating wavelength. But Hybrid solutions above C-band have two main advantages that make them worth further investigation: the reduction in semiconductor area needed, therefore drastically reducing the final cost, and the possibility of implementing the external matching and biasing networks on very low loss substrates, thus improving output power and efficiency capabilities. Alumina substrate has e.g. 10 times lower loss tangent at 10 GHz than SiC semiconductor, which is the most commonly used substrate for GaN transistors

The main advantage of the Hybrids is their price, since the amount of semiconductor required is much smaller than for the MMICs. This especially applies for technologies that are in their first commercialization stages like is the case of GaN. One of the main disadvantages of the Hybrids is the presence of bondwire transitions between substrate and power bar. They have to be carefully modeled and simulated with EM software. Furthermore, the bondwires introduce additional losses, couplings and larger module-to-module differences. As a consequence, the spreads in the response of the Hybrids are typically larger than for the MMICs. Hybrids have in general only one stage. Therefore, lower gains than the MMICs are achieved, and big external drivers are required. Multi-stage Hybrid amplifiers would require a more complex mechanical assembly process and a very careful design and modeling of the interstage matching network and the bondwire transitions. Furthermore, in a two stage design, the driver/booster ratio can be controlled to achieve higher overall efficiencies and larger bandwidths. The bandwidth is affected by the driver/booster ratio since the impedance transformation needed in the interstage matching network does influence the bandwidth [40]. This is the reason why MMICs are usually more broadband than the Hybrids.

The MMIC achieves a much more compact solution and they use the active area more efficiently, usually achieving larger power densities. But the Hybrids are usually achieving larger peak power levels.

In both MMIC and Hybrid solutions, via hole technology and backprocessing to thinner the wafer produces higher performance, since it improves the heat dissipation. Microstrip over coplanar technology is also preferred [41].

Along the next chapters, the design process of a 50 W C-band MMIC and a 100 W X-band Hybrid will be covered in detail. The designs presented here are of special interest because it is difficult to find publications in literature about MMICs at frequencies under C-band and Hybrids at X-band.





# Chapter 3

## C-band GaN MMIC High Power Amplifier for Next Generation of Radar Remote Sensing Satellites

This chapter describes the design and experimental performance assessment of a Solid State C-band High Power Amplifier using MMIC GaN technology from United Monolithic Semiconductors (UMS). The design will be used as a baseline for future developments of the next generation of T/R modules used in European Remote Sensing satellite radars. The two stages MMIC HPA feature a 6730 X 3750  $\mu\text{m}^2$  compact footprint. The driver stage comprises two 16X100  $\mu\text{m}$  cells, and the output stage four 16X150  $\mu\text{m}$  cells in parallel. The transistors use Vdd=30 V and low quiescent current biasing conditions. The overlapping between simulated drain current and voltage waveforms is minimized, thus providing good power added efficiency.

Pulsed high power measurements provided good results. The maximum average power level measured under pulsed operation was 47.26 dBm (53.16 W, Gain=15.9 dB) at a frequency of 4.74 GHz. Similar values were obtained between 4.6 and 5.1 GHz. The maximum overall PAE measured using calibrated current sensors was 55.8% at 4.9 GHz (Pout=47.19 dBm and Gain=17.51 dB). These maximum power levels and PAEs were measured when the device was working at compression points between 2.5 and 3 dB. These results are in good agreement with the simulated values.

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## 3.1 Motivation

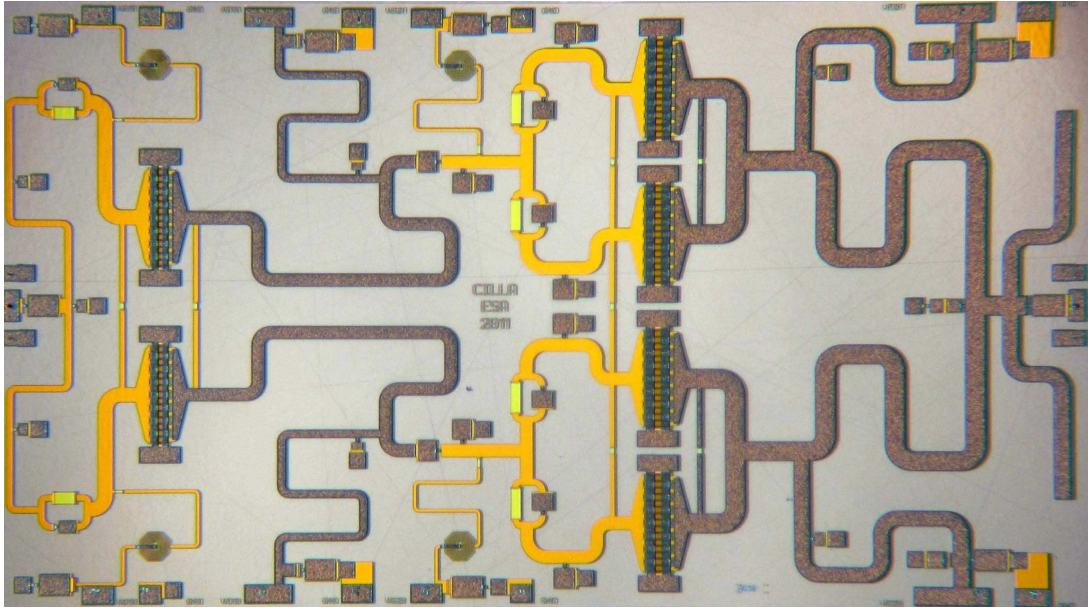
The current Sentinel satellite T/R module configuration consists of two  $5610 \times 4510 \mu\text{m}^2$  paralleled 11 W GaAs MMICs with PAE=36.9%. This power level is close to the technological limit of GaAs for a single chip. ESA plans to implement a new calibration mode for a next generation of Sentinel that requires reducing 10% of the receiving window, therefore degrading the SNR. In order to maintain the resolution, one option is to increase the transmitted power to 40 W. Two solutions are foreseen: the first one consists on parallel four 11 W GaAs transistors. But the losses in the combining structure (0.4 - 0.6 dB) would reduce the overall PAE to 31% while delivering 38 W. There would also be an increased risk of malfunction due to imbalances between the parallel stages and increased spreads created by the bondwire arrays and transitions. The second solution is to use the benefits of GaN technology to design a more compact and efficient 40 W MMIC using a single chip as it will be described within this chapter.

The C-band MMIC presented in this work has been fabricated at the UMS foundry using an early revision (iteration 1) of their process GH25. It uses  $0.25 \mu\text{m}$  gate length and is intended for MMIC design up to 20 GHz. A practical realization of the MMIC is shown in Figure 3.1.

## 3.2 State of the Art at C-band

It is difficult to find MMIC designs at C-band, and the most part of the designs reported at this frequency band are hybrid based.

The benefits of MMIC technology over hybrid for space applications are well known: a very compact footprint and increased reliability. In GaAs technology, the best MMIC reported is the one used in the current Sentinel satellite providing 11 W with PAE=36.9%.



**Figure 3.1** – Fabricated C-band MMIC HPA ( $6730 \times 3750 \mu\text{m}^2$ )

Hybrid GaAs designs have been reported delivering power levels between 20-27 W with PAEs around 60-70% as shown in [42] and [43].

Looking at GaN technology, a 70 W High Power Amplifier with  $\text{PAE} = 50\%$  has just been reported by TNO in [44]. The design uses an output stage periphery of 16 mm in contrast to the 9.6 mm used for the design presented here. Comparing both designs, the design from TNO holds the record in output peak power level, but it uses less efficiently the active area. Furthermore, a 20W pulsed power amplifier with 40% PAE at 5.75 GHz has been published in [45]. It is also possible to find commercial broadband MMICs with output power levels between 25-35W and PAEs around 30% [46] [47].

The most part of the published work is hybrid-based with outstanding power levels, combining typically two or four GaN power dies in parallel and achieving pulsed power levels ranging between 100-343 W and PAEs from 31% to 57% [48–53].

The work presented here represents, to the best of my knowledge, the highest two-stage efficiency (55.8%) ever reported on a single chip MMIC design at C-band for power levels above 50 W.

### 3.3 MMIC Design Process

In this section, the design procedure of an MMIC is described. Table 3.1 shows the specifications required for the High Power Amplifier. The specifications require central frequency of operation at 5.4 GHz, total output power  $>40$  W,  $\text{PAE} > 45\%$  and 150 degrees maximum junction temperature when using a baseplate temperature of 80 degrees.

f(GHz)	5.404
Bandwidth(MHz)	400
Pout(W)	>40
Gain(dB)	>20
PAE(%)	>45%
Flatness over BW(dB)	0.1
Input RL(dB)	>14
Backside Temperature (°C)	80
Vds(V)	30
Max. junction $T^a$	150

**Table 3.1** – HPA Specifications

The most important requirement in this case is the overall Power Added Efficiency, since the device is designed to operate in space, where the DC supply provided by the solar panels is limited, and any saving in this respect is always welcome. Furthermore, the junction temperature depends a lot on the efficiency, and this issue becomes critical, since the heat has to be dissipated only by conduction in the space environment. The frequency of operation is just at the border between the recommended applications for hybrid technologies using transistors with  $0.5 \mu\text{m}$  gate length and the MMIC process using  $0.25 \mu\text{m}$  gate length. Designing in the lower frequency range of the MMIC process implies the need of a relatively large MMIC area and also the need of lumped components with values close to the maximum ones available for this process. Since the project shared wafer run with another design, the MMIC size was constrained by the foundry to a maximum of  $6730 \times 3750 \mu\text{m}$ . The 0.1 dB 400 MHz bandwidth (7.5%) is a very challenging requirement. At the current stage of maturity of the technology process it is not worth to target this accuracy in the flatness. This is because the design kit libraries are still under development and the nonlinear models used for the design were not obtained from measurements using the same transistor version than the one that is used for the fabrication.

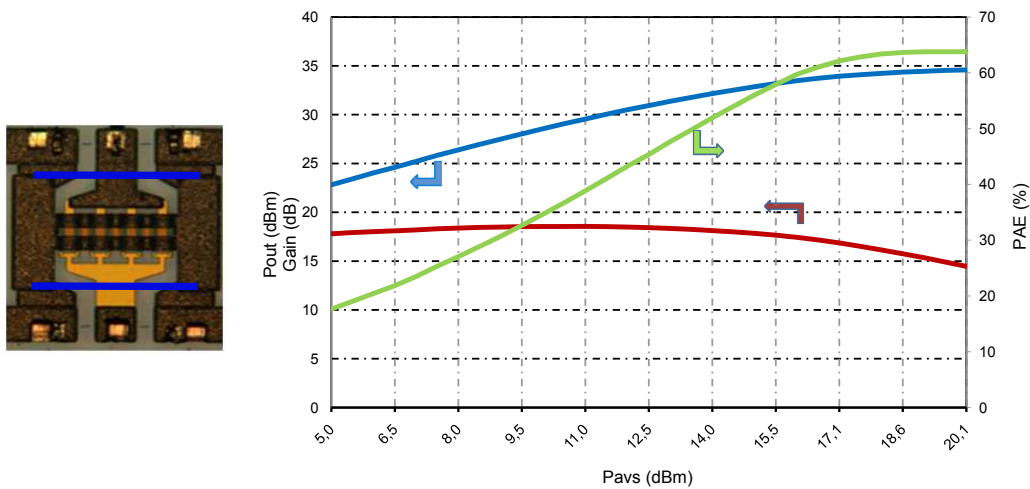
Once the specifications are clear, the design approach that is followed comprises:

- Technology feasibility assessment
- Small and large signal transistor model validation using load pull measurements
- Selection of the MMIC topology (number of stages, cell sizes)
- Selection of biasing point and operation principle
- Design using the validated nonlinear model in a harmonic balance simulator
- Stability analysis
- Matching network synthesis

- Passive components 3D EM simulation and spreads evaluation.

### 3.3.1 Technology Feasibility Assessment

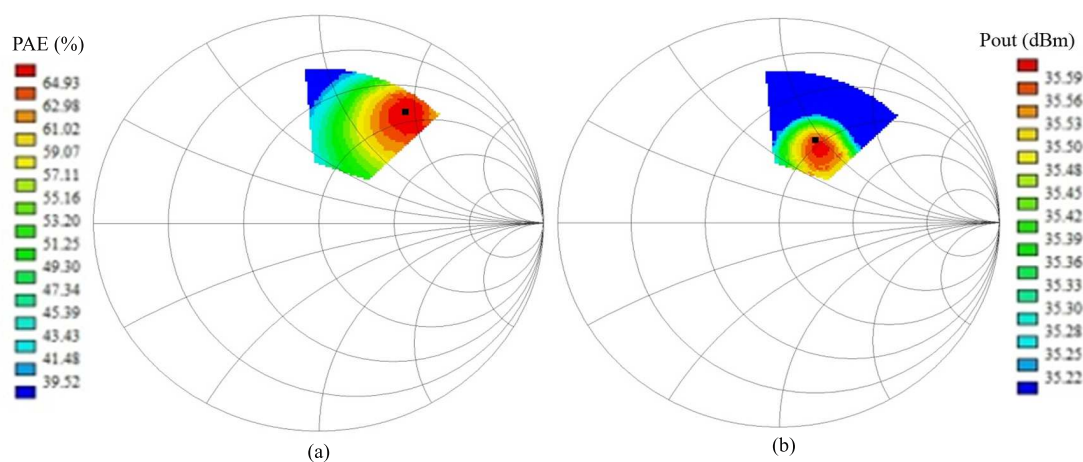
The first step was to evaluate the performance of the technology, in order to select the amount of active area required in order to fulfill specs. An on-wafer isothermal load-pull measurement campaign was performed over a small  $8 \times 75 \mu\text{m}$  v1s transistor cell, similar to the one shown in Figure 3.2. This cell size was chosen because there were no bigger ones available inside the wafer.



**Figure 3.2** – Power sweep measurement at 5.4 GHz over the  $8 \times 75 \mu\text{m}$  v1s GaN transistor cell shown on the left side. At P3dB the cell delivers 34.4 dBm that corresponds to 4.6 W/mm and performs with PAE=63.7%. The chunk was stabilized at 40 degrees and the selected biasing point was Vdd=30 V and Idc=13.5 mA

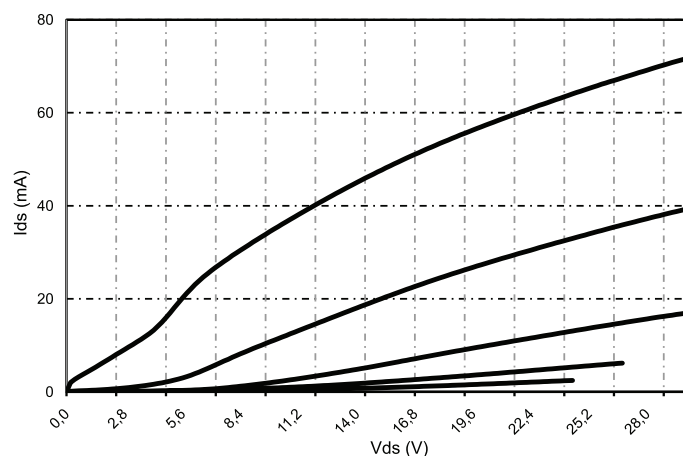
The graph in Figure 3.2 presents an example of a power sweep measurement over the mentioned cell at 5.4 GHz and up to the 3 dB compression point.

The data in Figure 3.3 show load pull measurements at constant 3dB compression, where the load impedance is swept at the fundamental frequency, while the  $2^{\text{nd}}$  and  $3^{\text{rd}}$  harmonic impedances are kept fixed to an optimal value. The load/source impedances were initially selected using the optimal values obtained from ADS Harmonic Balance (HB) simulations and afterwards tuned using load pull measurements. All the measurements were performed with the chunk at 40 degrees and the selected biasing point was Vdd=30 V and Idd=13.5 mA (22 mA/mm). Figure 3.3a shows the contours for PAE, while 3.3b shows output power contours. Power densities up to 6 W/mm and maximum PAE of 68% were measured at 5.4 GHz. This information was useful to select the total gate periphery needed to meet the specs. The foundry reported maximum power levels above this limit for this technology, but they recommend operating at close to 4 W/mm and not surpassing the 6 dB compression point. Power Added Efficiency >45% is feasible, as it was observed during the measurements.



**Figure 3.3** – Fundamental impedance load pull measurement at constant 3 dB compression for a  $8 \times 75 \mu\text{m}$  v1s cell with  $2^{\text{nd}}$  and  $3^{\text{rd}}$  harmonic fixed. (a) Measured PAE showing PAE max. 68% (b) Measured Pout showing Pout max. 35.65 dBm which corresponds to 6 W/m.

Figure 3.4 shows I/V curve measurements corresponding to  $8 \times 75 \mu\text{m}$  v1s devices. The curves show an atypical behavior inside the linear area, close to pinch-off. This might indicate the presence of trapping effects in the devices.



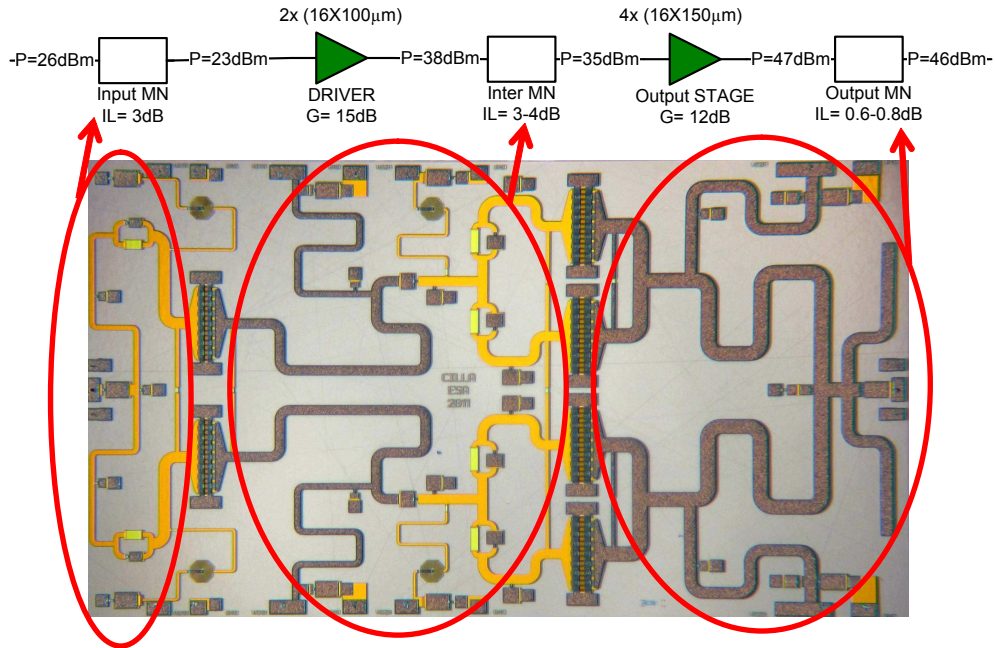
**Figure 3.4** – I/V curve measurements over  $8 \times 75 \mu\text{m}$  cell

### 3.3.2 Selection of MMIC Topology: Number of Stages and Cell Size

The size of the unit cell, number of gain stages, bias point and operational mode were selected to obtain a design fulfilling specs.

A schematic of the preliminary power budget is shown in Figure 3.5 together with

a view of the final layout design of the MMIC.



**Figure 3.5** – Initial power budget of the full MMIC design

Two stages were selected to achieve more than 20 dB power gain. A single stage would not be able to provide the required gain, and three or more stages would imply a lower associated PAE. The driver stage operates in the linear region, well under the 1 dB compression point, while the output stage operates around the 3 dB compression point.

The maximum output power available from a unit cell increases with the size of its gate periphery. At the same time, the cell gain is reduced. Increasing the cell gate periphery implies augmenting the length and/or number of transistor fingers. As an effect, the cell gate-source capacitance, the source inductance, the amount of heat dissipated by the cell and the current phase errors between fingers increase as well. The transconductance is also an inverse function of the channel temperature. A high gain per stage is an advantage because it contributes to a higher PAE. This is one of the reasons why small cells are typically used. Normally a gain of around 10 dB per stage gives good PAEs [54] p.161.

In the current design, the driver stage comprises of two 16X100  $\mu\text{m}$  cells (3.2 mm) and the output stage of four 16X150  $\mu\text{m}$  (9.6 mm) cells in parallel. The cell size of the driver stage was selected to deliver the required power to the output stage, while operating at 3 dB back-off from the 1 dB compression level. The driver stage was actually slightly oversized. The output stage to driver stage periphery ratio is three. The size of the cells at the output stage was selected to deliver 40 W being operated at

5.2 W/mm and, at the same time, to fit physically in the vertical direction of the given tile size. The power density level required is higher than the 4 W/mm recommended by the foundry. However, the measurements showed it is at these higher power densities that the achieved efficiency is higher. In the calculations, the output matching network losses were estimated to be between 0.6 to 0.8 dB at this frequency.

Another option would have been to combine 8 cells of  $8 \times 150 \mu\text{m}$  (9.6 mm total periphery) or 8 cells of  $16 \times 100 \mu\text{m}$  (12.8 mm), but the physical space was limited. Moreover, in these configurations the neighboring units cells had to share the source vias in order to fit in the vertical MMIC direction. Sharing vias would mean an increase of the source inductance per cell. As a result, the gain would decrease and the risk of oscillations would increase because of the higher negative feedback effect. This was observed in HB simulations performed in ADS. The effect of paralleling more cells also involves important loss of gain if there are phase imbalances when feeding the cells.

These relatively large cells were still providing more than 10 dB gain per stage, and therefore still allowed good PAE's.

### 3.3.3 Selection of Optimal Source and Output Loads

UMS provided both on wafer coplanar transistor cells and diced microstrip devices shown in Appendix A. The chosen cell size for the measurement campaign was the one closer to the cells used in the MMIC design ( $16 \times 150 \mu\text{m}$  and  $16 \times 100 \mu\text{m}$ ). Several versions of the transistors were provided with different physical distances from the gate to drain contacts in order to modify the performance and breakdown voltage. Version v1s was the final one used for the wafer manufacture.

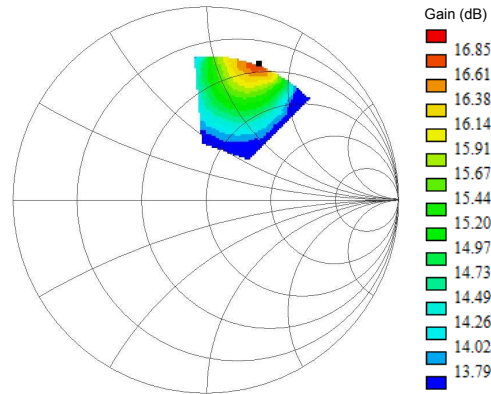
The load pull test bed shown also in Appendix A was installed in the RF Payload Systems Division Laboratory at ESA ESTEC to validate the large signal models and also select the optimal load and source impedances for the transistors in order to achieve maximum PAE [55–58].

Thermally controlled load pull measurements were performed on-wafer over a coplanar  $8 \times 75 \mu\text{m}$  v1s cell (device number AS45), and over microstrip  $8 \times 100 \mu\text{m}$  v9s diced devices attached to a gold carrier using AuSn 80/20 solder preform. The load impedance was tuned both at fundamental  $f_0$  and at harmonic frequencies ( $2f_0$  and  $3f_0$ ), and the source impedance only at fundamental  $f_0$ .

Measured load pull contours were shown previously in Figure 3.3, where the load impedance was swept at the fundamental frequency, while the  $2^{nd}$  and  $3^{rd}$  harmonic impedances were kept fixed to an optimal value, and the source impedance was selected to keep the device stable and at the same time provide a good matching at the input. Figure 3.6 also presents the measured transducer gain during this fundamental load pull sweep. The maximum transducer gain measured for the cell was around 16.8 dB. As expected the impedances giving better PAE are not the same as the ones allowing higher output power or higher transducer gain.

Load pull measurements of the  $2^{nd}$  and  $3^{rd}$  harmonic impedances were also per-





**Figure 3.6** – Measured Transducer Power Gain during a fundamental impedance load pull for a  $8 \times 75 \mu\text{m}$  V1S cell, while keeping the  $2^{\text{nd}}$  and  $3^{\text{rd}}$  harmonic fixed. Maximum measured value is 16.85 dB.

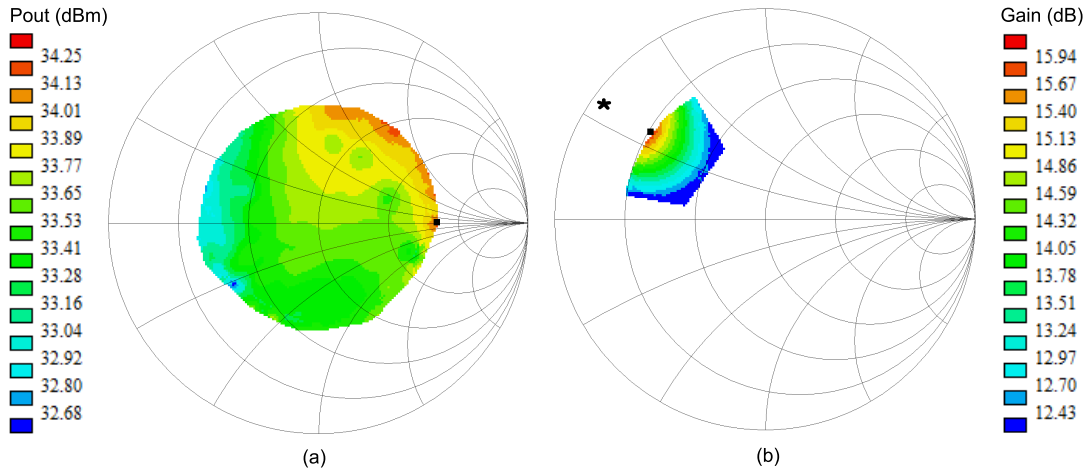
formed, while keeping the fundamental impedance fixed at the value of the one performing with higher PAE. But the data obtained was not as useful as the one obtained from the fundamental load pull, as explained hereafter.

The tuners used for the campaign were passive, and due to the losses in the test set up between the connector of the tuner and the transistor cell under test, it was not possible to present impedances at the device reference planes covering all the Smith chart. The insertion losses in the path were on the order of 1.8 dB at 5.4 GHz, and they were caused by a small coaxial cable, the probe head and the transitions. It is possible to get equations to find out what is the maximum value of the magnitude of the reflection coefficient that can be synthesized with a load pull tuner once the losses of the path are known [57]. At the frequency used here, the load pull tuner could synthesize loads with a maximum magnitude of reflection coefficient of 0.75, at the  $2^{\text{nd}}$  harmonic the maximum was 0.57 and 0.45 in the case of the third harmonic. Figure 3.7a presents the measured output power at 3 dB compression levels during a  $2^{\text{nd}}$  harmonic impedance load pull for the  $8 \times 75 \mu\text{m}$  v1s cell while keeping the fundamental and  $3^{\text{rd}}$  harmonic fixed to a constant optimal value. It is also possible to observe the maximum area of the Smith chart that is possible to cover, and that the impedances providing maximum power levels are located towards the area of high impedance level at the right hand side of the Smith chart. However, it is not possible to say if the optimal load level is in the unexplored area.

As it will be discussed later in more detail, it was decided to have the transistors operating under switching conditions in order to guarantee maximum efficiency. The harmonics were loaded at the transistor intrinsic plane with open or short loads. This typically implies that the optimal values of the harmonic loads at the outer reference plane of the transistor are located at the edges of the Smith chart. The transistor extrinsic parasitics afterwards transform the impedance level to a short or open at the

intrinsic reference plane.

It was not possible to synthesize these impedances at the edge with the tuners, and therefore the information obtained from these harmonic load pull measurements was only partially useful. The value of the second harmonic was selected from simulations. As expected, it was located at the edge of the Smith chart in the same angular direction as the optimal value shown in the measurements of Figure 3.7a

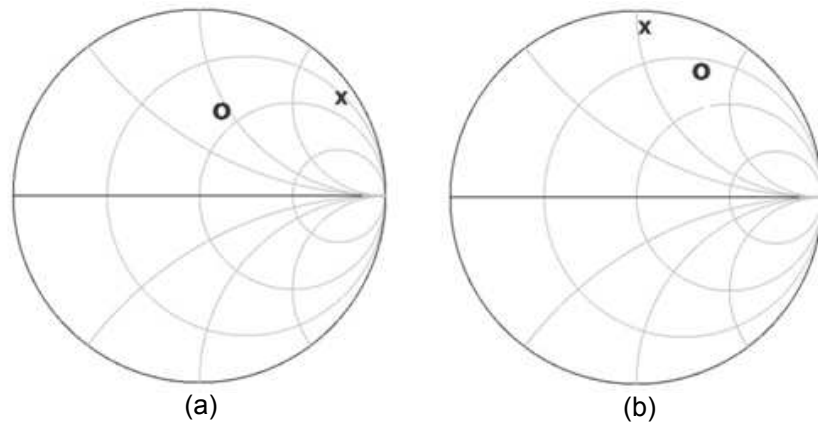


**Figure 3.7** – (a) Measured Pout during  $2^{nd}$  harmonic impedance load pull for  $8 \times 75 \mu\text{m}$  v1s while keeping fundamental and 3rd harmonic values fixed to a constant optimal value (b) Measured Transducer Power Gain during source impedance load pull over an  $8 \times 75 \mu\text{m}$  v1s transistor cell, while keeping the fundamental load fixed to a constant value providing optimal PAE and leaving  $2^{nd}$  and  $3^{rd}$  harmonics free.

Source pull measurements maintaining compression at 3 dB were also performed for the fundamental tone, while keeping the output load fundamental at a constant value providing optimal PAE, and leaving the  $2^{nd}$  and  $3^{rd}$  harmonics free. Figure 3.7b shows the measured transducer power gain during this source pull. As expected, the maximum gain is located in the edge of the swept area, in the direction of the complex conjugated input impedance of the transistor, shown in Figure 3.7b with \*. When attempting to move the source impedance in the direction of the complex conjugated matching input impedance, the device was starting to oscillate at some point. It was also possible to observe that the measured gate current was increasing from the  $\mu\text{A}$  range to the mA range when we were moving towards the impedance areas where the device was oscillating. Furthermore, a method to measure the input gate impedance of the transistor operating under large signal conditions, while loaded with the tuner optimal source impedance, was implemented and tested. This method is based on measuring the incident and reflected power with a dual directional coupler. It is not recommended to place the coupler at the output of the source tuner, close to the transistor gate, since the losses generated by the passive tuner contribute to further decrease the Smith chart area that could possibly be covered with the passive tuners. It is therefore necessary to sense

the inserted and reflected power levels with the coupler at the input of the tuner, and afterwards de-embed the effect of the tuner. The input tuner had been characterized before measuring the input reflection of the tuner when the output is loaded with three different well known standards.

As a result from this measurement campaign, the load at fundamental frequency providing the best PAE performance was selected for the final design, as shown in Figure 3.8b. The optimal load at  $2^{nd}$  harmonic frequency was selected from CAD simulations. Figure 3.8a also shows the combination of loads providing maximum output power.



**Figure 3.8** – Optimal combination of loading conditions at fundamental (circles) and  $2^{nd}$  harmonic frequency (cross) for  $8 \times 75 \mu\text{m}$  V1s cell with the device working at P3dB compression point (a) Loads providing maximum Pout and (b) Loads providing maximum PAE.

### 3.3.4 Small and Large Signal Model Validation

Transistor modeling is a very broad research field, and many publications can be found in the literature [59], [60]. Two models for this technology were provided at different time frames during the project:

1. UNIBO model

This model was available from the beginning and it was developed by the University of Bologna using on-wafer measurements of the same transistors cells that were tested during the load pull measurement campaign. This ADS model for the version v1s of the GH25 process is based on look-up tables and it includes thermal modelling [61], [62]. The model gave results close to the measurements, as it will be shown later, but it was computationally slow, and some convergence problems were experienced.

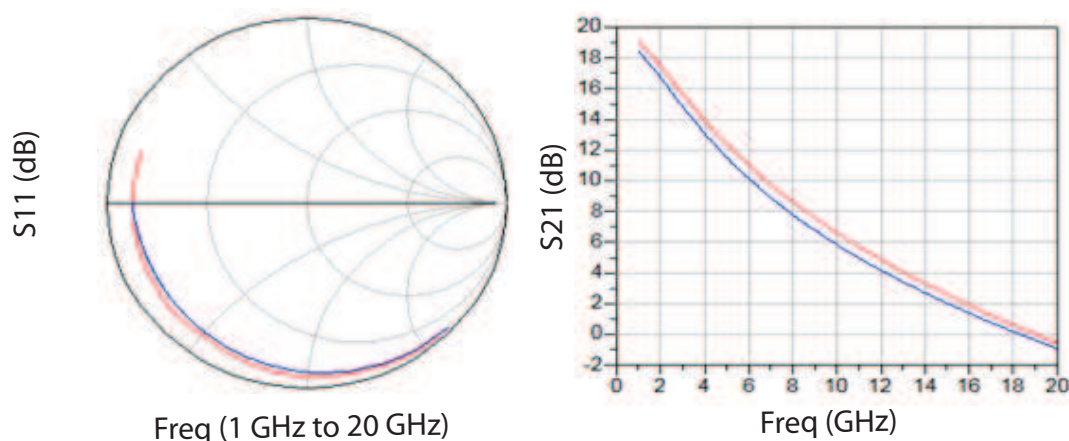
2. UMS model

This model was provided by the foundry at a later stage. It is based on measurements taken from version v3s of the process and represents an equation based

model that includes traps and self heating effects. This one was used for the final design since it is computationally better and without convergency problems.

The models provided can be biased up to 35 V. In this case  $V_{dd}=30$  V was selected to explore the GaN advantage of using higher voltages, thus reducing current levels and therefore losses. A larger operating DC voltage was not selected since high peak voltages can be problematic in space applications. Typically the solid state transmitters used in space applications are until now GaAs based, and they are supplied with low DC voltages on the order of 5-15 V. Furthermore, the capacitors used in this GaN process can handle a limited peak voltage.

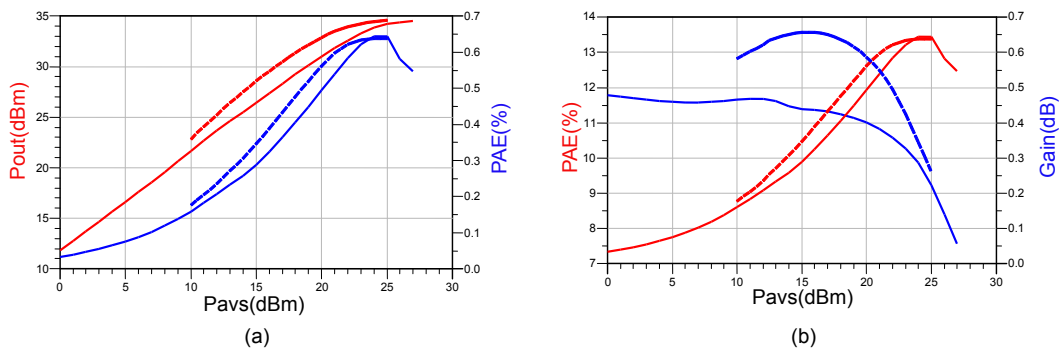
The model validation campaign included both small and large signal thermally controlled measurements. The UNIBO model is used for the comparisons shown here, since it was developed specially for this wafer run, but optimized for X-band frequencies used in other project parallel to this one. Figure 3.9 presents a comparison of the measured and simulated small signal parameters for the  $8 \times 75 \mu\text{m}$  v1s transistor cell at  $V_{ds}=30$  V and  $I_{ds}=30$  mA. Good agreement is observed, especially if we look at the input and output impedance levels, while there is a small difference in the gain of less than 1 dB. My experience shows that the most important for a model is to present a good agreement in the impedances, especially at the gate, where the input impedance level of large power transistors is very small, and a broadband matching becomes challenging.



**Figure 3.9** – Measured (red) vs. simulated (blue) small signal S-parameters for  $8 \times 75 \mu\text{m}$  v1s transistor cell at  $V_{ds}=30$  V and  $I_{ds}=30$  mA

Large signal model validation comprises comparisons of power sweeps and load pull data performed under CW conditions. The relatively low power levels delivered by the small cell up to around 4 W and the large area of GaN substrate available in the wafer for power dissipation, imply only small differences between pulsed and CW measurements. Figure 3.10a presents a comparison of the measured PAE and output power (dotted line) and the simulated ones (continuous line) during an input power sweep performed over the  $8 \times 75 \mu\text{m}$  v1s transistor cell at 5.4 GHz and using  $V_{dd}=30$  V and  $I_{dd}=13.6$

mA. The match between them is acceptable, and it is especially good close to the 3 dB compression point ( $P_{avs}=23.73$  dBm) and for small signal levels, in agreement with the results shown during the S-parameter measurements. At intermediate input power levels, there is a shift between measurements and simulations with respect to the available input power. This can also be appreciated while comparing the measured and simulated transducer gain, as shown in Figure 3.10b. This might indicate that the input impedance model is not that accurate for these intermediate input power levels.



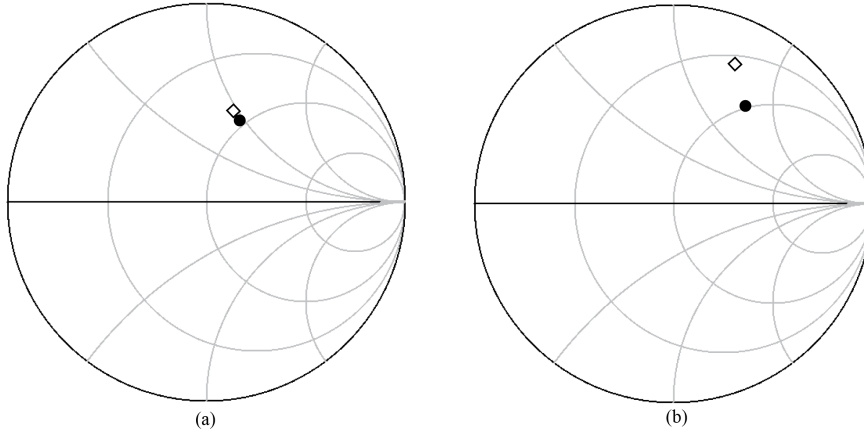
**Figure 3.10** – Comparison of the measurements (dotted lines) vs. simulations (continuous lines) during an input power sweep performed over the  $8 \times 75 \mu\text{m}$  v1s transistor cell at 5.4 GHz and using  $V_{dd}=30$  V and  $I_{dd}=13.6$  mA (a) PAE in blue and  $P_{out}$  in red (b) PAE in red and transducer gain in blue.

Figure 3.11a shows a comparison of the location in the Smith chart of the load delivering the highest output power during measurements and in the simulations, both at 3 dB compression. A good match is observed for the location of the maximum power. Figure 3.11b compares the location of the load delivering best PAE during measurements and in the simulations, both at 3 dB compression. In this case, the agreement is not as good as for the maximum output power, but still quite good, especially if we observe that the PAE drops very slowly while moving away from the maximum in Figure 3.3a.

The model received from UMS was also used to perform load pull simulations in ADS, and the location of the optimal impedances giving best  $P_{out}$  and PAE were very close to the ones measured for the  $8 \times 75 \mu\text{m}$  v1s cell. But the maximum value of the PAE and the output power obtained with the UMS model at those locations were more pessimistic than both the measurements and the simulations using the UNIBO model. This can be explained by the fact that the UMS model was developed for the iteration v3s of the process and the measured devices were belonging to iteration v1s.

### 3.3.5 Scaling

After validating the nonlinear model for the  $8 \times 75 \mu\text{m}$  v1s cell, scaling was required in order to choose the impedances for the larger  $16 \times 150 \mu\text{m}$  v1s cells used in the MMIC.



**Figure 3.11** – Comparison of load pull measurements (circles) vs. simulations (diamonds) for the  $8 \times 75 \mu\text{m}$  V1s cell with  $2^{\text{nd}}$  and  $3^{\text{rd}}$  harmonics optimally terminated. (a) The circle corresponds to  $\Gamma = 0.44 \angle 66.4$  with measured  $P_{\text{out}} = 35.65$  dBm and the diamond corresponds to  $\Gamma = 0.48 \angle 70$  with simulated  $P_{\text{out}} = 35.76$ . (b) The circle corresponds to  $\Gamma = 0.66 \angle 53.3$  with measured PAE = 67.9%, and the diamond corresponds to  $\Gamma = 0.75 \angle 68$  and simulated PAE = 70.68%.

Figure 3.12 shows how the optimal loading impedances moves along the Smith chart after the scaling both for fundamental and  $2^{\text{nd}}$  harmonic.

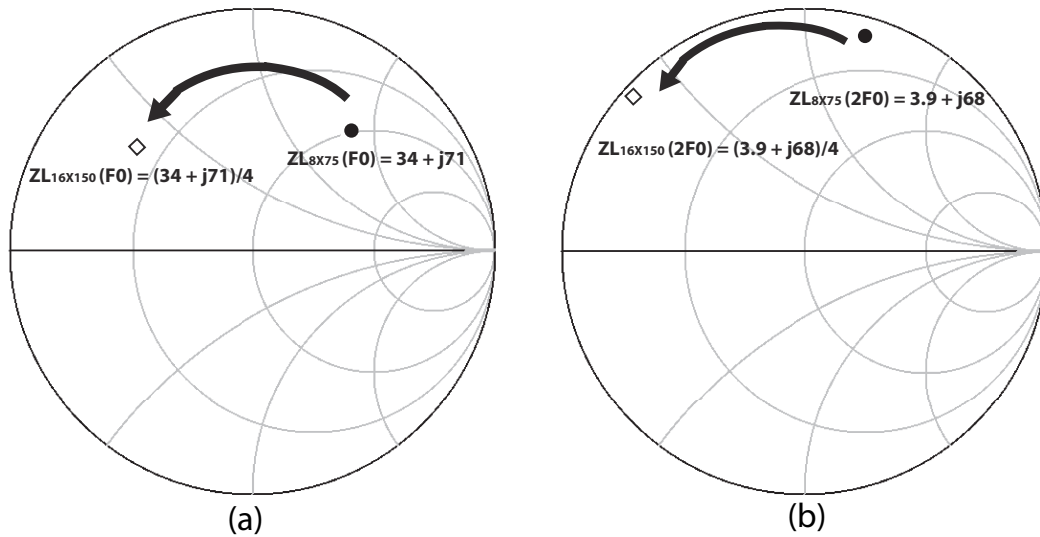
The UMS model was used for the most part of the full MMIC simulations, since the UNIBO models was very slow computationally. Figure 3.13a shows load pull simulations using the UMS scaled model, where the fundamental tone has been swept while the  $2^{\text{nd}}$  harmonic is placed around the optimal area obtained also from load pull simulations. The load stability circles are also plotted in blue in Figure 3.13b. All the circles that cross the Smith chart  $\Gamma = 1$  circle correspond to frequencies much lower than 5.4 GHz, while the circle at this frequency is just touching the edge of the  $\Gamma = 1$  circle in the Smith chart. In order to be on the safe side, and to avoid oscillations, the impedance selected at fundamental frequency for the final design is in the dark orange part of the swept area that is located farthest from the blue stability circles in Figure 3.13b.

Figure 3.14 presents a photo of the  $16 \times 150 \mu\text{m}$  v1s transistor cell fabricated in the same wafer run as the MMIC, and a  $2^{\text{nd}}$  harmonic load pull simulation for this cell using the UMS scaled model.

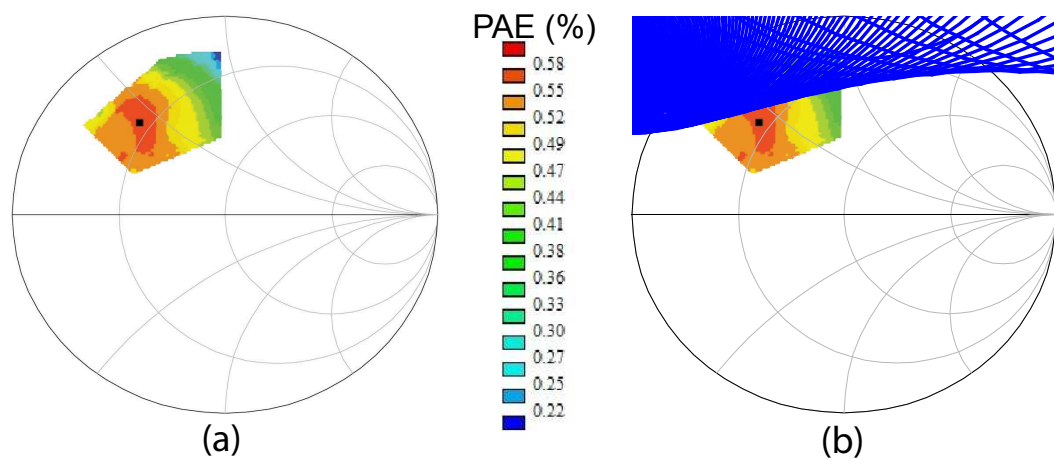
### 3.3.6 Selection of Biasing Point and Operational Conditions

Many efforts were required to establish the operation mode of the transistors and maximise their power efficiencies by ADS simulations. Harmonic Balance (HB) simulations using Advance Design Systems (ADS) were performed in order to select the operation mode of the transistor cells and maximize their power efficiency.

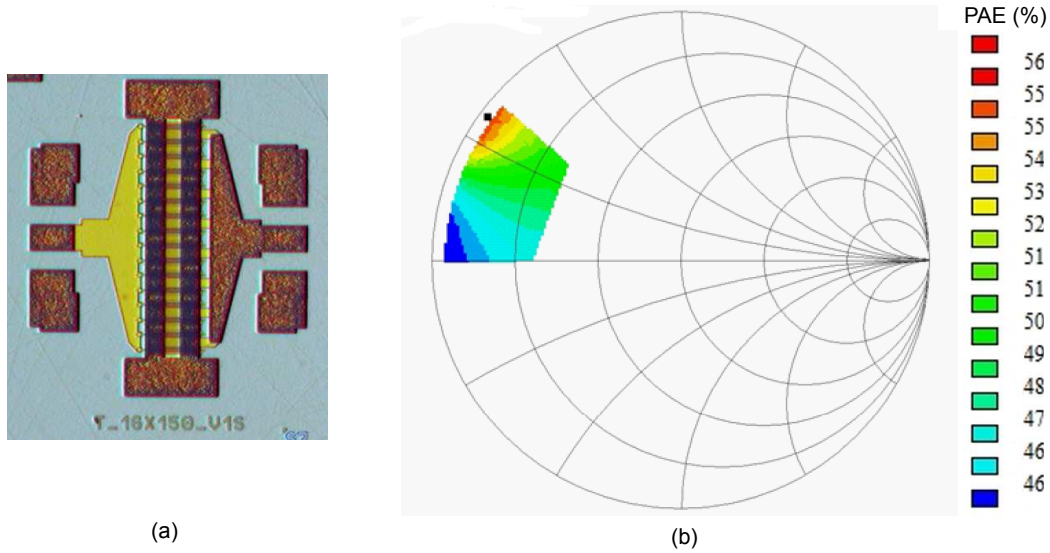
Figures 3.15 and 3.16 show the waveforms and load lines obtained at different nodes of an HB simulation performed over four paralleled  $16 \times 150 \mu\text{m}$  v1s cells. I used the



**Figure 3.12** – Optimal output impedance loading location (a) for the fundamental frequency and (b) for the 2<sup>nd</sup> harmonic after the scaling from the unit cell 8x75  $\mu\text{m}$  to the cell used in the design 16x150  $\mu\text{m}$



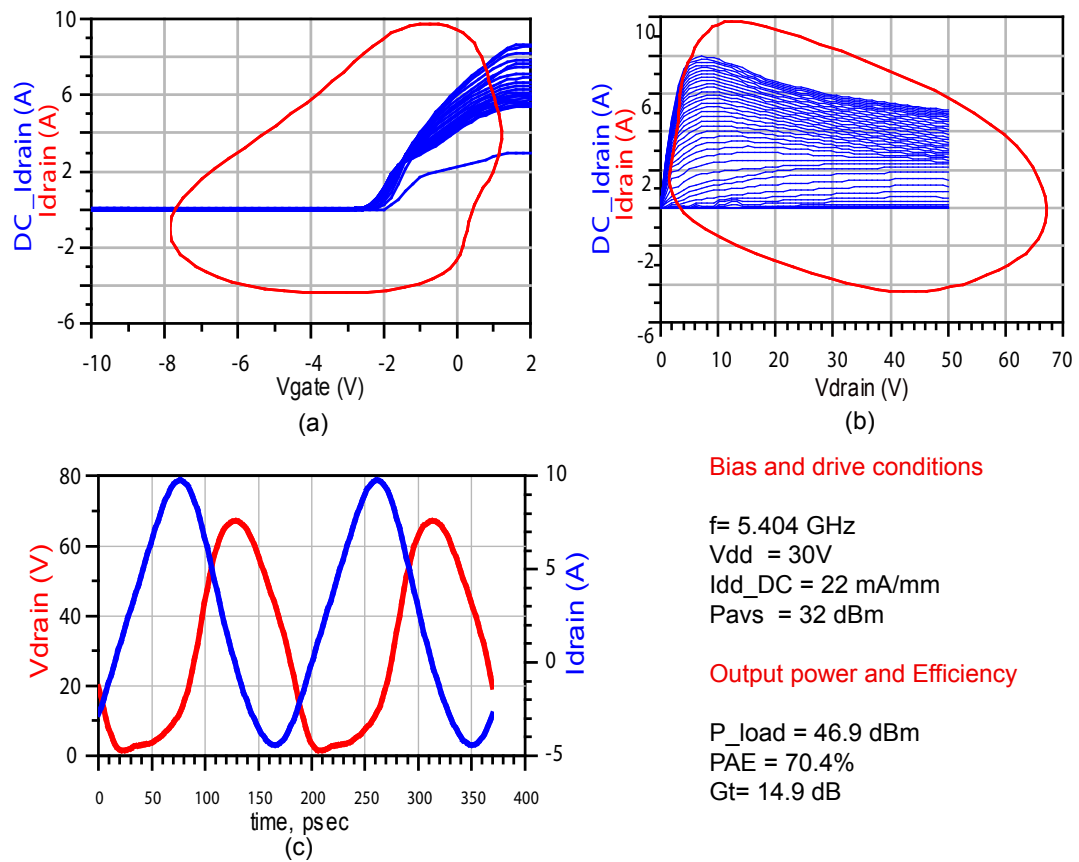
**Figure 3.13** – (a) Simulated PAE during fundamental impedance load pull for 4 paralleled 8x75  $\mu\text{m}$  v1s cells using UMS model at 4 dB compression point and 5.4 GHz. 2<sup>nd</sup> and 3<sup>rd</sup> harmonic fixed to a constant value (b) Small signal stability circles are also shown.



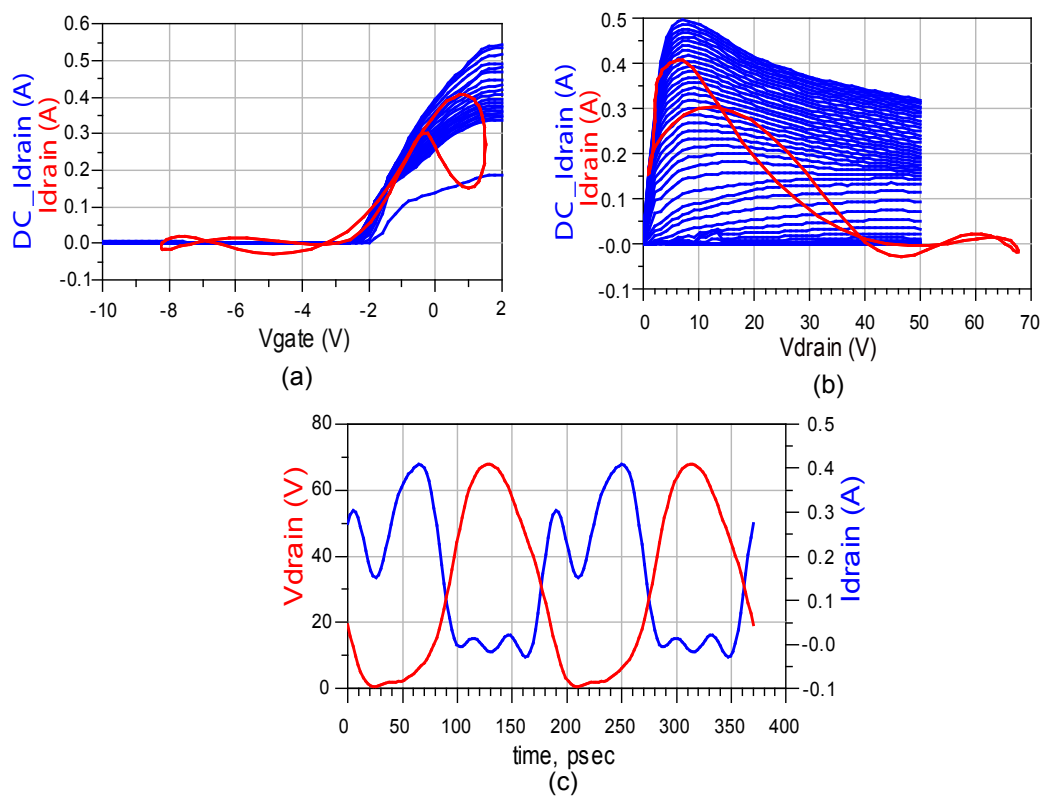
**Figure 3.14** – (a)  $16 \times 150 \mu\text{m}$  v1s transistor cell fabricated in the same run as the MMIC. (b) Simulated PAE during  $2^{\text{nd}}$  harmonic impedance load pull for 4 paralleled  $8 \times 75 \mu\text{m}$  v1s cells using UMS model at 4 dB compression point and 5.4 GHz. The fundamental and  $3^{\text{rd}}$  harmonic impedances were fixed to a constant value.

UNIBO model and ideal loading conditions providing maximum power added efficiency. The four devices in parallel perform with  $\text{PAE}=70.4\%$  and  $\text{Pout}=46.9 \text{ dBm}$  while using  $\text{Idd}_{dc}=22\text{mA/mm}$  and  $\text{Vdd}_{dc}=30 \text{ V}$  as DC biasing conditions. The waveforms in Figure 3.15c are measured at the external reference plane of the model that has been shown previously in blue in the photo of Figure 3.2. The dynamic load lines in red in Figures 3.15a and b are plotted over the blue DC I/V curves. The dynamic load lines do not always move following the DC curves due to the presence of capacitive and inductive parasitic extrinsic components in the model. This parasitics produce very different current and voltage waveforms at the intrinsic plane of the model, as it is shown in Figure 3.16c. These waveforms correspond to transistors operated in switching mode, and they explain the good efficiencies obtained in the simulations, since the overlapping between voltage and current at the drain is minimized as much as possible. Furthermore, the dynamic load lines in Figures 3.16 a and b follow the DC -IV curves quite well, indicating that the intrinsic plane has been identified correctly. The waveforms of a transistor operating under ideal switching mode are shown in Figure 3.17, where a semi sinusoidal drain voltage and a square-like drain current curve never overlap in time, avoiding power dissipation and producing an ideal, perfectly efficient amplifier [63]. In the design presented here, the efficiency is reduced due to the switching losses in the transistor, when the drain to source capacitor ( $C_{ds}$ ) is charged and discharged, and also due to the power dissipation losses in the channel resistance when the transistor is conducting [21], [64]. The waveforms are also useful to identify the peak voltage and

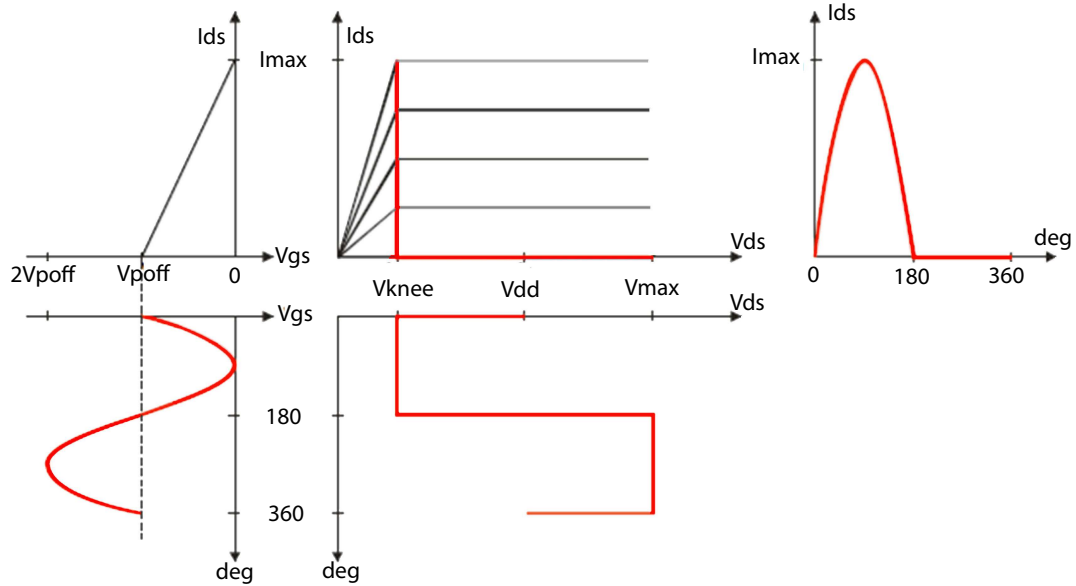




**Figure 3.15** – Waveforms and load lines at the EXtrinsic transistor reference plane obtained from an HB simulation performed over four paralleled 16x150 v1s cells (a)  $V_{\text{gs}}I_{\text{ds}}$  DC curves and dynamic load line. (b)  $V_{\text{ds}}I_{\text{ds}}$  DC curves and dynamic load line. (c) Waveforms at the EXtrinsic reference plane



**Figure 3.16** – Waveforms and load lines at the INtrinsic transistor reference plane obtained from an HB simulation performed over four paralleled 16x150 v1s cells. (a) VgsIds DC curves and dynamic load line. (b) VdsIds DC curves and dynamic load line. (c) Waveforms at the INtrinsic reference plane



**Figure 3.17** – Ideal waveforms of a transistor operating in switching mode.

current levels that will appear under large signal operation. The peak voltages up to 70-80 V shown in Figures 3.15 and 3.16 have to be considered carefully, in order to respect the breakdown voltage of the transistors and especially in this case not to surpass the maximum ratings of the capacitors [65]. An assessment of the peak current levels involved is useful to select the dimensions of the metal tracks and bondwire radius, in order to avoid electromigration and large losses in the matching networks [66], [54].

On the other hand, looking at the blue DC  $V_{ds}$ - $I_{ds}$  curves of Figure 3.16b, it is possible to observe that the model includes self heating effects because when the transistor is in the saturation region, with the channel open and operating far from pinch-off,  $I_{ds}$  decays as  $V_{ds}$  increases. This corresponds to a reduction of transconductance as the temperature increases because more power is dissipated in the device.

### 3.3.7 Matching and Biasing Networks Synthesis

Once the model has been validated and the final impedances have been selected, the next step is to synthesize these optimal impedances while keeping attention to other functions and requirements of the matching networks. The major challenge in the design was to match the low impedance levels at the same time at  $f_0$  and  $2f_0$ , while trying to get as much bandwidth as possible not only at  $f_0$ , but also at  $2f_0$ .

Details of the design of the matching networks will be provided in the next subsections, where I will often refer to Figure 3.18.

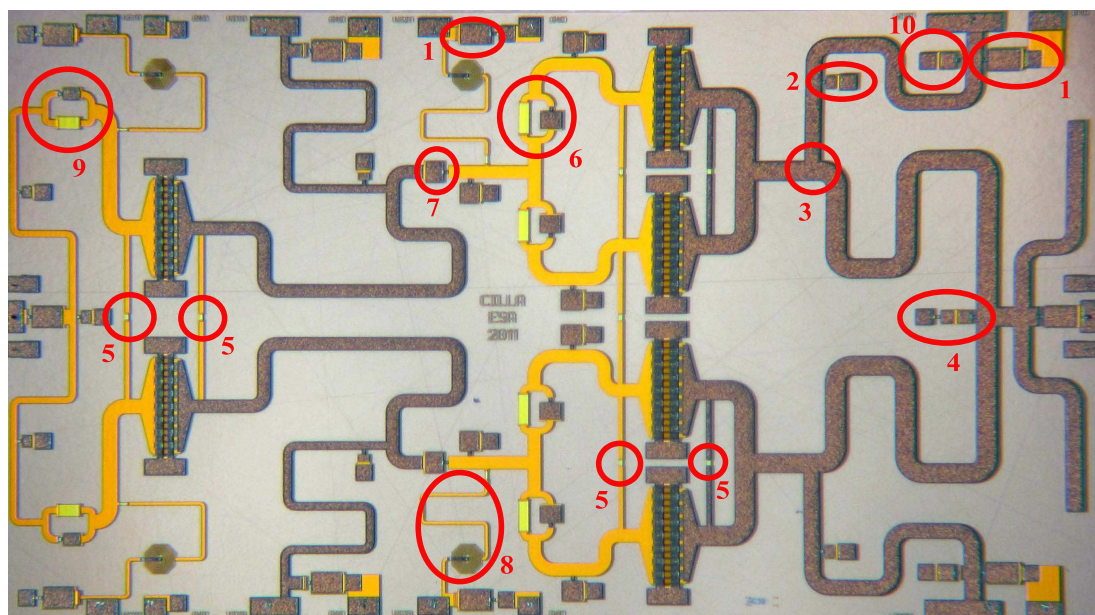


Figure 3.18 – Fabricated C-band MMIC

### 3.3.7.1 Biasing Network

The design of the biasing networks should be done in such a way that the structure is invisible at RF and a short at DC. The traditional way to implement this is to use a quarter wavelength transformer line loaded in the probe pad side by a capacitor or a butterfly stub that are a bypass (short) at the design frequency  $f_0$  [67] p.514. But this structure is not recommended in this particular design due to restrictions in the MMIC area. In this case a quarter wavelength structure over the GaN substrate occupies  $5387 \mu\text{m}$ , more than the width of all the MMIC. Therefore, other more compact structures have been used to synthesize the quarter wave transformer. In the biasing networks at the gates of the transistor cells, where low currents are involved, it is possible to use a series inductor (8 in Figure 3.18) to reduce the size of the quarter wave transformer. In the case of the biasing network at the drain of the transistors, the series inductors cannot withstand the high current levels expected with peaks up to 3-4 A. A lumped capacitor in parallel (2 in Figure 3.18) was used to reduce the required line length. These compact quarter wave structures are used to move in the Smith chart from the short created at RF by the big capacitor in the place where the DC pads are located (1 in Figure 3.18) to an open in the place where the biasing networks joins with the rest of the combining circuit (3 in Figure 3.18). The large capacitor (1 in Figure 3.18) produces a short at  $f_0$  because it is actually becoming inductive at our RF frequency due to the parasitics. This short also cancels any loading effect of the DC probes at RF. On the other hand, it is also important to consider carefully where to insert the DC biasing network in parallel with the matching network. In general it is better to place it close to the transistor ports, since the impedance levels at that points are lower, and

therefore the leakage through the bias network will be much smaller, keeping the losses under control. But it is of course also possible to place them in parallel in any other point of the matching network with low impedance level. The biasing network was also used as part of the network that controls the response at the  $2^{nd}$  harmonic, as it will be explained later in this section.

The biasing network was actually one of the critical structures in the design limiting the bandwidth due to its resonant-like behaviour. A quarter wavelength microstrip structure has a little more bandwidth than the compact quarter wave transformers used here. A solution to enlarge the bandwidth would be to use a structure with more cascaded segments. This was not done in this design since there was no more physical space available.

### 3.3.7.2 Output Matching Network

The output matching network presents symmetry around the centre axis and it was designed focusing basically on three issues:

1. Synthesize the load at fundamental  $f_0$  and second harmonic  $2f_0$  that provides optimal PAE. [68], [69]. Initially I intended to control fundamental  $f_0$ ,  $2^{nd}$  harmonic  $2f_0$  and  $3^{rd}$  harmonic  $3f_0$  impedances, but finally I decided to focus only on fundamental and  $2^{nd}$  harmonic since there was a limited space available and the structure needed to control the  $3^{rd}$  harmonic was also introducing extra losses that were hindering the improvement in efficiency. According to my ideal simulations, controlling the  $3^{rd}$  harmonic impedance was providing only a 2-3% improvement in efficiency. Hereafter, I explain how I implemented the harmonic manipulation, controlling the response at fundamental  $f_0$  and  $2^{nd}$  harmonic at the same time [70–77]. The small capacitor in the circle number 10 in Figure 3.18 is a short at  $2f_0$  and, as was mentioned in the previous section, the big capacitor with the tag number 1 in the same figure is a short at  $f_0$ . On the other hand, the quarter wave transformer structure at  $f_0$  is a full wave transformer at  $2f_0$ . Therefore, the biasing network transforms the short at  $2f_0$  in a new short at the point where the matching network joins the rest of the circuit (3 in Figure 3.18). In this way, the microstrip fork combining structure going from the output of the transistors in the output stage to the place where the biasing network joins the rest of the output matching network (3 in Figure 3.18) is used just to control only the  $2^{nd}$  harmonic impedance presented to the transistors. Since the biasing network is setting a short at the point where the biasing network joins the combining structure, all the elements placed in parallel between that point and the output of the MMIC are not affecting the  $2^{nd}$  harmonic matching. The rest of the structure between the point 3 in Figure 3.18 and the output of the MMIC is used to control the impedance loading level at fundamental  $f_0$ . This technique is used to isolate the structures controlling the impedances at  $f_0$  and  $2f_0$ , and in this way it is much easier to guarantee that they do not affect each other.

2. Creating a combining network presenting low insertion losses ( $< 0.8$  dB)

The insertion losses of the output network were controlled carefully, since they reduce the efficiency dramatically [78]. Therefore it is very important to understand the different mechanisms generating losses:

- Finite conductivity of the metal layer that composes the microstrip lines
- Parasitics in lumped components
- Dielectric losses in the substrate (tangent losses)
- RF Power leaked through the biasing lines

The metal used in MMIC design is typically gold. The finite conductivity of the metal has to be accurately estimated and cannot be changed, but the cross section area of the line can be increased in order to reduce the losses. The skin depth of gold at  $f_0$  is around  $1.1 \mu\text{m}$ , and as a rule of thumb it is typically recommended to use around 5 skin depth of metal height in order to avoid extra RF losses and waste of precious metals [79]. The top metal layer used to create the sandwiched structure of the lumped capacitors can be used to fabricate thicker microstrip lines with  $6.8 \mu\text{m}$  thickness instead of using only the regular metal layer with  $1.8 \mu\text{m}$  thickness. In our particular case the losses were reduced 0.3-0.4 dB when using this feature. The drawback of these thickened lines is that they are more prone to present spreads in the line width than the normal  $1.8 \mu\text{m}$  thick lines. But the impact has been proved not to be relevant in our design since the lines used are quite wide. It is important to highlight that the width of the lines was selected to handle a maximum of 18-20 mA/ $\mu\text{m}$  following the indications from the foundry. In the worse case scenario, assuming that the output stage operates at a PAE of just 40%, the average DC current required from the output network biasing lines would be 3.3 A, and the minimum line width required would be 90  $\mu\text{m}$ . At the end, lines of more than 120  $\mu\text{m}$  width were selected. Losses due to finite conductivity are also reduced if the lines are wider.

The parasitic in the lumped components has to be taken into account in order to estimate the losses. In the present design, the use of lumped components in the output matching network was minimized, because they introduce extra losses. Smaller capacitors used in parallel in the circuit present larger parasitic impedances in parallel and therefore generate smaller losses than larger capacitors. However, as a drawback, the small capacitors are more affected by the spreads during fabrication than larger capacitors. Capacitors in parallel with the combining structure are lossier in areas of the matching circuit with higher impedance levels, since the impedance in that point is closer to the value of the parasitic resistance. As an example, the losses of a 1.5 pF capacitor in a zone of the output matching network with impedance level of 4 Ohm was only 0.02 dB, while the same capacitor was generating losses around 0.2 dB in a zone of 50 Ohm impedance level.

Furthermore, the breakdown voltage of the capacitors indicated by the foundry is in the order of 40-50 V, and this peak values can be exceeded as it was shown in the waveforms of Figure 3.15c, reaching peak voltage levels up to 80-90V. Therefore, instead of a single capacitor in paralell, two capacitors in series (4 in Figure 3.18) had to be placed in parallel in selected places of the output matching network in order to withstand these levels, even thought this increases the losses.

Simulations in ADS of the full output matching combining network were performed and the power that leaks into the biasing network accounts for losses of around 0.1 dB.

### 3. Provide the required bandwidth

It is important to provide the required bandwidth at  $f_0$ , but also at  $2f_0$ . The bandwidth of the  $2^{nd}$  harmonic has to be double than the fundamental in order to keep high performance along all the band.

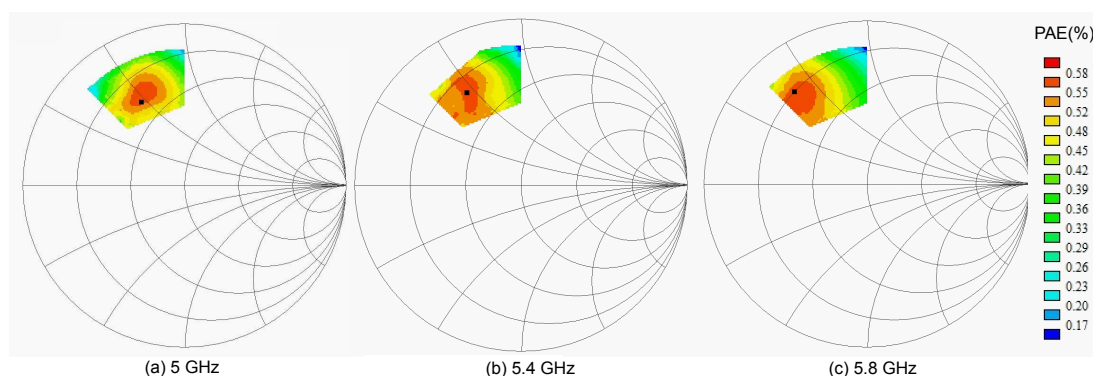
As it was mentioned before, one of the critical structures with respect to the bandwidth was the biasing networks. But the bandwidth of the rest of the matching networks are important as well. For the rest of the output matching network three different methods of providing bandwidth were tested:

- (a) During the matching impedance process I tried to stay with constant small Q factors in the Smith chart [80]. The relationship between bandwidth and Q factor is given by the following equation:

$$W_{3dB} = \frac{w_0}{Q} \quad (3.1)$$

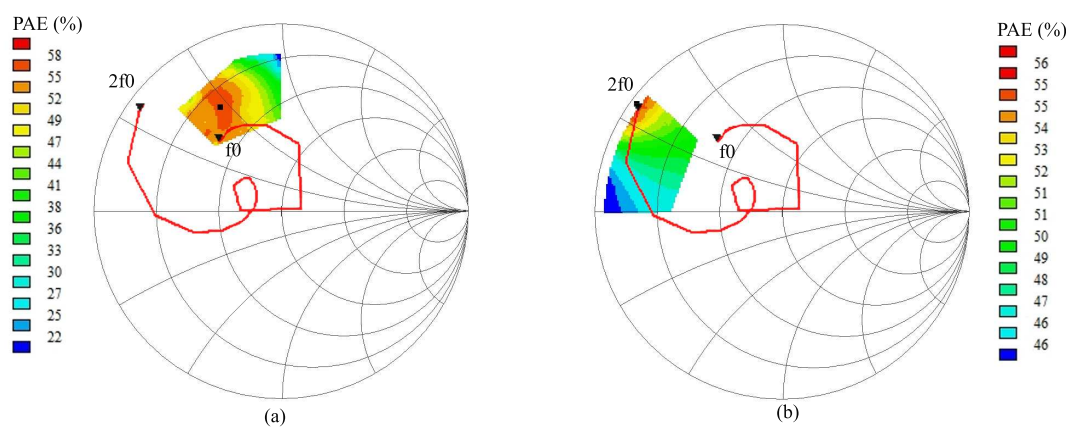
From the equation, it is possible to see that following low Q contours will imply having larger bandwidth. One of the ways of following low Q contours is to place multiple networks in series creating a high order structure. But this is not always possible as there is always a trade-off between the required bandwidth and the physical space available, the losses introduced by higher order networks and the increase in the spreads when networks with many sections are introduced.

- (b) It is possible use the parasitics of the lumped capacitors to create small loops in the impedance curve, as it will be shown later for the Intermediate matching network. This technique had the inconvenient that large capacitor values were needed, and therefore losses of the output matching network were increasing considerably. Therefore, this technique was not used for the Output matching network.
- (c) After performing load pull simulations of the transistor cell at different frequencies within the specified bandwidth, as shown in Figure 3.19, I tried to follow the load pull contours showing maximum PAE with the matching network design [81–83], but I could not find a network being able to follow this pattern while at the same time controlling the impedance at the harmonics.



**Figure 3.19** – Simulated PAE during fundamental impedance load pull for a  $16 \times 150 \mu\text{m}$  v1s cell using UMS model at 4 dB compression point and at different frequencies (a) 5 GHz (b) 5.4 GHz (c) 5.8 GHz

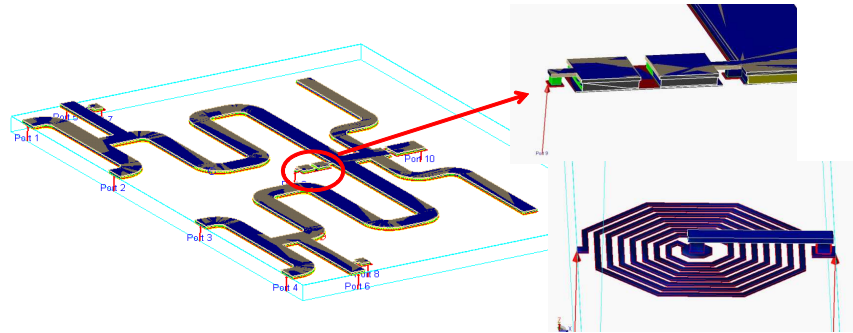
Figure 3.20 illustrates the synthesized impedance by the output matching network (red curve) and the PAE load pull contours for the  $16 \times 150 \mu\text{m}$  cell. It is possible to observe that I simultaneously managed to control the fundamental frequency and the  $2^{\text{nd}}$  harmonic frequency.



**Figure 3.20** – Synthesized output impedance (red curve) and load pull contours showing PAE contours for the  $16 \times 150 \mu\text{m}$  cell (a) at fundamental frequency  $f_0$  (b) at  $2^{\text{nd}}$  harmonic frequency  $2f_0$ .

Momentum 2.5D full-wave electromagnetic simulations of the lumped components and matching networks used in the MMIC had to be used in order to ensure accuracy. The simulations included the detailed stack of layers for the GH25 process provided by UMS. Lumped capacitors and inductors were simulated, obtaining responses shifted in frequency, when compared with the models available at the library. Full-wave simulations of the output matching network were also performed including the lumped capacitors. Figure 3.21 shows the 3D drawing of the simulated output matching network, two capacitors in series and an inductor.





**Figure 3.21** – Detail of 2.5D ADS Momentum Electromagnetic Simulation of the Output matching Network, two capacitors in series and an inductor.

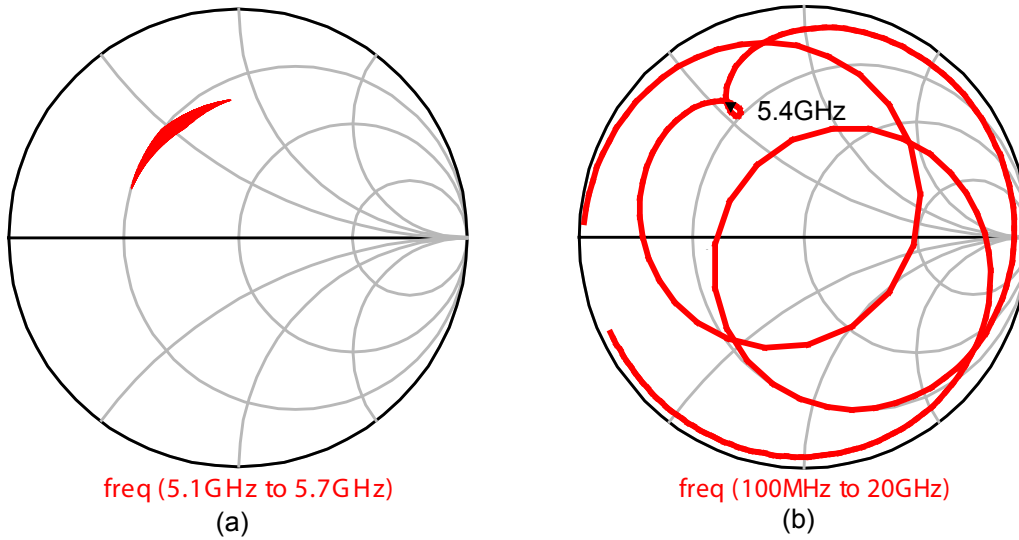
Moreover, Monte Carlo simulations of the full output combining network confirmed that the spreads were not affecting the performance significantly, as shown in Figure 3.22a. But it is also important to say that the losses of the matching network were oscillating 0.1-0.2 dB during the Monte Carlo analysis, even though the number of lumped components was minimized, and this greatly helped to control the spreads.

Monte Carlo simulations of the biasing network using 1000 trials were especially interesting in order to assess how the resonant like structure could shift in frequency affected by different dc pad impedance loading conditions and spreads in fabrication process. The conclusion was that the structure was almost unaffected by the dc probe loading impedance and slightly affected by the spreads in the capacitor value.

### 3.3.7.3 Interstage Matching Network

The inter-stage matching network was designed with focus on matching the gates of the output stage transistors with the impedance needed to transfer as much power as possible from the driver to the output stage. At the same time, it was also designed to load the output of the driver stage with the correct impedance. The driver is working in a linear region, at least 3 dB under the 1 dB compression point, and the impedance selected is the optimal one to ensure that the driver is providing maximum PAE at this point of operation. The inter-stage impedance matching is done directly without the need of going through the 50 Ohm point in the Smith chart.

The selected source impedance at the gate of the output stage was obtained from load pull measurements and it is not complex conjugated of the input impedance of the transistor. From the simulations and measurements it was observed that the input impedance of the transistor in this design is lower, and if complex conjugated was attempted, the device was starting to become unstable and oscillate. In this particular case, during the design process of the interstage matching network, the synthesized source impedance that the transistors at the output stage sees at the gate was selected



**Figure 3.22** – (a) Monte Carlo analysis of the impedance seen by one of the output stage transistors at  $f_0$ . The parameters spreads are the dc probe loading impedance and all the capacitor values. 1000 trials are plotted. (b) Load impedance at the driver stage output, synthesized by the interstage matching network and showing the loop at  $f_0$  for increased bandwidth operation.

to be  $Z_{source} = (15 + j18)/4 = 3.75 + j4.5$ . With this impedance the simulated gate input impedance was  $Z_{gate} = 0.34 - j4.3$ . As said before, trying to conjugate match at the gate creates a negative input impedance for the transistors. Therefore the technique that was followed consists of tuning the imaginary part, while the real part of the source impedance will be larger than the input impedance, creating mismatch, but contributing to a stable design.

The low frequency gain was controlled with the use of a parallel RC lumped structure tagged with 6 in Figure 3.18. This high pass network kills the large gain of the transistors at low frequencies avoiding low frequency oscillations, and it helps to compensate the device gain roll-off contributing to maintain the gain flat across the bandwidth of the design. There is a compromise between the maximum gain provided by the MMIC and the improvement in stability that is controlled by the values of the RC network. The RC network introduces extra losses at the transistors gate, but this does not have a big impact in the MMIC overall efficiency, since the small signal gain per stage is still around 10 dB. The MMIC gain was designed to be flat across our bandwidth, compensating the typical gain roll-off slopes of the active components with engineered slopes for the insertion and reflection losses for both the input and inter-stage matching networks.

A decoupling capacitor tagged with 7 in Figure 3.18 is also used to isolate the DC biasing of the two stages. All the decoupling capacitors have to resonate at the design frequency  $f_0$  to minimize losses when placed in series in the RF path.

The bandwidth of the interstage matching network was carefully considered. It was

achieved by creating a small loop in the synthesized impedance around  $f_0$  in the Smith chart by taking advantage of the parasitic components of the capacitors as shown in Figure 3.22b. This technique involves the use of relatively large capacitors that are lossier than smaller ones. But these losses in the interstage matching network do not have a big impact in the overall PAE of the MMIC, and they are actually needed to keep the design stable.

#### 3.3.7.4 Input Matching Network

The input matching network was designed taking care of the following aspects:

1. Insert as much power as possible into the MMIC driver.
2. Control the stability of the MMIC using a parallel RC network tagged with 9 in Figure 3.18.
3. Contribute to the MMIC gain flatness along the bandwidth

The input matching network matches the input of the driver transistors to 50 Ohms along the full bandwidth, allowing maximum insertion of power. The problem however was that the matching was not possible along the full bandwidth because of the limited chip area available for this network. Due to the lack of area, the input matching network is not broadband, and actually the mismatching differences between different frequencies of the band are also used to contribute partially to the flattening of the MMIC gain. For the next versions of the MMIC, it would be interesting to increase the chip area slightly in order to allow larger bandwidth of the input matching network.

An inductor in series is used to create a quarter wavelength structure in the biasing networks located at the gates of the transistors in both stages, and tagged with 8 in Figure 3.18. The use of lumped inductors is possible since the current levels consumed by the transistors at the gates are very small. The biasing networks at the gates have a bandwidth slightly larger than for the biasing networks at the drains. A resistor is also used in series with the inductor in order to improve stability at low frequencies. The value of this resistor was selected based on small and large signal stability analysis.

Moreover, in all the matching networks I have also used large stabilization resistors between the drains of the different cells, as well as between the gates, as shown in the circles tagged with 5 in Figure 3.18. This was done in order to avoid odd mode oscillations, and large signal stability analysis at different frequencies demonstrated that they were effective [84–86]. Theoretically no RF currents are flowing through these resistors if we assume that the voltage waveforms are symmetrical at both sides of the resistors, and therefore there are no voltage drops along the resistors. A small resistor was also placed in series with the parallel bypass capacitors located close to the DC pads, in order to have a resistive termination at the end of the biasing networks and to contribute to the stability of the design.

### 3.3.8 Full MMIC Harmonic Balance Simulations

The nonlinear model was used together with the synthesized matching networks to perform Harmonic Balance simulations using ADS. The results from a nonlinear simulation showing a power sweep for the full MMIC design at 5.4 GHz are presented in Figure 3.23.

Figure 3.24 presents the overall two stages PAE, output power, and transducer gain for a frequency sweep at constant input power  $P_{avs}=24$  dBm, close to 6 dB compression. As it can be seen, the simulated bandwidth is 450 MHz (5.1-5.55 GHz) for a gain variation of less than 0.5 dB (22-22.5 dB), with corresponding output power of more than 40 W (46-46.5 dBm), and a PAE variation of less than 3% (38% to 41%). The results are obtained using the UMS nonlinear model and also Momentum 2.5D full-wave electromagnetic simulations of the matching networks and lumped components that uses the stack of layers for the GH25 process provided by UMS.

Both small and large signal stability analysis were performed. The small signal or linear stability analysis included an investigation of the stability circles and the traditional Rollets factor. But this is certainly not enough, mainly because the method does not guarantee the internal stability of the circuit [87]. The large signal stability covers even and odd mode internal stability analysis, and is based on the introduction of a single- and multiple small perturbation in different internal nodes of the design (Floquet Multipliers [88]). A Harmonic Balanced simulation using mixer mode was performed using ADS and afterwards the poles and zeros of the transfer function were identified using the software tool STAN [89], [90]. Harmonic Balance simulations using Monte Carlo analysis were performed for the full MMIC using the spreads provided by the foundry and changing the loading impedances at the DC biasing ports. The spreads were shifting the response in frequency and degrading the performance as it is shown in Figure 3.25, but their influence was minimized when the device was operating under high compression conditions, as it can be observed in Figure 3.26, where 75 iterations were performed using the recommended spread in the physical parameters. It was not possible to present data at 6 dB compression point where performance was optimal, for the Monte Carlo frequency sweep in Figure 3.25 because there were problems with the model convergence at some frequencies.

## 3.4 Measurements

The photos presented in the Appendix B show the test set up that was built at the Payload Division Laboratory at ESA ESTEC, the MMIC probed and ready to be tested and other relevant photos from the measurement campaign. Three dies were mounted over two different types of carriers: CuMoCu carrier and aluminium diamond carrier. I selected the same dies that were partially tested on-wafer at UMS. The die S8, mounted over a CuMoCu carrier, was the one used for all the measurements presented

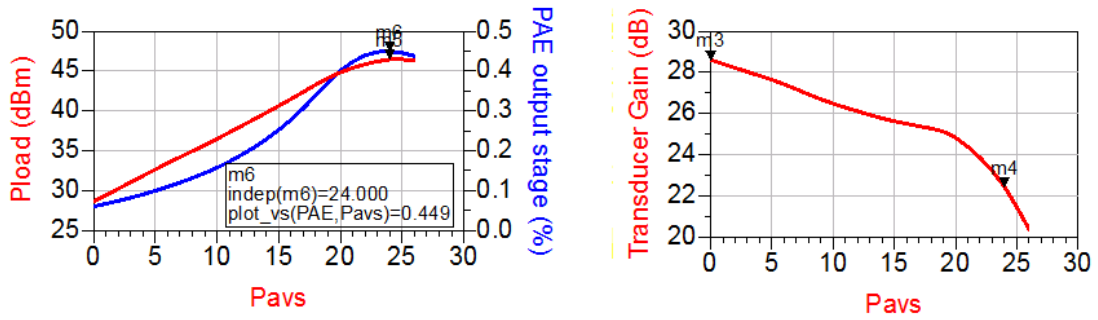


Figure 3.23 – Simulation of full MMIC power sweep at 5.4 GHz using UMS nonlinear model.

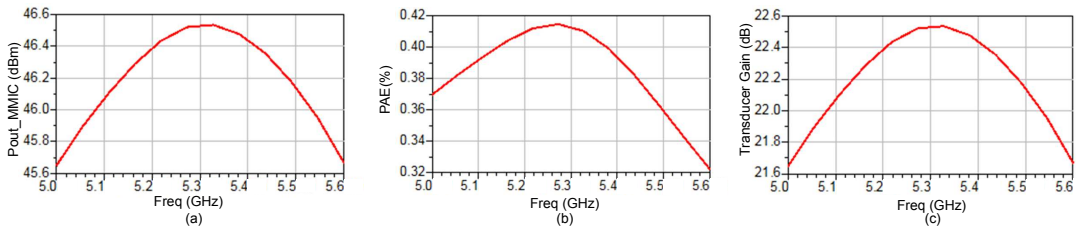


Figure 3.24 – Simulation of full MMIC frequency sweep using UMS nonlinear model at Pavs=24 dBm, close to 6 dB compression point.

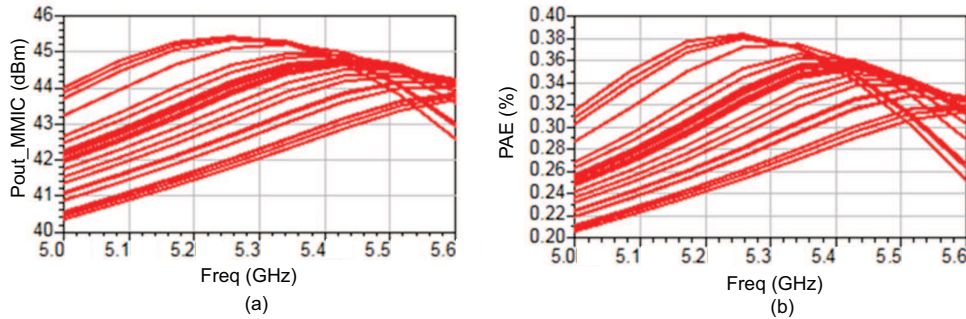


Figure 3.25 – Simulation of the spread of the MMIC performance over a frequency sweep at constant Pavs= 20 dBm (4 dB compression point)

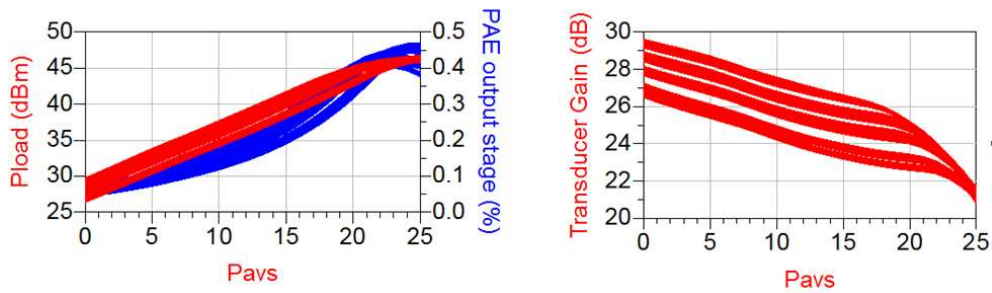


Figure 3.26 – Simulation of the spread of the MMIC performance over a power sweep at 5.4 GHz

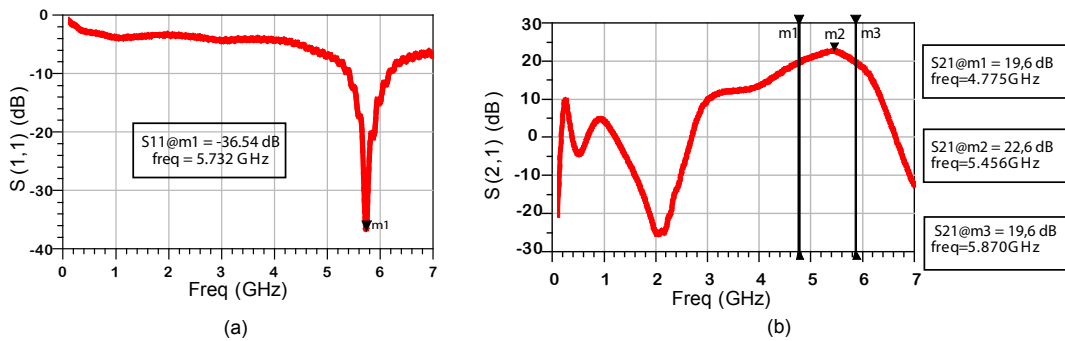
hereinafter.

All the passives included in the test set up were previously calibrated and their contribution has been de-embedded from the measurements. After calibrating the full test set up, the losses of a small on-wafer thru was measured using GSG probes with 200  $\mu\text{m}$  pitch. The losses measured were ranging between 0.1-0.15 dB while doing a source power sweep like the one used during the measurements afterwards.

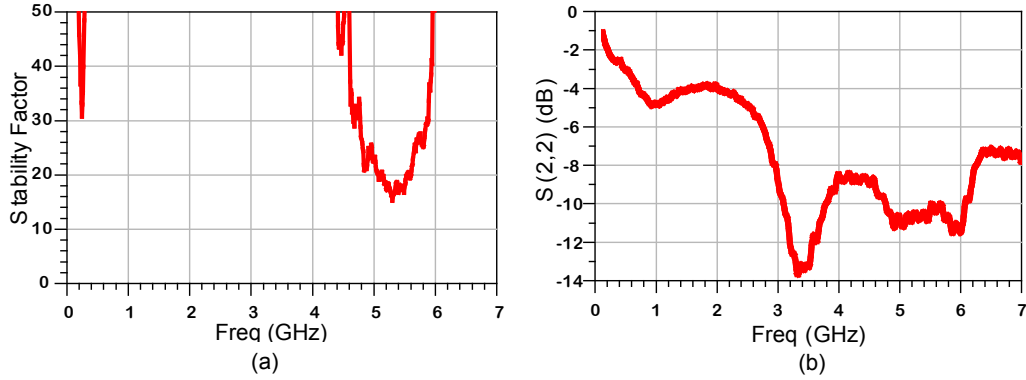
During the device DC biasing procedure, oscillations were appearing when the second stage drain quiescent current was increased above 126 mA. This problem was solved by placing a 20 Ohm resistor in series with the biasing network at the gate of both the driver and booster stages. No efficiency was lost since the current levels in these branches are in the micro Ampere range. Furthermore, the DC probes supplied by UMS, and shown in appendix B, already include resistors of 10 Ohms in series at the gate biasing lines and a shunt capacitor of 22 pF at all the DC biasing needles. Stability was also tested by using a small signal frequency sweep from 100 MHz to 7 GHz (Pin= -40 dBm) and observing the output at the spectrum analyzer. During the testing, it is important to apply bias in the correct sequence in order to avoid damage of the transistors, and also to limit the current levels of the DC supplies [91].

### 3.4.1 S-parameter Measurements

Figure 3.27 and 3.28 show S-parameter measurements of the full MMIC with the reference plane at the tips of the GSG probes. The DC biasing conditions used during the measurements included  $V_{dd} = 30\text{V}$ ,  $I_{d_{driver\_stage}} = 70\text{mA}$  and  $I_{d_{output\_stage}} = 278\text{mA}$ . Figure 3.27b shows the measured parameter S21 between the probe tips. The measured small signal 3 dB bandwidth is 1.1 GHz, corresponding to 20.4%. Figure 3.28a shows the measured Rollets stability factor, well above 1 in this case.



**Figure 3.27** – MMIC measured S-parameters at the tips of the probes (a)S11 (b)S21



**Figure 3.28** – (a)MMIC measured Rollets stability factor (b) MMIC measured S22 parameter at the tips of the probes

### 3.4.2 Pulsed Power- and Frequency Sweep Measurements

Pulsed power measurements were done sweeping the power available at the source from 16 dBm to the 5 dB compression point using steps of 0.3 dB. A pulse repetition frequency of 1 KHz and pulse length of 100  $\mu$ s were used, corresponding to 10% duty cycle. Input available power (Pavs), Output power (Pout), Transducer Gain and PAE were measured.

The Transducer Gain was calculated as the difference between output power (Pout) and the input power available at the reference plane located at the tips of the RF probes (Pavs). When there is perfect matching at input and output ( $\Gamma_L$  and  $\Gamma_S$  are zero), the small signal transducer power gain is equivalent to  $S_{21}$ .

Power Added Efficiency (PAE) calculations include the current consumed by both the driver and booster stages. PAE was calculated in two different ways:

1. The first one, obtaining the consumed current by measuring the voltage drop over high precision small resistors in series with the DC biasing lines. This measurement technique is more accurate than reading the current consumed from the GPIB buses of the DC sources. The DC currents were measured accurately using a 20 Ohm series resistor at the gates and a 0.5 Ohm resistor at the drains. The resistors used for the measurements were calibrated for different current levels. This method works well while doing CW measurements, but our experience shows that it is not optimal in the case of pulsed measurements, specially for duty cycles under 10%.
2. The second way of obtaining the PAE was to get accurate measurements of the pulsed current with a calibrated current sensor that was outputting 0.25 mV/A (Pearson Electronics INC model 6595). The pulsed output voltage coming out of the transformer was displayed over an oscilloscope. There was a decaying ringing in the current consumption at the beginning of each pulse. This is due to the lack

of large decoupling capacitors close to the MMIC. Actually there were long cables of at least 2 meters between the MMIC DC pads and the power supply terminals. The mission of the decoupling capacitors, used in the biasing lines, is to stabilize the voltage delivered to the circuit when there are constant changes in the current drawn by the transistors, as it occurs under pulsed operation, due to the switch ON and OFF of the RF source. The capacitors provide a source of charge, in order to provide the needed current as fast as possible without having drops in the supply voltage. Large capacitors should be placed close to the MMIC during future measurement campaigns.

The two methods do not provide the same results when performing pulsed measurements. This is mainly because of the ringing in the long cable between the supply terminal and the MMIC DC pads. This ringing appears at the first half of the pulse and makes the average current measured over the resistor not to be accurate enough. The PAE measurements shown hereafter are obtained using the second method. The measurements are accurate for pulsed operation, since the value of the current used in the calculations corresponds to the last part of the pulse, where the variations on current consumption and the DC voltage levels had fully stabilized.

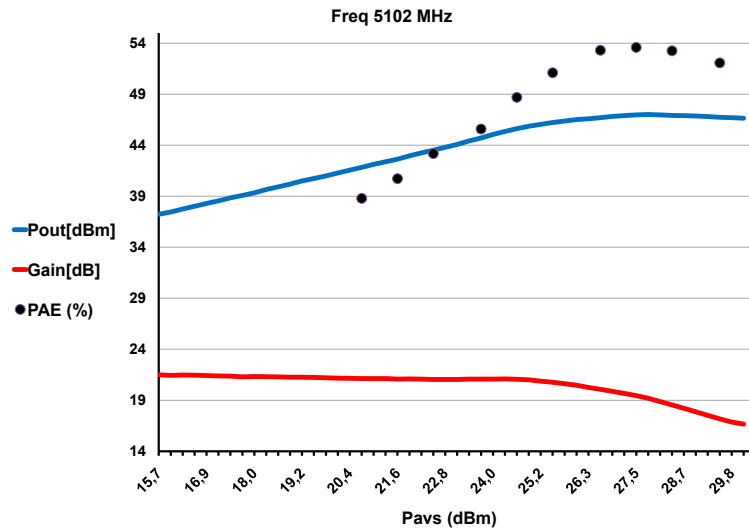
The drain of the driver stage was biased using a different DC supply than for the drain of the output stage. Both were also measured separately.

Pulsed power sweep measurements were recorded from 4.8 to 6 GHz. Gain and Output Power data were sampled using frequency steps of 50 MHz, and PAE data was obtained using frequency steps of 100 MHz. The DC biasing conditions used during all the pulsed measurements were the same as the ones used during the S-parameter measurements,  $V_{dd} = 30V$ ,  $I_{d_{driver\_stage}} = 70mA$  and  $I_{d_{output\_stage}} = 278mA$ .

Figure 3.29 shows the measured MMIC Pout in blue, Gain in red and PAE as a black dotted curve during a pulsed source power sweep at 5102 MHz. Power sweeps at other frequencies are not shown here for convenience, but the data retrieved was used to build the frequency sweep with constant Pavs shown in the AppendixC. During the campaign, the maximum average power level measured was 47.26 dBm (53.16 W, Gain=15.9 dB) at a frequency of 4.74 GHz. Similar values were obtained between 4.6 and 5.1 GHz. The maximum overall PAE measured using the calibrated sensor was 55.8% at 4.9 GHz (Pout=47.19 dBm and Gain=17.51 dB) These maximum power levels and PAE were measured when the device was working at compression points between 2.5 and 3 dB.

The PAE of the booster alone was calculated from the current consumptions after assuming that the gain between the input of the MMIC and the input of the booster stage is 9 dB. This gain value was obtained from ADS simulations. Under this assumption, the maximum booster PAE was around 64.7% at 5.1 GHz. This value is in agreement with the PAE measured during the load pull campaign over single cell transistors as it was shown in section 3.3.1. It also matches well with the maximum levels obtained during simulations using the UNIBO model, that were presented in section 3.3.4.





**Figure 3.29** – Measured MMIC performance during a pulsed source power sweep at 5102 MHz.

Figures in appendix C p.115 show measured PAE, Gain and Output Power along the frequency band 4.5 to 6.1 GHz using constant source available power. In order to analyze in detail the MMIC response, the representative data is reproduced here for convenience in Figures 3.30 and 3.31.

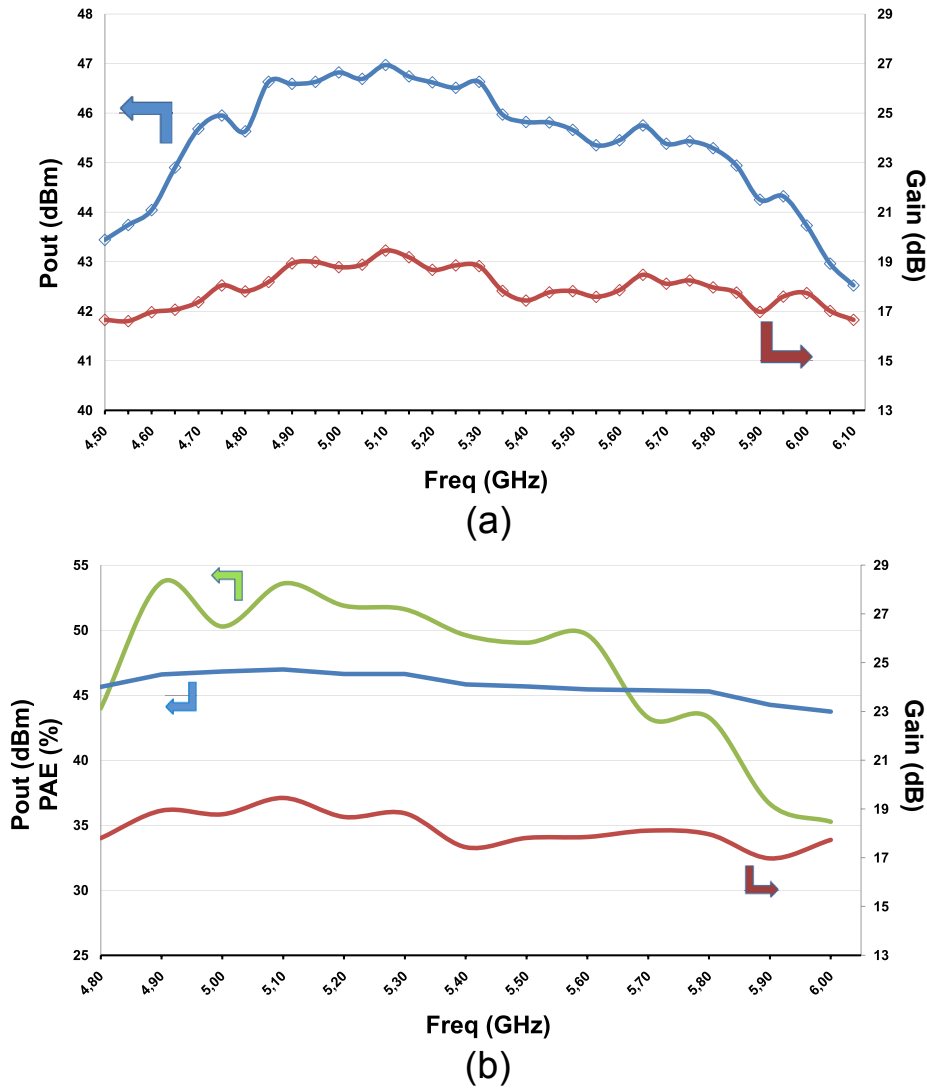
The MMIC presents a good bandwidth under large signal operation. Figure 3.30a presents data at 1-2 dB compression point, showing that in the frequency range from 4.85 GHz to 5.3 GHz the output power is larger than 40 W (46.75 dBm +/- 0.25 dB) with the gain ranging around 19 dB. This corresponds to a 0.5 dB bandwidth of 450 MHz. PAE varies between 50%-54% along all this frequency range as shown in Figure 3.30b.

Figure 3.31 presents data around 2-3 dB compression point, showing that in the frequency range from 4.85 GHz to 5 GHz the output power is larger than 50 W (47.15 dBm +/- 0.05 dB). This corresponds to a 0.1 dB bandwidth of 150 MHz. PAE is well above 50% along all this frequency range (Figure C.7 in appx. C, p.119).

It is also interesting to observe how the measured parameters are changing as we approach the 3 dB compression point. We can observe that the maximum PAE, Pout and Gain are centered at 5.4 GHz when operating in the linear region or at low compression levels, and it moves towards 4.9 GHz when operating at 3 dB compression point. The S-parameters presented previously in Figure 3.27, were centered at 5.4 GHz, as well as the performance shown in Figure C.1 of appx. C p.116, that corresponds to the operation around 0.5 dB compression point.

The Gain shown in Figure C.9 in appx. C and measured under small signal operation (Pavs=16 dBm), matches with the measured  $S_{21}$  shown in Figure 3.27b, at the frequency where there are matching at input and output. In both cases, gain is around 22 dB at

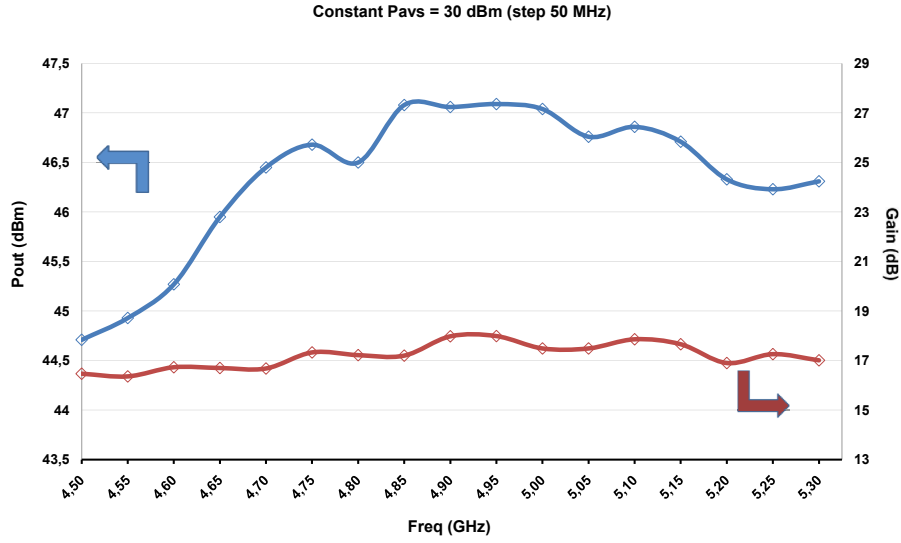
5.4 GHz.



**Figure 3.30** – (a) Measured MMIC Pout (blue) and Gain (red) during a frequency sweep using constant Pavs=28.5 dB (b) Measured MMIC Pout (blue), PAE (green) and Gain (red) during a frequency sweep with constant Pavs=28.5 dBm

### 3.4.3 Junction Temperature Calculations

The maximum junction temperature for GaN is typically around 200 degrees. Further information on GaN thermal performance can be found in [92] and [93]. Junction temperature specification has been identified as one of the challenges in future space based GaN high power amplifiers, due to the high power densities of the devices. Maximum junction temperature of 150 degrees was required for this design. The derated



**Figure 3.31** – Measured MMIC Pout(blue) and Gain(red) during a frequency sweep using constant Pavs=30 dBm

junction temperature for space operation is currently under review in Europe. In order to fulfill this requirement, a proper die attach and a design with very high efficiency is required. Thermal calculations for the cell used in the design are presented here.

The junction temperature for the 16x150  $\mu\text{m}$  cell was calculated under the following working conditions:

- MMIC mounted on a CuW carrier (2.5 x 1.5 cm) of 1 mm thickness.
- Baseplate temperature of 80 degrees.
- Device performing with the maximum efficiency measured during the campaign as it was presented in the previous subsection 3.4.2.

Starting with a baseplate temperature of 80 degrees, the equilibrium temperature reached by the backside of the MMIC once the device is operating is calculated.

$$T_{case} = T_p + P_{dissMMIC} * R_{thcc} \quad (3.2)$$

where  $T_{case}$  is the temperature on the backside of the MMIC under operation,  $T_p$  is the initial temperature of the baseplate (80 °C),  $P_{diss}$  is the dissipated power by the full MMIC and  $R_{thcc}$  is the carrier to case thermal resistance.

50  $\mu\text{m}$  thick AuSn 80/20, with 55 W/m°C solder to case conductivity, are used to attach the HPA on the carrier. The HPA dimensions are 6.73 mm X 3.75 mm. The carrier to case thermal resistance can be calculated as follows:

$$R_{thcc} = \frac{1}{R_{th\ soldertocase} * \frac{MMIC_{width} * MMIC_{length}}{solder_{thickness}}} = 0.036 \frac{^{\circ}\text{C}}{\text{W}} \quad (3.3)$$

Taking into account the possible imperfections during the soldering process a 50% reduction of the soldering surface has been assumed. This is a conservative assumption and therefore  $R_{thcc}$  will be considered  $0.072 \text{ }^\circ\text{C/W}$ . In this case, using the  $52.3 \text{ W}$  measured output power and  $55.8\%$  two-stage MMIC efficiency, the total dissipated power is  $41.42 \text{ W}$ . The case temperature becomes then:

$$T_{case} = 80 + 41.42 * 0.072 = 83^\circ\text{C} \quad (3.4)$$

The power dissipated by each of the four cells at the output stage is approximately  $7.13 \text{ W}$ . According to the measured-based calculated data presented in section 3.4.2, if the full MMIC is working under these conditions ( $P_{out} = 52.3 \text{ W}$ ,  $PAE = 55.8\%$ ), the cells of the output stage should be working at around  $PAE 64.7\%$ . The junction temperature can then be calculated as:

$$T_{junction} = T_{case} + P_{diss\ cell} * R_{thjtoc} \quad (3.5)$$

where

$$R_{thjtoc} = \frac{R_{th0\ 1mmcell}}{dieperiphery} + \frac{R_{thC\ 1mmcell}}{dieperiphery} * (T_p - 36) + \frac{R_{thP\ 1mmcell}}{dieperiphery^2} * P_{disscell} \quad (3.6)$$

where the data measured during parallel activities is used:

$$\begin{aligned} R_{th0\ 1mmcell} &= 14.75 \frac{^\circ\text{C}}{\text{W}} \\ R_{thC\ 1mmcell} &= 0.055 \frac{^\circ\text{C}}{\text{W}} \\ R_{thP\ 1mmcell} &= 0.6 \frac{^\circ\text{C}}{\text{W}^2} \\ dieperiphery &= 2.4\text{mm} \\ P_{disscell} &= 7.13\text{W} \\ T_c &= 80^\circ\text{C} \end{aligned}$$

Substituting this numbers we obtain  $T_{junction} = 137.8^\circ\text{C}$ . This junction temperature value fulfills the  $150^\circ\text{C}$  preliminary derated specification for space operation.

#### 3.4.4 CW Power- and Frequency Sweep Measurements

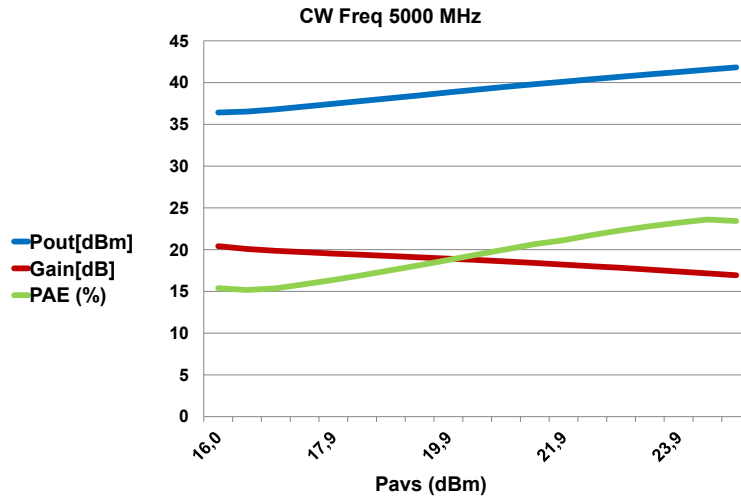
CW measurements were performed, after the pulsed ones, from  $4.6$  to  $5.8 \text{ GHz}$  using a  $50 \text{ MHz}$  step, and varying the source power up to the  $3 \text{ dB}$  compression point. A serious degradation of performance was observed when comparing with the pulsed measurements, because of the thermal effects. The device was also compressing at much lower power levels than in the case of the pulsed measurements. The baseplate temperature was keep constant at  $25$  degrees during both the CW and the pulsed testing with  $10\%$  duty cycle. The junction temperature in both cases can be calculated as it was done in subsection 3.4.3, but including the effect of the pulsing. The calculations show that the difference in junction temperature is  $45$  degrees in the best case. This can explain the degradation of performance observed during CW testing.

The DC biasing conditions used during all the CW measurements were very similar to the ones used during both the pulsed and the S-parameter measurements  $V_{dd} = 30V$ ,  $I_{d_{driver\_stage}} = 60mA$  and  $I_{d_{output\_stage}} = 290mA$ .

After performing the CW power and frequency sweeps, the DC biasing currents consumed by the device with the RF signal off had been modified to  $I_{d_{driver\_stage}} = 50.7mA$  and  $I_{d_{output\_stage}} = 190mA$ , even though the DC gate voltages applied were still the same. This indicates that there might have been some damage to the transistor channels or the transistor has very long memory effects. This deviation was also observed during the load pull measurement campaign over single cell transistors.

The maximum power level measured was only 41 dBm (PAE=24%, Gain=16 dB) at a frequency of 5 GHz, as shown in Figure 3.32. PAE has been calculated using the measured DC currents extracted from the voltage drop over a precision resistor.

Figures 3.33 and 3.34 show measured PAE, Gain and Output Power along the frequency band 4.6 to 5.8 GHz using constant available power at the source and 100 MHz as frequency step. Figure 3.33 presents data when the transistor is tested with a relatively low  $P_{avs}$ =17 dBm, and the device in Figure 3.34 is clearly compressing when  $P_{avs}$ =21 dBm is used. In both cases, the performance is poor if compared with the pulsed measurements, due to self-heating.



**Figure 3.32** – CW measured performance during a source power sweep at 5000 MHz

An on-wafer preliminary measurement campaign under pulsed conditions was also performed over three different devices at the foundry before the final test campaign. The available power was swept at the input up to only 24 dBm and the frequency from 5 to 5.8 GHz. The same testing and biasing conditions were used. It is important to emphasize that the devices were not pushed into compression during these preliminary measurements. The data obtained during both measurement campaigns is in agreement, and the most relevant information obtained from this preliminary campaign was that the three devices which were measured show similar performance.

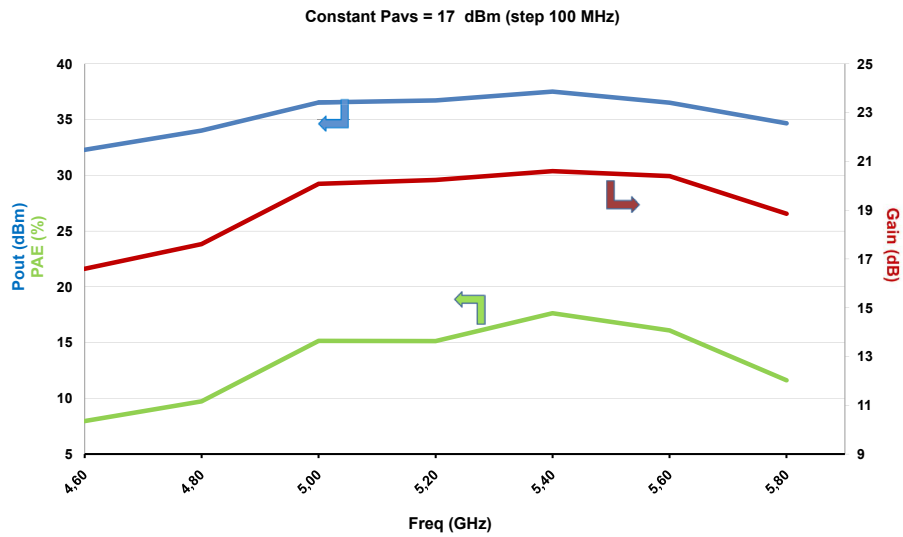


Figure 3.33 – Measured performance during a CW frequency sweep with Pavs=17 dBm

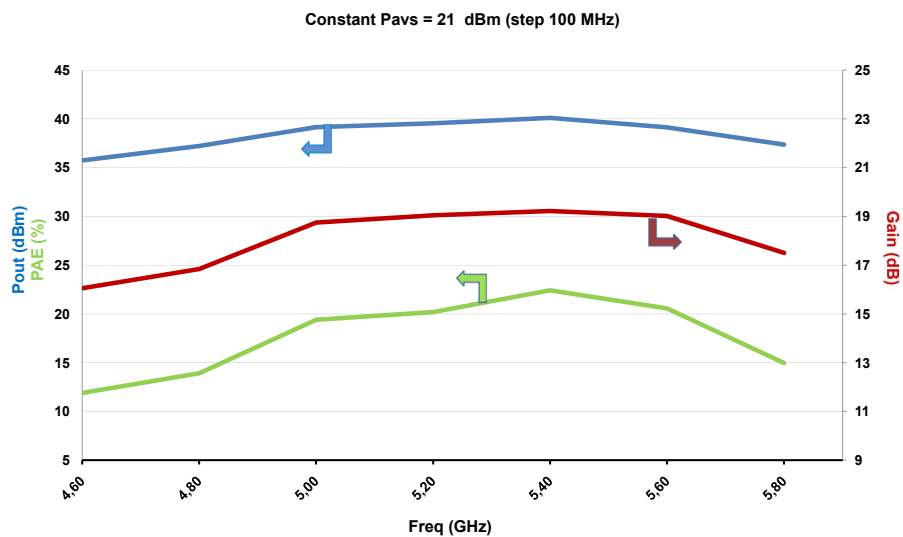


Figure 3.34 – Measured performance during a CW frequency sweep with Pavs=21 dBm

### 3.4.5 Comparison Measurements-Simulations

A comparison between simulations and measurements is a good exercise in order to demonstrate the usefulness of the models used for the project, since a lot of time was invested in ADS HB simulations. As it was mentioned in section 3.3.4, two models for this technology were provided. A comparison between the full MMIC simulation using the UMS model and the MMIC measurements is presented here, since I had convergence problems with the UNIBO model.

Figure 3.23 p.43 presented a power sweep of the full MMIC using the UMS model at 5.4 GHz, the center frequency of the design. On the other hand, Figure 3.29 showed the measurements obtained during a power sweep at 5.106 GHz, close to the measured center frequency of the MMIC. It is obvious that the MMIC design center frequency has been shifted down. The shift in frequency might be explained partially by the spreads introduced during the fabrication process as predicted in the Monte Carlo analysis shown in Figure 3.25 p. 43. This issue will be clarified in future measurement campaigns over several devices. It is not fully correct to compare responses at two different frequencies, but in my opinion it is still interesting to compare the simulated and measured power sweeps.

It is interesting to observe that the shape of the transducer power gain is quite different when comparing simulation and measurements. Direct comparison is not 100% fair, since the graphs have different Y-scales. But it is clear that in the simulations the device starts to compress at very low power levels, and the maximum output power and PAE were found when operating around the 6 dB compression point, while the measurements show a softer compression curve and optimal operation is found to be around 2-3 dB compression point. During the measurements, source available power levels on the order of 30 dBm had to be used in order to reach the 3 dB compression point, while simulations were showing hard compression operation at much lower power levels on the order of 24 dBm. The maximum power level simulated with the UMS model was 46.5 dBm as shown in Figure 3.23 p.43, while the maximum power measured was 47.2 dBm. It is also possible to observe that the simulated PAE's using the UMS model are worse than the measurements. Maximum overall simulated MMIC PAE using the UMS model was around 45%, while the measurements showed values of up to 55%. This was already observed during the single cell load pull measurement campaign presented in section 3.3.4, where it was also observed that the UNIBO model was predicting higher levels of PAE in agreement with the measured ones.

Looking at Figures 3.25 p.43 and 3.26 p. 43 we can conclude that the spreads of several parameters during fabrication alone cannot explain the 10% of difference in PAE performance between simulation and measurements. I believe the reason for this difference in PAE is mainly due to the fact that the UMS model was extracted from devices of technology iteration v3s, while the MMIC was fabricated using technology iteration v1s.

Furthermore, measurements showed a larger bandwidth than the one predicted by

the simulations. Both output power and especially PAE do not drop with the frequency as fast as it was predicted in the simulations. To illustrate this comparison, figures showing measured and simulated data during a frequency sweep with constant source available power will be used. This data corresponds to the operation point around where the optimal performance was measured.

The simulated PAE in Figure 3.24b p.43 was over 40% along 250 MHz, in the range 5.15-5.4 GHz, while the measurements in Figure 3.30 p.48 show that the PAE is over 50% along 550 MHz, in the range 4.85-5.4 GHz. Looking at output power while comparing Figures 3.24a p.43 and 3.31 p. 49, the simulation was showing that the power was in the range 46.25 dBm +/-0.25 dB between 5.1 and 5.5 GHz (along 400 MHz). Measurements show that output power is in the range 46.75 dBm +/- 0.25 dB between 4.85 and 5.3 GHz (along 450 MHz).

The increase of bandwidth observed during the measurements cannot be explained by looking at the responses affected by the spreads. Instead, I believe that there has been a trade off gain-bandwidth. The gain levels under high compression levels were smaller than forecasted, but the bandwidth was larger.

### 3.5 Conclusions and Future Work

The design process and measurements of a compact 50W GaN High Power Amplifier with PAE > 50% at C-band have been presented.

The results of the measurement campaign over the MMIC mounted over a CuMoCu carrier show that the  $S_{21}$  parameter presented a maximum at 5.4 GHz (22.6 dB) and the stability factor was always well above one. The measured small signal 3dB bandwidth is 1.1 GHz, centred at 5.4 GHz and corresponding to 20.4%.

Pulsed measurements provided excellent results, while the thermal effects were significantly degrading the performance under CW operation.

The maximum average power level measured under pulsed operation was 47.26 dBm (53.16 W, Gain=15.9 dB) at a frequency of 4.74 GHz. Similar values were obtained between 4.6 and 5.1 GHz. The maximum overall PAE measured using calibrated current sensors was 55.8% at 4.9 GHz (Pout= 47.19 dBm and Gain=17.51 dB). These maximum power levels and PAEs were measured when the device was working at compression points between 2.5 and 3 dB. The MMIC presented a satisfactory 0.5 dB bandwidth of 450 MHz, a 0.2 dB bandwidth of 300 MHz and a 0.1 dB bandwidth of 150 MHz.

Under CW operation, the maximum power level measured was only 41 dBm at a frequency of 5 GHz (PAE=24%, Gain=16 dB). Furthermore, the device was compressing at much lower source power levels than in the case of the pulsed measurements.

Comparisons between MMIC measurements and ADS HB simulations using a model provided by UMS have been presented, showing a relatively close agreement between them. The MMIC design center frequency has been shifted down and the measured PAE and output power are higher than in the simulations using the UMS model, while



the gain is lower.

UMS performed measurements over three devices without pushing the device into compression. Preliminary results show similar performance between devices. In future measurement campaigns it would however be very interesting to compare the performance between several devices at higher compression levels, in order to assess how the spreads are affecting the performance.

The C-band MMIC measurements that have been presented here represents state of the art results for a single MMIC chip as far as I know. It is not typical to find MMIC at these frequencies, since most of the reported power amplifiers at this frequency are hybrid based. The benefits of MMIC technology over hybrid for space applications are well known: a very compact footprint and increased reliability.

The amplifier fulfills the specifications regarding power ( $> 50W$ ), small signal gain (22.6dB) and efficiency ( $>40-50\%$ ). Wider bandwidths are also possible at the expense of footprint space and/or trade-off in maximum output power and efficiency. In the future, it could be interesting to increase the chip area available in order to improve the bandwidth of the input matching network.

Fulfilling the derated junction temperature for GaN technology in power amplifier applications is the main challenge for space applications. In this work, the calculated junction temperature is kept under 150 degrees for a reference baseplate temperature of 80 degrees. The capability of operation within the space radiation environment is being investigated, but previous tests performed for GaN indicate that radiation should not be a problem for this design [94],[95].

Overall an improvement of  $>15\%$  in PAE has been measured in comparison with a solution of four GaAs MMIC combined in parallel, while the output power levels are similar. Furthermore, the footprint size is around  $25mm^2$  both for the GaN design presented here and for the current Sentinel individual GaAs MMIC solution, thus leading to a considerable reduction in chip area by a factor of four or more if we consider the external power divider and combiners required to combine 4 GaAs MMIC chips.



# X-band Hybrid High Power Amplifier to Replace Vacuum Tubes in Ground Based Surveillance Radars

This chapter presents the design, assembly process and measurement campaign of 100W X-band hybrid high power amplifiers using GaN technology from Triquint. The motivation behind this project is in line with the efforts done at the Danish company Terma in order to replace the vacuum tubes in their ground based radars by solid state high power amplifier technology.

Outstanding results were obtained for a hybrid design using a power bar with 20 mm active area periphery. 94.5 W were measured under pulsed operation at 8.3 GHz and with a gain of around 7.6 dB. The power added efficiency obtained was >60%. The device was biased using  $I_{dd}=50$  mA. The device was working around 1 dB compression, and power levels on the order of 100 W and slightly higher are expected when testing it at higher compression levels with a more powerful driver.

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## 4.1 Motivation

Terma manufactures X-band radars operating at different frequencies between 8.85 to 9 GHz. The main civil applications covered by these radars are airport surveillance [96] and naval radars used for vessel traffic services and coast-guards [97]. Military applications are completely out of the scope.

The transmitters used in the current X-band radars at Terma contain vacuum tube based high power amplifiers, mainly travelling wave tubes. But they have started to commercialize radars with transmitters based on paralleling many GaAs solid state devices. As an example, one of their pulsed SSPA transmitters produces between 50-200 W average power, that is equivalent to 20-80 kW pulsed power using tubes.

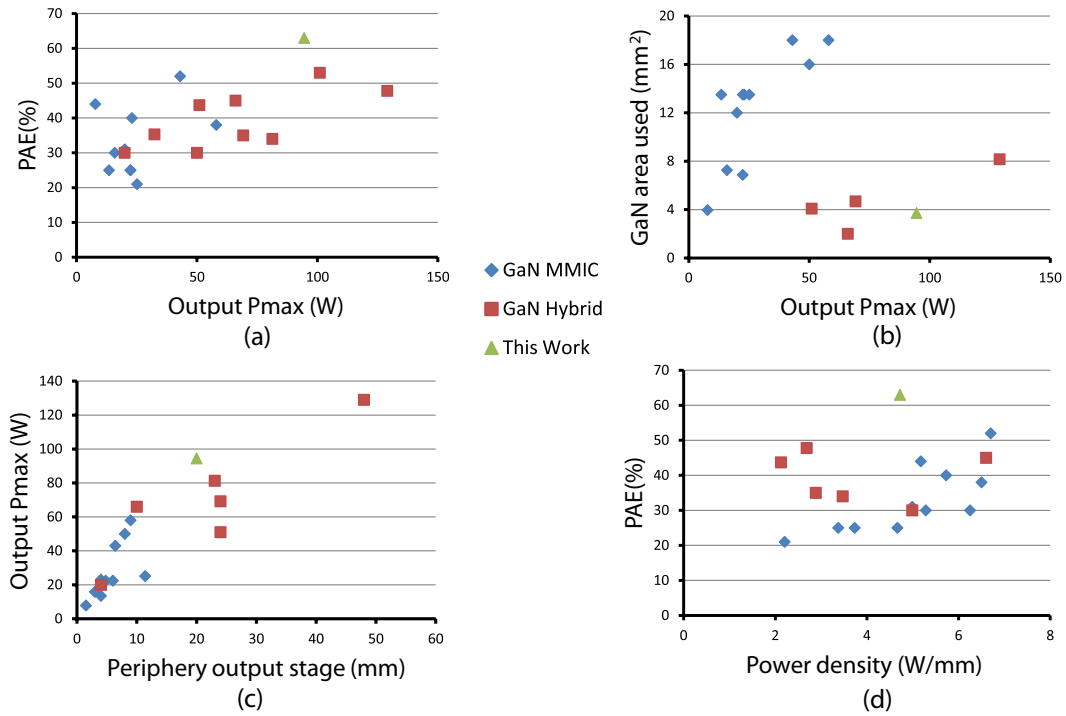
In comparison with solid state high power amplifiers, the tubes deliver higher peak power levels and they are currently more efficient, reaching PAE around 70% at X-band. But the main drawback for the tubes is their reliability and their large footprint and mass. Terma usually includes a back-up tube in their radars to increase the reliability of their radars. Linearity is also generally worse in tubes than in SSPAs, but this is irrelevant for the present application. The development of GaN solid state technology is creating interesting possibilities in the field of transmitters for pulsed radars, specially for phase array systems. GaN presents superior mean time between failure (MTBF) and occupies less area. The lower peak power levels can be compensated by increasing the average power levels by paralleling several modules. Furthermore, the reported efficiencies for GaN are approaching the levels obtained with the tubes, specially at frequencies under C-band.

The work presented here will demonstrate that GaN is already a serious candidate to be included in the future ground based radar transmitters at X-band.

## 4.2 State of the Art at X-band

In literature it is possible to identify two types of GaN Solid State High Power Amplifiers at X-band frequencies: the Hybrids and the MMICs. Figure 4.1 presents several graphics with the information extracted from more than 18 papers [40, 41, 48, 98–112]. The red squares represent the data from Hybrid designs, the blue diamonds the data from MMICs, and the green triangle corresponds to the results obtained within this work.

Figure 4.1a shows that the hybrid configurations held the power record at X-band, and both solutions have achieved power efficiencies ranging between 20% and 52%. The



**Figure 4.1** – Solid State High Power Amplifier state of the art at X-band (a) PAE (%) vs. maximum output power (W) (b) GaN substrate area used (mm<sup>2</sup>) vs. maximum output power (W) (c) maximum output power (W) vs. periphery of the output stage (mm) (d) PAE (%) vs. power density (W/mm).

hybrid power record is 129W and it has been reported by Toshiba [98], while the MMIC power record is 58W and it has been reported by Alcatel III-V Lab [99] as part of the European military project Korrigan [113] [114].

The hybrids have until now achieved higher power levels than the MMICs. Probably the foundries consider that nowadays it is not economically viable to build a GaN MMIC delivering power levels around 100 W and beyond, because of the large amount of GaN material required. It is important to highlight that to get around 50 W at X-band, an MMIC uses around 18 mm<sup>2</sup> [99], [110] of GaN material, while a hybrid uses only 4 mm<sup>2</sup> [98], as it can be observed in Figure 4.1b. Furthermore a very large MMIC would involve lower yields per processed wafer and also larger losses in the combining networks, since the GaN material is not optimal regarding losses. Apart from the extra material cost, the foundries would have to invest in research of passive components for the GaN process, such as resistors, capacitors and inductors, that are able to withstand the high voltages and current levels required for generating this power levels efficiently.

Figure 4.1c shows the maximum output power versus the total periphery of the output stage for hybrid and MMIC solutions. The total periphery is obtained adding all the gate widths of all the transistors used in the output stage. Larger peripheries have been used in the hybrids, thus obtaining larger power levels. This indicates that if

MMICs with larger peripheries are designed, power levels similar to the ones obtained with the hybrid solution can be achieved.

Figure 4.1d shows the power efficiency versus the power density, the former defined as the ratio of the maximum output power over the total periphery of the output stage. It is possible to observe that slightly higher power densities are achieved with MMIC solutions. This indicates that an MMIC uses the transistor area more efficiently.

All the reported X-band hybrids except [111] have only one stage. Multiple stage hybrid amplifiers require a more complex mechanical assembly process and a very careful design and modeling of the interstage matching network and the bondwire transitions. A two stage design would be very interesting in order to achieve a compact solution operating with high gain, but the work presented here was focused only in a single stage. Furthermore, in a two stage design the driver/booster ratio can be controlled to achieve higher overall efficiencies and larger bandwidths. The bandwidth is affected by the driver/booster ratio since the impedance transformation needed in the interstage matching network does influence the bandwidth [40]. On the other hand, the most part of the MMICs reported are a double stage design.

In the last years, some commercial Cree devices have appeared in the market [115], but their access often relies on an end user statement required by the International Traffic in Arms Regulations (ITAR), controlled by the USA government.

The work presented here is in line with the highest output power levels achieved at X-band. 100 W can be reached and slightly surpassed if a driver providing a little more input power is used, as it will be explained later. The PAE in this work is, to the best of my knowledge, higher than any other published for these power levels. I am convinced that the data presented here are correct, and the procedure for calculating the PAE has been reviewed in detail without finding any error. In order to fully verify these high efficiencies, it would be convenient to perform a new measurement campaign in the future, using different methods for measuring the currents consumed by the device. It is also fair to mention that this design covers the lower part of the X-band, while the most part of the designs published operate around 1 GHz above, between 9 and 10 GHz. This might explain to some extent the high efficiency achieved.

On the other hand, the GaN area and the 20 mm of periphery of the active area used here are in line with the published hybrids delivering similar power levels. But none of the published designs use a single power bar to get 100 W, instead they combine the power generated by two dies of 10 mm periphery each.

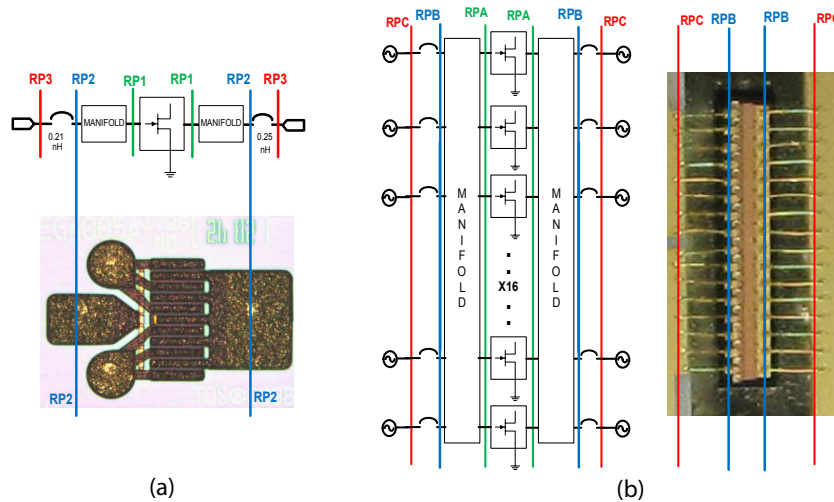
It is also possible to find publications presenting designs with several GaN high power modules in parallel using spatial combiners or low loss combiners. Structures delivering power levels up to 250 W have been reported at X-band, but higher power levels are possible if more modules are combined efficiently [116], [117].

### 4.3 Hybrid HPA Design Approach

This section will present the design process that was followed in order to get a 100 W X-band hybrid pulsed high power amplifier. The initial specifications required operation around 9.1 GHz and as much PAE and bandwidth as possible. An MMIC solution was discarded because of the prohibitive cost and the low yields per wafer due to the large active area required.

The GaN over Sic process from Triquint with 0.25  $\mu\text{m}$  gate length was selected among the very few available. This microstrip technology uses vias and the substrate is 100  $\mu\text{m}$  thick. It features field plate techniques optimizing the device to perform with high power added efficiency. It delivers power levels on the order of 5-7 W/mm, the transition frequency is  $f_t = 32$  GHz and the maximum frequency of oscillation  $f_{max} = 60$  GHz.

The smaller cell available is a discrete 1.25 mm HEMT with 10 gate fingers and 125  $\mu\text{m}$  gate width shown in Figure 4.2a. Dies with two, eight and sixteen cells in parallel were also available, corresponding to peripheries of 2.5 mm, 10 mm and 20 mm respectively.

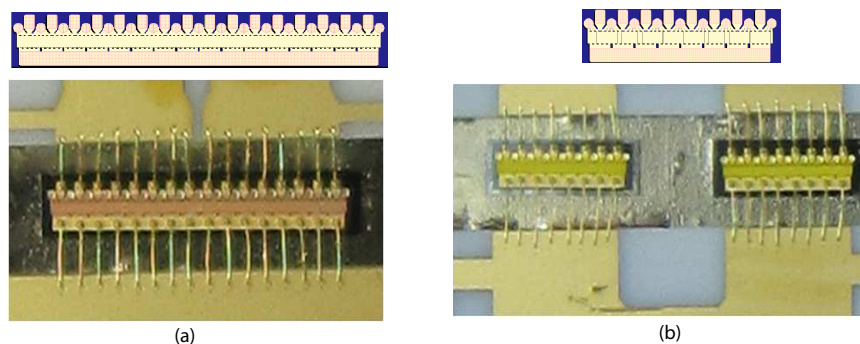


**Figure 4.2** – (a) Transistor single cell photo and model showing different referent planes (b) Power bar photo combining 16 single cells in parallel and model showing the different reference planes.

#### 4.3.1 Selection of Hybrid Topology

A single stage hybrid was selected as a first step. In order to get 100 W, it was possible to use a single 20 mm power bar with 16 single cells in parallel like the one shown in Figure 4.3a, or two 10 mm power bars with 8 single cells in parallel like the one shown in Figure 4.3b.

The final version of one of the hybrids manufactured using a single 20 mm power bar is presented in Figure 4.4. The device is comprised of a GaN power bar, alumina substrate, SMA connectors with miniaturized central pin, lumped resistors and capacitors, single layer capacitors and bondwires.



**Figure 4.3** – (a) 100 W 20 mm power bar. Dimensions 0.82 x 4.56 x 0.10 mm (b) Two 50 W 10 mm power bars in parallel. Dimensions 0.82 x 2.48 x 0.10 mm.

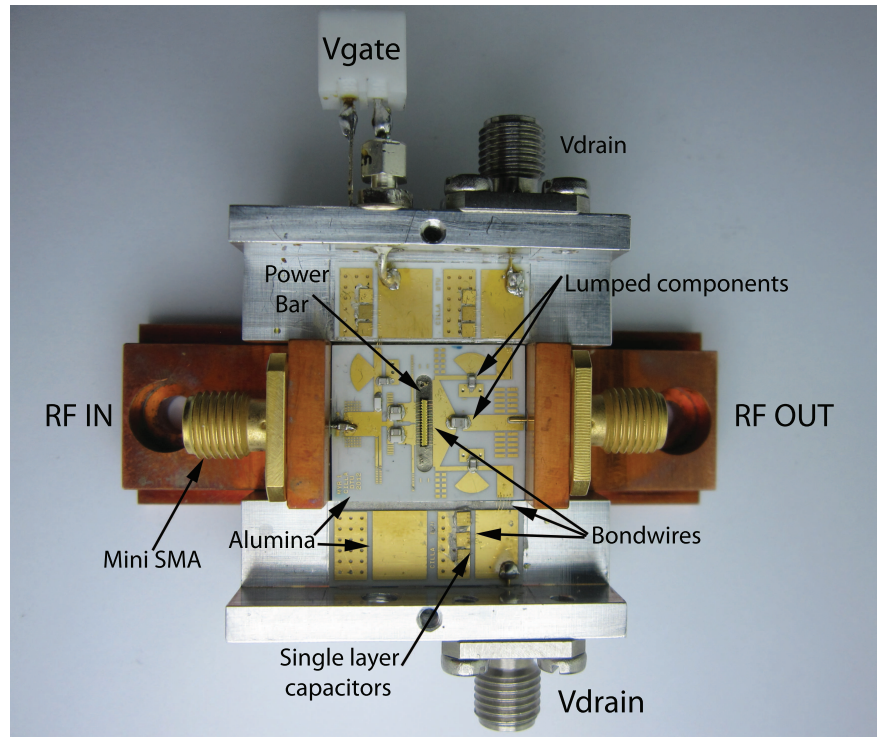
Alumina (99.6%) substrate was selected because:

- The expansion coefficient (8 ppm/C) matches well the one of the carrier and the GaN over SiC power bar. Mismatches between thermal coefficients can lead to failure in the bondwires and the eutectic attachment.
- It dissipates heat reasonably well. Its thermal conductivity is around 170 W/mK.
- Ceramic based substrates withstands the high temperatures required during the eutectic attach without expanding too much. Plastic based ones are not recommended.
- It has low tangent losses of  $2 \times 10^{-4}$ .

A compact solution was achieved by including the matching and biasing networks in the same print. The size of the center piece of alumina containing these networks is 18.5x15 mm. The permittivity of the substrate is around 9.8. Substrates with higher permittivity would allow a more compact solution, but they were not selected because of cost reasons. Aluminium Nitrate (AlN) material is also a good option. Its permittivity is 8.7 and its tangent losses  $5 \times 10^{-4}$ . It transports heat better than alumina but its expansion coefficient (4.6 ppm/C) does not match so well the carrier, and this is the reason why it was not selected here. The substrate thickness ( $254 \mu\text{m}$ ) was selected to match the thickness of the power bar as close as possible ( $100 \mu\text{m}$ ), while allowing it to synthesize wide enough 50 ohm lines capable of withstanding the required current levels.

According to [54], in CW applications the power handling of a microstrip lines depends on its losses, while for pulsed applications it normally depends on the breakdown





**Figure 4.4** – Fabricated hybrid X-band HPA

voltage of the substrate material. In our case, the power handling is not a problem, but we want to minimize losses in the lines. The trace resistance increases as the trace geometry gets smaller. Therefore, the thickness of the gold metallization layer over the alumina was selected to be  $5 \mu\text{m}$ , fulfilling the rule of thumb that advises to allocate around five times the skin depth of gold at the operating frequency ( $0.7 \mu\text{m}$ ).

The custom-made enclosure is made of copper and aluminium. Its dimensions were selected to avoid resonance at the operating frequency. It is not a commercial hermetic package, since their parasitics are typically more pronounced at this frequency and they would have hindered the performance due to extra losses. The number of transitions along the RF path is minimized with the present solution. We have the bondwire array transition from the power bar to the alumina substrate and the transition from the alumina substrate to the SMA connector with miniaturized central pin. Some publications can be found on GaN packaging [118], but more efforts have to be done in finding new packaging solutions for devices at high frequencies.

The differences in performance can be significant when mounting the die over different carrier materials, especially when operating under CW or with long pulses. The carriers used here guarantee a proper assembly of the GaN power bar, allowing good thermal dissipation and matching the expansion coefficient of the GaN over SiC power bar well. The majority of the devices were using a copper molybdenum-based carrier (CuMoCu) that presents thermal conductivity between 220-340 W/mK and coefficient

of Thermal Expansion of 8 ppm/K. But a few power bars were also mounted over state of the art Aluminium diamond-based (AID) carrier materials. Aluminium diamond has better thermal conductivity (500 W/mK) and a coefficient of Thermal Expansion of 7.5 ppm/K. More information about this new diamond based carrier materials can be found in [119–121].

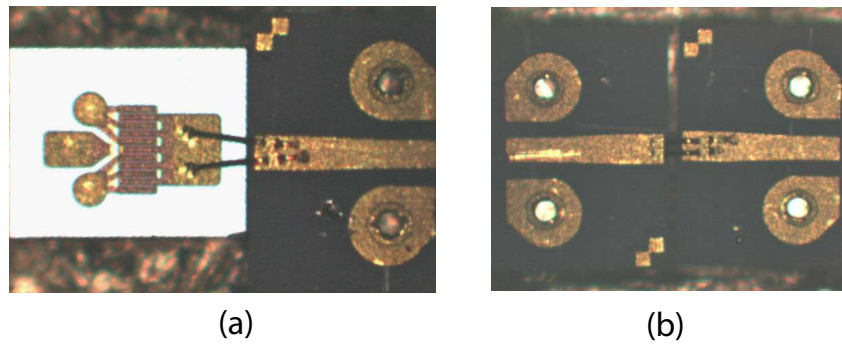
Lumped capacitors and resistors were used as part of the matching network. Tantalum thin film resistors and printed capacitors over the alumina substrate would have helped to control the spreads. They were, however, not selected here because they would not have withstood the high current levels and peak voltages required. Furthermore, they would have increased the bill of materials (BOM) considerably.

### 4.3.2 Technology Assessment

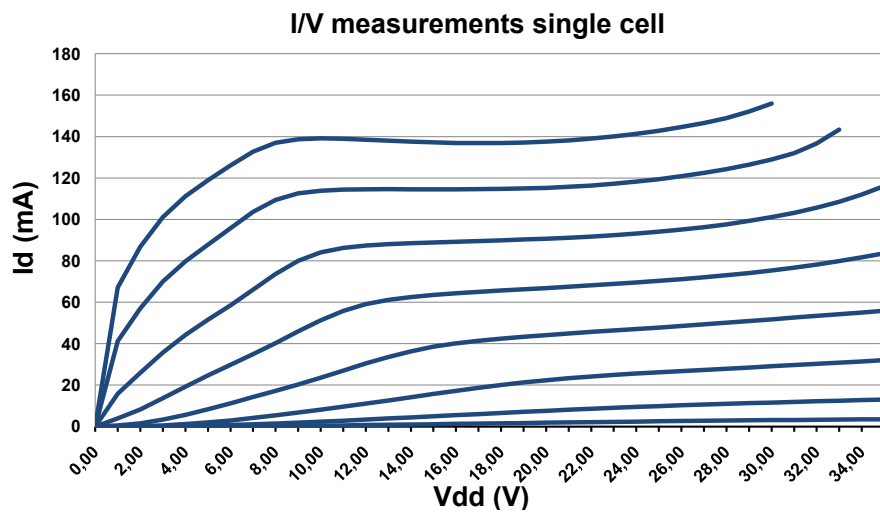
A preliminary evaluation of the technology was performed, as well as a load pull measurement campaign with the intention of validating the model and selecting the optimal load impedances. A 1.25 mm single transistor cell attached to a carrier using solder preform was tested. Figure 4.5a presents a photo of the single cell attached to a carrier. The drain of the transistor is bonded to a small fixture that allows GSG probe testing. Figure 4.5b shows a fabricated structure including two small fixtures back-to-back. This structure was used to de-embed the effect of the fixture from the measurements.

High power levels of around 7 W were measured. This corresponds to power density of 5.6 W/mm. Load pull equipment was only available up to 12 GHz. Therefore, it was not possible to guarantee that the 2<sup>nd</sup> and 3<sup>rd</sup> harmonics were properly calibrated. Manual load pull was performed by using initial impedances obtained from simulations. Important variations in output power and efficiency were observed while changing the fundamental load. Unfortunately, the cell was burnt before load pull data could be saved. It is very probable that the cell burnt because of problems dissipating heat while pushing it into hard compression. There might have been an air bubble under the die that was reducing the thermal conductivity of the sandwiched structure. Moreover, the tip of the probe was damaged and the lack of time prevented a new campaign. The model was not validated, and the optimum load and source impedances had to be found using load pull simulations.

Figure 4.6 presents the DC measurements of the I/V characteristic curves of a 1.25 mm single transistor cell. These were the only measurements that were stored before the device was destroyed. DC simulated data is shown in Figure 4.24e. The main difference between measurements and simulations is that the model does not include degradation of performance when the power dissipated increases. Furthermore, the snapback current effect is observed in the measurements for V<sub>ds</sub> levels of around 30 V, while the model presents this effect for much larger voltage levels.



**Figure 4.5** – (a) Transistor single cell with microstrip fixture bonded at the output (b) Structure built to de-embed the effect of the microstrip fixture from the measurements



**Figure 4.6** – Measured DC I/V characteristic curves of 1.25 mm single transistor cell

### 4.3.3 First Simulations for the Selection of the Operation Mode and Loading Conditions

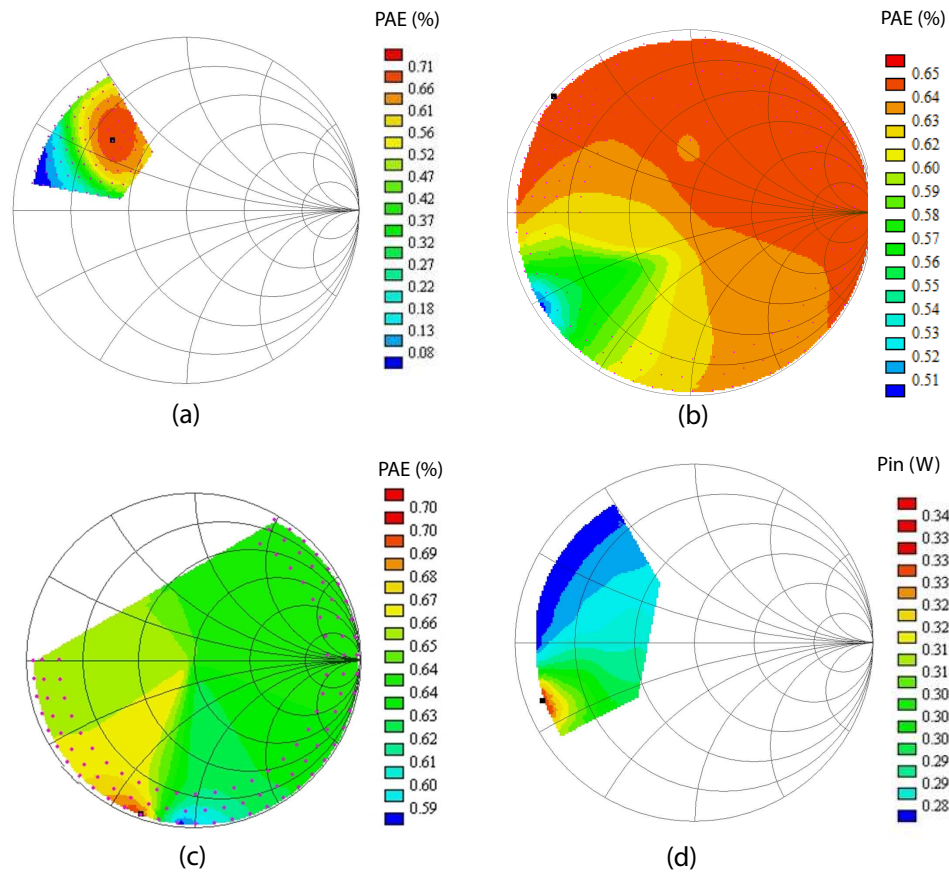
Simulations using ADS were performed using a nonlinear model provided by the foundry. The DC drain voltage for the model is valid only between 28 V and 32 V. The graph in Figure 4.2a shows that the model for a single cell includes a HEMT model from ADS library and manifold structures represented by 2 port S-parameter files. Furthermore, two small bondwires were added to the simulation. The model for the power bar is presented in Figure 4.2b. It comprises 16 HEMT single cell blocks in parallel combined by manifolds represented by 32 port S-parameter files. Via hole models are also included. The model does not include the effects of heat spread between neighbouring cells. Figure 4.2 also presents different reference planes for the models.

Load pull simulations were performed in order to select the optimal impedances for the design. Figure 4.7 presents load pull simulations for the 1.25 mm single cell including the bondwires. The simulations were performed at  $f_0 = 9$  GHz, constant 3dB compression point,  $V_{dd} = 30$  V and  $I_{dd} = 35$  mA. Figure 4.7a shows the PAE contours when the fundamental load impedance is load pulled and the 2<sup>nd</sup> and 3<sup>rd</sup> harmonics are fixed to get optimal PAE. Figures 4.7b and c show PAE contours when the 2<sup>nd</sup> and 3<sup>rd</sup> harmonics are respectively load pulled and the fundamental impedance is close to the optimal one proving maximum PAE. Figure 4.7d shows the power inserted into the transistor for different source loading impedances. The red area indicates the impedances that present better input matching.

Figures 4.8a to e show simulated data for the single cell using Harmonic Balance in ADS and loading conditions to obtain maximum PAE at 9 GHz. Figure 4.8a shows that the maximum PAE simulated was around 72.8%, when the device was delivering power levels of 5.9 W (4.72 W/mm) and the transducer gain was 11.79 dB. The current and voltage waveforms at the intrinsic terminals of the transistor are shown in Figure 4.8c. The waveforms are also plotted in Figure 4.8c as loadlines over the DC  $V_d$ - $I_d$  characteristic curves. It is important to highlight that these high efficiencies are obtained because the transistor is operated in switching mode. In this way, the overlapping between current and voltage waveforms at the intrinsic plane is avoided as much as possible. Figure 4.8b shows a frequency sweep containing data obtained at 3dB compression point. The output power and PAE does not peak at the same frequency. This is typical in high power amplifiers. A 0.2 dB bandwidth of 1 GHz was simulated with output power between 37.7 +/- 0.1 dB and PAE above 55%.

The Rollets stability factor obtained during the small signal stability analysis is presented in Figure 4.8e. The K factor is under 1 at frequencies under 7 GHz. This is to a large extent due to the huge gain of the device at low frequencies. The stability circles were also analyzed and techniques to stabilize the device by reducing the gain at low frequencies will be presented later.

Simulations of the 16 cells power bar were also performed using a schematic model like the one presented in Figure 4.2b. Each gate port of the power bar was fed in phase

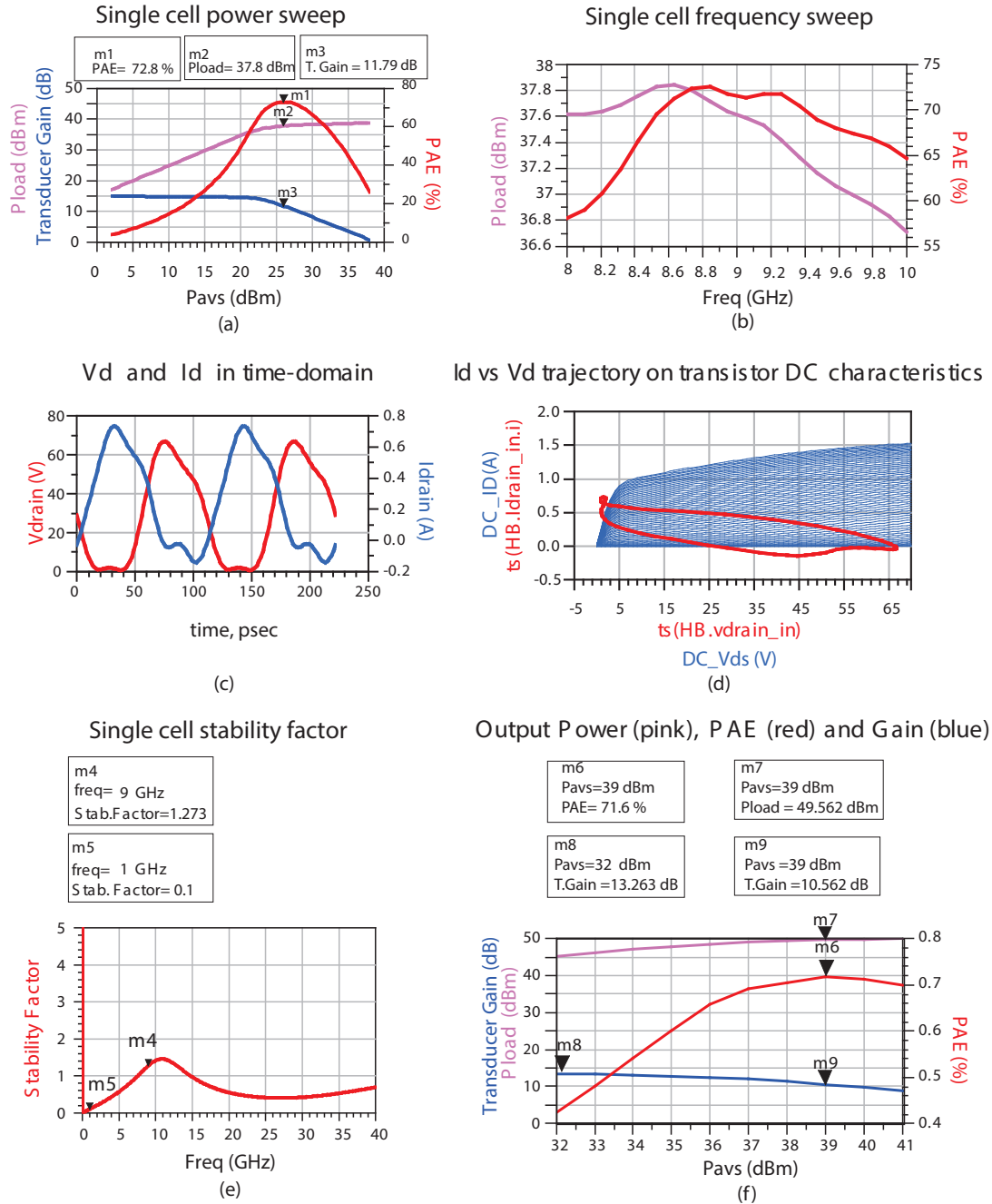


**Figure 4.7** – Load pull simulations for a single 1.25 mm cell at 3dB compression,  $V_{dd}=30$  V,  $I_{dd}=35$  mA. Simulations include the effect of two bondwires. (a) PAE fundamental load pull at 9 GHz when harmonics are loaded to get optimal PAE (b) PAE second harmonic load pull at  $2f_0$  (c) PAE third harmonic load pull at  $3f_0$  (d) Power inserted into the transistor during a source load pull at  $f_0$

and the output power was collected over 16 loads. This simulation helped to conclude that the effect of the manifold structure was not a problem at this frequency. Figure 4.8f presents a power sweep for the power bar at 9 GHz and using loading conditions providing optimal PAE performance. The maximum PAE simulated was around 71.6%, when the device was delivering power levels of 49.56 dB. These simulations indicated that a 100 W high power amplifier was possible using the 20 mm power bar.

#### 4.3.4 Analysis of Bondwire Arrays, Transitions and Passive Components

A careful evaluation of the bondwire arrays, lumped components and transitions included in the design was undergone.



**Figure 4.8** – (a) Power sweep for a single cell at 9 GHz. (b) Frequency sweep for a single cell at constant 3 dB compression point (c) Current and voltage waveforms at the intrinsic plane of the single cell during a power sweep. (d) Loadline of the single cell overlapped with the DC I/V curves (e) Simulated Rollets stability factor for a single cell (f) Power sweep for the full power bar using the manifold structures.

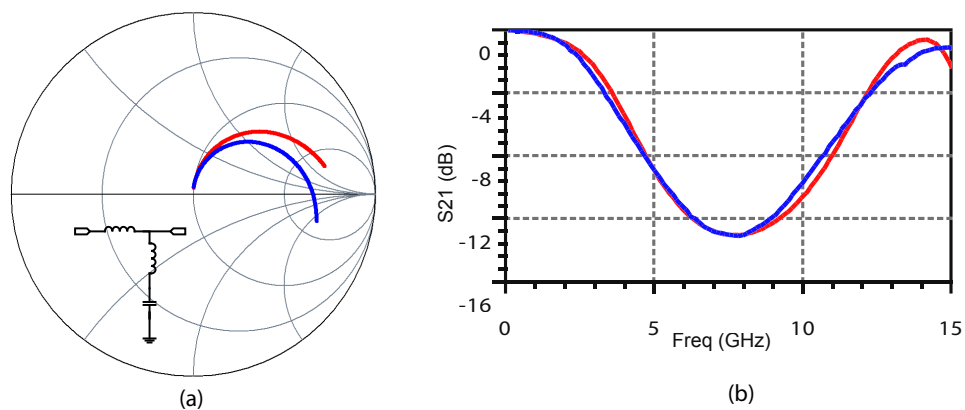
#### 4.3.4.1 Bondwire Arrays

Bondwire arrays are extensively used in electronic packaging and to interconnect microwave components. An example of this is the electrical connection provided in the design presented here between the power bar die and the external matching structures. Large arrays using many bondwires in parallel are usually found in the large single tabs of the output ports of transistor power bars. The number of bondwires in parallel and the radius are chosen to properly accommodate the current at the output power stage and avoid electromigration. The table in [122] presents the typical fusing current for a bondwire depending on its diameter and material. The equations used to build the table can be found in [123]. Gold bondwires with a diameter of  $50\ \mu\text{m}$  were selected for this work.

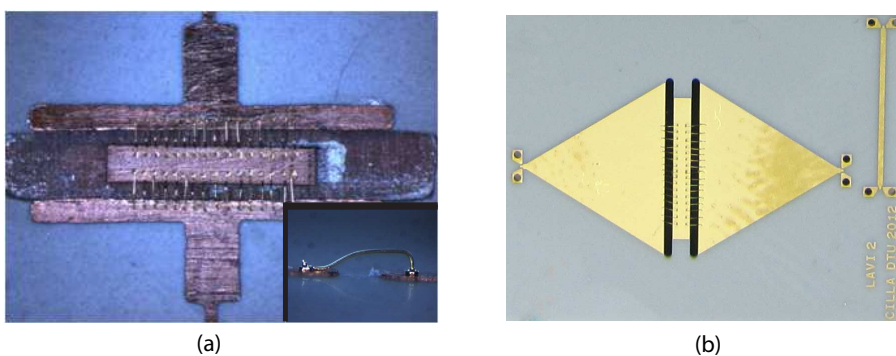
Hybrid design above C-band requires a good model of the bondwires and their transition, in order to achieve a proper matching and to avoid the need of tuning after manufacturing, if even possible. Previous research has focused on closed-form equations used to compute self and mutual inductances of the bondwire arrays [124–128]. Full wave software simulations of single and multiple bondwires have also been published [129–131].

Traditionally, at low frequencies, the bondwire is considered to have an inductive behavior, and it is a good principle to keep it as short as possible. The rule of thumb says that a single bondwire presents an inductance of around  $0.6\ \text{nH/mm}$ . The ADS bondwire array model [126] is based on self and mutual inductance calculations, modeling each bondwire with five segments of a given radius, conductivity, distance from ground plane and separation between adjacent bondwires. At higher frequencies, however, the bondwire-to-microstrip transition becomes significant, and the behavior depends on the permittivity and thickness of the substrate used, the bondwire-to-microstrip connection angle and the distance from the connection point to the substrate edge. Figure 4.9a shows a comparison up to  $32\ \text{GHz}$  of a single bondwire simulation using the inductor-based ADS model and a simulation using 3D full wave electromagnetic simulation software. Both models match up to around  $6\ \text{GHz}$ , but not at higher frequencies. In Figure 4.9a, a lumped equivalent of the bondwire-to-microstrip transition can be added to the ADS model in order to fit both curves.

Figure 4.10 shows photos of the 16 bondwire array structure that has been fabricated to validate simulations, while Figure 4.11 presents the CAD 3D model used to simulate the structures with the finite elements method (FEM) in HFSS. A microstrip step impedance transformer was used as a test fixture. Structures were fabricated with both miniature coaxial connectors and GSG pads for probes. HFSS lumped ports were used because they only excite one mode in the structure, while wave ports would excite several modes. Figure 4.9b shows good agreement between measurements and simulations of the array up to  $15\ \text{GHz}$ . The behavior was also validated using CST software, based on the finite-difference time-domain method (FDTD). A good matching between simulation and measurements was also observed for single bondwires.



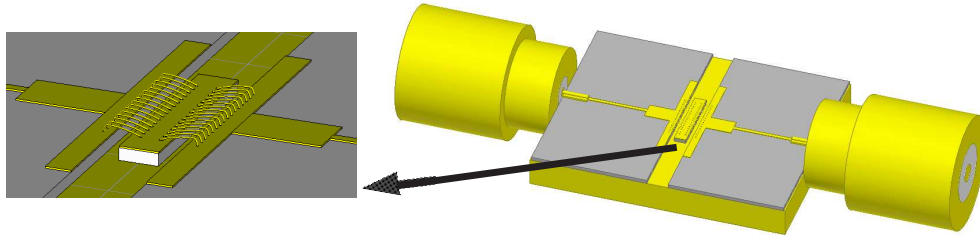
**Figure 4.9** – (a) Single bondwire  $S_{11}$  parameter using ADS inductance-based model (Red) and full wave 3D simulation (Blue) from 1 to 32 GHz. The graph also shows the lumped equivalent model of the bondwire-to-microstrip transition, which added to the ADS model, would make both curves to match. (b) Comparison between measurement (blue) and full wave electromagnetic simulation (red) of fabricated structure.



**Figure 4.10** – Fabricated bondwire arrays to validate the CAD simulations and the assembly process.



When paralleling bondwires, the overall parasitic inductance is reduced, while the capacitance to ground increases, relative to a single bondwire, due to the paralleling. This makes the full wave 3D modeling even more necessary than in the case of a single bondwire. 3D EM CAD programs like HFSS or CST are efficient, considering the computers available nowadays.

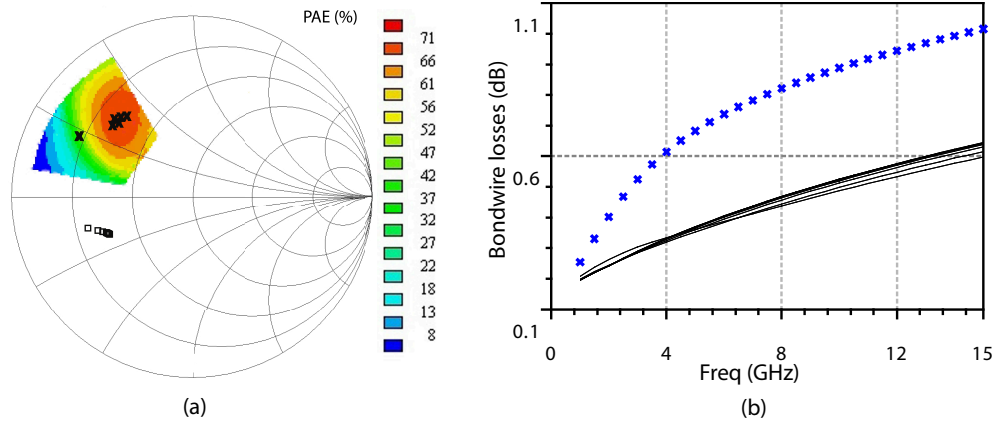


**Figure 4.11** – 3D CAD model for the bondwire array and fixture, including transition from microstrip to coaxial connector.

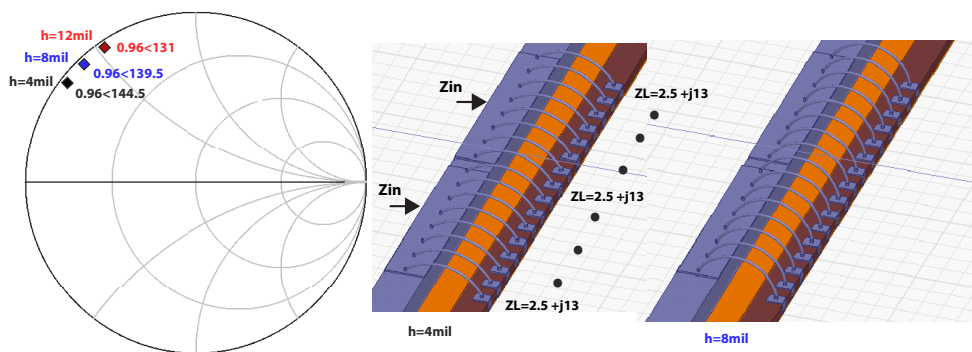
The process of designing a hybrid power amplifier using multi-transistor power bars can be greatly improved by the use of the accurate models available nowadays, both for the active and passive elements. Figure 4.12a shows the Power Added Efficiency (PAE) contours for the transistor cell operating at 9 GHz, where the red area corresponds to the optimal performance in terms of PAE. A multiport bondwire array model obtained with a full wave solver facilitates the simulation of the impedance that each of the cells of the array is loaded with at their drains. The crosses in Figure 4.12a represent the output impedances seen by the individual transistors of a 16 cell power bar at 9 GHz when using the full-wave array model during the matching network design process. The squares represent the impedances seen when the full-wave array model is substituted by an inductor based one. When looking at the PAE corresponding to both cases, we can conclude that the use of a non accurate model can completely detune the performance of the hybrid design.

Another example that confirms the importance of modelling the bondwire array properly can be observed in Figure 4.13. The Smith Chart presents simulations of the different input impedance levels seen at the tabs located at the left side of the array structures. Different bondwire heights between the ground plane and the higher part of the bondwire were simulated. The small ports on the right side of the array structures correspond to the gate of the single cell transistors. For this particular case, and based on simulations, we assumed that the transistor input impedance was  $Z_L = 2.5 + j13$ . The simulations confirm that small changes in the height of the bondwires over the ground plane involve large detuning of the matching circuits. When paralleling many cells in a power bar, the impedances to match are typically very low. Therefore, only narrowband designs are often possible, and it is necessary to design the matching networks, including an accurate bondwire array model.

There also are imbalances in the synthesized impedance along the different ports



**Figure 4.12** – (a) Load pull data for a single transistor cell showing PAE circles at 9 GHz and synthesized impedances for each one of the 16 cells of a power bar, using the bondwire full wave model (crosses) and the inductor-based model (squares) (b) Losses along the two bondwires at the edges of the array in blue (crosses) and for the other 14 bondwires in black.



**Figure 4.13** – Different input impedances seen at the tab in the alumina substrate for different distances between the ground plane and the bondwires. The small ports on the right side of the structure are loaded with  $Z_L = 2.5 + j13$

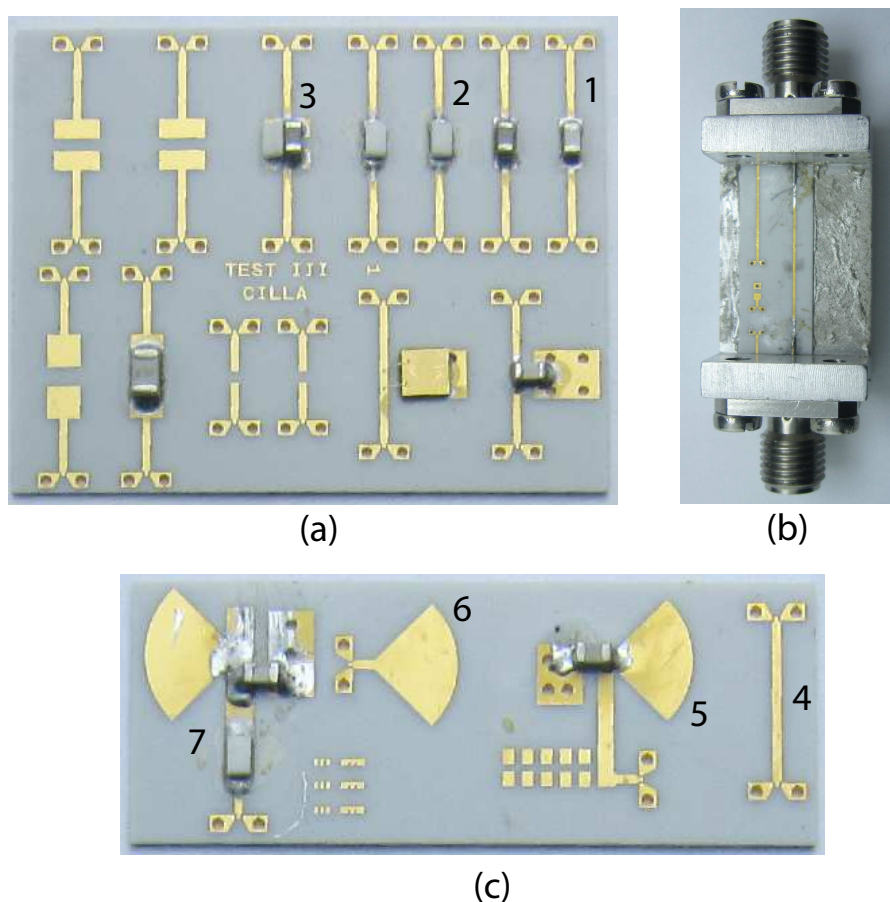
of the bondwire array, partially because of the fact that the two bondwires on the edges of an array only have one neighboring bondwire instead of two. This modifies the magnetic and electric fields along the array, and therefore, the couplings and losses between the different bondwires will also vary along the array. The bondwire losses will also depend on the loading impedance levels, when compared to the equivalent characteristic impedance of the bondwire [126]. Figure 4.12b corresponds to a simulation showing the variation of the insertion losses along the different bondwires of an array used at the gate of a 16 cell hybrid power transistor. At the gate, these variations in loss-levels will create differences in the operating compression point of each of the individual cells. At the drain, the differences in synthesized impedance for each of the cells will create differences in performance between the cells. These differences in performance between the cells will add to other imbalances created, for instance, because of the temperature gradient along the bar. The latter imbalances might be dominant, but it was not possible to verify it because of the lack of an electrothermal coupled model.

#### 4.3.4.2 Lumped Passive Components and Transitions

Measurements of the lumped components, connectors and transitions used in the designs were performed. Some of the test structures fabricated are shown in Figure 4.14. These measurements were very useful to select the final values of the components to be used in the design.

A small test fixture with the coaxial SMA to microstrip transition was fabricated as shown in Figure 4.14b. The printed line was designed with 50 Ohm characteristic impedance. Figure 4.15a presents the measured  $S_{21}$  and  $S_{11}$  of this structure. Insertion losses of 0.35 dB and return losses larger than -15 dB were measured at 9.1 GHz. The 50 Ohm line tagged with the number 4 in Figure 4.14c was measured using GSG probes. Figure 4.15b shows very small insertion losses of 0.059 dB and return losses larger than -30 dB at 9.12 GHz. These measurements certify the suitability of the transition at this frequency, the accuracy in the fabrication of the printed lines and the permittivity of the substrate.

Lumped capacitors with resonance at the centre design frequency were used in the biasing networks and as DC blocks. Measurements were taken with the probe station, and the reference planes were corrected afterwards and placed at the edge of the printed line where the lumped component is soldered. In Figure 4.15c it is shown how by looking at the  $ABCD_{12}$  of a lumped component in series, we can obtain the series impedance  $Z$ . Figure 4.15d presents in red measurements of the the  $ABCD_{12}$  parameter of the 0.9 pF series capacitor tagged with number 1 in Figure 4.14a. The frequency of resonance of the capacitor is 9.1 GHz. This data are in strong disagreement with the data provided by the manufacturer. The datasheet indicated that a 1.6 pF capacitor was instead resonating at this frequency. This demonstrates that the RF behaviour of lumped components is very dependent on the thickness and permittivity of the substrate they are mounted over, and also on whether they have other lumped components placed behind. This is

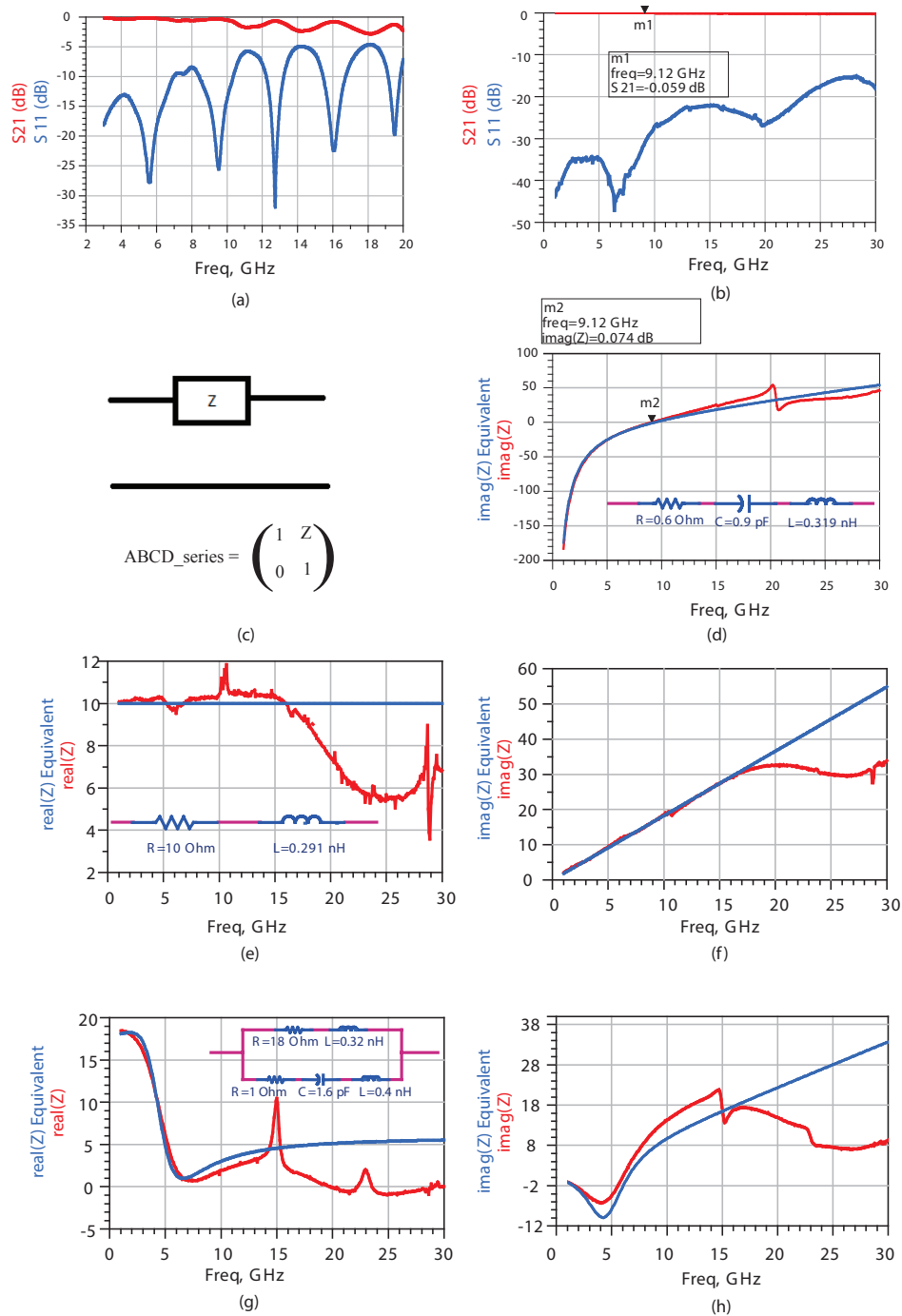


**Figure 4.14** – (a) Alumina print for characterization of resistors and capacitors used during the design. (b) Small fixture including a 50 Ohm line and coaxial-to-microstrip transitions. (c) Alumina print including biasing networks used in the designs.

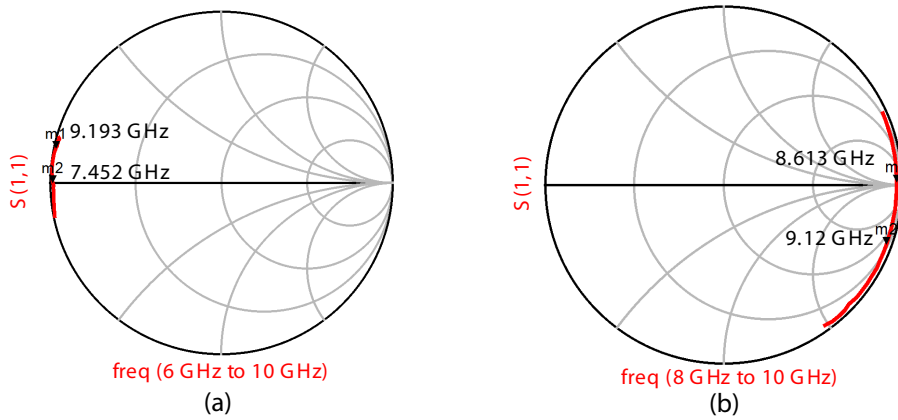
particularly noticeable at high frequencies. The blue curve in Figure 4.15d corresponds to the response of an equivalent lumped network also shown in the same Figure. This equivalent model was used afterwards in the simulations of the High power amplifier.

The capacitor physical size is selected in order to withstand the power and current levels involved in the design. The maximum current that a capacitor in series can withstand is determined by the power that it can dissipate, as it is shown in [132]. The series DC block capacitor size used at the input matching network is 0402. A bigger capacitor with size 0608 is used as DC block at the output matching network. Single layer capacitors shown in 4.14a were also analyzed.

High frequency resistors were used at the input matching network. The red curve in Figures 4.15e and f shows the measurements of the real and imaginary part of the impedance of a 10 Ohm resistor tagged with 2 in Figure 4.14a. The blue curve corresponds to the simulated response using the lumped equivalent model shown also in Figure 4.15e. The measurements confirm that the resistor is suitable for applications



**Figure 4.15** – (a) Measured  $S_{21}$  and  $S_{11}$  of the fixture shown in Figure 4.14b. (b) Measured  $S_{21}$  and  $S_{11}$  a printed 50 Ohm line. (c) Relationship between ABCD parameters and impedance for a component in series. (d) Measured imaginary part of the impedance of a 0.9 pF series capacitor (e) Measured real part of the impedance of a 10 Ohm series resistor. (f) Measured imaginary part of the impedance of a 10 Ohm series resistor. (g) Measured real part of the impedance of an 18 Ohm series resistor in parallel with a 1.6 pF capacitor. (h) Measured imaginary part of the impedance of an 18 Ohm series resistor in parallel with a 1.6 pF capacitor.



**Figure 4.16** – (a) Measured  $S_{11}$  of the radial stub tagged with 6 in Figure 4.14c. (b) Measured  $S_{11}$  of the biasing network tagged with 5 in Figure 4.14c.

at X-band.

High frequency pass parallel networks of lumped capacitors and resistors were used in series at the gate of the transistors, in order to control the high gain at low frequencies, thus improving the stability. The series impedance introduced by the structure is high at low frequencies, and very low at the operational frequency. The component tagged with 3 in Figure 4.14a shows an RC structure using a capacitor of 1.6 pF and a 18 Ohm resistor. A measurement of the real part of the impedance is shown in red in Figure 4.15g. A measurement of the imaginary part of the series impedance is shown in red in Figure 4.15h. In the same figures, the blue curve represents the data obtained from an equivalent lumped component model.

The biasing networks were also tested separately. Radial stubs like the one tagged with 6 in Figure 4.14c were used. Figure 4.16a shows a measurement of this radial stub. The impedance is very low at our design frequency. Equations describing this stubs can be found in [133–135]. The biasing network used at the output matching network is tagged with 5 in Figure 4.14. It includes a radial stub, a parallel capacitor resonating at 9.1 GHz and a quarter wave transformer. Figure 4.16b shows measurements for this structure. The quarter wave transformer converts the low impedances into high impedances at 9.1 GHz. This results in small leakages of RF power through the biasing networks.

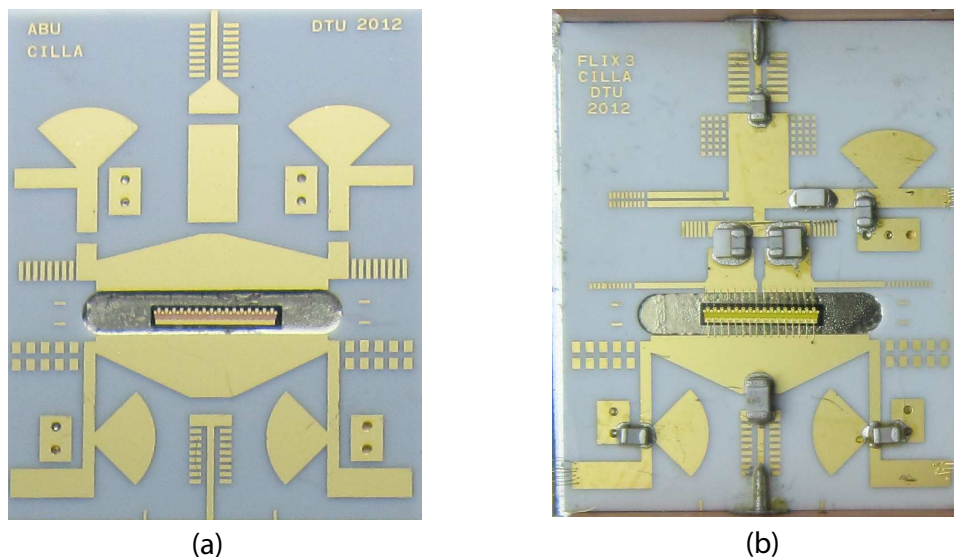
### 4.3.5 Matching Network Design and Full Hybrid HB Simulations

Once the lumped components, bondwire arrays and transitions had been fully characterized, the next step was to use their models combined with microstrip structures to create the matching networks. Three different designs using a single 20 mm power bar will be presented first. Afterwards, a design using two 10 mm power bars in parallel will be addressed.

#### 4.3.5.1 Designs Using a Single 20 mm Power Bar

The 20 mm power bar used was presented in Figure 4.3a. At the beginning of the design stage, the first issue that had to be addressed was whether such a long power bar could operate at X-band without oscillating. The cells along the power bar were driven with phase differences mainly due to the physical distance between them. Taking into account the permittivity of the SiC substrate, the larger phase difference between the two cells at the edges of the power bar was 122.5 degrees at 9.1 GHz. This is a significant fraction of the wavelength. The difference in phase was hindering the gain and output power obtained from the bar because the power that each cell contributed was not combined in phase. Furthermore, the gradients of temperature along the bar and the differences in the insertion losses of each of the bondwires along the array were also contributing to differences in the operation between cells. At frequencies under 5 GHz, the hybrid designs are very common, and since the wavelength is large, long power bars can be used without having too many problems with the phase differences between the cells. Actually, the temperature of operation is usually the factor limiting the size of the power bar at low frequencies under 1 GHz. But at higher frequencies, both the phase differences and thermal dissipation are important when selecting the size of the device to be used.

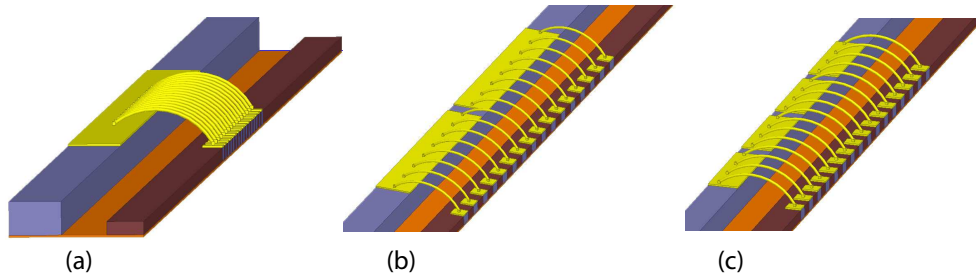
It is possible to find a few publications on design of combining networks for high power amplifiers. Reference [136] classifies the type of combining networks depending on its loss, size, frequency bandwidth, bias compatibility, and effects over stability.



**Figure 4.17** – (a) Hybrid design ABU combining 16 cells in a single microstrip tab at the input matching network. The design was never fully assembled due to failure during die attach. (b) Hybrid design FLIX3 combining 8 cells in each of the two microstrip tabs at the input matching network. The photo shows the device fully assembled and ready for testing.

Looking at the drain of the bar in Figure 4.3a, it can be observed that a so called "bus-bar combining structure" has been adopted by the foundry. The drains of the 16 cells of the device are combined together at a single wide bus-bar. The design of a bus-bar combiner and its analysis can be found in [137]. This publication states that the intermediate point between two cells of the bar can be seen as a "virtual open circuit" under the following requirements: the separation between cells is small compared with the wavelength and the cells are driven without large phase differences at the gate. This guarantees that no signal is running between the cells. According to [138], this structure contributes positively to avoiding odd-mode oscillations in power bars. On the contrary, on the gate side, each of the cells has its own small pad, and they can be driven individually. The cells also have 14 Ohm resistors between the gates, in order to avoid odd-mode oscillations.

To implement the matching networks, it was decided to use impedance transforming networks based on lumped and distributed elements. Figure 4.17 shows two of the three different layout designs that were fabricated using a single 20 mm power bar. The third design is shown in Figure 4.31a. The output matching network is shown at the bottom of the photos. Since all the 16 cells were combined in a bus-bar, it was relatively easy to select the configuration of the output matching network. In all the designs a broad single microstrip line is used. Paralleled bondwires connected the bus-bar in the GaN power bar and the broad tab printed over alumina. There was room for more bondwires, but it was found that 16 were enough to withstand the expected currents levels.



**Figure 4.18** – Simulated bondwire array in HFSS combining in the same tab (a) 16 transistor gates (b) 8 transistor gates (c) 4 transistor gates.

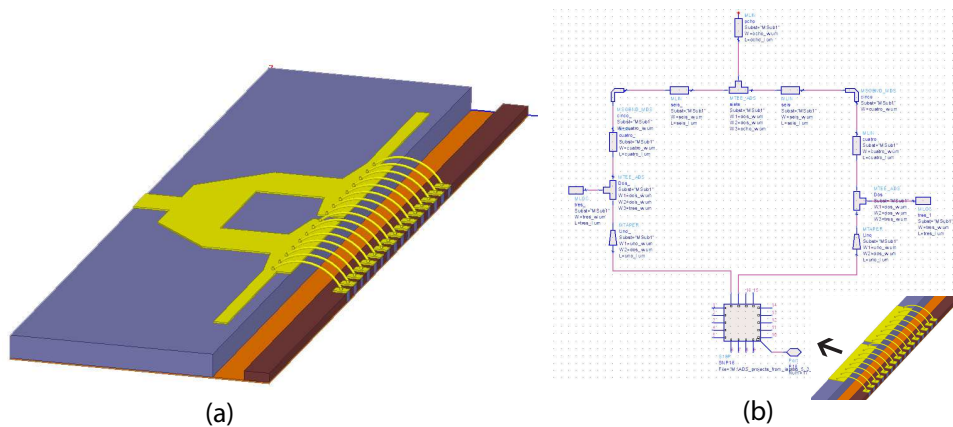
On the gate side of the power bar, it was not so straightforward to select the configuration of the matching network. If each cell had to be driven individually at the gate, a complicated network with 16 branches was required. The line width of each of the lines in the branches should be narrow because of physical constraints. The high characteristic impedance of these lines was making it difficult to match the low input impedance at the gate, and the design was becoming impractical. In order to simplify the structure, an investigation of the effect of combining several cells at the gate in parallel was performed.

Simulations were ran using HFSS for the structures shown in Figure 4.18 combining 4, 8 and 16 cells in the same tab. They were simulated from 0.01 to 32 GHz with a



100 MHz step. The accuracy achieved with HFSS simulations was demonstrated before, with the example of the bondwire array that was discussed in section 4.3.4.1. The design named "ABU" and shown in Figure 4.17a combines the gate of the 16 transistors in a single tab. The designs named "FLIX" and "MYR" combine the gate of 8 cells in two different tabs. Photos are shown in Figures 4.17b and 4.31a respectively. Designs combining 4 transistor gates using the structure in Figure 4.18c were not fabricated. The simulations demonstrated that at this frequency and for this power bar, using four tabs was not convenient. The layout was becoming too complicated and there was not a great deal of physical space available. The only advantage was the possibility of increasing the bandwidth at the expense of increasing considerably the footprint.

Simulations of larger structures including the bondwire array and the microstrip combining structures build over the alumina substrate were also performed. One example is shown in Figure 4.19a. The HFSS simulation of this structure was compared with a simulation in ADS. The ADS simulations included microstrip lines from the MLIN library and a multi-port S-parameter file corresponding to the simulated bondwire array shown in Figure 4.18b. The agreement between both simulations was acceptable, and only a 300 MHz shift in frequency was found. Therefore, most of the matching networks were designed in ADS including S-parameter files from HFSS. Simulations in ADS were much faster, and tuning was much easier. This allowed reducing the complexity of the design process considerably.

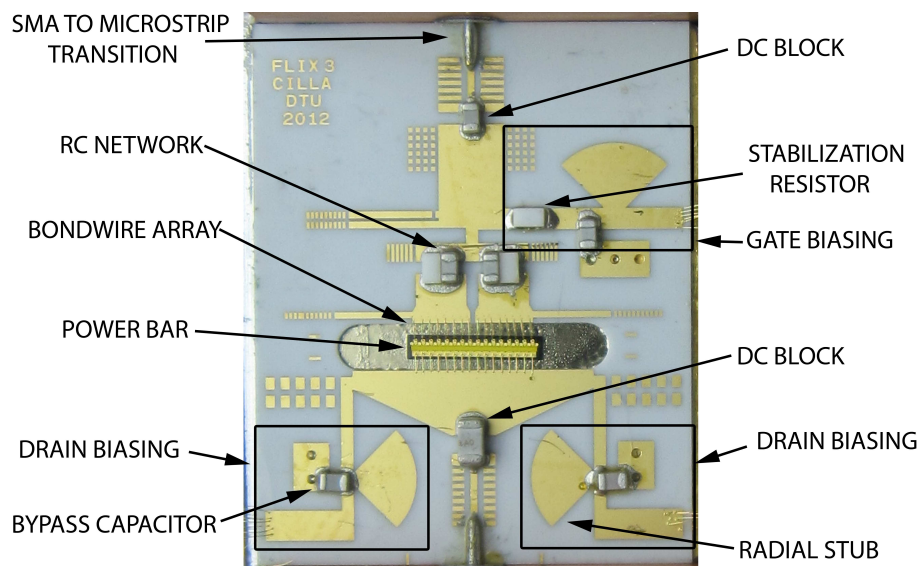


**Figure 4.19** – (a) 3D model of part of the input matching network simulated in HFSS (b) Schematic of the same structure simulated in ADS using regular MLIN components and an S-parameter file obtained from HFSS.

#### "FLIX" AND "MYR" DESIGNS:

A more detailed photo of the fabricated layout for the design "FLIX" is shown in Figure 4.20. It is possible to observe the SMA to microstrip transitions, the input and output DC blocks and the biasing networks. The DC block capacitors are resonating at the frequency of operation  $f_0$ . Therefore they just introduce a small series loss at this frequency. Symmetry was respected at the output by inserting the DC power through

two different biasing networks. Low losses for the output matching network was one of the main concerns during the design. The design also includes two lumped RC parallel networks at the gate contributing to the stability of the circuit, as it was explained in subsection 4.3.4.2.

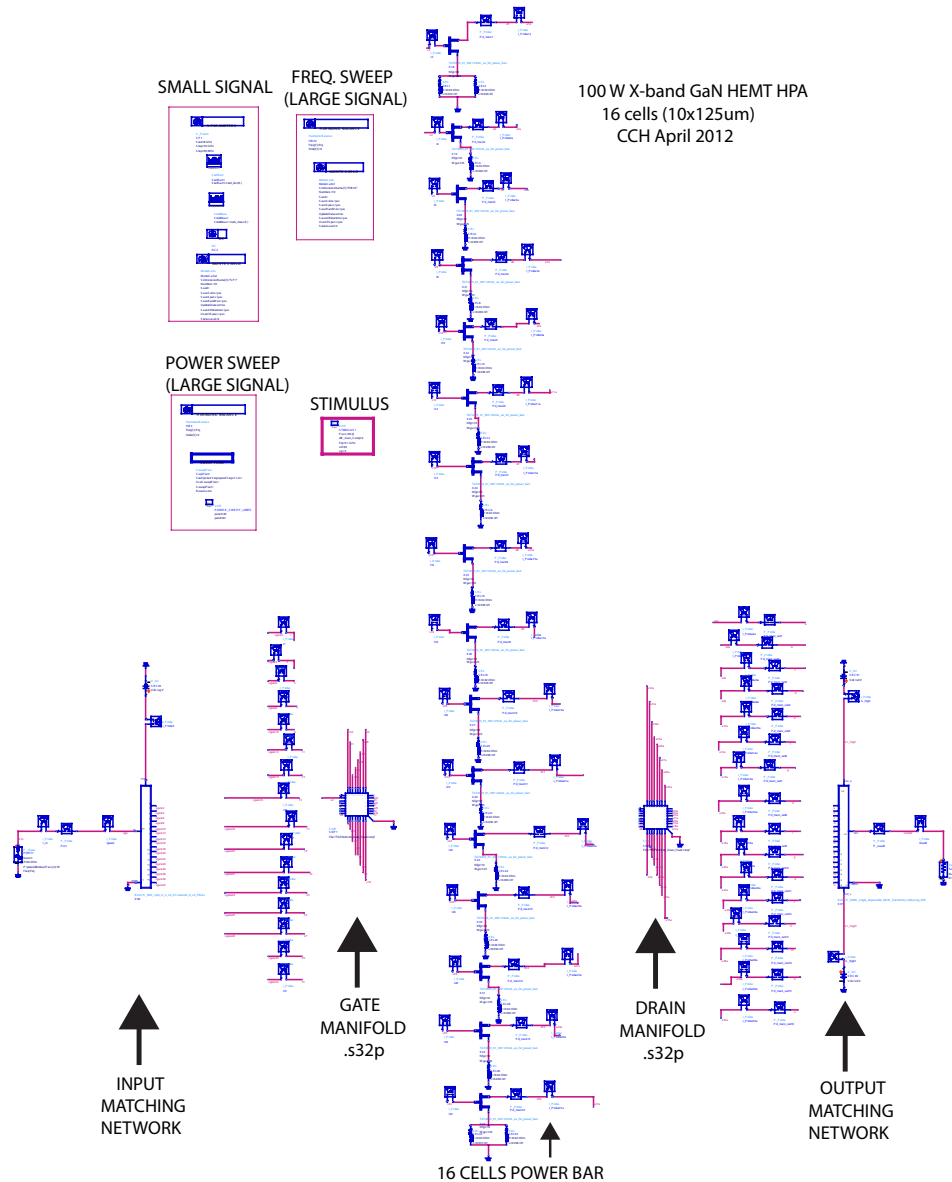


**Figure 4.20** – Photo of the Hybrid amplifier FLIX3 including a description of the main components. Biasing networks inside squares.

The design "MYR" in Figure 4.31a is very similar to "FLIX". The same design principles are followed and the same lumped components are used. The only differences are the movements along the Smith Chart followed during the matching network synthesis. The simulations obtained in ADS were almost identical for "MYR" and "FLIX". Only simulations for MYR will be presented here.

Figure 4.21 shows the schematic used in ADS to simulate the circuit "MYR". The blocks are interconnected by using variables due to the large number of connections. The input and output matching networks have a hierarchy underneath where the bondwire arrays and transitions simulations from HFSS are used together with ADS MLIN components and models for the lumped elements. Small signal characterization, large signal power sweeps, frequency sweeps as well as Monte Carlo analysis were performed. Furthermore, large signal stability was verified.

Figure 4.22 shows small signal parameters simulated for "MYR". The simulations were using  $V_{dd}=30$  V and  $I_{dd}$  DC biasing of 12.6 mA/mm of active area. Figure 4.22a shows the  $S_{11}$  parameter matched at 9.1 GHz. The small signal gain shown in Figure 4.22b was 8.6 dB. Figure 4.22c presents the traditional small signal stability Rollets factor  $K$ . The parameter was under 1 for frequencies around 251 MHz. The problem was disappearing when the transistor was operating loaded with 50 Ohm at the input and output as it can be estimated by looking at the augmented stability factor in Figure 4.22d. This indicates that the design always has to be operated loaded at input and



**Figure 4.21** – Schematic used in ADS corresponding to the full design of the 100 W high power amplifier at X-band. The components representing the input and output matching network have a hierarchy underneath where the bondwire arrays and transitions from HFSS are used together with ADS components.

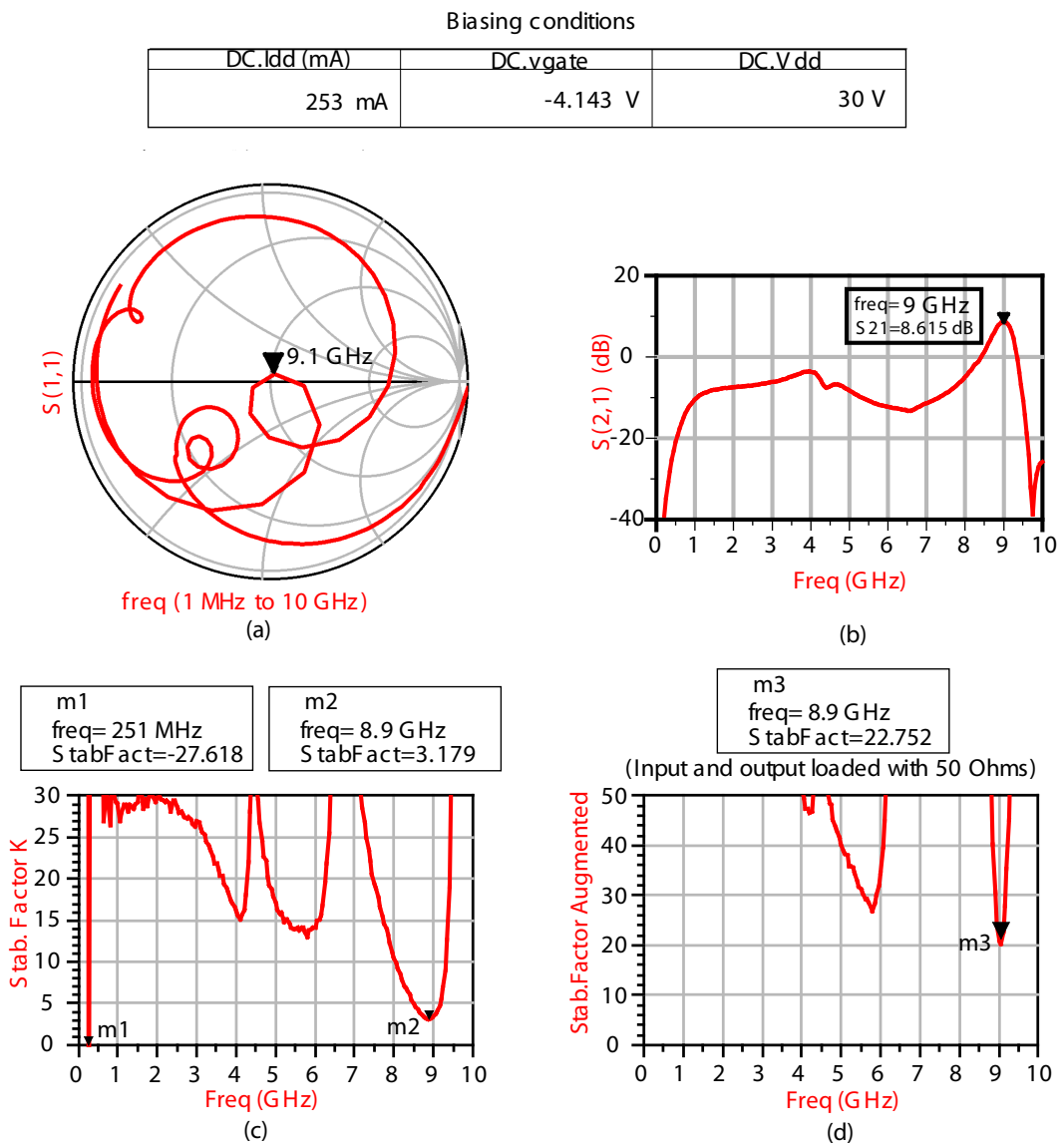
output. The stability circles were also analyzed.

A lot of efforts were placed into synthesizing matching networks with as much bandwidth as possible. Several techniques were available:

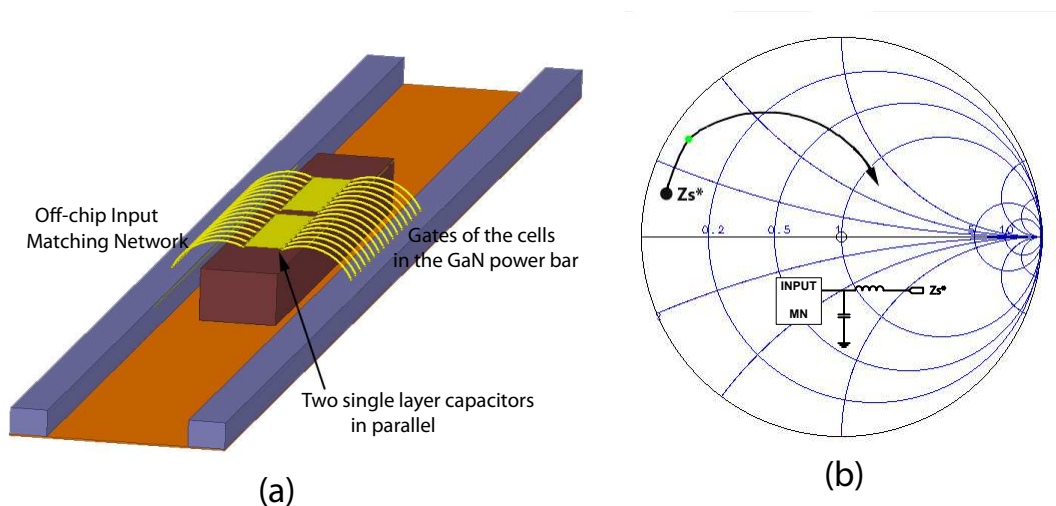
- Staying with constant small Q factors in the Smith chart helps to improve the bandwidth. This was especially difficult at the input matching network design. The impedance obtained after combining 8 gates in a single tab was very low and close to the edge of the Smith Chart, where the Q factor was already high.
- Following the optimal PAE load pull contours with the response of the matching network also allows larger bandwidths. This was not targeted in this design.
- The frequency response of structures like an open- or short- circuited stub can be used to create loops in the matching network. This technique was employed in the designs "MYR" and "FLIX". This allowed creating a loop close to the center of the Smith chart, as it can be observed in the  $S_{11}$  parameter shown in Figure 4.22a.

The low impedances at the input were specially difficult to match for a broad bandwidth. Another technique that would have allowed more bandwidth at the input matching network would have been to place a capacitor in parallel as close as possible to the gates. This technique has been implemented in the past in LDMOS hybrid designs at lower frequencies by using MOS capacitors. In this design, the technique could have been implemented by using two single layer capacitors in the same piece of substrate. The concept is illustrated in Figure 4.23a. The 16 transistor cells are combined in two groups of 8 cells that are connected by bondwires to two different single layer capacitors. The single layer capacitors are connected to the input matching network over the alumina also using bondwires. Figure 4.23b shows the movements that this structure would produce in the Smith Chart if we wanted to conjugate match the impedance  $Z_s$ . It has been assumed that the bondwires would have inductive behaviour. The capacitor in parallel allows to get closer to the center of the chart very efficiently. A capacitor of 1.3 pF in parallel was used in this example. This technique was not implemented for the actual design because it was increasing the complexity of the assembly and bonding process.

Figure 4.24 presents the simulation results obtained during a power sweep for the design "MYR" at 9.1 GHz. DC biasing of  $I_{dd}=12.6$  mA/mm of active area is used. All the data shown in this figure corresponds to the operating point indicated by the "MARKER" in Figure 4.24b. Maximum PAE of 47% was achieved, output power of 86.4 W and transducer gain of 7.37 dB, when using  $P_{avs}=42$  dBm. The losses introduced by the input matching network were around 2.95 dB and 0.47 dB for the output matching network. In Figure 4.24b, it is possible to observe gain expansion effect as  $P_{avs}$  is increased. This is due to a self biasing effect and the change in the input impedance of the transistors as the power increases. Figure 4.24c presents the drain current and voltage waveforms for one of the cells when driven with different  $P_{avs}$  power levels.



**Figure 4.22** – Small signal S-parameters and stability factor simulated for the design "MYR" (a)  $S_{11}$  (b)  $S_{21}$  (c) Rollets stability factor K (d) Rollets stability factor when the input and output are loaded with 50 Ohms.



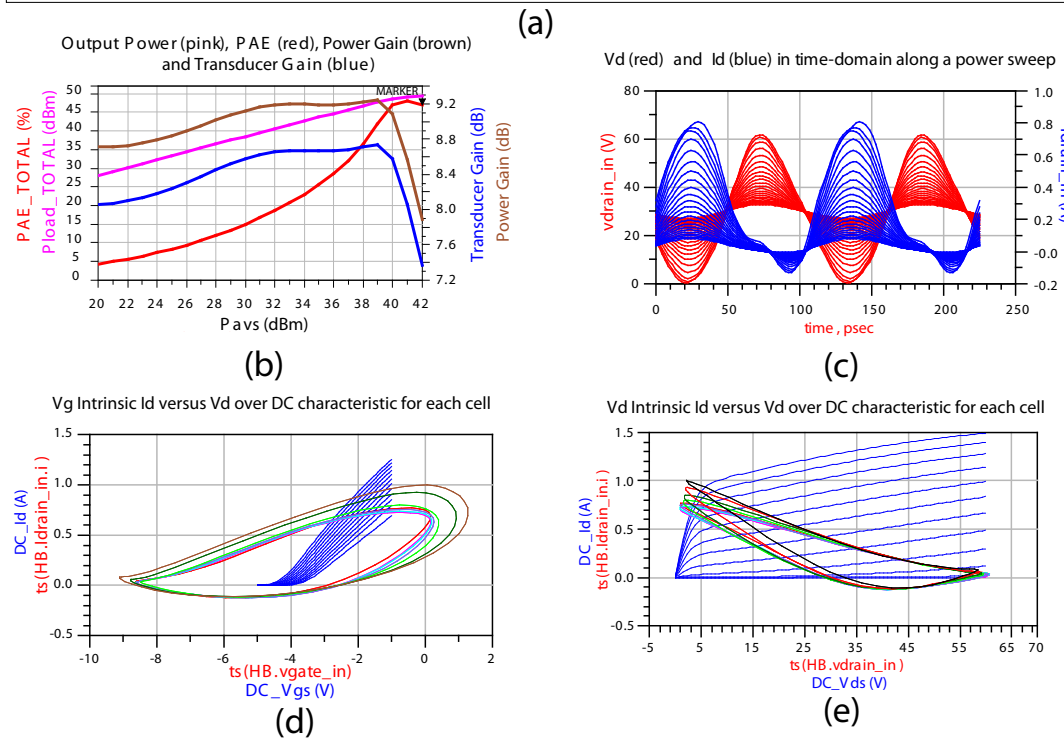
**Figure 4.23** – (a) Graphical illustration of the idea of matching the input by using two parallel single layer capacitors as close as possible to the gates of the transistors (b) Movements in the Smith chart produced by this structure.

The waveforms were measured at the intrinsic plane of the transistor represented as reference plane A (RPA) in Figure 4.2b. The waveforms were slightly different for the 16 transistor cells of the design, as it can be observed in Figures 4.24d and e. In these figures, the voltage and current waveforms are plotted over the DC characteristics of a single cell.

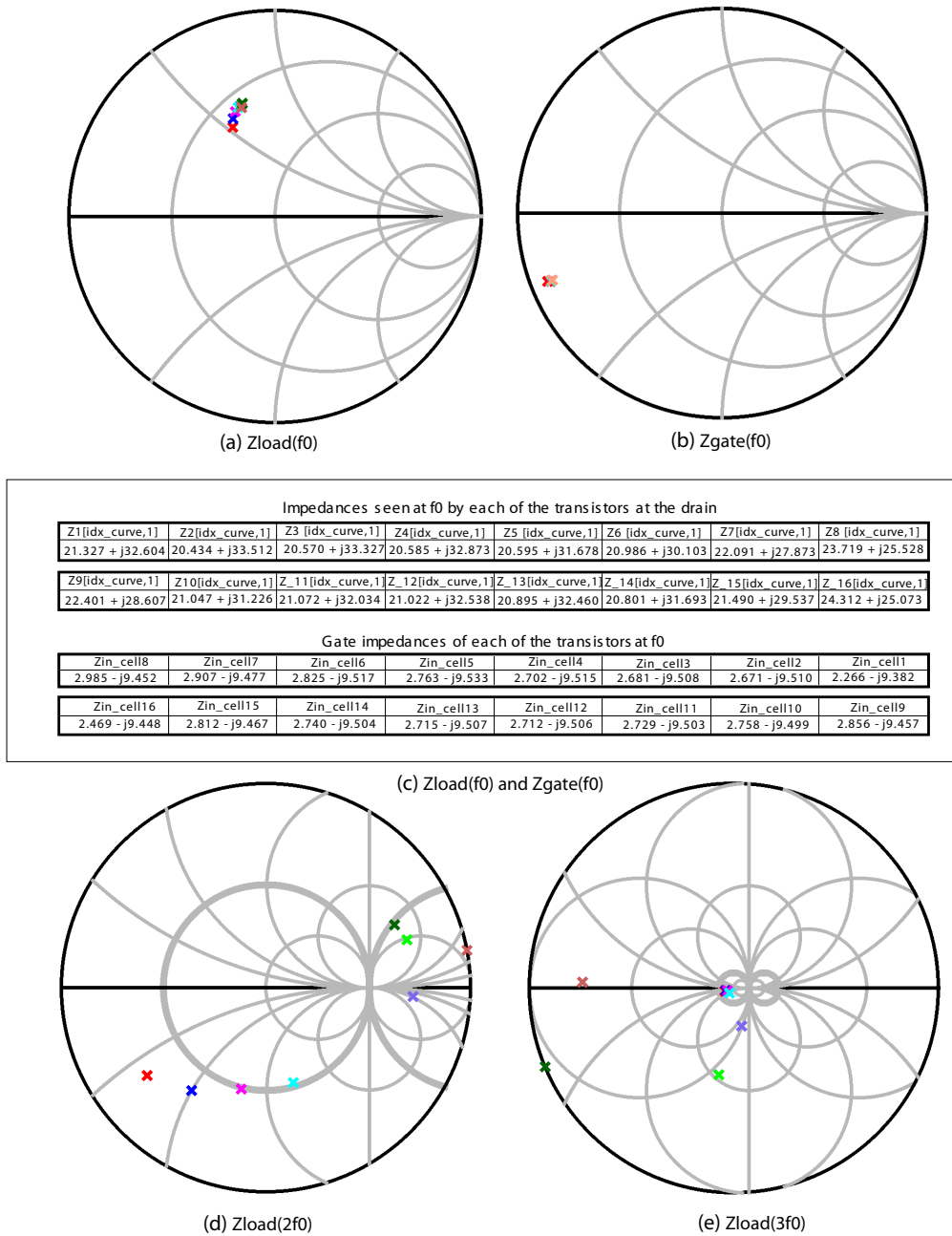
Figure 4.25 presents the impedances seen by each of the 16 cells of the power bar when operating at the point indicated by the "MARKER" shown in the power sweep of Figure 4.24b. Figure 4.25a shows the fundamental impedances seen at the drain intrinsic plane of each of the cells. As it was expected, the impedances seen by each of the cells are different, but still located closely. This is due to differences in the phase of the signal feeding each cell when using the combining configuration that was presented before. Figure 4.25b shows the input gate impedance of the different cells of the power bar. Figures 4.25d and e show the 2<sup>nd</sup> and 3<sup>rd</sup> harmonic impedances seen by the different cells at the intrinsic plane. For some of the cells, the impedances are out of the Smith Chart. This indicates that, in the simulations, there were leakages between the cells at the harmonics. This is the reason why harmonic matching was not targeted in the present design. At such high frequencies, the distance between neighbouring cells becomes more comparable to the wavelength. Therefore, the bus combiner at the output does not present the "virtual open impedance" between each of the cells. The isolation between cells is poorer at  $2f^0$  and  $3f^0$ , and harmonic currents run between the cells. In principle, this does not give stability problems.

Figure 4.26 shows four different simulated frequency sweeps when using four different Pavs for the design "MYR". The frequency was swept between 8.5 to 9.5 GHz.

Supply and input power levels			
Pbat	PinTOTAL	Pin_dBmTOTAL	Pavs
154.06 W	14.07 W	41.48 dBm	42.00 dBm
DC Bias conditions			Power levels at drain of transistors, before bondwire array
DC.Idd	DC.vgate	DC.Vdd	P_out_TOTAL_cells
253 mA	-4.143 V	30.00 V	96.442 W
			PAE_TOTAL_before_bondwires
			49.843 dBm
			0.535 %
Power levels at 50 ohm load ADDING contribution from all the cells		Power Efficiency at 50 ohm load	
Pload_TOTAL	Pload_dBmTOTAL	Eff_d_TOTAL	PAE_TOTAL
86.491 W	49.370 dBm	0.561%	0.470 %
Gain calculations		DC current under RF drive	Losses Matching Networks
Gsimp_dB_TOTAL	Gtot_dB_TOTAL	ldd	Losses_IMN_total
7.888 dB	7.370 dB	5.135 A	2.957 dB
			Losses_OMN_total
			0.473 dB

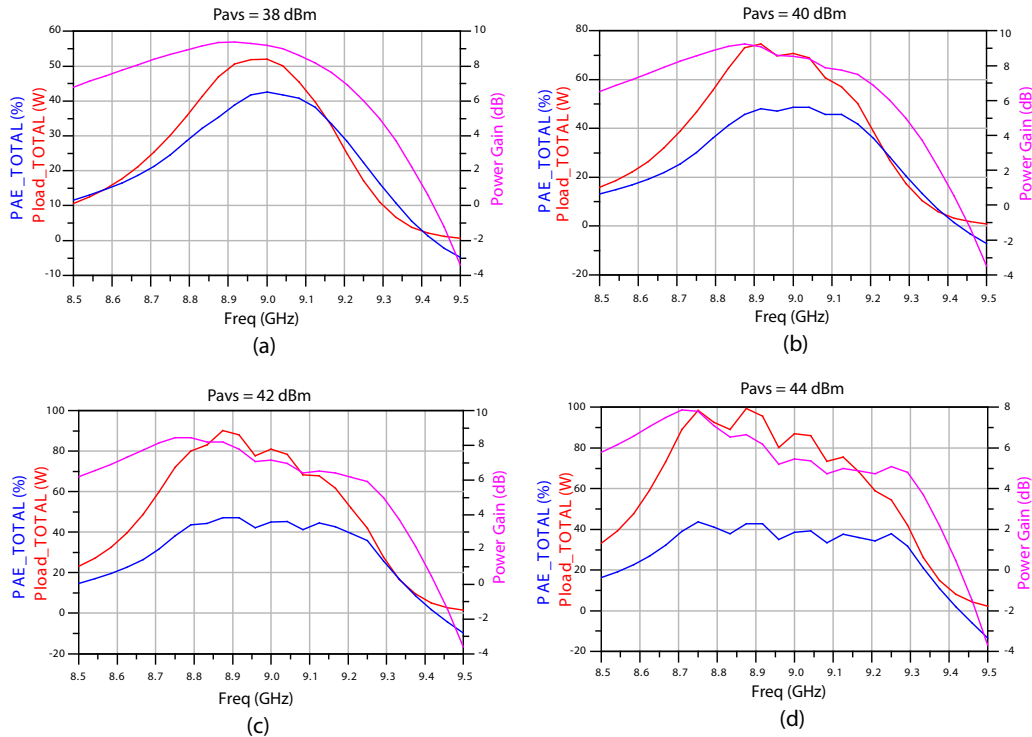


**Figure 4.24** – (a,b) Simulated data at compression obtained during a power sweep for the design "MYR" at 9.1 GHz . The "MARKER" shows the operation point for all the data presented in the table. (c) Drain current and voltage waveforms for one of the cells when driven with different Pavs power levels (d) Intrinsic drain currents vs intrinsic gate voltage for each of the 16 cells of the bar plotted over DC characteristics. (e) Intrinsic drain currents vs intrinsic drain voltages for each of the 16 cells of the bar plotted over DC characteristics.



**Figure 4.25** – Impedances seen by each of the 16 cells at the drain intrinsic plane. The operational point is indicated by the marker in Figure 4.24b. (a) Fundamental impedances. (b) Gate impedances. (c) Fundamental and gate impedances shown in a table. (d)  $2^{nd}$  harmonic impedances. (e)  $3^{rd}$  harmonic impedances.



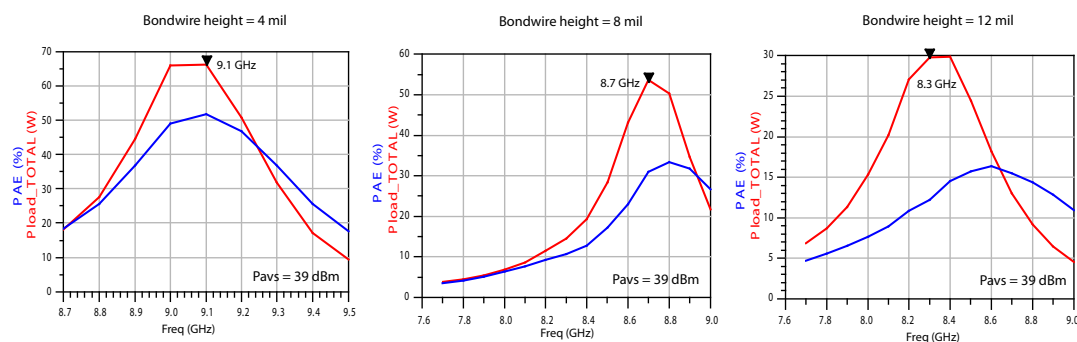


**Figure 4.26** – Four different simulated frequency sweeps for the design "MYR" when using (a) Pavs= 38 dBm (a) Pavs= 40 dBm (a) Pavs= 42 dBm (a) Pavs= 44 dBm

The effect of the fabrication spreads in the response was also investigated using Monte Carlo analysis. The value of the lumped components and the substrate characteristics were varied randomly within a given range. The  $\pm 5\mu\text{m}$  tolerance in the line widths was very tight and it was not significantly affecting the performance. The changes in substrate height and permittivity were more relevant. Furthermore, it was of special importance that the resonance frequency of the capacitors was accurately positioned around  $f_0$ . Figure 4.27 shows three different frequency sweeps that corresponds to simulations using bondwire arrays with different heights. The height of the bondwire was taken as the distance from the ground plane to the highest point in the bondwire. The three different bondwire arrays were simulated using HFSS. As it can be appreciated, the frequency response is very sensitive to the characteristics of the bondwire array. This was already anticipated in the discussion related to Figure 4.13 in subsection 4.3.4.1.

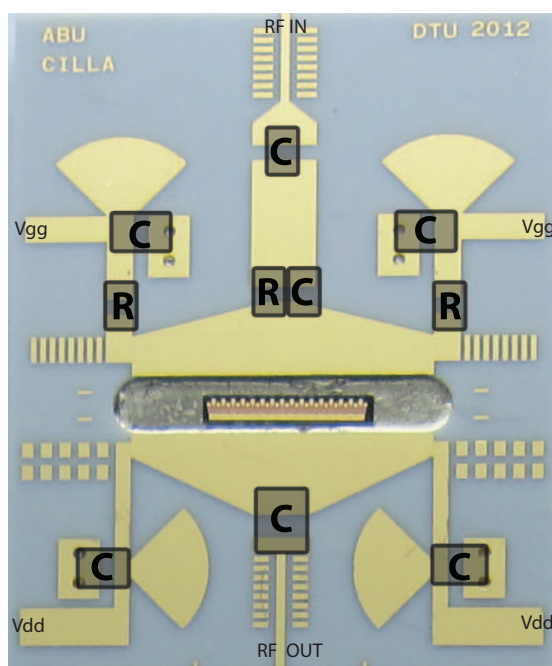
#### "ABU" DESIGNS:

The design "ABU" uses a single 20 mm power bar and combines the 16 cells using matching networks with a single tab both at the input and output. Figure 4.28 presents a detailed view of the design. The lumped components used here have the same functions as in the designs "MYR" and "FLIX". At the gates, the broad microstrip tab where all the 16 cells are combined presents capacitive behaviour. This allows realizing the



**Figure 4.27** – Simulated frequency sweeps for the design "MYR" using  $P_{avs} = 39\text{dBm}$  and bondwire height (a)  $h=4$  mil (b)  $h=8$  mil (c)  $h=12$

input matching following a similar procedure to the one that was illustrated in Figure 4.23 using a single layer capacitor in parallel.

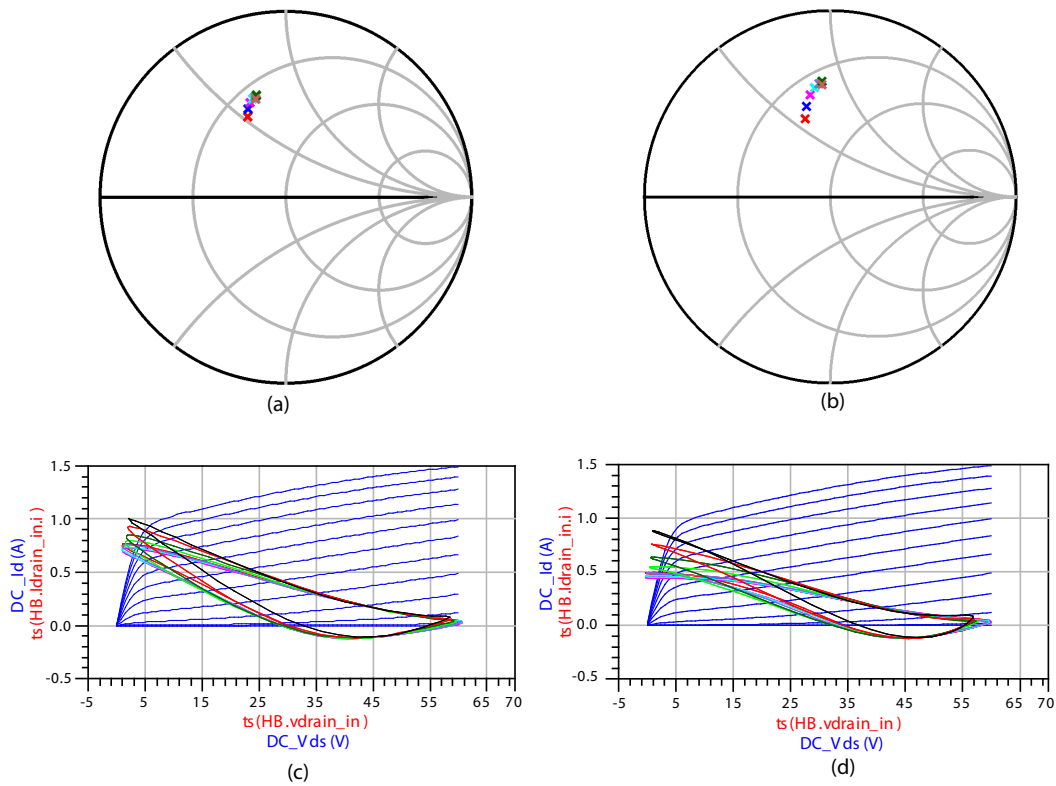


**Figure 4.28** – Fabricated layout of the design "ABU". The photo includes the lumped resistors and capacitors used in the design.

The simulated design ABU presented maximum PAE of 49.8% when using  $P_{avs}=39$  dBm, output power of 67.14 W and transducer gain of 9.27 dB at 9.1 GHz. The losses of the matching networks were similar to those of the design "MYR" and "FLIX". For the input matching network, they were around 2.27 dB, while for the output matching network they were around 0.48 dB. All these simulations were performed with DC biasing of  $I_{dd}=12.6$  mA/mm of active area.

Figures 4.29a and b show the simulated impedances loading the drain of each of

the cells when the designs "MYR" and "ABU" are delivering maximum PAE. The impedances synthesized in the design "ABU" (Fig.4.29b) are more spread in the Smith chart than the ones for the design "MYR" (Fig.4.29a). The same single tab configuration has been used in ABU and MYR for the output matching network, but not for the input matching network. Figure 4.29c and d shows the loadlines in the intrinsic planes for each of the transistor cells of the designs "MYR" and "ABU", overlapped over the DC characteristics of the cells. As expected there are more differences in the operation between the cells of the design "ABU" (4.29d) than of the design "MYR" (4.29c).

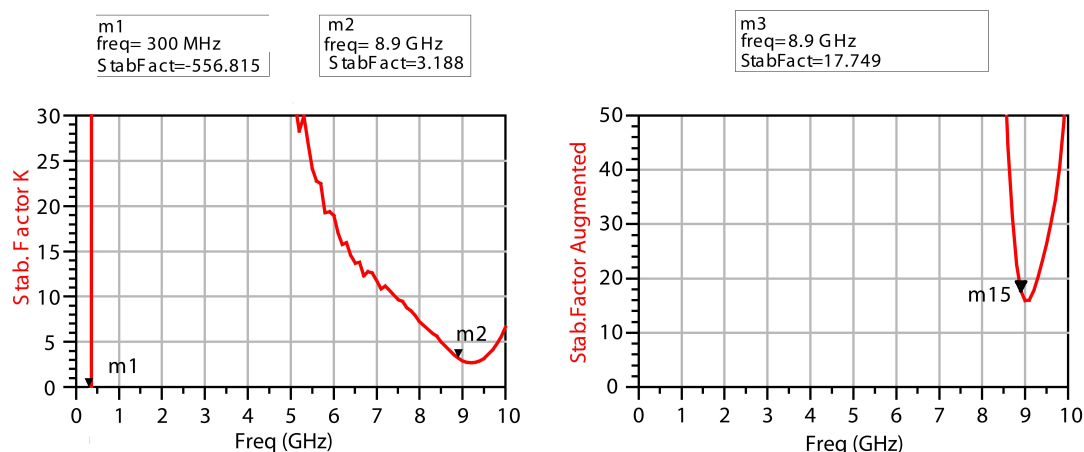


**Figure 4.29** – Load impedances and loadlines seen by each of the cells of the power bar at the drain intrinsic plane when they are performing with maximum PAE in the designs (a,c) "MYR" and (b,d) "ABU".

More uniformity in the operation of the cells was one of the advantages of combining the power bar cells in two groups of 8 instead of combining the 16 of them together in the same tab. This was the reason why larger power levels were obtained in the simulations for the design "MYR" and "FLIX" than for the design "ABU". But the most important reason why the design "MYR" and "FLIX" was more promising than the design "ABU" had to do with stability issues, as it will be explained next.

Figure 4.30a presents the simulated stability factor for the design "ABU". The K parameter was lower than 1 around 300 MHz, but the problem was solved when the

circuit was operating loaded by 50 Ohms at the input and output, as it can be observed in the augmented stability factor presented in Figure 4.30b. The same was happening with the design "MYR", as it was explained before.



**Figure 4.30** – (a) Simulated K stability factor for the design "ABU". (b) Augmented stability factor for the design "ABU".

Large signal stability analysis was performed using ADS and the commercial tool STAN. The method is based on the introduction of a single- and multiple small perturbations in different internal nodes of the design (Floquet Multipliers [88]). Current and voltage perturbation sources can be used as explained in [86]. A Harmonic balance simulation using mixer mode was performed using ADS. Afterwards, the poles and zeros of the transfer function for the perturbation probe were identified using the software tool STAN. If any of the poles of the transfer function were located at the right hand side of the imaginary plane, this was an indication of large signal stability problems [89], [90]. Power sweeps were performed at different frequencies. The frequency band between 10 MHz and 10 GHz was analyzed. The probe was placed in different locations of the circuit, and simulations using two perturbation probes simultaneously were also performed.

During the analysis done for the circuits "MYR" and "FLIX", a pole in the right hand side was appearing for power levels under  $P_{avs}=38$  dBm. It was solved by increasing the value of the resistor in the RC parallel structure from 10 Ohms to 18 Ohms. Increasing the resistor value to 25 Ohms was making the poles to move even further from the right hand side of the complex plane. For the design "ABU" there was a pole of the transfer function at 2.9 GHz that was on the right hand side of the complex plane. The pole was appearing if  $P_{avs} = 39$  dBm. There was also a pole at 690 MHz that was appearing when  $P_{avs}= 20$  dBm. A lot of different stabilization strategies were tried. But it was not possible to find a point in the design where inserting components in the circuit was solving the stability problems without compromising the performance. It is very probable that these parametric oscillations were caused by internal unstable loops

between the cells of the power bar. The design "MYR" and "FLIX" were overcoming this problem by combining the cells of the power bar in two groups. Even though the simulations were predicting stability problems for the design "ABU", it was decided to fabricate it in order to verify it with measurements.

It is also important to highlight that in spite of the reported large signal stability problems, the simulations for the three designs presented until now were not giving harmonic balance convergence problems for frequencies between 7.5 to 9.5 GHz. Furthermore, the parametric oscillations were not detected using the small signal stability analysis. This indicates the importance of performing large signal stability analysis during the design process.

#### 4.3.5.2 Design Using a Single 10 mm Power Bar

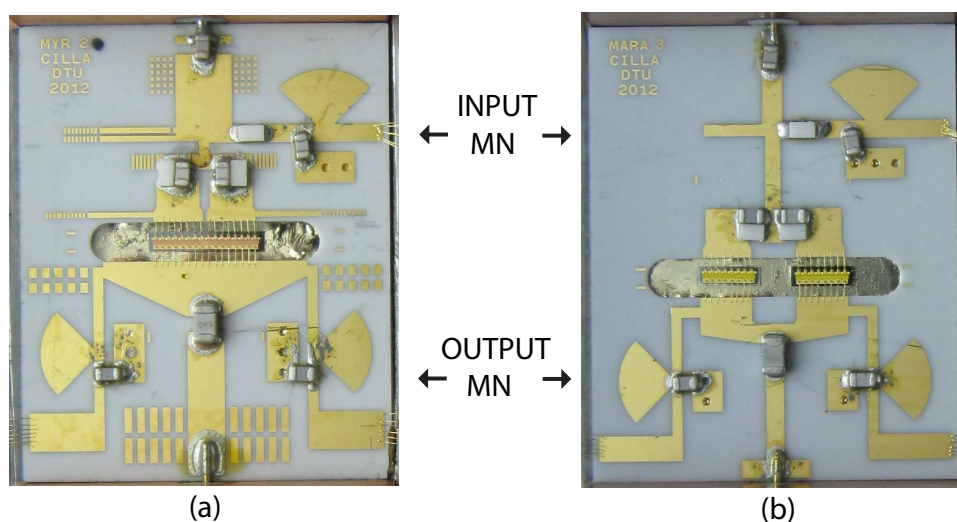
Figure 4.31b presents a photo of the fabricated circuit "MARA". The design uses two separate power bars with 8 cells in parallel each. Both the input and output matching networks combine the active devices in two branches. The design MARA was done based on the optimal impedances obtained from load pull simulations for the single cell. The lumped components used here have the same functions as in the design "MYR" presented before. This circuit was fabricated to compare the difference in performance when using designs with one single power bar and when using two separated ones. The expected differences are mainly due to an improvement of thermal performance in this solution. It is important to highlight that the model did not include thermal modelling, so it was not possible to assess if an increase in the temperature of the transistors could give rise to new oscillations or other problems. The simulated power levels and efficiencies obtained were similar to the ones of the designs "FLIX" and "MYR". Large signal analysis did not forecast problems. The value of the resistor needed in the RC parallel to ensure large signal stability was 10 Ohm, smaller than the 18 Ohms required in the designs "MYR" and "FLIX".

## 4.4 Fabrication and Assembly of a Hybrid HPA

Apart from the design process using CAD tools, the project also focused on setting up the fabrication capabilities and the know-how required to successfully assemble and operate hybrid GaN amplifiers at X-band. It was the first time that high power GaN dies were assembled using the facilities available at the Danish National Microelectronic Clean Room. Figure 4.32a shows a drawing with all the materials that were used for the hybrid fabrication. Figure 4.32b shows a photo of the hybrid assembled over the copper enclosure.

The assembly steps that were followed comprise of:

- 1) The first step was to attach the power bar and the alumina print to the CuMoCu carrier at the same time. The eutectic attachment was done using a 25 $\mu$ m thick AuSn solder preform with 280 degrees melting point. A thin AuSn preform improves the

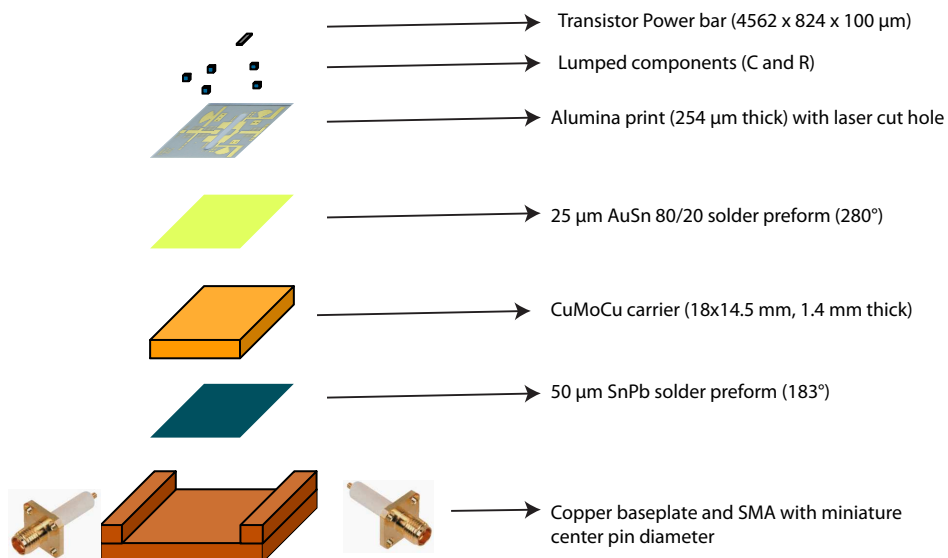


**Figure 4.31** – (a) Hybrid design MYR2 combining 8 cells in each of the two microstrip tabs at the input matching network. The photo shows the device fully assembled and ready for testing. (b) Hybrid design MARA using two separated power bars combined in parallel.

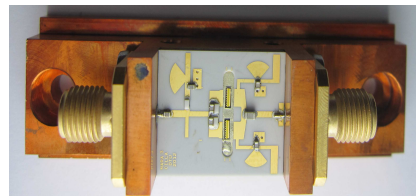
thermal performance. The CuMoCu carrier was heated at 320 degrees for a few seconds in order to make sure that the solder had melted. It is important to perform this operation under clean conditions and to apply a flow of nitrogen gas to avoid oxidation during the solder process and guarantee proper attachment. Furthermore, pressure was applied over the power bar with the placing tool, to make sure that no air bubbles were trapped between the power bar and the carrier. Alignment of the power bar within the laser cut hole was also important.

2) Afterwards, the lumped capacitors and resistors were attached over the gold pads in the alumina print using 60/40 SnPb solder paste that melts at 191 degrees. The center pins of the SMA connectors were also attached using solder paste. Simultaneously, the CuMoCu carrier was attached to the copper enclosure using a  $50\mu\text{m}$  layer of SnPb solder preform melting at 183 degrees. All the process was performed placing the copper enclosure over a hot plate and rising the temperature up to 220 degrees until the flux from the solder had evaporated. The AuSn solder was not melting at this temperature, so the the power bar was not moving during this step. This step was also tried using a reflow oven, but the process was faster and easier to control over the hot plate. The PTFE insulator inside the SMA connectors was expanding around 0.08 mm in length during the assembly over the hot plate. But no damage was detected. The connector is specified to operate between a temperature from -65 to 165 degrees.

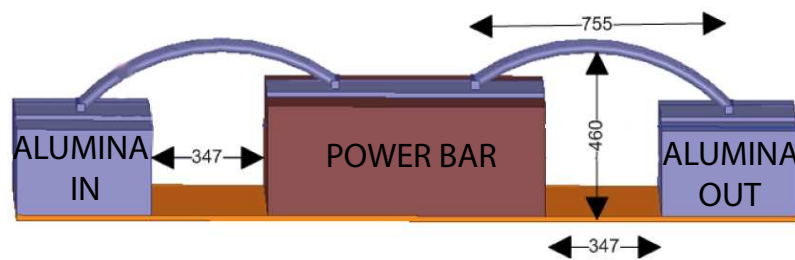
3) The third step was to place all the bondwires required. The bondwire dimensions are shown in Figure 4.32c. They were carefully specified according to the data used during the simulations.



(a)



(b)



(c)

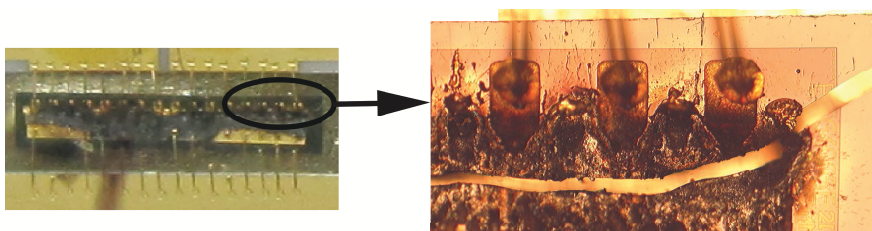
**Figure 4.32** – (a) Materials used for the hybrid assembly (b) Hybrid assembled over copper enclosure (c) Bondwire dimensions at the interface power bar-to-alumina prints.

## 4.5 Measurement Campaign Results

In total, 11 modules using one 20mm long power bar per design and 3 modules using two smaller 10 mm dies in parallel were manufactured. Out of these 11 single bar modules, 2 did not pass the fabrication stage. The other 9 were tested for small signal operation and four of them were also tested for large signal operation. At the end of the test, 2 out of the 9 modules were burnt.

Out of the 3 modules using two power bars in parallel, only one was tested for small signal and none of them for large signal operation. Two of the modules did not pass the fabrication stage and the last module was burnt during small signal testing.

It was possible to DC bias the modules that were burnt, and small signal measurements were recorded for them. The modules were failing when the drain bias current was increased, indicating problems with the heat dissipation. The current in the supplies was limited, so the possibility of having an oscillation generating an overcurrent was discarded. The assembly process was reviewed. The modules burnt were corresponding to the first ones fabricated. No pressure was applied over the die while heating up the carrier during the eutectic attach process. This was probably causing bubbles of air to be created under the die. In the second and third fabricated batches, pressure was applied during the attach process by using the tip of the placing tool. It was important to take care not to break the air bridges while doing this. These modules were not failing when the DC drain bias current was increased. This theory is also supported by the observations of the power bar after burning. Figure 4.33 shows a photo with a burnt power bar, and a detailed view of the die. It is possible to observe that the die was cracked in the middle. Half of the power bar was fully detached from the carrier. This supports the idea that the bar was actually not properly attached to the carrier and that there were air bubbles under it.



**Figure 4.33** – Design with the power cell burnt and cracked after testing.

The design included large electrolytic capacitors placed externally in the gates and drains for supplying the required charge during pulsed operation. Without these capacitors I found oscillations at very low frequencies under 100 KHz. Apart from the capacitors, a 1 KOhm resistor in series at the gate DC supply terminal was used. Different single layer decoupling capacitors were placed at the gate and at the drain DC supplies.

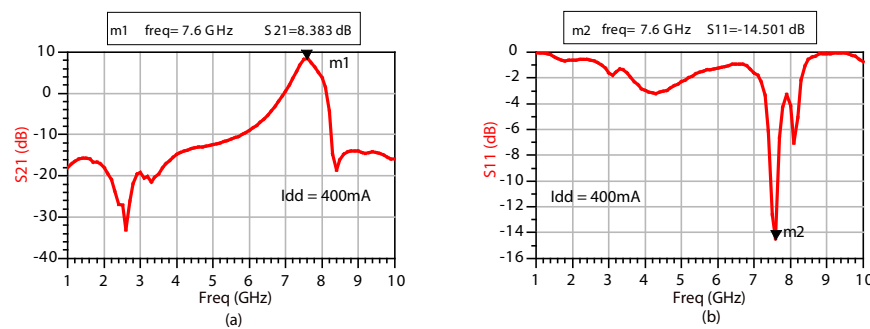
Photos of the test bed that was build at DTU are shown in Appendix D.



### 4.5.1 S-parameter Measurements

The modules passing successfully the assembly process were tested for small signal behaviour using different DC biasing  $I_{dd}$  currents from 0 mA (pinched-off) up to 500mA. The S-parameters were measured using  $P_{avs} = -20\text{dBm}$ .

Figure 4.34 presents S-parameter measurements for the module "FLIX" using  $I_{dd} = 400\text{ mA}$ . The device presents  $S_{21} = 8.383\text{ dB}$ . Looking at the  $S_{11}$  parameter, it is possible to identify the double resonance matching. It is also possible to observe how the gain at low frequencies is reduced efficiently.



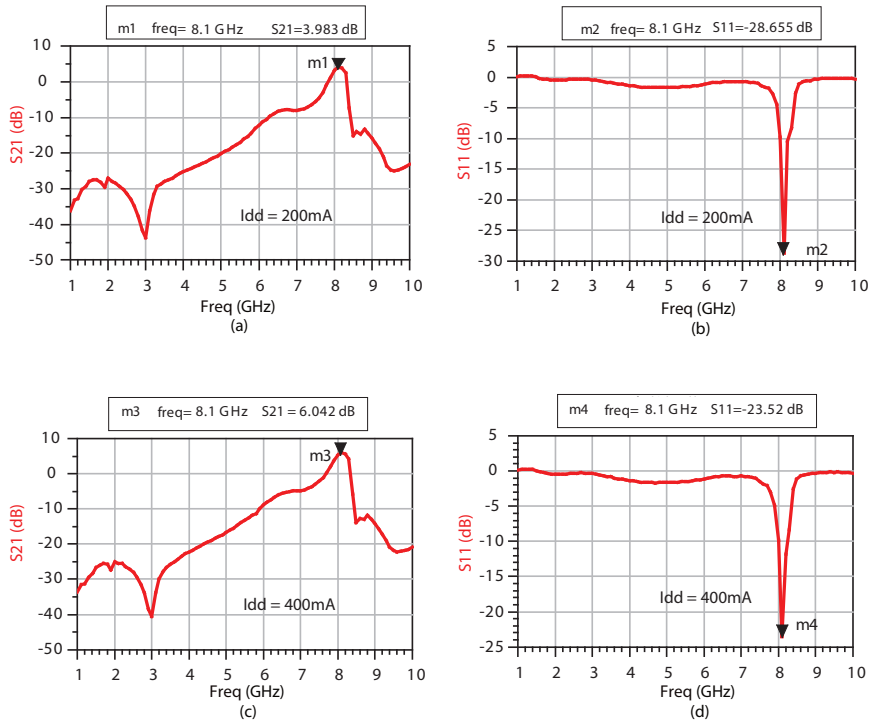
**Figure 4.34** – Measured S-parameters for the design "FLIX" using  $I_{dd} = 400\text{ mA}$

Figures 4.35a and b show small signal measurements for the device "MYR" when using  $I_{dd} = 200\text{ mA}$ , while Figures 4.35c and d use  $I_{dd} = 200\text{ mA}$ . The design is centered around 8.1 GHz.

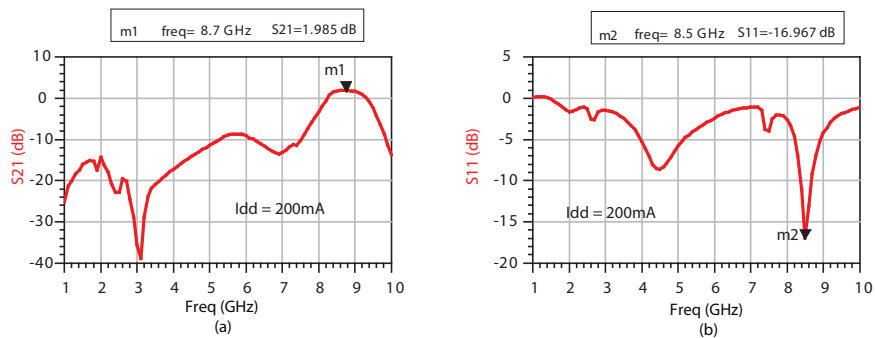
Figure 4.36 presents S-parameter measurements for the design "MARA" using  $I_{dd} = 200\text{ mA}$ . The design was burnt when  $I_{dd}$  was increased to 300 mA. Only measurements using lower  $I_{dd}$  were recorded for this device. The most probable explanation is that one of the two bars was not properly attached to the carrier and it was not dissipating the heat correctly. This might be explained because during the assembly process, pressure was applied with the placing tool only over one of the two power bars. The small signal gain of the design was low at these DC biasing levels. Tuning was required. It is possible to observe that the  $S_{21}$  response was more broadband than for the devices "MYR" and "FLIX". Broader bandwidth was one of the foreseen advantages of having a design with two dies. It would have been interesting to test the design for large operation, but there were no more power bars available.

### 4.5.2 Large Signal Pulsed Measurements

High power sweeps were done at different DC biasing conditions and for different frequencies for the devices "MYR" and "FLIX". Table 4.1 offers a summary of the most outstanding large signal measurements for these devices. The power measured by the peak power meter was an average of the power within each pulse removing the first and last 25  $\mu\text{sec}$  of the pulse.



**Figure 4.35** – Measured S-parameters for the design "MYR" using (a)(b)  $I_{dd}=200\text{ mA}$  (c)(d)  $I_{dd}=400\text{ mA}$



**Figure 4.36** – Measured S-parameters for the design "MARA" using  $I_{dd}=200\text{ mA}$

Design / Measured parameter	MYR	FLIX
$f_0$ (GHz)	8.3	8.3
I <sub>dd</sub> (mA)	50	200
P <sub>max</sub> (W)	94.5	75
Large Signal Gain (dB)	7.6	7
PAE (%)	> 60%	> 50%

**Table 4.1** – Summary of the large signal measurements for the designs MYR and FLIX. The devices were operating slightly under 1 dB compression point. Large signal testing of the designs MARA and ABU was not performed because the few devices available did not pass the fabrication stage or were burnt during small signal testing.

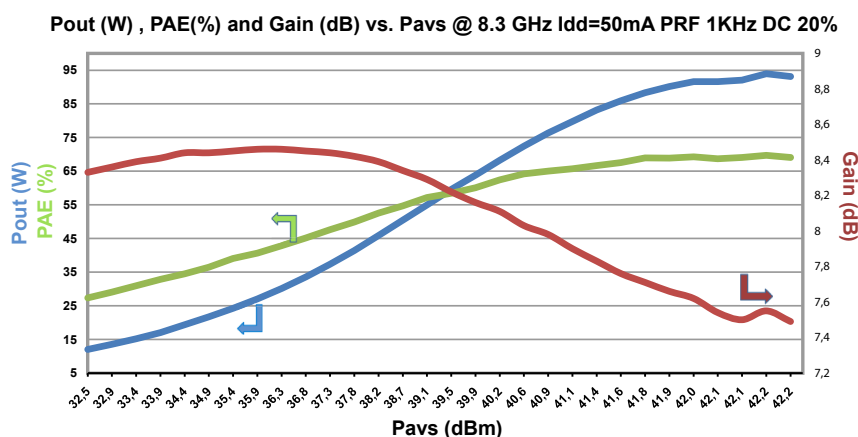
The designs were shifted down in frequency, and the linear driver available had to be used in a frequency range where the performance was not optimal, but still acceptable. The maximum power delivered by the driver was around 44.5 dBm (30 W) along the operating frequency band between 8.5 and 9.5 GHz. At 8.1 GHz, the center frequency for the design "MYR", the maximum P<sub>avs</sub> was around 43.8 dBm. At 7.5 GHz the maximum P<sub>avs</sub> was around 34 dBm. Furthermore, there were losses between the driver output and the input of the DUT of around 2 dB. The losses were coming from the isolator, cables and an hybrid coupler. This contributed to limit even further the power available from the driver. Therefore, it was not possible to drive the device into hard compression.

Two different pulses with different duty cycles were used. Pulses with 9.63% and 20.54% duty cycle. The modulating pulses were analyzed carefully by using the oscilloscope and a crystal detector in order to measure their duration, rise and fall times. These parameters are very important to calculate accurately the PAE under pulsed operation. In the case of 9.63% duty cycle, the measured pulse length was 996  $\mu$ sec and the pulse width was 96  $\mu$ sec. In the case of 20.54% duty cycle, the measured pulse length was 1480  $\mu$ sec and the pulse width was 304  $\mu$ sec. The results obtained with the two different pulses were very similar.

The most outstanding result was obtained for the device MYR 4 and it is presented in Figure 4.37. The device was biased using I<sub>dd</sub>=50 mA. 94.5 W were measured under pulsed operation at 8.3 GHz and with a gain of around 7.6 dB. The device was working around 1dB compression, but it was not possible to push it further into compression since the driver used was compressing as well. It would be possible to reach and slightly surpass 100W if a driver amplifier providing enough power at this frequency is used. The high efficiency obtained (>60%) is looking too good at this frequency. The process to get the efficiency was analyzed carefully and no errors were found. The power levels were measured correctly and accurately using an advanced peak power meter and the test set up losses were carefully de-embedded. The consumed average power levels were also measured using an accurate current meter.

In Figure 4.37 it is possible to observe the effect known as gain expansion. The gain is

lower when the device is operated at small signal levels, and it increases as we approach the large signal operation, to be reduced again when entering into compression. This is due to self biasing of the devices at large drive power levels, and also due to the large changes of the input impedance of the devices with the source available power.



**Figure 4.37** – Measured power sweep for the design "MYR" at 8.3 GHz. Pout in blue, PAE in green and Gain in red. Idd=50 mA, PRF=675 Hz, Duty Cycle 20.54%

Figure 4.38 presents a frequency sweep for the device "MYR". The measurements were done for seven frequencies between 8 and 8.4 GHz and using different constant Pavs, Idd=100 mA, PRF=1 KHz and 9.63% duty cycle. The smaller constant source available power used for the test (38.8 dBm) corresponds to the one where the device gain starts to compress. At this operational point and in the band between 8.1 to 8.3 GHz, the output power of the device is larger than 45W, the PAE is above 30% and the gain is around 8.5 dB. The larger constant source available power used for the test (41.8 dBm) drives the device close to the 1dB compression point. Under these conditions and along the 200 MHz band between 8.1 to 8.3 GHz, the output power of the device is larger than 75W, the PAE is above 35% and the gain oscillates between 7.5 +/- 0.5 dB. The PAE varies fast between 35% and 60% along the band.

CW measurements were not performed due to the high risk of burning the device, because of the large amounts of average power involved.

Measurements of the device "FLIX" showed slightly worse performance than the design "MYR". Power sweeps were performed from 7.9 to 8.4 GHz and Idd=200 mA. Maximum power level of 75 W was measured at 8.3 GHz, with Gain= 7 dB, and the device working under P1dB. PAE was larger than 50%.

Comparing with the simulations, the response of the fabricated devices was shifted 1 GHz down in frequency. This can be due to several reasons:

- The simulations of the bondwire transitions were done in HFSS and the printed substrates were simulated separately in ADS. As it was explained in section 4.3.5, a shift of 300 MHz was observed if compared with a full HFSS simulation of the

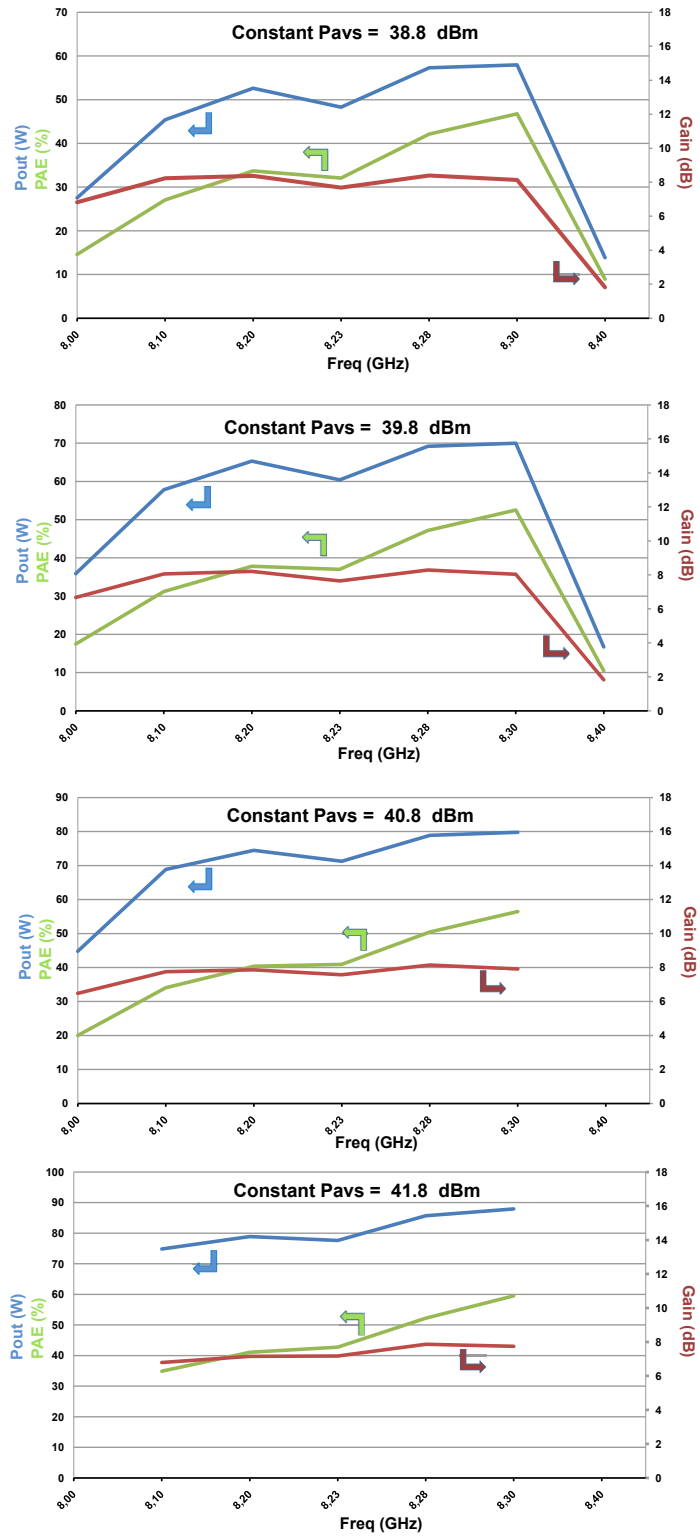


Figure 4.38 – Measured frequency sweep for the design "MYR" at different constant Pavs. Pout in blue, PAE in green and Gain in red. Idd=100 mA, PRF=1KHz, Duty Cycle 9.63%

transition plus the circuit over the alumina substrate.

- The height of the bondwires was not controlled accurately during the fabrication. In subsection 4.3.4.1, Figure 4.13 showed the shift in the input impedance to match when different bondwire heights were used. Furthermore, Figure 4.27 in subsection 4.3.5.1 presented the effect of the bondwire height in a full HB simulation. A considerable shift in frequency was observed.
- The resistors used in the parallel RC networks at the gate had more parasitic inductance than the one specified in the datasheet. This was because the lumped component was mounted over a different substrate than the one used for the specifications.
- The large signal model was not validated with measurements. The really small input impedance at the gate makes very difficult to get a broadband match. Model gate impedance was not validated. Furthermore, the input impedance was changing fast with the power level used.

In spite of the shift in frequency, the measured maximum power levels and the associated gain were in agreement with the simulations. The measured PAE was higher than expected. Furthermore, the  $I_{dd}$  DC biasing current required to get best performance was smaller than in the simulations. Best simulated performance was obtained with  $I_{dd}=250$  mA while during the measurements,  $I_{dd}=50$  mA was giving best results.

## 4.6 Conclusions and Future Work

The goal of the project presented here was to develop a high power amplifier for X-band frequencies with capabilities to replace the vacuum tubes used in radar systems designed by Terma, the company co-funding the project. An MMIC solution was discarded because of the high cost involved, due to the large GaN area needed and the low yields expected. A 100 W GaN hybrid high power amplifier design operating at X-band has been presented. 94.5 W were measured under pulsed operation at 8.3 GHz and 1 dB compression. The device was biased using  $I_{dd}=50$  mA. The associated gain was 7.6 dB and the PAE >60%. It will be possible to surpass the 100W output power when a more powerful driver is used to operate the device into harder compression. The power level achieved here is in agreement with the highest ones that have been published at this frequency. The PAE is higher than any other one published for these power levels. The PAE measurement procedure was reviewed carefully. The pulse width and duration were measured accurately and an advance peak power meter was used. Several frequency sweeps were performed at different constant input available power levels. Limited bandwidth was achieved. In the 200 MHz band between 8.1 to 8.3 GHz, and at 1 dB compression, the device was delivering power levels larger than 75 W, PAE >35% and gain oscillating between 7.5 +/- 0.5 dB. Simulations predicted power levels

similar to the ones measured. But the measurements were shifted down in frequency by 1 GHz. Possible reasons for this disagreement include non accurate control of the bondwire height during manufacturing, simplifications done during the simulations and possible errors in both the nonlinear model and the linear resistor model. Furthermore, the transistor model did not include thermal characterization.

The single stage hybrid design approach has been described in detail. The first step was the selection of the 0.25  $\mu\text{m}$  SiC over GaN power bar technology from Triquint. Preliminary load pull simulations in ADS were performed over a single 1.25 mm cell in order to select the optimal loading conditions. The technology was evaluated by performing a measurement campaign over a single cell. The device was operated under large signal delivering 5.6 W/mm. This demonstrated that a 100W design was feasible by using 20 mm of active area.

Alumina substrate was selected for synthesizing the matching networks, SMA connectors with miniaturized central pin and lumped capacitors and resistors. Custom made CuMoCu and Aluminium diamond carriers were used.

The bondwire array transitions were analyzed carefully by performing extensive 3D EM simulations using HFSS. The usefulness and accuracy of full-wave electromagnetic simulation tools for modeling bondwire arrays has been validated with a purpose built 16 bondwire array structure. The accuracy of the inductor-based bondwire model is not always enough. This work has revealed the importance of using an accurate bondwire array model during the design of hybrid power amplifiers above C-band.

The suitability of the lumped components, biasing networks and transitions was also evaluated with measurements. The resonance frequency of the capacitors was very dependent on the substrate height and permittivity used.

Two different designs have been discussed: one using a 20 mm power bar and the other one using two 10 mm bars in parallel. The 20 mm bar comprises of 16 cells in parallel and each of the 10 mm bar has 8 cells.

For the design using a single 20 mm power bar, the number of cells to be combined at the gate side was considered. Nonlinear models for the transistors, HFSS data for the bondwire arrays and transitions and linear models for the manifold structures and the matching networks were used to perform Harmonic Balance simulations. They showed that the device was easier to match at the gate if two separated tabs were used to combine the cells into two groups of 8. Furthermore, large signal pole-zero stability analysis showed that the device was always oscillating if all 16 gates of the cells were combined into a single tab. Different strategies were followed to avoid instabilities. Parallel RC networks were used in series with the gates to kill the huge gain of the device at low frequencies and avoid oscillations. Three different designs were manufactured using a single 20 mm bar. Two of them called "MYR" and "FLIX" combining the gates of the 16 cells into two tabs. One called "ABU" combining the 16 cells in the same tab. Only measurements of the former ones were performed, obtaining the good results reported before. The design "ABU" did not pass the fabrication stage and it was never

tested. It might be interesting to fabricate this device in the future to verify that the design always oscillates independently of the elements inserted to try to stabilize it.

The advantages of the design with two 10 mm cells in parallel were a better thermal performance and impedances easier to match along a broader bandwidth. Small signal measurements of the design called "MARA" showed promising results with increased bandwidth. Unfortunately, two of the three modules fabricated were destroyed during the assembly process. The last one was burnt during small signal testing probably due to improper die attach. Gain was low and tuning will be required in future activities.

The assembly process was complex, requiring many steps. A lot of time was invested in setting up the fabrication facilities to perform proper eutectic die attach and bonding. It was important to perform the die attach under clean conditions and to apply a flow of nitrogen gas. It was also necessary to apply a gentle mechanical pressure over the die during the attachment to avoid air bubbles under it and guarantee efficient heat transfer.

Follow up activities within this project would focus on centering the response at 9.1 GHz. Better control of the bondwire height helps in this direction. Full electromagnetic simulations of the array, transitions and matching networks might also be beneficial. Preliminary tuning activities were done based on data extracted from the simulations. It proved to be useful, but time consuming. A module to module performance comparison to assess yields should be required. It would also be interesting to test the devices at larger  $V_{ds} = 48 - 50$  V and compare performance. The lumped components used can withstand these voltage levels, but the simulation models did not allow them. A nonlinear electrothermal model could also be very useful to perform simulations using temperature gradients between the cells. Measurements of the heat distribution along the power bar might also be interesting. More units of the design "MARA" using two 10 mm cells should be manufactured.

Higher gain is desired. A two stage hybrid design is possible after the design and manufacturing experience earned with this project. Two stage hybrid designs for X-band have already been reported in [111]. An MMIC delivering 100 W at X-band is possible, but it would require a lot of GaN chip area and low yields. An attractive alternative is a semi-hybrid solution including two stages integrated in a single MMIC chip and the output matching network implemented over alumina substrate and joined to the MMIC with a bondwire array. This solution saves GaN area, thus reducing cost. It might also benefit from the low losses of the alumina compared to the GaN, improving PAE.

To conclude, efforts have to be placed in the design of efficient combining structures in order to place several modules in parallel. A transmitter delivering 500 W average power would be a good candidate to substitute the tubes used in the radars designed by Terma. At least eight 100 W modules are required to reach these power levels. Spatial combining using coaxial to air waveguide transitions might be worth investigating [116], [117].



## PhD. Dissertation Conclusions

Solid State Power amplifiers have received much attention in the last years due to the fast development of GaN HEMT technology. This technology provides exceptional advantages when compared to tube-based amplifiers. A smaller footprint size, an improved reliability and their suitability for modern phase array systems makes GaN SSPAs serious candidates for tube replacement. Nowadays, the use of SSPAs has already surpassed the use of tubes in applications using frequencies of up to 4 GHz, and this tendency is expected to continue at higher frequencies in the near future.

The work presented here focuses on SSPAs designs using both MMIC and hybrid solutions for replacement of GaAs SSPA and amplifier tubes respectively. A lot of research has been done in the field of GaN, but there are still many interesting topics address such as improvements in thermal performance, efficiency enhancement and push the technology higher in frequency.

A compact 50 W GaN High Power Amplifier with PAE  $> 50\%$  at C-band for the next generation of Sentinel satellites has been presented. The results of the measurement campaign provide excellent results. The maximum average power level measured under pulsed operation is 53.16 W and the maximum overall PAE measured is 55.8%. The MMIC presents a satisfactory 0.5dB bandwidth of 450 MHz centered at 5.1 GHz. The work presented here represents, to the best of my knowledge, the highest efficiency ever reported on a single chip MMIC design at C-band for power levels above 50 W. In comparison with a solution of four GaAs MMICs combined to deliver the same power level, an improvement of  $> 15\%$  in PAE and a footprint reduction by a factor of four or more has been demonstrated.

A 100 W GaN hybrid high power amplifier design operating at X-band for tube replacement has been presented. 94.5 W have been measured under pulsed operation at 8.3 GHz and 1 dB compression. The associated gain is 7.6 dB and the PAE  $> 60\%$ . It will be possible to surpass the 100 W output power when pushing the device into harder compression. Limited bandwidth is achieved. Between 8.1 to 8.3 GHz and at 1

dB compression, the device delivers power levels larger than 75 W, PAE  $>35\%$  and gain oscillating between  $7.5 \pm 0.5$  dB. The maximum power level achieved for this design is in agreement with the highest ones that have been published at this frequency. The PAE is higher than any other one published for this power level. The PAE measurement procedure has been carefully reviewed.

The design process has been described in detail for both designs. The usefulness of using accurate nonlinear models and electromagnetic simulators has been confirmed. The models have been validated through S-parameter and load pull measurements.

The designs addressed here are especially relevant because it is rare to find publications in literature on MMICs below C-band and Hybrids above the same band. The reader is encouraged to refer to the conclusion sections of chapter 3 and 4 for a more detailed summary of the achievements of the present PhD dissertation.

Carlos Cilla Hernandez

Copenhagen, December 2012

# Appendices



# Appendix A

## C-band GaN transistors load-pull campaign photos

This appendix presents photos of the GaN C-band MMIC and the the test beds that were build during the load pull and measurement campaigns.



**Figure A.1** – Load pull measurement set up installed inside the Payload Division clean room

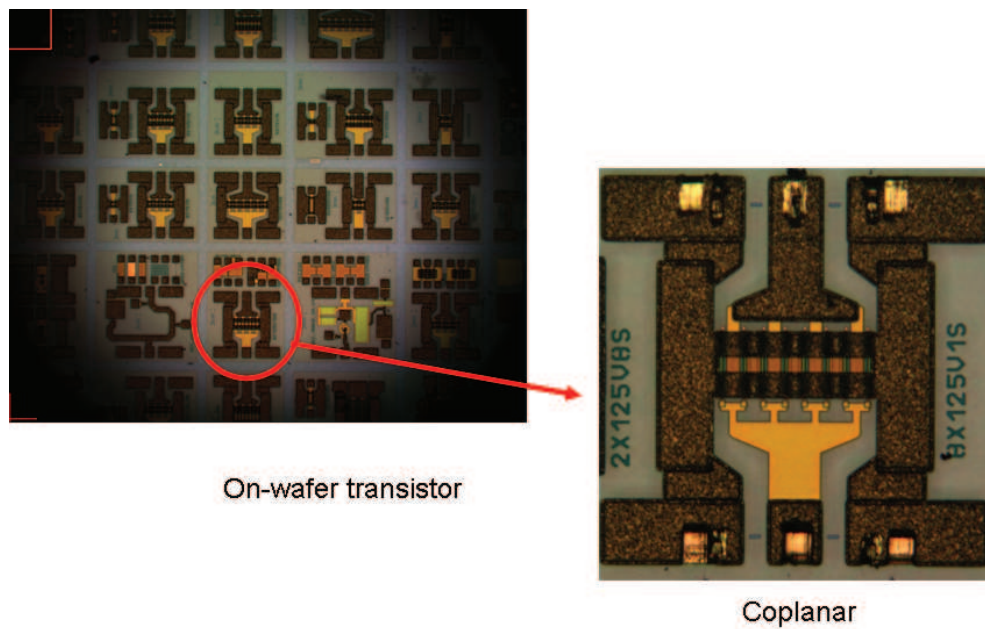


Figure A.2 – Overview of on-wafer transistor (coplanar)

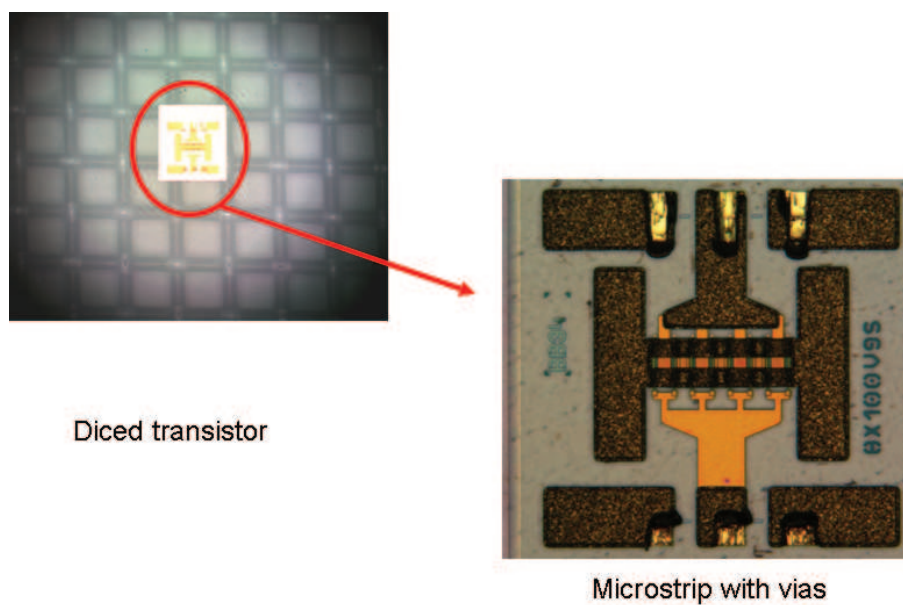


Figure A.3 – Overview of diced transistor (microstrip)

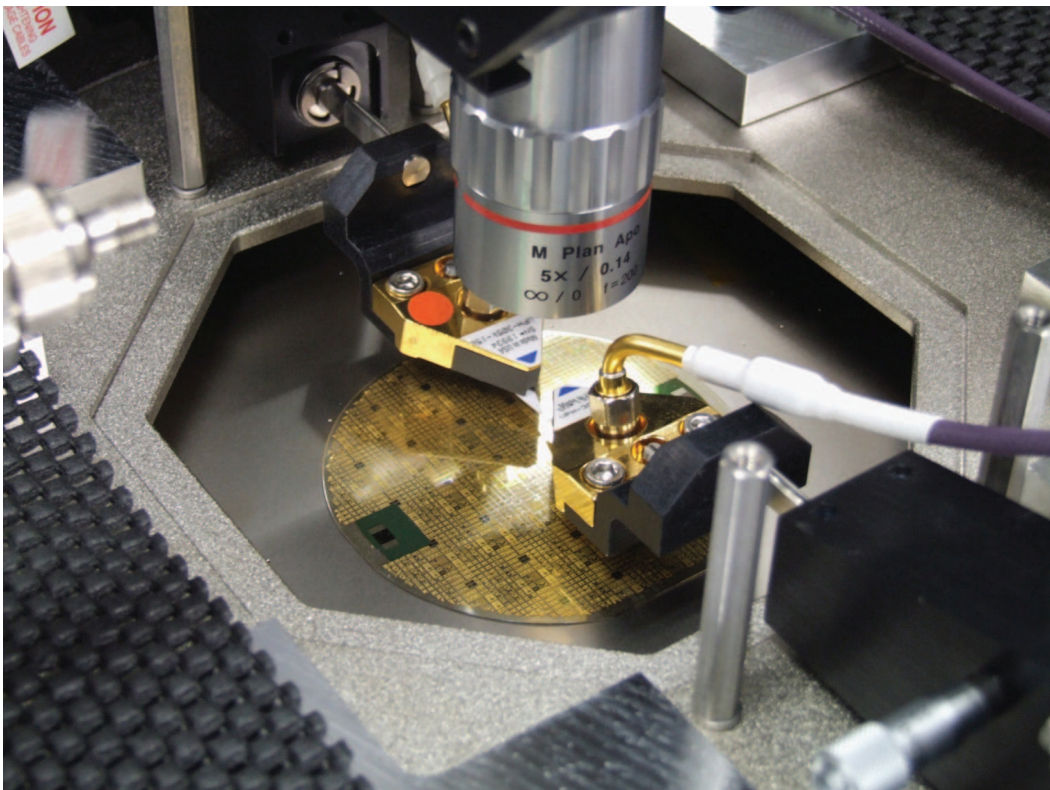


Figure A.4 – GaN wafer placed on the probe station





# Appendix B

## C-band MMIC test campaign photos

This appendix presents photos of the GaN C-band MMIC the test beds that were build during the final measurement campaign.



**Figure B.1** – Test bed prepared at ESA ESTEC Payload Division Laboratory

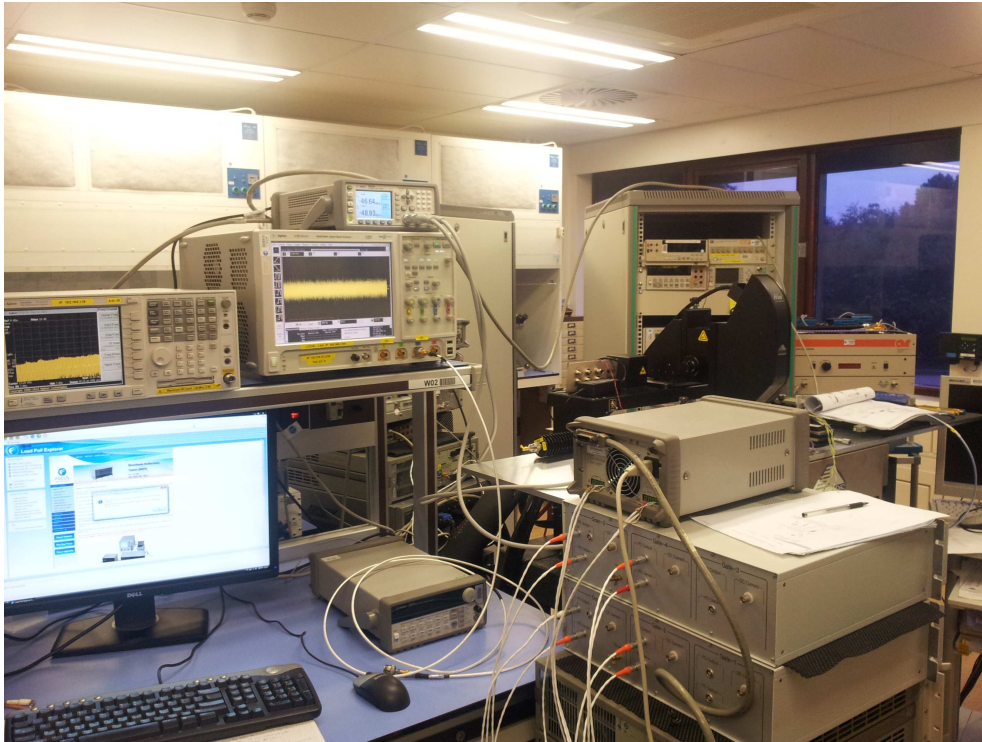


Figure B.2 – Test bed for MMIC test campaign



Figure B.3 – Custom made DC probes with SMC male connectors

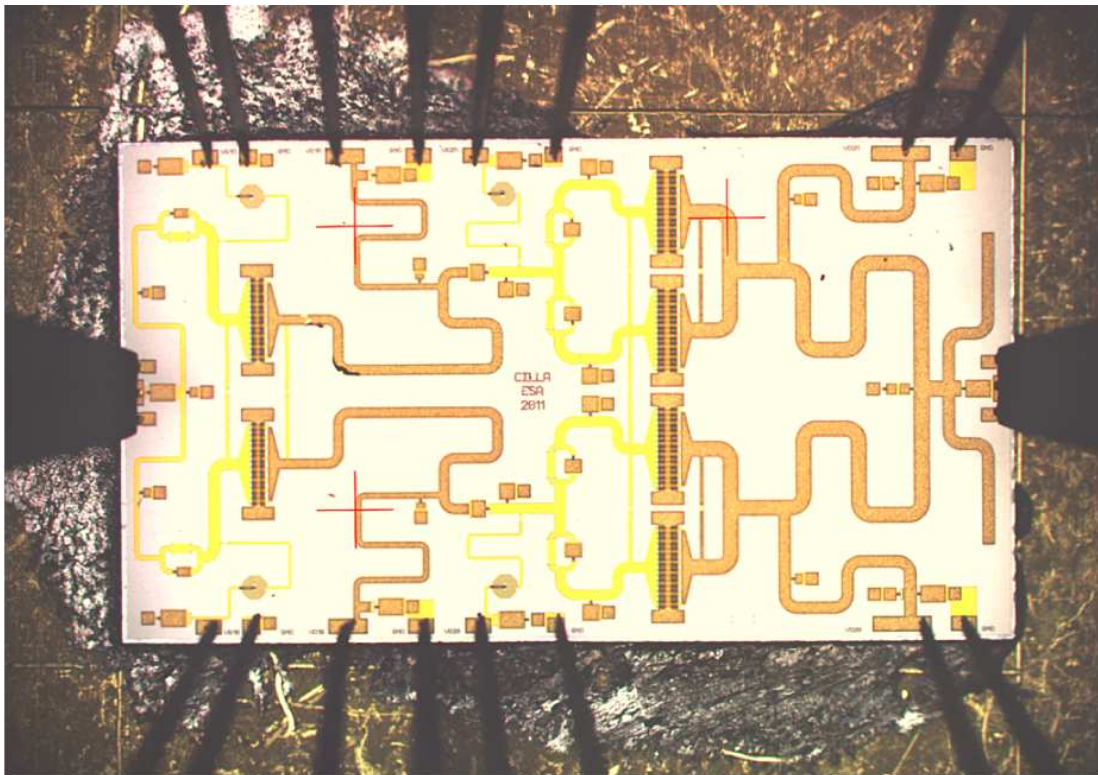


Figure B.4 – MMIC mounted over CuMo carrier and probed



# Appendix C

## MMIC High Power Measurements

### Pulsed frequency sweep measurements

Figures C.1 to C.8 show measured PAE, Gain and Output Power along the frequency band 4.8 to 6GHz using constant source available power and 100MHz as frequency step. Figures C.9 to C.19 present measurements along the frequency band 4.5 to 6.1GHz using constant available power at the source and 50MHz as frequency step. The number of sampled points is double than in the case of Figures C.1 to C.8. Furthermore, the smaller scales used in the axis allow more accurate readings of the output power and gain levels.

Figure C.16 presents data around 2dB compression point, showing that in the frequency range from 4.85GHz to 5.15GHz the output power is 46.9dBm +/- 0.1dB. This corresponds to a 0.2dB bandwidth of 300MHz. PAE varies between 50%-55% along all this frequency range, as shown in Figure C.7. Figure C.8 presents maximum PAE performance achieved around 4.9GHz when operating around 3dB compression point.

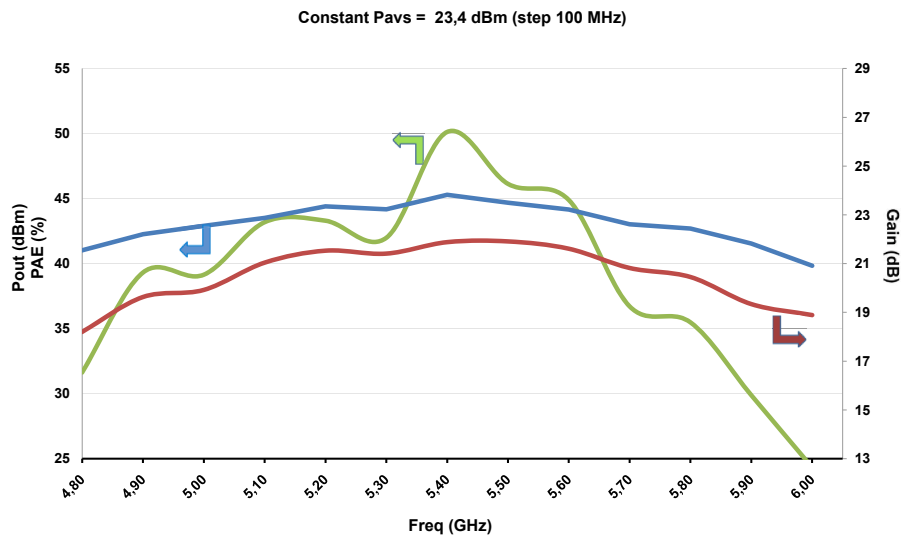


Figure C.1 – Measured performance during a frequency sweep with constant Pavs=23.4dBm

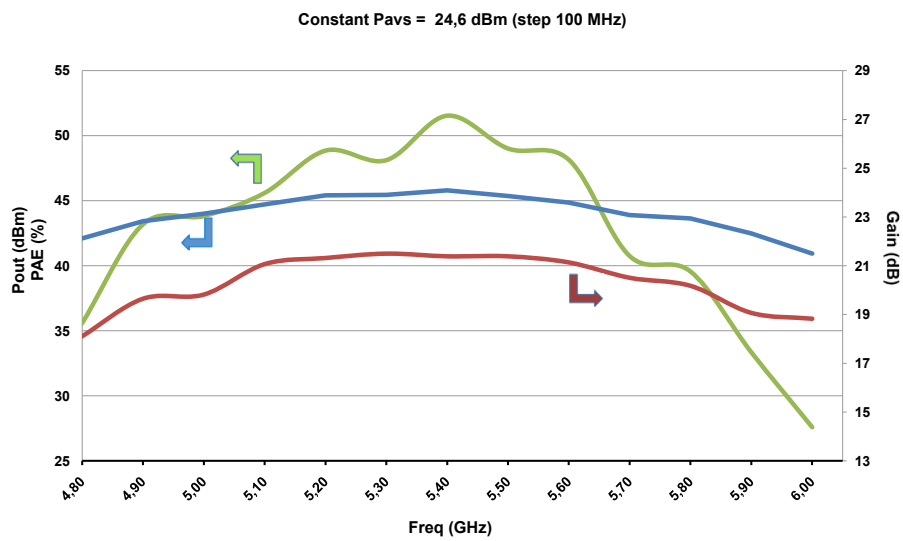


Figure C.2 – Measured performance during a frequency sweep with constant Pavs=24.6dBm

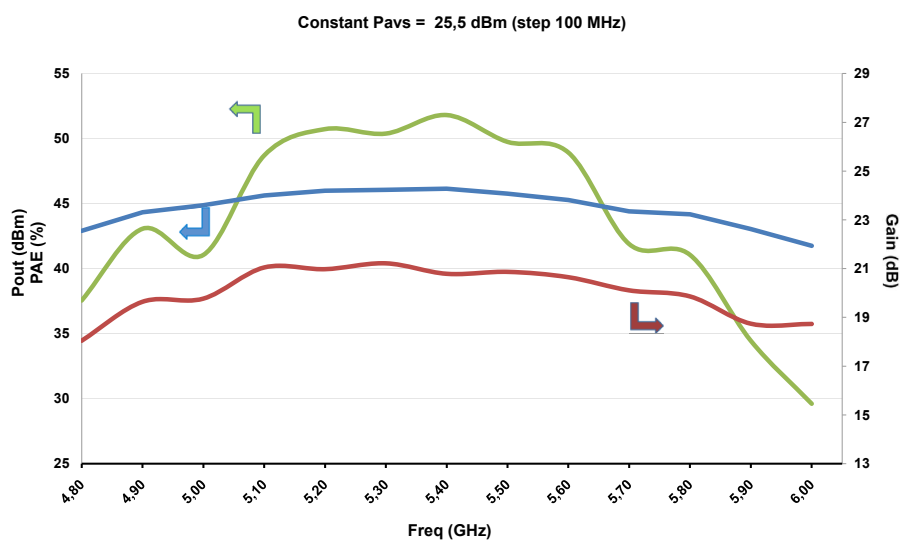


Figure C.3 – Measured performance during a frequency sweep with constant Pavs=25.5dBm

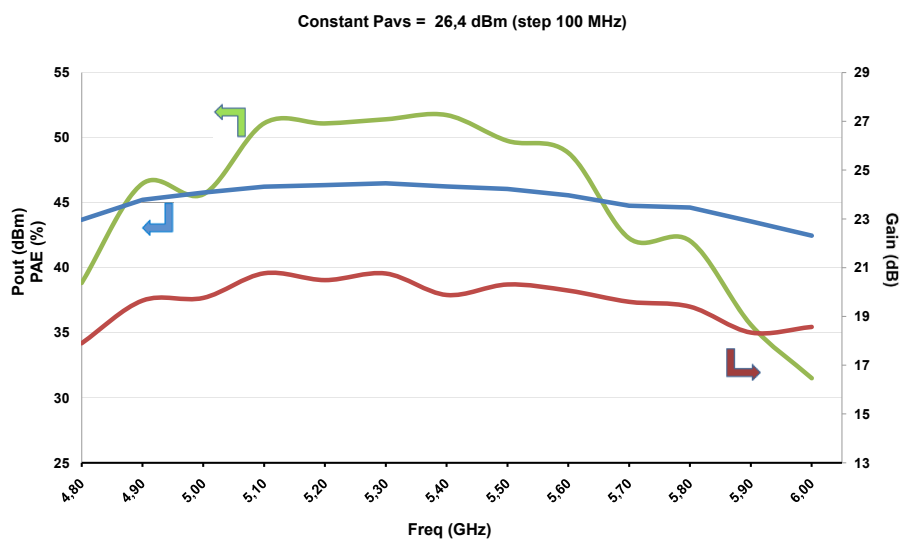


Figure C.4 – Measured performance during a frequency sweep with constant Pavs=26.4dBm



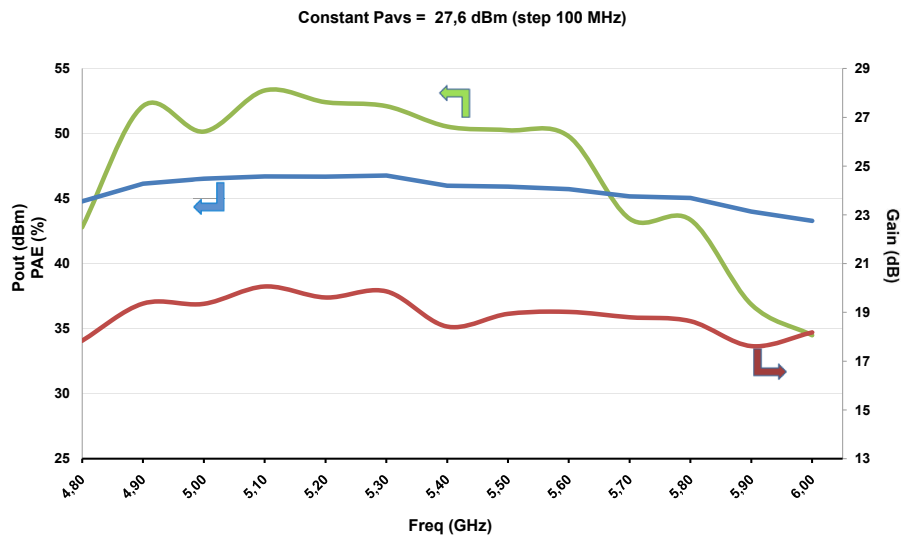


Figure C.5 – Measured performance during a frequency sweep with constant Pavs=27.6dBm

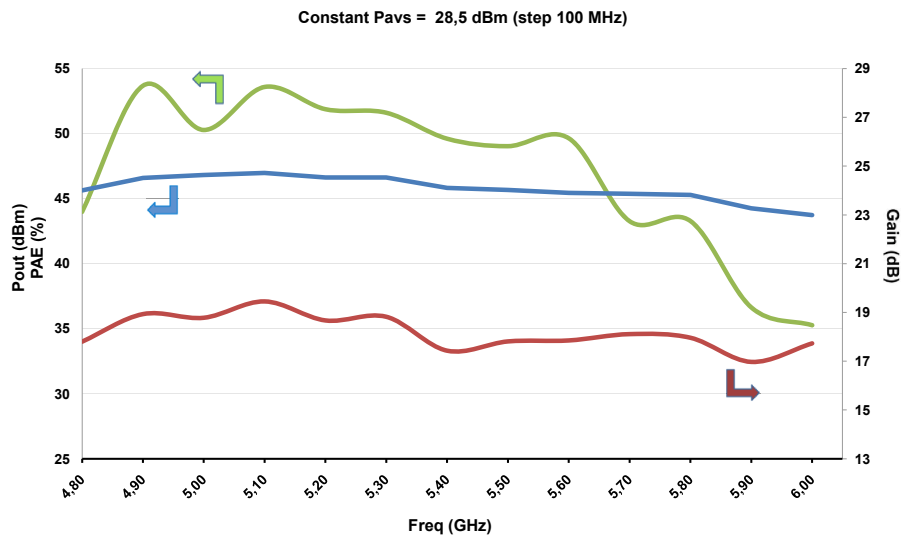


Figure C.6 – Measured performance during a frequency sweep with constant Pavs=28.5dBm



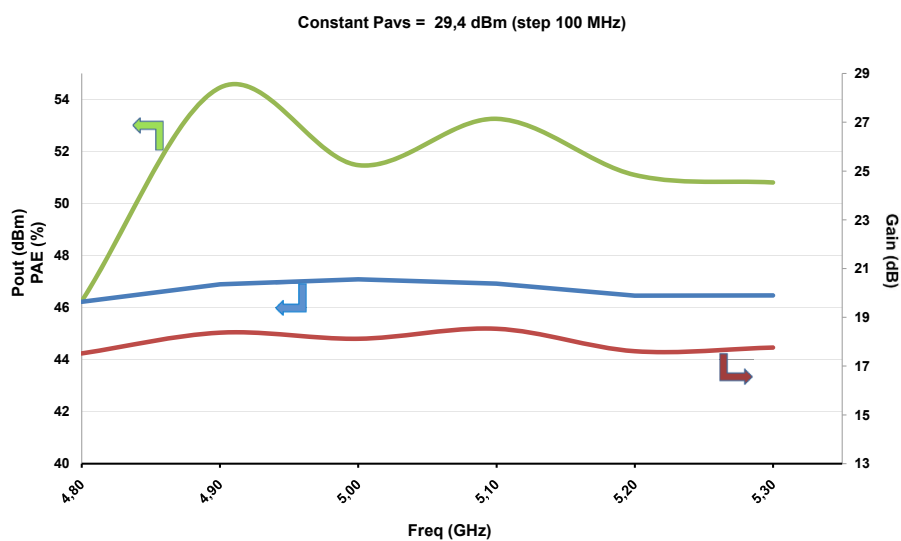


Figure C.7 – Measured performance during a frequency sweep with constant Pavs=29.4dBm

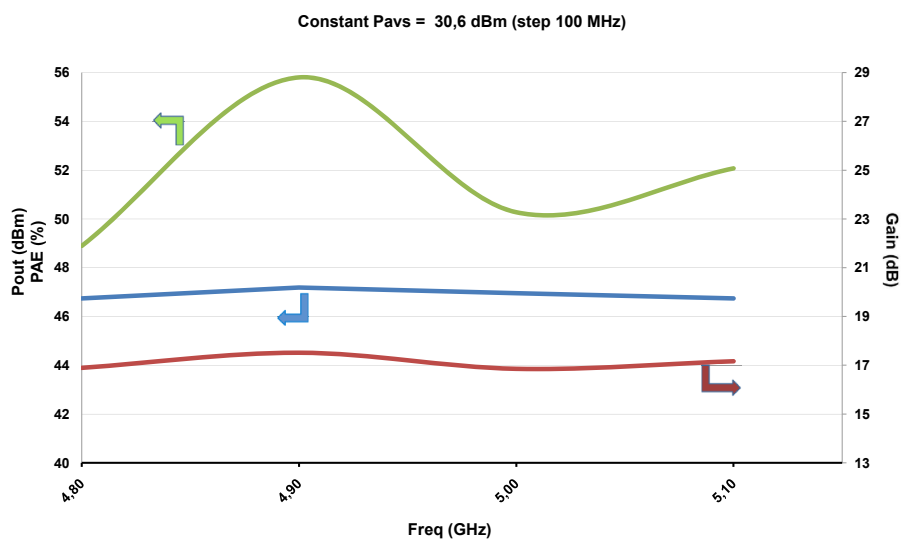


Figure C.8 – Measured performance during a frequency sweep with constant Pavs=30.6dBm

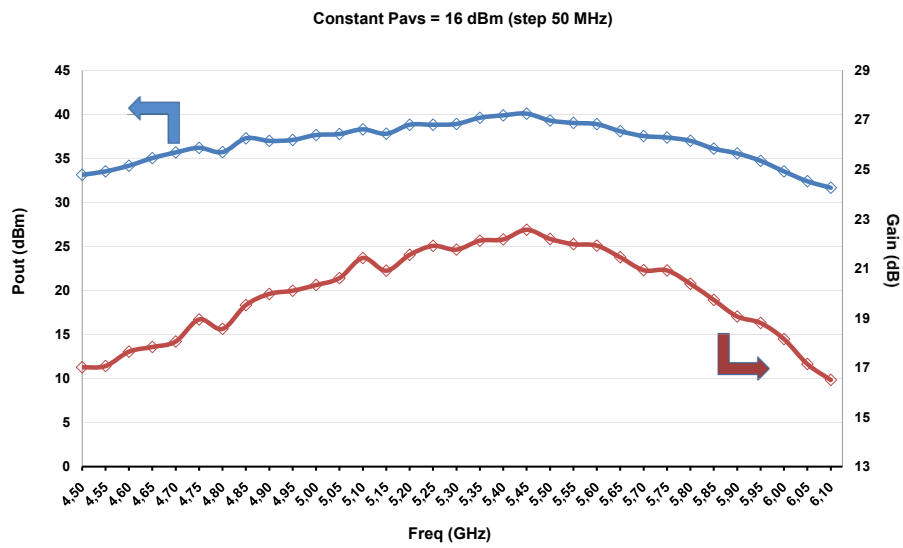


Figure C.9 – Pout and Gain during a frequency sweep using constant Pavs=16dBm

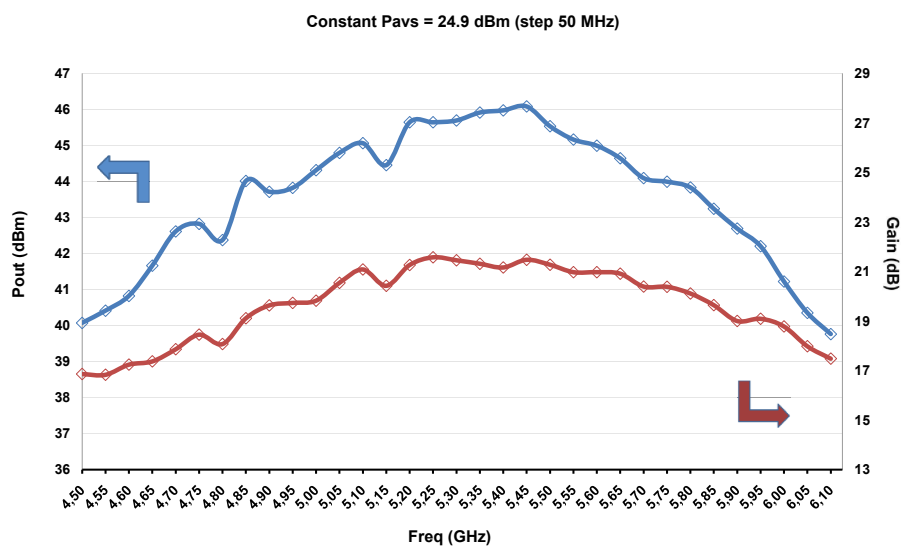


Figure C.10 – Pout and Gain during a frequency sweep using constant Pavs=24.9dBm

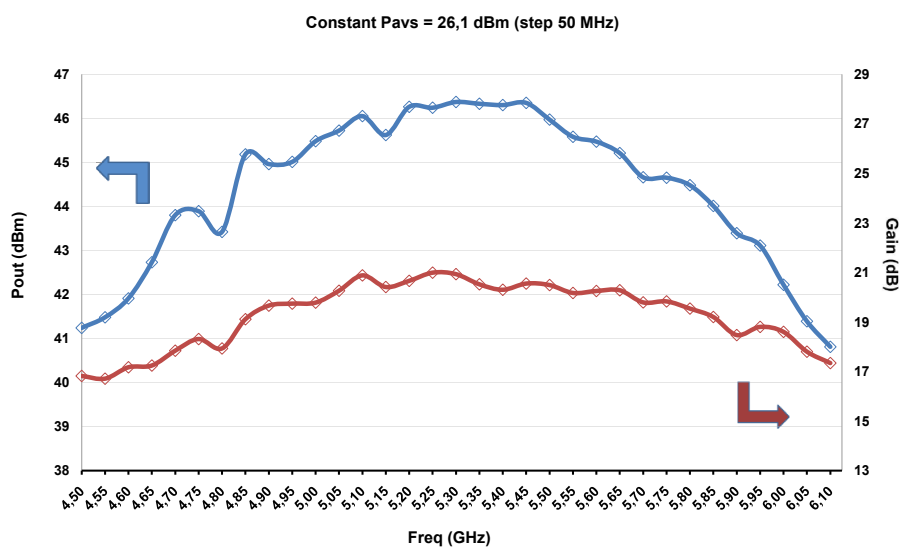


Figure C.11 – Pout and Gain during a frequency sweep using constant Pavs=26.1dBm

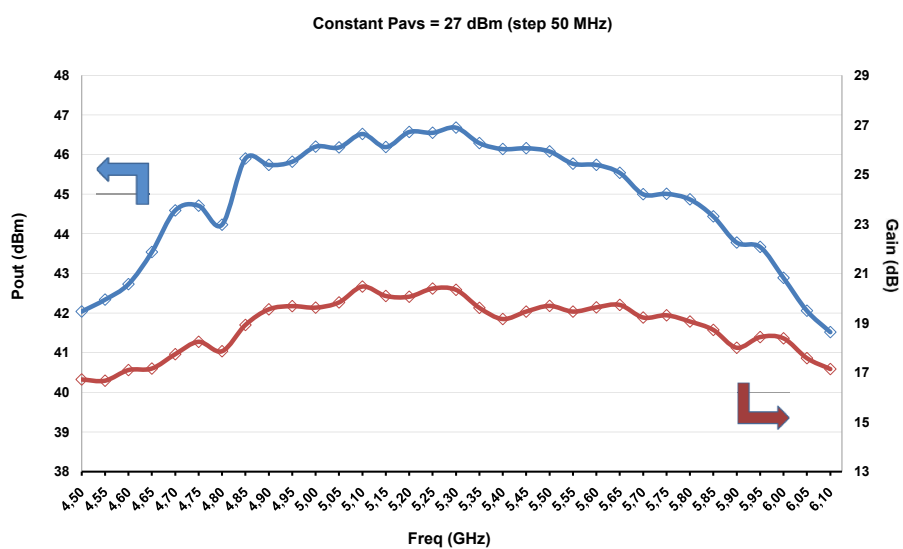


Figure C.12 – Pout and Gain during a frequency sweep using constant Pavs=27dBm

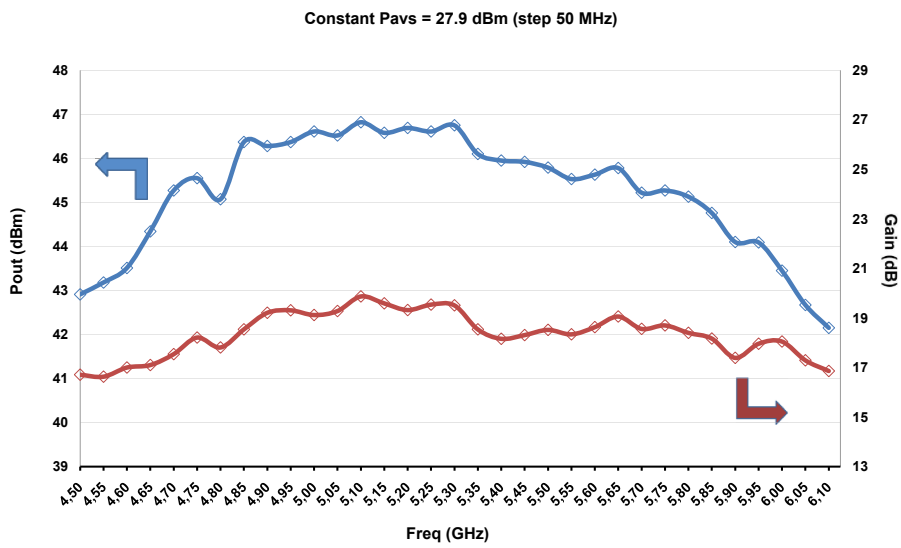


Figure C.13 – Pout and Gain during a frequency sweep using constant Pavs=27.9dBm

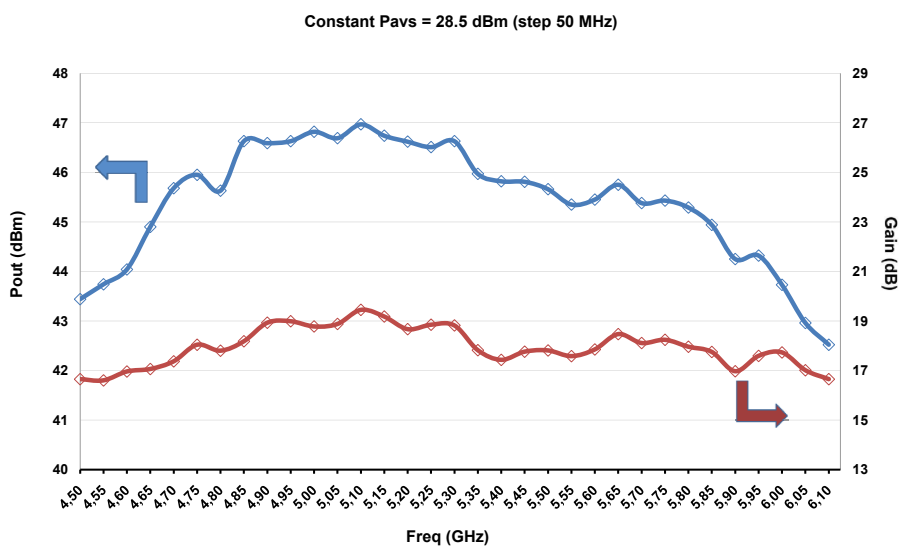


Figure C.14 – Pout and Gain during a frequency sweep using constant Pavs=28.5dBm

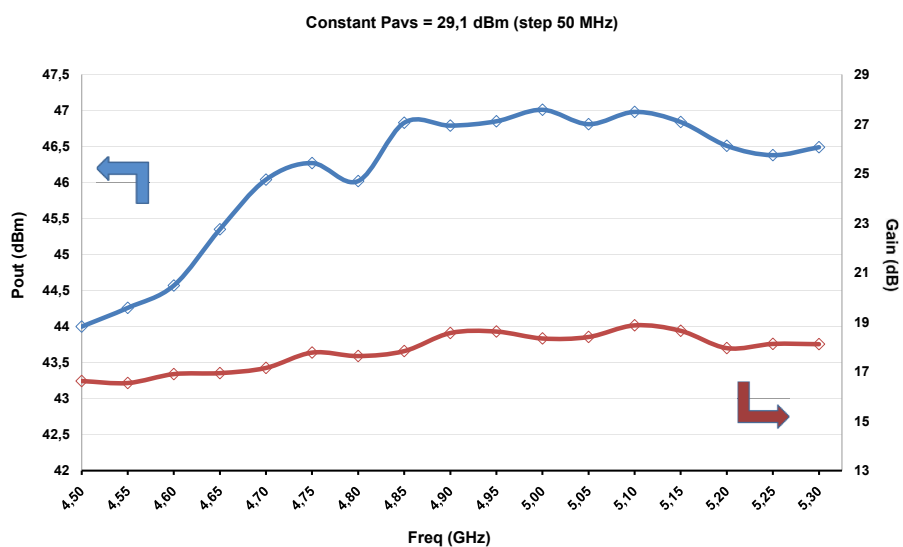


Figure C.15 – Pout and Gain during a frequency sweep using constant Pavs=29.1dBm

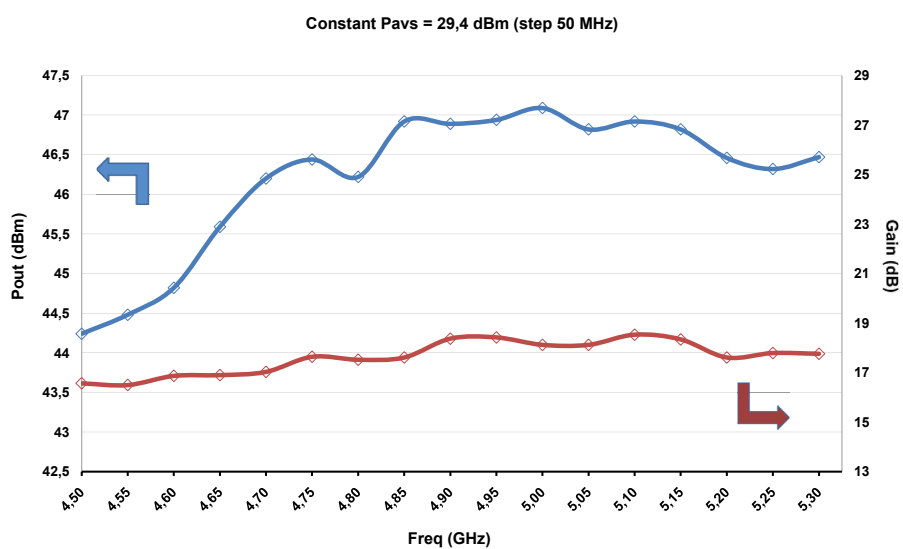


Figure C.16 – Pout and Gain during a frequency sweep using constant Pavs=29.4dBm

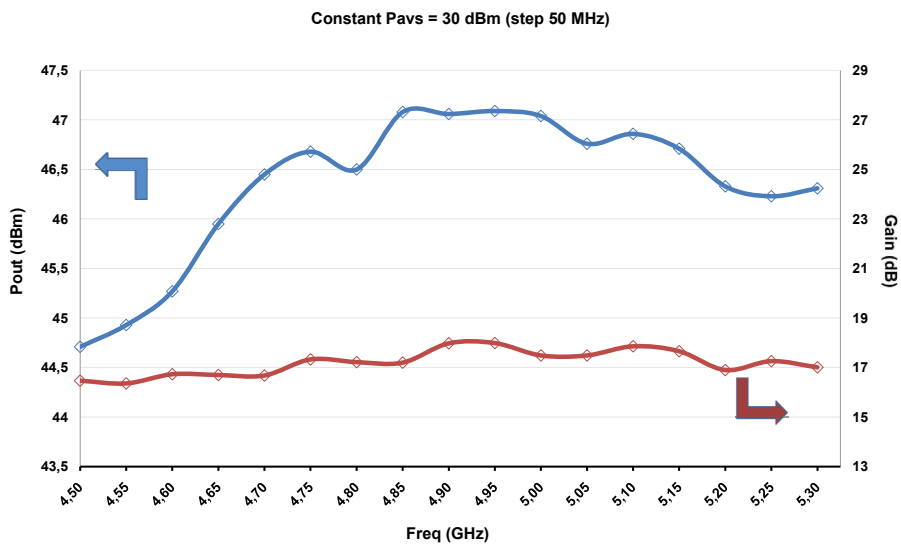


Figure C.17 – Pout and Gain during a frequency sweep using constant Pavs=30dBm

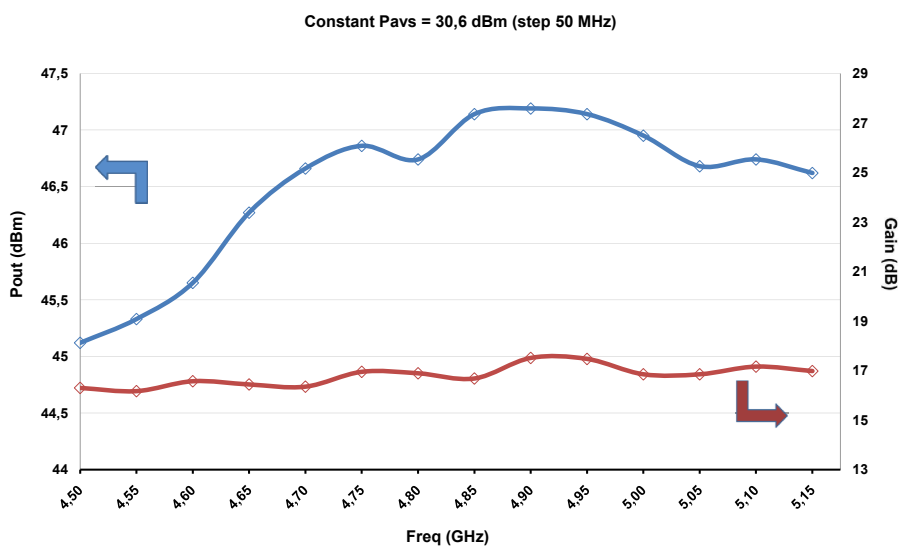


Figure C.18 – Pout and Gain during a frequency sweep using constant Pavs=30.6dBm

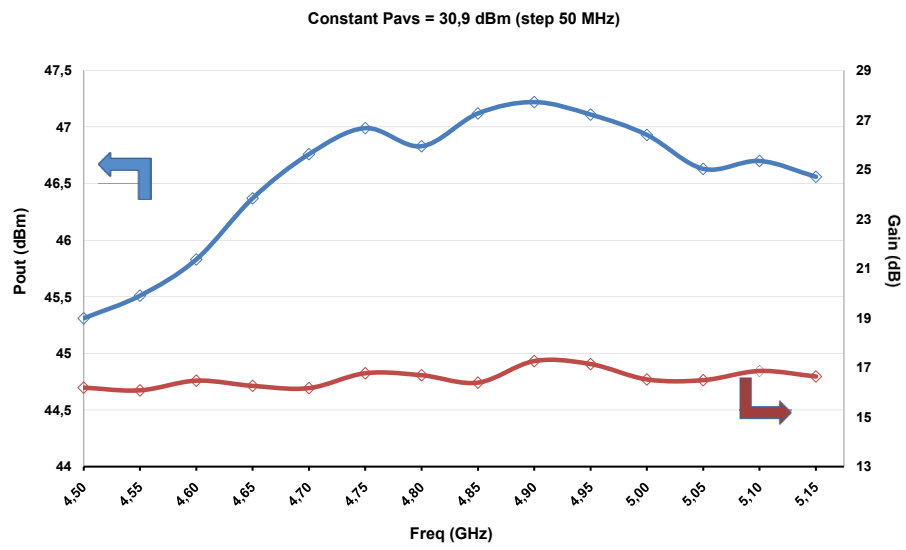


Figure C.19 – Pout and Gain during a frequency sweep using constant Pavs=30.9dBm





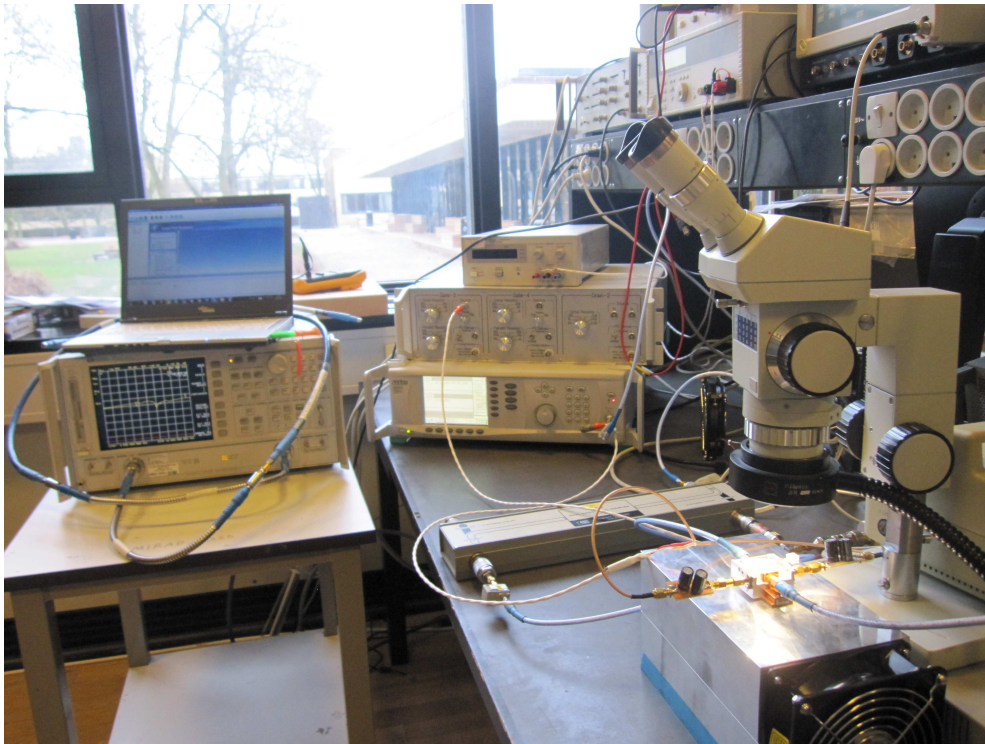
# Appendix D

## X-band Hybrid HPA test campaign photos

This appendix presents photos of the GaN X-band Hybrid HPA, and the test bed that was build during the final measurement campaign at DTU.



**Figure D.1** – Test bed prepared at DTU



**Figure D.2** – Test bed for Hybrid test campaign

# Appendix E

## Publications Attached

The papers that I have written during the PhD time frame are listed below. Furthermore, two journal publications, based on the work presented in this dissertation, are under preparation.

- **40 W C-band GaN MMIC High Power Amplifier for Next Generation of Sentinel Satellites**, C.Cilla, N.Le Gallou, A.Chowdhary and J.Castelein, 6<sup>th</sup> Space Agency MOD Round Table Workshop on Wide Bandgap Semiconductors and Components, ESA 2012. (Appendix E p.130)
- **Bondwire Array Modeling for the Design of Hybrid High Power Amplifiers above C-band**, C.Cilla, S.Jonasson, J.Hanberg, Asia Pacific Microwave Conference 2012. (Appendix E p.137)
- **POLARIS: ESA's Airborne Ice Sounding Radar Front-End Design, Performance Assessment and First Results**, C. Cilla, V.Krozer, J.Vidkjær and J.Dall, International Microwave Symposium 2009. (Appendix E p.140)
- **High Power High Efficiency Amplifiers for P-Band in LDMOS, GaAs and GaN Technology**, V.Krozer, J.Vidkjær, D.Hadziabdic, C.Cilla Hernandez, N. Le Galou, European Space Agency Workshop on Advanced RF Sensors and Remote Sensing Instruments, ESA 2009. (Appendix E p.144)

## 40 W C-band GaN MMIC High Power Amplifier for Next Generation of Sentinel Satellites

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### ABSTRACT

The paper describes the design and experimental performance assessment of a Solid State C-band High Power Amplifier (HPA) using European MMIC GaN technology from United Monolithic Semiconductors (UMS). The design will be used as a baseline for future developments of the next generation of Sentinel satellite T/R modules.

The two stages MMIC HPA features a 6730 X 3750  $\mu\text{m}^2$  compact footprint. The driver stage comprises two 16X100  $\mu\text{m}$  cells, and the output stage four 16X150  $\mu\text{m}$  cells in parallel. The transistors use  $V_{\text{dd}}=30\text{V}$  and low quiescent current biasing conditions. The overlapping between simulated drain current and voltage waveforms is minimized, thus providing good power added efficiency.

The MMIC has been fabricated at the UMS foundry using an early revision of their process GH25, which currently is under final development. It uses 0,25  $\mu\text{m}$  gate length and is intended for MMIC design up to 20GHz. Preliminary on-wafer pulsed measurements show output power levels in the order of 36-40W with associated 46,7% overall two stages PAE and 21,6 dB large signal Gain at 5,4 GHz. These results are in good agreement with the simulated values.

### INTRODUCTION

The current Sentinel satellite T/R module configuration consists of two 5610 x 4510  $\mu\text{m}^2$  paralleled 11W GaAs MMICs with PAE=36.9%. This power level is close to the technological limit of GaAs for a single chip. ESA plans to implement a new calibration mode for a next generation of Sentinel that requires reducing 10% of the receiving window, therefore degrading the SNR. In order to maintain the resolution, one possible solution is to increase the transmitted power to 40W. Two solutions are foreseen: the first one consists on parallel four 11W GaAs transistors. But the losses in the combining structure (0.4-0.6dB) would reduce the overall PAE to 31% while delivering 38W. There would also be an increased risk of malfunction due to imbalances between the parallel stages and increased spreads created by the bondwire arrays and transitions. The second option is to use the benefits of GaN technology to design a more compact and efficient 40W MMIC using a single chip as it will be described within this paper.

The C-band MMIC presented in this work has been fabricated at the UMS foundry using an early revision (iteration 1) of their process GH25, which currently is under final development. It uses 0,25  $\mu\text{m}$  gate length and is intended for MMIC design up to 20GHz. A practical realization of the MMIC is shown in Fig.1.

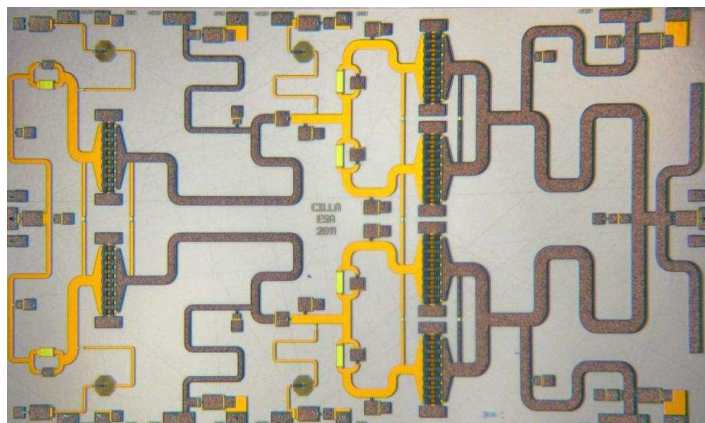


Fig.1. C-band MMIC HPA (6730 X 3750  $\mu\text{m}^2$ )

The frequency of operation is just at the border between the recommended applications for the UMS technologies GH50 and GH25. The latter will be used since it allows the design of MMICs, while GH50 is only for discrete power bars. Designing in the lower frequency range of the process implies the need of a relatively large MMIC area and also the need of lumped components with values close to the maximum ones available for this process.

### MMIC DESIGN PROCESS

The design approach comprises: feasibility assessment, small and large signal transistor model validation using load pull measurements, selection of the MMIC topology (number of stages, cell sizes), selection of biasing point and class of operation, design using the validated nonlinear model in a harmonic balance simulator, stability analysis, matching network synthesis, passive components 3D EM simulation and spreads evaluation.

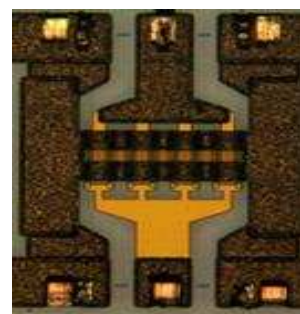


Fig.2. GaN transistor cell

The specifications require central frequency of operation at 5.4 GHz, total output power between 35-40W, PAE > 45% and 150 degrees maximum junction temperature when using a baseplate temperature of 80 degrees.

### Feasibility assessment

The first step was to evaluate the performance of the technology. An on-wafer isothermal load-pull measurement campaign was performed over a small  $8 \times 75 \mu\text{m}$  v1s transistor cell, similar to the one shown in Fig. 2. The data in Fig.3 show measurements at constant 3dB compression, where the load impedance is swept at the fundamental frequency, while the 2nd and 3rd harmonic impedances are kept fixed to an optimal value. The measurements were performed with the chunk at 40 degrees and the selected biasing point is  $V_{\text{dd}}=30\text{V}$  and  $I_{\text{dd}}=13.5\text{mA}$  (22 mA/mm). Fig.3a shows the contours for PAE, while Fig.3b shows output power contours. Power densities up to 6W/mm and maximum PAE of 68% were measured at 5.4GHz. This information was useful to select the total gate periphery needed to meet the specs. The foundry reported power levels up to 6.6 W/mm, but they recommend operating close to 4W/mm.

### Small and large signal model validation

Two nonlinear models for this technology were provided through the project. One developed by the University of Bologna (UNIBO) for the version v1s of the GH25 transistors and other one from UMS for the v3s version. The model validation campaign included both small/large signal measurements, thermally controlled for a  $8 \times 75 \mu\text{m}$  v1s cell. Fig.4 presents a comparison of the measured and simulated small signal parameters for  $8 \times 75 \mu\text{m}$  v1s transistor cell at  $V_{\text{ds}}=30\text{V}$  and  $I_{\text{ds}}=30\text{mA}$ . Good agreement is observed, especially if we look at the input and output impedance levels, while there is a small difference in the gain of less than 1dB. The experience shows that the most important for a model is to present a good agreement in the impedance levels.

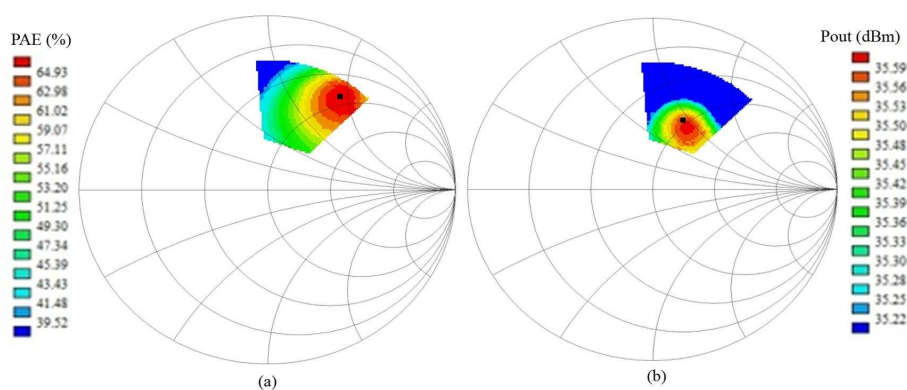


Fig.3. Fundamental impedance load pull for  $8 \times 75 \mu\text{m}$  V1S with 2nd and 3rd harmonic fixed. (a) Measured PAE showing PAE max. 68%. (b) Measured Pout showing Pout max. 35.65 dBm which corresponds to 6 W/m.



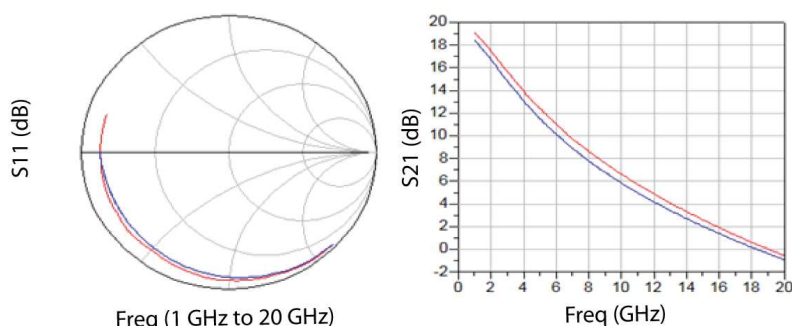


Fig.4. Measured (red) vs. simulated (blue) small signal S-parameters for  $8 \times 75 \mu\text{m}$  v1s transistor cell at  $V_{\text{ds}}=30\text{V}$  and  $I_{\text{ds}}=30\text{mA}$

A load pull test bed was installed in the in the RF Payload Systems Division Laboratory at ESTEC, to validate the large signal models and also select the optimal load and source impedances for the transistors in order to achieve maximum PAE. This was done by tuning both at fundamental and at harmonic frequencies the load impedance.

Fig.5a shows a comparison of the location in the Smith chart of the load delivering the highest output power during measurements (circle) and in the simulations (diamond), while Fig.5b compares the location of the load delivering best PAE during measurements (circle) and in the simulations (diamond). A good match is observed, especially for the location of the maximum power.

Based on these measurements the fundamental and 2nd harmonic loads providing the best PAE performance were selected for the final design.

#### Selection of MMIC topology and class of operation

The MMIC footprint was constrained by the foundry to  $6730 \times 3750 \mu\text{m}^2$ , since the design was part of a multi-project wafer run. Two stages were selected to achieve more than 20dB power gain. The driver stage comprises two  $16 \times 100 \mu\text{m}$  cells, and the output stage four  $16 \times 150 \mu\text{m}$  cells in parallel. The size of the cells at the output stage was selected to deliver 40W being operated at  $5.2\text{W}/\text{mm}$  and, at the same time, to fit physically in the vertical direction given tile size. The power density level is higher than the  $4\text{W}/\text{mm}$  recommended by the foundry, but there was not enough physical space for using more cells in parallel, and measurements demonstrated that this technology is able to deliver such power level densities. The transistors use  $V_{\text{dd}}=30\text{V}$  and  $I_{\text{dd}}=22 \text{mA}/\text{mm}$  biasing conditions.

Fig.6 shows the waveforms at the intrinsic interface to the transistor drain that are obtained from a HB simulation. A quasi semi sinusoidal voltage and a square-like current curve can be observed. These waveforms, tending towards  $F^{-1}$  class, explain the good efficiencies obtained in the simulations, since the overlapping between voltage and current at the drain is avoided as much as possible.

Junction temperature spec. has been identified as one of the challenges in future space based GaN high power amplifier implementation, due to the high power densities of the devices. In order to fulfill this requirement, a proper die attach and a design with very high efficiency is required. Thermal calculations for the  $16 \times 150 \mu\text{m}$  cell were also performed to ensure a maximum derated junction temperature of 150 degrees, following the demands for space applications. The calculations assume that the device is mounted on a CuMo carrier ( $2, 5 \times 1, 5 \text{cm}$ ) of 1mm thickness, using  $50 \mu\text{m}$  thick AuSn 80/20 solder perform, and using 80 degrees as baseplate temperature.

#### Matching networks synthesis

After validating the nonlinear model for the  $8 \times 75 \mu\text{m}$  v1s cell, scaling was required in order to choose the impedances for the larger cells used in the MMIC. The matching and biasing networks were designed to synthesize the optimal impedances while keeping attention to other requirements. The major challenge in the design was to match the low impedance levels at the same time at  $f_0$  and  $2f_0$ , while trying to get as much bandwidth as possible. Fig.7 illustrates the synthesized impedance by the output matching network (red curve) and the PAE load pull contours for the  $16 \times 150 \mu\text{m}$  cell, both at fundamental frequency and at 2nd harmonic frequency.

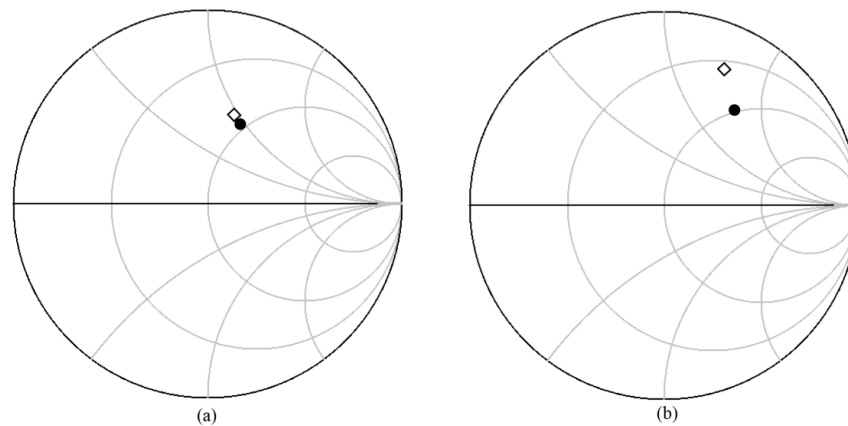


Fig.5. Comparison of load pull measurements (circles) vs. simulations (diamonds) for  $8 \times 75 \mu\text{m}$  V1s cell.  
(a) Load providing maximum  $P_{\text{out}}=35.65$  dBm (b) Load providing maximum PAE=68%

### Output Matching Network

The output matching network presents asymmetry around the centre axis and synthesizes the load at fundamental  $f_0$  and second harmonic  $2f_0$  that provides optimal PAE. In this design, it was decided not to take into account the third harmonic  $3f_0$  impedance, since there was a limited space available and the structure needed was also introducing extra losses that were hindering the improvement in efficiency. Furthermore, the simulations show that controlling the third harmonic impedance was providing only a 2-3% improvement in efficiency. Focus was placed in providing enough bandwidth at  $f_0$ , but also at  $2f_0$ . The biasing network was actually the critical structure in the design limiting the bandwidth due to its resonant-like behaviour.

The insertion losses of the output network were controlled carefully, since they reduce the efficiency dramatically. It is very important to understand the different mechanisms generating losses: finite conductivity, parasitic in lumped components, losses in the dielectric materials and RF Power leakage through the biasing lines. Losses  $< 0.6$  dB were achieved.

### Inter-stage Matching Network

The inter-stage matching network was designed with focus on matching the gates of the output stage transistors with the impedance needed to transfer as much power as possible from the driver to the output stage and at the same time load the output of the driver stage with the correct impedance. The driver is working in a relative linear region, at least 3 dB under the 1 dB compression point, and the impedance selected is the optimal one to ensure that the driver is providing maximum PAE at this point of operation.

The low frequency gain was controlled with the use of a parallel RC structure. This high pass network kills the large gain of the transistors at lower frequencies avoiding low frequency oscillations, and it helps to compensate the device gain roll-off maintaining the gain flat across the bandwidth of the design. There is a compromise between the maximum gain provided by the MMIC and the improvement in stability that is controlled by the values of the RC network.

### Input Matching Network

The input matching network has a small bandwidth due to the limited chip area available in the wafer. It was designed to insert as much power as possible into the MMIC, and at the same time control the stability.

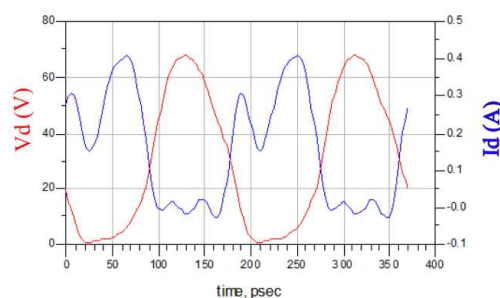


Fig.6. V/I waveforms from HB simulation at the intrinsic drain interface under optimal loading conditions.

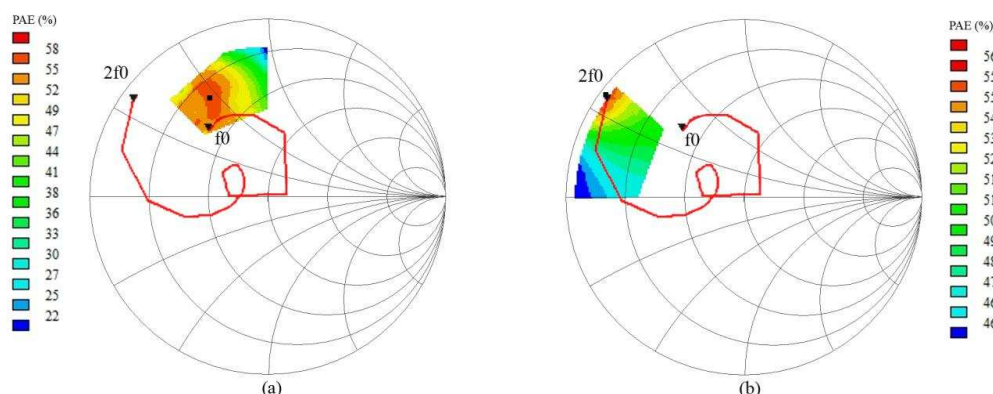


Fig.7 Synthesized output impedance (red curve) and load pull contours showing PAE contours for the 16x150 $\mu$ m cell (a) at fundamental frequency  $f_0$  (b) at 2<sup>nd</sup> harmonic frequency  $2f_0$ .

The MMIC gain was designed to be flat across our bandwidth, compensating the gain slopes of the active components with engineered slopes for the insertion and reflection losses for both the input and inter-stage matching networks.

#### Full MMIC Harmonic Balance simulations

The nonlinear model was used together with the synthesized matching networks to perform Harmonic Balance simulations (HB) using ADS. The results from a nonlinear simulation showing a power sweep for the full MMIC design at 5.4GHz are presented in Fig.9. On the other hand, Fig.10 presents the overall two stages PAE, output power, and transducer gain for a frequency sweep at constant input power  $P_{avs}=24\text{dBm}$  (close to 6dB compression). As it can be seen, the bandwidth is simulated to be 450MHz (5.1-5.55 GHz) for a gain variation of less than 0.5dB (22-22.5dB), with corresponding output power of more than 40W (46-46.5dBm), and a PAE variation of less than 3pts (38% to 41%). The results are based on 2.5D full-wave electromagnetic simulations (Momentum) of the matching networks and the stack of layers for the GH25 process provided by UMS. The 3D drawing of the output matching network is illustrated in Fig.8.

Both small and large signal stability analysis were performed. The small signal or linear stability analysis included an investigation of the stability circles and the traditional Rollets factor. But this is certainly not enough, mainly because the method does not guarantee the internal stability of the circuit. The large signal stability covers even and odd mode internal stability analysis, and is based on the introduction of a single- and multiple small perturbations in different internal nodes of the design (Floquet Multipliers [1]). A Harmonic balanced simulation using mixer mode was performed using ADS and afterwards the poles and zeros of the transfer function were identified using the CAD tool STAN ([2],[3]). Stabilization resistors between drains and sources were used in order to avoid odd mode oscillations. Harmonic Balance simulations using Monte Carlo analysis were performed using the spreads provided by the foundry and changing the loading impedance at the DC biasing ports. The spreads were shifting the response in frequency and degrading the performance, but their influence was minimized when the device was operating under high compression conditions.

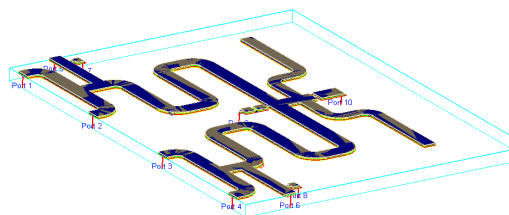


Fig.8 Output matching network drawing in 3D EM simulator



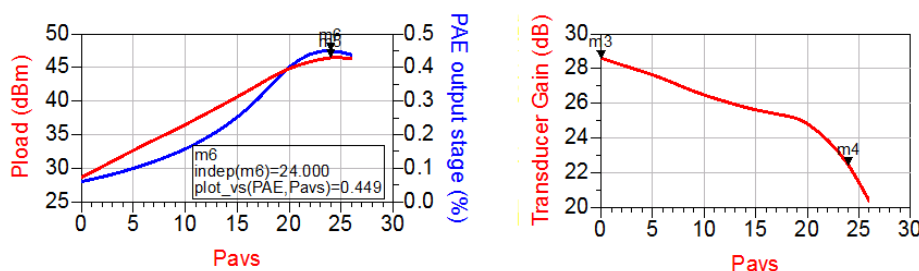


Fig.9 Simulation of full MMIC power sweep at 5.4GHz using nonlinear model.

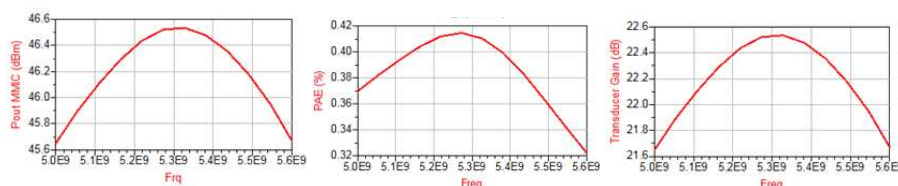


Fig.10 Simulation of full MMIC frequency sweep at Pavs=24dBm (6dBcomp) using nonlinear model.

## PRELIMINARY MEASUREMENTS

On-wafer preliminary measurements under pulsed conditions were performed over three different devices, sweeping the available power at the input up to 24dBm and the frequency from 5 to 5.8 GHz. The RF test used a 25 us short pulse and 10% duty cycle. The MMIC was DC biased under the same conditions that were used during the simulations and the load pull validation measurements (22-25 mA/mm).

The data in Fig.11 and 12 show maximum measured power levels around 36 W, with 46,7 % overall two stages PAE and 21,6 dB transducer gain. The three devices that have been measured show similar performance, and a relatively close agreement between simulated and experimental results is observed when comparing Fig.10 and Fig.11. A junction temperature of 140 degrees is obtained when using the measured data as inputs for the calculations under the mounting conditions specified previously in this paper. It is important to emphasize that the devices were not pushed into compression during the preliminary measurements, so it will be possible to get better performance during the final measurements. The results from the final test campaign, with the MMIC properly attached to a CuMo carrier, will be presented at the workshop.

## CONCLUSIONS

The design process of a compact 40W GaN High Power Amplifier has been presented.

The amplifier fulfills the specifications regarding power (36-40W), gain (21.6 dB) and efficiency (46.7%). Wider bandwidths are also possible at the expense of footprint space and/or trade-off in maximum output power and efficiency.

Fulfilling the derated junction temperature for GaN technology in power amplifier applications is the main challenge for space applications. In this work, the calculated junction temperature is kept under 150 degrees for a reference baseplate temperature of 80 degrees. The capability of operation within the space radiation environment is being investigated but is expected to be sufficient [4].

The final measurements related to dice MMIC test campaign will be discussed during the workshop presentation.

Overall an improvement of >15% in PAE has been measured in comparison with a solution of four GaAs MMIC combined in parallel, while the output power levels are similar. Furthermore, the footprint size is around 25 mm<sup>2</sup> both for the GaN design presented here and for the current Sentinel individual GaAs MMIC solution, thus leading to a considerable reduction in chip area by a factor of four or more if we consider the external power divider and combiners required to combine 4 GaAs MMIC chips.

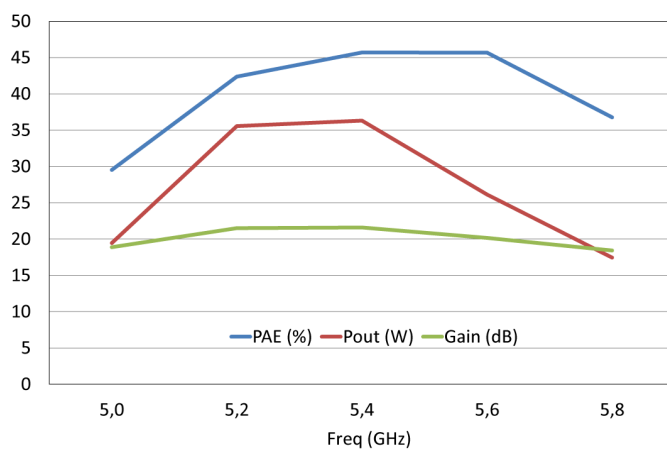


Fig. 11 C-band MMIC frequency sweep measurements at Pavs=24dBm (device S8)

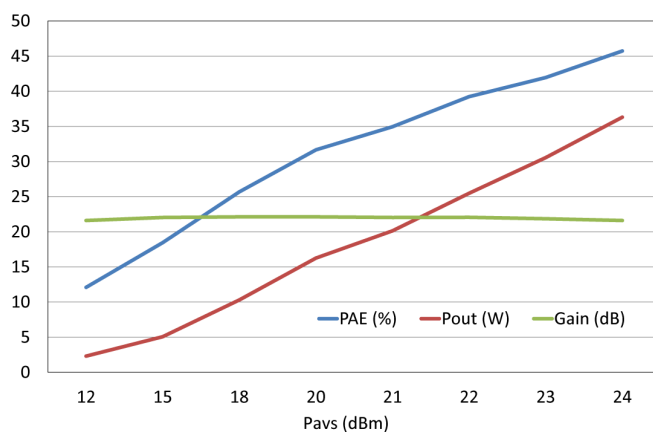


Fig. 12 C-band MMIC power sweep measurements at 5.4 GHz (device S8)

#### ACKNOWLEDGEMENT

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## Bondwire Array Modeling for the Design of Hybrid High Power Amplifiers above C-band

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**Abstract** — This paper presents a bondwire array model obtained using a software based on the finite elements method and validated up to 15 GHz by measurements over a purpose-build array structure. This work addresses the limits of the inductor-based bondwire model when used at frequencies above C-band to simulate the large bondwire arrays that are used in long multi-transistor power bars. The usefulness of an accurate 3D EM model during the amplifier's matching network design process is highlighted using a practical example, and the effect of the insertion loss variations along the different bondwires comprising the array on the hybrid performance is discussed.

**Index Terms** — High power amplifier, Hybrid integrated circuits, Integrated circuit packaging, Power transistors, Semiconductor device packaging, Wafer bonding.

### I. INTRODUCTION

Bondwire arrays are extensively used in electronic packaging and to interconnect microwave components. An example of this is the electrical connection provided between the power bar die, comprising several transistor cells in parallel, and the external matching structures.

Lately, there has been a renewed interest in high power amplifier design thanks, to a large extent, to the development of GaN semiconductor technology that is already having an important impact into the wireless and radar market. At frequencies below 6GHz, it is typical to find hybrid packaged transistor power bars with prematched structures like MOS capacitors and bondwire arrays connecting to the package flange.

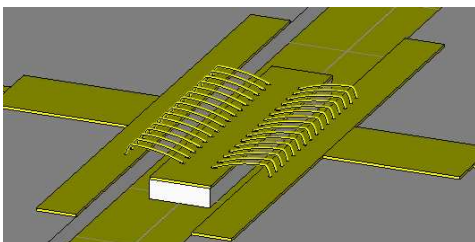


Fig. 1. Drawing of the fabricated bondwire structure using full wave simulation CAD

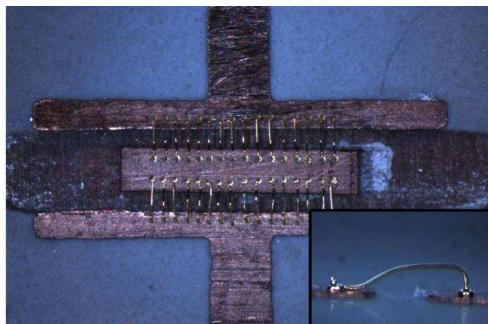


Fig. 2. Fabricated structure with two, 16 bondwire arrays in parallel. A close-up of a bondwire is illustrated in the lower right corner.

At frequencies above 6 GHz, MMIC solutions dominate the market, and it is challenging to find hybrid solutions, since the package and bondwire parasitics become increasingly important at sizes comparable to the operating wavelength.

Hybrid solutions above C-band have two main advantages that make them worth further investigation: the reduction in semiconductor area needed, therefore reducing drastically the final cost, and the possibility of implementing the external matching and biasing networks on very low loss substrates, thus improving output power and efficiency capabilities. Alumina substrate has e.g., 10 times lower loss tangent at 10GHz than SiC semiconductor which is the most commonly used substrate for GaN transistors.

Hybrid design above C-band requires a good model of the bondwires and their transition (see Fig. 1), in order to achieve a proper matching and to avoid the need of tuning after manufacturing, if even possible.

Previous research has focused on closed-form equations used to compute self and mutual inductances of the bondwire arrays [1]-[5]. Full wave software simulations of single and double bondwires have also been published. [6], [7].

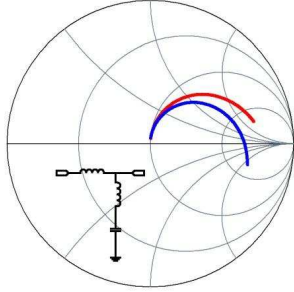


Fig.3. Single bondwire  $S_{11}$ -parameter using ADS inductance-based model (Red) and full wave 3D simulation (Blue) from 1 to 32 GHz. Also shown the lumped equivalent model of the bondwire-to-microstrip transition, which added to the ADS model, would make both curves to match.

In this paper we examine the limitation of the inductor-based bondwire model at frequencies above 6 GHz. Section II presents a comparison between measurements of the fabricated array structure, shown in Fig. 2, and data obtained from a full wave simulation up to 15 GHz. Finally, Section III focuses on the importance of having an accurate bondwire model during the design process of hybrid high power amplifiers.

## II. BONDWIRE MODEL

Traditionally at low frequencies, the bondwire is considered to have an inductive behavior, and it is a good principle to keep it as short as possible. The ADS bondwire array model [3] is based on self and mutual inductance calculations, modeling each bondwire with five segments of a given radius, conductivity, distance from ground plane and separation between adjacent bondwires.

At higher frequencies however, the bondwire-to-microstrip transition becomes significant, and the behavior depends on the permittivity and thickness of the substrate used, the bondwire-to-microstrip connection angle and the distance from the connection point to the substrate edge.

Fig. 3 shows a comparison up to 32 GHz of a single bondwire simulation using the inductor-based ADS model and a simulation using 3D full wave electromagnetic simulation software. Both models match up to around 6GHz, but not at higher frequencies. 3D EM CAD programs like HFSS or CST are efficient with the computers available nowadays, and a good matching between simulation and measurements was verified both for the single bondwire and for more complex structures, as shown in the next section. In Fig.3, a lumped equivalent of the bondwire-to-microstrip transition can be added to the ADS model in order to fit both curves.

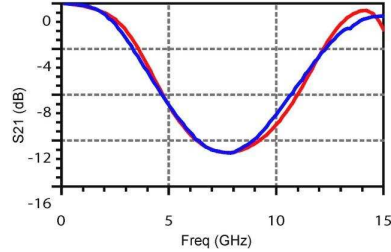


Fig. 4. Comparison between measurement (blue) and full wave electromagnetic simulation (red) of fabricated structure.

## III. BONDWIRE ARRAY: MEASUREMENTS VS SIMULATIONS

Large arrays using many bondwires in parallel are usually found in the large single tabs of the output ports of transistor power bars. The number of bondwires in parallel and the radius are chosen to accommodate properly all the current at the output power stage.

When paralleling bondwires in the same tab as shown in Figs. 1 and 2, the overall parasitic inductance is reduced while the capacitance to ground increases, relative to a single bondwire, due to the paralleling. This makes the full wave 3D modeling even more necessary than in the case of a single bondwire.

Fig. 4. shows good agreement between measurements of the structure shown in Fig. 2 and simulations in Fig. 1, using the finite elements method (FEM) up to 15 GHz. The behavior was also validated using software based on the finite-difference time-domain method (FDTD).

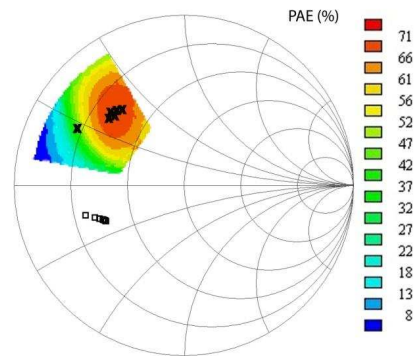


Fig. 5. Load pull data for a single transistor cell showing PAE circles at 9 GHz and synthesized impedances for each one of the 16 cells of a power bar, using the bondwire full wave model (crosses) and the inductor-based model (squares)

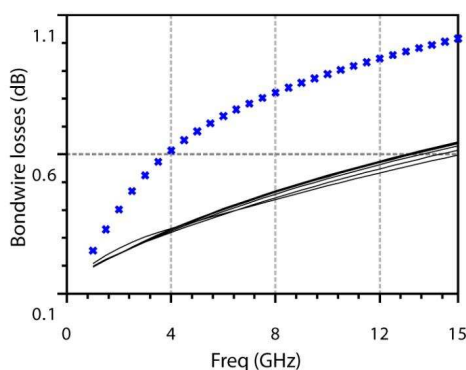


Fig. 6. Losses along the two bondwires at the edges of the array in blue (crosses) and for the other 14 bondwires in black.

#### IV. HOW AN ACCURATE BONDWIRE MODEL IMPROVES THE HYBRID DESIGN PROCESS

The process of designing a hybrid power amplifier using multi-transistor power bars can be greatly improved by the use of the accurate models available nowadays both for the active and passive elements. The first step in the design is to find optimal loading conditions for a single cell performing load and source pull. Fig. 5 shows the Power Added Efficiency (PAE) contours for a given transistor cell operating at 9 GHz, where the red area corresponds to the optimal performance in terms of PAE. Next step is to design the matching networks for the power bar containing several cells in parallel, taking into account that the bondwire array is actually part of the matching structure. Using a multipoint bondwire array model obtained using a full wave solver makes possible to simulate the impedance that each of the cells of the array is loaded with.

When paralleling many cells in a power bar, the impedances to match are typically very low, therefore only narrowband designs are often possible, and it is therefore necessary to be very careful when designing the matching networks.

The crosses in Fig 5 represent the output impedances seen by the individual transistors of a 16 cells power bar at 9 GHz when using the full-wave array model during the matching network design process, and the squares represent the impedance seen when the full-wave array model is substituted by an inductor based one. When looking at the PAE corresponding to both cases, we can conclude that the use of a non accurate model can completely detune the performance of the hybrid design.

There exist also imbalances in the synthesized impedance along the different ports of the bondwire array, partially due to the fact that the two bondwires on the edges of an array only have one neighboring bondwire instead of two. This

modifies the magnetic and electric fields along the array, and therefore the couplings and losses between the different bondwires will also vary along the array. The bondwire losses will also depend on the loading impedance levels when compared with the equivalent characteristic impedance of the bondwire [3].

Fig. 6 corresponds to a simulation showing the variation of the insertion losses along the different bondwires of an array used at the gate of a 16 cells hybrid power transistor. At the gate, these variations in loss-levels will create differences in the operating compression point of each of the individual cells. At the drain, the differences in synthesized impedance for each of the cells will create differences in performance between the cells. These differences in performance between the cells will add to other imbalances created due e.g. to the differences in the temperature of operation along the bar.

#### V. CONCLUSION

The usefulness and accuracy of full-wave electromagnetic simulation tools for modeling bondwire arrays has been validated. A 16 bondwire array structure has been fabricated obtaining a good matching between measurements and the full-wave model up to 15 GHz. It has been demonstrated that the accuracy of the inductor-based bondwire model is not always enough above 6GHz, which is especially true in the case of bus bar arrays with many bondwires in parallel. This work has revealed the importance of using an accurate bondwire array model during the design of hybrid power amplifiers above C-band.

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## POLARIS: ESA's Airborne Ice Sounding Radar Front-End Design, Performance Assessment and First Results

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**Abstract** — This paper addresses the design, implementation and experimental performance assessment of the RF front-end of an airborne P-band ice sounding radar. The ice sounder design comprises commercial-of-the-shelf modules and newly purpose-built components at a centre frequency of 435 MHz with 20% relative bandwidth. The transmitter uses two amplifiers combined in parallel to generate more than >128 W peak power, with system >60% PAE and 47dB in-band to out-of-band signal ratio. The four channel receiver features digitally controlled variable gain to achieve more than 100dB dynamic range, 2.4dB noise figure, 160 ns receiver recovery time and -46dBc 3<sup>rd</sup> order IMD products. The system comprises also, a digital front-end, a digital signal generator, a microstrip antenna array and a control unit.

All the subsystems were integrated, certified and functionally tested, and in May 2008 a successful proof-of-concept campaign was organized in Greenland. The system detected the bedrock under 3 km of ice, and internal layers were mapped up to 1.3 km.

**Index Terms** — Airborne radar, microwave power amplifiers, microwave switches, power dividers, radar transmitters, radar receivers

### I. INTRODUCTION

The European Space Agency (ESA) has proposed a spaceborne ice sounding radar as a candidate for the next Earth Explorer missions [1]. A mapping of the ice with its internal ice sheets structure would help to understand the ice past history and predict the future evolution and the impact of the climate changes in the ice poles. However, the scattering properties of the ice at P-band are not sufficiently well known. In order to close this knowledge gap, an airborne P-band ice sounding radar demonstrator has been initiated, called hereafter Polaris. Within two years, DTU has designed and implemented the full instrument including aircraft installation, a proof-of-concept campaign and data processing.

Key parameters of the instrument are listed in Table I and additional specifications and requirements are found in [2].

TABLE I  
P-SOUNDER SPECIFICATIONS

Centre frequency	435 MHz
Bandwidth (goal)	85 MHz
Polarization	Quad
Maximum pulse length	50 $\mu$ s
Peak power	100 W
Maximum PRF	20 kHz

The capabilities of the system include a fairly high relative bandwidth (20%), an accurate internal calibration, thermal stabilization, a large dynamic range, pulse-to-pulse coherence, a high sensitivity sufficient to detect the bedrock through 4 km of ice and sufficient surface clutter suppression. The former was implemented using a novel technique based on a multi-aperture antenna.



Fig. 1. Polaris system installed in the Twin Otter aircraft.

The system comprises an RF front-end, a digital front-end, a digital signal generator, a control unit, a storage module, a navigation module and a newly developed wideband probe-fed dual-linear polarization wideband microstrip patch antenna. All the subsystems have been successfully developed and integrated, and they were presented in previous publications [3],[4],[5].

The radar was installed, certified and functionally tested on a Twin Otter aircraft (Fig. 1) in March 2008, and the proof-of-concept campaign took place in May 2008 in Greenland.



This paper presents the RF Front-End design and performance assessment. At the end, a few results from the May 2008 campaign are presented.

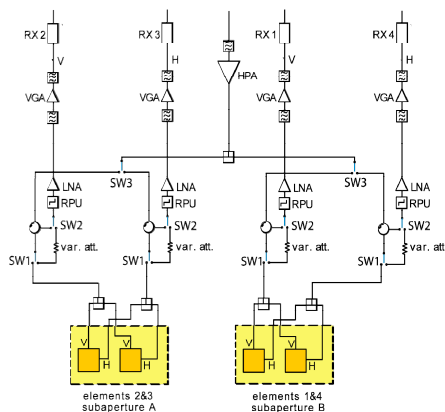


Fig. 2. RF Front-End Architecture.

## II. SYSTEM IMPLEMENTATION

The RF Front-End architecture (Fig. 2) comprises a classical design with a central transmitter and four receiver channels mounted inside the aircraft plus a four patches dual-polarized antenna mounted underneath the aircraft body. This configuration has been selected over a more advanced distributed system with transmit and receive modules mounted directly behind the antenna elements mainly because of aircraft certification restrictions. The Polaris design is based on in-house module developments for the antenna, power amplifier, the high power nanosecond switch, a variable gain amplifier and power dividers and combiners, while all other components are commercial-off-the-shelf (COTS).

The transmitter is composed of two high power high-efficiency LDMOS amplifiers combined in parallel (HPA), a high power SPDT PIN switch (SW3), a circulator, a slow high power relay for calibration and in-phase and out-of-phase high power splitters. A system analysis based on ice scattering models [6] showed that the selected configuration with a transmitter peak power of 100W would be sufficient to detect the bedrock down to 4 km.

The receiver comprises a pin diode limiter (RPU), a low-noise amplifier, band pass filters and a variable gain amplifier that provides sufficient gain to drive optimally the A/D converters in the digital acquisition unit. The variable gain receiver is used to provide a high dynamic range exceeding 100dB, allowing a shallow/deep sounding approach. Alternating the receiver gain in a pulse-to-pulse basis makes it

possible to map both the near-surface and near-bottom ice windows simultaneously.

Based on DTU's experience with the airborne EMISAR system [7], the internal calibration is implemented by toggling the switches SW1 and SW2 in order to loop the generated pulses around the system.

Below, the three in-house purpose-built modules used in the system are briefly outlined: in-phase and out-of-phase high power dividers, a high power SPDT PIN switch and a solid state high efficiency power amplifier. Further details about these newly developed modules can be found in [5].

We have developed lumped element Wilkinson type in-phase and out-of-phase power dividers. Such realizations have been presented earlier [8],[9], but did not have the RF power handling capabilities. Both designs present the required 20% bandwidth with return loss better than 15dB and 100W power handling. The in-phase design presents amplitude difference of 0.1dB, insertion loss of 0.2dB and phase balance  $< 1^\circ$ , while the out-of-phase performs with 0.23dB amplitude unbalance, 0.5dB insertion loss and phase balance  $< 2^\circ$ . Layout details have been presented earlier [4],[5].

A high power PIN diode switch controlled by a TTL signal, and with 90W power handling capabilities has been developed [10]. The measured return loss at the three ports is better than 15dB, the insertion loss is lower than 0.6dB and the isolation is better than 42.5 dB across the full band. The turn-on time is 500 ns and the turn-off time 300 ns, without observing high voltage switching transients.

We have developed a 70W CW LDMOS power amplifier (Fig. 3) with 60% PAE, 0.1dB 395-475MHz bandwidth and 38.9dB gain. The design operates in class E and it comprises a driver and a power stage. Measured parameters are in excellent agreement with simulated results using the Freescale LDMOS model.



Fig. 3. Purpose-build Power Amplifier module.

## III. SYSTEM PERFORMANCE

### A. Transmitter

The transmitter contains two in-house purpose-built 70 W high power amplifiers combined in parallel by high power

lumped element Wilkinson combiners. The bias networks of both amplifiers were carefully adjusted to achieve identical performance and to avoid imbalances. A maximum combined power of 128.8W CW was measured, but due to power handling limitation of the power combiners and in order to guarantee a high reliability, it was decided to operate both power amplifiers in back-off during flight. Therefore, during the proof-of-concept campaign, the transmitter was generating 102W peak power at 475MHz with a total PAE of 44%.

Comparing the single amplifier performance with the combined one, the gain flatness is degraded from 0.1dB to 1dB and the efficiency is reduced from 60% to 40%. This is a direct consequence of driving the power amplifiers in back-off, and also due to the limited bandwidth of the power combiners. The former imply that the power amplifiers are not loaded with 50 Ohms at the higher order harmonics, and this can have a significant impact in the performance [11].

The transmitter was tested with an 85MHz bandwidth pulsed signal generated by the Digital Signal Generator (DSG), and the measured in-band to out-of-band signal ratio was larger than 47.6dB. The measured noise generated by the transmitter during reception was found to be under the noise floor of the spectrum analyzer (-90.5 dBm). This is important since the transmitter and receiver are separated only by a circulator.

### B. Receiver

The receiver chain S-parameter measurements were performed between the cables connected to the antenna ports and the receiver output. The input power level used during the measurements was adjusted to have always -20dBm at the receiver output. Fig. 4 shows the transducer gain of one of the channels for different gain settings. An in-band ripple of around 1dB is observed. The return loss at the input is better than 12.8dB across the bandwidth. The S-parameters were measured for the four receiving channels, observing always a good agreement among each other. This is important in order to implement the surface clutter suppression algorithms. The noise figure of the receiver was initially around  $NF = 0.5$  dB, but subsequently deteriorated by the limiter, the circulator and other passives placed in front of the LNA. However it is still better than 2.4dB for the high gain settings, whereas it is notably degraded when using low gain settings.

The PIN diode limiter placed in front of the LNA is needed to protect the receiver during the transmission of high power pulses, but it also introduces a recovery time. This is defined as the time until the receiver recovers its normal sensitivity after an overvoltage at the input of the limiter. Figure 5 shows the recovery time measured with an oscilloscope. The channel on the foreground is the result of combining a -45dBm CW signal and a pulsed signal that activates the limiter, and the channel in the background is the output of the receiver. It is possible to observe that the evolution of the receiver output is

distorted during 800ns, but the time that the receiver is completely blind is only around 160ns.

Measurements of the receiver third order IMD products were performed placing two combined tones at 435 and 436 MHz at the receiver input, and adjusting the input power to have 0dBm at the receiver output. The third order IMD products are around -52dB in the low gain range, and -46dB in the high gain range.

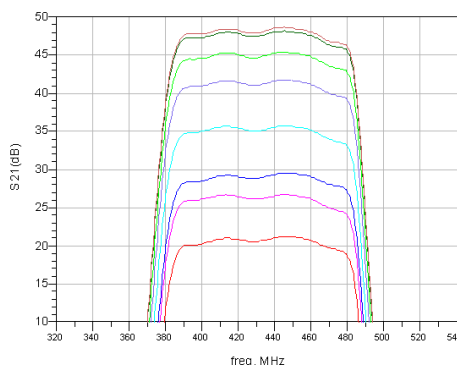


Fig. 4. Receiver transducer gain for different gain settings.

The transmitter and receiver were tested together looping the generated high power pulses around the calibration path (PRF= 10 KHz, Pulse Length=10 $\mu$ s, BW=85MHz and Duty Cycle=10%). The spectrum shown in Fig. 6 was measured at the output of the receiver depicting a 1.5dB ripple in the system response across the full bandwidth. This ripple was carefully compensated using digital pre-distortion techniques.



Fig. 5. Receiver measured recovery time. .



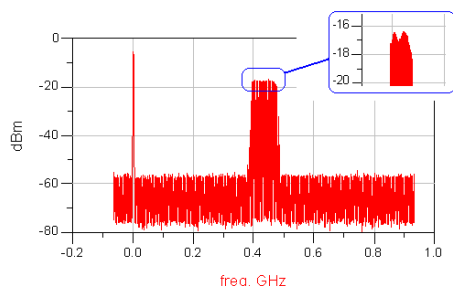


Fig. 6. Spectrum at the output of the receiver when high power pulses are looped around the system during a system calibration.

#### IV. CAMPAIGN RESULTS

The proof-of-concept campaign took place in Greenland in May 2008. Fig. 7 shows the bedrock detected through almost 3 km of ice in the dry snow zone in Greenland. According to ice models [6], 2.5 km of warm ice in Greenland are comparable to 4 km of cold ice in Antarctica. Internal ice layers were also detected with a resolution of several meters, but are subject of another paper.

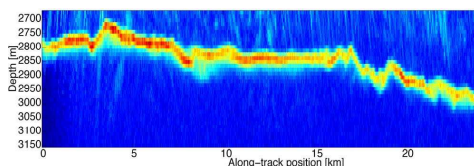


Fig. 7. Bedrock in Greenland detected through 3 km of ice.

#### V. CONCLUSION

We have presented the RF Front-End design and performance assessment of an airborne P-band ice sounding radar. State-of-the-art modules have been developed for the system: compact high power power dividers with 100 CW power handling, a high power SPDT PIN switch handling 90W CW and nanosecond switching times, and a 70W CW high efficiency LDMOS power amplifier with >60% PAE. The transmitter generates more than 128 W peak power, with 60% PAE and 47dB band to out of band signal ratio. The receiver performance features more than 100dB dynamic range, 2.4dB noise figure, 160 ns receiver recovery time and -46dBc 3rd order IMD products in the worse case.

In May 2008, a successful proof-of-concept campaign was organized in Greenland, detecting internal ice layers and the bedrock under 3 km of ice. New activities related to the project are ongoing: a new microstrip antenna with eight dual polarized patches is being designed, the transmitted peak power will be increased with a new power amplifier operating in the 200 W range with >60% PAE and new data acquisition campaigns are foreseen in the near future.

#### ACKNOWLEDGEMENT

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## High Power High Efficiency Amplifiers for P-Band in LDMOS, GaAs, and GaN Technology

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### Abstract

ESA has commissioned an airborne POLarimetric Airborne Ice Sounding Radar (POLARIS), which has been developed and tested by the Technical University of Denmark (DTU). This radar system operates at P-band frequencies. High power amplifier with high efficiency in excess of 60% at 100 W output power has been identified as one of the problem areas in future space based instrument implementation. The current project preliminary results of which will be presented here focuses on identifying a prominent technology platform for high power high efficiency amplifiers operating in pulsed mode. We have been studying several technologies, with special emphasis on space worthiness, high output power and high efficiency operation.

We have implemented several high power amplifiers in LDMOS, GaN HEMT, and GaAs HBT technologies, respectively. Most of these technologies rely on European sources. We will demonstrate that at P-Band frequencies around 435 MHz with a bandwidth of 5 MHz, it is possible to achieve  $P_{out} = 200$  W with an efficiency of  $>65\%$  in pulsed operation using LDMOS technology. In case of GaN HEMT technology, we have experimentally achieved  $P_{out} = 100$  W with an efficiency of  $\sim 70\%$ . We have also designed GaAs HBT power amplifiers with an output power of  $P_{out} > 80$  W with  $>70\%$  efficiency. The HPA are all compact with a footprint of around  $10 \times 7$  cm. All results respect the necessary derating of voltages, currents and junction temperatures, which are demanded for space applications. Wider bandwidths are also possible at the expense of footprint space. In fact, we have tested an LDMOS HPA with  $P_{out} > 200$  W with an efficiency of  $> 60\%$  across 80 MHz bandwidth, which is compatible with the POLARIS system bandwidth. We will present details on the amplifier design approach and a comparison of the different technologies during the talk.

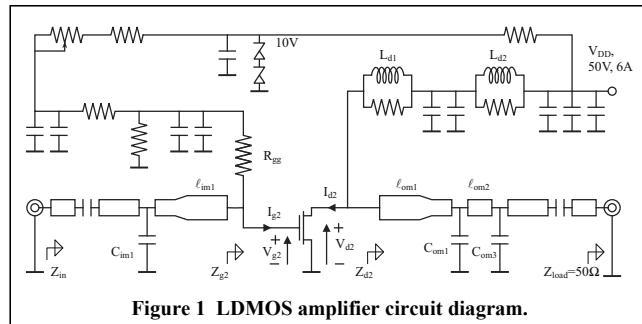
### Introduction

ESA has commissioned an airborne POLarimetric Airborne Ice Sounding Radar (POLARIS), which has been developed and tested by the Technical University of Denmark (DTU) [1]-[5]. This radar system operates at P-band frequencies. High power amplifier with high efficiency in excess of 60% at 100 W output power has been identified as one of the problem areas in future space based instrument implementation. The amplifiers to be developed are intended for pulsed operation with pulse rise and fall times  $< 50$  ns and PRF of 900 Hz 25% duty cycle and 6000 Hz 36% duty cycle, respectively. The centre frequency is 435 MHz.

We have implemented several high power amplifiers in LDMOS, GaN HEMT, and GaAs HBT technologies, respectively. Most of these technologies rely on European sources. We demonstrate that at P-Band frequencies around 435 MHz with a bandwidth of 5 MHz, it is possible to achieve  $P_{out} = 200$  W with an efficiency of  $>65\%$  in pulsed operation using LDMOS technology. In case of GaN HEMT technology, we have experimentally achieved  $P_{out} = 100$  W with an efficiency of  $\sim 70\%$ . We have also designed GaAs HBT power amplifiers with an output power of  $P_{out} > 80$  W with  $>70\%$  efficiency. The HPA are all compact with a footprint of around  $10 \times 7$  cm. All results respect the necessary derating of voltages, currents and junction temperatures, which are demanded for space applications. Wider bandwidths are also possible. In fact, we have tested an LDMOS HPA with  $P_{out} > 200$  W with an efficiency of  $> 60\%$  across 80 MHz bandwidth, which is compatible with the POLARIS system bandwidth.

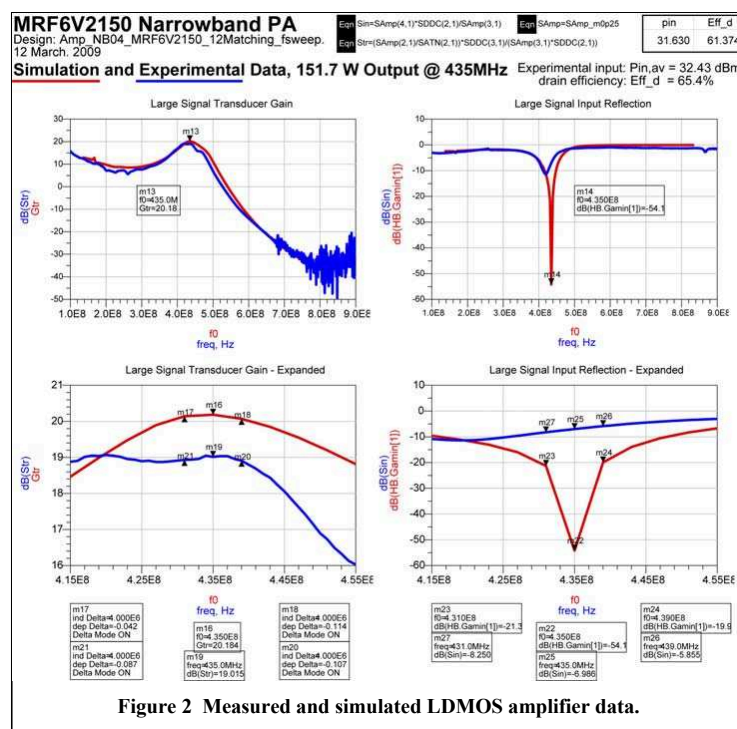
**Power amplifier realisation based on LDMOS Transistors**

The initial LDMOS amplifier is designed following the series tuned approach outlined in [6], which means that the power transistor is supposed to operate with sinusoidal currents and pulse shaped voltages. This is a simple and controllable way of designing PA's when the required loading and driving impedances are rather low. Taking outset in the basic circuit schematic, Figure 1, the series tuning is achieved by series line segments  $\ell_{im1}$  and  $\ell_{om1}$  that are the matching circuit components, which connect directly to the transistor. While the input matching is made by a single section circuit,  $\ell_{im1}$ ,  $C_{im1}$ , in this narrowband design, two sections,  $\ell_{om1}$ ,  $C_{om1}$ , and  $\ell_{om2}$ ,  $C_{om2}$ , are used in the output in an attempt to simultaneously flatten the power and efficiency frequency characteristics across the desired bandwidth.



**Figure 1 LDMOS amplifier circuit diagram.**

The design objectives are chosen such that a minimum gate current flows through the transistor at most power levels, the maximum voltage swing is restricted to 70% of the breakdown voltage, a quiescent current is set and an efficiency is prescribed. A set of analytical equations are then solved to obtain the required load impedances. With a quiescent transistor current adjusted to 0.3A and we get 150W with 61% efficiency at a gain of 20dB and a final junction temperature, incl. the ambient contribution, of 42.5 °C. The major challenge in the design is the realisation of the load impedances given the fact that the gate input and the drain load impedances are rather low, in the  $1 \Omega$  range. Without making any further adjustments the results presented in have been achieved.



**Figure 2 Measured and simulated LDMOS amplifier data.**

Photograph of the power amplifier and its pulse performance is shown in Figure 3 and Figure 4. The performance of the amplifier is summarized in Table 1 and Table 2. It is clear from Table 1 that the performance of the amplifier in terms of output power deteriorates as the pulses approach CW operation, but the efficiency always stay at a minimum

of 60% and the output power is  $P_{out} > 135W$  under all conditions. The drop in performance is due to thermal dissipation in CW operation.



Figure 3 LDMOS amplifier photo.

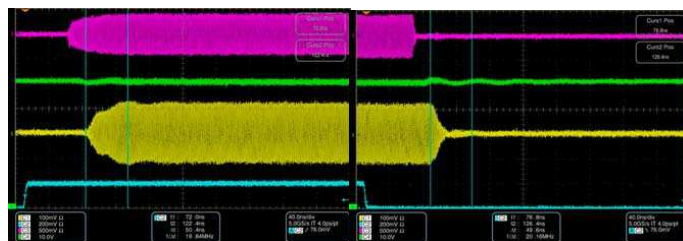


Figure 4 Leading and trailing edges for a PRF = 900Hz, period 1.111ms, 25% duty cycle, and pulse width of 277  $\mu$ s.

Table 1 LDMOS amplifier CW performance,  $f = 435MHz$ ,  $V_{DD} = 50V$ ,  $I_O = 300mA$

CW duration sec.	$P_{in}$ dBm	$P_{out}$ dBm	Gain dB	$P_{out}$ W	$I_{DD}$ A	Eff. %
0	32.17	52.09	19.9	161.8	4.84	66.9
10	32.17	51.49	19.3	140.9	4.61	61.1
60 +	32.17	51.41	19.2	138.4	4.63	59.8

Table 2 LDMOS amplifier pulsed performance,  $f = 435MHz$ ,  $V_{DD} = 50V$ ,  $I_O = 300mA$

Length sec	$P_{out,mean}$ dBm	$I_{DD,mean}$ A	Eff <sub>mean</sub> %	$P_{out,peak}$ dBm	$P_{out,peak}$ W	$I_{DD,peak}$ A	Eff <sub>peak</sub> %
2	45.89	1.49	51.8	51.92	155.7	5.07	61.4
60+	45.82	1.52	49.9	49.9	152.8	5.06	60.4
2	47.60	2.02	56.7	56.7	159.8	5.08	63.0
60+	47.53	2.04	55.2	51.97	157.3	5.06	62.1

On the other hand, the pulse performance of the LDMOS amplifier shows excellent performance without appreciable pulse droop and with peak efficiencies  $> 60\%$  with peak output power higher than 150W. It should be mentioned that efficiency determination in pulse operation is difficult and we believe that the actual efficiency is better than these numbers. A similar performance is expected from a similar devices from NXP, which is being studied now.

#### Power amplifier realisation based on GaN Transistors

A similar design strategy has been employed for the GaN power amplifier using a Cree device CGH120F. The device has been chosen because it is the first commercially available unmatched GaN transistor providing more than 100 W output power in the frequency range of interest.

Figure 5 shows the practical realization of a 120W GaN (Cree CHG40120F) design. The circuit is mounted on an enforced cooling heat-sink with three fans.

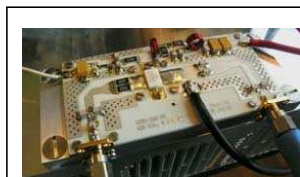


Figure 5 GaN amplifier photo.

Without making any component changes to the initial design in ADS, the high output power frequency sweep in Figure 2 was obtained. The figure demonstrates a relatively close resemblance between simulated and experimental results but it is clear from the curves that the experimental amplifier needs a better tuning. The data in the figure show that even without any further adjustments, the amplifier comes close to specifications regarding power (121.6 W obtained), gain (16.6 dB), efficiency (67.2%), and gain flatness across the band ( 0.2 dB variation). An improvement is foreseen when the circuit becomes adjusted since the efficiency with the present circuit is 71.3 % at 445MHz with 123W output power and 76.7% at 455MHz with 119.7W output power.

GaN power amplifiers have more severe small-signal stability problems than their LDMOS counterparts. To ensure low frequency stability, resistive gain reduction is required and realized by series resistors in the signal path prior to the gate as seen in Figure 5. At higher frequencies there is a region from 1.4GHz to 2.3GHz where the experimental data still show potential instability which is due to a significantly higher S12 feedback at the critical frequencies in the practical amplifier.

The self-heating of the transistor chip when a large signal is applied makes CW measurements time dependent. Table 3 summarizes the CW centre frequency results when the amplifier is operated around its maximum output power. The duration is the time since the CW signal was applied. Zero duration results are based on the automatic peak value readings in the power and the DC current supply meters that are used in the measurements. The duration of 10+ indicates that the amplifier settles thermally after approximately 10 seconds, which is fast compared to the similar LDMOS results in Table 1 on page 3.

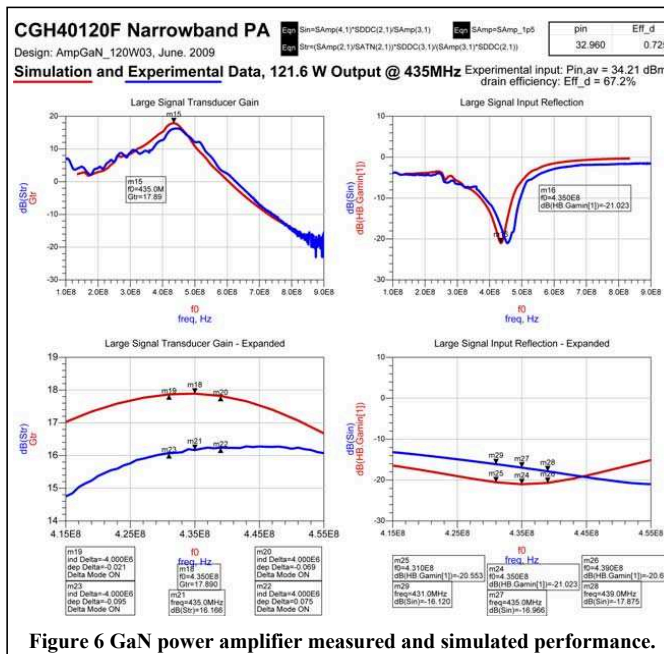


Figure 6 GaN power amplifier measured and simulated performance.

Table 3 GaN amplifier CW performance, f= 435MHz, V<sub>DD</sub>=28V, I<sub>O</sub>=350mA

CW duration sec.	P <sub>in</sub> dBm	P <sub>out</sub> dBm	Gain dB	P <sub>out</sub> W	I <sub>DD</sub> A	Eff. %
0	33.16	50.97	17.8	125.0	6.12	73.0
10 +	33.16	50.70	17.5	117.5	6.01	69.8

Measurements under pulses operations are summarized below in Table 4. The mean value results are taken directly from the mean value power and current reading in the measurement setup. If the amplifier was equipped with a bias gating function shutting off the quiescent current outside the pulse period, the average date would equal the peak performances. With the GaN amplifier the first observation is that very high efficiencies are obtained. No effects of self heating are observed and it is supposed that the amplifier stabilizes thermally before the power meter averaging settles. Comparing the two pulse modes, it seems here

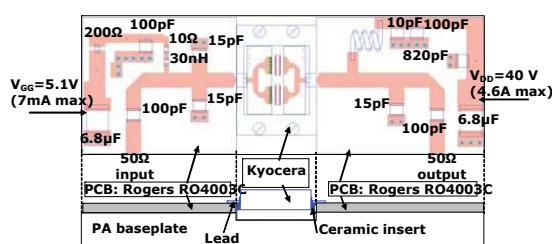


that in contrast to the LDMOS case, it is now the duty-cycle rather than the pulse width that dominates the thermal performance reductions.

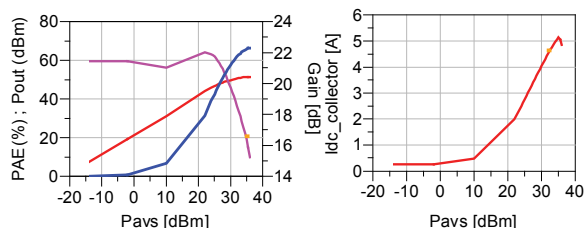
**Table 4 GaN amplifier pulsed performance,  $f=435\text{MHz}$ ,  $V_{DD}=28\text{V}$ ,  $I_0=350\text{mA}$**

Pulse No	Duration sec	$P_{out,mean}$ dBm	$I_{DD,mean}$ A	$Eff_{mean}$ %	$P_{out,peak}$ dBm	$P_{out,peak}$ W	$I_{DD,peak}$ A	$Eff_{peak}$ %
1	2+	44.57	1.50	68.2	50.59	114.6	4.95	82.7
2	2+	46.17	2.11	70.1	50.61	115.0	5.24	78.4

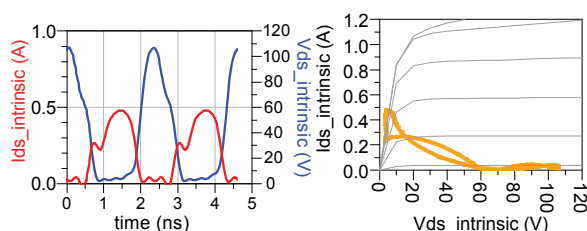
Another GaN HEMT amplifier has been designed based on power bar chips provided from III-V Alcatel Thales Lab. The layout of the amplifier can be depicted in Figure 7 for the center frequency of 435 MHz and the other parameters equivalent to the power amplifiers shown above. The output power, efficiency, gain, and drain current are depicted in Figure 8,



**Figure 7: Layout of the HPA using GaN power bars from III-V Alcatel Thales Lab.**



**Figure 8: Simulated output power, efficiency, gain and drain current versus available input power at 435 MHz for the circuit in Figure 7.**



**Figure 9: Dynamic voltages and currents for the circuit in Figure 7.**

this amplifier reaches  $P_{out} > 80\text{ W}$  with an efficiency of 70% and a similar gain as the GaN amplifier. The bandwidth of the HPA with HBT devices is narrower and is predicted to be around 7 MHz.

which shows simulated results. If one chooses an input power of 35 dBm, gain drops to acceptable 16 dB, the efficiency achieved is close to 65%, and the output power is more than 130 W. The dynamic loadlines are also provided in Figure 9. It can be depicted that the voltage excursion reaches 110V in the dynamic loadline, which is still acceptable due to the high breakdown voltage of GaN HEMT devices. The input return loss across a bandwidth of 14 MHz ( $P_{out,pp} < 0.5\text{ dB}$ ) is  $RL > 15\text{ dB}$ . The total associated drain DC current is around  $I_{DS} = 4.6\text{ A}$ . Comparison of the results achieved with European GaN supplier and Cree devices, shows that similar performance can be achieved with both devices. The numbers quoted for the output power, efficiency and gain include all package losses.

#### Power amplifier realisation based on HBT Transistors

The HBT power amplifier is based on UMS power cells, developed in a separate ESA project. Due to the lower power capabilities of HBT devices, it is necessary to employ more power cells within a package. The layout of the HPA is illustrated in Figure 10 together with the simulated output power, efficiency, dynamic currents and DC currents. The challenge with this amplifier has been among others that the collector current becomes very large and packaging becomes a problem. The output power of

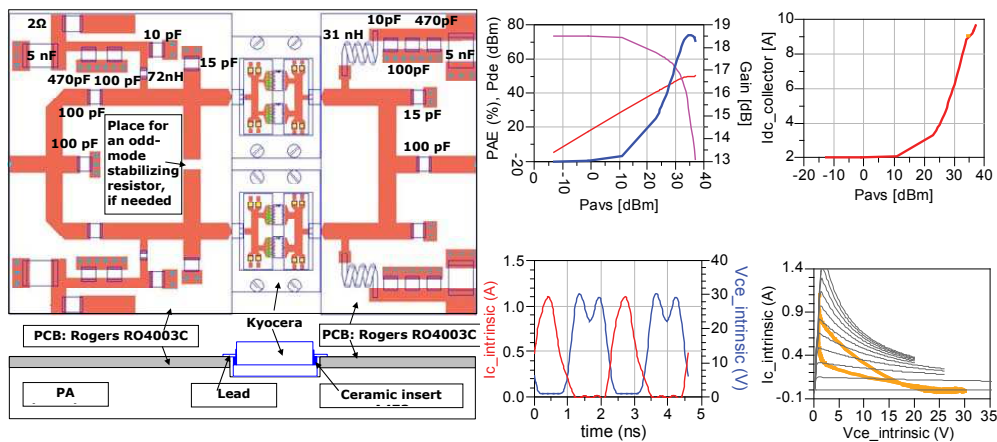


Figure 10: Layout, output power, efficiency, DC current, and dynamic loadlines for GaAs HBT HPA.

### Conclusions

We have shown that at P-Band frequencies around 435 MHz and 5 MHz bandwidth, it is possible to achieve  $P_{out} = 200$  W with an efficiency of  $>65\%$  in pulsed operation using LDMOS technology,  $P_{out} = 100$  W with an efficiency of  $\sim 70\%$ , in case of GaN HEMT technology, and  $P_{out} > 80$  W with  $>70\%$  efficiency with GaAs HBT power amplifiers. All results are under pulse operation. These results demonstrate that high-efficiency power amplifiers with high output powers are feasible partially with technologies already available in Europe. All results respect the necessary derating of voltages, currents and junction temperatures, which are demanded for space applications. Wider bandwidths are also possible at the expense of footprint space and trade-off in efficiency. In fact, we have tested an LDMOS HPA with  $P_{out} > 200$  W with an efficiency of  $> 60\%$  across 80 MHz bandwidth, which is compatible with the POLARIS system bandwidth.

### Acknowledgement

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