



Design of Integrated Circuits Approaching Terahertz Frequencies

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Design of Integrated Circuits Approaching Terahertz Frequencies

Lei Yan

September 21, 2012

Abstract

In this thesis, monolithic microwave integrated circuits(MMICs) are presented for millimeter-wave and submillimeter-wave or terahertz(THz) applications. Millimeter-wave power generation from solid state devices is not only crucial for the emerging high data rate wireless communications but also important for driving THz signal sources. To meet the requirement of high output power, amplifiers based on InP double heterojunction bipolar transistor (DHBT) devices from the III-V Lab in Marcoussic, France are designed for the power generation at millimeter-wave frequency range. For future THz heterodyne receivers with requirements of room temperature operation, low system complexity, and high sensitivity, monolithic integrated Schottky diode technology is chosen for the implementation of submillimeter-wave components. The corresponding subharmonic mixer and multiplier for a THz radiometer system are designed based on the monolithic membrane supported Schottky diodes, which is under development at Chalmers University of Technology, Sweden. To simplify the baseband circuitry, the received IF signal from the subharmonic mixer is further amplified and down-converted to the DC range with a low noise amplifier and an active mixer by using GaAs pseudomorphic high electron mobility transistor (pHEMT) technology available from OMMIC, France.

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Kgs. Lyngby, August 2012

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Publication List

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2. L.Yan, T.K.Johansen, and J.Kammersgaard "Stability Investigation for InP DHBT mm-wave Power Amplifier", *International Journal of RF and Microwave Computer-Aided Engineering*, accepted, 2012
3. L.Yan, M.Tang, V.Krozer, V.Zhurbenko, C.Jiang, and T.K.Johansen "Filter designs based on coupled transmission line model for double split ring resonators ", *Microwave and Optical Technology Letters*, 2011
4. L.Yan, M.Tang, V.Krozer, V.Zhurbenko, T.Jensen, C.Jiang, and T.K.Johansen, "Transmission line model for coupled rectangular double split-ring resonators ", *Microwave and Optical Technology Letters*, 2011
5. T.K.Johansen and L.Yan, "Design of Mm-wave InP DHBT Power Amplifiers", *SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference*, 2011
6. L.Yan, V.Krozer, S.Delcourt, V.Zhurbenko, T.K.Johansen, and C.Jiang "GaAs Wideband Low Noise Amplifier Design for Breast Cancer Detection System", *Asian Pacific Microwave Conference, 2009 Singapore*
7. L.Yan, T.K.Johansen, and V.Krozer, "Low Noise Design Strategy for Mixers and Amplifiers", *Germany Microwave Conference, 2008 Hamburg*
8. J.Stake, H.Zhao, P.Sobis, A.Y.tang, V.Drakinskiy, A.Hülsmann, I.Kallfass, A.Tessman, A.Leuther, T.Bryllert, J.Hanning, T.Pelikka, A.Emrich, H.Richter, H.W.Hübers, L.Yan, T.K.Johansen, and V.Krozer, "Development of a compact 557GHz heterodyne receiver", *6th ESA Workshop on Millimeter-wave Technology and Applications and 4th Global Symposium on Millimeter Waves*, 2011
9. C.Jiang, V.Krozer, T.K.Johansen, H.G.Bach, G.G.Mekonnen, and L.Yan "Behavioral electromagnetic models of high-speed P-I-N photodiodes", *Microwave and Optical Technology Letters*, 2011

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10. C.Jiang, T.K.Johansen, L.Yan, and B.Anja, "Cantilever-Based Microwave Biosensors: Analysis, Designs and Optimizations", *Proceedings of the 27th Annual Review of Progress in Applied Computational Electromagnetics, 2011*

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List of symbols

$\Delta\phi$	Barrier height lowering due to image force
δ_{sub}	Skin depth of SUB layer
ϵ	Permittivity of GaAs material
μ_{epi}	Electron mobility in EPI layer
μ_{sub}	Electron mobility in SUB layer
ω_d	Energy relaxation frequency for dielectric material
ω_p	Plasma frequency of the material
ω_s	Mean scattering frequency
ϕ_b	Barrier height
ρ	Resistivity of Ohmic contact
σ_{epi}	Conductivity of EPI layer
σ_{sub}	Conductivity of EPI layer
$\widehat{I}_m(x)$	Modified bessel function of order m
ξ	Potential difference between the Fermi level and bottom of the conduction band
A	Area of the anode
a	Radius of anode contact
A_e	Emitter area
b	Radius of Ohmic contact

C_{epi}	Junction capacitance from EPI layer
C_{sub}	Junction capacitance from SUB layer
CB	Common base
CC	Common collector
CE	Common emitter
CL	Conversion loss
CPW	Coplanar waveguide
$DHBT$	Double heterojunction bipolar transistor
E_C	Bottom of the conduction band
E_{max}	Maximum electric field within the depletion region
f_c	Cutoff frequency
F_{min}	Minimum noise figure
FIR	Far-infrared
G	Power gain
$G(t)$	Time variant conductance
G_m	Transconductance
I_c	Collector current
IF	Intermediate frequency
J	Current density
k_B	Boltzmann constant
L_D	Debye length
LNA	Low noise amplifier
m^*	Effective electron mass
$MMIC$	Monolithic microwave integrated circuit

<i>mmwave</i>	Millimeter-wave
N_f	Ideality factor
N_{epi}	Doping of EPI layer
N_{sub}	Doping of EPI layer
NDF	Normalized determinant function
NF	Noise figure
NF_{dsb}	Double sideband noise figure
P_{1dB}	Output 1dB compression point
P_{LO}	Local oscillator power level
P_{sat}	Saturated output power
PA	Power amplifier
PAE	Power added efficiency
<i>pHEMT</i>	Pseudomorphic high electron mobility transistor
R_{opt}	Real part of impedance for optimum noise matching
RD	Return difference
RR	Return ratio
SHM	Subharmonic mixer
SOA	Safe operation area
<i>Submm – wave</i>	Submillimeter-wave
T	Device temperature
T_{epi}	Thickness of EPI layer
T_{sub}	Thickness of EPI layer
THz	Terahertz
V_T	Thermal voltage

V_{bi}	Built-in Potential
V_{ce}	Collector emitter voltage
v_{drift}	Drift velocity of electron
v_d	Diffusion velocity of electron
v_I	Recombination velocity of electron
V_j	Junction voltage on diode
V_p	Punch through voltage
w_{epi}	Depletion width of EPI layer
w_{sub}	Depletion width of SUB layer
X_{opt}	Imaginary part of impedance for optimum noise matching
Z_{IF}	Optimum load at IF port
Z_{LO}	Optimum load at LO port
Z_{opt}	Optimum load impedance
Z_{RF}	Optimum load at RF port
Z_{skin}	Skin depth impedance from SUB layer
Z_{sp}	Spreading impedance from SUB layer

Chapter 1

Introduction

This chapter will first introduce the general background and research motivation of this work. Thereafter, an outline of the thesis will be provided.

1.1 Background and motivation

We are faced with an increasing demand for monolithic microwave integrated circuits (MMICs) for communications, remote sensing and instrumentation systems operating at frequencies approaching terahertz (THz) frequencies. This drives the development of the cutting-edge technologies for millimeter-wave and submillimeter-wave MMICs such as: power amplifiers, subharmonic mixers, and multipliers with the frequency range of E-band (60-90 GHz), D-band (110-170 GHz), G-band (140-220 GHz), and beyond. These MMICs will have several promising markets including wireless broadband communications systems with data speeds of several Gbit/s, submillimeter-wave heterodyne receivers for future instruments in Earth observation and space science, and low-noise receivers employed in imaging instrumentation for security applications.

The 71-76 and 81-86 GHz bands, also known as the E-band, provide an opportunity for line of sight (LOS) links with longer range and higher data rates [1]. Millimeter-wave (mm-wave) communication systems operate at E-band frequencies requires power amplifiers to boost transmitted signals over distances of 6-10 km. However, the practically achievable communication range is limited by atmospheric attenuation and output power attainable from semiconductor devices [2].

A wireless communication link at E-band with the capability of high data rate (in excess of 10 Gbps) requires high signal to interferer and noise ratio (SINR). The practical achievable SINR is limited by the local oscillator (LO) phase noise, noise figure of low noise amplifier (LNA), inter-channel interference, output power and linearity of the power amplifier [1, 3]. In this work, integrated mm-wave power amplifiers are designed based on InP double heterojunction bipolar transistor (DHBT) devices from the III-V Lab in Marcoussic, France. InP DHBT are generally considered for the power generation due to its higher breakdown voltage and power density compared with Silicon based devices such as SiGe HBTs and CMOS. Fig.1.1 shows a typical mm-wave communication system diagram. The inserted microphotographies are the integrated power amplifier and active subharmonic mixer [4] designed by using III-V lab InP DHBT technology. The mm-wave power generation with solid state components also has an important use as drivers for THz signal sources.

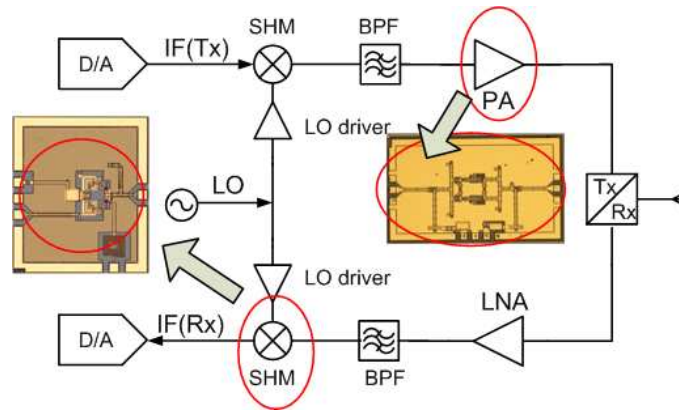


Figure 1.1: Mm-wave RF transceiver system diagram.

THz frequencies normally mean the frequency range between 300 GHz and 10 THz with its respective wavelength from 1 mm to $30 \mu\text{m}$ [5]. It is located between the regime of microwave and the far-infrared (FIR) in the electromagnetic spectrum. As is the case in other spectral regions, astronomers and atmospheric scientists drive much of the cutting-edge technology development for this frequency range [6–12]. More recently, THz heterodyne receivers have been applied to non-destructive testing, biomedicine [13, 14], and security. Specially, the application of THz imaging systems for stand-off

detection of threats has attracted significant interests [15–17].

THz heterodyne receivers offer the highest sensitivity at the low FIR frequency range due to the fact that a baseband LNA can be used to reduce system noise [7, 10, 18]. As the frequency increases, the direct detection instruments becomes more attractive [18]. At present, the ultimate low noise with the highest sensitivity heterodyne receivers used for submillimetre-wave(submm-wave) radio astronomy are based on cryogenic devices [19]. Typical mixers use Superconductor-Insulator-Superconductor tunnel junctions operating up to 1 THz [20, 21] and Hot Electron Bolometers operating from 1 to 7 THz [22, 23]. However, both types of mixers must operate at temperature below 4 K if sensitivity is stressed [7]. For commercial applications where cryogenic operation is not possible due to elevated sizes and costs, Schottky diode technology is a good candidate and can operate properly at room-temperature. The penalty of operating at room temperature typically carries a factor of 5 to 10 in sensitivity [7]. But the new advances in monolithic integrated membrane circuits are making Schottky diode technology ever more attractive [24].

For future THz applications, a versatile and flexible receiver technology is needed to allow high level system integration [19, 25–27]. These motivate the integration and custom designs of front-end components. The traditional low level integration based on individual packaged waveguide mixers, multipliers, and low noise amplifiers(LNAs) has difficulties to satisfy requirements to future systems. One important issue is to reduce the power loss of LO signals from the source to mixer. A typical solution is to integrate the mixer and the last stage multiplier on to the same circuit. This leads to several compact radiometer elements by integrating a subharmonic mixer(SHM) and a tripler together [27–29]. The second issue is to separate the signal bands to improve the sensitivity by reducing the noise contribution from the image band. In this case, image rejection SHMs are preferred [30, 31]. Another issue is the standing waves between SHMs and IF LNAs. To minimize the power reflection between them, LNAs are considered to be embedded into the metallic housing together with the SHM [19].

Another objective of this research work is the development of a low noise subharmonic mixer and resistive multiplier for a THz radiometer system at 557 GHz based on membrane Schottky technology. The system diagram of a 557 GHz heterodyne receiver system is shown in Fig.1.2. The inserted microphotographies are integrated circuits designed during this work, including

an IF low noise amplifier(LNA), an active mixer, a submm-wave tripler, and a submm-wave subharmonic mixer(SHM). The SHM and tripler are designed based on the monolithic integrated Schottky diode technology, which is under development at Chalmers University of Technology, Sweden. To amplify the received IF signal from the SHM and down-convert it to the baseband, a LNA and an active mixer are designed with GaAs pHEMT technology available from OMMIC, France.

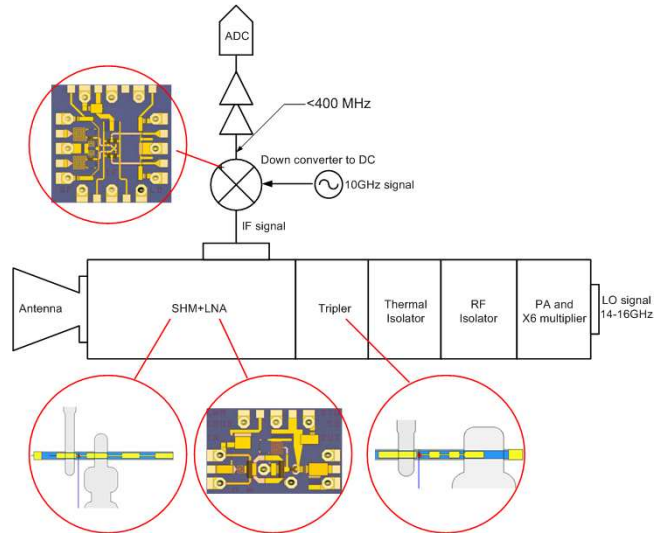


Figure 1.2: System diagram of the THz heterodyne receiver at 557 GHz.

1.2 Outline of the thesis

The main part of the thesis is divided into four additional chapters.

Chapter 2 focuses on the E-band power amplifier design by using InP DHBT technology. Different power amplifier topologies are discussed and compared in term of small/large-signal characteristics. A new power cell based on the interstage matched cascode configuration is proposed to improve the saturated output power. The even/odd-mode instability of power amplifiers at the mm-wave frequency range is extensively investigated. The relevant measurement results are presented to verify the analysis. A summary is given at the end to conclude the chapter.

Chapter 3 focuses on the design methodology of a subharmonic mixer and a tripler by using the monolithic integrated Schottky diode technology. Both designs are based on the crossbar configuration on a GaAs membrane. The discussions on conversion loss, propagation mode, attenuation, mixer optimum impedance, matching circuits design, and statistical analysis are presented. The large-signal characteristics of the designed SHM and tripler based on the ADS diode model are summarized. Finally, a summary is given at the end to conclude the chapter.

Chapter 4 focuses on the implementation of a physical based Schottky diode model to include features such as barrier height lowering and hot electron noise. To verify the implemented diode model, simulated I-V and C-V characteristics are compared with the measurement results from Chalmers. Predicted noise temperatures are compared with the experimental data found from open literatures. The performance of designed SHM with physical based diode model and ADS model are compared. A summary is given at the end to conclude the chapter.

Chapter 5 focuses on an IF low noise amplifier and active mixer design by using GaAs pHEMT technology. A low noise amplifier based on a cascode configuration with an output buffer is proposed for wideband stable operation. The simultaneously noise and power matching is explored by using gate and source degenerated inductors. The active mixer is implemented with the standard Gilbert cell topology. The associated measurement results for both components are presented. A summary is given at the end to conclude the chapter.

Chapter 6 concludes the thesis work.

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Chapter 2

Millimeter-wave Power Amplifier Design

2.1 Introduction

A bottleneck today for emerging high speed wireless applications such as the E-band standard is the availability of high power amplifiers [1–4]. There are only few solutions available today for the power generation in this frequency range, most of them involving HEMT technologies. Recently, the most impressive results of an E-band power amplifier based on GaN HEMT devices show 250 mW (24 dBm) at 1dB compression at 84 GHz with a linear power gain of 15 dB [5]. And a three-stage design [6] shows a saturated output power of 1.3 W (31.13 dBm) at 75 GHz. The reported InP power amplifiers from the open literatures [7–13] for mm-wave applications are summarized in Table.2.1. The highest reported output power with InP DHBT devices is 20.8 dBm at 1dBm compression point at 72 GHz [9]. The single-stage common-emitter InP DHBT amplifier recently demonstrated in [13] shows 8.7 dBm output power with an associated linear gain of 5 dB at 172 GHz. Another reported InP DHBT amplifier [14] shows 3.5 dB gain at 255 GHz.

From Table.2.1, it can be seen that the most popular circuit topologies for mm-wave HBT power amplifiers are based on common-base(CB) and cascode(Cas) configurations. These configurations are suitable for mm-wave applications due to the higher power gain and higher optimum load impedance compared with common-emitter(CE) or common-collector(CC) topologies. Despite the fact that mm-wave power amplifiers based on HBT technologies reported to date deliver less output power than their HEMT

Topology	N-way	Freq [GHz]	G [dB]	P_{1dB} [dBm]	P_{sat} [dBm]	PAE [%]	A_e [μm^2]	Ref
Cas	1	90	8.5	9.5	>12	NA	128	[7]
Cas	12	72	12	17.8	20.6	13.9	120	[8]
Cas	4x12	72	8.25	20.8	23	5.9	480	[8]
Cas	4	68	13.5	13.7	15.1	12	51.2	[9]
Cas	4	94.5	8.5	13.5	14.4	NA	80	[10]
Cas	4	75	7.5	9.4	NA	NA	200	[11]
CB	2	85	8.5	14	>12	NA	128	[7]
CB	4	75	5.5	18	20.6	13.9	256	[12]
CB	4	82.5	5.3	9.7	23	5.9	100	[11]
CB	4	84	5.6	12.7	15.1	12	38.4	[13]
Cas(meas)	1	67.2	9.2	9.0	12.3	9.1	14	This work
Cas(sim)	2	73.5	9.2	14.2	15.7	11.7	28	This work
Cas(meas)	2	72	9.5	17.0	18.6	12	84	This work
Topology	Cascade	Freq [GHz]	G [dB]	P_{1dB} [dBm]	P_{sat} [dBm]	PAE [%]	L_g [μm]	Ref
CS^*	2x4	94	8.9	NA	26.3	20	0.15	[15]
CS^*	1x1x2	75-110	>13	NA	16.5	>6.0	0.1	[16]
CS^*	1x1x2	140-170	>12	10	12	~5.5	0.1	[17]

Table 2.1: Summary of reported power amplifiers based on InP DHBT and InP HEMT technologies. The sign * represents the designs based on InP HEMT; N-way means n-way parallel power combining; G is the linear power gain; P_{1dB} is the output 1dB compression point; P_{sat} is the saturated output power; PAE represents the power added efficiency; A_e is the emitter area; L_g means the length of gate strip.

counterparts [15–19], InP DHBT technology allows the development of a single-chip solution with high level of integration. Compared with SiGe HBT and CMOS technology, InP DHBT devices generally show better voltage handling ability, which means a higher load impedance for maximum output power and broadband matching [8]. For typical E-band power amplifier specifications: $P_{1dB} > 20$ dBm, power-added efficiency (PAE) > 10 %, linear gain > 12 dB and low harmonic and intermodulation distortions, InP DHBT devices can compete with that of HEMT devices [13, 14, 20].

The content of this chapter is divided into several sections: Section 2.2 starts with submicron InP DHBT device characterization. Section 2.3 shows the measurement results from a previously designed PA using the standard cascode configuration. Potential problems in the previous design are discussed. Section 2.4 presents the design technique of using interstage matched

cascode configuration. To improve the output power, wideband power combining technique is introduced in Section 2.5. Simulation and measurement results from single and two-way combined PAs based on single-finger and multi-finger devices are presented in Section 2.5 and Section 2.6. The mm-wave power amplifier analysis in terms of even/odd-mode instability is extensively discussed in Section 2.7. The universal amplifier stability detection methods based on the two-port K-factor, linear three-port μ factor, pole-zero identification, circuit modal analysis, and normalized determinant functions are compared. The stabilization techniques employed are verified by the measurement results from fabricated power amplifier chips. Section 2.8 gives the summary for this chapter.

2.2 InP DHBT device characterization

The submicron InP DHBT devices used in this work are from the III-V Lab in Marcoussic, France. The feature size of the technology is $0.7 \mu\text{m}$. We consider the single-finger device with emitter area of $0.7 \times 10 \mu\text{m}^2$. The composite collector, consisting of an InGaAs spacer, InGaAsP layers, and an delta-doped InP region, has been optimized for high breakdown voltage and high cut-off frequency. Fabricated devices show a breakdown voltage $BV_{ceo} > 4.75 \text{ V}$ and cut-off frequency f_T in the range of 250-300 GHz at a collector current density of $J_c = 7 \text{ mA}/\mu\text{m}^2$ and a collector-emitter voltage of $V_{ce} = 1.6 \text{ V}$. The maximum oscillation frequency f_{max} is slightly lower at around 240 GHz with the same bias condition. The large-signal model in Agilent ADS [21] is used for circuit designs.

To deliver the largest output power, the optimum DC operation point (Q-point) should be chosen for each device. The bias point of InP DHBT devices is mainly restricted by thermal breakdown as indicated by the safe operation area (SOA). Thermal breakdown is measured experimentally to occur around $P_{diss} = 80 \text{ mW}$ for an InP DHBT single-finger device. The estimated SOA contour with a breakdown voltage at $BV_{ceo} = 4.75 \text{ V}$ puts limit on the choice of bias point. As shown in Fig.2.1, the chosen Q-point of $V_{ce} = 2.5 \text{ V}$ and $I_c = 20.0 \text{ mA}$ guarantees sufficient margin to the SOA limit. If a knee-voltage $V_{knee} = 1.0 \text{ V}$ is assumed, the maximum output power from a single-finger common-emitter device for class A operation is 15 mW (11.8 dBm) with optimum load impedance $R_{opt} = 75 \Omega$.

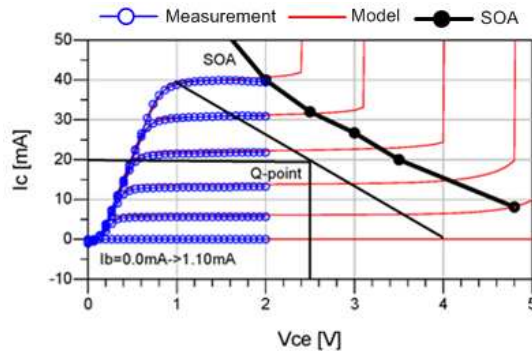


Figure 2.1: Bias point selection for a InP DHBT single-finger device with emitter area: $0.7 \times 10 \mu\text{m}^2$.

The measurement setup for large-signal characterization of InP DHBT devices is shown in Fig.2.2. It consists of an x6 active multiplier from RPG able to deliver +6 dBm output power in the frequency band from 65-110 GHz, an 0-50 dB attenuator, a 70-90 GHz medium power amplifier from RPG able to deliver approximately 15 dBm saturated output power, Anritsu bias-Tee's, and an Agilent power meter with W-band head. The through losses in the setup were measured to be around 16 dB at the lower E-band frequency range. This leads to an estimated maximum input power at the probe tips of +7 dBm.

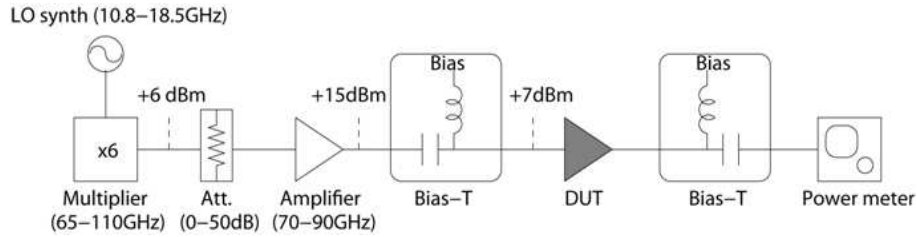


Figure 2.2: Measurement setup for large-signal characterization.

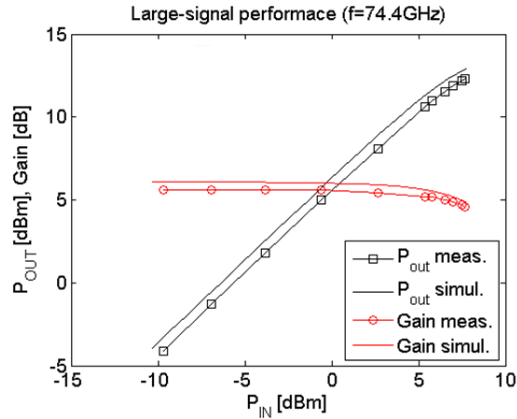


Figure 2.3: Large-signal performance from power sweeping measurement for a single-finger common-emitter device at 74.4 GHz with 50Ω terminations.

Fig.2.3 shows the measured and simulated large-signal performance for a single-finger InP DHBT device at 74.4GHz. The frequency 74.4 GHz was

chosen because the available measurement setup has minimum loss at this frequency. The device is biased at $V_{ce}=2.5$ V and $I_c=20.0$ mA for maximum output power. As a load-pull system is not available for device characterization at mm-wave frequencies, the device under test is terminated with 50Ω at the input and output for comparison with the device model. The measurements show an output power of approximately 12.3 dBm at 1dB compression with an associated power gain of 4.6 dB. The simulation result from the in-house developed device model follows the measurements very well and shows an output power of 12.9 dBm at 1dB compression with an associated power gain of 5.1 dB. The slightly difference for small signal power gain is due to the finite source and load reflection in the large signal measurement setup. An isolator could be used for the more accurate measurement. However, the associated power loss due to the isolator will limit the available input power to the device.

2.3 Measurements on previously designed PA

The microphotograph in Fig.2.4 shows a previously designed PA targeting the lower E-band frequency range(71-76 GHz) [22]. It consists of a four-way combined standard cascode configuration. The common-emitter device is biased for peak f_T around $V_{ce}=1.6$ V, while the common-base device is biased for maximum output power with $V_{ce}=2.55$ V. The current for each branch is $I_{cc}=20$ mA.

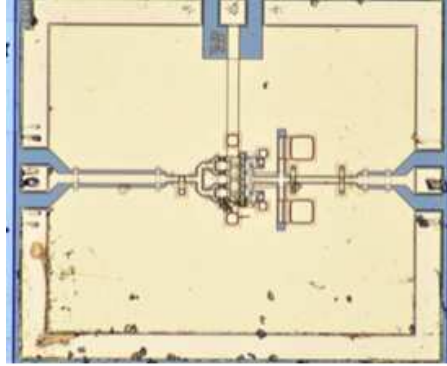


Figure 2.4: Microphotograph of the four-way combined standard cascode power amplifier with chip dimension $1250 \times 1500 \mu m^2$.

The measured large-signal characteristics are compared with simulations in Fig.2.5. The measurements and simulation show good agreement on small signal gain around 12 dB. However, the measured PA enters the power compression state much earlier than indicated by simulation. The achieved saturated output power in measurement is 11.3 dBm. There are two possible reasons for this effect: one is the nonlinear instability which depends on the input power levels [23–25]. However, the pole-zero identification based on the closed loop transfer function at the measured power compression point does not show unstable poles. Another possible reason is that the output impedance is shifted from the designed optimum load for maximum output power [22]. The designed power amplifier has two potential problems: 1) from the practical point of view, it is necessary to insert odd-mode stabilizing resistors R_{odd} between the combined power cells to suppress the odd-mode instability. 2) early power saturation of the standard cascode configuration is due to the common-base device. The low input impedance of the common-base device limits the voltage swing of the common-emitter stage.

At the power compression point, the common-emitter device delivers much less power than its optimum value. This further limits the overall saturated output power from the standard cascode configuration.

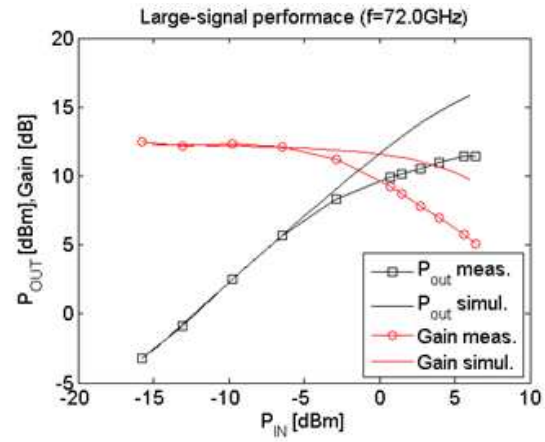


Figure 2.5: Measured large-signal characteristics of the four-way combined standard cascode power amplifier.

2.4 New efficient power cell design

In this section the power cell topologies for mm-wave InP DHBT power amplifiers are investigated and designed for best output power. The best topology is expected to depend on the given device technology. Among the issues to consider is the available power gain from the devices at mm-wave frequencies, breakdown-voltage and thermal limitations. The considered topologies here are CE, CB, and standard cascode configuration as shown in Fig.2.6. For mm-wave class-A type of power amplifiers it is common practice to optimize the load impedance for maximum delivered output power and the source impedance for maximum power gain. This is accomplished by performing load-pull simulations in Agilent ADS. For each topology single-finger devices are biased at the previously mentioned Q-point. The associated large-signal performance for each topology are summarized in Table2.2. It shows that the CE topology has the highest saturated output power of 14.9 dBm with a peak PAE of 38.0 %. However, the mm-wave power gain at 73.5 GHz is only 8.5 dB which is much lower than the others. The CB topology shows a larger linear power gain with 13.8 dB at 73.5 GHz but with less output power of 11.7 dBm at 1dB compression point. The cascode topology shows the highest power gain of 15.7 dB, P_{1dB} of 13.7 dBm and medium peak PAE of 22.2 %.

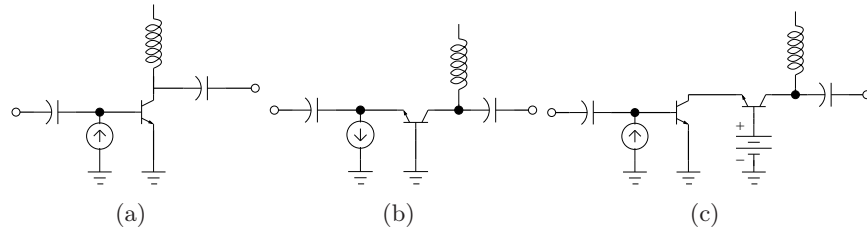


Figure 2.6: Three standard circuit topologies: (a) common-emitter, (b) common-base, (c) cascode configurations.

Another important criterion for the choice of circuit topology is the circuit stability. The comparison of two-port K-factor and maximum available gain (G_{max}) in Fig.2.7 shows that the CE configuration is unconditional stable at the design frequency but requires stabilization resistors to prevent the potential instability at the lower frequency region. The CB and cascode configurations are unstable across most part of the mm-wave region. Therefore, stabilization resistors are necessary for these topologies. This will reduce the corresponding values predicted in Table2.2. From the previous discussions,

	Common Emitter	Common Base	Cascode
G [dB]	8.5	13.8	15.7
P_{1dB} [dBm]	12.5	11.7	13.7
PAE [%]	38.0	38.0	22.2
P_{sat} [dBm]	14.9	13.5	14.2
Z_S [Ω]	19.5+j7.7	4.3-j18	18.8+j13.5
Z_L [Ω]	42.9+j35.6	37.1+j55.6	43.9+j48.8

Table 2.2: Comparison of three standard circuit topologies in term of G , P_{1dB} , peak PAE, P_{sat} , together with corresponding source and load impedance. The large-signal simulation is performed at 73.5 GHz without stabilization resistors and layout parasitics. All devices are biased on $V_{ce}=2.5$ V, $I_c=20$ mA.

the cascode topology is chosen for mm-wave PA designs in this work. Furthermore, the cascode topology has the advantage that it remains thermally stable once several single-finger HBTs are combined to form a power cell [26].

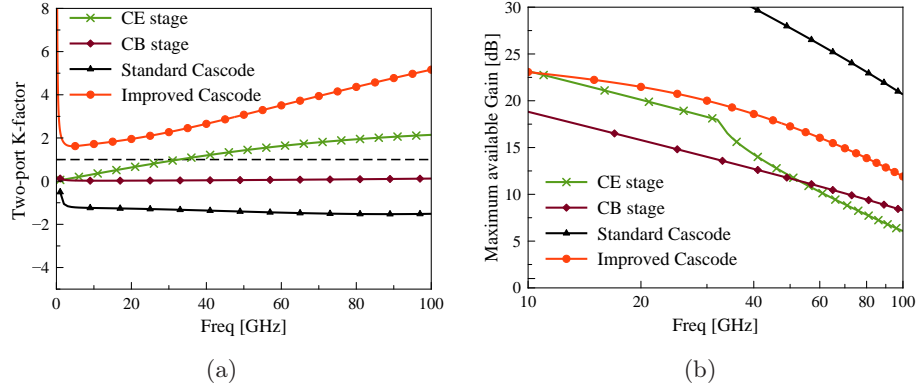


Figure 2.7: Comparison of K-factor and maximum available gain(G_{max}) for CE, CB and standard Cascode configurations. The improved K-factor of the inter-stage matched cascode configuration discussed later is also shown.

Fig.2.7(a) shows that the standard cascode has an issue with stability over a wide frequency range. The corresponding solutions depends on the frequency range. At low frequencies it can be improved by either series or parallel resistance at the input or output. This follows from the K-factor

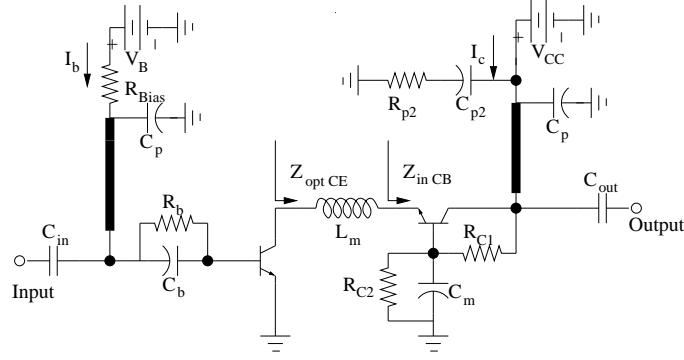


Figure 2.8: Cascode configuration with inter-stage matching between common-emitter and common-base devices.

calculation with its h-parameter,

$$K = \frac{2(\text{Re}\{h_{11}\} + \underline{\underline{R_s}})(\text{Re}\{h_{22}\} + \underline{\underline{g_L}}) - \text{Re}\{h_{21}h_{12}\}}{|h_{21}h_{12}|} \quad (2.1)$$

where h_{xx} defines the two-port h-parameters, R_s represents a series resistor at the input, and g_L represents a parallel resistor at the output. For our power cell, a base-ballasting network $R_b C_b$ and a resistor R_{Bias} in the CE base biasing circuitry are employed as shown in Fig.2.8. The base-ballasting network is used to solve the thermal runaway due to the positive feedback between the current and the junction temperature [27]. The parallel capacitor C_b is inserted with a value of $1/\omega C_b \ll R_b$ to ensure that the RF performance will not be significantly degraded. R_{Bias} from the base biasing circuitry can improve circuit stability at low frequencies. Its value has to be chosen to satisfy the condition of $R_{Bias} \gg 1/\omega C_p$ to minimize the power loss at high frequencies. Similarly, R_{p2} at the collector increases the low-frequency K factor, while the RF power loss is minimized by C_p . The overall stability is further improved by using a self-biasing network of R_{C1} and R_{C2} in the CB stage with minor influence on the linear power gain and PAE [28]. The resulting K-factor is compared with the other standard power cells in Fig.2.7(a). It shows unconditional stable operation for the whole frequency band. Additionally, two-port stability between the base and collector biasing ports is checked as well to avoid instability arising from the biasing lines [29]. More strictly, stability between the linear three-port network: RF input, RF output and collector biasing port is also calculated to guarantee unconditional stable operations under all circumstances even with an undefined impedance below the cutoff frequency of the waveguides used at RF

ports in the large-signal measurement [30].

In addition to the poor circuit stability, the other main drawback of the standard cascode configuration is its early power saturation [31–33]. This is due to the fact that the input impedance of CB devices is significantly different from the optimum load impedance of CE devices for maximum output power. As shown in Fig.2.9, the dynamic loading line from the CE device show much smaller voltage swing. The strong power mismatch drives the CB device into compression earlier, which results much more base current flowing through the CB device due to the forward biased base-collector junction. This further limits the thermal stability of the amplifier.

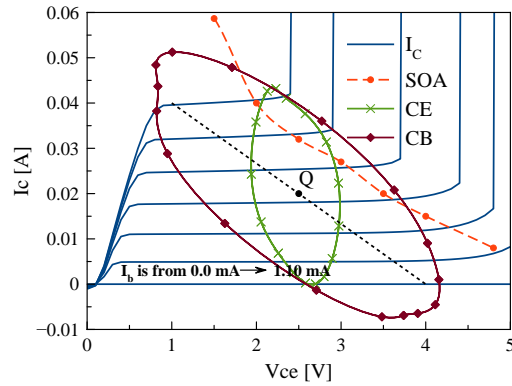


Figure 2.9: Dynamic loading line of the CE and CB devices in the standard cascode power cell are represented by the solid lines with symbols. The blue solid line represents the simulated output characteristic of a single-finger device model. The measured safe operation area(SOA) is indicated by the red dashed line.

To increase the linearity and total saturated output power, the inter-stage matching components L_m and C_m as shown in Fig.2.8 can be used to improve the power matching between the two stages. To investigate the functionality of C_m and L_m , input impedance looking into the emitter of CB devices and its transfer function from emitter to collector are analyzed. The simplified equivalent small-signal circuit in Fig.2.10 is used for derivations. The internal feedback networks $Z_{bci} = R_{bci}/(1 + sC_{bci}R_{bci})$ and $Z_{bcx} = R_{bcx}/(1 + sC_{bcx}R_{bcx})$ are ignored for now.

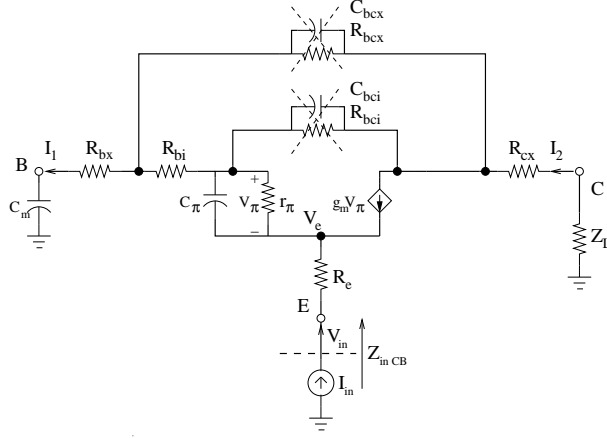


Figure 2.10: Equivalent small-signal circuit of the CB device. The relevant component values are extracted at $I_c=20$ mA and $V_{ce}=2.50$ V: $C_\pi=346.4$ fF, $r_\pi=50.2$ Ω , $R_{bi}=20.7$ Ω , $R_{bx}=6.8$ Ω , $R_e=4.0$ Ω , $R_{cx}=4.0$ Ω , $g_m=773$ mS, $R_{bcx}=10.0$ k Ω , $R_{bci}=73.5$ k Ω , $C_{bcx}=12$ fF, $C_{bci}=3.3$ fF, and C_m is swept up to 200 fF.

From the simplified equivalent circuit in Fig.2.10, the current flowing through the collector is

$$I_2 = -g_m I_1 Z_\pi \quad (2.2)$$

and the node voltage V_e is calculated as

$$V_e = I_1 (Z_\pi + Z_{bs}) \quad (2.3)$$

where $Z_\pi = r_\pi / (1 + s r_\pi C_\pi)$, $Z_{bs} = R_{bi} + R_{bx} + Z_{Cm}$, and $Z_{Cm} = 1/s C_m$. From Kirchhoff current law, the current relationship between all branches can be established as

$$I_1 = I_{in} + I_2 \quad (2.4)$$

To calculate the input impedance, the total voltage at the testing current source I_{in} is

$$V_{in} = I_{in} R_e + V_e \quad (2.5)$$

By solving the relevant linear equations listed above, the input current and voltage relationship can be written as

$$Z_{in,CB} = R_e + \frac{Z_\pi + Z_{bs}}{1 + g_m Z_\pi} \quad (2.6)$$

For the standard CB configuration with an infinite C_m , $Z_{in,CB}$ in Eq.2.6 can be simplified to be

$$Z_{in,CB} \approx R_e + \frac{1}{\frac{1}{Z_\pi} + g_m} \simeq R_e + r_e \quad (2.7)$$

with the assumption of $Z_\pi \gg Z_{bs}$ and $g_m \gg 1/Z_\pi$. This is the well-known solution at low frequencies for a standard CB configuration. For the case with a finite C_m , the real part of $Z_{in,CB}$ from Eq.2.6 is

$$Re(Z_{in,CB}) = R_e + \frac{(r_\pi + R_b + r_\pi^2 g_m + r_\pi R_b g_m + \omega^2 C_\pi^2 r_\pi^2 R_b) + \frac{C_\pi}{C_m} r_\pi^2 g_m}{\omega^2 C_\pi^2 r_\pi^2 + r_\pi^2 g_m^2 + 2r_\pi g_m + 1} \quad (2.8)$$

where $R_b = R_{bx} + R_{bi}$. The validity of the equation can be proofed by checking $Re(Z_{in,CB})|_{\omega \rightarrow 0} = R_e + (r_\pi + R_b)/(1 + r_\pi g_m)$ and $Re(Z_{in,CB})|_{\omega \rightarrow \infty} = R_e + R_b$. It can be seen From Eq.2.8 that $Z_{in,CB}$ is independent of the load impedance at the collector due to the ignored base-collector feedback networks. Fig.2.11 shows the numerical responses of $Re(Z_{in,CB})$ for a wide frequency range based on Eq.2.8. It indicates that the large impedance transformation ratio can be achieved by reducing C_m to a minimum. The dashed line represents the case with an infinite large value of C_m . The high frequency response increases and approximates to be $R_{bx} + R_{bi} + R_e$ as expected due to the short-circuit base-emitter junction.

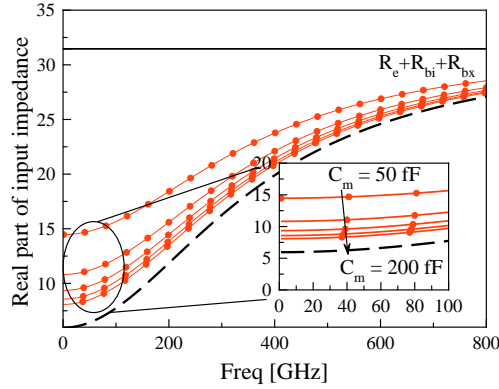


Figure 2.11: Numerical response of the real part of the input impedance for the simplified CB device shown in Fig.2.10.

The Influence of intrinsic and extrinsic feedbacks network from Z_{bci} and Z_{bcx} on the input impedance can be taken into account by re-solving the

current equations at each relevant circuit node. The derived input impedance of the CB device for the general situation is shown in Eq.2.9,

$$Z_{in,CB} = R_e + \frac{Z_\pi^2((-KMN R_{bi}^2 + N)Z_{bci}^2 Z_{bcx}^2 + MR_{bi}^2 Z_{bci}^2) + KR_{bi}^2 Z_{bcx}^2 + (-Kg_m R_{bi}^2 Z_{bcx} - g_m R_{bi} Z_{bci} + 2R_{bi})Z_{bci} Z_{bcx}}{(Z_\pi g_m + 1)((NZ_\pi + KN R_{bi}^2 - KMN Z_\pi R_{bi}^2)Z_{bci}^2 Z_{bcx}^2 + (-1 + MZ_\pi)R_{bi}^2 Z_{bci}^2 + KZ_\pi R_{bi}^2 Z_{bcx}^2 + 2Z_\pi R_{bi} Z_{bci} Z_{bcx})} \quad (2.9)$$

where

$$K = \left(\frac{1}{R_{bi}} + \frac{1}{Z_{bcx}} + \frac{1}{R_{bx} + Z_{Cm}} \right)$$

$$M = \left(\frac{1}{R_{bi}} + \frac{1}{Z_{bci}} + \frac{1}{Z_\pi} \right)$$

$$N = \left(\frac{1}{R_{cx} + Z_L} + \frac{1}{Z_{bci}} + \frac{1}{Z_{bcx}} \right)$$

The validity of Eq.2.9 can be proofed by setting Z_{bci} and Z_{bcx} to infinity, and then it is equal to Eq.2.6 with the corresponding updated K , M and N . To have more insight on the feedback effect, the condition of finite Z_{bci} is applied on Eq.2.9. The derived input impedance with only Z_{bci} is,

$$Z_{in,CB(Z_{bci})} = R_e + \frac{\overbrace{(R_{cx} + Z_\pi + Z_L + Z_{bci} + R_{cx}Z_\pi g_m + Z_\pi Z_L g_m)} Z_{Cm} + P}{(Z_\pi g_m + 1)(R_{cx} + Z_L + Z_{Cm} + R_{bi} + R_{bx} + Z_{bci})} \quad (2.10)$$

where

$$P = (R_{cx} + Z_\pi + Z_L + Z_{bci})(R_{bi} + R_{bx}) + (R_{cx} + Z_L + Z_{bci} + g_m(Z_L R_{bx} + R_{cx} R_{bi} + Z_L R_{bi} + R_{cx} R_{bx}))Z_\pi$$

It can be seen from the numerator of the derived $Z_{in,CB}(Z_{bci})$ in Eq.2.10 that the input impedance is increased due to the finite feedback effect, and the load at the collector is also reflected to the emitter. The DC analysis on $Z_{in,CB}$ shows a direct relationship with Z_{bci} and the collector load:

$$\begin{aligned} & \frac{(R_{cx} + Z_\pi + Z_L + Z_{bci} + R_{cx}Z_\pi g_m + Z_\pi Z_L g_m)Z_{Cm}}{(Z_\pi g_m + 1)Z_{Cm}} \\ &= R_e + \frac{1}{g_m} + \underbrace{\left(\frac{R_C + Z_L|_{\omega=0} + R_{bci}}{g_m R_{be}} + R_C + Z_L|_{\omega=0} \right)} \quad (2.11) \end{aligned}$$

As compared with Eq.2.7, an increase of impedance level can be seen due to the last term. Both feedbacks at the base-collector junction and the load at the collector contribute to the increased impedance level. The influence of different mechanisms on $Z_{in,CB}$ are summarized in Fig.2.12. The numerical responses are based on the equivalent circuit model from Fig.2.10 with a fixed $C_m=65$ fF and $Z_L=44+j67 \Omega$. Fig.2.12 shows that the derived Eq.2.9 is accurate and the effect of using finite C_m to increase the input impedance is enhanced by the base-collector feedback networks. As compared with Fig.2.17(c), the combination effect of C_m and the base-collector feedbacks has a much larger impedance transformation ratio for the whole frequency band. At the lower band, due to the open-circuit of Z_{bcx} and Z_{bci} , the self-biasing network element $R_{C1}=400 \Omega$ and $R_{C2}=1000 \Omega$ improves the impedance level. At the high end of frequency band, the slightly lower ratio is due to the fact of multiple feedback networks in parallel.

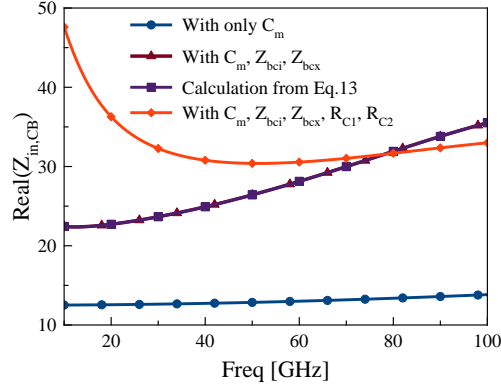


Figure 2.12: Numerical influence on the real part of $Z_{in,CB}$ due to different feedback mechanisms.

The consequence of input impedance optimization is a reduction of power gain. To analyze this in more details, transfer functions from the emitter to the collector in Fig.2.10 is derived. To calculate the transfer function, the current source is replaced by a voltage source V_S with an internal impedance Z_S . For the case with infinite large C_m , from the node equations at the collector and emitter:

$$V_o = g_m \frac{V_e Z_\pi}{R_b + Z_\pi} Z_L \quad (2.12)$$

$$\frac{V_e}{R_e + Z_S} + \frac{V_e}{R_b + Z_\pi} + g_m \frac{V_e Z_\pi}{R_b + Z_\pi} = \frac{V_S}{R_e + Z_S} \quad (2.13)$$

transfer function can be derived as:

$$\frac{V_o}{V_S} = \frac{g_m r_\pi Z_L}{s C_\pi r_\pi (R_e + R_b + Z_S) + R_e + r_\pi + R_b + Z_S + (R_e + Z_S) r_\pi g_m} \quad (2.14)$$

where $R_b = R_{bx} + R_{bi}$. For the case with a finite C_m : by simply replacing R_b with $Z_{bs} = R_b + Z_{C_m}$ in Eq.2.12 and Eq.2.13, the corresponding transfer function can be rewritten as,

$$\frac{V_o}{V_S} = \frac{s g_m r_\pi C_m Z_L}{s^2 a + s b + 1} \quad (2.15)$$

where

$$a = C_m C_\pi r_\pi (R_e + R_b + Z_S)$$

$$b = C_\pi r_\pi + C_m (R_e + r_\pi + R_b + Z_S) + (R_e + Z_S) C_m r_\pi g_m$$

Eq.2.15 indicates that an extra transmission zero at DC is introduced by C_m , and this is due to the fact of a floating base. The numerical responses by sweeping C_m up to 200 fF are summarized in Fig.2.13. It can be seen that below 100 GHz, a finite C_m reduces the power gain of the CB stage. However, for high frequencies with $1/\omega C_m \ll 1$, the transfer response converge to the ideal CB case as indicated by the dashed line. It seems that power gain reduction is the main consequence of the interstage matched cascode topology.

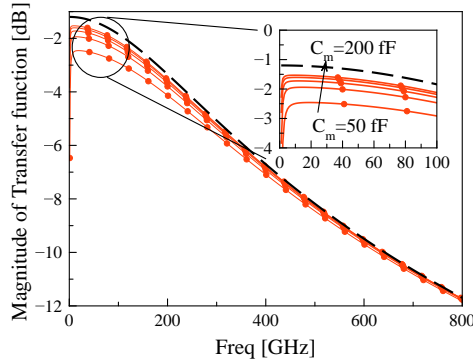


Figure 2.13: Numerical response of the transfer function for the CB device based on Eq.2.15.

From the analysis above, it can be concluded that two main drawbacks of the standard cascode topology are: poor circuit stability and early power

saturation. The series and parallel resistance at the base and collector together with a base-ballasting network and a self-biasing network can be used to improve the circuit stability over the whole frequency band. The early power saturation due to the power mismatch between CE and CB devices can be reduced by optimizing the input impedance of CB devices. This can be realized by using a finite base capacitance and an external feedback from self-biasing network at the CB stage. Analytical expressions for the input impedance are derived for the cases with/without feedback networks from the base-collector junction. As indicated, the feedbacks enhance the effect of finite capacitance at the base of the CB device. Together with parasitic inductance L_m arising from the interconnection between CE and CB devices as shown in Fig.2.8, $Z_{in,CB}$ can be transformed toward to the optimum load of CE stage ($Z_{opt,CE}$). The determination of component value for C_m and L_m has to compromise among the location of $Z_{opt,CE}$, gain reduction, and physical implementation of matching components. To demonstrate the use of the interstage matched cascode technique at mm-wave frequencies, three InP DHBT based power amplifiers are implemented for verification.

2.4.1 Common-emitter stage

Fig.2.14 shows the layout of CE stage. The open stub near the device is used for interconnection of an odd-mode stabilization resistor R_{odd} . For even-mode analysis, it presents an extra capacitive load. The input part includes a base-ballasting network with component values of $R_b=250\ \Omega$ and $C_b=117\ \text{fF}$. The choice of component value is based on the compromise among thermal feedback, power loss, and circuit stability. Fig.2.15(a) shows the extracted capacitance C_b from the layout. The resonance effect at high frequencies is due to the series inductance 29.4 pH from the access lines. Fig.2.15(b) and Fig.2.15(c) show power transmission efficiency of the base-blasting network and stability factor of the CE stage with different R_b . For a given input bandwidth, power transmission efficiency defined as $S_{21}^2/(1 - S_{11}^2)$ is one of the criterions to choose R_b for a fixed C_b . The associated low frequency K-factor below 20 GHz is emphasized in Fig.2.15(c). Due to the fact that K-factor is partially below one, source and load stability circles in Fig.2.15(d) are calculated to confirm the appropriate choice of Z_S and Z_L for large-signal simulations.

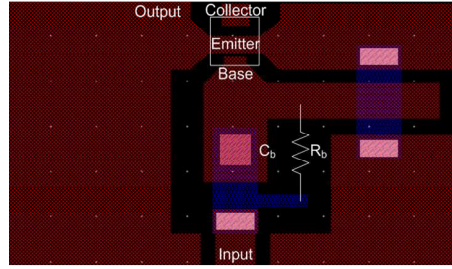


Figure 2.14: Layout of CE stage with a base-ballasting network of $R_b/(1 + j\omega R_b C_b)$ and an open stub for interconnection of odd-mode stabilization resistor.

G[dB]	P_{1dB} [dBm]	PAE [%]	P_{sat} [dBm]	Z_S [Ω]	Z_L [Ω]
7.45	12.9	34.0	14.9	$19.1+j11.1$	$33.8+j34.2$

Table 2.3: Large-signal characteristics of CE stage including layout parasitics at 73.5 GHz.

Large-signal performance of CE stage is simulated by using EM circuit co-simulation in Agilent ADS. In this approach active components are connected

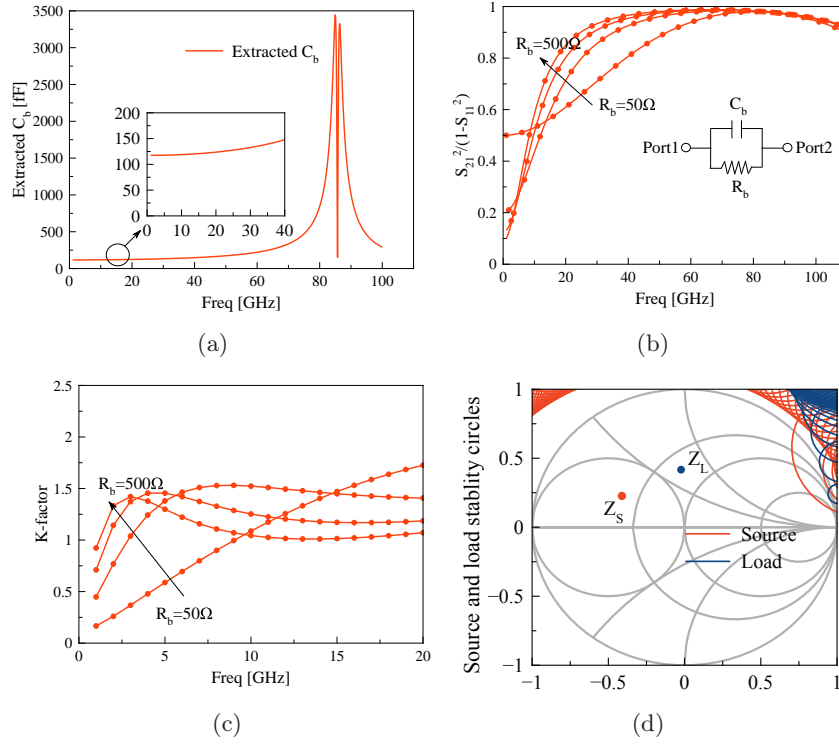


Figure 2.15: (a) Extracted capacitance C_b from the layout (b) and (c) is the transmission efficiency of the base-blasting network and the associated low-frequency K-factor of the CE stage by sweeping R_b , respectively (d) source and load stability circles (1-110 GHz) with fixed $R_b=250 \Omega$ and $C_b=117$ fF. Z_S and Z_L are from Table2.3.

to passive part of the circuit using non-calibrated ports in the EM simulator based on method of moments (MoM). MIM capacitors are part of the passive structure. The resistors are simulated with ideal circuit components. The corresponding large-signal performance is summarized in Table2.3. Compared to Table2.2, source impedance Z_S is shifted due to the open stub. The optimum load impedance Z_L is tuned to have the same real part as the input impedance of CB stage to simplify the inter-stage matching circuit later.

2.4.2 Common-base stage

As shown in Fig.2.16, the self biasing network with R_{C1} and R_{C2} is included into CB stage to improve circuit stability and input impedance level as analyzed before. Voltage at the base of the CB device is set to be 3.4 V for $V_{CC}=5$ V and the ratio between R_{C1} and R_{C2} is 0.4. The value of R_{C1} is chosen by checking the associated K-factor and G_{max} as shown in Fig.2.17(a) and Fig.2.17(b). The value of interstage matching component C_m is chosen by calculating the input impedance and G_{max} as indicated in Fig.2.17(c) and Fig.2.17(d). The component values after optimization are $R_{C1}=400 \Omega$, $R_{C2}=1000 \Omega$, and C_m is 100 fF at 73.5 GHz. The final circuit performance and input/output stability circles is shown in Fig.2.17(e) and Fig.2.17(f), respectively.

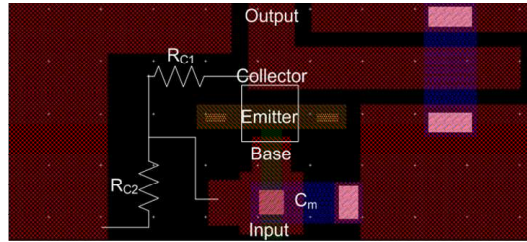


Figure 2.16: Layout of CB stage with a self-biasing network of R_{C1} , R_{C2} , an inter-stage matching capacitor C_m .

The extracted C_m in Fig.2.17(e) from layout at E-band is about 100 fF. The simulated K-factor is not well above one for the whole frequency range. The source and load stability circles are checked in Fig.2.17(f) to ensure the impedance used for large-signal simulation stay in the stable area. The relevant large-signal performance is summarized in Table2.4. Compared to the standard CB cell listed in Table2.2, power gain reduces due to the finite C_m and self-biasing network. The variation of Z_S and Z_L is due to the open stub and interstage matching consideration.

G[dB]	P_{1dB} [dBm]	PAE [%]	P_{sat} [dBm]	Z_S [Ω]	Z_L [Ω]
4.9	12.7	18.7	14.3	31.1-j25.1	13.3+j35.7

Table 2.4: Large-signal characteristics of the CB stage including layout parasitics at 73.5 GHz.

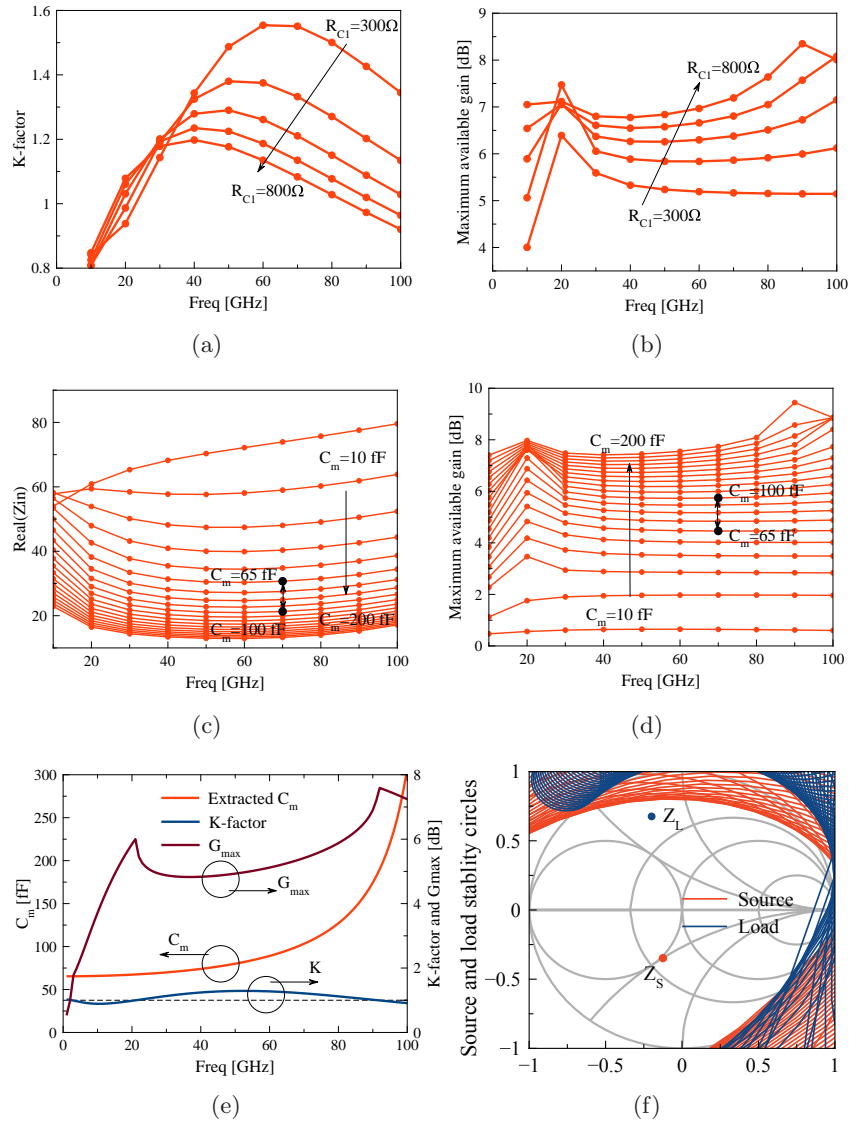


Figure 2.17: (a) and (b) For a fixed $C_m=100\text{ fF}$ and resistance ratio of 0.4 between R_{C1} and R_{C2} , K-factor and G_{max} is checked by sweeping R_{C1} from 300 to 800 Ω respectively (c) and (d) real part of input impedance and G_{max} of the CB device with swept C_m (e) extracted capacitance C_m from Y-parameter together with relevant K-factor and G_{max} by fixing $R_{C1}=400\text{ }\Omega$ and $R_{C2}=1000\text{ }\Omega$ (d) source and load stability circles (1-100 GHz) with component values after optimization. Z_S and Z_L are from Table 2.4.

2.4.3 Cascode with interstage matching

For interstage power matching, L_m arising from the interconnection line between the CE and CB device is used to increase the imaginary part of $Z_{opt,CE}$ and match it to $Z_{in,CB}$. The associated schematic for the whole chip with input and output matching circuits is shown in Fig.2.18.

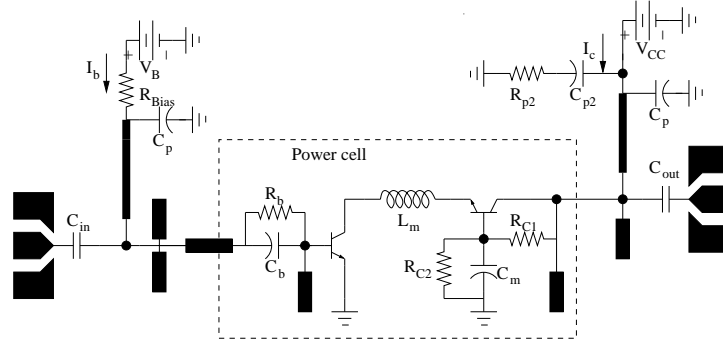


Figure 2.18: Single-branch power amplifier with the interstage matched cascode power cell.

Table 2.5 summarizes the large-signal characteristics of the power cell with an inter-stage matching network. Compared with the previous results for the standard cascode cell in Table 2.2, reduced linear gain and output power at 1dB compression point is observed. However, the major performance improvement is the saturated output power where the cascode cell with inter-stage matching network is able to deliver 2.2 dB more than the standard cascode cell. The associated dynamic loading lines for both CE and CB devices are shown in Fig. 2.19. Compared to the one in Fig. 2.9 from the standard cascode, the voltage swing and output power of the common-emitter device is improved.

G[dB]	P_{1dB} [dBm]	PAE [%]	P_{sat} [dBm]	Z_S [Ω]	Z_L [Ω]
13.2	13.2	20	16.4	19.1+j11.1	13.3+j35.7

Table 2.5: Large-signal characteristics of the power cell from the dash-line box in Fig. 2.18 at 73.5 GHz.

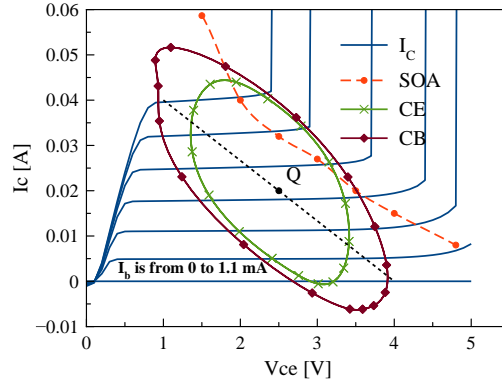


Figure 2.19: Dynamic loading line of the CE and CB devices in the interstage matched cascode power cell are represented by the solid lines with symbols. The blue lines represent the simulated DC characteristics from the device model. The measured safe operation area(SOA) is indicated by the red dashed line.

Fig.2.20 shows microphotography of the designed single-branch power amplifier with the interstage matched technique. The measured S-parameters from several chips on the same wafer show little fabrication spreading. The center frequency of the power amplifier is down shifted with 7 GHz. This is due to that the capacitive loading from the ground bridges is not well modeled. Fig.2.21 show that simulated S-parameters with different dielectric thickness from $0.8 \mu\text{m}$ to $1.0 \mu\text{m}$ between the signal strip and bridge layers. EM-circuit co-simulation agrees very well with the measurements up to 95 GHz for a dielectric thickness of $1.0 \mu\text{m}$. The large-signal performance is characterized with the same setup as used for device characterization shown in Fig.2.2. The measured output power and efficiency at 67.2 GHz is compared with simulation results from the harmonic balance in Fig.2.22. The measurement follows the simulations well and demonstrates an output power of 9.0 dBm at 1dB compression point, a peak efficiency of 9.1 % and a saturated output power 12.3 dBm with associated 9.2 dB linear gain. The fast drop of gain and efficiency in the saturation region is due to the inaccuracy of device model within deep compression.

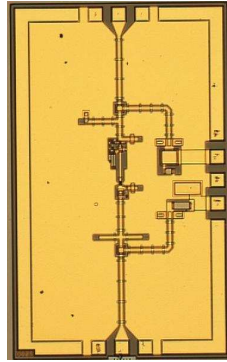


Figure 2.20: Microphotography of designed single-branch interstage matched cascode power amplifier with chip dimension of $1500 \times 2400 \mu\text{m}^2$.

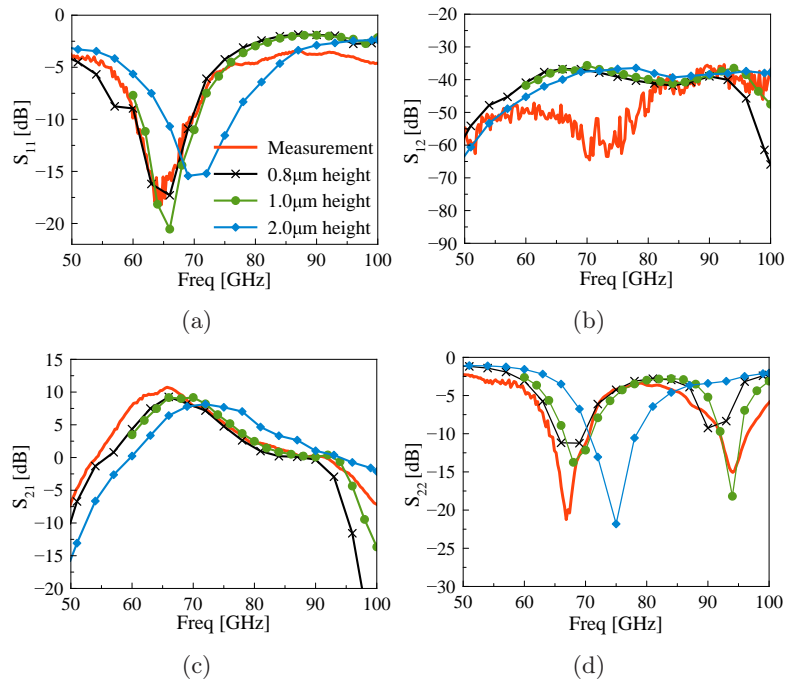


Figure 2.21: Comparison of measured and simulated S-parameters with different dielectric thickness. The DC biasing points used for measurement are: $V_{ce}=5.0$ V and $I_c=22$ mA.

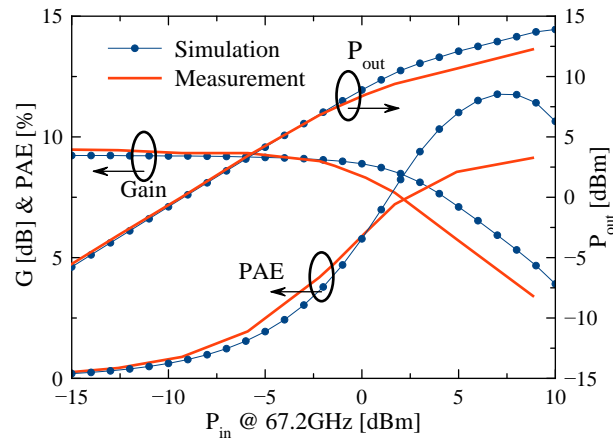
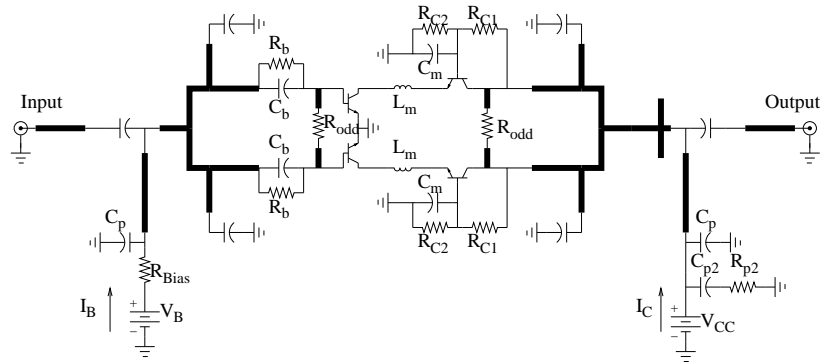


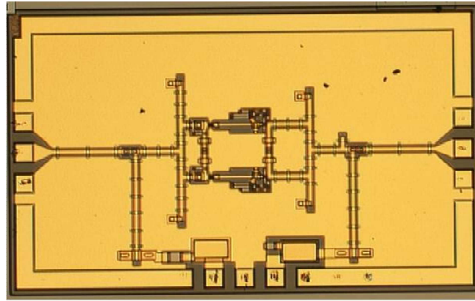
Figure 2.22: Large-signal characterization of single-branch PA based on single-finger devices. The comparison is done at 67.2 GHz due to the down-shifting of the designed PA: the red solid line represents the measured output power, power gain, and efficiency; the blue line with symbol represents the corresponding simulated result.

2.5 Two-way combined single-finger cascode PA design

To increase the total output power, a two-way combined single-finger PA is implemented. The matching components are used inside of the power combination network to improve the amplifier bandwidth. The simulated small/large-signal performance of the designed power amplifier are summarized in this section. Fig.2.23 shows the schematic and microphotography of the chip layout. The stabilization R_{odd} resistors are inserted close to the transistors to suppress the odd-mode instability. The corresponding values are decided to be 15Ω based on the stability analysis discussed later in Section 2.7.



(a)



(b)

Figure 2.23: (a) Schematic of two-way combined power amplifier based on single-finger devices (b) Microphotography of the fabricated chip with dimension of $1500 \times 2400 \mu\text{m}^2$.

To increase the large-signal matching bandwidth and simplify the matching network, open and short-circuit stubs are utilized within the power combining network. To get a better insight into properties of the power combining network, a simplified analytical procedure is presented. In this approach, the phase of reflection coefficients at different reference planes is analyzed. As shown in Fig.2.24, the circuit under investigation includes an optimum load Y_{opt} , an open-circuit stub with electrical length of βl_1 , a piece of transmission line with electrical length of βl_2 , and a short-circuit stub with electrical length of βl_3 . Due to the symmetry, only half of the circuit for a two-way combining network is considered.

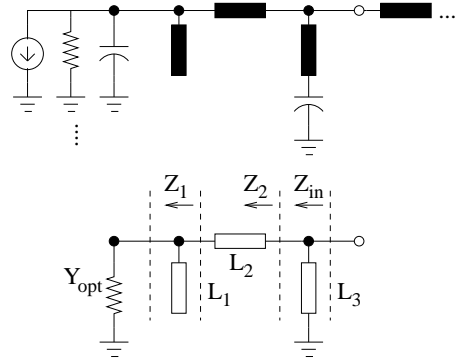


Figure 2.24: Simplified half of the proposed power combining network.

As well known, for a given load Z_{opt} or $1/Y_{opt}$, the impedance looking into a transmission line with electrical length of βl and characteristic impedance of Z_C is defined as.

$$Z_{in} = Z_C \frac{Z_{opt} + iZ_C \tan \beta l}{Z_C + iZ_{opt} \tan \beta l} \quad (2.16)$$

and the reflection coefficient is

$$\Gamma = \frac{\frac{Z_{opt} + iZ_C \tan \beta l}{Z_C + iZ_{opt} \tan \beta l} - 1}{\frac{Z_{opt} + iZ_C \tan \beta l}{Z_C + iZ_{opt} \tan \beta l} + 1} = -(Z_{opt} - Z_C) \frac{i \tan \beta l - 1}{(i \tan \beta l + 1)(Z_1 + Z_C)} \quad (2.17)$$

The phase of Eq.2.17

$$\angle(\Gamma) = \arctan\left(-\frac{2 \tan \beta l}{1 - \tan^2 \beta l}\right) = -2\beta l \quad (2.18)$$

has linear relationship with frequency and the high frequency part rotates faster. For wideband power matching purposes, it is always desirable to minimize the frequency dependency of phase variation. As shown in Fig.2.24, the impedance looking into the circuit with an open-circuit stub is equal to

$$Z_1 = \frac{1}{Y_{opt} + \frac{1}{(-iZ_C \cot(\beta l_1))}} \quad (2.19)$$

Together with an ordinary transmission line and a short-circuit stub, the input impedance can be expressed as

$$Z_{in} = \frac{1}{\frac{1}{Z_2} + \frac{1}{iZ_C \tan \beta l_3}} \quad (2.20)$$

where

$$Z_2 = Z_C \times \frac{Z_1 + iZ_C \tan(\beta l_2)}{Z_C + iZ_1 \tan(\beta l_2)} \quad (2.21)$$

By inserting Z_2 into Eq.2.20, the input impedance can be re-written as

$$Z_{in} = Z_C \tan \beta l_3 \frac{Z_1 + iZ_C \tan \beta l_2}{Z_C \tan \beta l_2 - iZ_1 + Z_C \tan \beta l_3 + iZ_1 \tan \beta l_2 \tan \beta l_3} \quad (2.22)$$

After substituting Z_1 from Eq.2.19, the reflection coefficient can be formulated as,

$$\Gamma = -\frac{-A + B + i(C - D)}{A + B + i(C + D)} \quad (2.23)$$

where

$$A = \cot \beta l_1 \tan \beta l_3 - \tan \beta l_2 \tan \beta l_3$$

$$B = Z_C (\cot \beta l_1 \tan \beta l_2 + \cot \beta l_1 \tan \beta l_3) Y_{opt}$$

$$C = -\cot \beta l_1 + \tan \beta l_2 + \tan \beta l_3 + \cot \beta l_1 \tan \beta l_2 \tan \beta l_3$$

$$D = Z_C (\cot \beta l_1 \tan \beta l_2 \tan \beta l_3) Y_{opt}$$

To simplify the analysis on Eq.2.23, assumptions are made: 1) $\beta l_1 = \beta l_2 = \beta l_3 = \beta l$ 2) the imaginary part of Y_{opt} can be taken into account by tuning the electrical length βl_1 of the open stub. Eq.2.23 can be simplified to

$$\Gamma = -\frac{(\tan^2 \beta l - 1 + 2K) + i(-\cot \beta l + 3 \tan \beta l - K \tan \beta l)}{(1 - \tan^2 \beta l + 2K) + i(-\cot \beta l + 3 \tan \beta l + K \tan \beta l)} \quad (2.24)$$

where K is the impedance ratio defined as $K = Z_C / \text{Re}(1/Y_{opt})$. Further derivations for conditions of $\beta l \ll 1$ and $K \gg 1$ or $K \ll 1$ show that phase

response still has linear frequency dependency. However, for the special case with impedance ratio K equal to one, the reflection coefficient reduces to be

$$\Gamma = -\frac{(\tan^2 \beta l + 1) + i(-\cot \beta l + 2 \tan \beta l)}{(-\tan^2 \beta l + 3) + i(-\cot \beta l + 4 \tan \beta l)} \quad (2.25)$$

Additional simplification can be made based on the condition of $\tan(\beta l) \approx \beta l$ and $\cot(\beta l) \gg \tan(\beta l)$ if $\beta l \ll 1$. This approximation is applied because it is always desirable to minimize the dimension of the power combining network due to power loss considerations. The reflection coefficient in Eq.2.25 is simplified to be

$$\Gamma = -\frac{1 - i\frac{1}{\beta l}}{3 - i\frac{1}{\beta l}} = -\frac{\beta l - i}{3\beta l - i} \quad (2.26)$$

The associated phase of Eq.2.26 is

$$\angle(\Gamma) = \arctan\left(-2\frac{\beta l}{3(\beta l)^2 + 1}\right) \quad (2.27)$$

With the condition of $\beta l > 0$, the phase in Eq.2.27 has the property of

$$\begin{aligned} -2\frac{\beta l}{3(\beta l)^2 + 1} &\geq \frac{-1}{\sqrt{3}} \Big|_{\beta l = \frac{1}{\sqrt{3}} = 33^\circ} \\ \Rightarrow \angle(\Gamma) &\geq 150^\circ \end{aligned} \quad (2.28)$$

where the last derivation is from the fact of $a+b \geq 2\sqrt{ab}$ if $a>0$ and $b>0$.

Eq.2.27 is the phase responses of reflection coefficient for the special case with the conditions: equal electrical length for each transmission line, $K=1$, and $0 < \beta l \ll 1$. As indicated in Eq.2.28, it has a minimum value of 150° if $\beta l = \frac{1}{\sqrt{3}} = 33^\circ$. From this special case, we can see that phase response of the proposed structure is different from the ordinary impedance transformation from Eq.2.18. Its frequency dependency is not linear any more but with ripples. If the phase at the lower and upper frequency boundaries is close, the reflection curve is folded on the Smith chart and can be explored for wideband matching purposes. To proof the derived formula, the simplified circuit in Fig.2.24 is simulated with component values: $Z_C = \text{Re}(1/Y_{opt}) = 50 \Omega$ and $\beta l = 33^\circ$ at 73.5 GHz. Fig.2.25(a) shows that the derived expression for input reflection coefficient in Eq.2.25 is correct. The value of Γ from Eq.2.27 does not capture all details due to the fact that $\beta l \ll 1$ is not valid

any more with increased frequencies. However, it shows an indication of slow phase response of the proposed structure. The simulated reflection coefficients for the proposed structure and the case with ordinary transmission lines are compared on Smith chart in Fig.2.25(b). As indicated, the benefit of wideband properties is quite obvious for the designed network.

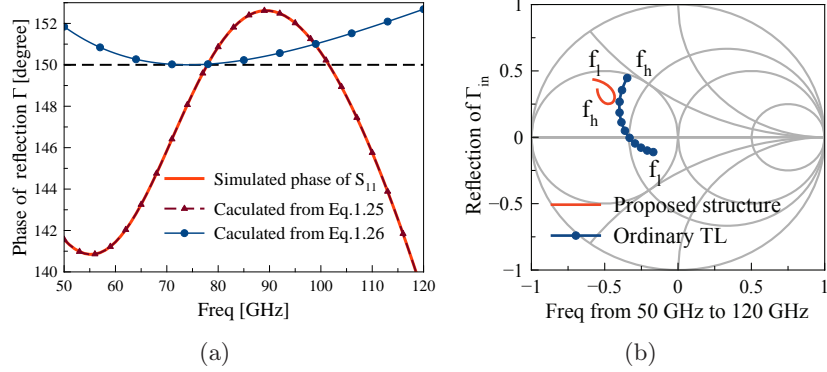


Figure 2.25: (a,b) Phase responses from the proposed structure in Fig.2.24 and reflection on Smith chart with $Re(1/Y_{opt})=Z_C=50 \Omega$ and $\beta l=33^\circ$ at 73.5 GHz.

Fig.2.26 shows a complete two-way power combining and matching network. With the conditions of $Re(1/Y_{opt})=Z_C=50 \Omega$ and $\beta l_1=\beta l_2=\beta l_3=33^\circ$ at 73.5 GHz, Eq.2.26 is used to calculate the reflection coefficient at this point: $\Gamma_3=\frac{1}{\sqrt{3}}e^{j150^\circ}$. Assuming that βl_4 has the same electrical length as the open-circuit stub, the remaining components in Fig.2.26 are derived to be $\beta l_5=20^\circ$, $\beta l_6=20^\circ$, and $C_s=35$ fF, respectively. These values are used as a starting point for the circuit optimization.

For the practical PA, the optimum load impedances of the power cell at Γ_1 in Fig.2.26 plane are collected from load-pull simulations from 69 to 79 GHz. The complex impedances are imported into ADS as a frequency dependent network. The real part of impedance shows little variation and is fixed to be 12.55Ω , while the imaginary part is reproduced by a fourth order polynomial as,

$$\text{Im}(Z_{opt}) = a_1 f^4 + a_2 f^3 + a_3 f^2 + a_4 f^1 + a_0 \quad (2.29)$$

where f is with unit of GHz and the other fitted coefficients are defined as: $a_1=-1.5048\text{e-}3$, $a_2=4.542137\text{e-}1$, $a_3=-5.136125\text{e+}1$, $a_4=2.5776293\text{e+}3$, and

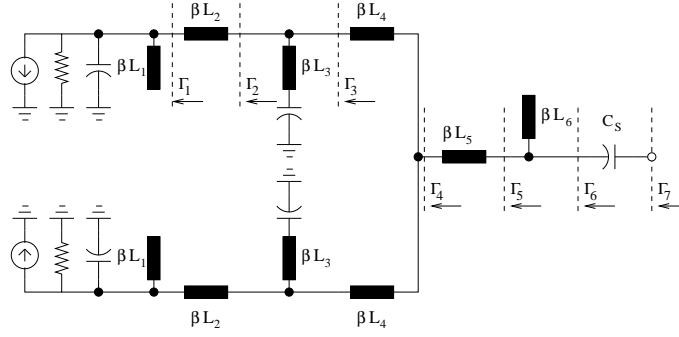


Figure 2.26: Two-way output power combining and matching network.

$a_5 = -4.838577e+4$. Fig.2.27 shows the fitted real and imaginary part of the optimum load at each individual frequency in band.

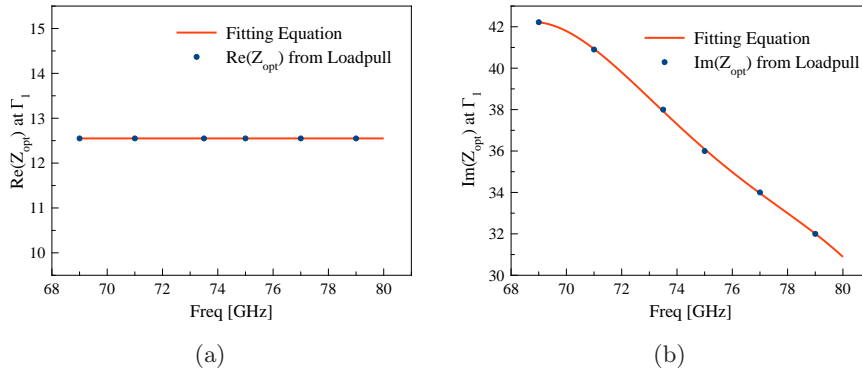


Figure 2.27: Comparison of (a) real and (b) imaginary part of Z_{opt} at Γ_1 from load pull simulation with the numerical values from fitting equation.

The electrical dimension of the relevant components in Fig.2.26 are optimized based on the initial values decided before. The reflections at different reference planes are shown in Fig.2.28(a). To evaluate the performance of the designed output network, EM numerical result is compared with circuit simulation by using ideal transmission lines in Fig.2.28(b). It shows good agreement and the difference is due to that the parasitics in the physical layout are not modeled in the circuit simulation. For 10 GHz targeting bandwidth, the output power combining network shows return loss better

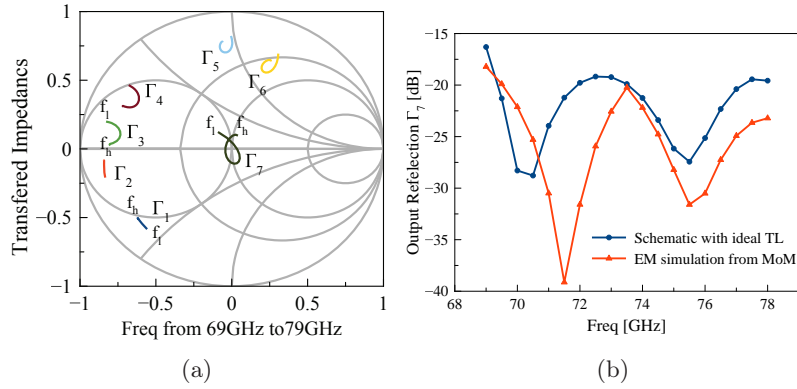


Figure 2.28: (a) Reflections at different reference planes (b) numerical results from EM numerical and circuit simulator.

than 18 dB.

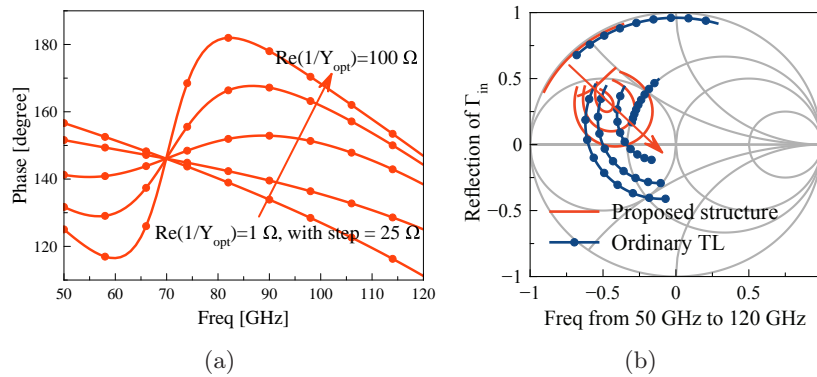


Figure 2.29: (a,b) Phase responses and reflection from the proposed structure in Fig.2.24 and on Smith chart with different $Re(1/Y_{opt})$ and $\beta l=33^\circ$ at 73.5 GHz.

To complete the discussion on Eq.2.24, the influence of different impedance ratio K is checked and the associated phase variation and reflections on Smith chart are summarized in Fig.2.29(a) and Fig.2.29(b). It can be seen that the proposed circuit topology works well for cases with $Re(1/Y_{opt})$ comparable to Z_C . However, for a low output impedance, frequency dependency of phase variation is still linear.

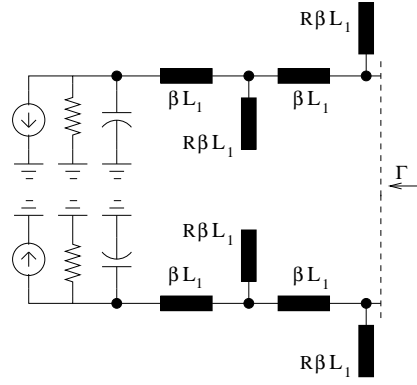


Figure 2.30: Two-way power combining network for large power devices with low $Re(1/Y_{opt})$.

To overcome this problem, the idea of using capacitive loaded transmission lines to form a low impedance line is considered. Fig.2.30 shows a modified version of combining network: the short-circuit stub is replaced with an open-circuit stub. Two sections are used to reduce the electrical length of the individual transmission line. To facilitate the analysis, both open stubs are set with an electrical length of $R \times \beta l_1$, where βl_1 is for the series ones. The associated reflection Γ by virtually combining two branches is derived as

$$\Gamma = \frac{Z_{in}/2Z_C - 1}{Z_{in}/2Z_C + 1} \quad (2.30)$$

where

$$Z_{in} = -Z_C \frac{A + iB}{C + iD}$$

$$A = \tan(\beta l_1) \tan(R\beta l_1) + \tan^2(\beta l_1) - 1$$

$$B = -2K \tan(\beta l_1) + K \tan^2(\beta l_1) \tan(R\beta l_1)$$

$$C = K - K \tan^2(\beta l_1) + K \tan^2(\beta l_1) \tan^2(R\beta l_1) - 3K \tan(\beta l_1) \tan(R\beta l_1)$$

$$D = 2 \tan(\beta l_1) + 2 \tan(R\beta l_1) - \tan(\beta l_1) \tan^2(R\beta l_1) - \tan^2(\beta l_1) \tan(R\beta l_1)$$

With the assumption of $\beta l_1 \ll 1$, further simplifications indicate that for high impedance ratio $K=5$ or 10 , a good starting point is that βl_1 is between 12° to 15° and R is between 2 to 3.75 at 73.5 GHz. It can be seen from Fig.2.31(a) and Fig.2.31(b) that this structure is suitable to combine power and transform impedance for extra large power devices: the phase

response does not has linear frequency dependency and additional transmission lines can be utilized for combining the power (rotating the reflection curve clockwise on Smith chart) and series capacitor for matching to 50Ω .

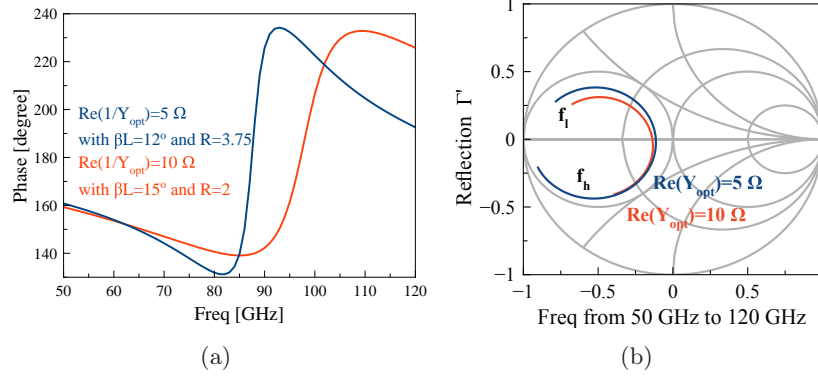


Figure 2.31: (a,b) Phase responses and reflection at Γ with $Re(1/Y_{opt})=5$ or 10Ω and $\beta l_1=12^\circ$ or 15° and different ratio R at 73.5 GHz.

The simulated small-signal performance of the two-way combined power amplifier is summarized in Fig.2.32. The simulated K-factor shows unconditional stable operation in the whole frequency band with a minimum value of 8.0 at 75.6 GHz. With layout parasitics, the amplifier shows a linear gain of 9.4 dB at 75.6 GHz with 3 dB bandwidth of 15 GHz.

The large-signal characteristics are shown in Fig.2.33. The simulation is performed at three different frequencies: 69 GHz, 73.5 GHz, and 79 GHz with the input power up to 15 dBm. As shown, the saturated output power for different cases has similar values. This further confirms the features of the wideband output matching technique. The predicted output power and PAE at 1 dB compression point is 14.3 dBm and 11.7 % with an associated linear gain of 9.4 dB at 73.5 GHz. The output power does not show saturation until an input power of 15 dBm. The measurement results are not presented for this chip due to failure of the transistors during fabrication.

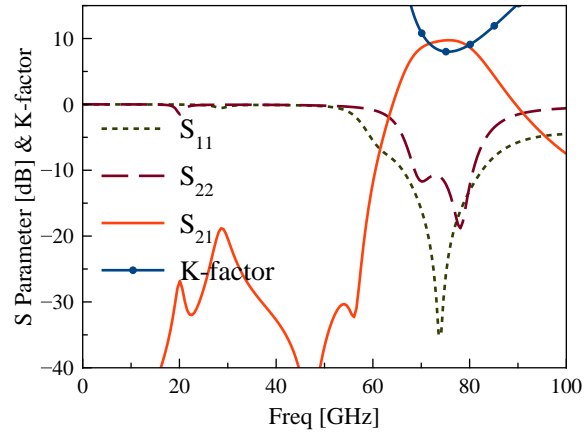


Figure 2.32: Small-signal performance of designed two-way combined PA with the DC bias conditions: $V_{CC}=5$ V, $I_C=45.6$ mA and $V_B=1.16$ V, $I_B=1.25$ mA.

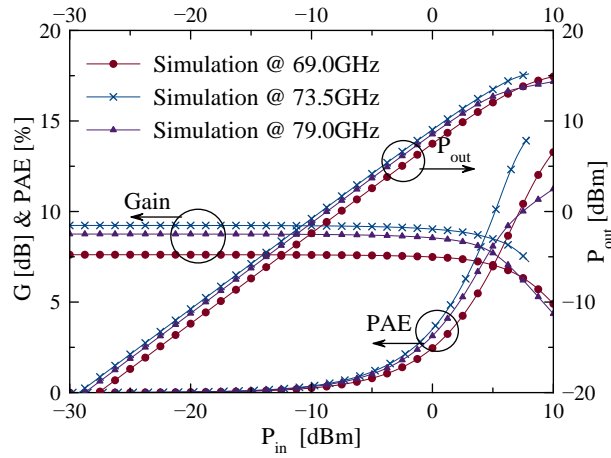


Figure 2.33: Large-signal performance of the designed PA at 69 GHz, 73.5 GHz, and 79 GHz with DC bias conditions: $V_{CC}=5$ V, $I_C=45.6$ mA and $V_B=1.16$ V, $I_B=1.25$ mA.

2.6 Two-way combined multi-finger PA design

To further improve the output power, multi-finger devices are preferred. The choice of finger number has to take the parasitic emitter inductance and thermal coupling between the fingers into account. Measurements on multi-finger devices indicate that parasitic emitter inductance of the three-finger device does not significantly degrade the RF performance. But thermal issues are specially important for multi-finger devices without base-ballasting resistor for each individual finger. A two-way combined power amplifier based on three-finger devices is designed and shown in Fig.2.34. The design employs the interstage matched cascode configuration discussed before.

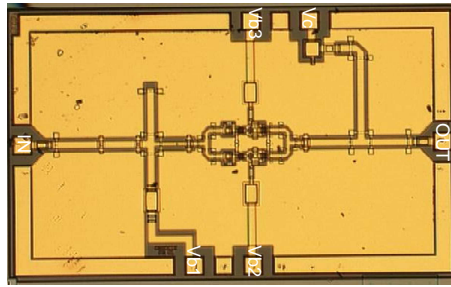


Figure 2.34: Microphotography of two-way combined PA based on three-finger devices with the chip dimension of $1500 \times 2400 \mu\text{m}^2$.

Three-finger devices have slightly worse thermal stability and lower current gain β compared with single finger devices. The measured power amplifier can only be biased at 76 % of the nominal collector current. Further increasing base current leads to the destruction of the transistors due to thermal breakdown. Even though the amplifier does not work at its nominal operation conditions, measurements show promising results. The measured S-parameters are compared with simulations in Fig.2.35. The downshifting of small-signal responses is due to the extra parasitics from non-calibrated ports used in EM circuit cosimulations. The relevant large-signal characterization is performed at 72 GHz with minimum difference for S_{21} . Fig.2.35(e) shows that the measured PA agrees well with the simulations and demonstrates an output power of 17.0 dBm at 1dB compression point, a saturated output power of 18.6 dBm and a peak efficiency of 12 % with 9.5 dB linear power gain.

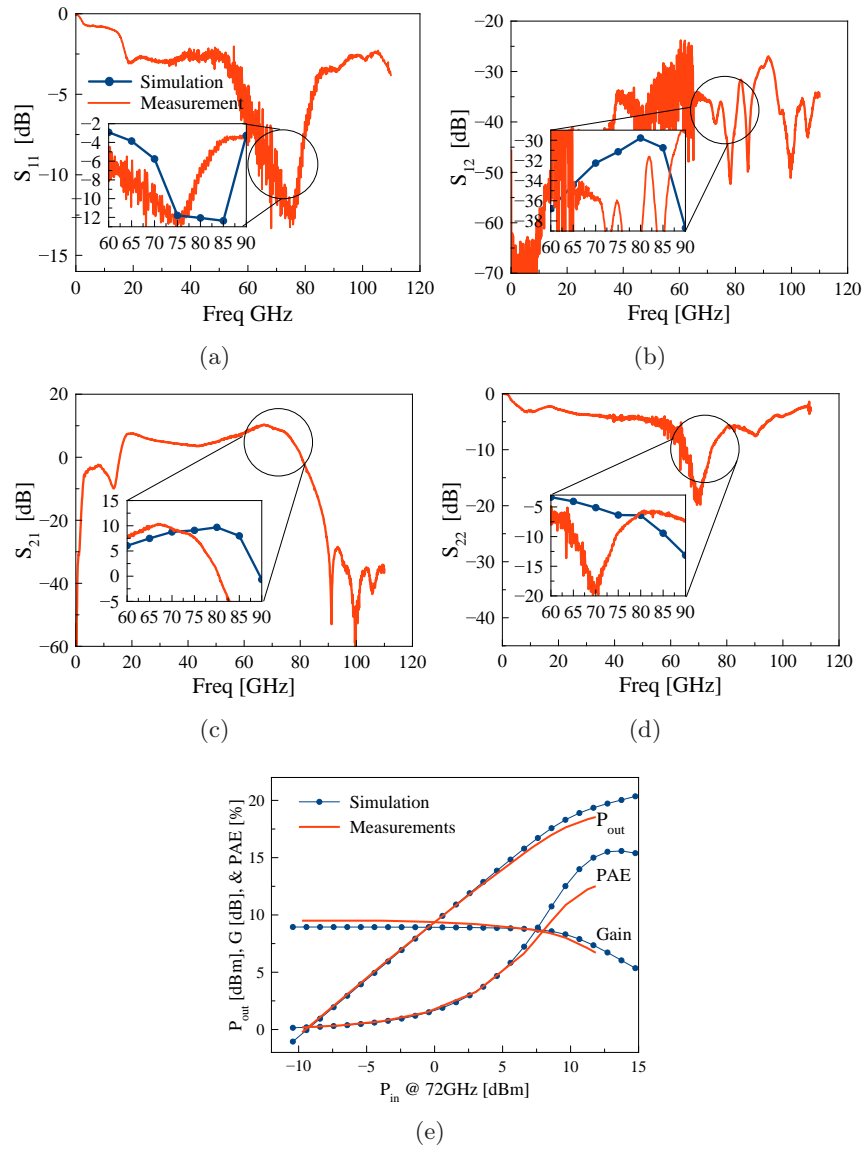


Figure 2.35: Measured small/large-signal performance at DC bias conditions of $I_{cc}=90\text{mA}$ and $V_c=5.0\text{V}$: solid line represent the measurement results; the line with symbols is the simulation result.

2.7 Stability Issues

In this section, a mm-wave InP DHBT based power amplifier with a detected instability at 15 GHz is used as a case study. With the aim to make the experimental-verified instability appear in the simulations, the analysis presented in this section reviews the available instability detection methods based on the classical two-port K - Δ pair, three-port analysis, system identifications, circuit modal analysis, and normalized determinant functions (NDF). In order to confirm the discussed stabilization techniques, new experimental results from a re-designed MMIC power amplifier with odd-mode stabilization resistors are presented.

A bottleneck today for emerging high speed wireless applications such as the E-band standard is the availability of high power amplifiers. To achieve the specified output power levels at this frequency range, integrated power amplifiers (PA's) require to combine multiple power cells on chip. However, this increases the risk of instability between the combined cells even if the relevant K -factor is well above one to guarantee unconditional stable operation for each individual cell.

Generally speaking, the even-mode circuit stability can be checked with two-port K - Δ pair. However, a necessary condition for unconditional stability is that the S -parameters have no RHPs (right hand poles) [34]. For the case of conditional stable amplifiers, further analysis with source and load stability circles are necessary. From a practical point of view, MMICs always have a third port for bias. In this manner, the circuit can be represented as a three-port network (RF input, RF output, and DC ports). At mm-wave frequencies, waveguide interface is widely used for system assembly. Due to the fact that the impedance is not well defined at frequencies below cut-off frequency of the RF waveguides, it is necessary to check the circuit stability between any RF and bias ports [30, 35]. For more complicated circuits where unstable modes are hidden by the circuit symmetry, there are several other techniques reported for the instability detection. Based on two-port K - Δ pair, it has been shown that the potential odd-mode instability can be detected by using push-pull simulation setups [29] which force odd-mode operations between combined cells by using ideal transformers at power combining points. Another method for stability analysis is system identification from the calculation of driving point impedance within feedback loops. The driving point impedance is derived from an auxiliary current or voltage source used to inject a small signal perturbation into circuits at

certain critical nodes [24, 36, 37]. Another technique included in this work is the circuit modal analysis [38]. This method splits a N-way combined power cell into two halves at its input or output: one part includes active devices, the other part includes passive power combining networks. With ports inserted at the circuit division point, an N-by-N impedance network can be formulated for each half of the circuit. Therefore, analysis of the circuit operation mode is transformed into an eigenvalue problem. Furthermore, based on the in-house developed multi-finger transistor model, the universal detection method based on NDF method [39–41] for a network with N-dependent sources is included as well.

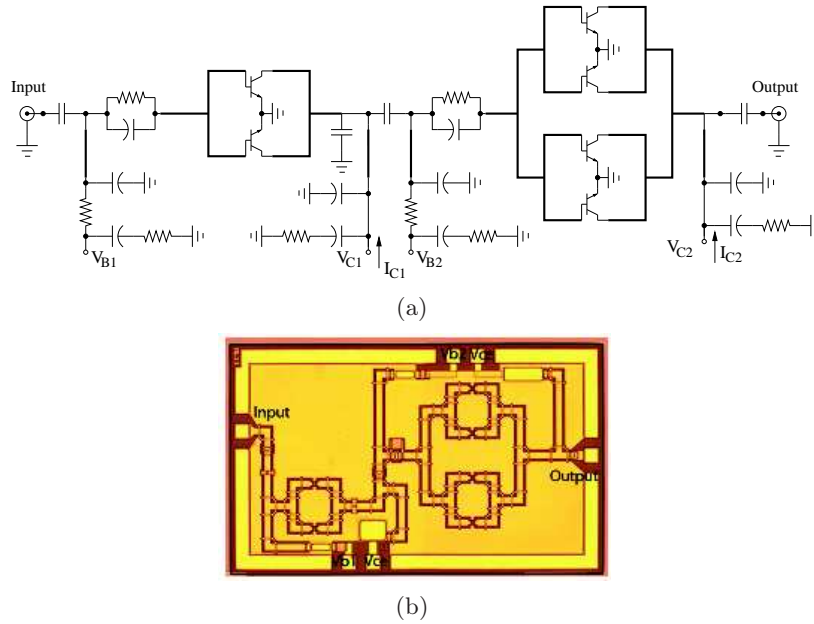


Figure 2.36: (a) Schematic and (b) microphotography of the fabricated two-stage common-emitter power amplifier with nominal DC biasing conditions: $I_{C1}=96$ mA, $I_{C2}=196$ mA, $V_C=2.5$ V.

2.7.1 Testing PA

The relevant circuit schematic and microphotography of the fabricated chip are shown in Fig.2.36. It has a two-way combined driver stage and a four-way combined power cell for the power stage. At nominal DC bias conditions: $I_{C1}=98$ mA, $I_{C2}=196$ mA, and $V_{C1}=V_{C2}=2.5$ V, the designed PA has an es-

timated linear gain of 9 dB and return loss better than 10 dB from 71 -76 GHz. The large signal simulation predicts 19.6 dBm output power at 1dB compression point with a power added efficiency of 9.8 %. Unfortunately, on-wafer measurements detect an off-band instability at 15 GHz with reduced DC operation conditions: $I_{c2}=6$ mA and $V_{c2}=1.2$ V as shown in Fig.2.37.

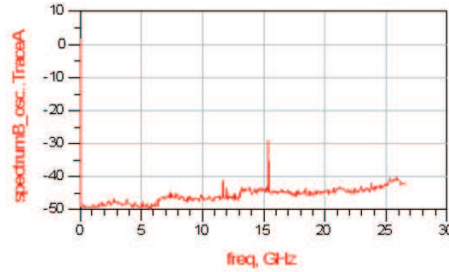


Figure 2.37: Captured spectrum showing the oscillation around 15 GHz.

To capture the frequency spectrum, the output pad is monitored through a GSG probe, which is attached to a coaxial cable with attenuators and fed into a HP8563E spectrum analyzer with a frequency range up to 26.5 GHz. Further investigations reveal that the detected instability arises from the four-way combined power stage. It remains whether the driver stage turns on or off and the input port is terminated or left open circuited. The power level of the detected signal is low due to the reduced bias conditions and the associated attenuations within the measurement setup.

A well-known problem in mm-wave power amplifier designs is that odd-mode oscillation can occur even if K-factor of the circuit is larger than one within the complete frequency range covered by an active device [41]. For the purpose of simplifying the analysis, only the four-way combined power stage is analyzed with the different instability detection methods. The simulated results are discussed and compared with measurements.

2.7.2 Classical two-port K-factor

K-factor is the most common and important criterion for evaluating the stability of a power amplifier from RF input to output. It is derived from

properties of two-port networks.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta_s|^2}{2|S_{21}S_{12}|} > 1 \quad (2.31)$$

where Δ_s is the determinant of the two-port S-parameter matrix. The circuit stability can be enhanced with augmented source and load terminations. However, this is different from the case of odd-mode instability, which is independent on the load and source impedance due to the virtual ground seen at power combining points [34, 38]. For PA design in this work, a capacitive loaded quarter wave transmission line with a series resistor is used for device base biasing as shown in Fig.2.38(a). The collector biasing adopts a similar circuit but without serial resistors to reduce DC losses. The associated two-port K-factor is checked by Eq.2.31 between RF ports. Fig.2.38(b) shows that the amplifier is unconditional stable at both DC biasing points. The observed instability does not arise between RF ports.

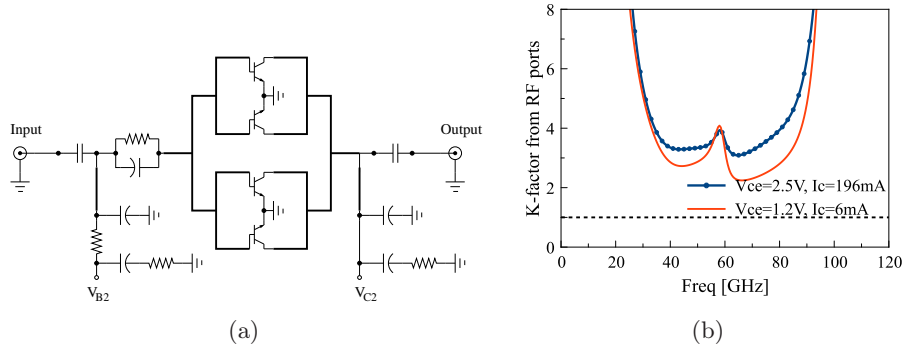


Figure 2.38: RF Two-port K-factor analysis at the nominal and reduced DC biasing conditions.

2.7.3 Two-port K-factor from biasing line

This method is usually used to detect a potential low frequency instability arising from biasing circuitries, but it also works well at higher frequencies. As shown in Fig.2.39(a), RF ports are terminated with 50Ω , while detection ports are inserted at the biasing circuitries: one is applied to the base biasing line of the devices, while the other one is applied to the collector. The calculated K-factors at low frequencies for both DC operation conditions are shown in Fig.2.39(b), and the results for higher frequencies are not displayed

due to the fact that the relevant values are well above one.

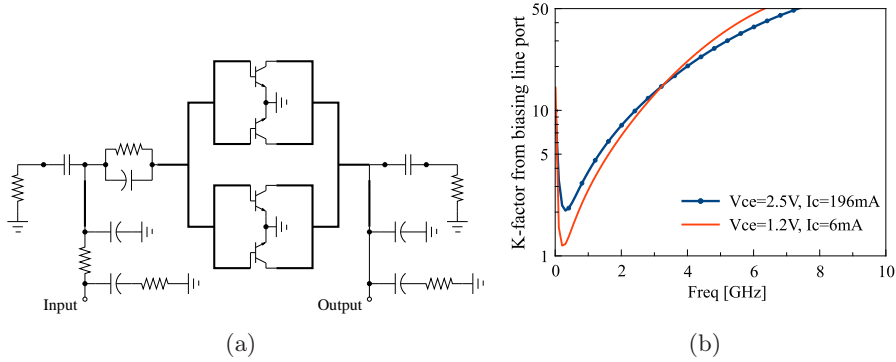


Figure 2.39: Stability analysis on biasing lines at the nominal and reduced DC biasing conditions. RF ports are terminated with 50Ω .

Several questions arise about why 50Ω are used for the RF port terminations, whether the unconditional stability between RF ports is affected by the impedances at the other port such as DC biasing line, and whether the unconditional stable operation is guaranteed between any RF port and biasing-line port at off-band frequencies. To answer the questions above, the complete stability test of three-port network would be desirable. Due to the fact that base bias circuitry includes a series resistor and a base-ballasting network, there is no instability arising from this branch. Therefore three-port S-parameters are calculated between RF input, RF output port and collector bias terminal. The stability condition for linear three-port analysis is based on the well-established two-port criterion in Eq.2.32.

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta_s S_{11}^*| + |S_{21} S_{12}|} > 1 \quad (2.32)$$

With the assumed Γ_k for the reflection at the third port k, the reduced network parameters are used to substitute into Eq.2.32. The generalized three-port unconditional stable condition is derived as Eq.2.33 [30]. The graphical analysis is implemented in ADS within the load-pull setup to solve the associated boundary condition:

$$\mu_3(\Gamma_k) = \frac{N(\Gamma_k)}{D(\Gamma_k)} = 1 \quad (2.33)$$

where

$$N(\Gamma_k) = |1 - S_{kk}\Gamma_k|^2 - |S_{ii} - \Delta_{jj}\Gamma_k|^2 \quad (2.34)$$

$$D(\Gamma_k) = |(S_{jj} - \Delta_{ii}\Gamma_k)(1 - S_{kk}^*\Gamma_k^*) - (\Delta_{kk} - \Delta_3\Gamma_k)(S_{ii}^* - \Delta_{jj}^*\Gamma_k^*)| + |J(\Gamma_k)| \quad (2.35)$$

$$J(\Gamma_k) = (S_{ij} + \Delta_{ji}\Gamma_k)(S_{ji} + \Delta_{ij}\Gamma_k) \quad (2.36)$$

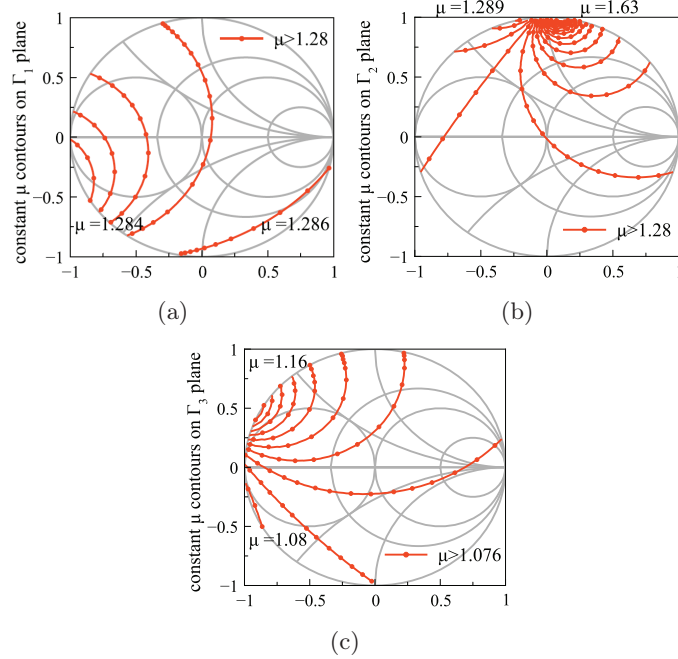


Figure 2.40: Constant contours of μ_k calculated from three-port S-parameter of the power stage with nominal DC bias operation conditions at 14 GHz: (a) viewed on the Γ_1 plane (b) viewed on the Γ_2 plane (c) viewed on the Γ_3 plane.

where i,j,k is $1,2,3;1,3,2\dots$, Δ_{ij} is the cofactor of the matrix element at (i,j) , and Δ_3 is the determinant of the three-port S-parameters. $\mu_3(\Gamma_k)$ is defined as the two-port stability criterion with a fixed load impedance at the third port. In this way, the unconditional stable condition between any two ports can be mapped on to the third impedance Γ_3 plane. To facilitate the design procedure, a graphical representation of related boundary conditions in Eq.2.33 is preferred to identify the associated impedance region for the case of conditional stable. For the power amplifier under investigation, the corresponding S-parameter at each frequency from 1 to 40 GHz have to be checked with all passive terminations at all three ports to assure the unconditional stable operation. Fig.2.40 shows the corresponding calculation results at 14 GHz with the nominal DC operation conditions. The constant

contours of $\mu_3(\Gamma_k)$ on each impedance plane are displayed with a minimum value of 1.28, 1.28, and 1.076, respectively. This means that the simulated three-port network is unconditional stable at a single frequency of 14 GHz.

To check the wideband instability with three-port analysis, minimum μ_k on each plane are calculated and shown from 1 to 40 GHz in Fig.2.41. It indicates that the observed instability does not arise due to the undefined impedances presented by waveguide interfaces and biasing lines.

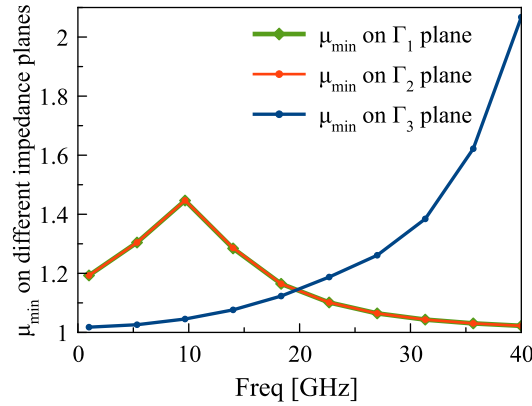


Figure 2.41: Minimum μ_k for the frequency range from 1 to 40 GHz at the nominal DC operation conditions.

2.7.4 Two-port K-factor from push-pull simulation

If an ideal transformer is applied at circuit power combining points as shown in Fig.2.42(a), the two-port K- Δ pair can be used to check circuit stability under odd-mode operation [29]. As indicated by the location of the ideal transformer, the odd-mode operation is considered between the two-way combined power cells. For the purpose of a clear and concise picture, the biasing network, which uses ideal RF Choke and AC coupling capacitor to separate the DC and RF path, is not shown. From the calculated K-factor, the amplifier is conditional stable below 30 GHz for both biasing conditions. Further analysis with stability circles for the frequency range from 13 to 16 GHz is shown in Fig.2.44. It indicates that source and load impedance (tightly space dots) are inside the stable area on Smith chart.

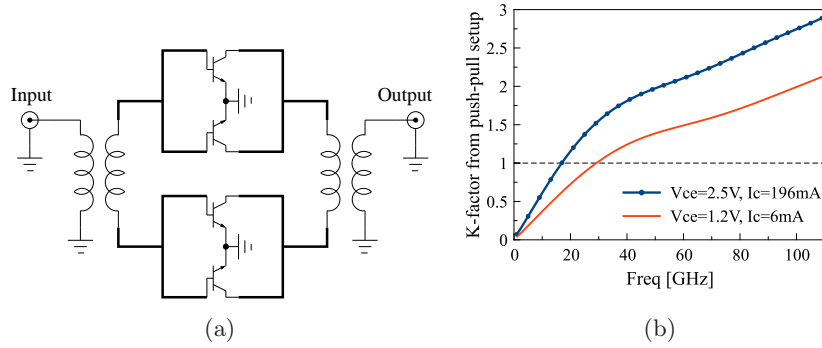


Figure 2.42: Push-pull analysis at the nominal and reduced DC biasing conditions.

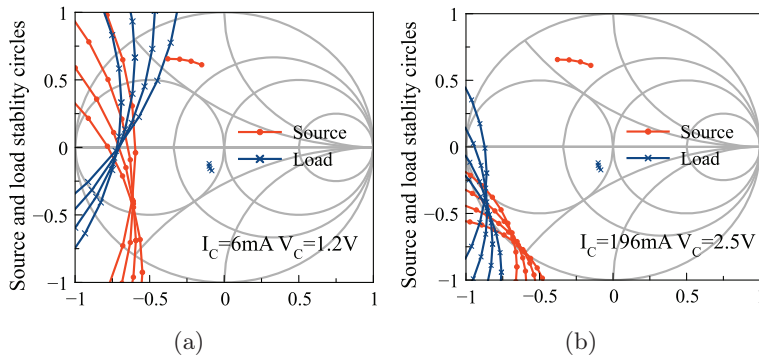


Figure 2.43: Source and load stability circles for frequency range from 13 to 16 GHz under the nominal (a) and reduced (b) DC biasing points.

2.7.5 Pole-zero identification

Driving point impedance Z_{dpi} can be used to catch the determinant information of a feedback system [42]. Its definition is derived from its generalized format of transimpedance within a N-port network as shown in Fig.2.44(a). The associated terminal current and voltage are related by Eq.2.37,

$$\mathbf{I}(s) = \mathbf{Y}(s)\mathbf{V}(s) \quad (2.37)$$

where $\mathbf{Y}(s)$ is the indefinite admittance of the subject network because the reference point to all network potentials is an arbitrary node extrinsic to the network. The transimpedance $Z_{rp,sq}$ shown in Fig.2.44(b) between the node

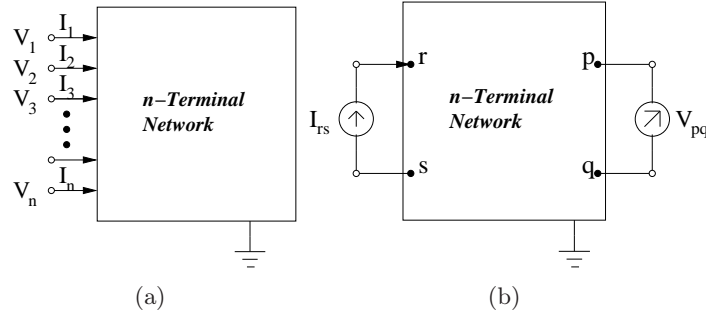


Figure 2.44: (a) general symbolic representation of N-port network (b) system abstraction for the measurement of transimpedance.

pair rs and pq is expressed in Eq.2.38,

$$Z_{rp,sq} = \frac{V_{pq}}{I_{rs}} = \frac{Y_{rp,sq}}{Y_{uv}} \quad (2.38)$$

where Y_{uv} is the first order cofactor of the element y_{uv} in the indefinite admittance matrix $\mathbf{Y}(s)$ and equals to

$$Y_{uv} = (-1)^{u+v} \det(\mathbf{Y}_{uv}) \quad (2.39)$$

\mathbf{Y}_{uv} is a submatrix obtained by deleting the u^{th} row and v^{th} column from $\mathbf{Y}(s)$. $Y_{rp,sq}$ is the second order cofactor of the element y_{rp} and y_{sq} in $\mathbf{Y}(s)$ and can be expressed as

$$Y_{rp,sq} = \mathbf{sgn}(r-s)\mathbf{sgn}(p-q)(-1)^{r+q+s+q} \det(\mathbf{Y}_{rp,sq}) \quad (2.40)$$

where $r \neq s$ and $p \neq q$, $\mathbf{Y}_{rp,sq}$ is obtained by striking out the r^{th} , s^{th} rows and p^{th} , q^{th} columns from $\mathbf{Y}(s)$, and the \mathbf{sgn} function is defined as

$$\left. \begin{aligned} \mathit{sgn}(u) &= +1 \text{ if } u > 0 \\ \mathit{sgn}(u) &= -1 \text{ if } u < 0 \\ \mathit{sgn}(u) &= 0 \text{ if } u = 0 \end{aligned} \right\} \quad (2.41)$$

When $r=p$ and $s=q$, $Z_{rp,sq}$ in Eq.2.38 simplifies to be the driving point impedance Z_{rs} . Due to the equicofactor properties of the matrix $\mathbf{Y}(s)$,

$$Y_{uv} = Y_{ij} \quad (2.42)$$

where u, v, i, j can be $1, 2, \dots, N$ and the fact that one of the N linear equations in Eq.2.37 is superfluous, then the system determinant can be correctly

captured by any one of the first order cofactor of the indefinite admittance matrix $\mathbf{Y}(s)$. If $u=v$ and is chosen to be the reference node for the subject system, then the pole information from the calculated transimpedance in Eq.2.38 or its special case: driving point impedance(with $r=p$ and $s=q$) can be used to check the circuit stability.

As shown in Fig.2.44(b), Z_{dpi} can be calculated by injecting a small current perturbation I_{sg} into a circuit at certain critical nodes and measuring its voltage responses V_{samp} . For practical circuits with multiple feedback loops, the signal injection point is chosen to be closed to devices such as A, B, C, and D in Fig.2.45 to include all possible instability modes [37]. The corresponding magnitude and phase responses of the calculated driving point impedance are then fitted by a synthesized transfer function with high order polynomials.

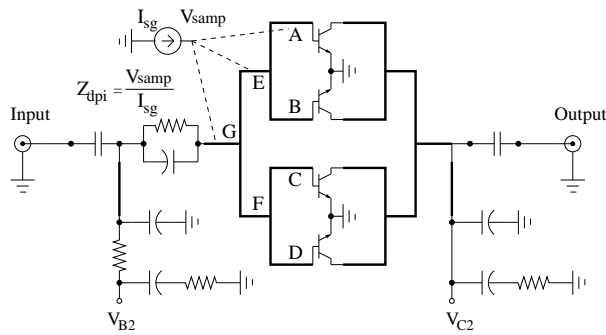


Figure 2.45: Calculation of the driving point impedance with an auxiliary small-signal current source: Z_{dpi} at different injection points has different pole information due to the circuit symmetry.

Fig.2.46 shows the simulated magnitude and phase responses from the driving point impedance calculation at the reduced DC bias point with the observed instability during measurements. The areas within the dashed lines at 15 GHz and 36 GHz are the frequency bands worth to investigate due to the high gain and zero phase transition. The targeting frequency band between 13-16 GHz is used as an example for the pole-zero identification purpose.

There are numerical difficulties to control system identification process to avoid over/under modeling of a system due to the unknown exact orders

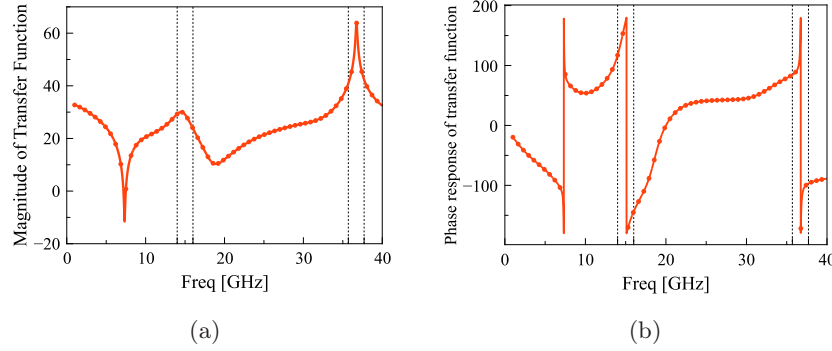


Figure 2.46: Magnitude(a) and phase(b) response of the simulated driving point impedance at A point in Fig.2.45 with the reduced DC biasing conditions: $I_{c2}=6$ mA $V_{c2}=1.2$ V.

of polynomials [24]. The criterion of fitting error for magnitude and phase comparisons might also change the order of estimated transfer function and as a result the total number of pole-zeros. In this work, the modeling errors in the synthesis procedure are minimized by the techniques of iterative band division and out-of-band pole zero filtering. The number of sub-bands can be iteratively decided until the order of the polynomials for each sub-band is below an user define value. The off-band pole-zeros are filtered out by the upper and lower boundary of that sub-band. The maximum order of polynomials and criterion of magnitude and phase fitting errors can be variables to find the repeated RHPs to improve the accuracy of the identification procedure.

As shown in Fig.2.47, the synthesized transfer function shows the same frequency responses as the original one. The frequency range from 13 to 16 GHz is divided into many sub-bands iteratively with a maximum polynomial order below 4 and fitting error well below $1e-3$. The predicted pole-zero map shows a RHP around 14.6 GHz as indicated. The similar analysis shows that the other instability might occur at 36.7 GHz.

To identify the corresponding oscillation loops for the detected instabilities, Z_{dpi} is recalculated at the other circuit nodes such as E and G [37]. Fig.2.48 summarizes the frequency response of Z_{dpi} at all three injection points. Compared with the phase responses of Z_{dpi} at A point, calculated Z_{dpi} at E does not catch the instability at 36.7 GHz. This means that the related instability mode(+ - + -) is inside the two-way combined power cell,

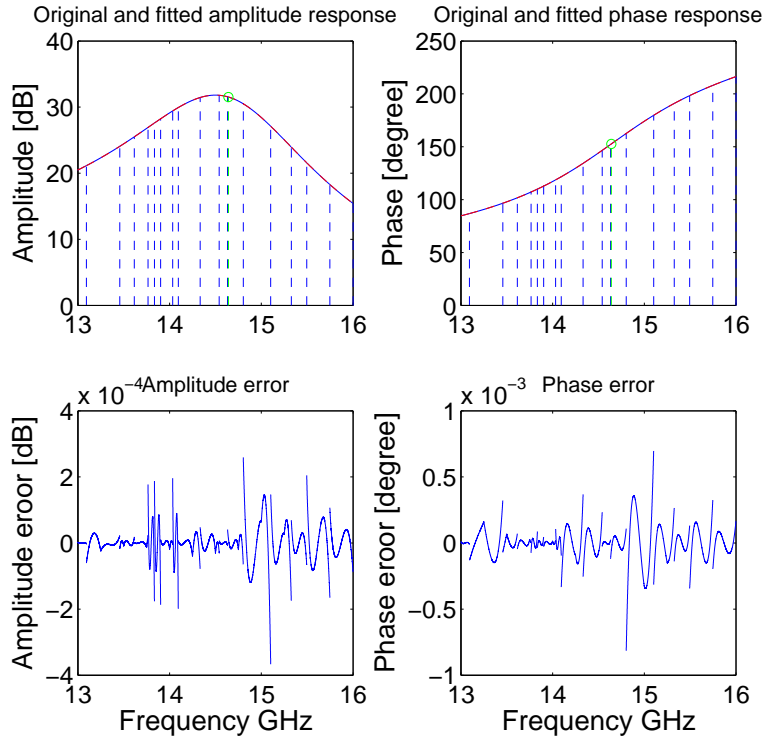


Figure 2.47: Magnitude and unwrapped phase responses from the simulation (red solid line) and synthesized (blue dash line) transfer functions. One RHP between 14.5 to 15 GHz can be identified directly.

and the corresponding injection port is not within the oscillation loop. The instability at 14.6 GHz is repeatedly found at E but not at G. This implies that the potential oscillation loop for this mode (+ + - -) is between the two-way combined power cells. Further movement of the injection point to G misses both instability frequencies due to the circuit symmetry.

To complete the analysis, there are two additional questions to answer: 1) where to insert stabilization resistors and 2) how to choose their values. From the identified potential oscillation loops, odd-mode stabilization resistors can be inserted either at collector or base of the devices. For both cases, the frequency responses of the driving point impedance at A are recorded in Fig. 2.49 by sweeping the value of stabilization resistors from 10 to 100 Ω . It shows that the high gain and sharp phase transition at the detected

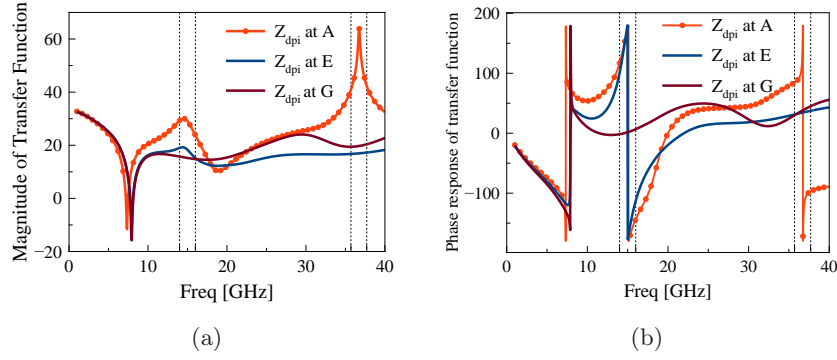


Figure 2.48: Magnitude(a) and phase(b) response of the calculated driving point impedance at A, E, and G point in Fig.2.45 with the reduced DC biasing conditions.

instability frequency 14.6 GHz become lower and much more smooth as long as the value of odd-mode stabilization resistors is chosen to be from 10 to 50 Ω . It seems that the inserted base stabilization resistors behave more efficiently in this case.

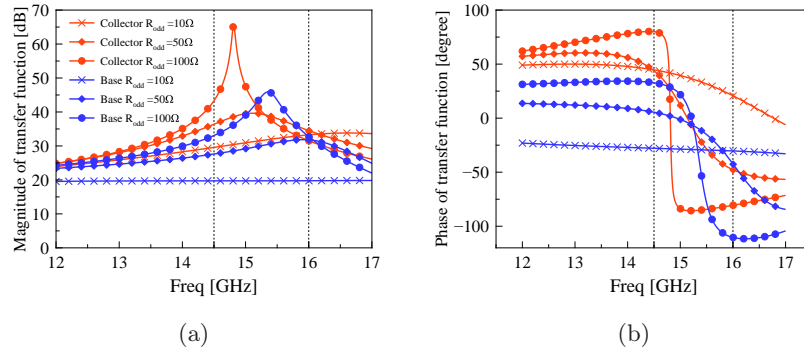


Figure 2.49: Magnitude(a) and phase(b) response of the calculated driving point impedance at A point in Fig.2.45 with the reduced DC biasing conditions. Odd-mode stabilization resistors with the values of 10 Ω , 50 Ω , and 100 Ω are inserted either at collector or base of the devices.

2.7.6 Circuit modal analysis

In this method [38], the circuit is divided into two parts at the collectors of four parallel devices as shown in Fig.2.50(a). For each half, a Z-matrix is used to represent the circuit properties and the simplified format due to the circuit symmetry is given in Eq.2.43. The terminal current and voltage relationship for each half circuit is shown in Eq.2.44.

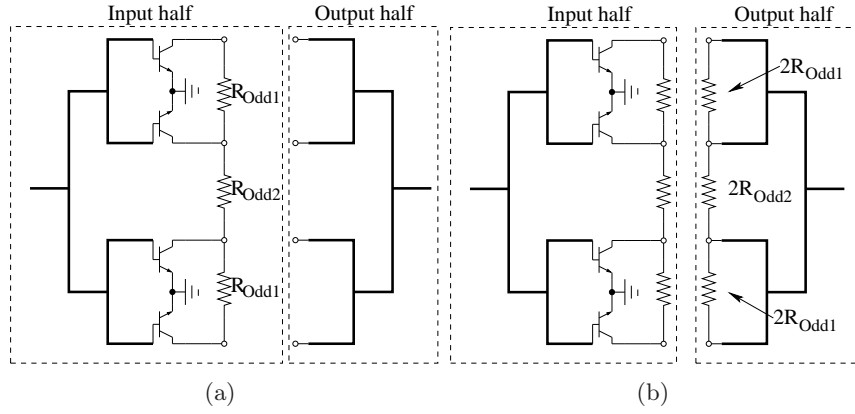


Figure 2.50: Configuration for standard modal analysis(left) and extended modal analysis.

$$Z_{input/output} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{12} & Z_{22} & Z_{23} & Z_{13} \\ Z_{13} & Z_{23} & Z_{22} & Z_{12} \\ Z_{14} & Z_{13} & Z_{12} & Z_{11} \end{bmatrix}, \quad (2.43)$$

$$[Z_{input/output}] [I_{half}] = [V] \leftrightarrow \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{12} & Z_{22} & Z_{23} & Z_{13} \\ Z_{13} & Z_{23} & Z_{22} & Z_{12} \\ Z_{14} & Z_{13} & Z_{12} & Z_{11} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix}, \quad (2.44)$$

where $[Z_{input/output}]$ represents the Z-matrix either from the input or output half circuit. Based on that, an eigenvalue equation can be formulated as Eq.2.45,

$$[Z_{input/output}] [I_{half}] = \lambda [I_{half}], \quad (2.45)$$

where λ is the eigenvalue and $[I_{half}]$ is the corresponding eigenvector, which represents linearly independent or orthogonal currents and can be generalized

Table 2.6: Eigenvalues for two most common eigenvectors $[I_{half}]$.

$[1 \ b_1 \ b_1 \ 1]$
$b_1 = ((-\beta_1/\alpha_1) \pm ((\beta_1/\alpha_1)^2 + 4)^{1/2})/2$
$\lambda_1 = Z_{11} + Z_{14} + (Z_{12} + Z_{13})b_1$
$\beta_1 = (Z_{11} + Z_{14} - Z_{22} - Z_{23})$ $\alpha_1 = (Z_{12} + Z_{13})$
$[1 \ b_2 \ -b_2 \ -1]$
$b_2 = ((-\beta_2/\alpha_2) \pm ((\beta_2/\alpha_2)^2 + 4)^{1/2})/2$
$\lambda_2 = Z_{11} - Z_{14} + (Z_{12} - Z_{13})b_2$
$\beta_2 = (Z_{11} - Z_{14} - Z_{22} + Z_{23})$ $\alpha_2 = (Z_{12} - Z_{13})$

to be

$$[I_{half1}] = \begin{bmatrix} 1 \\ b_1 \\ b_1 \\ 1 \end{bmatrix}, [I_{half2}] = \begin{bmatrix} 1 \\ b_2 \\ -b_2 \\ -1 \end{bmatrix} \quad (2.46)$$

And the corresponding solutions of the eigenvalue equation are listed in Table 2.6.

The special case: without stabilization resistors R_{odd1} and R_{odd2} can be analyzed by choosing them infinite large. Therefore, the solutions in Table I are simplified: $\beta=0$, $b_1=\pm 1$ and $b_2=\pm 1$ due to the circuit symmetry: $Z_{12}=Z_{22}$ and $Z_{23}=Z_{14}$. The simplified solutions correspond to the four modes discussed in [38]: one even-mode with $b_1=1$ and the other three odd-mode operations $b_1=-1$ and $b_2=\pm 1$. The effect for $b_1=-1$ is same as $b_2=-1$, which indicates a potential oscillation loop between the devices inside each two-way combined power cell.

For an ordinary case with finite values of R_{odd1} and R_{odd2} , eigenvalues from both halves of the circuit can not be summed directly for some eigenvectors such as $[1 \ b_2 \ -b_2 \ -1]$. This can be explained by the different eigenvectors $[I_{half}]$ used at the circuit division point for each half circuit [38]. For practical purposes, we propose to extend the circuit modal analysis by replacing R_{odd} with two parallel resistors $2R_{odd}$ in both parts of the circuit as shown in Fig.2.50(b). The un-symmetry at each half is kept identical and eigenvalues for all the modes can be summed together.

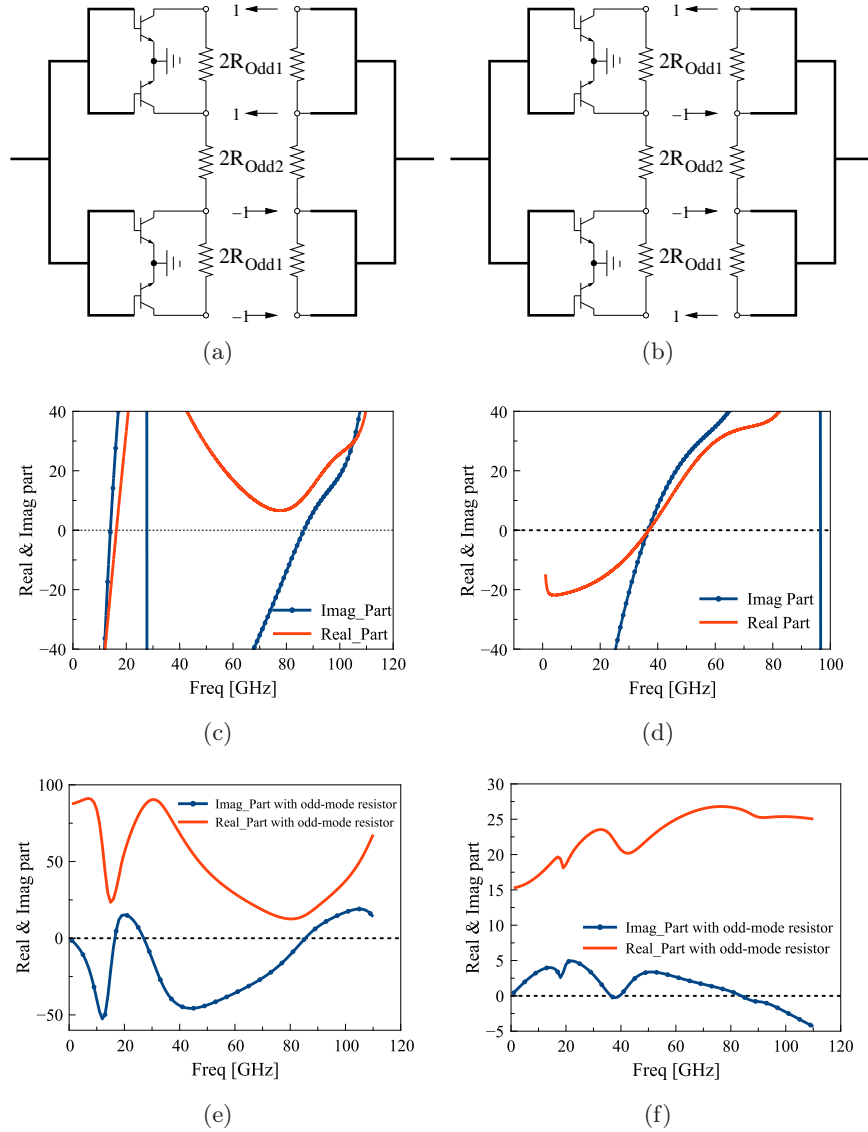


Figure 2.51: Eigenvalue sums for modes of $[1 \ 1 \ -1 \ -1]$ and $[1 \ -1 \ -1 \ 1]$ under the reduced DC biasing conditions of $I_{c2}=6 \text{ mA}$ and $V_{c2}=1.2 \text{ V}$: (a,b,c) shows the circuit schematic with the assumed eigenvector mode of $[1 \ 1 \ -1 \ -1]$, its corresponding eigenvalue sum with infinite large R_{odd1} and R_{odd2} , and updated eigenvalue sum with finite value of $2R_{odd1}$ and $2R_{odd2}=20 \ \Omega$, respectively; (d,e,f) shows the circuit schematic with the assumed eigenvector of $[1 \ -1 \ -1 \ 1]$, its corresponding eigenvalue sum with infinite large R_{odd1} and R_{odd2} , and the updated eigenvalue sum with finite value of $2R_{odd1}$ and $2R_{odd2}=20 \ \Omega$, respectively.

Based on the extended circuit modal analysis, two eigenvector modes are analyzed. Fig.2.51(a) shows the schematic of the circuit with the considered current eigenvector of $[1 \ 1 \ -1 \ -1]$. The corresponding eigenvalue sum for this mode with infinite large R_{odd1} and R_{odd2} is shown in Fig.2.51(b). As indicated, a potential instability arising from the four-way combined power stage occurs at 14.0 GHz. According to the considered eigenvector mode of $[1 \ 1 \ -1 \ -1]$, the oscillation loop can be easily identified, which is between the two-way combined power cells. To suppress this mode, a stabilization resistor R_{odd2} of $10 \ \Omega$ is inserted within the oscillation loop. The updated eigenvalue sum with the stabilization resistors is shown in Fig.2.51(c) to confirm the choice of the location and value of odd-mode stabilization resistors.

A similar analysis is used to check the eigenvector of $[1 \ -1 \ -1 \ 1]$ as shown in Fig.2.51(d). The calculation results from Fig.2.51(e) indicate the other potential instability at 36.7 GHz. For this mode, the associated oscillation loop is between the two devices inside of the two-way combined power cells. With the help of stabilization resistors R_{odd1} of $10 \ \Omega$, the circuit stability is improved as shown in Fig.2.51(f).

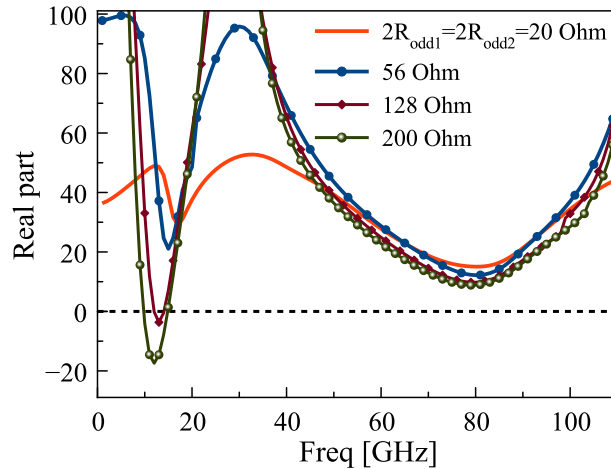


Figure 2.52: Real part of eigenvalue sums for the mode of $[1 \ 1 \ -1 \ -1]$ with different values of $2R_{odd1}$ and $2R_{odd2}$ at the reduced DC bias conditions.

Furthermore, the proper choice of stabilization resistors deserves some comment as well. To give an example of this, the oscillation mode of $[1 \ 1 \ -1 \ -1]$, which has a potential instability at 14 GHz, is further investigated.

The eigenvalue sums are calculated by sweeping the values of stabilization resistors. The comparison in Fig.2.52 indicates that the small value of odd-mode stabilization resistors in the range of 10-50 Ω is preferred for this design.

2.7.7 Return difference and normalized determinant function(NDF)

The concept of return difference(RD) of a feedback amplifier with respect to a dependent source with a parameter of x shown in Fig.2.53(a) is defined as the ratio of two functional values assumed by the first order cofactor of an element of its indefinite admittance matrix, under the condition that parameter x assumes its nominal value and the condition that parameter x assumes a null value [42].

$$RD(x) = \frac{Y_{uv}(x)}{Y_{uv}(0)} \tag{2.47}$$

where $Y_{uv}(x)$ is the first order cofactor(Eq.2.39) of the subject network as a function of parameter x and

$$Y_{uv}(0) = Y_{uv}(x)|_{x=0} \tag{2.48}$$

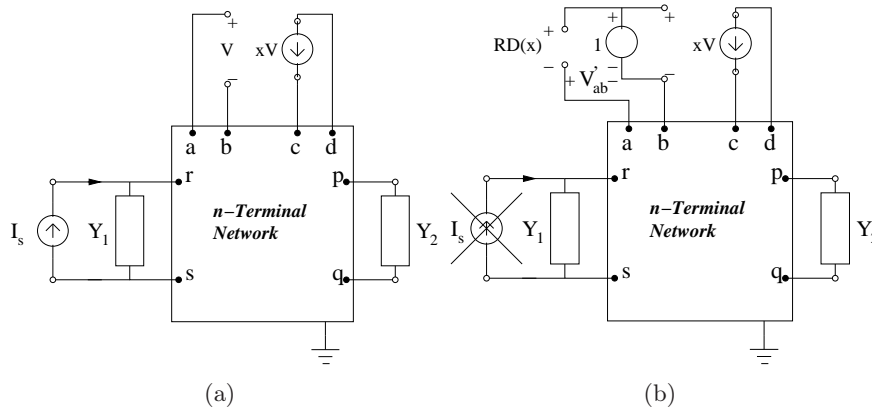


Figure 2.53: (a) A generalized feedback network with a dependent current source with a parameter of x (b) physical significance of return difference $RD(x)$.

If the controlled current source in Fig.2.53(b) is replaced with an independent current source of x amperes and the excitation source I_s is set to be

zero, then the voltage established between the node a and b is expressed as

$$V'_{ab} = x \frac{Y_{da,cb}(0)}{Y_{uv}(0)} = -x \frac{Y_{ca,db}(0)}{Y_{uv}(0)} \quad (2.49)$$

where the transimpedance(Eq.2.38) from the node pair dc to ab is invoked. The concept of return ratio(RR) is introduced to be the negative voltage of V'_{ab} or $RR=-V'_{ab}$. In view of this observation, the physical significance of the return difference RD(x) in Fig.2.53(b) can be explained as the voltage difference between the 1-volt excitation and the return voltage V'_{ab} :

$$\begin{aligned} RD &= \frac{Y_{uv}(x)}{Y_{uv}(0)} = 1 + RR = 1 - V'_{ab} = 1 + x \frac{Y_{ca,db}(0)}{Y_{uv}(0)} \\ &= \frac{Y_{uv}(0) + xY_{ca,db}(0)}{Y_{uv}(0)} = \frac{Y_{db}(x)}{Y_{uv}(0)} = \frac{Y_{uv}(x)}{Y_{uv}(0)} \end{aligned} \quad (2.50)$$

where the equicofactor properties(Eq.2.42) of the indefinite admittance matrix $\mathbf{Y}(s)$ and linear superposition principle: $Y_{db}(x)=Y_{db}(0)+xY_{ca,db}$ are invoked.

It is worth to mention that return difference $RD=1+RR$ shares the same general format as the feedback factor $1-\mu\beta$, where μ is the transfer function of a unilateral forward active path and β represents the transfer function of a unilateral feedback path. The negative of return ratio RR is close to the format of loop gain $\mu\beta$ [43], but there is significant discrepancy between them [44].

To illustrate the calculation procedure of RD, a circuit with common-emitter configuration is considered in Fig.2.54(a). Three-port network parameters are necessary to calculate the relevant determinants. However, to facilitate hand analysis, the effect of series feedback is ignored firstly by setting $R_e=0$ and the dimension of the circuit matrix reduces to 2 by 2. Then the two-port Y-parameter of the simplified network is

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} \frac{1}{r_\pi} + \frac{1}{R_F} & -\frac{1}{R_F} \\ G_m - \frac{1}{R_F} & \frac{1}{R_C} + \frac{1}{R_F} + \frac{1}{r_o} \end{bmatrix} \quad (2.51)$$

The corresponding return ratio for this case is

$$RD = \frac{Y_{11}Y_{22} - Y_{12}Y_{21}}{Y'_{11}Y'_{22} - Y'_{12}Y'_{21}} = \frac{(\frac{1}{r_\pi} + \frac{1}{R_F})(\frac{1}{R_C} + \frac{1}{R_F} + \frac{1}{r_o}) - (G_m - \frac{1}{R_F})(-\frac{1}{R_F})}{(\frac{1}{r_\pi} + \frac{1}{R_F})(\frac{1}{R_C} + \frac{1}{R_F} + \frac{1}{r_o}) - (0 - \frac{1}{R_F})(-\frac{1}{R_F})}$$

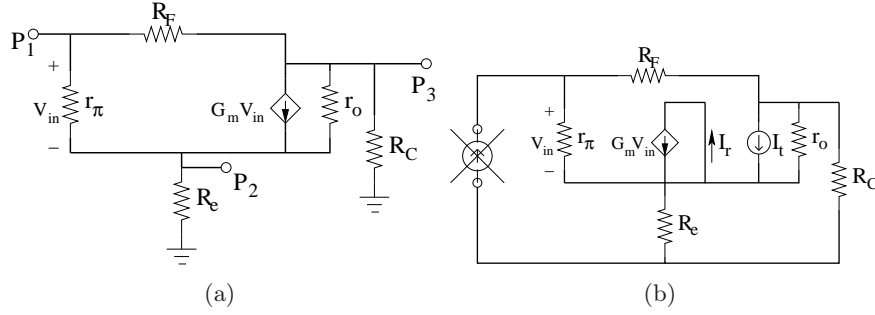


Figure 2.54: RD analysis of a circuit with common-emitter configuration: (a) the schematic for determinant calculation of the subject network (b) RD calculation by disconnecting the dependent source and injecting the small-signal tone.

$$= \frac{R_F^2 + R_F(r_\pi + R_{to}) + G_m R_F(r_\pi R_{to})}{R_F^2 + R_F(r_\pi + R_{to})} = 1 + \frac{G_m(r_\pi R_{to})}{R_F + r_\pi + R_{to}} \quad (2.52)$$

where Y'_{xx} represents the two-port network with $G_m=0$ and $R_{to}=R_C||r_o$. It can be imagined that the analytical expression of network determinants will be difficult when the practical network is more complicated.

To avoid direct calculation of network determinant, the physical interpretation of RD in Fig.2.53(b) tells that the return ratio can be measured by inserting a small-signal current into the circuit. The step for calculating the return ratio for this case are as follows: 1) set all independent sources zero 2) disconnect the connection of dependent source to the circuit 3) insert a small-signal tone I_t with the same polarity as shown in Fig.2.54(b) 4) the negative ratio of the short circuited current I_r to the injection signal I_t is the return ratio for this dependent source [44]. The low frequency return ratio for the circuit in Fig.2.54(b) is expressed as

$$RD = 1 + RR = 1 - \frac{I_r}{I_t} = 1 + G_m r_\pi \frac{r_o || (R_C + R_e)}{r_o || (R_C + R_e) + (R_F + r_\pi)} \quad (2.53)$$

It has the same results as in Eq.2.52. From the practical point of view, this method is preferred for complicated circuits where network determinants are difficult to calculate directly.

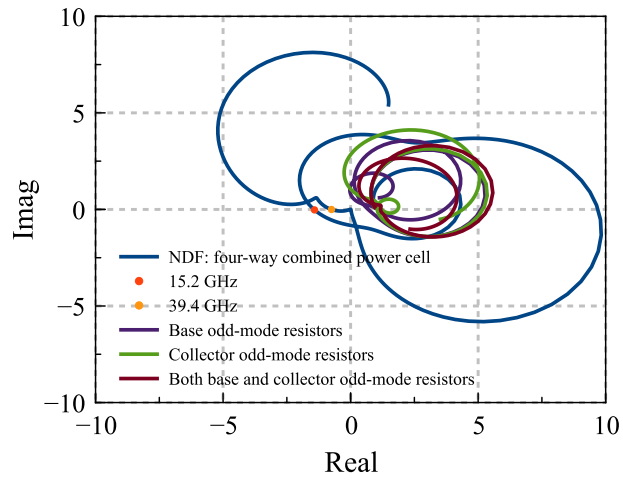
The return difference concept was further extended for the case of feedback networks with multiple dependent sources [39]. The normalized determinant function (NDF) is defined as a ratio of determinant Δ from the full

network and determinant Δ_0 from the resulting passive network where all N dependent sources are set to zero. To reduce the complexity of matrix calculation, NDF of a network with N dependent sources can be iteratively calculated as

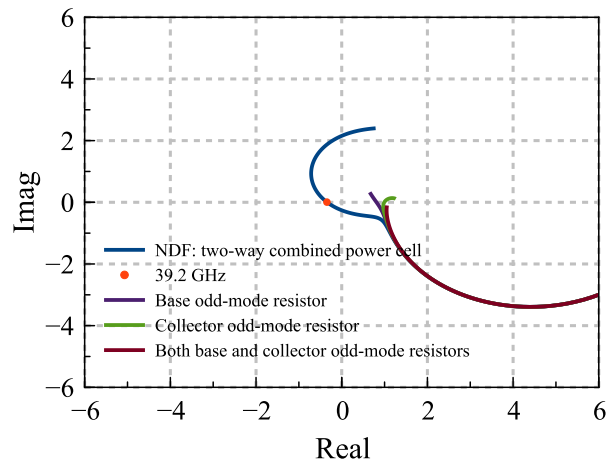
$$NDF = \frac{\Delta}{\Delta_0} = \frac{\Delta}{\Delta_1} \times \frac{\Delta_1}{\Delta_2} \times \frac{\Delta_2}{\Delta_3} \dots \times \frac{\Delta_{N-1}}{\Delta_0} = \prod_{i=1}^N (RR_i + 1) \quad (2.54)$$

where Δ_i represents the network determinant with first i dependent sources set to zero, and RR_i is the return ratio for this dependent source. Based on the stability analysis by applying Nyquist criterion, the system is unstable if the locus of RD has right-hand zeros. And the number of right-hand zeros is equal to the number of times the locus encircles the origin in the clockwise direction on complex plane. For the case of four-way combined PA, calculation of RR_i is separately done by turning off first $i-1$ dependent sources.

To calculate the individual return ratio RR_i for the PA under investigation, a detailed small-signal device model of InP DHBT device is employed. The calculated NDF from 1 to 50 GHz for the four-way combined power cell at reduced bias conditions is shown on complex plane in Fig.2.55(a). As indicated by the two dots, the locus of RD encircles the origin twice at the frequency of 15.2 GHz and 39.4 GHz, respectively. The slightly difference of the predicted instability frequencies compared with previous analysis is due to the accuracy of the extracted device parameters. To confirm the location for inserting odd-mode stabilization resistors and their values, the corresponding calculated NDF for the circuit are compared in Fig.2.55(a). With inserted odd-mode stabilization resistors, the improvement of circuit stability is obvious, and the updated NDF locus have no origin encirclements any more. The instability loop around 37 GHz can be identified by repeating the calculation procedure within the two-way combined cells. Fig.2.55(b) shows that the instability at 39.2 GHz is repeatedly found. This result confirms that the second instability mode arise within the two-way combined power cell. And the updated NDF locus with stabilization resistors a either base or collector and both terminals are included for comparison as well.



(a)



(b)

Figure 2.55: NDF locus of the (a) four-way (b) two-way combined power cells for the frequency range from 1 to 50 GHz. The blue curve is the original NDF locus without stabilization resistors. The other color solid line represents the case with stabilization resistors at only base, collector and both terminals respectively.

Further extension of NDF to large signal regime is described in [40] by using an ideal filter network to filter out the sideband signals to keep the open loop operation for $\omega_k + \Omega$ and pass the fundamental and higher harmonics of a large pumping signal, where ω_k represents the frequency of the pumping signal and K is between $-N$ and $+N$ the number of harmonics considered, while Ω is the swept frequency of the external perturbation signal. The return ratio RR_i for each individual dependent source can be calculated in the same way as before by setting $(i-1)$ dependent sources to zero for perturbation signal but not for steady state large signal.

2.7.8 Measurements

To verify the previous discussions on the circuit stability techniques, a re-designed power amplifier chip with odd-mode stabilization resistors of $15\ \Omega$ for both R_{odd1} and R_{odd2} is fabricated and tested with an on-wafer measurement setup. The output pad of the chip is monitored with the spectrum analyzer HP8563E through a wafer probe. The captured spectrums are shown in Fig.2.56.

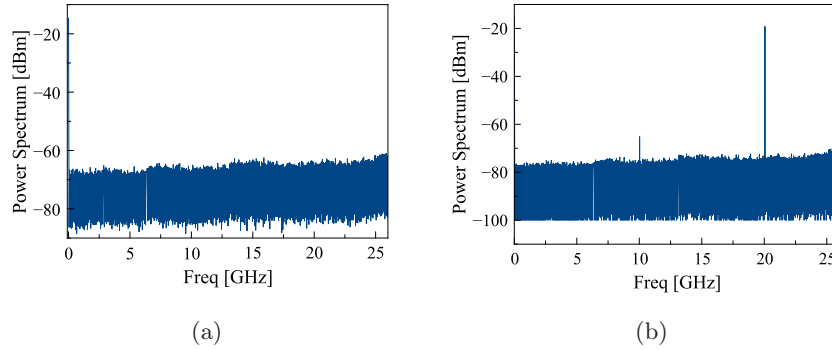


Figure 2.56: Captured frequency spectrum from the re-designed PA with odd-mode stabilization resistors of $15\ \Omega$ for both R_{odd1} and R_{odd2} : (a) power spectrum without incoming RF signal (b) power spectrum with an injected tone from the network analyzer into the PA.

The DC operation point of the PA is swept up to $I_{c1}=78\ \text{mA}$, $I_{c2}=130\ \text{mA}$, and $V_{ce}=2.5\ \text{V}$. The amplifier is biased close to the nominal conditions. Further increasing the collector current leads to the thermal breakdown. No instability is observed during the measurements. Fig.2.56(a) shows the captured powers spectrum from the re-designed PA chip. To check the amplifier

stability around 36 GHz, a signal at 20 GHz is injected from the network analyzer into the input pad of the PA. The captured output power spectrum in Fig.2.56(b) is clean and does not show any mixing products.

2.7.9 Discussion

Different instability detection methods are reviewed and employed in this work to analyze the measured instability from a two-stage common emitter PA design. The classical two-port K - Δ pair is fast and effective way to check the even-mode operation of the circuit. Further investigation with source and load stability circle is necessary for the conditional stable circuits. The generalized three-port stability analysis is derived from two-port stability criterion by terminating the third port. The simplified graphical analysis is a valuable and fast way to detect the instability due to undefined impedances below the cutoff frequencies of RF waveguides. However, both of them are insufficient to guarantee unconditional stable operations if there are hidden oscillation modes due to the circuit symmetry. The push-pull setup indicates that the circuit is conditional stable for some frequency range, but further analysis from input and output stability circles does not confirm the measured instability for this case.

System identification methods based on synthesis of closed loop transfer functions does capture the potential instability frequencies, while special attentions have to be paid to avoid under or over-modeling of a system function. The advantage of this method is that it does not require the detailed transistor model and it can be further extended for the detection of parametric oscillations due to different input power levels. The circuit modal analysis is extended in this work to allow the choice of stabilization resistor values. For PA designs at mm-wave frequency, parallel symmetric power cells are generally adopted to deliver higher output power. In this situation, the advantages of the circuit modal analysis is that it can detect potential instabilities, identify the corresponding oscillation loops, and improve circuit stability at the very beginning of the design procedure without knowledge of the details from device modeling. However, it is only useful under small-signal circumstances. NDF is the most universal and rigorous method for the stability analysis: N-dependent sources, multiple feedback loops, any circuit topologies. However, designers have to access into the detailed device models for both small and large signal analysis. Table 2.7 summarizes all reviewed methods, and the comparison is given in term of implementation,

application circumstances, pre-knowledge of device models, and the ability of odd-mode instability detection.

Method	Circuit simulator	Small or large-signal	device	odd-mode
K-factor	yes	small	no	no
Push-pull	yes	small	no	no
Linear three-port	yes	both	no	no
Pole-zero	no	both	no	yes
Modal analysis	yes	small	no	yes
NDF	yes	both	yes	yes

Table 2.7: Comparison of all instability detection methods in term of implementation, application circumstances, pre-knowledge of device models, and the ability of odd-mode instability detection.

2.8 Summary

In this chapter, mm-wave power amplifiers using InP DHBT technology for E-band application are investigated. To improve the overall output power, several PA designs are implemented. The circuit stability at millimeter-wave frequencies are extensively investigated as well.

The problems of early power saturation from a previously designed PA are identified. Based on the comparison of standard circuit topologies, the interstage matched cascode configuration is employed in this work to improve the overall saturated output power. The measured single-finger PA design shows an output power of 9.0 dBm at 1dB compression point, peak efficiency 9.1 % and saturated output power of 12.3 dBm with associated linear gain of 9.2 dB at 67.2 GHz. The observed frequency down shift is due to the capacitive loading from the airbridges, which can be characterized accurately by reducing the dielectric thickness from 2 μm to 1 μm . With the corrected layer stack, the measured small-signal S-parameters agree very well with the EM-circuit co-simulation up to 95 GHz.

Advanced power combining network with matching properties is proposed to improve the overall large-signal matching bandwidth. The open and short-circuit stubs are used to modify the phase responses of the power combining structure. The analytical expressions on the different impedance transformation ratio are derived. Based on the proposed power combining

structure, the simulated linear power gain is about 9.4 dB for a two-way power combined PA with 15 GHz 3 dB bandwidth. At the 1dB power compression, the simulated PA shows 14.1 dBm output power with associated PAE of 11.1 % at 73.5 GHz. Unfortunately, the base-emitter junction of the fabricated single-finger transistor does not work properly. Therefore, the measurements are not presented in this work.

The most promising result is from a two-way combined three-finger design. The measured PA demonstrates 17.0 dBm output power at 1dB compression point, peak efficiency 12 % and 18.6 dBm saturated output power with associated linear power gain of 9.5 dB at 72 GHz. The inserted odd-mode stability resistors suppress odd-mode oscillations. Potential nonlinear stability due to the different input power levels is not detected during measurements.

The topic of circuit stability is investigated in an independent section. All available instability detection methods are reviewed and implemented to check even and odd-mode instability on a measured power amplifier. Among them, the classical two-port, biasing line, linear three-port, and push-pull analysis are based on the traditional K-factor. However, they are not sufficient to predict the measured odd-mode oscillation hidden due to the circuit symmetry. The other methods such as pole-zero identification, circuit modal analysis, and NDF are compared as well and successfully explain the observed instability at 15 GHz during the measurements.

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Chapter 3

Submillimeter-wave SHM and Tripler Designs

3.1 Introduction

As mentioned before, THz heterodyne receivers have many applications in the fields of astronomy, atmospheric sounding, non-destructive testing, biomedicine, and security imaging. The system diagram of the targeting THz heterodyne receiver based on Schottky diode technology is shown in Fig.1.2. One of the most important receiver components is the SHM. It is used to down-convert the signal that carries information to baseband by using a local oscillator(LO) signal which is only half of the RF signal frequency. A typical SHM circuit topology based on the antiparallel diode configuration is shown in Fig.3.1. The commercial diode chip is flip-chip mounted on a thick quartz substrate, which is then embedded into a metallic housing. The difference between Fig.3.1(a) and Fig.3.1(b) is that the latter one employs the balanced configuration to achieve image rejection and improve the reflection at LO and RF ports.

Sub-harmonically pumped mixers have a number of practical advantages over its fundamental mixer counterparts. For the submillimeter-wave applications where the LO power source is scarce, the main advantage of SHMs is that the local oscillator signal is much easier to generate with solid-state components due to the reduced frequency. Secondly, an IF output impedance close to 100Ω is much easier for applications requiring a wide IF bandwidth [1]. The third reason is that due to the intrinsic circuit symmetry, even order harmonics are terminated automatically and the corresponding

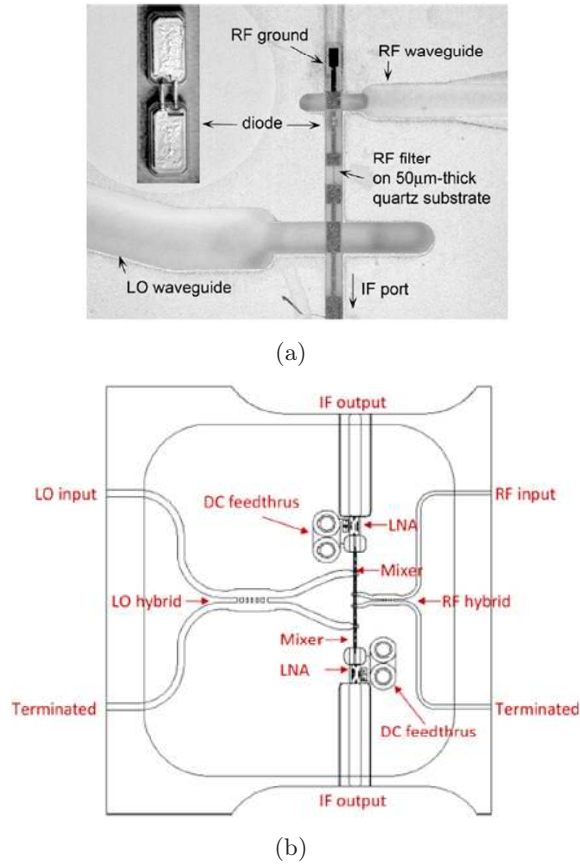
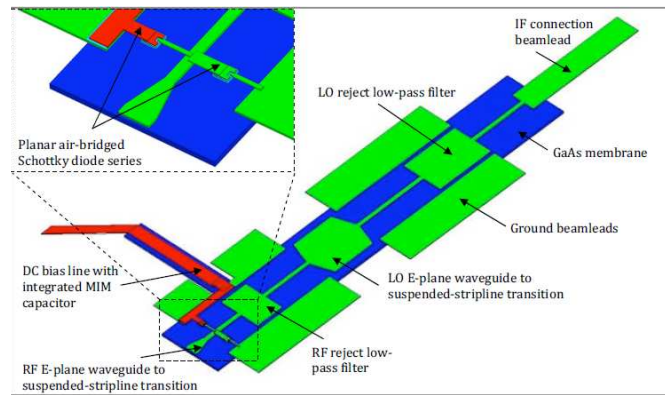


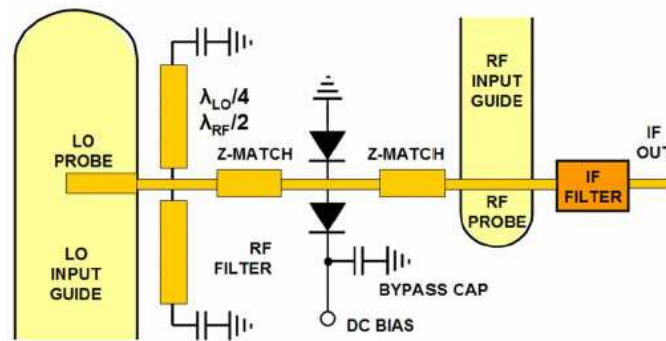
Figure 3.1: SHM circuits based on the anti-parallel configuration: (a) low noise SHM at 300 to 360 GHz [2] (b) balanced SHM design with waveguide branch-line couplers at 340 GHz [3].

matching circuits for LO and RF ports are simplified.

One drawback of this type SHMs is that the antiparallel diode pair has to be substantially pumped to saturate the mixer performance unless the DC bias is provided for each device. For a balanced design for image rejection in Fig.3.1(b), an extra 3 dB is required for the LO power. An alternative solution is the crossbar configuration as shown in Fig.3.2. The crossbar configuration was first used for fundamental mixer applications to improve the LO-RF isolation due to the mode orthogonality [6–11]. For this case, one side of the series diode pair has a direct DC contact with the side wall of



(a)



(b)

Figure 3.2: SHM circuits based on the crossbar diode configurations: (a) crossbar SHM design at 810 to 910 GHz [4] (b) crossbar SHM design at 520 to 590 GHz [5].

metallic housing. With the use of a single bypass capacitor, DC bias is possible. Based on this topology, the requirement on LO source power levels is lower and noise performance of the SHM can be improved [12, 13].

Many designs of submillimeter-wave SHMs have been proposed during the last decade from Jet Propulsion Laboratory(JPL), Rutherford Appleton Laboratory(RAL), and LERMA Observatoire de Paris for the applications mentioned above. Most circuits use essentially planar discrete diodes from US based company such as Virginia diode, Inc (VDI) and European research institutions like RAL or UMS(United Monolithic Semiconductors). Among those designs, the antiparallel diode pair is transferred to a thick and low dielectric quartz substrate with $\sim 50 \mu\text{m}$ to reduce parasitics capacitance from pad to pad [1, 2, 14–18]. However, the disadvantages of this approach include the thick substrate needed to survive the bonding process, power loss due to the parasitic surface mode propagation, lower limit of footprint area, inevitable bump-bond parasitics, and the alignment tolerance during the mounting procedure [19, 20].

Recently, an ultra-thin GaAs membrane with $3\sim 5 \mu\text{m}$ thickness [1, 21] was adopted to overcome the previous drawbacks. Fig.3.3 shows the top and cross section view of the E-plane split blocks with membrane circuits embedded. As shown, the GaAs membrane where the schottky diode and passive circuits are fabricated on is supported by beamleads. The beamleads provide the electrical connection and mechanical support for membrane circuits [19]. Fundamental mixers and SHMs based on monolithic integrated Schottky diodes [4, 5, 12, 13, 20, 22] demonstrate better results than the previous designs with discrete diodes. Multiplier designs based on the same membrane technology can be found from the open literatures [23–27] as well.

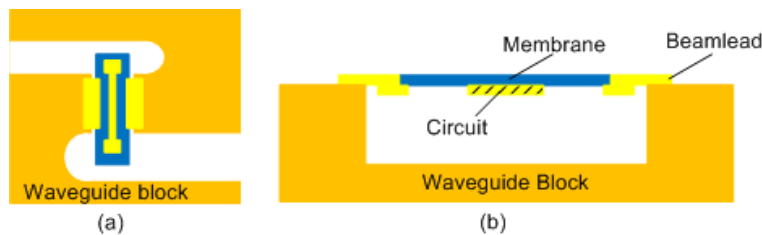


Figure 3.3: Schematic pictures of the membrane circuits (a) top view (b) cross section.

This chapter focus on the SHM design methodology for a 557 GHz heterodyne receiver. As shown in Fig.3.4, SHM circuit is divided into several key elements such as E-probes and matching networks. The corresponding components are discussed in details. Section 3.2 shows the specifications of SHM and the diode parameters used for the design. The theoretical investigation based on conversion matrix analysis is presented for an estimation of conversion loss. Section 3.4 focuses on the choice of circuit topology, discusses EM propagation mode inside of the metallic housing, and analyzes the attenuation of an uniform transmission line. Section 3.5 investigates the influence of the parasitics from the crossbar structure on the embedding impedance of the SHM. Section 3.6, 3.7, 3.8, and 3.9 focus on the design techniques of the E-probes, matching circuits, rejection filters and the IF output circuit. The characteristics of the designed SHMs are summarized in Section 3.10 and 3.11. Finally, a summary are given at the end of this chapter.

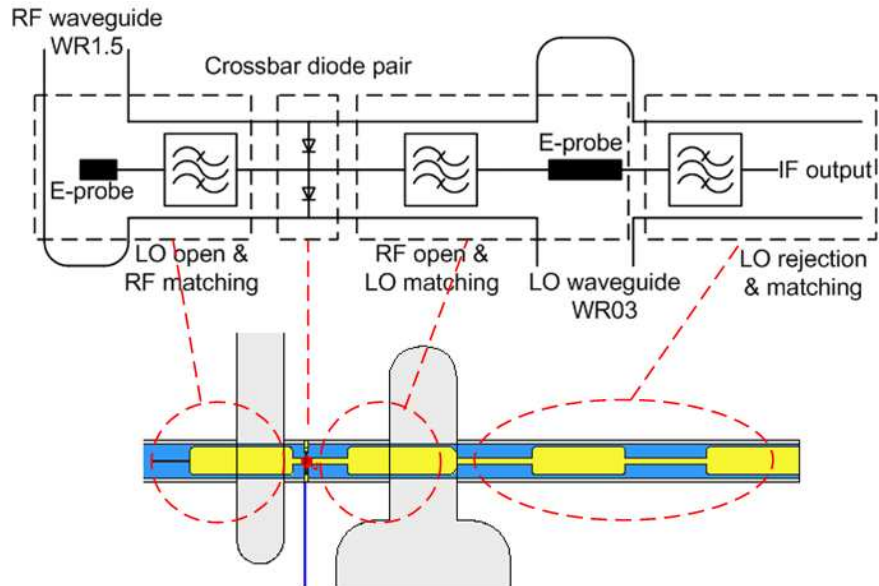


Figure 3.4: Generalized SHM schematic at 557GHz.

For measurement purposes, a tripler is designed for the generation of a RF signal at 557 GHz. The generalized schematic diagram of the tripler is shown in Fig.3.5. The circuit consists of E-probe transitions and filtering

networks at both input and output ports. As indicated, the designed tripler is the last stage of signal generation chain consisting of an x6 active multiplier from RPG able to deliver +6 dBm output power from 65 to 110 GHz, attenuator, the previously designed InP DHBT power amplifier, RF&thermal isolator, and a tripler working from 180 to 210 GHz.

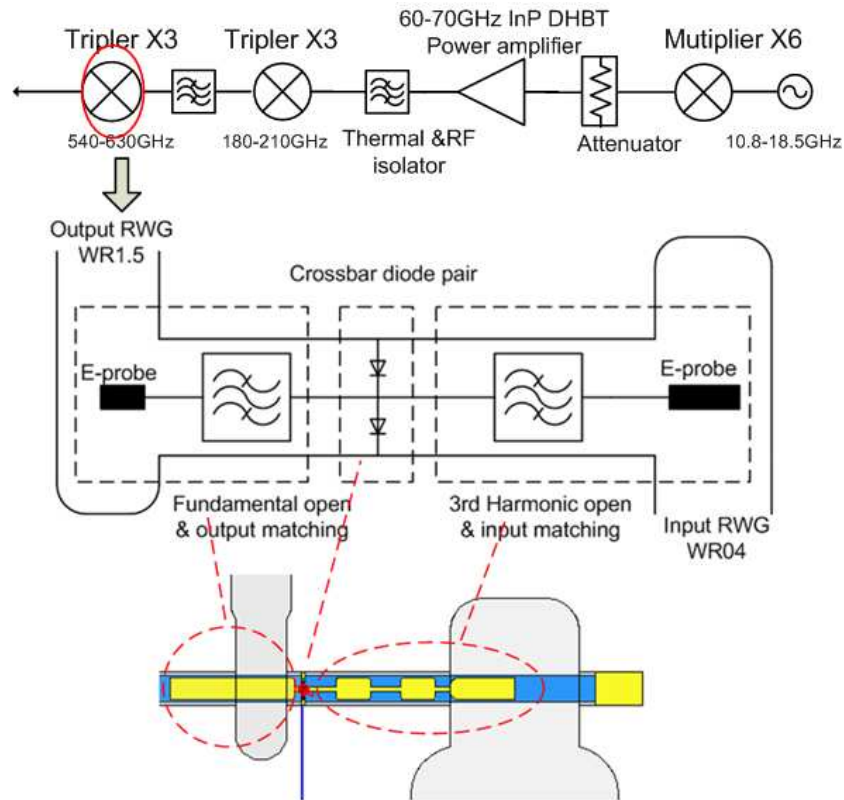


Figure 3.5: RF signal generation chain by combining the designed tripler and InP DHBT power amplifiers in this work. The inserted figure shows the generalized schematic diagram of the tripler.

The SHM and Tripler designs presented in this chapter are based on the non-biased crossbar configuration. It is relatively straightforward to modify the shown crossbar structure in order to implement the bias-able design foreseen in the future. This requires, however, a bypass capacitor to be integrated on the membrane circuit. Due to the additional complications

associated with this fabrication step it is chosen to implement the cross-bar SHM design without the bias possibility as the first iteration.

3.2 SHM specifications

The SHM design is based on Schottky diodes fabricated monolithically on a thin-film GaAs membrane. The SHM will be used to down-convert a RF signal at 557 GHz to an IF signal at 6 GHz. The associated LO input power is expected to be in the range from 2-4 mW. RF and LO ports use waveguide flanges with WR1.5(adapted to horn antenna) and WR03, respectively. The detailed specifications of the SHM are given Table.3.1.

RF frequency [GHz]	530-590
LO frequency [GHz]	274-286 (268-292)
IF frequency [GHz]	6
LO power [mW]	2-4
Conv. Loss [dB]	<13 (10)
Noise Temp. [K]	<5000 (2000)

Table 3.1: Sub-harmonic mixer specifications (Numbers in parenthesis are goals).

The Schottky diode technology used in this work is under development at Chalmers University of Technology. The microscope picture of the fabricated single-finger diode and measured IV curve are shown in Fig.3.6. The extracted diode parameters from DC and capacitance measurement are summarized in Table.3.2. The doping level of the epitaxial(EPI) and substrate layer is $5e+23 m^{-3}$ and $5e+24 m^{-3}$, respectively. The thickness of EPI layer is chosen to be 48 nm for low DC resistance under zero biasing condition.

Area [μm^2]	C_{j0} [fF]	R_s [Ω]	N_f	I_s [A]	V_j [V]
0.8	1.9	8.5	1.3	8e-14	0.85

Table 3.2: Extracted diode parameters from DC and capacitance measurements.

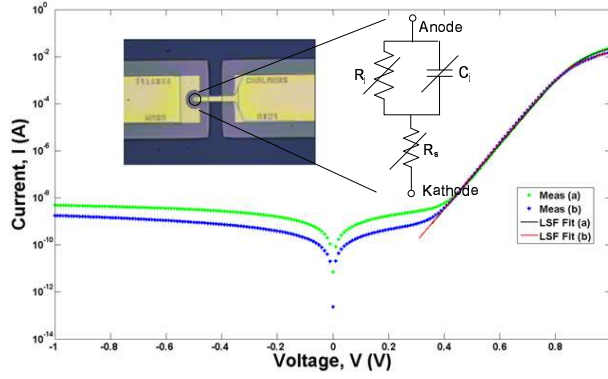


Figure 3.6: Measured IV curve from the single finger diode. Inserted picture is the fabricated single device from Chalmers and its simplified equivalent circuit model for the metal-semiconductor contact [28].

Cutoff frequency of the diode from Chalmers can be characterized by its extracted series resistance and zero-junction capacitance as

$$f_c = 1/(2\pi R_s C_{j0})$$

With the measured series resistance R_s of 8.5 Ω and zero junction capacitance C_{j0} of 1.9 fF, the estimated cut-off frequency for this diode is 9.8 THz, which is much larger than the operation frequency of SHM. The maximum current to handle for this diode is derived from the saturated electron velocity. With the EPI doping level of $N_{epi} = 5 \times 10^{23} \text{ m}^{-3}$, mobility of $\mu_{epi} = 3000 \text{ cm}^2/\text{Vs}$, and assumed 3.2 kV/cm field strength for start of electron velocity saturation, the peak current can be calculated as

$$I = AJ = A\sigma E = AqN_{epi}\mu_{epi}E \quad (3.1)$$

where the dependence of mobility on E field is ignored for a rough approximation. For the diode with anode radius of 0.5 μm , an estimated peak current would be 6 mA. The transient current through the diode needs to be checked to avoid the degraded conversion loss due to the increased impedance from the low electron mobility.

3.3 Mixer and Resistive Multiplier Theory

The mixing properties of the crossbar diode pair can be seen from the power series of two antiparallel nonlinear elements. As shown in Fig.3.7, the voltage controlled current of a single nonlinear element can be expressed as,

$$I_1(t) = K + aV_{LO}(t) + bV_{LO}^2(t) + cV_{LO}^3(t)... \quad (3.2)$$

The current flow through the reversed component is

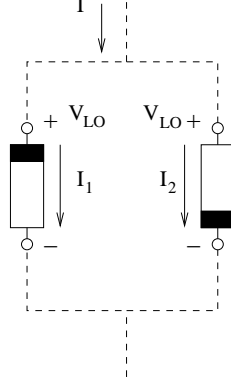


Figure 3.7: The current and voltage relationship of two antiparallel nonlinear elements.

$$I_2(t) = -K + aV_{LO}(t) - bV_{LO}^2(t) + cV_{LO}^3(t)... \quad (3.3)$$

The total current

$$I = I_1(t) + I_2(t) = 2aV_{LO}(t) + 2cV_{LO}^3(t)... \quad (3.4)$$

has only odd order harmonic currents, and the even order harmonic currents internally circulates inside the loop due to the circuit symmetry. By calculating the derivative, the large-signal effective conductance can be formulated as,

$$G(t) = \frac{dI(t)}{dV_{LO}} = 2a + 6cV_{LO}^2(t)... \quad (3.5)$$

This time-variant conductance has only even order frequency components of the large driving signal. The small-signal current due to the superimposed signal v_{RF} will be

$$i(t) = G(t)v(t) = \left(\sum_{n=-\infty}^{\infty} G_n \exp(jn\omega_{LO}t) \right) v_{RF}(t) \quad (3.6)$$

where G_n is the coefficients of its fourier series. Its even order components will mix together with the incident RF signal.

The time-variant conductance of a Schottky diode can be derived from its current and voltage relationship

$$G(t) = \frac{dI_s(\exp(\frac{V_{LO}+V_{bias}}{N_f V_t}) - 1)}{dV_{LO}} = \frac{I_s}{N_f V_t} \exp(\frac{V_{bias}}{N_f V_t}) \exp(\frac{V_{LO}}{N_f V_t}) \quad (3.7)$$

The fourier coefficients is found to be,

$$G_n = \frac{I_s}{N_f V_t} \exp(\frac{V_{bias}}{N_f V_t}) \widehat{I}_m(x) \quad (3.8)$$

where $\widehat{I}_m(x)$ is the modified bessel function of order m with argument $x = V_{LO}/(N_f V_t)$. The numerical results of even order components such as $G_0, G_2, G_4...$ can be calculated based on the detailed diode parameter given in Table.3.2. Further investigation on the conversion loss of a crossbar SHM is handled by conversion matrix analysis [29]. To facilitate the analysis, the frequency of the mixing products is noted as $\omega_{IF} + n\omega_{LO}$ $n=0, -2, 2...$ According to this, the frequency of the incoming RF, image, and IF output signals can be represented as:

$$\omega_{IF} + 2\omega_{LO} = \omega_{RF} \quad (3.9a)$$

$$\omega_{IF} - 2\omega_{LO} = \omega_{Imag} \quad (3.9b)$$

$$\omega_{IF} + 0\omega_{LO} = \omega_{IF} \quad (3.9c)$$

With ignoring the higher orders of G_n , the current and voltage relationship of the nonlinear network can be formulated as

$$I_{-2}^* = G_0 V_{-2}^* + G_{-4} V_2 + G_{-2} V_0 \quad (3.10a)$$

$$I_0 = G_2 V_{-2}^* + G_{-2} V_2 + G_0 V_0 \quad (3.10b)$$

$$I_2 = G_4 V_{-2}^* + G_0 V_2 + G_2 V_0 \quad (3.10c)$$

where V_n $n=0, 2, -2$ is the incident RF, IF, image voltage components, and the conjugate sign is used for the negative frequency component. The corresponding current is represented as I_n .

The generic small-signal equivalent circuit for the crossbar SHM is shown in Fig.3.8 where $Y(\omega_{IF} + 2\omega_{LO})$ is the source admittance at the RF port,

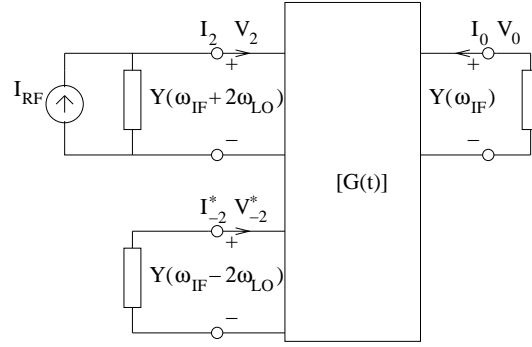


Figure 3.8: Generic small-signal equivalent circuit of the crossbar SHM circuit.

$Y(\omega_{IF})$ is the IF load admittance, and image impedance is represented as $Y(\omega_{IF} - 2\omega_{LO})$. By combining Eq.3.10, the current conservation for each port can be written as,

$$I_{RF} = Y(\omega_{IF} + 2\omega_{LO})V_2 + G_4V_{-2}^* + G_0V_2 + G_2V_0 \quad (3.11a)$$

$$0 = Y(\omega_{IF})V_0 + G_2V_{-2}^* + G_{-2}V_2 + G_0V_0 \quad (3.11b)$$

$$0 = Y(\omega_{IF} - 2\omega_{LO})V_{-2}^* + G_0V_{-2}^* + G_{-4}V_2 + G_{-2}V_0 \quad (3.11c)$$

With the assumption: real and even function of $G(t)$ and zero impedance of image signal, the coupled equations from Eq.3.11(a,b) between RF and IF ports can be simplified to be a two-port representation and the associated conversion loss is calculated as [30]

$$G_{conv} = 4 \left| \frac{G_2}{G_0 + Y(\omega_{IF})} \right|^2 \left| \frac{1}{Y(\omega_{IF} + 2\omega_{LO}) + Y_{in}(\omega_{IF} + 2\omega_{LO})} \right|^2 \times \Re(Y(\omega_{IF} + 2\omega_{LO})Y(\omega_{IF})) \quad (3.12)$$

where

$$Y_{in}(\omega_{IF} + 2\omega_{LO}) = G_0 - \frac{G_2G_2}{G_0 + Y(\omega_{IF})}$$

The estimated conversion loss of the crossbar SHM is shown in Fig.3.9. The numerical response is based on some empirical impedance values for RF and IF port from [29]: $Z_{IF} = 75 \Omega$ and $Z_{RF} = 50 \Omega$ in parallel with $3.0C_{j0}$ at 557 GHz. The estimated minimum conversion loss is about 5 dB. The similar procedure can be used for the resistive $\times 3$ multiplier with a fundamental

input frequency of 190 GHz as well, however the port impedance and frequencies for the incident and output signal are different. Fig.3.9 shows that the numerical result of conversion loss for a crossbar tripler is 10 dB. This agrees well with the statement of resistive $\times n$ multiplier with an efficiency of $1/n^2$ [29]. The extra loss compared to the SHM is due to the fact that the junction is loaded by the capacitance both at the fundamental input and third order harmonic output frequencies.

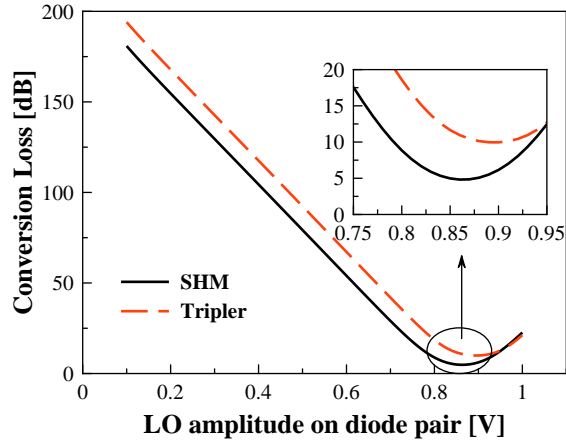


Figure 3.9: Numerical results of the conversion loss by using the crossbar diode pair (same as an antiparallel diode pair). The diode parameter listed in Table 3.2 are used in the calculation of large-signal conductance. The empirical impedance values for RF and IF ports [29] are used for estimation.

In reality, if both nonlinear series resistance, nonlinear junction capacitance, and non-zero image impedance are taken into account, the analysis of mixer circuit becomes complicated. In general, harmonic balance by checking all harmonic currents at each nonlinear element is used to search the correct time domain waveform for a junction voltage for example. Most of nonlinear simulation work in the later sections are completed with the harmonic balance tool.

3.4 Circuit configuration, propagation mode and power losses

3.4.1 Circuit configuration

Fig.3.2 summarizes two possible circuit topologies of the crossbar SHM. The main difference between them is the location to extract IF signal. In this work, the IF signal is extracted through the LO rejection filter as indicated in Fig.3.10. The SHM design shown in Fig.3.2(a) is very compact, however the RF E-probe presents a capacitive loading at the fundamental LO frequency limiting the LO bandwidth and the crossbar structure is too close to the RF waveguide wall increasing assembly difficulty. To minimize this parasitic open stub and make the circuit assembly easier, a half-wavelength transformer at the fundamental LO frequency is implemented to present an open circuit to the diode pair. This will simplify the design of LO matching circuit. To prevent the RF signal propagating into the LO port, two types of rejection filters are considered: the step-impedance and folded open stubs. Both types are designed and simulated, the comparison of two types of rejection filter are discussed later in Section

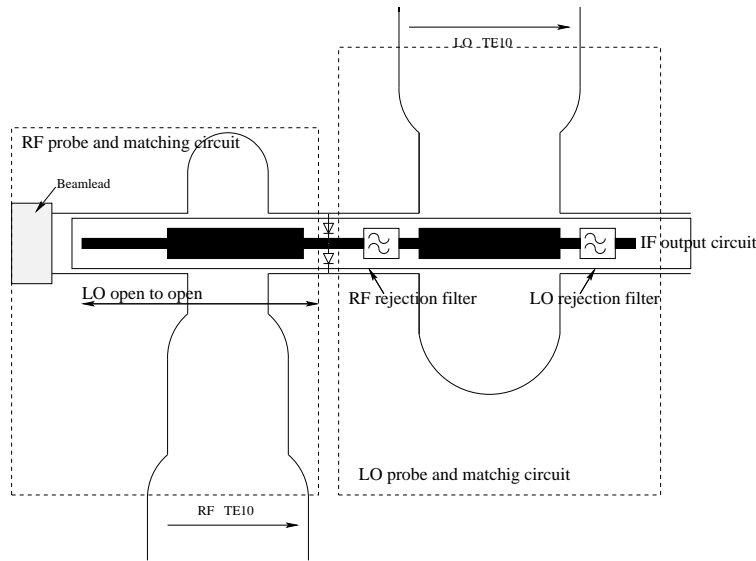


Figure 3.10: SHM circuit configuration employed in this work.

3.4.2 Propagation mode

As shown in Fig.3.10, the beamleads are used at both ends of the membrane to stabilize its position. The signal in this situation is propagated as suspended stripline mode. An alternative choice is to use extra beam leads which is clamped by upper and lower half waveguides such as in Fig.3.2(a). For this case, the propagation mode is dominated by the CPW even-mode. However, the cutoff frequency of the parasitic mode is significantly influenced by the gap between the center signal strip and beamleads. Unless much smaller channel dimension is used, the circuit is prone to the excitation of parasitic propagation modes due to the asymmetries introduced by waveguide to stripline transitions and the crossbar structure. As shown in Fig.3.11, for a fixed dimension of the micro-machined channel, the smaller the gap is, the lower the cutoff frequency is. For a fixed gap, the cutoff frequency reduces with the increased micro-machined channel dimension. Due to these considerations, the suspended stripline mode propagation is chosen and the channel dimension is $104 \times 150 \mu m^2$. Similar channel dimension with $80 \times 160 \mu m^2$ is adopted in a crossbar tripler design for 540 to 640 GHz application [27].

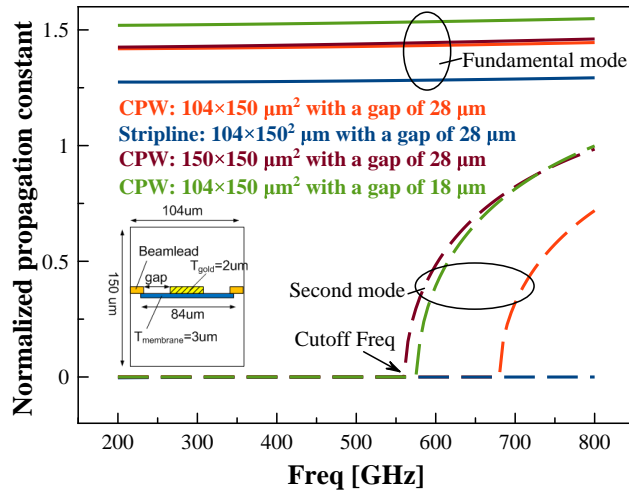


Figure 3.11: The normalized propagation constant towards $\beta_0 = \omega / \sqrt{\mu_0 \epsilon_0}$ for different channel dimensions. The normalized fundamental and second mode propagation constant of a specific channel dimension are represented by solid and dashed lines with the same color. The inserted figure shows the dimensions used for the mode calculation.

3.4.3 Power loss

The power loss due to the conductor and dielectric materials is investigated. For conductor loss, there are two ways for EM numerical solver to take into account of the skin effect at this high frequency region: surface mesh(sheet conductor) or volume mesh (solve inside of the metal). As expected, the former one uses only surface meshes on the high conductivity materials to save the computation efforts but is less accurate than the latter one. Both methods are used to characterize an uniform transmission line of 123Ω with a width of $15 \mu\text{m}$. Fig.3.12 shows that if only conductor loss is considered, volume mesh is more accurate compared to the theoretical calculation. The dielectric loss is included further by setting the loss tangent of GaAs material to 0.006. Two slopes of frequency dependency are used for dielectric (slope=1) and conductor loss (slope=0.5) identification. As shown in Fig.3.12, the conductor loss dominates at the low frequency region. The high frequency range is dominated by the dielectric loss due to its linear frequency dependence. The dielectric attenuation from theory is over-estimated due to the fact that homogeneous dielectric material is assumed in the calculation. To estimate the power loss of a membrane circuit with length of 2 mm, the extracted attenuation constant at 600 GHz is used for calculation. This indicates the highest power loss of 1.1 dB.

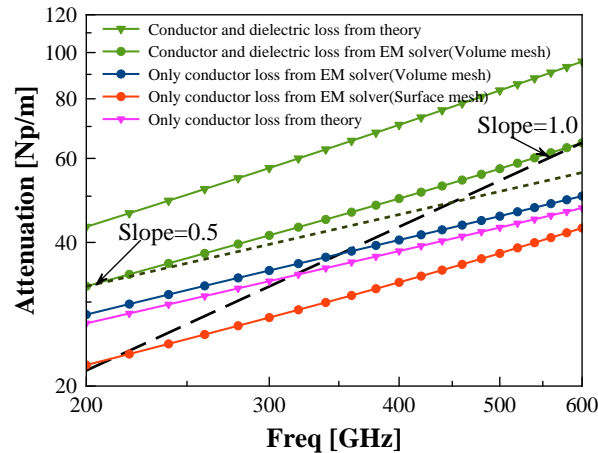


Figure 3.12: Attenuation analysis of an uniform suspended strip line: the simulated power loss from conductor and dielectric material with different mesh seeding methods. The theoretical power loss is also shown for comparison. Two dashed lines with different slopes are used for identifying the dominant loss contribution.

3.5 Optimum impedances

3.5.1 Optimum impedance of the SHM

To investigate the variations of the optimum impedance for the crossbar SHM due to the parasitics, a detailed parameterized diode EM model is build in the 3D EM simulator, HFSS. The corresponding diode can be represented by a lumped port [12, 20, 27, 31] inside of the structure. The S-parameters from the EM numerical simulation are imported into ADS as a four-port device for further analysis, where two ports are used for diode connection and the other two are wave ports for transmission line connection. The EM-circuit co-simulations are performed to get the optimum impedance of each port by using a load pull simulation setup [32]. This means that several iterations are needed to make the optimum impedance converge for all the ports simultaneously.

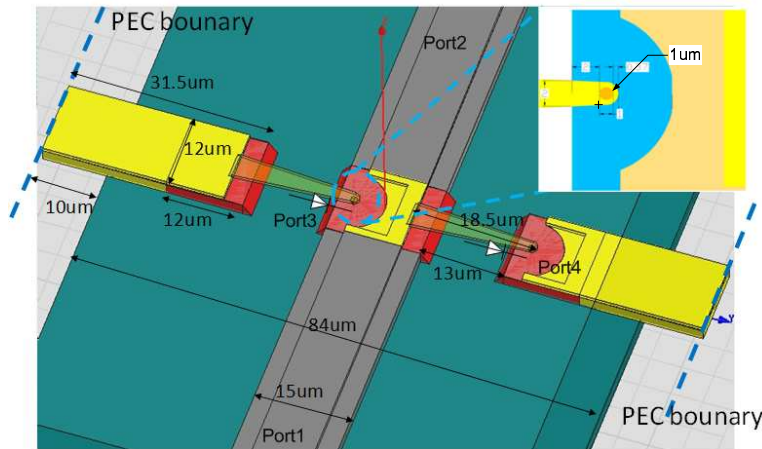


Figure 3.13: EM model of the crossbar configuration inside of the metallic housing. The inserted figure shows the tapered finger geometry [28].

Fig.3.13 shows the crossbar structure under investigation. The diodes are fabricated on a GaAs membrane with the feature technology: $18.5 \mu\text{m}$ finger length, $13 \mu\text{m}$ mesa to mesa distance and $1 \mu\text{m}$ diameter of anode contact. The direct connection to the side walls of the micro-machined channel provides DC&IF return path for the series diode pair. The channel dimension is chosen to be $104 \times 150 \mu\text{m}^2$ from the previous investigation to avoid

the propagation of higher parasitic modes. The suspended membrane has a width of $84 \mu\text{m}$ with a thickness of $3 \mu\text{m}$. The material of the transmission lines is gold with a thickness of $2 \mu\text{m}$. The parasitics from the crossbar configuration is expected to arise from the finger inductance and capacitances between the finger to mesa and mesa to mesa [31, 33]. To improve the simulation accuracy, the mesh density is increased locally on the finger and related mesa structures [12, 20, 23]. The load pull simulation setup uses 283 GHz and 560 GHz for the fundamental LO and RF frequencies, respectively. The LO pumping level is chosen to be -1 dBm. The reason for using this rather low LO pumping level is that initial investigations show that this level is sufficient to fully saturate the SHM.

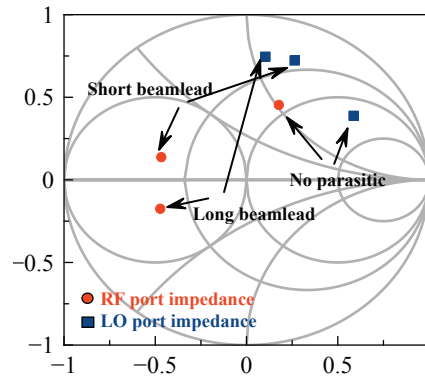


Figure 3.14: Investigation of the beamlead parasitic influence. The RF and LO optimum impedance are represented with red and blue color respectively. The diode parameters used in the load pull setup are listed in Table 3.2. The SHM is simulated at $LO_{freq}=283 \text{ GHz}$, $RF_{freq}=560 \text{ GHz}$ and $LO_{freq}=6 \text{ GHz}$.

To check the influence of parasitics from the beamlead, the PEC boundary in Fig. 3.13 is shifted to the different locations. The corresponding optimum LO and RF impedance are compared on Smith chart with the case of ideal crossbar configuration in absence of any parasitics in Fig. 3.14. The extra beamlead introduces parasitic inductance and shift the impedance on the constant resistance circles. To check the sensitivity of the optimum impedances due to the different symmetric plane and mesa size, several different structures shown in Fig. 3.15(a) are compared. To keep the consistency of the simulations, the frequencies used are kept same as in Fig. 3.14. Fig. 3.15(b) shows that the corresponding optimum impedance converges to

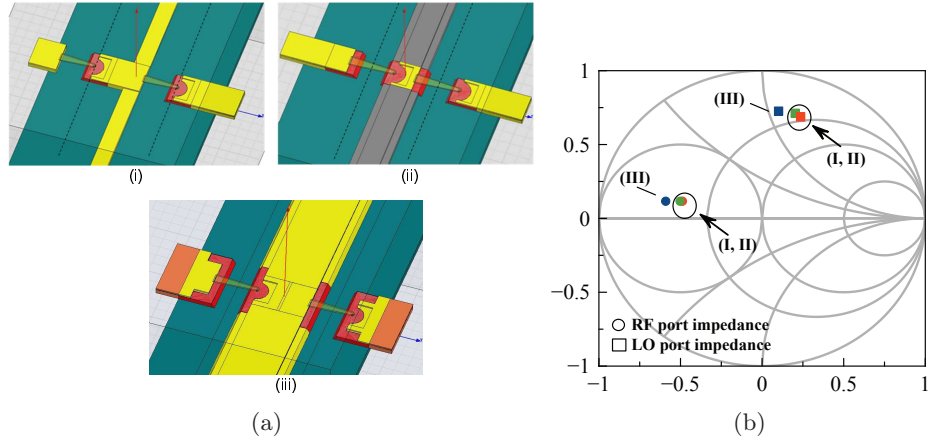


Figure 3.15: (a) Comparison of different structures: (i) the diode is anti-symmetric about the central strip line [12] (ii) the finger structure is anti-symmetrical about the central strip line (iii) the larger dimensions of central mesa. (b) the corresponding optimum impedance on Smith chart.

the same region.

To get accurate optimum impedance for matching circuit synthesis, iterative load pull simulations are performed until the convergence of optimum impedance for each individual port. Fig.3.16 shows the contours of conversion loss for each port. They are found by sweeping the port impedance on the Smith chart at the LO power of -1 dBm. And the corresponding conversion loss for each tested impedance is recorded. The optimum IF impedance is very close to 100Ω for most cases. The final optimum impedances for the SHM design are listed below.

- $Z_{LO} = (11.2 + j*68.5)\Omega$
- $Z_{RF} = (17.6 + j*6.3)\Omega$
- $Z_{IF} = 100\Omega$

Based on the optimum impedance from the load pull, the conversion loss and power matching performance are checked by sweeping the LO power up to +4 dBm with an available RF power of -30 dBm. Ideal impedance networks and narrow band filters are used to short the other mixing products and higher order harmonics. Fig.3.17(a) shows that the conversion loss and

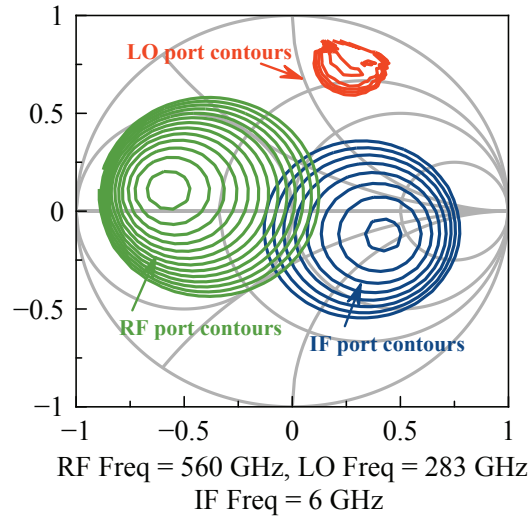


Figure 3.16: Conversion loss contours for each port of the SHM. Numerical results are based on LO power level -1 dBm. The step of contours for LO port is 0.25 dB, the other ports are with a step of 0.5 dB. All impedance are normalized to $Z_0=50 \Omega$.

coupled RF power saturate at the LO power level larger than -1 dBm. The corresponding return loss at the LO&RF port is better than 10 dB as shown in Fig.3.17(b). Fig.3.17(c) shows the coupled LO power, which has a slope of one at the high end of power sweeping due to the lossless matching network. The time domain current waveforms for both diodes with the LO power of -1 dBm are shown in Fig.3.17(d). The peak current through the individual diode is smaller than 6 mA (calculated peak current before). The dynamic current wave form provides useful information to maintain the diode working in the safe operation region [34].

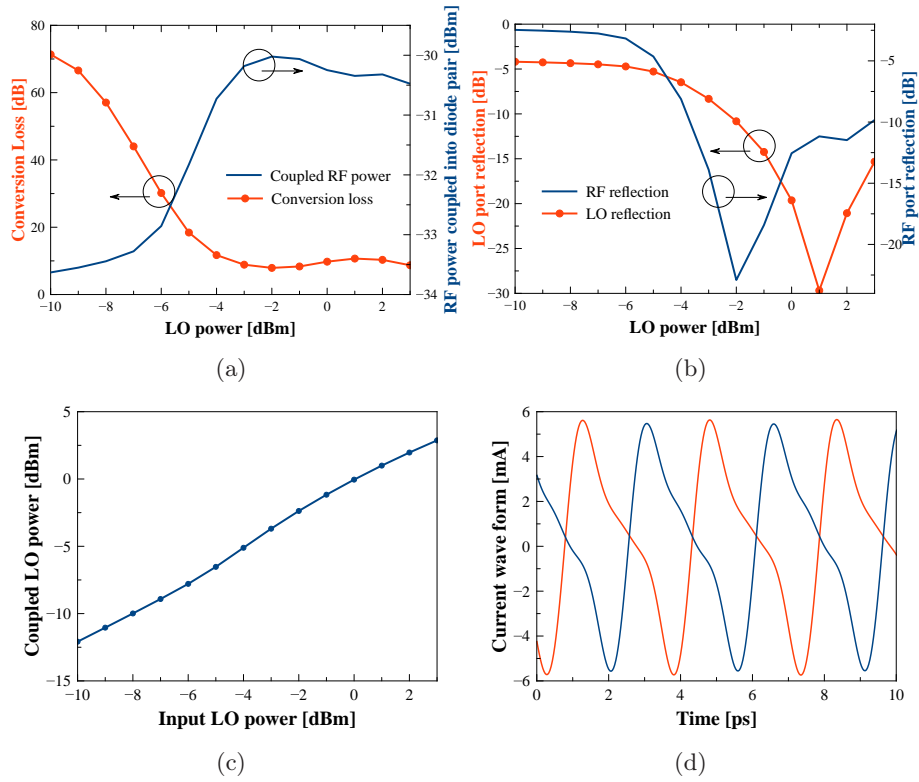


Figure 3.17: SHM large-signal performance by sweeping the LO power levels with ideal filtering networks and terminations for all other mixing components and high order harmonics: (a) conversion loss and coupled RF power into the diodes (b) LO and RF port reflection (c) LO power coupled into the diodes (d) time domain current waveforms for both diodes at -1 dBm LO power level.

3.5.2 Optimum impedance of the tripler

A similar load pull simulation setup has been used to find the optimum impedance for the tripler design with the aim to generate the RF signal at 557 GHz for measurement purposes. As shown in Fig.3.18, the contours of conversion loss and coupled input power are shown with fundamental input power of +3 dBm at 186 GHz. They converge to the same area on Smith chart. Fig.3.18 also indicates that the associated fundamental source impedance is very concentrated. The optimum source impedance can be easily identified for the minimum conversion loss. The simulated conversion loss with ideal impedance networks is 10.6 dB corresponds to a peak efficiency of 8.7 %. This agrees well with the conversion matrix analysis in Section 3.3.

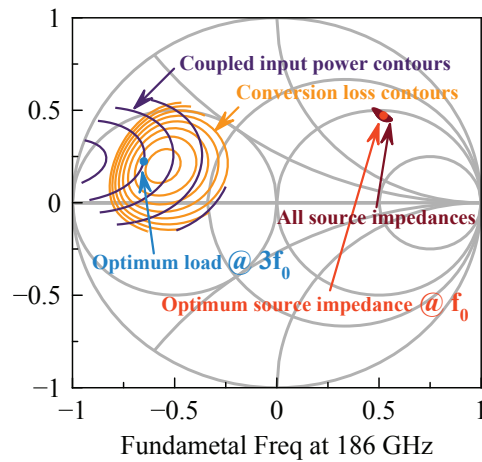


Figure 3.18: Conversion loss contours with a step of 0.1 dB and coupled fundamental input signal power contours with a step of 0.05 dB are shown. The corresponding source impedances at the fundamental frequency are also indicated. The final optimum load and reflected input impedance for circuit simulation are noted. All impedance level are normalized to 50Ω .

With the knowledge of the optimum impedance for each port, the matching circuit design can be synthesized. The designed planar circuit is typically embedded in E-plane split blocks which is by far the most common way in sub-millimeter wave system. The waveguide probes are necessary to couple the EM energy from the standard TE_{10} mode to the planar circuits. The probe pattern can be used to simplify the matching circuit and optimize the bandwidth. Therefore, the equivalent circuit model of E-probes is investigated firstly.

3.6 Equivalent circuit model for E-probe transition

In order to understand how the probe pattern interferes with the transformed impedance, an equivalent circuit model of the transition junction is highly desirable. Previous works [35–37] have shown that either capacitive or inductive probe can be used for energy coupling. Both types of probes can be used for transition junction where the suspended membrane is perpendicular as well as parallel to the broadside wall of waveguide. As shown in Fig.3.19(a) and Fig.3.19(b), the cross-section view on the $[X-Y]$ plane indicates that the membrane can be placed either perpendicular or parallel to the broad waveguide wall. From the cross-section view on the $[X-Z]$ plane, Fig.3.19(c) and Fig.3.19(d) show that both capacitive and inductive probes can be used for transition junction in a perpendicular orientation as well.

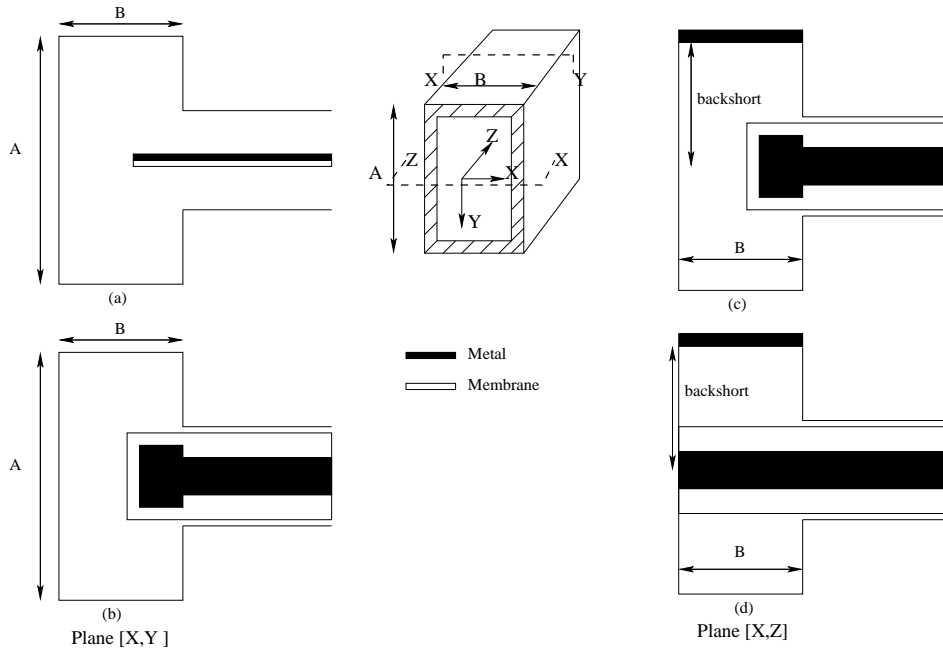


Figure 3.19: Summary of the substrate orientation and probe types:(a) EM energy is coupled into the circuit with the substrate perpendicular to the broadside wall of the waveguide (b) the substrate is parallel to the broadside wall of the waveguide (c) capacitive E-probe with perpendicular orientation of the substrate (d) inductive E-probe with perpendicular orientation of the substrate.

Previous studies [15, 38] have stated that the inductive probe can be modeled with a parasitic inductor which connects the suspended strip line to the broadside wall of the waveguide. This type of probe is particularly useful for SHMs based on the antiparallel configuration due to the associated DC&IF return path. The capacitive probe is also widely used in mixer and multiplier designs. In this section, improved equivalent circuit models for both inductive and open transitions are reported. The dimension of the micro-machined channel is $104 \times 150 \mu\text{m}^2$. The reduced height waveguide is $381 \times 126 \mu\text{m}^2$, the other relevant dimension parameter for the simulation setup are indicated on Fig.3.20.

The equivalent circuit model in Fig.3.20(a) shows that the transition junction of an inductive E-probe can be modeled with a series lumped inductor L_p and a shunt parasitic capacitor C_p . The length of back short and input reduced height waveguide L_{bs} and L_{in} are tunable to take into account the influence of the aperture on the waveguide. By fitting the proposed equivalent circuit model to the EM simulation results, the values of L_p and C_p are estimated to be 40 pH and 1.2 fF for the structure under investigation, respectively. Fig.3.21(a) shows that the equivalent circuit model reproduces the frequency responses of the transition in the wide frequency range. The negative reactance indicates that the shunt parasitic capacitor C_p is necessary to be included in the equivalent circuit model because it dominates for high frequency range. Similarly, the equivalent circuit model for a capacitive E-probe is shown in Fig.3.20(b). A fringing capacitor C_f is used to replace the L_p in the previous case. The corresponding C_f and C_p are fitted with 1.18 fF and 2.6 fF. Even though the resulted equivalent circuit models of capacitive probe does not perfectly fit the EM simulations at all frequencies, it helps to understand the principle behind the similar probes and use them to be part of the matching circuit. Depending on the position of optimum impedances, the pattern of the E-probe can be optimized to simplify the matching circuit and increase the bandwidth.

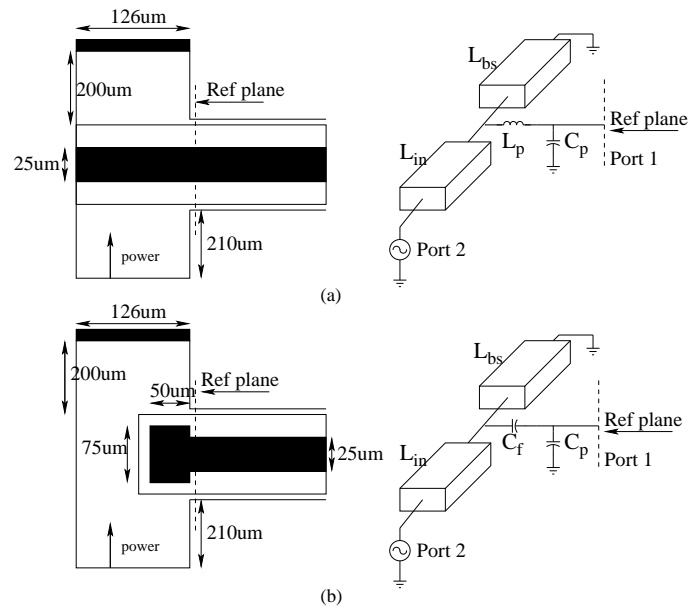


Figure 3.20: Equivalent circuit models of (a) inductive E-probe and (b) capacitive E-probe.

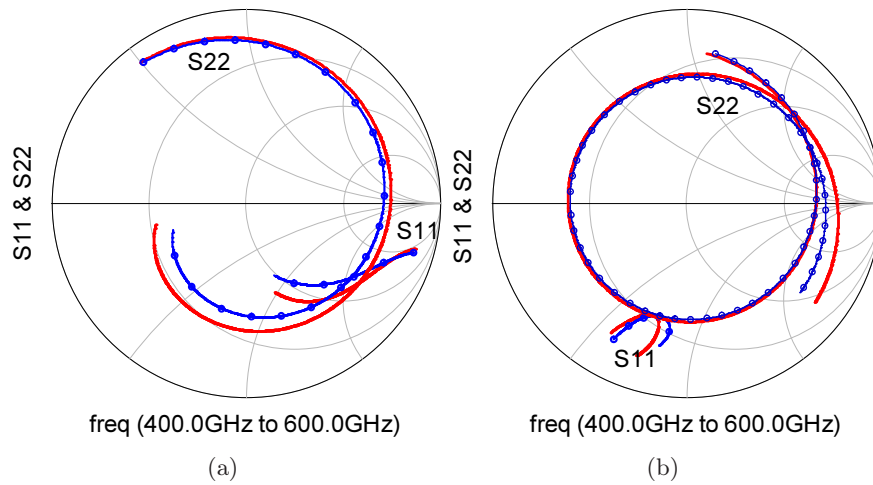


Figure 3.21: Comparison of frequency responses from EM numerical simulation and the corresponding equivalent circuit model: (a) inductive E-probe (b) capacitive E-probe.

3.7 RF probe and matching circuits

Based on the previous discussion on the equivalent circuit model of the E-probe, RF matching circuit can be optimized for wideband performance. EM-circuit co-simulation method is widely used for matching circuit design in this work. Due to the fact that both TE_{10} and suspended strip line modes are involved for the E-probe transition design, different type of impedances have to be considered. To keep the consistency of the impedance definition between standard rectangular waveguide and EM simulator, the power-voltage definition is used to calculate wave impedance in HFSS [39]. With the frequency dependent impedance definition for waveguide components, the EM-circuit co-simulations can predict wideband frequency response accurately and reduce EM computation efforts.

The methodology of a matching circuit design is to use the E-probe transition itself and the reduced height waveguide: L_{bs} and L_{in} to be part of the RF matching circuit. The reduced height waveguide is employed to lower the impedance ratio between the waveguide and suspended strip line mode [7, 10] and moves the impedance curve closer to the center of Smith chart.

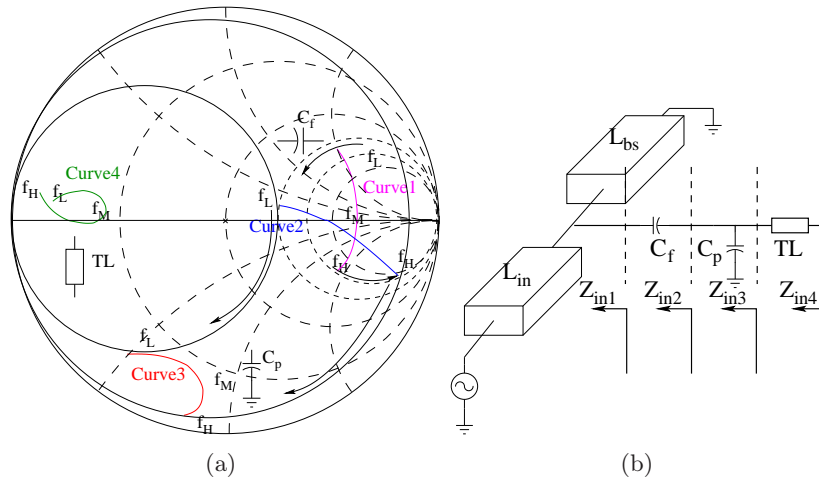


Figure 3.22: Generalized impedance transformation procedure with a capacitive E-probe. The impedance at different reference planes corresponds to the different impedance curves on Smith chart.

To generalize the impedance transformation procedure, the impedance curves at different reference planes are shown and compared on Smith chart in Fig.3.22. At first, a quarter-wavelength back short waveguide is designed at the middle frequency f_m of the interested band. Due to the short-circuit to open-circuit transition of the back short waveguide, the wave impedance Z_{redwg} of the reduced height waveguide is presented at the strip line port. At the lower and upper frequency boundaries: f_L and f_H , the quarter wavelength waveguide presents a reactive component. This means that the impedance curve 1 follows the constant conductance circle. However, due to the frequency dependence of the waveguide impedance, the impedance curve bends toward infinity at the lower boundary of frequency range. The combination effect of series capacitor C_f and shunt C_p leads to the impedance curve 3 shown in Fig.3.22. The length of the back short waveguide, reduced height dimension, width of the probe, and the probe penetration distance into the waveguide are important parameters to optimize the probe behavior. Based on the optimized geometry of the probe pattern, capacitive impedance curve 3 transforms to the optimum RF impedance through a short transmission line. Due to the fact that lower and upper frequency boundaries move with different phase velocity, the final impedance curve 4 is curled and achieves wideband impedance matching properties.

An example of this type matching circuit design is shown in Fig.3.23(a). In this case, the RF E-probe behaves like a capacitive loading at the fundamental LO frequency. Its response can be fitted by an open stub with 58° as shown in Fig.3.23(b). With the knowledge of the optimum RF impedance: $Z_{RF} = (17.6 + j6.3)\Omega$, the width of E-probe pattern is optimized for wideband performance. The associated frequency response is shown in Fig.3.23(b). The curled impedance curve implies the wideband matching properties. The capacitive loading from the RF E-probe at the fundamental LO_{freq} will increase the difficulty of wideband matching at the LO port.

To overcome this problem, another type of RF probe can be employed which integrates the half wavelength of open to open transformer at the fundamental LO frequency. Fig.3.24(a) shows the layout of the new RF probe. As indicated, the micro-machined channel has to go through the RF waveguide, and the GaAs membrane is clamped at the far end. Width of the probe is optimized to simplify the matching circuit, and the frequency response is shown in Fig.3.24(b). Markers indicates that the RF matching circuit behaves as open-circuit at the fundamental LO_{freq} and presents an optimum impedance Z_{RFopt} at RF_{freq} to the diode pair, respectively.

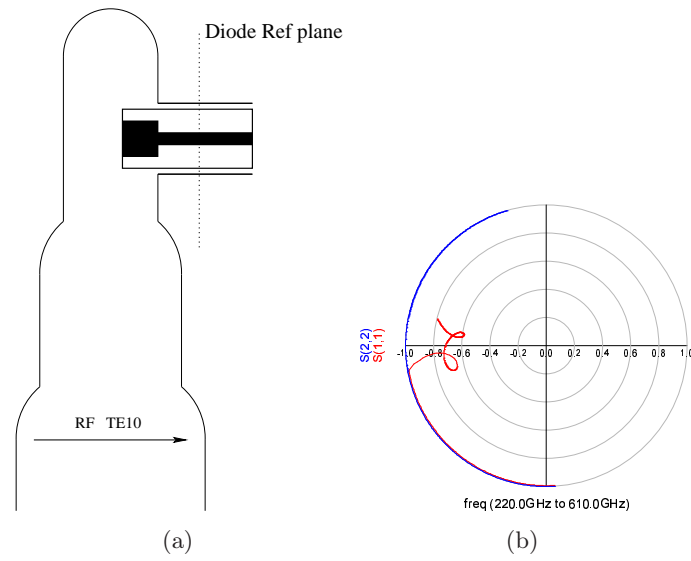


Figure 3.23: Frequency responses of RF capacitive E-probe: (a) physical layout (b) the corresponding frequency responses. An open stub (blue color) at fundamental LO frequency is used to fit the low frequency response of the RF matching circuit (red color).

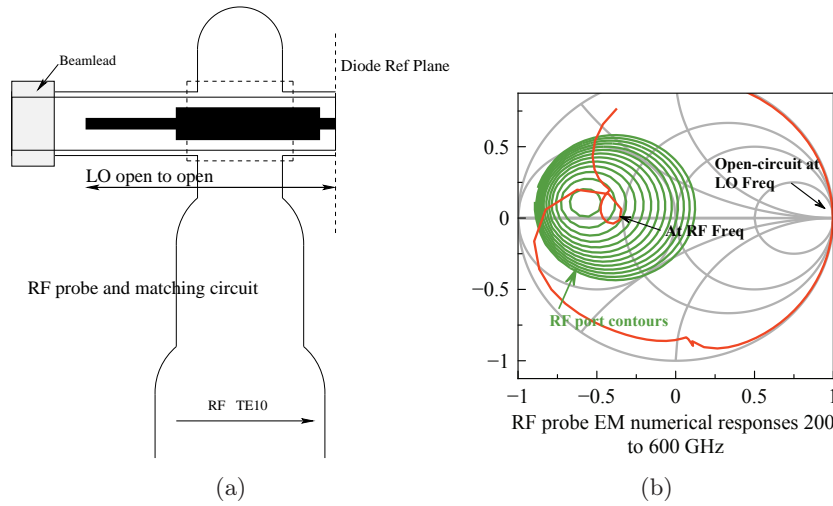


Figure 3.24: Frequency responses of the RF E-probe with half wavelength transformer: (a) physical layout and (b) responses on the Smith chart. The contours of conversion loss for RF port is also shown.

3.8 RF rejection filter

Contrary to the typical antiparallel configuration [15, 22, 40], crossbar structure needs an open circuit for both fundamental RF and LO signals [5, 12]. In this section, a comparison between step-impedance and open stub(OS) rejection filters is presented. The purpose is to find the optimum solution in term of the circuit complexity, circuit model, and power loss.

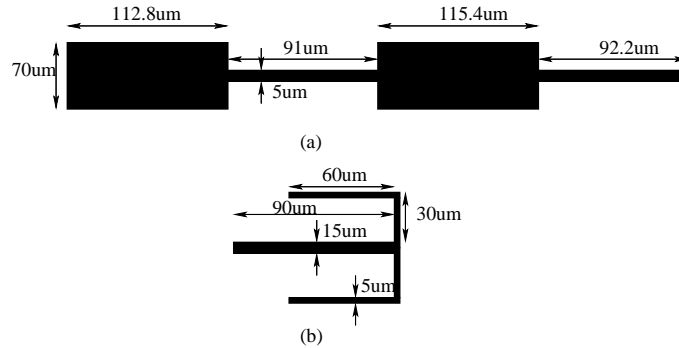


Figure 3.25: Two types of RF rejection filters:(a) two-section step impedance rejection filter (b) folded open stubs filter.

For the channel dimension of $104 \times 150 \mu m^2$, the achievable lowest and highest line impedance is 60Ω and 156Ω . The physical dimensions shown in Fig.3.25(a) are used to build two-section step-impedance rejection filter. The different physical length of the step-impedance section means that length compensation is already taken into account for minimizing the parasitics influence from the discontinuities. The physical dimension of the rejection filter with open stub is shown in Fig.3.25(b). As compared, the latter one has an advantage of smaller dimension.

Fig.3.26 shows the simulation results from the circuit models and the full wave EM simulator for both rejection filters. The good agreement shown in Fig.3.26(a) indicates that the step impedance rejection filter can be modeled precisely with the ideal transmission line elements. While Fig.3.26(b) shows that there is a large discrepancy between EM numerical result and schematic simulations for the open stubs filter. It is due to that the coupling effect between the stubs, central strip, and the side walls of the channel are not correctly modeled. To predict the circuit response accurately, the coupled multiple suspended strip lines should be resorted.

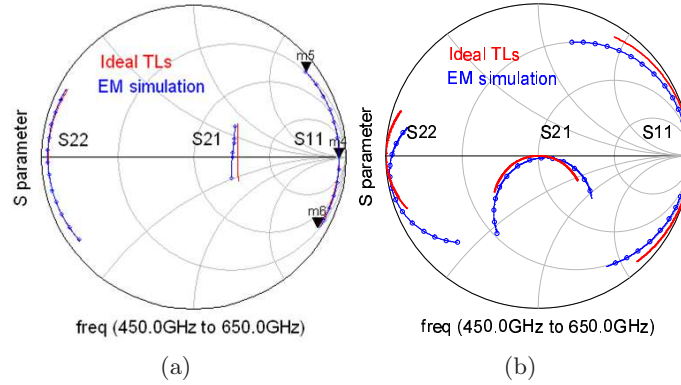


Figure 3.26: Simulation results from circuit models and EM solver are compared: (a) step-impedance rejection filter (b) OS rejection filter

To compare both types of rejection filters, one criterion is the rejection level. As shown in Fig.3.26, for a limited RF bandwidth (<60 GHz), the open stub rejection filter is superior than the other. The other criterion of comparison is the power loss. The associated normalized power loss ($1 - |S_{11}|^2 - |S_{21}|^2$) of each filter is summarized in Fig.3.27. Both filters are simulated with lossless dielectric material. The power loss considered here are due to the conductor loss and radiation. Volume mesh (solve inside) is employed to solve the EM field inside of the conductor accurately, and the multiple layers of thin conductors are used to increase the mesh density. The simulation result with surface mesh is included as well. As shown in Fig.3.27, the power loss is more accurately estimated by volume mesh method. The radiation loss from the open stub structure is higher than step-impedance filter for the frequency range from 500 to 600 GHz. However, the higher power loss of step-impedance filter at lower frequency range below 400 GHz is due to the large conductor loss by the long circuit dimension. Both types of rejection filters are implemented for the SHM design. Due to the higher dispersion from the folded open stubs, there is no accurate circuit model and this limits the optimization freedom for the matching network synthesis.

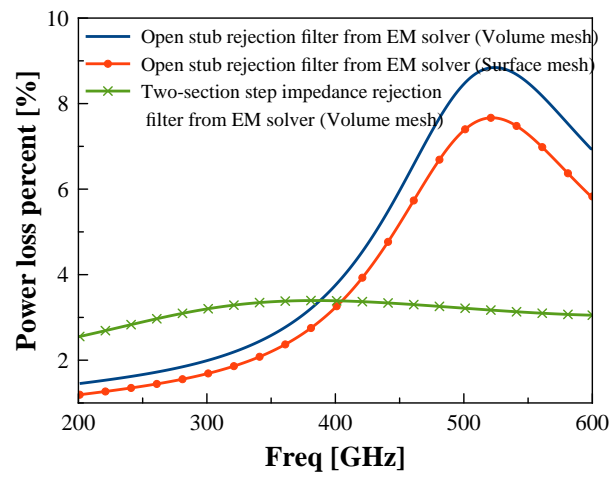


Figure 3.27: Power loss comparison with surface and volume mesh for both rejection filters.

3.9 LO matching and IF output circuit

Similar EM-circuit co-simulation routines are used for optimizing the LO matching circuit. The different rejection filters are compared in term of LO matching bandwidth. With the knowledge of the LO optimum impedance, an open-circuit is provided to LO signal by an OS rejection filters as shown in Fig.4.12(a). The high isolation due to the open stubs minimizes the LO-IF leakage and ensures that the LO power is effectively coupled into the diode pair. The good isolation also implies that the IF circuit can be designed separately. The impact of beamlead dimension is small and can be chosen with a great freedom to make robust mechanical support. Due to the low IF frequency, a transmission line with characteristic impedance of 100 Ω is directly used for output power matching. Fig.4.12(b) shows LO and IF matching circuits are designed based on step impedance filter. The transformed LO impedance are shown on the Smith chart in Fig.3.28(c) together with conversion loss contours for LO port. It indicates that both design have a similar bandwidth.

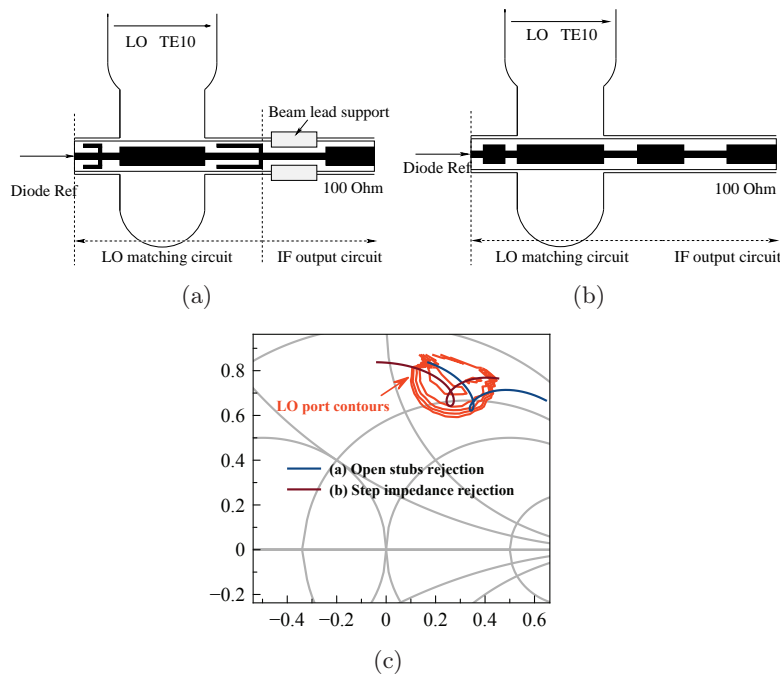


Figure 3.28: Two types filters employed for LO & RF rejections: (a) Open stubs (b) step-impedance (c) the transformed LO impedance on Smith chart. The conversion loss contours of LO port is also displayed.

3.10 SHM performance

The designed SHMs are characterized by sweeping the LO power (P_{LO}), RF frequency (f_{RF}) and LO frequency (f_{LO}) to check the conversion loss and bandwidth performance. To terminate the unwanted mixing components and higher order harmonics, EM structures of RF, LO and IF circuits are separately simulated up to 1.5 THz due to the reduced computation efforts. The final circuit performance are estimated by combining all different parts. The accuracy of this procedure is verified in Section.3.10.3. Due to the fact that LO bandwidth is always the limiting factor of SHM design, extra efforts are put to achieve better LO bandwidth performance.

3.10.1 The first SHM design

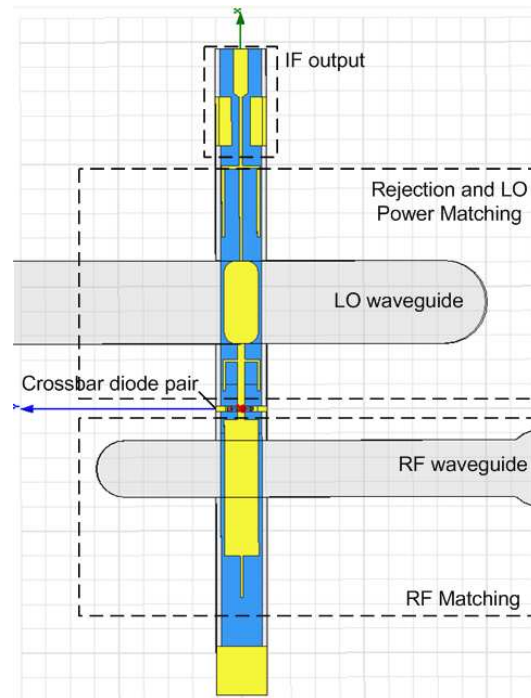


Figure 3.29: The proposed SHM layout.

The first SHM design shown in Fig.3.29 uses the folded open stubs to improve the rejection and minimize the overall circuit length. Fig.3.30 shows

the SHM large-signal performance obtained by sweeping the LO power from -4 to +4 dBm with a RF power of -30 dBm. Fig.3.30(a) shows that the simulated conversion loss and coupled RF power show saturation for LO power levels from +3 to +4 dBm. At these power levels, the corresponding return loss at both RF and LO ports in Fig.3.30(b) are better than 10 dB. The predicted noise temperature is shown in Fig.3.30(c). The noise sources of the simple diode model include the thermal noise of the series resistance and the shot noise of the junction. The predicted SHM noise temperature is from 1300 to 500 K for LO power levels from +1 to 4 dBm. However, the hot-electron noise is expected to give rise to an additional 1000 K increase in the noise temperature [5]. It should be noticed that the presence of hot-electron noise actually would lead to an increase for higher LO power levels.

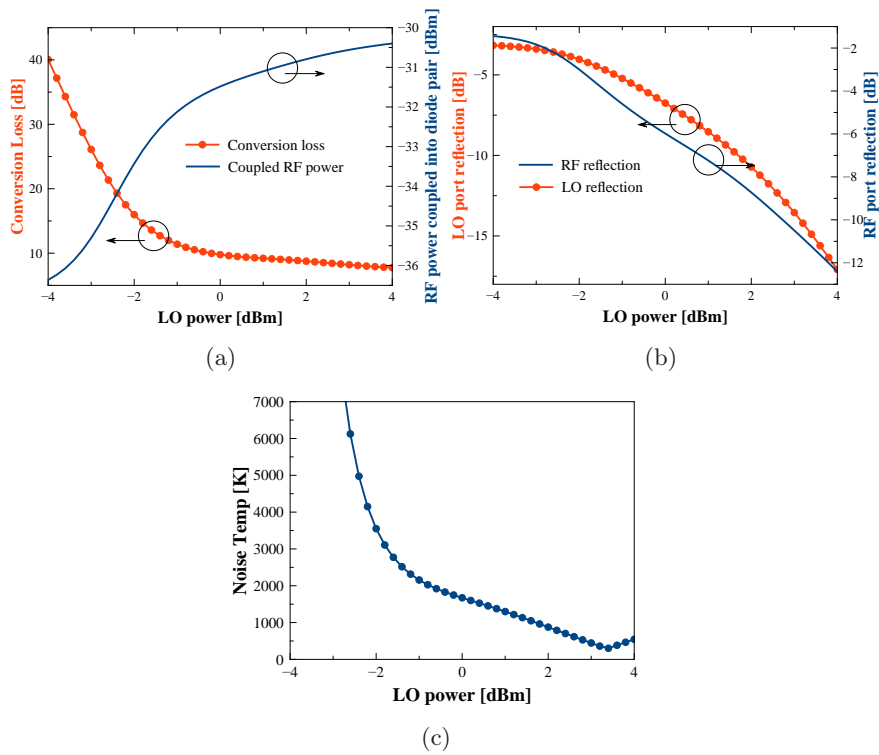


Figure 3.30: SHM performance by sweeping the LO power from -4 dBm to +4 dBm for a fixed RF_{freq} at 560 GHz and LO_{freq} at 283 GHz: (a) conversion loss and coupled RF power (b) reflection at RF& LO port (c) noise temperature.

Fig.3.31 shows the RF bandwidth performance of the SHM at different

LO power levels. With a fixed LO_{freq} at 276 GHz, the estimated conversion loss in Fig.3.31(a) is better than 10 dB for a 120 GHz bandwidth. Fig.3.31(b) shows that the RF port return loss has 10 dB bandwidth from 520 to 610 GHz. By sweeping the LO_{freq} from 250 to 300 GHz with a fixed IF_{freq} at 6 GHz, the associated RF and LO port responses are summarized in Fig.3.32 and Fig.3.33. With the knowledge of -30 dBm available RF power at $2LO_{freq}+IF_{freq}$, Fig.3.32 indicates that the estimated power loss on RF path is about 0.4 dB and RF port has a 60 to 70 GHz bandwidth for 10 dB return loss. Fig.3.33 shows that the LO port has a 25 GHz bandwidth for 10 dB return loss and 40 GHz bandwidth for conversion loss better than 10 dB.

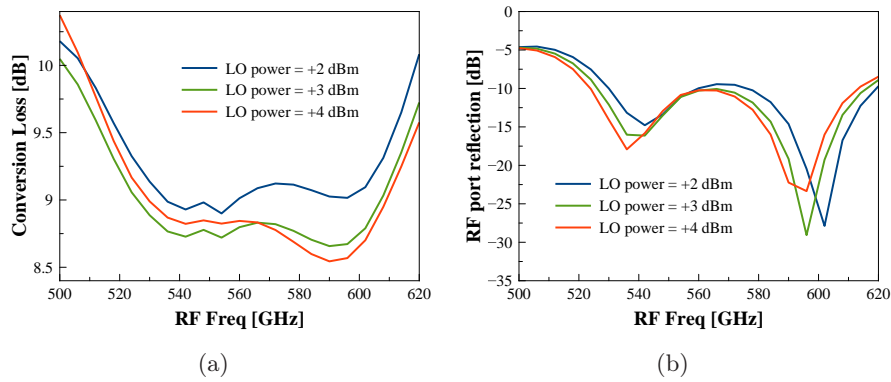


Figure 3.31: RF bandwidth performance with different LO input power levels from +2 to +4 dBm and a fixed LO_{freq} at 283 GHz: (a) conversion loss (b) RF port bandwidth.

The LO port shows similar bandwidth as the goal of SHM specification as specified in Table3.1. The design flexibility for power matching circuits is limited due to the lack of available accurate circuit model for the coupled open stubs. However, this is compensated by manipulating the LO input waveguide sections [23, 26]. The second version of SHM is based on the step impedance filters, and its responses can be well modeled. This of course increases the optimization freedom.

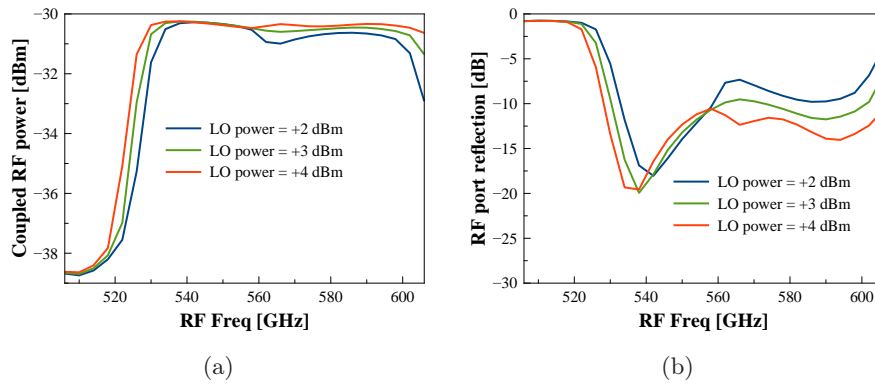


Figure 3.32: RF port responses by sweeping LO_{freq} from 250 to 300 GHz with different LO power levels from +2 to +4 dBm. IF_{freq} is fixed at 6 GHz and RF_{freq} is set to be the upper sideband signal at $2LO_{freq} + IF_{freq}$: (a) coupled RF input power (b) RF port reflection.

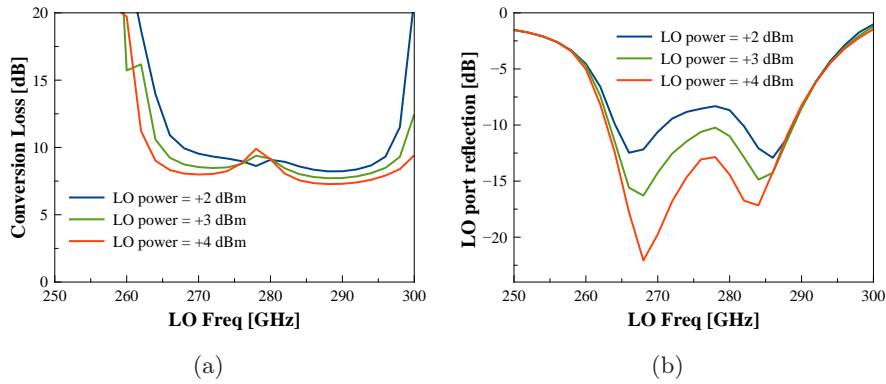


Figure 3.33: LO RF port responses by sweeping LO_{freq} from 250 to 300 GHz with different LO power levels from +2 to +4 dBm. IF_{freq} is fixed at 6 GHz and RF_{freq} is set to be the upper sideband signal at $2LO_{freq} + IF_{freq}$: (a) conversion loss (b) LO port reflection.

3.10.2 The second SHM design

Fig.3.34 shows the layout overview of the second SHM circuit. For this design, the RF rejection from the LO waveguide direction is accomplished by an one-section of step-impedance filter. At the IF output part, a two-section step-impedance filter is used to provide an open-circuit. To maximize the total performance of the SHM, all matching circuit at RF, LO, and IF ports are optimized simultaneously. Fig.3.34 also shows the fabricated crossbar diodes and the passive membrane circuit. Due to the lack of waveguide metallic housing, only predicted performance is shown.

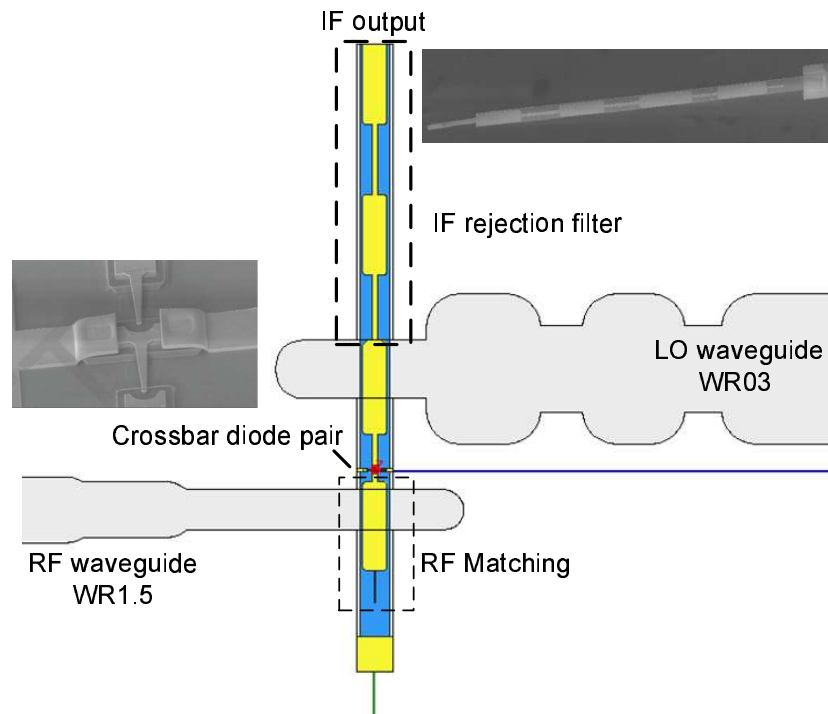


Figure 3.34: Layout overview of the second SHM design.

Fig.3.35 shows the SHM large-signal performance by sweeping LO power from -4 dBm to +4 dBm with an available RF power of -30 dBm. Fig.3.35(a) shows that with LO power levels larger than +2 dBm, the predicted minimum conversion loss is about 7-8 dB and coupled RF input power saturates at the same time. At those power levels, Fig.3.35(b) indicates that both LO and RF ports have 10 dB return loss. The corresponding simulated noise temperature is shown in Fig.3.35(c). The values is from 1116 K to 357 K for the LO power levels from +1 to 3.2 dBm.

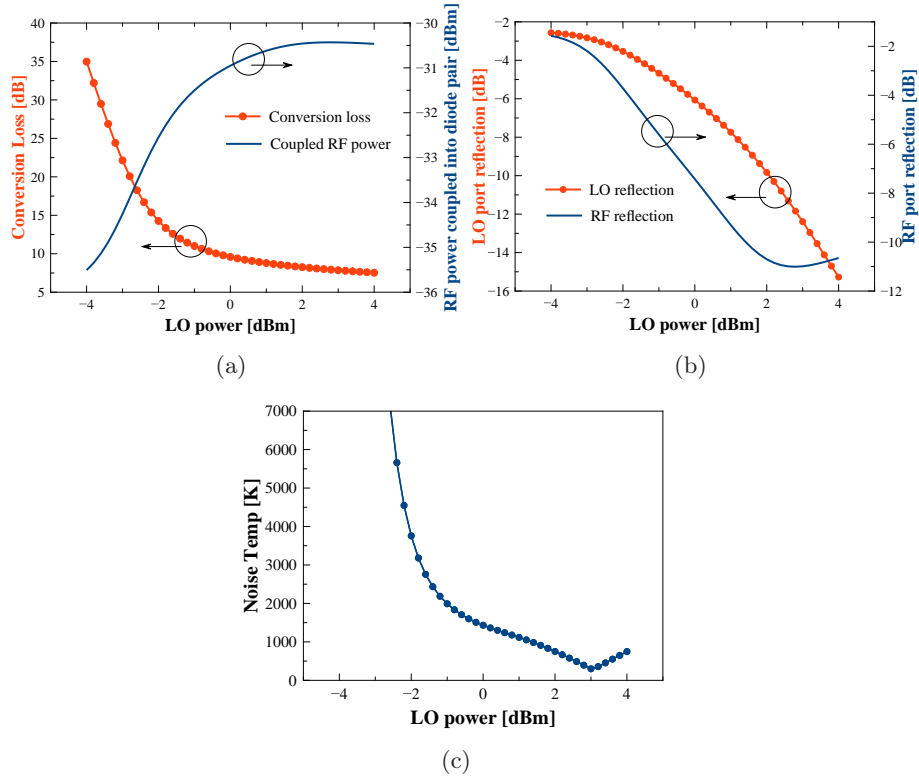


Figure 3.35: SHM performance by sweeping the LO power from -4 dBm to +4 dBm for a fixed RF_{freq} at 560 GHz and LO_{freq} at 283 GHz: (a) conversion loss and coupled RF power (b) reflection at RF& LO port (c) noise temperature.

The RF bandwidth of the second SHM with a fixed LO_{freq} at 283 GHz is shown in Fig.3.36. For different LO power levels from +2 to +4 dBm, the simulated conversion loss is better than 10 dB for a bandwidth of 110 GHz. The associated RF port return loss is better than 10 dB for the frequency range from 520 to 600 GHz.

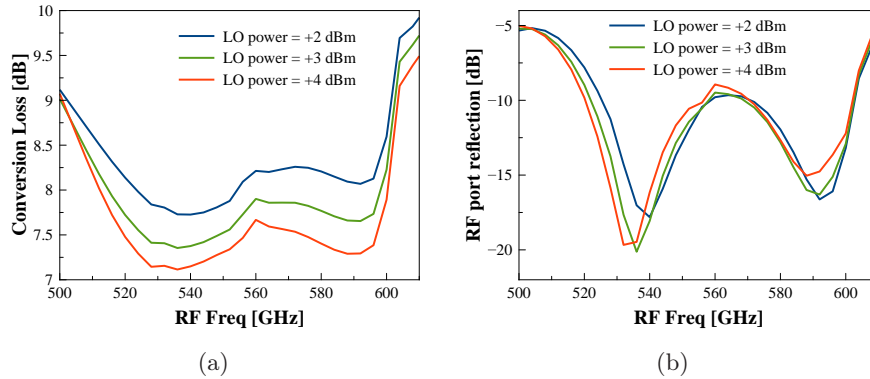


Figure 3.36: RF bandwidth performance with different LO input power from +2 to +4 dBm and a fixed LO_{freq} at 283 GHz: (a) conversion loss (b) RF port bandwidth.

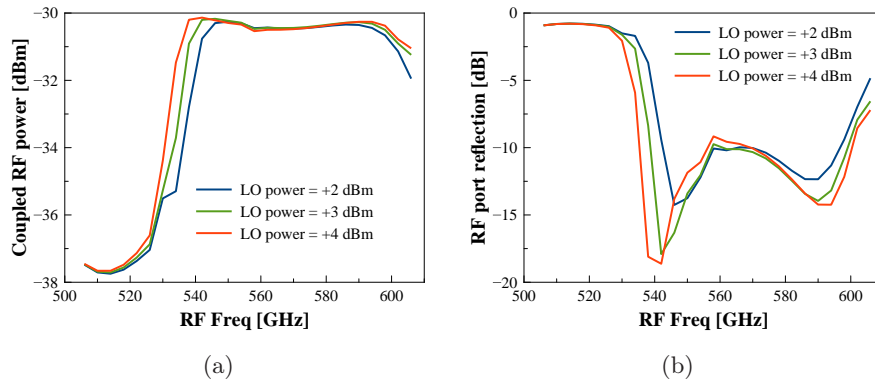


Figure 3.37: RF port responses by sweeping LO_{freq} from 250 to 300 GHz with different LO power levels from +2 to +4 dBm. IF_{freq} is fixed at 6 GHz and RF_{freq} is set to be the upper sideband signal at $2LO_{freq}+IF_{freq}$: (a) coupled RF input power (b) RF port reflection.

The LO port bandwidth is checked by sweeping the LO_{freq} from 250 to 300 GHz with a fixed IF_{freq} at 6 GHz. The RF signal is set at the

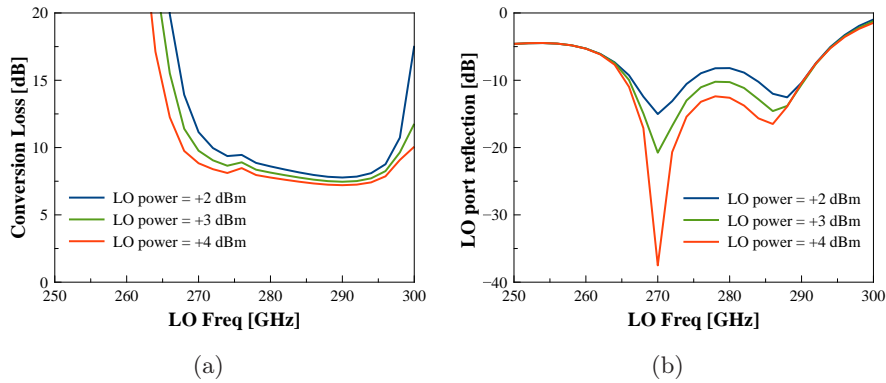


Figure 3.38: LO RF port responses by sweeping LO_{freq} from 250 to 300 GHz with different LO power levels from +2 to +4 dBm. IF_{freq} is fixed at 6 GHz and RF_{freq} is set to be the upper sideband signal at $2LO_{freq}+IF_{freq}$: (a) conversion loss (b) LO port reflection.

upper sideband: $2LO_{freq}+IF_{freq}$ with -30 dBm as well. For different LO pumping levels, the RF and LO port responses are summarized in Fig.3.37 and Fig.3.38. As shown in Fig.3.37, there is 0.5 dB power loss on the RF signal path and 65 GHz RF bandwidth for 10 dB return loss. Fig.3.38 indicates that the new design extends the 10 dB return loss bandwidth to 25 GHz at the LO port. And the conversion loss is below 10 dB for 35 GHz. Further increasing the bandwidth is possible by simplifying the two-section step-impedance filter at the IF region, but a large in band ripple is observed. The solution now is a good trade-off between the in band ripple and 10 dB return loss bandwidth.

3.10.3 Sensitivity analysis

Sensitivity analysis is performed to check the SHM design against fabrication tolerance. Statistical analysis based on the full-wave EM numerical simulation of the full waveguide mixer is not feasible. A fast estimation of the circuit performance is highly desirable. For this purpose, a comprehensive component library of waveguide, E-probe, and the step-impedance transitions is built. The simulation results from the circuit model of the second SHM are used to compare with the EM numerical results for full waveguide mixer. The good agreement, as shown in Fig.3.39, indicates that the circuit model is precise enough for further evaluation. Monte Carlo analysis is used together with the circuit model to perform statistical analysis.

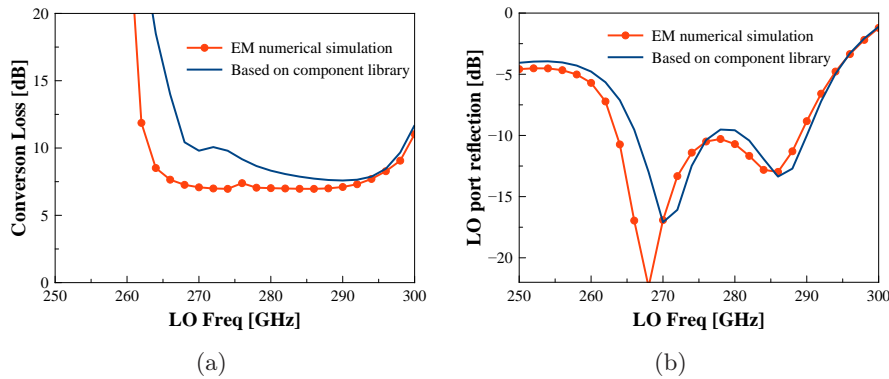


Figure 3.39: Comparison of circuit model and full-wave EM simulation results. The simulation conditions are the ones used in Fig.3.38 with LO pumping level of +3 dBm: (a) conversion loss (b) LO port reflection.

A total number of 2000 iterations were performed to analyze the influence from the fabrication tolerances. With a fixed IF_{freq} at 6 GHz and swept LO_{freq} from 250 to 300 GHz at a power level of +3 dBm, the associated conversion loss and LO port return loss are monitored for the statistical analysis. The tolerance of the waveguide structure including width, height and length is $\pm 10 \mu\text{m}$, the fabrication error of the passive circuit dimensions on the membrane is $\pm 4 \mu\text{m}$, and the impedance variation of the transmission line is $\pm 5 \Omega$. Fig.3.40(a, b) shows the collected conversion loss and return loss from 250 to 300 GHz. The histogram of conversion loss and return loss at a specific LO frequency of 282 GHz are shown in Fig.3.40(c, d) as well. The statistical results for a wide frequency range from 270 to 295 GHz in Fig.3.40(e, f) further confirm that the designed SHM has the highest probability for a conversion loss of 7.2-8.5 dB and LO return loss of 8-15 dB.

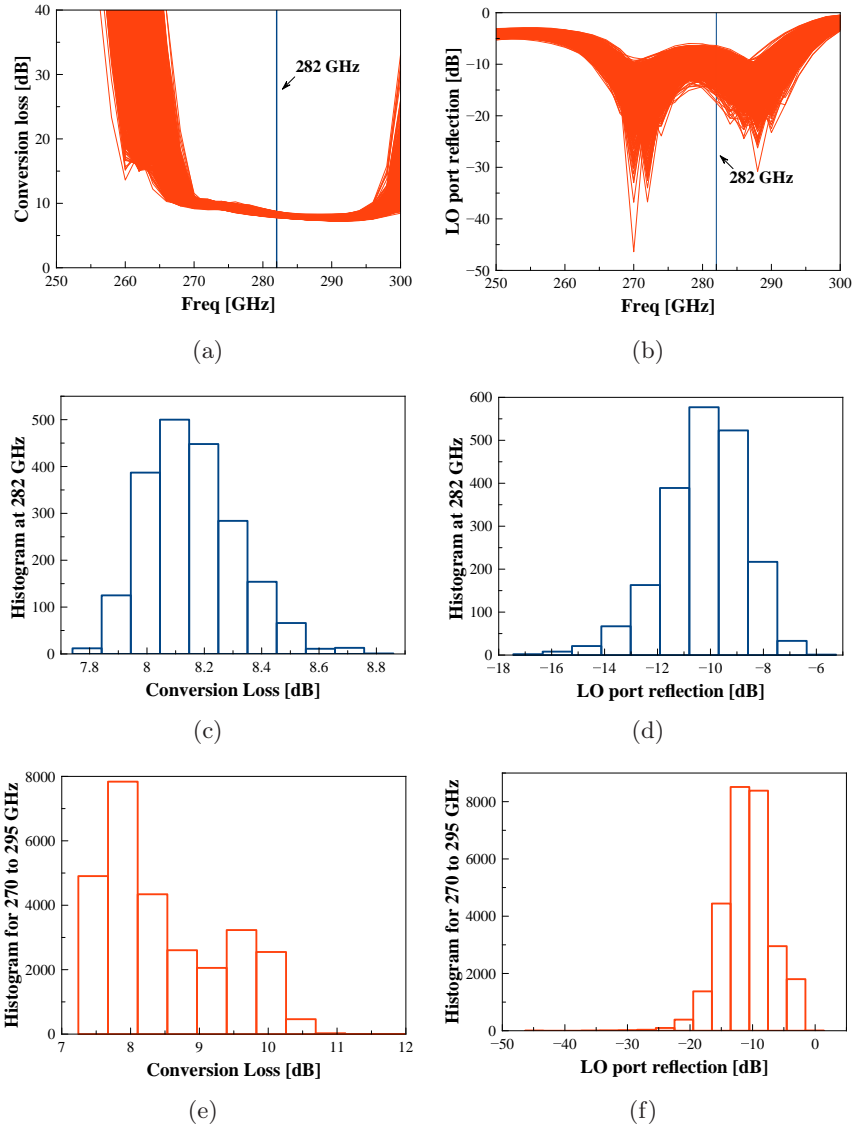


Figure 3.40: Histogram of conversion loss and associated LO port reflection for frequency range from 270 to 295 GHz: (a) collected conversion loss from 2000 iterations (b) collected LO port reflection from 2000 iterations (c) histogram of conversion loss at 282 GHz (d) histogram of LO port reflection at 282 GHz (e) histogram of conversion loss from 270 to 295GHz (f) histogram of LO port reflection from 270 to 295 GHz.

3.11 Tripler design

Fig.3.41 shows the layout overview of the tripler circuit. The tripler circuit can be divided into several key elements as indicated. Different patterns of probes were investigated for the largest bandwidth. As shown in Fig.3.41, the input matching circuit consists of tailored waveguide, capacitive E-probe and a two-section step impedance filter. This rejection filter provides a well defined impedance at the output frequency(third order harmonic). At the output side, the waveguide is integrated with a transformer to provide an inductive termination. This will shift the original position of the optimum source impedance as shown in Fig.3.42.

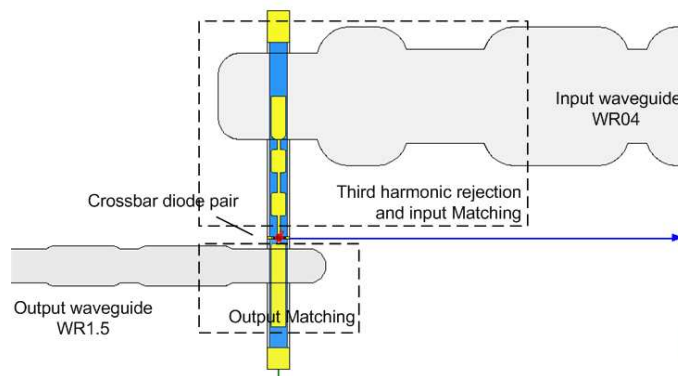


Figure 3.41: Tripler layout with non-biased crossbar diode pair configuration.

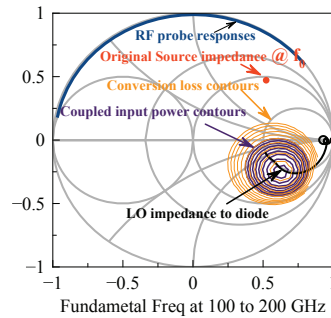


Figure 3.42: Tripler input matching responses. The output probe response is also shown. The markers indicate the original optimum source impedance at the beginning of the design procedure and the new impedance due to the inductive output probe.

Fig.3.43 shows tripler performance by sweeping power levels at the input frequency 190 GHz. As shown in Fig.3.43(a,b), the simulated conversion loss and port reflection saturates for the power from +3 to +5 dBm, with a minimum conversion loss of 11.7 dB. Fig.3.43(c) indicates the peak efficiency of 6.7 % at the input power level of +4 dBm. The power coupled efficiency in Fig.3.43(d) is defined as the ratio of power into the individual diode to the half of the input available power [27]. As shown, the power is equally distributed to the two diodes.

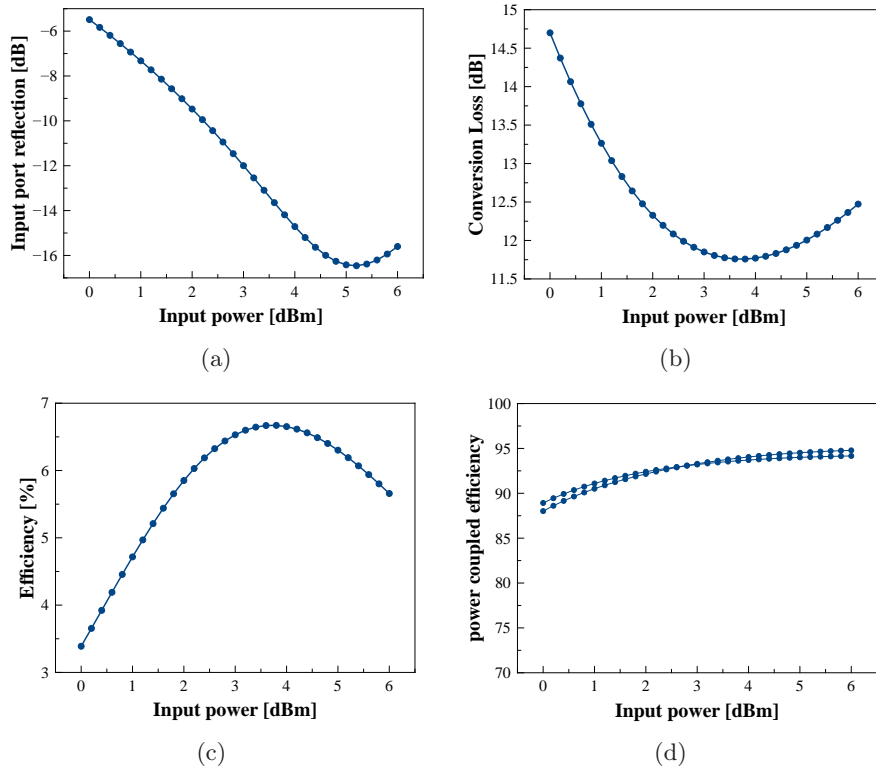


Figure 3.43: Tripler large-signal performance by sweeping the input power levels at a fixed input frequency at 190 GHz: (a) input reflection (b) conversion loss (c) efficiency (d) power coupled efficiency into each diode.

The bandwidth performance of the tripler by sweeping the input frequency from 120 to 220 GHz at different input power levels are summarized in Fig.3.44. As shown in Fig.3.44(a), the conversion loss achieves minimum values for the pumping levels from +2 to +6 dBm. The conversion loss

increases at lower power levels due to the degraded input power matching. Fig.3.44(b) shows that the input port has 30 GHz bandwidth for 10 dB return loss at the input power of +4 dBm. Fig.3.44(c) indicates that the designed tripler has a peak efficiency of 6-7 % for the input frequency range from 180 to 210 GHz. For the same frequency range, the third order harmonic suppression at input port is between 20-60 dB.

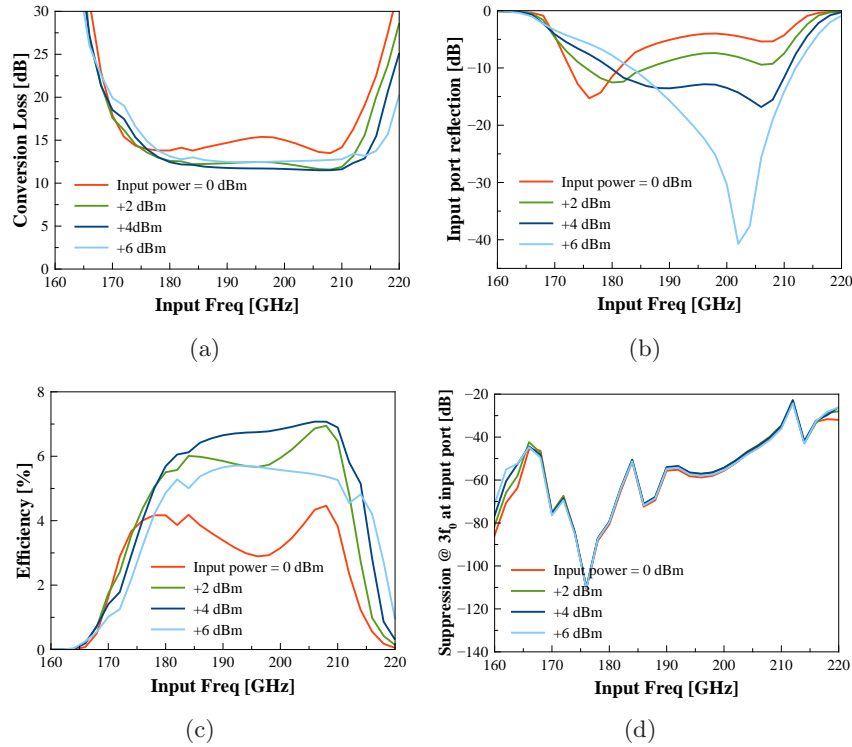


Figure 3.44: Tripler bandwidth performance by sweeping the input frequency from 120 to 220 GHz with the input power levels from 0 to +6 dBm: (a) conversion loss (b) input reflection (c) efficiency (d) third order harmonic suppression at the input port.

3.12 Summary

This chapter presents the detailed design methodology of SHM designs using a crossbar configuration. The content covers the discussion of the SHM configuration, propagation mode, power loss analysis for an uniform transmission line, the optimum impedance of the crossbar configuration, equivalent circuit models of the E-probes, rejection filter comparison, matching network design, and the complete SHM performance evaluations.

During this work, a parameterized 3D EM model is built into the full-wave 3D EM simulator, HFSS, to take the parasitics from the structures into account. A high local mesh density with volume mesh seeding is used to increase the simulation accuracy. The developed equivalent circuit models of capacitive and inductive E-probes are important for understanding of the impedance transformation due to the different probe patterns. The corresponding circuit models are utilized for the synthesis of matching circuit. The EM-circuit co-simulation routine is used to optimize the bandwidth and provides a fast way for statistical analysis of the full waveguide SHMs as well.

Two SHM designs are presented in this chapter. Different rejection strategy is considered for each design. The design with open stubs for signal rejection shows similar bandwidth as the other one with step-impedance filters. It seems that the lack of accurate circuit model of coupled stubs can be compensated by manipulating the LO input waveguides. On the other hand, the well modeled step-impedance filters provides extra optimization freedom. The designed SHM shows state-of-art performance as summarized in Table 3.3. With the input LO power levels from +2 to +4 dBm, LO port has 25 GHz bandwidth for 10 dB return loss and 35 GHz bandwidth for conversion loss below 10 dB. The associated RF bandwidth is more than 110 GHz. The simulated noise temperature with ADS diode model is well below 1000 K.

A tripler based on the crossbar configuration is designed for generating RF signal for testing SHM. The wideband performance is achieved by optimizing rejection filter, E-probes and input waveguides all together. The simulated tripler shows 10 dB input return loss from 180 to 210 GHz at the input power of +4 dBm. The predicted conversion loss and efficiency for the corresponding frequency range is 11-12 dB and 6-7 %. Table 3.4 summarizes the state of art tripler performance for different frequency bands.

Configuration	Freq [GHz]	CL [dB]	N_T [K]	Ref
Antiparallel SHM	370-390	10.5-12	<6000	[41]
Antiparallel SHM	330-345	7	<1000	[14]
Antiparallel SHM	380	14	NA	[20]
Antiparallel SHM	320-360	10-11	3400	[17]
Antiparallel SHM	320-360	6-14	<3500	[32]
Antiparallel SHM	300-360	6-7	<1000	[2]
Crossbar SHM	520-600	7	<2360	[42]
Crossbar SHM	830-900	10-12	5000-6000	[4]
Crossbar FBM	520-590	<9	<4000	[13]
Crossbar SHM	520-590	<14	3000-4000	[5]
Crossbar SHM	500-610	<10	<1200	This work

Table 3.3: Summary of SHM performance for both antiparallel and crossbar configuration from the open literatures. SHM: Sub-Harmonic Mixer, CL: Conversion Loss, FBM: Fundamental Balanced Mixer, N_T : Noise Temperature.

Configuration	Anodes	Freq [THz]	Peak Efficiency [%]	Ref
Crossbar	12	0.26-0.34	11(300K)	[23]
Crossbar	4	0.54-0.64	12(120K)	[27]
Crossbar	2	1.6-1.7	3(120K)	[24]
Crossbar	2	1.7-1.9	1(120K)	[24]
Crossbar	2	0.54-0.63	<7(300K)	This work

Table 3.4: Summary of tripler performance from the open literatures. Comparison is given in term of circuit topology, number of anodes, output frequency range, and peak efficiency.

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Chapter 4

Physical Schottky Diode Model

4.1 Introduction

To have a more accurate estimation on the designed SHM, a physical Schottky diode model is built based on the anode radius a , effective Ohmic contact radius b , doping level of both epitaxial(EPI) and substrate(SUB) layers N_{epi} and N_{sub} , thickness of both layers T_{epi} and T_{sub} , barrier height ϕ_b , specific contact resistivity ρ , and device temperature T . This work is a part of an effort to establish an accurate circuit model of a Schottky diode based on its physical parameters. The advantage of using a physical diode model is that the non-ideal features such as electron velocity saturation due to high electric field, barrier height lowering due to image force, and excessive noise due to hot-electrons can be included. Furthermore, with a physical device model, circuit designers can see the influence on the circuit performance due to the different fabrication parameters such as area, doping profile, and layer thickness. Those parameters are often used to optimize the Schottky diode characteristics for some specific applications such as mixers or multipliers [1, 2].

4.2 Model implementation

Fig.4.1 shows a cross sectional view of a planar Schottky-barrier diode. Metal-semiconductor contact is formed on top of a lightly doped EPI layer. A highly doped SUB layer with low resistance is used to form the Ohmic contact. Modulation on depletion region plays a key role in mixer and multiplier operations. Corresponding to its vertical structure, Fig.4.1 also shows

an equivalent circuit model of the diode. It includes two parts: 1) a junction which is represented by a parallel network with nonlinear conductance and capacitance 2) series impedance which represents the contributions from undepleted EPI layer, SUB layer, and Ohmic contact.

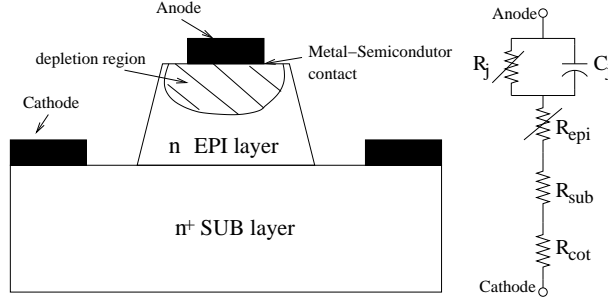


Figure 4.1: Cross-section of the diode structure. The equivalent circuit model is also shown.

4.2.1 Depletion layer and junction capacitance

The variation of depletion width is crucial for the analysis of diode, because the most important diode properties such as conductance, capacitance, and resistance are all dependent on the depletion width. The depletion width w_{epi} of the contact is shown in Fig.4.2. With the knowledge of physical doping level and bias voltage, an approximation of the depletion width can be calculated by

$$w_{epi} = \sqrt{\frac{2\epsilon}{qN_{epi}}(V_{bi} - V_j - V_T)} \quad (4.1)$$

where N_{epi} is the defined doping level of the EPI layer, V_j is the applied voltage on the diode junction, V_T is the thermal voltage, ϵ is the permittivity of GaAs material. V_{bi} represents the built-in potential of the junction, and it is calculated from the barrier height ϕ_b and ξ . The latter is the potential difference between bottom of the conduction band E_C and Fermi level E_F on semiconductor side, as indicated in Fig.4.2. With the uniform doping profile within the EPI layer, the space charge in the depletion region increases linearly, and the maximum electric field at the metal-semiconductor interface can be formulated as

$$E_{max} = \frac{qN_{epi}}{\epsilon}w_{epi} \quad (4.2)$$

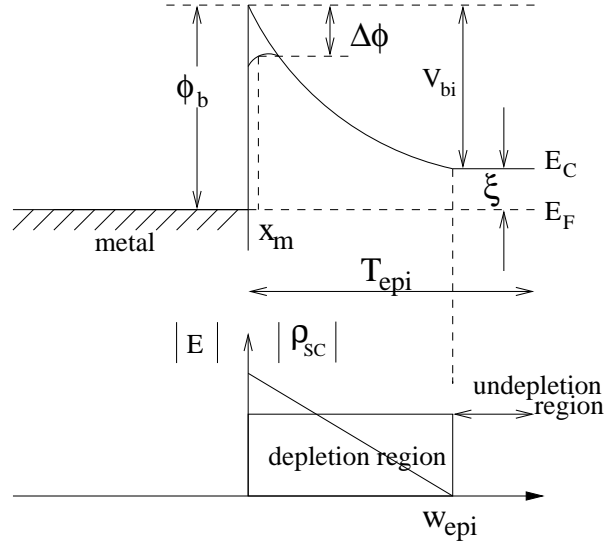


Figure 4.2: Energy diagram of Schottky contact. The magnitude of space charge and electric field are also shown. E_C is bottom of the conduction band, E_F is the Fermi level in the semiconductor side, V_{bi} is the junction built-in potential, ϕ_b is the barrier height, $\Delta\phi$ is the barrier height lowering due to the image force, T_{epi} is the total EPI layer thickness, w_{epi} is EPI depletion width. E is the electric field in the depletion region, ρ_{sc} is the space charge density.

Eq.4.1 indicates that the depletion width w_{epi} approaching zero when the junction voltage V_j reaches $V_{bi} - V_T$, but there is always a physical thin layer remaining and can be characterized by the Debye-length,

$$L_D = \sqrt{\frac{\epsilon k_B T}{N_{epi} q^2}} \quad (4.3)$$

where k_B is Boltzmann's constant, T is the device temperature. When the diode is reversely biased, Eq.4.1 remains valid until the punch through voltage V_p is reached where the EPI layer is completely depleted. With the condition of $w_{epi} = T_{epi}$, punch through voltage can be solved from Eq.4.1 to be:

$$V_p = V_{bi} - V_T - \frac{q N_{epi} T_{epi}^2}{2\epsilon} \quad (4.4)$$

When voltage is further increased in reverse situation, a very thin SUB layer will also be depleted due to its high doping profile. This depletion

width can be calculated as

$$w_{sub} = \begin{cases} 0 & V_j \geq V_p \\ \sqrt{\frac{2\varepsilon}{qN_{sub}}(V_p - V_j)} & V_j < V_p \end{cases} \quad (4.5)$$

The total depletion width of a Schottky diode is expressed as $w_{tot} = w_{epi} + w_{sub}$. With the knowledge of depletion width and anode area, total space charge can be formulated as

$$Q_{SC} = Q_{SC,epi} + Q_{SC,sub} = (qN_{epi}w_{epi} + qN_{sub}w_{sub})A \quad (4.6)$$

Therefore, junction capacitance from both layers can be expressed from their derivatives toward junction voltage

$$C_{epi} = \left| \frac{dQ_{SC,epi}}{dV_j} \right| = \frac{qN_{epi}d(w_{epi})}{dV_j} = \frac{\varepsilon}{w_{epi}}A \quad (4.7)$$

$$C_{sub} = \left| \frac{dQ_{SC,sub}}{dV_j} \right| = \frac{qN_{sub}d(w_{sub})}{dV_j} = \frac{\varepsilon}{w_{sub}}A \quad (4.8)$$

Capacitors from both EPI and SUB layers are in series when junction voltage V_j is smaller than punch through voltage V_p , and the value of total capacitance is

$$\frac{1}{C_{tot}} = \frac{1}{C_{epi}} + \frac{1}{C_{sub}} \Rightarrow C_{tot} = \frac{\varepsilon}{w_{epi} + w_{sub}}A \quad (4.9)$$

It is worth to mention that to make the circuit simulator easier to converge, it is important to have a higher order continuous function of depletion width w_{tot} versus junction voltage V_j . Both Eq.4.7 and Eq.4.8 indicate that junction capacitance is proportional $\sim \frac{dw}{dV_j}$ and higher order continuous function of $w_{tot}(V_j)$ is always preferred. To avoid the singularity in the calculated junction capacitance, the simple switching sentence in the case of w_{epi} approaching L_D has to be replaced by a five order polynomial equation to ensure a smooth transition [3]:

$$w_{tot} = \begin{cases} T_{epi} + w_{sub} & \text{for } V_p \geq V_j \\ w_{epi} & \text{for } V_0 \geq V_j > V_p \\ P(V) & \text{for } V_m \geq V_j > V_0 \\ L_D & \text{for } V_j > V_m \end{cases} \quad (4.10)$$

where

$$P(V) = a + b(V - V_0) + c(V - V_0)^2 + d(V - V_0)^3 + e(V - V_0)^4 + f(V - V_0)^5 \quad (4.11)$$

$V_0 = (V_{bi} - 3V_T)$ and $V_m = (V_{bi} - V_T)$ is the lower and upper boundary of the transition region, respectively. The relevant coefficients of $P(V)$ can be calculated by boundary conditions listed in Eq.4.12:

$$P(V_0) = w_{epi}(V_0) \quad (4.12a)$$

$$P(V_m) = L_D \quad (4.12b)$$

$$\left. \frac{dP(V)}{dV} \right|_{V=V_0} = \left. \frac{dw_{epi}(V_j)}{dV_j} \right|_{V=V_0} \quad (4.12c)$$

$$\left. \frac{d^2P(V)}{dV^2} \right|_{V=V_0} = \left. \frac{d^2w_{epi}(V_j)}{dV_j^2} \right|_{V=V_0} \quad (4.12d)$$

$$\left. \frac{dP(V)}{dV} \right|_{V=V_m} = 0 \quad (4.12e)$$

$$\left. \frac{d^2P(V)}{dV^2} \right|_{V=V_m} = 0 \quad (4.12f)$$

The corresponding solution of each coefficients is formulated as:

$$a = w_{epi}(V_0) \quad (4.13a)$$

$$b = w'_{epi}(V_0) \quad (4.13b)$$

$$c = \frac{1}{2}w''_{epi}(V_0) \quad (4.13c)$$

$$d = -\frac{10a + 6bh + 3ch^2 - 10L_D}{h^3} \quad (4.13d)$$

$$e = \frac{15a + 8bh + 3ch^2 - 15L_D}{h^4} \quad (4.13e)$$

$$d = -\frac{6a + 3bh + ch^2 - 6L_D}{h^5} \quad (4.13f)$$

where h is equal to $V_m - V_0$ and represents the transition length. Fig.4.3 shows the relationship of space charge and capacitance versus junction voltage. For reverse bias region, depletion width increases. Beyond the punch through voltage, derivative of charge toward junction voltage becomes small and junction capacitance can be roughly estimated by $\epsilon A/T_{epi}$. On the other hand, forward bias voltage reduces the depletion width and increases the junction capacitance. With continuously increasing forward voltage, w_{epi} has a smooth transition to L_D , and the associated capacitance reduces to zero softly.

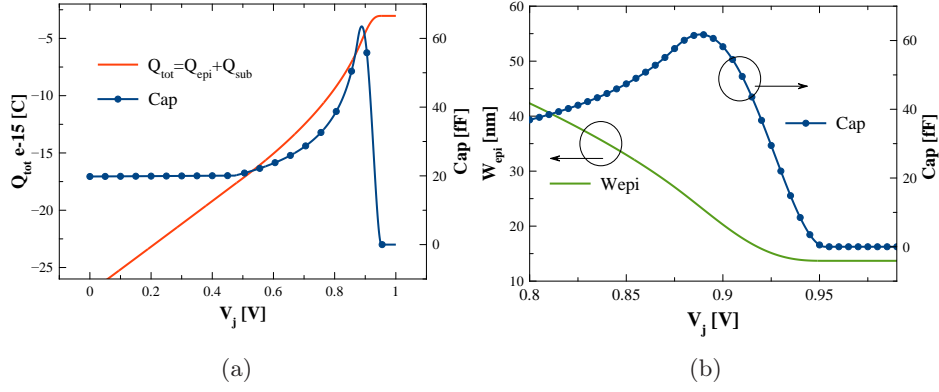


Figure 4.3: (a) Calculated total charge Q_{tot} and capacitance C_{tot} in EPI and SUB layers for different junction voltages V_j . (b) depletion width of EPI layer w_{epi} under large forward bias. Calculation is based on the assumed values of $T_P=300$ K, $V_T=0.025$ V, $N_{epi}=1e23$ m^{-3} , $N_{sub}=4e24$ m^{-3} , $T_{epi}=80$ nm, $T_{sub}=5$ μm , $a=2.1$ μm , $Area=13.8$ μm^2 .

4.2.2 Series Impedance

As shown in Fig.4.1, series impedance of a diode is divided into three parts: 1) nonlinear impedance from the undepleted EPI layer due to the voltage dependency of w_{epi} 2) a small DC resistance from SUB layer due to its high doping profile. AC impedance due to current spreading and skin depth effects plays an important role for high frequency applications and should also be included 3) resistance from the Ohmic contact.

EPI layer resistance DC resistance from EPI layer is proportional to the undepleted width and can be formulated as

$$Z_{epi} = \frac{T_{epi} - w_{epi}}{\sigma_{epi} A} \quad (4.14)$$

where $A = \pi a^2$ is the area of the anode; T_{EPI} and w_{EPI} represents total EPI layer thickness and depletion width, respectively; σ_{epi} is the conductivity of the EPI layer, which can be calculated from its doping level N_{epi} and electron velocity v_{epi} or mobility μ_{epi}

$$\sigma_{EPI} = qN_{epi}v_{epi} = qN_{epi}\mu_{epi}(E)E \quad (4.15)$$

Eq.4.14 indicates that zero-bias DC resistance from EPI layer can be mini-

mized by carefully choosing T_{EPI} [1]:

$$T_{epi} = \sqrt{\frac{2\varepsilon}{qN_{epi}}(V_{bi} - V_j - V_T)} \Big|_{V_j=0} \quad (4.16)$$

Both Eq.4.14 and Eq.4.15 indicate that Z_{epi} has a bias dependency. The first order effect comes from the voltage controlled depletion width w_{epi} , and the second order effect arises due to the saturated electron velocity of GaAs materials under a strong electric field. This can be explained by intervalley scattering effect. As the electric field increases, electron energy increases and electrons can scatter into the upper valley, where the larger effective electron mass results a lower mobility [4]. To decide the mobility of electrons in EPI layer under different bias conditions, electric field information can be calculated by using current flowing through the junction, diode area, and low field mobility as an initial guess: $I/(AqN_{epi}\mu_{epi0})$ [5]. The calculated mobility due to its field dependency will affect the total current again. It can be imagined that accuracy of the simulation results at large forward conditions(close to flat band) will be heavily influenced by the reduced mobility and increased impedance from EPI layer.

SUB layer resistance: DC resistance from the substrate layer is generally much lower than EPI layer due to its higher doping levels. The associated value does not have a strong bias dependency and should be considered as a linear component. The calculation of its value is similar to Eq.4.14 except that the corresponding width and conductivity of SUB layer should be used instead.

Apart from the DC resistance from SUB layer, AC impedance Z_{sp} and Z_{skin} from the spreading and skin effect of the substrate layer should also be correctly modeled. The closed form of it is derived in [6],

$$Z_{sp} + Z_{skin} = \frac{1}{2\pi\sigma_{sub}a} \tan^{-1}\left(\frac{b}{a}\right) + \frac{1+j}{2\pi\sigma_{sub}\delta_{sub}} \ln\left(\frac{b}{a}\right) \quad (4.17)$$

where $\delta_{sub} = \sqrt{\frac{2}{\omega\mu_0\sigma_{sub}}}$ represents the skin depth of the substrate material. Furthermore, when frequencies are larger than 1 THz, effect of displacement current (C_{dis}) and charge carrier inertia (L_{ine}) from both EPI and SUB layers become important [7]. To characterize these two effects, an equivalent circuit model can be employed as shown in Fig.4.4.

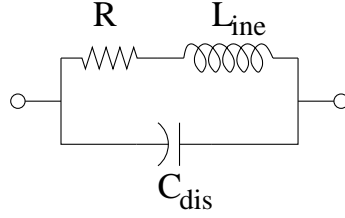


Figure 4.4: The effect of displacement current and charge carrier inertia are taken into account by a parallel network with a capacitance of C_{dis} and an inductance of L_{ine} . R is the DC resistance from EPI or SUB layer.

The total impedance of this resonance network can be expressed as,

$$Z = R \frac{1 + j\omega L_{ine}/R}{1 - \omega^2 L_{ine} C_{dis} + j\omega C_{dis} R} = R \frac{1 + j\omega/\omega_s}{1 - \omega^2/(\omega_s \omega_d) + j\omega/\omega_d} \quad (4.18)$$

where R is the DC resistance, ω_s , ω_d , and ω_p is mean scattering, dielectric relaxation, and plasma frequency of GaAs material. The relationship of them with circuit components can be established as

$$1/\omega_s = L_{ine}/R = m^* \mu/q \quad (4.19a)$$

$$1/\omega_d = C_{dis} R = \epsilon/(qN_D \mu) \quad (4.19b)$$

$$1/\omega_p^2 = 1/(\omega_s \omega_d) \quad (4.19c)$$

where m^* is the effective electron mass and ϵ is the permittivity of the GaAs material. The total impedance from Eq.4.18 can be re-formulated by replacing R with a general resistance expression $l/(A\sigma)$, where l is the length of a semiconductor material, A is its cross-section area, and σ is its static conductivity:

$$Z = \frac{l}{A} \frac{1}{\sigma} \frac{1 + j\omega/\omega_s}{1 - \omega^2/(\omega_s \omega_d) + j\omega/\omega_d} = \frac{l}{A} \frac{1}{\sigma \left(\frac{1}{1 + j\frac{\omega}{\omega_s}} + j\frac{\omega}{\omega_d} \right)} \quad (4.20)$$

The right hand side of Eq.4.20 indicates that the effect of displacement current and charge carrier inertia in EPI and SUB layers can be taken into account by simply considering that the conductivity has a frequency depen-

dency.

$$\sigma_{epi0} \left(\frac{1}{1 + j \frac{\omega}{\omega_{s,epi}}} + j \frac{\omega}{\omega_{d,epi}} \right) \quad (4.21a)$$

$$\sigma_{sub0} \left(\frac{1}{1 + j \frac{\omega}{\omega_{s,sub}}} + j \frac{\omega}{\omega_{d,sub}} \right) \quad (4.21b)$$

By inserting Eq.4.21 into Eq.4.14 and Eq.4.17, AC impedance from the EPI layer and SUB layer can be accurately modeled. Fig.4.5 shows a total impedance arising from EPI and SUB layers. At the corresponding plasma frequencies for each layer, the parallel resonance network presents the peak of real part of impedance.

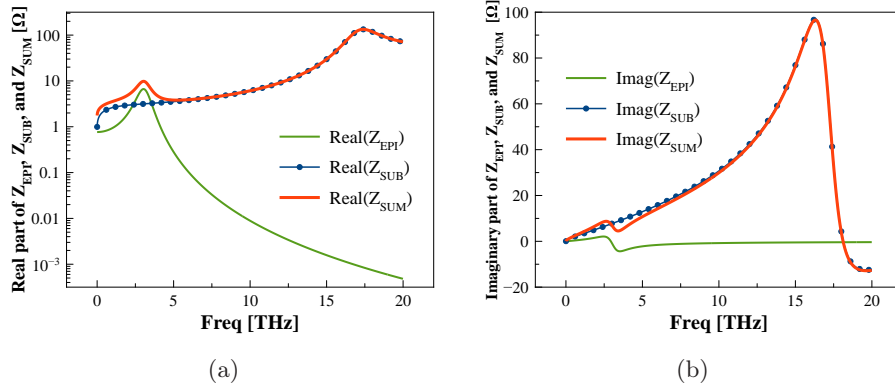


Figure 4.5: Calculated real and imaginary part of impedance from Z_{EPI} , Z_{SUB} , and Z_{SUM} . AC conductivity of the EPI and SUB layer are considered by Eq.4.21. The total impedance is calculated as $Z_{SUM} = Z_{EPI} + Z_{SUB}$. The calculation procedure are based on the assumed values of $T_P=300$ K, $V_T=0.025$ V, $N_{epi}=1e23$ m^{-3} , $N_{sub}=3e24$ m^{-3} , $\mu_{epi}=4123$ cm^2/Vs , $\mu_{sub}=2068$ cm^2/Vs , $\omega_{s,epi}=6.78e+12$ rad/s, $\omega_{d,epi}=5.69e+13$ rad/s, $\omega_{s,sub}=1.36e+13$ rad/s, and $\omega_{d,sub}=8.57e+14$ rad/s, $\epsilon=1.16e-10$ F/m.

Ohmic contact: Ohmic contact is formed similarly as Schottky contact but with much higher doping level semiconductor material, and the purpose is to avoid significant voltage drop. Current transportation mechanism is dominated by the tunneling effect. The corresponding circuit parameter is

specific contact resistivity:

$$\rho = \left(\frac{dJ}{dV} \right)^{-1} \Big|_{V=0} \quad (4.22)$$

The total resistance from the Ohmic contact of the diode is formulated as

$$Z_C = \frac{\rho}{\pi b^2} \quad (4.23)$$

where b is the radius of Ohmic contact.

4.2.3 Current transport

The current transport mechanism can be divided into three components: field emission, thermionic field emission, and thermionic emission-diffusion. The field emission is due to highly doped semiconductor or low temperature of devices, electrons at the Fermi level tunnel through the barrier directly. The second mechanism is due to the thermally excited electrons at a energy level where the barrier is thinner and probability of tunneling higher. The last mechanism is due to the electrons thermally excited with enough energy to overcome the barrier. The last one is discussed in this section, for the model implementation, tunneling currents from the first two mechanisms are calculated based on the discussions in [8–10].

Thermionic emission/diffusion theory

The effects of diffusion and thermionic emission of electrons are essentially in series. In practice, the true behavior lies somewhere between the two extremes [10]. The total current density flowing through the junction is formulated as,

$$J_{TE/D} = qN_C \exp\left(-\frac{\phi_b - \Delta\phi}{V_T}\right) \exp\left(\frac{V_j}{V_T} - 1\right) \frac{v_r}{1 + \frac{v_r}{v_d}} \quad (4.24)$$

where N_C is density of state in the conduction band, ϕ_b is the barrier height, and $\Delta\phi$ is the barrier height lowering due to the image force. Depending on the ratio of recombination velocity v_r and diffusion velocity v_d , the different current transfer mechanism applies. Eq.4.24 indicates that the thermal emission applies when $v_r \ll v_d$, however drift and diffusion current mechanism dominates when $v_r \gg v_d$.

The recombination velocity v_r of electrons is expressed as [11],

$$v_r = \frac{v_{drift}}{2} \left[1 + erf\left(\frac{v_{drift}}{v_{r0}}\right) \right] + \frac{v_{r0}}{2} \exp\left(-\frac{v_{drift}^2}{v_{r0}}\right) \quad (4.25)$$

where erf is the error function and v_{r0} is the surface recombination velocity of electron under zero bias condition. Its value depends on the temperature T and effective electron mass m^* ,

$$v_{r0} = \sqrt{\frac{2k_B T}{m^* \pi}}$$

The diffusion velocity is formulated as [10],

$$v_d = \left[\frac{q}{\mu K T} \exp(-\phi_b/V_T) \int_0^{w_{epi}} \exp(E_C/V_T) dx \right]^{-1} \quad (4.26)$$

where the conduction band energy potential E_C can be derived from Fig.4.2:

$$E_C = \phi_b + \frac{qN_d}{2\epsilon}(x^2 - 2w_{epi}x) \quad (4.27)$$

Image force

The generated electric field by an electron in a dielectric at a distance of x from the metal is same as if there is an image positive charge located at the same distance x within the metal. The barrier height lowering due to the image force is illustrated in Fig.4.2.

The barrier height has its maximum when image force and electric force due to the induced space charge is equal [4, 10]:

$$\frac{q}{16\pi\epsilon x^2} \simeq E_{\max} \quad (4.28)$$

The depletion width x_m at the barrier peak can be solved from Eq.4.28,

$$x_m = \sqrt{\frac{q}{16\pi\epsilon E_{\max}}} \quad (4.29)$$

The reduced barrier height then can be characterized by

$$\Delta\phi = 2E_{\max}x_m = \sqrt{\frac{qE_{\max}}{4\pi\epsilon}} = \sqrt{\frac{q}{4\pi\epsilon}} \sqrt{\frac{qN_{epi}}{\epsilon} w_{epi}} =$$

$$= \sqrt{\frac{q^2 N_{epi}}{4\pi\epsilon^2} \sqrt{\frac{2\epsilon}{qN_{epi}}(V_{bi} - V_j - V_T)}} = \sqrt[4]{\frac{q^3 N_{epi}}{8\pi^2\epsilon^3}(V_{bi} - V_j - V_T)} \quad (4.30)$$

where maximum electric field E_{max} and depletion width w_{epi} are inserted by using Eq.4.2 and Eq.4.1. Eq.4.30 indicates the barrier lowering is proportional to $\sim (N_{epi}(V_{bi} - V_j))^{0.25}$. For a practical diode, the influence of doping levels and bias dependency on barrier height lowering is shown in Fig.4.8(a). For low forward bias region, the barrier height lowering can be described by

$$\Delta\phi = \Delta\phi_0 - \beta V_j \quad (4.31)$$

where β is the slope.

The physical diode model has no ideality factor N_f , however this parameter is often extracted from measured IV characteristics. And it is also used in the theoretical calculation of conversion loss for both the SHM and resistive multiplier. It would be good to understand the physical meaning behind this parameter. By inserting Eq.4.31, diode current from Eq.4.24 can be expressed in a form

$$J_{TE/D} \simeq Const \times \exp\left(\frac{(1-\beta)V_j}{V_T}\right) = Const \times \exp\left(\frac{V_j}{N_f V_T}\right) \quad (4.32)$$

where the constant term is

$$Const = qN_C \frac{v_r}{1 + \frac{v_r}{v_d}} \exp\left(-\frac{\phi_b - \Delta\phi_0}{V_T}\right)$$

and N_f is introduced as the ideality factor [10]. By assuming the constant term has no bias dependence, the ideal factor is then derived from Eq.4.32 to be

$$\frac{1}{N_f} = 1 - \beta \quad (4.33)$$

The right side of equation above can be further extended by using Eq.4.30,

$$\frac{1}{N_f} = 1 - \frac{d\Delta\phi}{dV_j} = 1 - \frac{1}{4} \sqrt[4]{\frac{q^3 N_{epi}}{8\pi^2\epsilon^3}} (V_{bi} - V_j - V_T)^{-\frac{3}{4}} \quad (4.34)$$

Eq.4.34 indicates that large doping level results in a large ideality factor. Fig.4.8(b) shows calculated ideality factors for two different doping levels. The trends follows the prediction from Eq.4.34. .

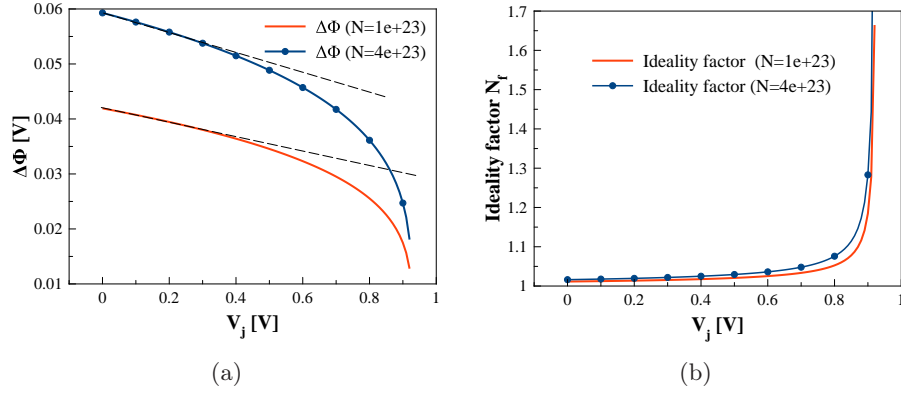


Figure 4.6: (a) Barrier height lowering $\Delta\phi$ with different junction voltages V_j and doping levels (b) the corresponding ideality factor N_f . Calculation is based on the assumed values of $T_P=300$ K, $V_T=25$ mV, $N_{epi}=1e+23$ m^{-3} , $V_{bi}=0.953$ V, $\epsilon=1.16e-10$ F/m. It is also assumed that the dependency of V_{bi} on N_{epi} is weak and can be ignored.

4.2.4 Noise

The noise sources within the Schottky diode arise from three sources: 1) thermal noise $\langle v^2 \rangle = 4k_B T R_{s,tot} \Delta f$ due to series resistance from un-depleted EPI layer, SUB layer, and Ohmic contact 2) shot noise $\langle i^2 \rangle = 2qI\Delta f$ from conduction current through the junction 3) excessive noise from hot-electrons. The derivation of hot-electron noise arises from electron energy and momentum balance equations [12]:

$$\frac{d\zeta}{dt} = eEv - (\zeta - \zeta_0)/\tau_d \quad (4.35a)$$

$$\frac{d(m^*v)}{dt} = eE - m^*v/\tau_s \quad (4.35b)$$

$$\zeta = \frac{3}{2}k_B T_e \quad (4.35c)$$

where ζ is the average electron energy for the electric field applied, ζ_0 is for electron energy without field. The average electron velocity is represented by v . τ_s and τ_d is the mean scattering and energy relaxation time for GaAs material, which are defined by Eq.4.19(a) and Eq.4.19(b). m^* is the effective electron mass. By setting time derivative to zero, the equivalent noise temperature from the coupled steady state equations can be solved as

$$T_e = T_0 + [(2q^2\tau_s\tau_d E^2)/3k_B m^*] \quad (4.36)$$

By inserting E field calculated from diode current $E = I/(Area \times q \times N_{EPI} \times \mu_{epi})$ and $\tau_s = m^* \mu_{epi}/q$ from Eq.4.19(a), T_e versus junction current can be formulated as:

$$T_e = T_0 + K_h I^2 \quad (4.37)$$

where

$$K_h = \frac{2\tau_d}{3qk_B\mu_{epi}N_{epi}^2A^2}$$

It can be seen that the excessive noise is from the second term, which has $\sim I^2$ relationship with the junction current. The discussion of Eq.4.37 in [12] uses an assumed value of τ_d (1 ps), however, the direct calculation based on $\epsilon/(qN_{epi}\mu(E))$ from Eq.4.19(b) shows a much smaller value. The comparison of noise temperature based on assumed and calculated τ_d is shown in Fig.4.7. The dramatic difference indicates that the final noise measurement has to be fitted with a factor to correctly characterize the slope of noise temperature. Once the technology settles down, this parameter should not show big difference between devices.

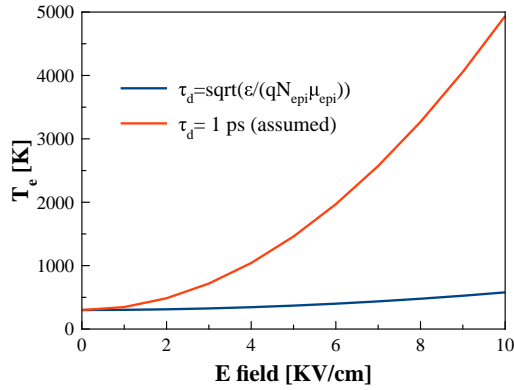


Figure 4.7: Calculated equivalent noise temperature with different τ_d : one with assumed 1ps, the other is calculated based on Eq.4.19(b). The parameters used in the calculation are $T_P=300$ K, $V_T=0.025$ V, $N_{epi}=2e+22$ m^{-3} , $\tau_s=2.3e-13$ s from Eq.4.19(a), $\tau_d=6.04e-14$ s from Eq.4.19(b), $\epsilon=1.16e-10$ F/m, $\mu_{epi}=6000.0$ cm^2/Vs , $m^* = 0.068m_0$, and m_0 is electron mass with $9.1e-31$ kg.

4.3 Model verification

To verify the model based on the physical defined parameters, I-V and C-V characteristics for a specific diode from Chalmers are used for comparison. Due to the reason that experimental data of noise behavior is not available, the simulated noise temperatures from physical diode models are compared with the results found from open literatures.

With the detailed knowledge of Chalmers Schottky technology, and the relevant diode parameters are set to be $T_P=300$ K, $a=0.5 \mu m$, $b=23.9 \mu m$, barrier height $\phi_b=1.02$ V, $N_{epi}=5e+23 m^{-3}$, $N_{epi}=5e+24 m^{-3}$, $T_{epi}=48 nm$, $T_{sub}=2 \mu m$, and resistivity of Ohmic contact $\rho=5e-9 \Omega m^2$. Even though the measurement data is quite old compared to the technology developed until today, this preliminary comparison shows that the model works well.

Fig.4.8 shows the I-V characteristics of two diodes with different anode areas. The surface leakage for low forward bias region ≤ 0.4 V is modeled by a parallel resistor of $R_p=330 M\Omega$ for both diodes. As shown, there is a good agreement between the measurement and simulation results. Fig.4.9 shows the junction capacitance versus voltage. The extracted capacitance data is not valid for larger bias points, and for reverse bias region the diode model predicts a 30 % lower capacitance than the measurement. This error might be due to a parasitic capacitance or originate from the extraction procedure where the pad-pad capacitance are de-embedded. Therefore, an extra overlapping capacitance of 0.7 fF is added to the physical diode model

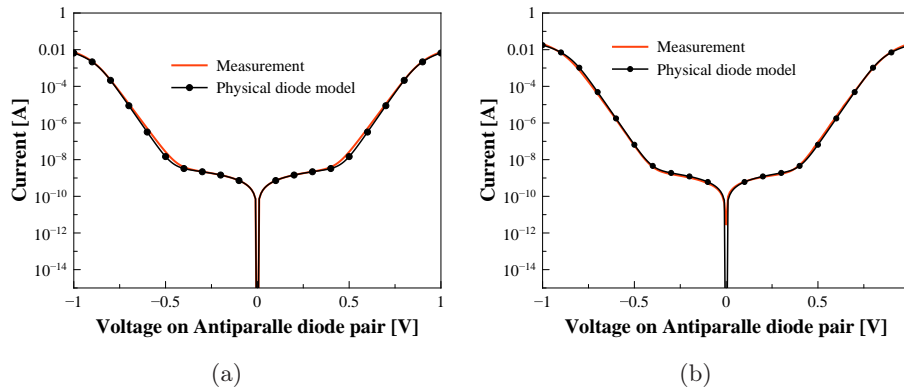


Figure 4.8: The comparison of measured and simulated current-voltage characteristics for two antiparallel diodes with (a) $a=0.5 \mu m$ (b) $a=1.0 \mu m$.

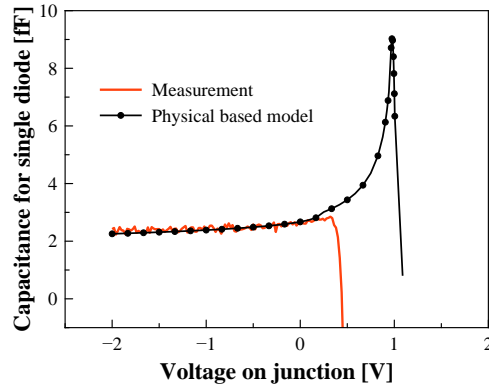


Figure 4.9: The comparison of junction capacitance -voltage characteristics on a diode with $a=0.5 \mu m$. Simulation results from physical diode model is shown.

The simulated noise temperatures at 1.5 GHz are compared to measurement results from [12, 13]. τ_d used in the calculation of hot-electron noise is increased by a factor of 20 for both comparisons. Fig.4.10(a) shows that the simulated noise temperature agrees well with the measurement. Fig.4.10(b) shows the comparison with the other diode, which has a different doping level and size. The prediction from the model follows the trend quite well. At large forward bias, the model predicts less noise temperature, which is due to the fact that extra noise sources from the intervalley scattering mechanism is not included. Intervalley scattering mechanism becomes critical when the diode operates at high forward bias and the electron velocity becomes saturated [12].

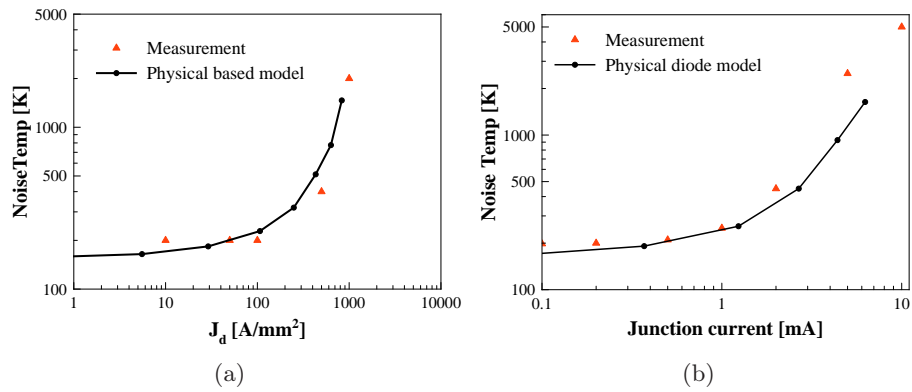


Figure 4.10: (a) Noise temperature versus current density. The measured data is from [11] with diode parameters of $N_{epi}=2e+22 \text{ m}^{-3}$, $a=1.5 \mu\text{m}$, and $\phi_b=0.99 \text{ V}$. (b) noise temperature versus current through the junction. The measured data is from [12] with diode parameters of $N_{epi}=4e+22 \text{ m}^{-3}$, $a=0.89 \mu\text{m}$, $T_{epi}=120 \text{ nm}$, and barrier height $\phi_b=1.0 \text{ V}$.

4.4 SHM with physical diode model

To check the influence of the physical diode model on the performance of the designed SHM, LO port contours are compared in Fig.4.11. It indicates that the LO optimum impedance is slightly shifted. This might be due to the different C-V characteristics in the ADS model and the physical diode model. It is expected that with the originally designed matching network, reflection at LO port will degrade.

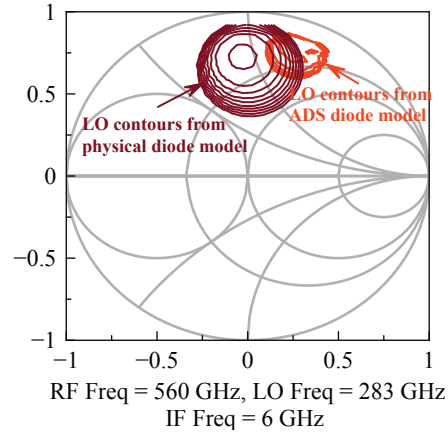


Figure 4.11: Comparison of LO port contours with two different diode models.

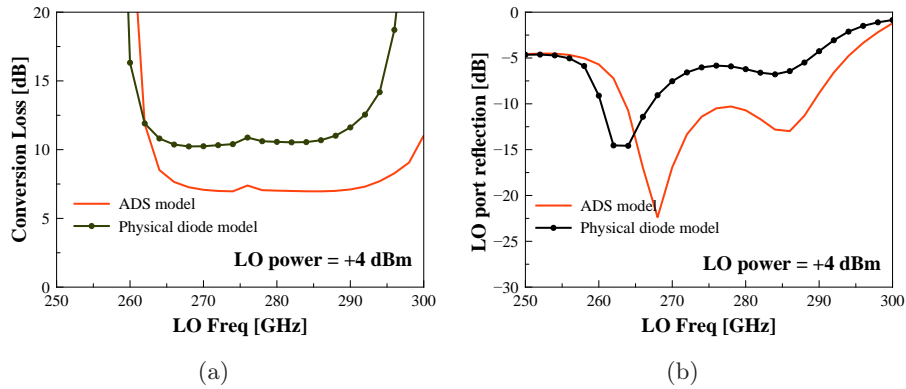


Figure 4.12: Comparison of LO port responses by using different diode models with the same LO input power +4 dBm (a) conversion loss (b) LO port reflection.

The corresponding conversion loss and matching performance are compared in Fig.4.12. With the physical diode model, conversion loss of the designed SHM degrades 2 dB for the whole frequency band and LO matching response is also down shifted. The associated simulated noise temperature are compared in Fig.4.13. With different factors to evaluate the hot electron noise contributions, it can be seen that the hot electron noise only become critical when the fitting factor is above 1000. This number is unrealistic and much larger than the value used before to fit noise temperature measurement for different diodes. It can be concluded that the hot electron noise will not degrade this SHM performance dramatically for +4 dBm LO power level. According to the simulation using physical Schottky diode model, the minimum noise temperature of the designed SHM should be in the range of 2000 to 3000 K. As shown, this result is much larger than the one predicted by ADS model.

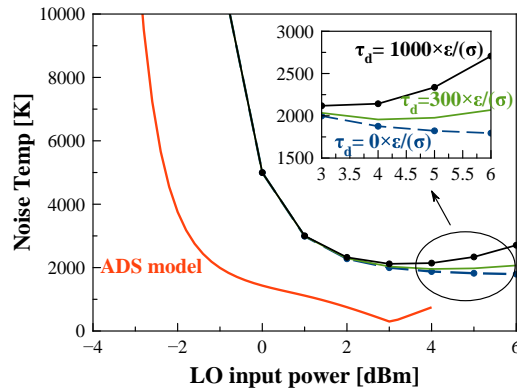


Figure 4.13: Comparison of simulated noise temperature for designed SHM by using ADS model and physical diode model. The simulated noise temperature with different factors are also compared. For the factor of zero, the hot electron noise is turned off.

4.5 Summary

In this chapter, a physical model of Schottky diode is presented. It includes features of the nonlinear impedance from EPI layer, barrier height lowering, velocity saturation, frequency dependent conductivity, and hot electron noise. The measurement of I-V and C-V characteristics from Chalmers are compared with simulation results from the physical diode model. There is a good agreement for IV characteristics, however the predicted capacitance from the model is slightly lower than the measurements. The possible error might arise from the parasitic capacitance or extraction procedure. The noise properties of the diode model is verified by the measurement data from the open literature. Two diodes with different doping and size are chosen for comparison. The good agreement has been shown for the verification of the noise sources implemented in the model.

Simulated SHM performance by using the physical Schottky diode model shows degraded performance compared with the results by using the ADS model. Firstly, the SHM saturates at higher LO power levels and the predicted conversion loss degrades 2 dB for the whole frequency band. The responses of LO port are down shifted due to the difference of modeled capacitance. The estimated noise temperature of the designed SHM from the physical diode model is much larger. With a conservative estimation, the noise temperature of designed SHM will be in the range of 2000 to 3000 K.

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Chapter 5

Low Noise IF Amplifier and Active Mixer

5.1 Wideband low noise IF amplifier

The low noise amplifier is a very important component in the terahertz heterodyne receiver. Its performance influence the overall system sensitivity because it is the first block to amplify the received IF signal from the SHM. To minimize the power reflection between the amplifier and SHM, it is considered best to embedded the LNA into the metallic housing together with the SHM [1]. Some reported low frequency LNAs are summarized in Table5.1. The ones with CMOS technology [2–13] are mostly between 1.4-5.9 dB with a very limited bandwidth. The lowest reported ones from Table5.1 is 0.475 dB to 1.4 dB measured at 1-2 GHz with GaAs HEMT technology [14–16]. In this work, OMMIC's 0.18 μm GaAs pHEMT technology is employed to achieve ultra wideband low noise performance.

From Table5.1, it can be seen that the most commonly used topology for broadband LNA design is the cascode configuration due to its high gain and reduced Miller effect [3–6, 9, 10, 17–20]. Various circuit techniques were used to achieve wideband noise, input matching, and good stability. In this work, transistor size and DC bias are tailored for the best noise performance. Source degeneration, gate and shunt peaking inductors are used to explore simultaneous wideband noise and power matching at the input port. The overall circuit stability is improved by combining a source follower at output stage.

Configuration	Freq [GHz]	Gain [dB]	NF[dB]	Ref
Cascode+feedback [†]	2-6.5	11.9	4.1-4.6	[3]
Cascode [†]	3.1-10.6	<9.3	4-8	[4]
Cascode [†]	3.0-7.0	<15	<1.9	[5]
Cascode [†]	3.0-10.7	11.3	2.2-5	[6]
CG+feedback [†]	0.1-0.93	13	3.6-4.88	[7]
CS [†]	2.8-10.5	13	4.2	[8]
Cascode [†]	3.1-5.15	11.2-12.1	2.29-2.48	[9]
CG+Cascode [†]	3.1-10.6	14.6-18.2	2.9-5.8	[10]
CS+differential [†]	3.1-6.0	15.5-18.2	3.4-5.9	[11]
Inverter [†]	0.2-1.5	<13.8	1.8-2.4	[13]
Cascode [†]	0.5-2.0	20	1.4-1.8	[17]
DA cascode*	3.1-10.6	10	<5.5	[18]
CS+CG+feedback**	0.5-5.0	25-30	1-1.5	[14]
Cascode**	1.9-2.0	23	0.35-0.7	[15]
CS+feedback**	0.6-1.6	<20.9	<0.5	[16]
Cascode**	0.8-8.0	13-17	0.6-1.6	This Work

Table 5.1: Summary of LNA performance from the open literatures. [†] represents that the design is based on CMOS technology, * is for SiGe BiCMOS technology, ** means GaAs technology. Noise Figure(NF), Distributed Amplifier(DA), Common Source(CS), Common Gate(CG).

The DC bias point of the input common-source device is important for the overall amplifier noise figure. The minimum noise figure F_{min} and optimum source impedance from a simple FET model [15, 21] are given as,

$$F_{min} = 1 + \frac{C_N q I_D}{2KT_0} \frac{(\omega C_{gs})^2}{R_{opt} g_m^2} (R_{opt} + R_c + R_g)^2 + \frac{R_c}{R_{opt}} + \frac{R_g}{R_{opt}} \quad (5.1)$$

where C_N is the dimensionless factor found during the modeling procedure of the drain noise current i_{nd}^2 , C_{gs} is the gate source capacitance, R_g is the gate resistance, R_c is part of the channel resistance at the source side, and the real and imaginary part of optimum source impedance for minimum noise figure is formulated as

$$R_{opt} = \sqrt{(R_c + R_g)^2 + \frac{2KT_0 g_m^2 (R_c + R_g)}{C_N q I_D (\omega C_{gs})^2}} \quad (5.2)$$

and

$$X_{opt} = \frac{1}{\omega C_{gs}} \quad (5.3)$$

For the frequency band interested, the second term in Eq.5.2 is dominant, R_{opt} can be simplified to be

$$R_{opt} \simeq \frac{g_m}{(\omega C_{gs})} \sqrt{\frac{2KT_0(R_c + R_g)}{C_{Nq}I_D}} \quad (5.4)$$

With Eq.5.4, F_{min} from Eq.5.1 can be further simplified to be

$$F_{min} = 1 + \frac{(\omega C_{gs})}{g_m} \sqrt{\frac{(R_c + R_g)C_{Nq}I_D}{2KT_0}} \quad (5.5)$$

For a fixed drain current and frequency, $F_{min} - 1$ is proportional to the ratio of

$$F_{min} - 1 \propto C_{gs} \sqrt{R_c + R_g} / g_m \quad (5.6)$$

where all the terms are device size dependent: C_{gs} has a linear relationship with the width of the device, while R_c and R_g have an inverse relationship with the width of the device. For a fixed I_D , g_m can be expressed by

$$g_m\left(\frac{I_D}{I_{DSS}}\right) = g_m(x) = g_{mo} \times f(x) = g_{mo} \times \frac{(1 + a + b)x^2}{x^2 + ax + b} \quad (5.7)$$

where I_{DSS} is the drain current at zero gate bias and has a linear dependency of device width, $f(x)$ is an empirical equation for fitting $g_m(x)$, and g_{mo} represents the case of $g_m(x)|_{I_D=I_{DSS}}$. The first order derivative of $g_m(x)$ is high when $x \ll 1$ for a large device, and becomes small when x approaches one. The optimum value of device size can be estimated by calculating the derivative of Eq.5.6,

$$\frac{d}{dx} \left(\frac{x^2 + ax + b}{(1 + a + b)x^2} \times \sqrt{x} \right) = -\frac{1}{2x^{2.5}} \frac{-x^2 + ax + 3b}{2} \quad (5.8)$$

By solving x for zero numerator, the optimum x_{opt} is found as

$$x_{opt} = \frac{1}{2}(a + \sqrt{a^2 + 12b}) \quad (5.9)$$

For the OMMIC process with technology feature of gate length $0.18 \mu m$, $a \approx 0.159$ and $b \approx 0.00069$ [15], $x_{opt} \simeq a$. This means that for the best noise performance, I_D of the input common-source stage should be 16% of the zero gate bias drain current. To determine the dimension of the transistor for this work, the relevant R_{opt} , X_{opt} , g_m , and NF_{min} are calculated based on

the Eq.5.2, Eq.5.3, Eq.5.7, and Eq.5.1 with simple model scaling parameters defined in Eq.5.10:

$$R_g = R_{g0} \frac{w_0}{w} \quad R_c = R_{c0} \frac{w_0}{w} \quad (5.10a)$$

$$I_{dss} = I_{dss0} \frac{w}{w_0} \quad g_{m0} = g_{mp0} \frac{w}{w_0} \quad (5.10b)$$

$$C_{gs} = C_{gs0} \frac{w}{w_0} \quad C_{gd} = C_{gd0} \frac{w}{w_0} \quad (5.10c)$$

where the reference size $w_0=1$ mm, $R_{c0}=2.64 \Omega$, $R_{g0}=0.20 \Omega$, $I_{dss0}=211$ mA, $g_{mp0}=0.49$ S, $C_{gs0}=708$ fF, and $C_n=2.55$.

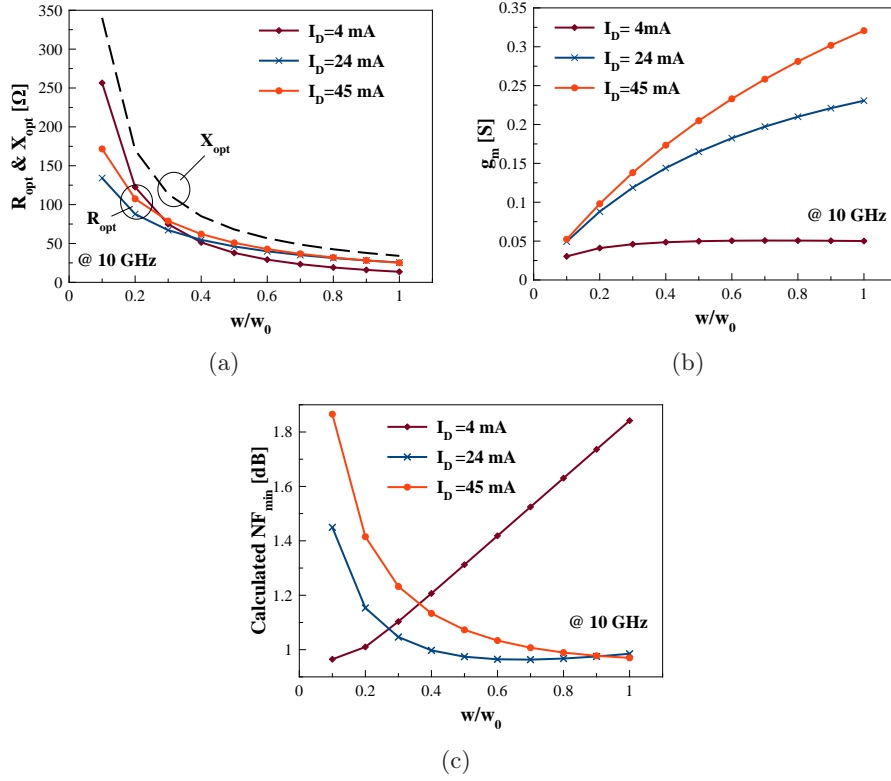


Figure 5.1: (a) Calculated R_{opt} and X_{opt} (b) g_m (c) NF_{min} versus w/w_0 at 10 GHz for a common source configuration. The associated model parameters are based on the Eq.5.10.

Fig.5.1(a) indicates that for a good wideband noise matching, the device size should be around 0.6 mm, where the optimum source impedance

are close to 50Ω . X_{opt} for three different current levels in Fig.5.1(a) is the same due to the fact that the dependency of C_{gs} on I_d is not included in this simple model. The choice of drain current can be seen from Fig.5.1(b) and Fig.5.1(c). Apparently, g_m is too low for a drain current of 4 mA. The amplifier with such a low power gain can not suppress the noise contribution from the later stages. The calculated NF_{min} in Fig.5.1(c) clearly shows that to have a good broadband noise performance at 10 GHz, it is important to use a high drain current for such a large device. For a 0.6 mm dimension, x_{opt} derived from Eq.5.9 indicates an optimum drain current of 24 mA. This explains the increase of NF_{min} for a higher current level of 45 mA. However, the little sacrificed noise figure brings an extra gain from the device to suppress the noise afterwards. The final choice of the bias point needs a few design iterations. By simulating the available device model from the foundry, the choice of DC bias point for a 0.6 mm device is more clear. Fig.5.2 shows a wideband NF_{min} and the derivatives of the transconductance from the device at different gate voltages. It is obvious that the gate bias for a 0.6 mm common-source device should be between -0.4 V and -0.3 V with a drain current of 24-45 mA.

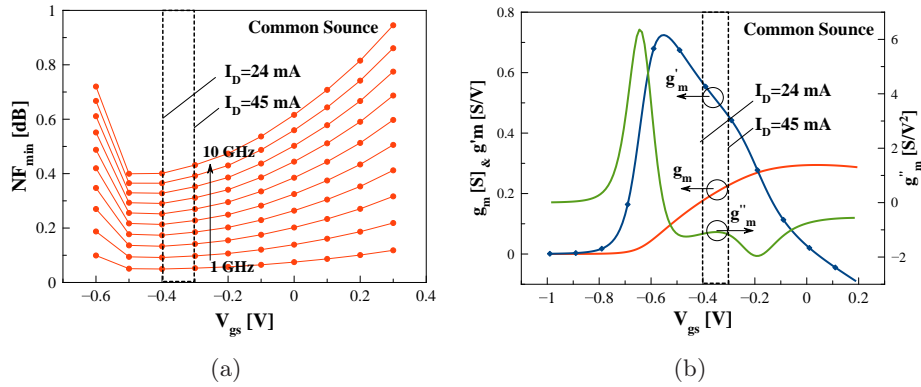


Figure 5.2: (a) Simulated NF_{min} with a 0.6 mm device up to 10 GHz for different bias point (b) g_m , its first order derivative g'_m , and second order derivative g''_m .

With the correct choice of device size and drain current for the cascode stage, the peaking inductor is employed to further improve the flatness of the power gain. To overcome the stability problem of the cascode configuration, a source follower is DC coupled to it for the maximum bandwidth. The

associated bias point and transistor size is optimized for a wideband output matching. The resulting final circuit schematic is shown in Fig.5.3(a). The photography of the MMIC is in Fig.5.3(b) with a chip dimension of $1500 \times 1000 \mu\text{m}^2$.

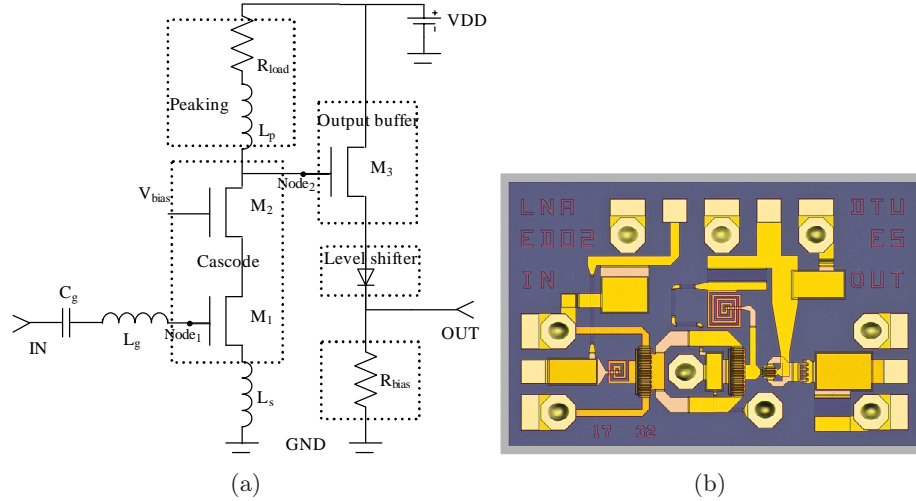


Figure 5.3: (a) Circuit schematic of LNA with the relevant components values: $R_{load}=40 \Omega$, $R_{bias}=100 \Omega$, $L_g=0.33 \text{ nH}$, $L_p=1.5 \text{ nH}$, $C_g=6 \text{ pF}$, $600 \mu\text{m}$ gate width for cascode devices (b) Microphotography of LNA MMIC.

The noise figure of the LNA is characterized by an evaluation board using a HP8970 series noise meter due to the some accuracy problem in the on-wafer measurement. As shown in Fig.5.4, the evaluation board is composed of SMA connectors, 50Ω transmission lines, and long bonding wires. The measured LNA demonstrates good stability for various DC operation points tested as shown in Fig.5.5. To accurately evaluate the noise performance of the designed LNA, the first part of the amplifier within the dashed lines as shown in Fig.5.4(a) has to be de-embedded from the total noise figure of the evaluation board. The error matrix due to the SMA connector and 50Ω transmission line are characterized by the standard SOL calibration at the input port. The associated bonding wire is modeled by a lumped component model [22] including very small DC loss, capacitance and large inductance as a function of the dimension as shown in Fig.5.4(a).

Fig.5.6(a) show that the calibrated NF is smaller than 1 dB up to 6 GHz

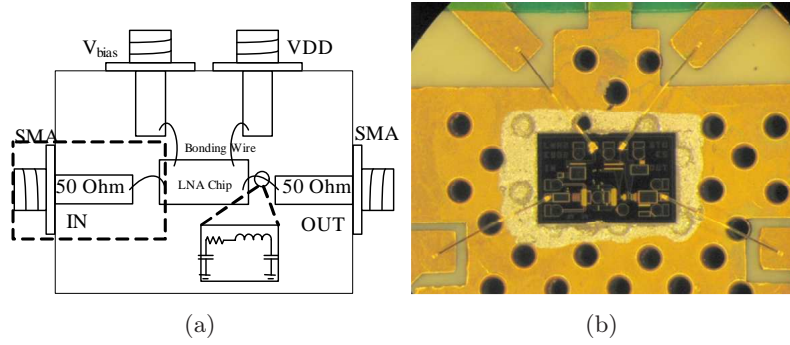


Figure 5.4: (a) Evaluation board for noise characterization: the influence of SMA connector, 50 Ω transmission line, and the bonding wire within the dashed line box has to be de-embedded (b) LNA chip is connected to the PCB evaluation board with long bonding wires.

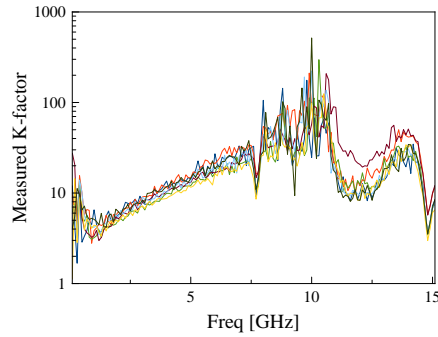


Figure 5.5: Measured K-factor at various DC bias points from $I_D=30$ mA and $V_{CC}=3$ V to $I_D=60$ mA and $V_{CC}=5$ V.

with a minimum value of 0.6 dB for the frequency range from 1.0 GHz to 2.2 GHz. The discontinuity in the measured noise figure at 900 MHz and 1800 MHz is due to the GSM interference during the measurement. At the high end of the frequency band, the noise figure degrades faster than the simulation to a value of 1.5 dB at 8 GHz. The associated input, output return loss and power gain are compared with the results from EM-circuit co-simulations in Fig.5.6(b). It shows that EM modeling of the circuit is accurate. However, the input port is not well matched both in the measurement and simulation. This is due to the fact that the input return loss is compromised for a better wideband noise performance. The difficulty of wideband simultaneous noise and power matching can be seen by observing

Eq.5.2 and Fig.5.6(c). Eq.5.2 indicates that R_{opt} is close to 50Ω from 5 GHz. However, the input impedance of the common-source device due to the large device size is quite small. Using a large source degeneration inductor L_s to boost the input impedance reduces the power gain dramatically. The value of it has to be selected with a great care. The constant noise figure circles at different frequencies in Fig.5.6(c) shows that the predicted noise figure of the complete amplifier after optimization is 0.4 dB above its NF_{min} for the whole frequency range. The output port shown in Fig.5.6(b) has a return loss better than 10 dB. The small difference compared to the EM-circuit co-simulation is due to the accuracy of the diode model. The predicted power gain has 10 GHz bandwidth, while the measurement has only a 3dB bandwidth of 6 GHz. This is due to the over-estimated inductance for peaking. The high power gain and good output return loss help to suppress noise influence from the later stages. The suggested simultaneous power and noise matching by using a shunt RC feedback network [3, 5, 9, 14, 16] between node2 and node1 as shown in Fig.5.3(a) does not improve the noise figure nor input matching when the amplifier operates close to the minimum noise figure.

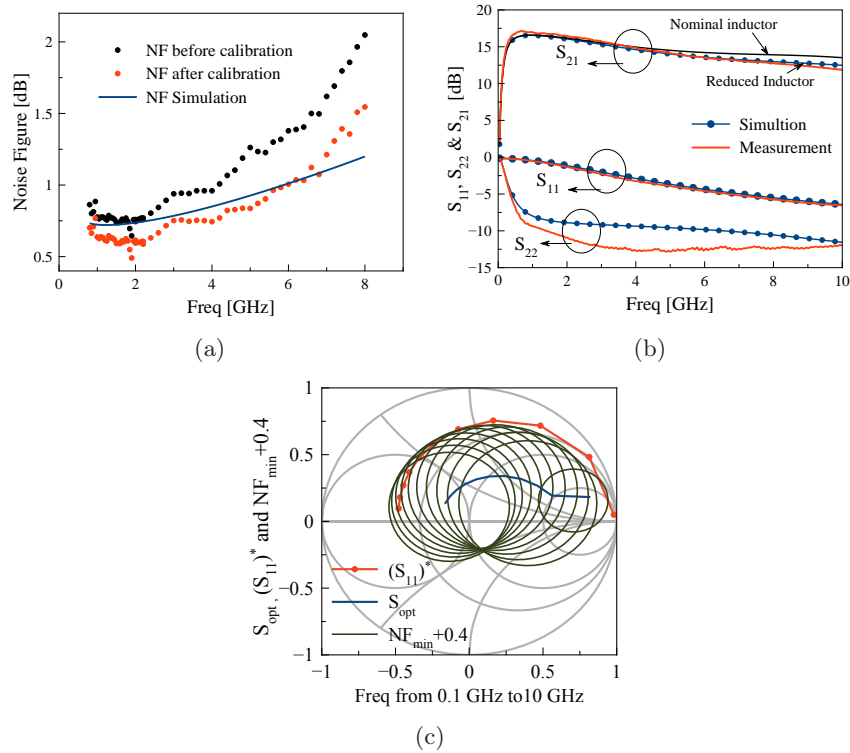


Figure 5.6: (a) Measured and simulated noise figure from 0.8 to 8 GHz: discrete circles represent the measured noise figure before and after calibration; the solid line represents the simulation result; (b) Measured and simulated input, output return loss, and power gain (c) simulated S_{opt} , $(S_{11})^*$, and constant noise figure circles with predicted $NF = NF_{min} + 0.4$ dB from 0.1 to 10 GHz.

5.2 Active mixer

An active double-balanced mixer is designed by using OMMIC's 0.18 μm GaAs pHEMT technology to down-convert the amplified signal from the LNA to baseband. The Gilbert cell mixer was chosen for best LO-IF isolation [23], while in reality it is always limited by the asymmetry introduced by the layout, finite impedance at current tail, and parasitic capacitance due to the coupling of the signal traces. Fig.5.7(b) shows the schematic and microphotography of the implemented double balanced mixer. DC operation conditions are chosen for the largest transconductance G_m and fastest switching for the LO switching quad [24–27]. The degenerated source and gate inductors are used for power matching at the RF port. The noise figure of the mixer core is optimized based on the discussions in [28–30] for an IF frequency at 400 MHz due to the uncertainty of noise model below 100 MHz. With 5 V system voltage and total current of 20 mA, the designed mixer has a predicted conversion loss of 3.0 dB and double sideband noise figure(NF_{dsb}) of 8.7 dB.

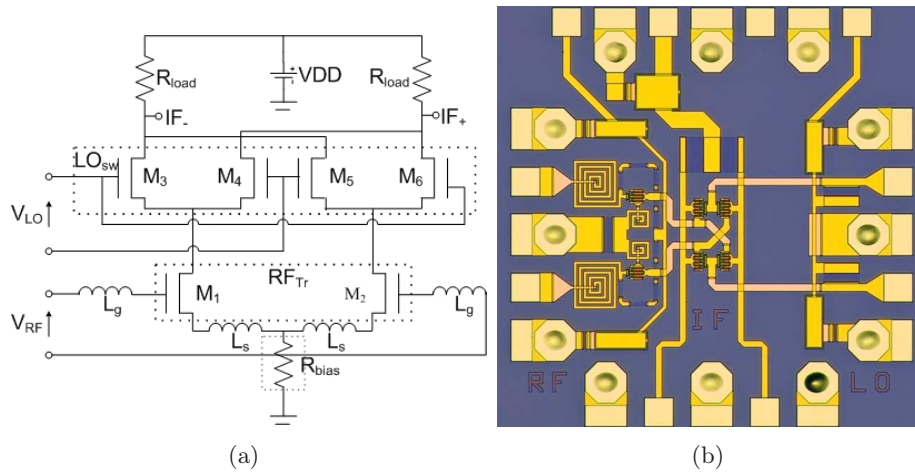


Figure 5.7: (a) Circuit schematic of the active mixer with components values: $R_{load}=100 \Omega$, $R_{bias}=50 \Omega$, $L_s=0.25 \text{ nH}$, $L_g=1.5 \text{ nH}$, $112 \mu\text{m}$ gate width for devices in the transconductance stage, and $90 \mu\text{m}$ gate width for devices in the switching stage (b) Microphotography of the implemented Gilbert cell mixer with the chip dimension of $1200 \times 1200 \mu\text{m}^2$.

The measured conversion loss of the active mixer at different LO pumping

levels are compared with the EM-circuit co-simulation in Fig.5.8(a). EM modeling of the circuit shows good accuracy. The conversion loss without calibration is 4 dB for LO power level larger than +8 dBm. Considering the additional loss from the connection cables and probes, the simulation results agree well with the measurements. The associated RF bandwidth of the mixer is shown in Fig.5.8(b). The high conversion loss for IF frequencies lower than 3 MHz is due to the low frequency limitation of the bias Tee used in the measurement setup. Fig.5.9 shows the measured and simulated double sideband noise figure for IF frequencies below 400 MHz. The increased noise figure at IF frequencies lower than 100 MHz is due to the background 1/f noise of the device. The measured conversion loss from NF meter further confirms that the associated power loss within the measurement setup is about 1.2 dB.

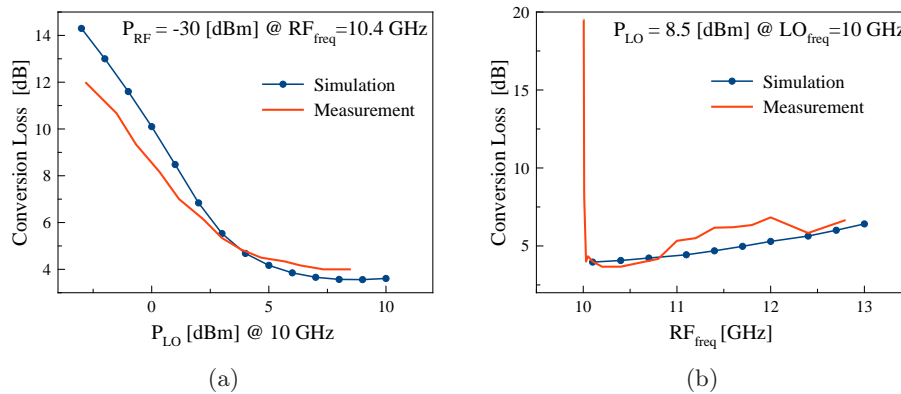


Figure 5.8: (a) Measured and simulated conversion loss versus LO power levels at $LO_{freq} = 10$ GHz and $RF_{freq} = 10.4$ GHz (b) RF bandwidth performance with the fixed LO power of +8.5 dBm and $LO_{freq} = 10$ GHz.

5.3 Summary

A baseband low noise amplifier and an active mixer are designed for the receiver chain. The low noise performance is stressed. The designed LNA uses a cascode configuration with a source follower for wideband stable operation. The simultaneous noise figure and power matching are achieved by using source and gate inductors at the common-source device of the cascode stage. With 5 V system voltage and current consumption of 68 mA, measurements of the LNA chip show 3dB bandwidth of 6 GHz. The measured

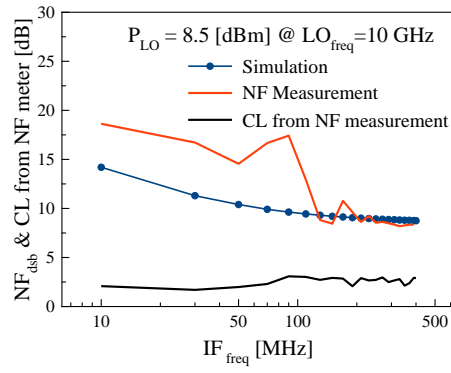


Figure 5.9: Measured and simulated double sideband NF at different IF frequencies. The calculated conversion loss from NF meter are also shown.

noise figure is below 1.5 dB up to 8 GHz with a minimum value of 0.6 dB from 1.0 GHz to 2.2 GHz. The active mixer is designed with the Gilbert cell. The measurement of the mixer core shows a conversion loss of 2.5 dB and NF_{dsb} of 8.0 dB at IF frequencies higher than 200 MHz. The sharp increase of the noise figure at IF frequencies lower than 100 MHz is due to the background $1/f$ noise of the device.

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Chapter 6

Conclusions

In this Ph.D thesis work, power amplifiers for mm-wave applications and key elements for a THz heterodyne receiver system at 557 GHz are designed and documented. The associated mm-wave power generation is achieved with InP DHBT devices. For space applications where low system complexity, long lifetime, and high sensitivity are of concern, the monolithic integrated Schottky diode technology is considered to be a suitable solution. The relevant submm-wave SHM and multiplier are designed by using Schottky diodes on a thin-film GaAs membrane. To simplify the baseband circuitry, a low noise amplifier and an active mixer are designed by using GaAs pHEMT devices to down-convert the receiving signal from the SHM to the DC range. The thesis is divided into several chapters to present the design techniques and measurement results for each individual component, respectively.

In this work, mm-wave power amplifiers with InP DHBT technology for E-band application are investigated. To improve the overall output power and proof the stability analysis, several PA designs are implemented for verification purposes. Based on the comparison of standard power amplifier topologies in term of large-signal characteristics, an interstage matched cascode configuration is proposed for high output power requirements. The measurement results show good linearity and high power density. Another important topic about mm-wave power amplifier is the circuit stability. Stability analysis in terms of even/odd-mode is extensively investigated during this work. The instability detection methods based on the two-port K-factor, linear three-port graphical, and push-pull analysis are discussed and compared. Furthermore, the classical circuit modal analysis is extended based on the symmetry consideration. This means that under small-signal operations,

this method can be used to identify the oscillation loops and determine the location and values of the corresponding stabilization resistors. However, it has an intrinsic problem for stability analysis under large-signal operations. To solve this problem, the pole-zero identification and normalized determinant functions should be considered. The pole-zero identification involves an iterative procedure to synthesize the closed loop transfer function and predict the circuit instability from the pole-zero information. The latter one is the most universal and rigorous method for the stability analysis. However, designers have to access into the detailed device models for both small and large signal analysis. The analysis result from both methods converge under small-signal conditions. The predicted odd-mode oscillation by using circuit modal analysis, pole-zero identification, and normalized determinant functions explains the observed instability from the fabricated two-stage cascade common-emitter PA very well.

This work presents the detailed design methodology of submm-wave SHM by using monolithic integrated Schottky diodes as well. SHM is considered for terahertz heterodyne receiver due to the fact that the local oscillator signal is much easier to generate with solid-state components because of the reduced frequency. The crossbar configuration is employed for the SHM design for this work due to the possibility of DC bias. For such a high frequency component, a fully parameterized 3D EM model of the crossbar structure has to be built in the EM simulator to take the parasitics from the finger structures into account. A large-signal loadpull simulation setup in harmonic balance is used for finding the optimum impedance for each port. To simplify the E-probe design, improved equivalent circuit models of capacitive and inductive E-probes are proposed for the matching circuit synthesis and bandwidth optimization. The associated design procedure and optimization routine are presented as well. To check the SHM performance against the fabrication tolerance, a comprehensive component library is built for accurate EM-circuit co-simulation to save full-wave numerical computations efforts. Furthermore, Monte Carlo analysis is used together with the component library to perform sensitivity analysis. Based on the same crossbar structure, a wideband tripler is presented as well with the aim to generate a RF signal at 557 GHz for the measurement purpose. The designed tripler shows comparable efficiency and bandwidth performance with reported triplers at this frequency range. The tripler design can be down scaled in frequency to be used in the LO chain of the terahertz receiver as well.

Due to the fact that ADS diode model only includes very limited features

for diode modeling, a physical model based on the fabrication parameters is implemented to include electron velocity saturation, barrier height lowering, nonlinear impedance from EPI layer, tunneling current, frequency dependent conductivity, and hot electron noise. To proof the model, simulation results are compared with measurements from Chalmers and open literatures. Good agreement has been achieved for I-V, C-V, and noise comparisons. The predicted SHM performance with physical diode model degrades but is more realistic.

The received IF signal from the SHM is further amplified and down-converted to the DC range by two components: an IF LNA and an active mixer. Both components are designed by using GaAs pHEMT devices. The LNA employs a cascode configuration with an output buffer to improve the circuit stability and achieve the low noise wideband performance. The measurement results confirm the wideband frequency responses of the noise figure. The active mixer is designed based on the simple and straight forward Gilbert cell. The measurements agree very well with designed mixer for the conversion loss and double sideband noise figure.