SOFT-SWITCHING HIGH-FREQUENCY AC-LINK UNIVERSAL POWER CONVERTERS WITH GALVANIC ISOLATION

A Dissertation

by

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ABSTRACT

In this dissertation the ac-link universal power converters, which are a new class of power converters, are introduced and studied in detail. The inputs and outputs of these converters may be dc, ac, single phase, or multi-phase. Therefore, they can be used in a variety of applications, including photovoltaic power generation, wind power generation, and electric vehicles. In these converters the link current and voltage are both alternating and their frequency can be high, which leads to the elimination of the dc electrolytic capacitors and the bulky low-frequency transformers. Therefore, the ac-link universal power converters are expected to have higher reliability and smaller size. Moreover, these converters are soft switching, which results in negligible switching losses and minimized current and voltage stress over devices.

In the first part of the dissertation, the parallel ac-link universal power converter is studied in detail. This converter is an extension of the buck-boost converter. The series ac-link universal power converter, which is dual of the parallel ac-link universal power converter, is proposed in the second part of this dissertation. This converter is an extension of the Cuk converter. A modified configuration with fewer switches, named sparse ac-link universal power converter is proposed in the third part of this dissertation. The sparse ac-link universal power converters can appear as parallel or series.

The performance of all these configurations is evaluated through simulations and experiments.

To my parents, Minoo and Mohammad

To my husband, Siavash

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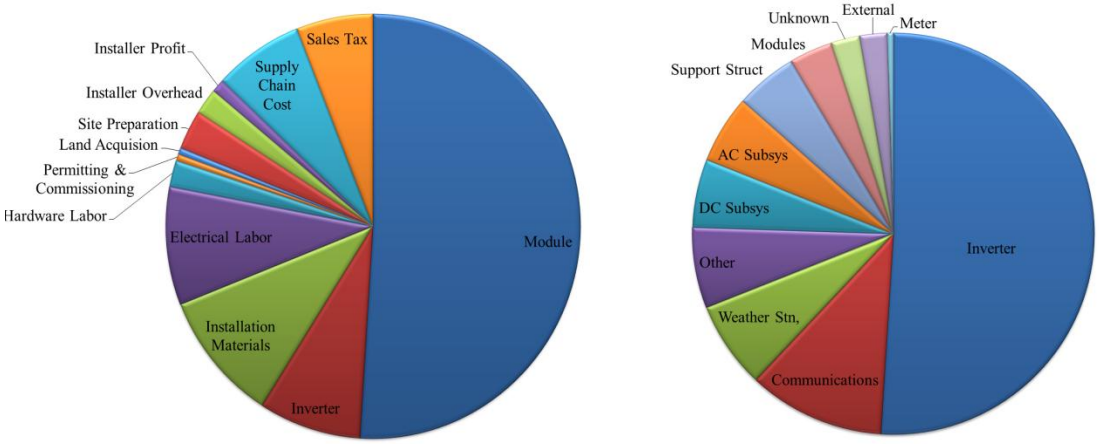
1. INTRODUCTION

In this dissertation a new class of power converters, named ac-link universal power converters, is introduced. These converters have several advantages over the other types of converters that make them an excellent candidate for use in renewable energy systems and for use in electric and hybrid-electric vehicles.

Concerns regarding fossil fuel prices, energy security, and climate change have led to a significant amount of research on renewable energy systems and the methods facilitating their higher penetration. Among these active research areas is power electronics. Power converters are essential components of many systems, including renewable energy systems. In a photovoltaic (PV) system, for instance, inverters account for almost 8% of the total upfront cost, and are responsible for more than 50% of the total failures. The total cost breakdown and the total failures by main components in a PV system are represented in Figure 1 [1, 2]. The high failure rate of the inverters apparently decreases their lifetime. The lifetime of the PV inverters is usually between 5 to 10 years; whereas the lifetime of the PV modules is about 25 years. Therefore, PV inverters need to be replaced two or three times within the lifetime of a PV system. Consequently, the actual cost of a PV system should include periodic inverter replacements [3].

Similarly, in a wind power generation system, converters and transformers account for about 10% of the wind turbine cost; and, from the reliability point of view, power modules in general account for almost 37% of the overall down time. The total

cost breakdown of a wind power generation system and the percentage contribution of different components of a wind power generation system to overall downtime are shown in Figure 2 [4, 5].

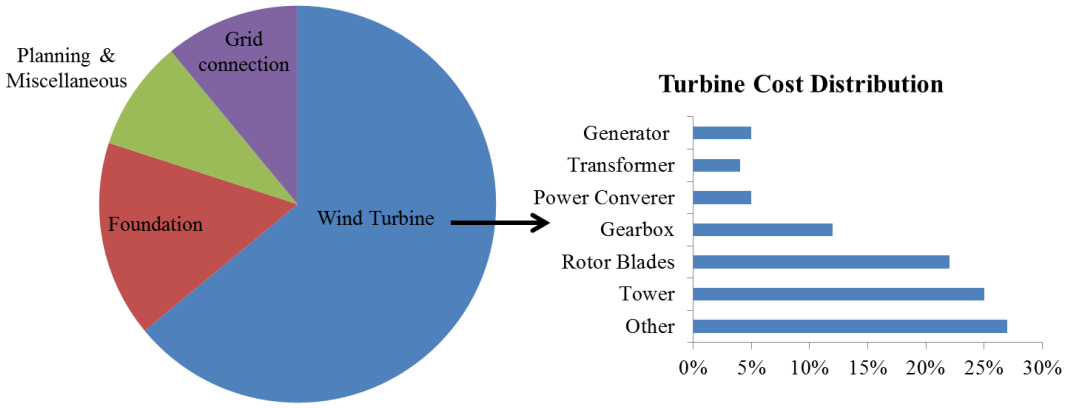


(a) Cost breakdown of a utility-scale PV system [1]

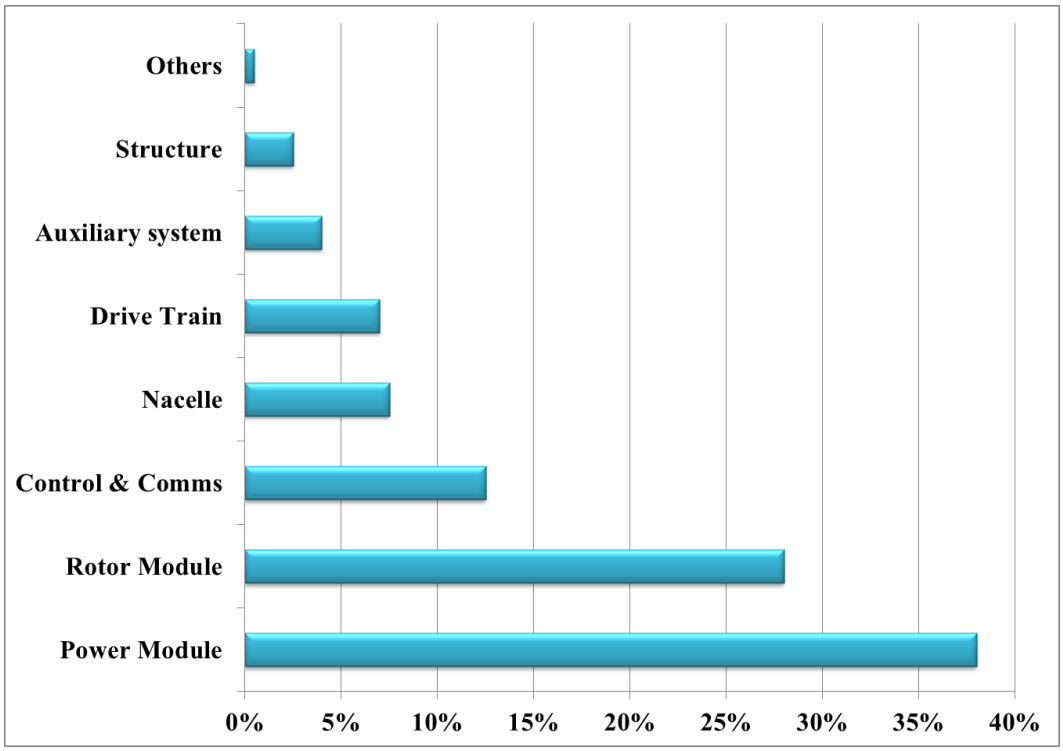
(b) Leading Causes of "Hard" PV System Failures[2]

Figure 1 Total cost breakdown and the total failures by main components in a PV system

The importance of power electronics in renewable energy systems can be concluded from the above statistics. The addition of power electronics usually adds cost to renewable energy systems, as well as contributing to reliability problems. In this part there will be a brief overview of the power converters employed in wind and PV power generation systems, two of the fastest growing renewable energy technologies. The main problems associated with converters that are employed in these systems are reviewed. Converter problems may hinder the higher penetration of renewable energy systems.



(a) Capital cost breakdown for a typical onshore wind power system and turbine [4]



(b) Percentage contribution to overall failure rate [5]

Figure 2 Total cost breakdown of a wind power generation system and the percentage contribution of different components of a wind power generation system to overall downtime

In past designs, a centralized converter-based PV system was the most commonly used type of PV system. As shown in Figure 3, in this system, PV modules

are connected to a three-phase voltage source inverter. The output of the inverter is connected to the grid through a three-phase low-frequency transformer, which steps up the voltage and provides galvanic isolation [6].

Low-frequency transformers are considered poor components mainly because of their large size, which can indirectly add costs to the system. This is because a large transformer requires a bulkier, and consequently, a more expensive foundation. To avoid the need for low-frequency transformers, multiple-stage converters are widely used in PV systems. The most common topology, which is represented in Figure 4, includes a voltage-source inverter and a dc-dc converter. Commonly, the dc-dc converter contains a high-frequency transformer. Despite offering a high boosting capability and galvanic isolation, this converter consists of multiple power processing stages that lower the efficiency of the overall system. Moreover, electrolytic capacitors are required for the dc link. Electrolytic capacitors, which are very sensitive to temperature, might cause severe reliability problems in power converters and an increase of even 10 °C can halve their lifetime. Therefore, PV inverters containing electrolytic capacitors are not expected to provide the same lifetime as the PV modules. Consequently, the actual cost of the PV system involves periodic replacement of the inverter, which increases the levelized cost of energy extracted from the PV system [3, 6-9].

Different configurations of variable speed wind turbine systems are illustrated in Figure 5. As seen in this figure, the bulky low-frequency transformer is an inseparable part of these configurations.

Traditionally, dc-link converters, which are formed by a rectifier and an inverter, are employed in wind power generation systems. In the simplest case, the rectifier can be formed by a diode bridge. To improve the currents, the dc-link converter can be implemented by a pulse-width modulated (PWM) rectifier and a PWM inverter. Regardless of the inverter and the rectifier topologies, a dc electrolytic capacitor, which deteriorates the circuit reliability and lifetime, is an integral part of the dc-link converters. High switching losses and high device stresses are other important limitations of this type of converter [10, 11].

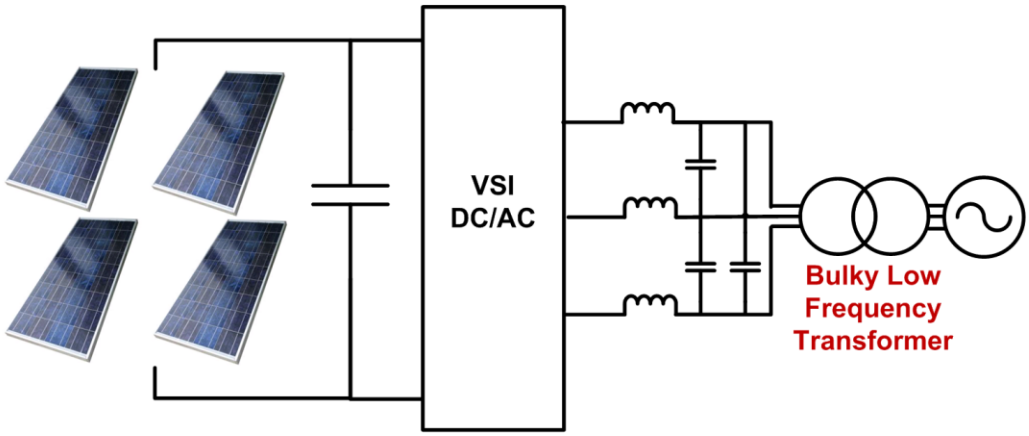


Figure 3 Centralized converter-based PV system

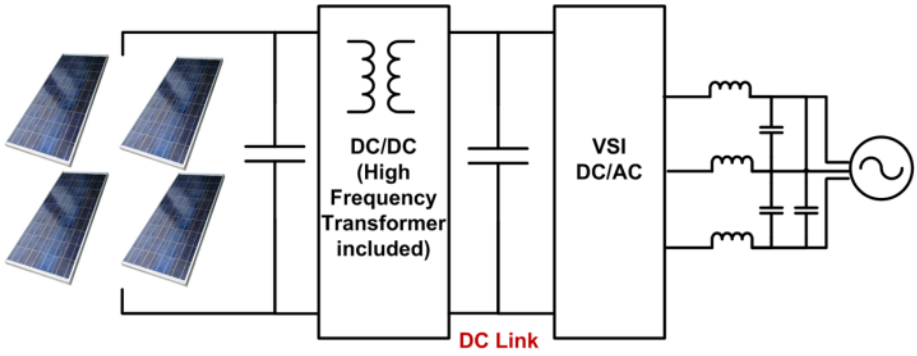


Figure 4 Multiple-stage conversion systems used in PV applications

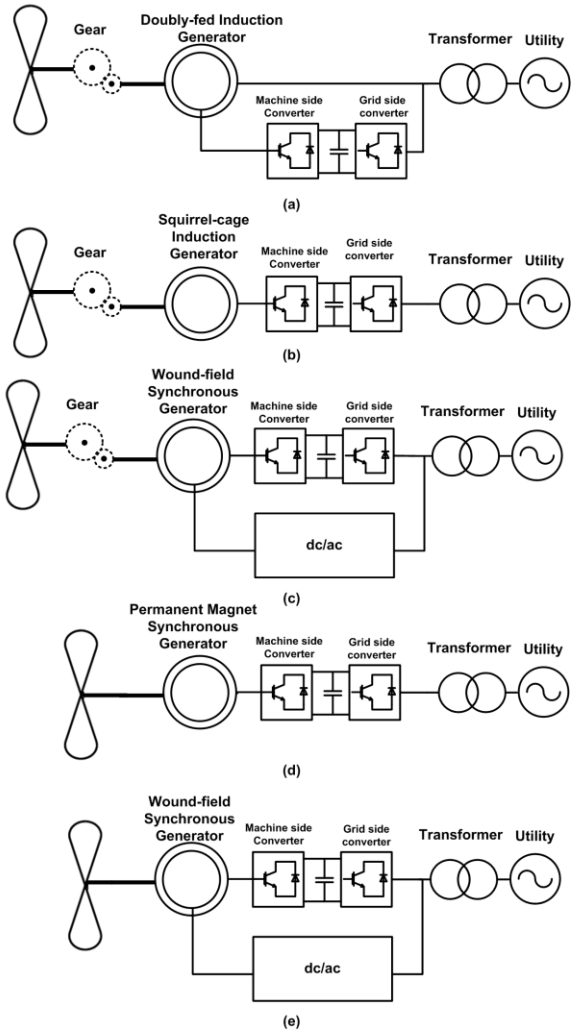


Figure 5 Wind turbine configurations in variable speed constant frequency systems: (a) indirect drive using doubly-fed induction generator, (b) indirect drive using squirrel-cage induction generator, (c) indirect drive using wound-field synchronous generator, (d) direct drive using permanent magnet synchronous generator, (e) direct drive using wound-field synchronous generator [10].

Considering the aforementioned problems, for the long-term success of renewable energy sector it is essential to support the design of alternative power converters with higher reliability and lower cost.

As an alternative to the currently available converters, ac-link universal power converters were proposed. This category of power converters is described as “universal” because their inputs and outputs can be dc, ac, single-phase, or multi-phase. Therefore, they can be employed in a variety of applications including, but not limited to, PV power generation, battery-utility interfaces, battery chargers, and wind power generation.

In the ac-link universal power converters, the link current and voltage are both alternating and they may have a high frequency; therefore, there is no need for dc electrolytic capacitors at the link. Considering all the problems associated with the electrolytic capacitors, such as temperature dependency, this converter is an excellent alternative to dc-link converters. Moreover, in these converters galvanic isolation can be provided by adding a single-phase high-frequency transformer to the link. Therefore, no low-frequency transformers are employed in ac-link universal power converters. Another merit of these converters is soft switching of the switches that leads to negligible switching losses. Moreover, due to soft switching of the switches, the current and voltage stress over the switches is minimized and there is no need for snubbers in these converters.

The parallel ac-link universal power converter, which was first introduced in [12], is currently available in the market. The dc to three-phase ac parallel ac-link universal power converter has recently been included in the California Energy Commission (CEC) list of approved PV inverters. This converter is an extension of the dc-dc buck-boost converter. Of course, several modifications have been applied to provide the alternating link current and soft switching. In this converter, switches are all

turned on at zero voltage and their turn-off is capacitance buffered. Some of the applications of this converter have been studied in [13-25]. In section 2 the principles of the operation of this converter along with its design and detailed analysis are presented. With the analysis introduced, the performance of the converter can be predicted at any power level. Moreover, the hybrid parallel ac-link universal power converter will be proposed in section 2.

Section 3 of this dissertation proposes the series ac-link universal power converter. Similar to the parallel ac-link universal power converter, the series ac-link universal power converter has several advantages over the other types of converters. In this converter the switches are turned off at zero current and their turn on is soft [26, 27]. The major advantage of this converter over the parallel ac-link universal power converter is that due to the zero current turn off of the switches, silicon controlled rectifiers (SCRs) may be used as well. SCRs have several benefits over the other types of switches: They are available at both high current and high voltage ratings; They have low losses; and, They are inexpensive and reliable. Therefore, they are very popular in high power applications and reliability demanding applications. The series ac-link universal power converter is the dual of a parallel ac-link universal power converter. Therefore, it is in essence an extension of the dc-dc Cuk converter and several modifications have been applied to provide the alternating link voltage and soft switching.

Despite having numerous advantages, both the series and parallel ac-link universal power converters have more switches compared to most of the other

converters. In order to simplify the design and to further increase reliability, the sparse and the ultra-sparse ac-link universal power converters are proposed in section 4 of this dissertation. These converters have all of the advantages of the original configurations, but they use fewer switches [28, 29]. Two patents on the novel topologies presented in this dissertation have been filed [30, 31].

Finally, the main points of this dissertation will be summarized in section 5.

2. PARALLEL AC-LINK UNIVERSAL POWER CONVERTER*

2.1. Introduction

This section introduces the parallel ac-link universal power converters. This converter is an extension of the dc-dc buck-boost converter. By adding the complementary switches and by modifying the switching scheme, the link inductor, which is the main energy storage element in this converter, can have alternating current instead of the direct current. This approach improves the performance of the converter and significantly increases the utilization of the link inductor.

The following section presents a summary of the required steps to form a three-phase ac-ac ac-link buck-boost converter from the conventional dc-dc buck-boost converter. It will be shown that placing a small capacitor in parallel with the link inductor enables the converter to benefit from soft switching, which significantly increases its efficiency. The principles of operation of this soft switching converter, which is called the parallel ac-link universal power converter, are studied in section 2.3.

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1. "High Frequency ac-Link PV Inverter" by M. Amirabadi, A. alakrishnan, H. Toliyat, and W. Alexander, IEEE Transactions on Industrial Electronics, vol. 61, pp. 281-291, 2014. Copyright 2013 by IEEE.
2. "Partial resonant AC link converter: A highly reliable variable frequency drive" by M. Amirabadi, H. A. Toliyat, and W. C. Alexander, in Proc. IEEE Industrial Electronics Society Annual Conference (IECON), 2012, pp. 1946-1951. Copyright 2014 by IEEE.
3. "A Multi-Port ac Link PV Inverter with Reduced Size and Weight for Stand-alone Application" by M. Amirabadi, H. A. Toliyat, and W. C. Alexander, IEEE Transactions on Industry Applications, 2013, in press. Copyright 2013 by IEEE.
4. "Battery-utility interface using soft switched ac link supporting low voltage ride through" by M. Amirabadi, H. A. Toliyat, and W. C. Alexander, in Proc. IEEE Energy Conversion Congress and Exposition Conference (ECCE), 2009, pp. 2606-2613. Copyright 2009 by IEEE.
5. "Chapter 5: AC-Link Universal Power Converters: A New Class of Power Converters for Renewable Energy and Transportation" by H. A. Toliyat and M. Amirabadi in "Power Electronics for Renewable Energy Systems, Transportation and Industrial Applications" edited by Haitham Abu-Rub, Marius Malinowski, and Kamal Al-Haddad, 2013, John Wiley & Sons, Ltd., West Sussex, UK. Copyright 2013 by John Wiley & Sons, Ltd.

The design procedures and the analysis of this converter are presented in sections 2.4 and 2.5, respectively. In section 2.6, the low voltage ride-through feature of this converter will be studied and it will be shown that the converter is capable of injecting reactive power in case of a load voltage drop. In section 2.7 it will be shown that the control scheme studied in section 2.3 has certain constraints on the load power factor for providing soft switching. An improved control scheme, which results in soft switching of the switches regardless of the load power factor and the input and output voltage levels, will be proposed in this section. The hybrid parallel ac-link universal power converter is introduced in section 2.8. Some of the applications of the parallel ac-link universal power converter along with the simulation and experimental results are presented in section 2.9, and finally, section 2.10 summarizes this section.

2.2. Evolution of the Parallel AC-Link Universal Power Converter and the Background

We will start from the most basic configuration; a dc-dc buck-boost converter, as shown in Figure 6. In a buck-boost converter, the link inductor is first charged from the input and then discharged into the output. Clearly, this circuit has two modes of operation: mode 1, charging the link, and mode 2, discharging the link. During mode 1, switch S1 conducts and during mode 2, switch S2 conducts. It is assumed that this buck-boost converter operates at the boundary of continuous and discontinuous conduction modes. Switch S2 must block reverse voltage. Hence, in Figure 6, a diode is placed in series with this insulated-gate bipolar transistor (IGBT). Voltages V1 and V2 are both assumed to be positive. In a conventional buck-boost converter, switch S2 is usually

removed and the diode conducts during mode 2. This converter can also be demonstrated, as represented in Figure 7. Although the bottom diode, switch S3 and switch S4 are unnecessary for this case, they are required for the subsequent steps.

In order to have an alternating inductor current, or in other words, to allow the link inductor to charge and discharge in both positive and negative directions, four other switches should be added, as depicted in Figure 8. The link cycle can then be divided into two half cycles, with the positive link current during the first half cycle and the negative link current during the second half cycle. This configuration results in an alternating link current. This converter has four modes of operation: mode 1, charging the link with positive current; mode 2, discharging the link with positive current; mode 3, charging the link with negative current; and mode 4, discharging the link with negative current. Switches S1, S2, S3, and S4 conduct when the inductor current is positive. Whereas, switches S5, S6, S7, and S8 conduct in the case of a negative link current.

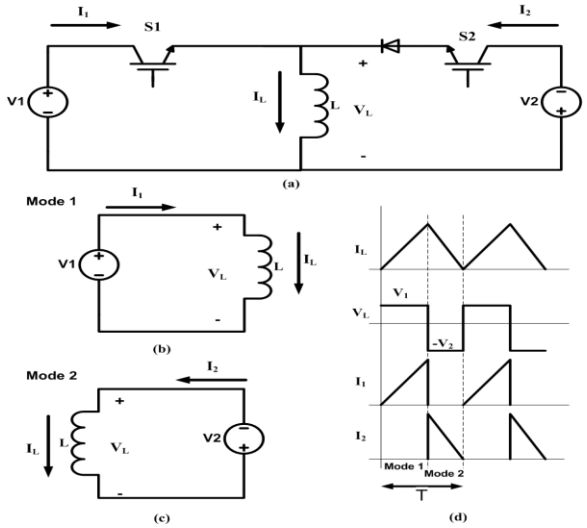


Figure 6 Dc-dc buck-boost converter: (a) configuration, (b) energizing mode (mode 1), (c) de-energizing mode (mode 2), (d) voltage and current waveforms

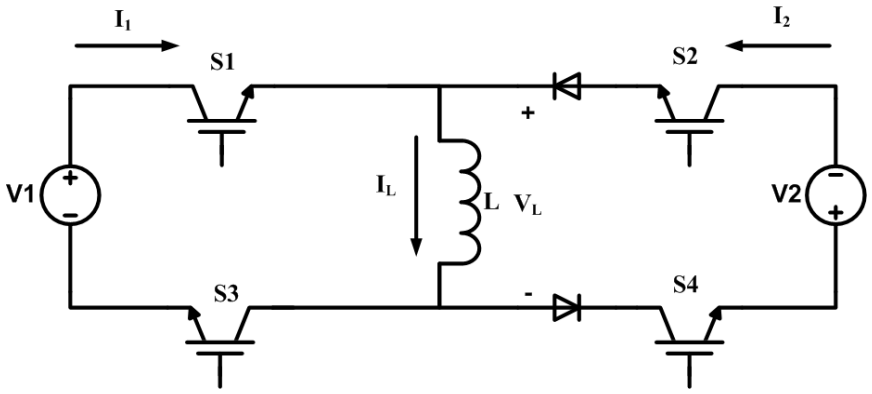


Figure 7 An alternative representation of the dc-dc buck-boost converter

If bidirectional power flow is required, then the number of switches must be doubled, as shown in Figure 9. Switches S1–S8 transfer the power from V1 to V2 and switches S9–S16 are responsible for transferring the power from V2 to V1. The converter shown in Figure 9 is a bidirectional dc-dc ac-link buck-boost converter.

Adding more legs to each side of this converter yields multi-phase bidirectional ac-link converters, such as the dc to multi-phase ac, multi-phase ac to dc, and multi-phase ac to multi-phase ac configurations. The dc to three-phase ac, three-phase ac to dc, and three-phase ac to ac configurations are shown in Figure 10.

The principles of operation of the multi-phase converter are similar to those of the dc-dc converter; however, the main challenge is to determine the contribution of each phase of the multi-phase system to the charging or discharging of the link. Let us consider a three-phase inverter, as shown in Figure 10 (a). As the input of the inverter is dc, the charging of the link in this case is similar to that of the dc-dc converter. However, during the discharging mode, there is one link to be discharged and two phase-pairs to be charged from the link. In order to have lower Total Harmonic Distortion (THD) on the

currents, the discharging mode may be split into two modes. In a balanced three-phase system, the sum of the phase currents at any instant is zero. One of them is highest in magnitude and of some polarity while the two with lower magnitude are of the opposite polarity. Although there are three phase-pairs in a three-phase system, considering the polarity of the current in each phase, only two of these phase-pairs can provide a path for the current when connected to the link. Therefore, the charged link transfers power to the output by discharging into two phase-pairs. The two phase-pairs are the one formed by the phases having the highest current and the second highest current, and the one formed by the phases having the highest current and the lowest current, where the currents are sorted as highest, second highest, and lowest in terms of magnitude alone. For example, if $I_{a\_o} = -10$ A, $I_{b\_o} = 7$ A, and $I_{c\_o} = 3$ A are the three-phase currents, then phase-pairs "ab" and "ac" are chosen to be charged from the link. Therefore, in the case of dc to three-phase ac, there are six modes of operation. Similarly, in a three-phase ac-ac system, each charging and discharging mode will be split into two modes, which results in eight modes of operation. By splitting the charging mode into two modes, the input power factor may be controlled, as well.

It must be noted that, in practice, the incoming switches on the output side need to be turned on before turning off the outgoing switches on the input side. However, being reversed biased, the incoming switches do not conduct before the outgoing switches are turned off. On the other hand, the incoming switches on the input side might need to be turned on after the link current is zero and the outgoing output-side

switches are turned off. This might result in operation of the converter in discontinuous conduction mode.

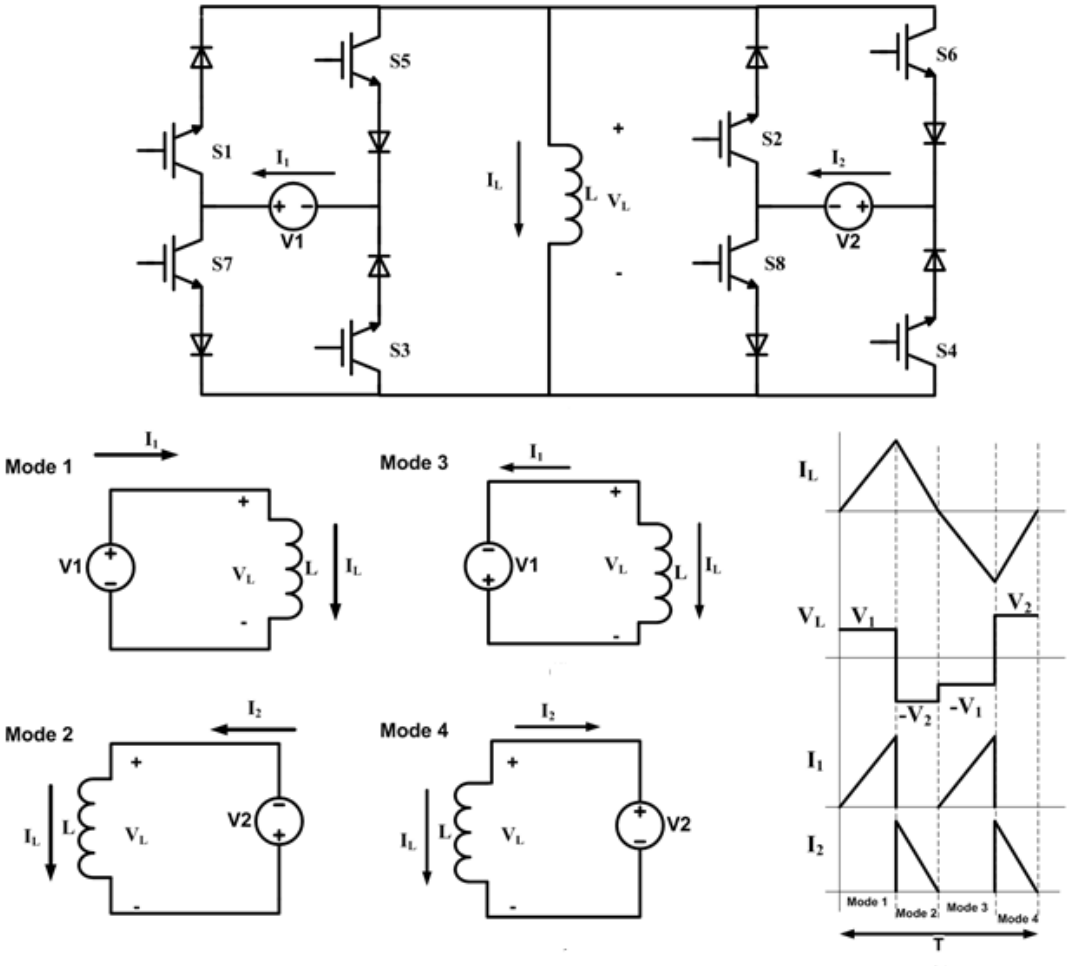


Figure 8 Dc-dc ac-link buck-boost converter: configuration, behavior of the circuit during different modes, and waveforms

This converter transfers power entirely through the link inductor (L). Placing a small capacitor (C) in parallel with the link inductor allows the switches to be turned on at zero voltage, as well as benefitting from soft turn-off. This converter, which is called the parallel ac-link universal power converter in this dissertation, was first proposed in

[12]. Figure 11 shows the configuration of a three-phase ac-ac parallel ac-link universal power converter.

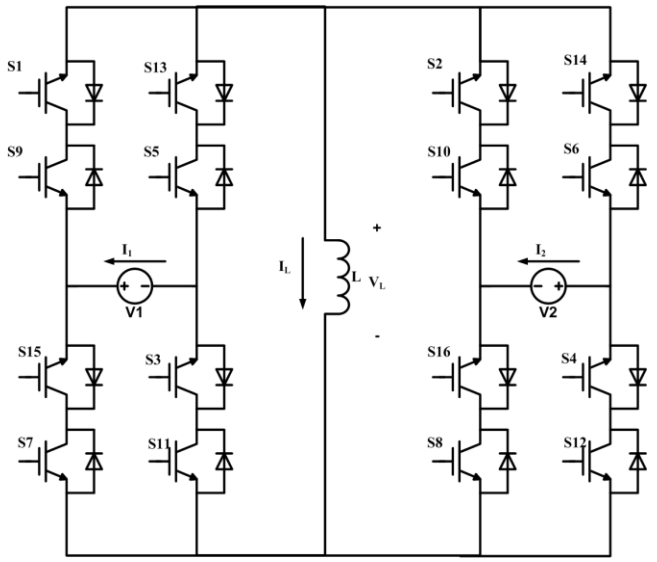


Figure 9 Bidirectional dc-dc ac-link buck-boost converter

In this converter, between each charging and discharging mode, there is a resonating mode during which none of the switches conduct and the link resonates to facilitate the zero voltage turn-on and soft turn-off of the switches. This converter is a partial resonant converter, i.e., only a small time interval is allocated to resonance in each cycle. Hence, while the resonance facilitates the zero voltage turn-on and soft turn-off of the switches, the LC link has low reactive ratings and low power dissipation.

Now that the evolution of the parallel ac-link universal power converter has been discussed in detail, it is appropriate to study the historical development of this converter, as well.

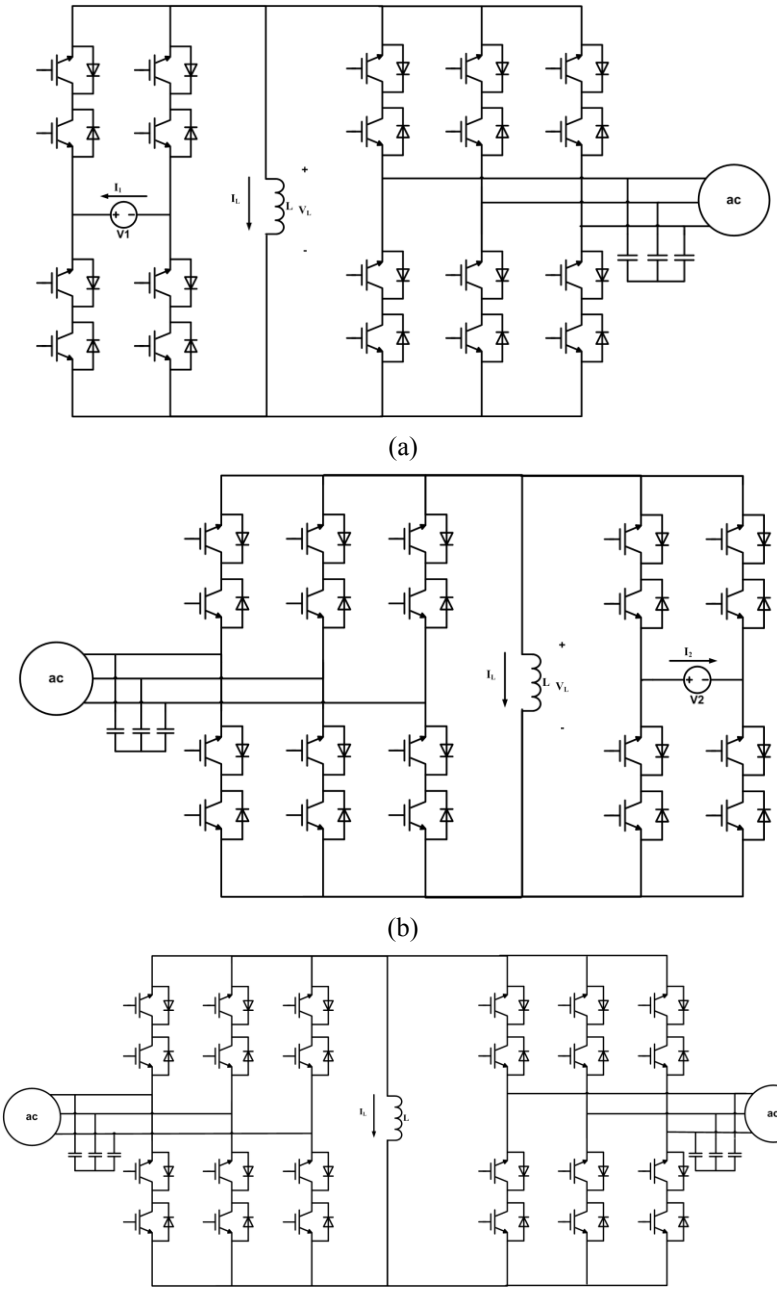


Figure 10 (a) bidirectional dc-ac ac-link buck-boost converter, (b) bidirectional ac-dc ac-link buck-boost converter, (c) bidirectional ac-ac ac-link buck-boost converter

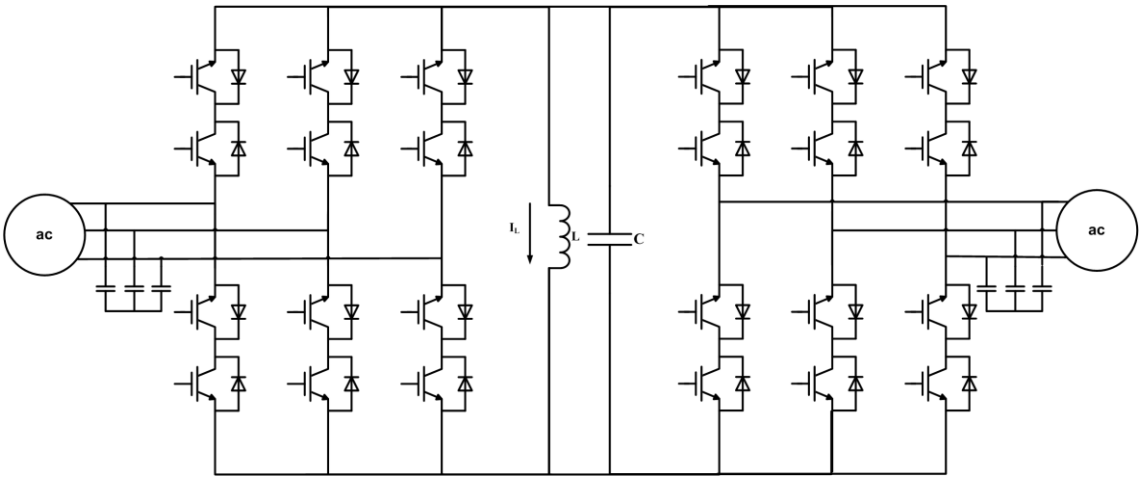


Figure 11 Soft-switching bidirectional ac-ac ac-link buck-boost converter (ac-ac parallel ac-link universal power converter)

Hard switching dc-ac, ac-dc, and ac-ac dc-link buck-boost converters were first proposed in [32]. These converters were extensions of the dc-dc buck-boost converter. The three-phase ac-ac configuration was formed by twelve unidirectional switches. The inductor current in this converter was dc and the converter was hard switching. This configuration is shown in Figure 12.

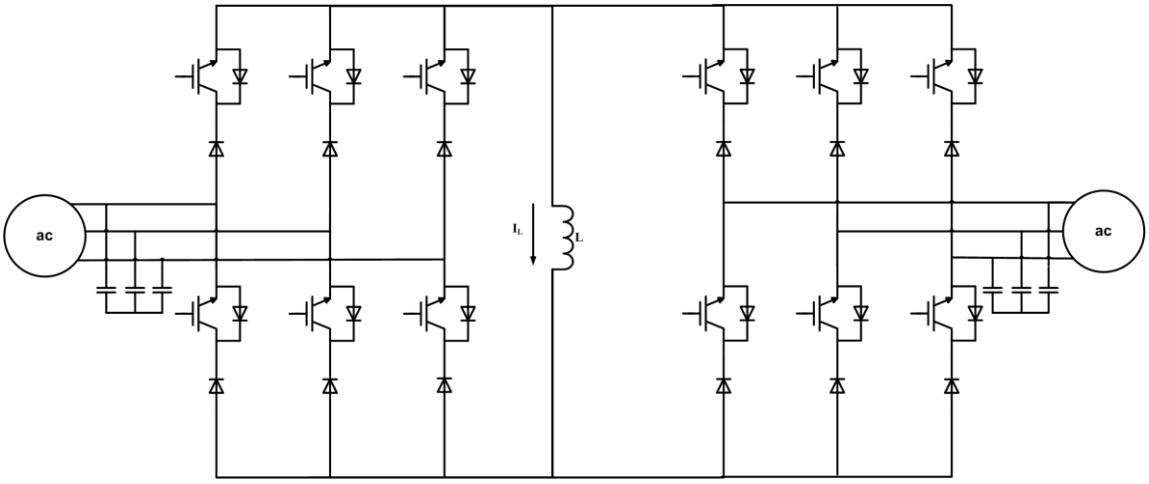


Figure 12 Ac-ac dc-link buck-boost converter proposed in [32]

Resonant ac-ac converters, which are classified as ac-link converters, have been proposed as an alternative to dc-link converters [33, 34]. Despite being a breakthrough in the 1980s, these types of converters have some limitations which prevent their widespread use. In [34], the parallel ac voltage resonant converter was proposed. The link in this converter, which is illustrated in Figure 13, is formed by a parallel LC pair resonating continuously. Therefore, the passive link components need to have high reactive ratings and there is high power dissipation in the link. Moreover, the load inductance and capacitance can affect the link resonance. Hence, this type of converter is not suitable for all types of loads. Other types of resonant ac-ac converters were introduced in [33, 35-37].

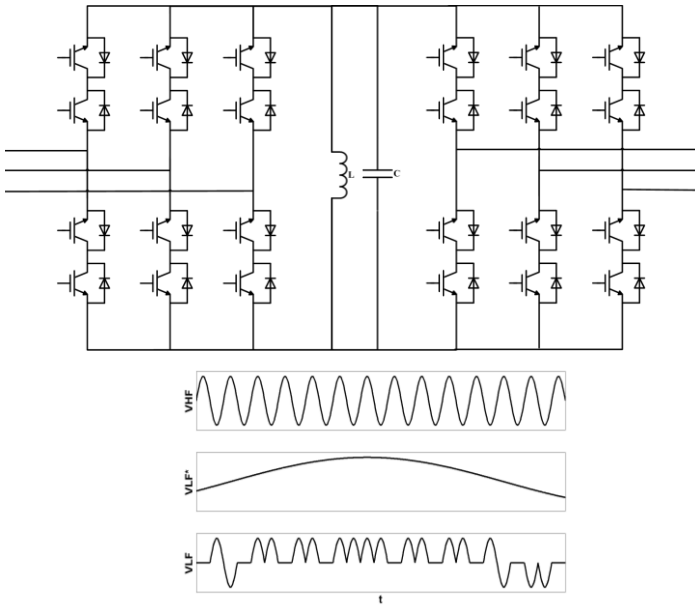


Figure 13 Parallel ac voltage resonant converter [33, 34]

A partial resonant topology with twelve unidirectional switches, shown in Figure 14, was proposed in [38]. This converter was a soft switching ac-ac dc-link buck-boost converter. Soft switching was possible in this converter by adding a capacitor in parallel

with the link inductor. Despite the high frequency of the link and soft switching, this converter suffers from reduced utilization of the inductor due to the dc component of the link current and long quiescent resonant swing back time during which no power is transferred [12].

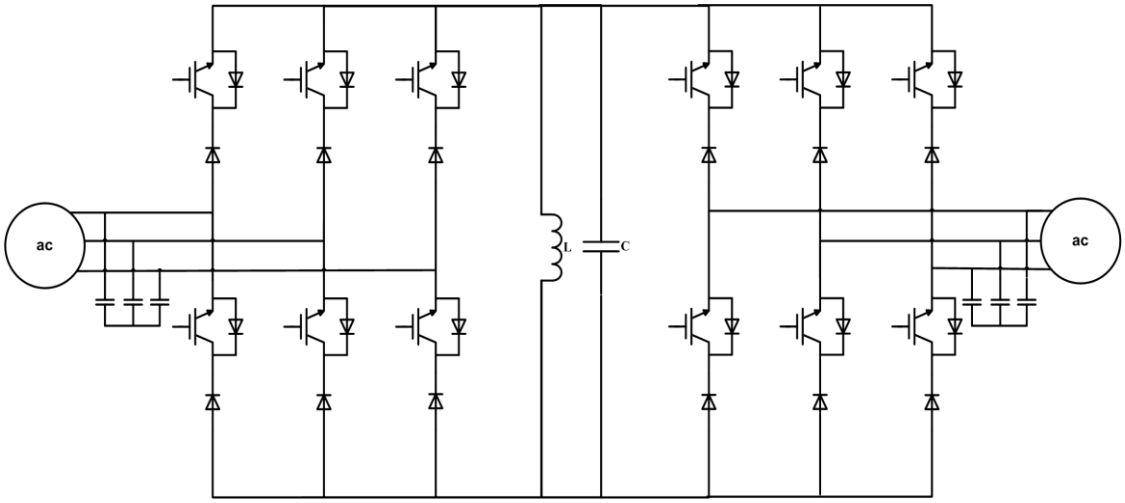


Figure 14 Soft switching ac-ac dc-link buck-boost converter [38]

2.3. Principles of Operation

To explain the principles of operation of the parallel ac-link universal power converters, a three-phase ac-ac configuration is considered. The basic operating modes and relevant waveforms of this converter are represented in Figure 15 and Figure 16. Each link cycle is divided into 16 modes, with 8 power transfer modes and 8 partial resonant modes taking place alternately. The link is energized from the input phase-pairs during modes 1, 3, 9, and 11, and is de-energized to the output phase-pairs during modes

5, 7, 13, and 15. Modes 2, 4, 6, 8, 10, 12, 14, and 16 are resonating modes. The various operating modes are explained below:

Mode 1 (Energizing): Before the start of mode 1, the input-side switches that are supposed to conduct during modes 1 and 3 are turned on (S6, S10 and S11 in Figure 15 and Figure 16); however, they do not immediately conduct because they are reverse-biased. Once the link voltage, which is resonating before mode 1, becomes equal to the maximum input line-to-line voltage that is supposed to charge the link (V_{AB} in Figure 15 and Figure 16), the proper switches (S6 and S10) become forward-biased, initiating mode 1. Therefore, the link is connected to the input phase-pair having the highest voltage via switches that charge it in the positive direction. Owing to the high frequency of the link, V_{AB} can be assumed constant during mode 1. The link current (i_{Link}) during mode 1 can be calculated using the following equations:

$$V_{AB} = L\frac{di_{Link}(t)}{dt} \tag{1}$$

$$i_{Link}(t) = \frac{1}{L}\int_0^t V_{AB}dt = \frac{V_{AB}t}{L} + i_{Link}(0) \tag{2}$$

In the above equations, L is the link inductance. During this mode, the link voltage is equal to V_{AB}, as shown in Figure 15.

The link charges until the current of phase B on the input side, when averaged over a power cycle, meets its reference value. Each link cycle contains two power cycles. It is assumed that phase A carries the maximum input current; hence, it will be involved in charging the link during both modes 1 and 3. At the end of mode 1, switch

S10 is turned off. As mentioned earlier, the link capacitor acts as a buffer across the switches during their turn-off, which results in negligible turn-off losses.

Mode 2 (Partial resonance): During this mode, none of the switches conduct and the link resonates until its voltage becomes equal to that of the other input phase-pair, which is supposed to charge the link during mode 3 (V_{AC} in Figure 15 and Figure 16). The voltage across this phase-pair is lower than the voltage across the phase-pair that charged the link during mode 1. In this mode, the circuit behaves as a simple LC circuit described by the following equations:

$$i_c(t) = -i_{Link}(t) = C\frac{dV_{Link}(t)}{dt} \tag{3}$$

$$V_{Link}(t) = L\frac{di_{Link}(t)}{dt} \tag{4}$$

In the above equations, $i_c(t)$, $V_{Link}(t)$, and C are the capacitor current, the link voltage, and the link capacitance, respectively. As the current passing through the capacitor is equal to "$-i_{Link}(t)$" and the inductor current is positive, $\frac{dV_{Link}(t)}{dt}$ is negative, implying the link voltage is decreasing.

Mode 3 (Energizing): Once the link voltage reaches the voltage across the input phase-pair AC, switches S6 and S11 are forward-biased, initiating mode 3, during which the link continues to charge in the positive direction from the input phase-pair having the second highest voltage (V_{AC}). At the end of mode 2, the link voltage is equal to V_{AC}. Hence, at the instant of switch turn-on, the voltage across the corresponding switches is zero. This implies that the turn-on occurs at zero voltage as the switches transition from reverse to forward bias. For the case shown in Figure 15, during mode 3, the link charges

until the current of phase A on the input side, averaged over a power cycle, meets its reference value. All the input switches are then turned off, initiating another resonating mode.

Mode 4 (Partial resonance): During mode 4, the behavior of the circuit is similar to that of mode 2 and the link voltage decreases until it reaches zero. At this point, the output switches that are supposed to conduct during modes 5 and 7 are activated (S19, S20, and S21 in Figure 15 and Figure 16); however, because they are reverse-biased, the switches do not conduct immediately.

The sum of the three-phase output currents (I_A, I_B, and I_C) at any instant is zero. Current of one of the three phases (for example, I_A) is highest in magnitude and of some polarity. Currents of the other two phases (for example, I_B and I_C) are of the opposite polarity to I_A. In addition, currents of phases B and C are lower in magnitude than current of phase A. As mentioned earlier, the charged link transfers power to the output by being discharged into two output phase-pairs. These two output-phase-pairs are identified as follows: One phase-pair is formed by the phases that have the highest current and the second highest current; the other phase-pair is formed by the phases that have the highest current and the lowest current. Note the currents are sorted as highest, second highest, and lowest in terms of magnitude. The phase-pair with the lower line-to-line voltage is chosen as the first pair into which the link is discharged. In Figure 15 and Figure 16, it is assumed that phase A carries the maximum output current. Once the link voltage, which is decreasing in a negative direction, reaches V_{ACO} (assuming $|V_{ACO}|$ is

lower than $|V_{ABO}|$), switches S21 and S20 will be forward-biased and will start to conduct, initiating mode 5.

***Mode 5 (De-energizing)*:** The output switches (S20 and S21) are turned on at zero voltage to allow the link to discharge into the chosen phase-pair until the current of phase C on the output side, averaged over the power cycle, meets its reference. At this point, S20 will be turned off, initiating another resonating mode.

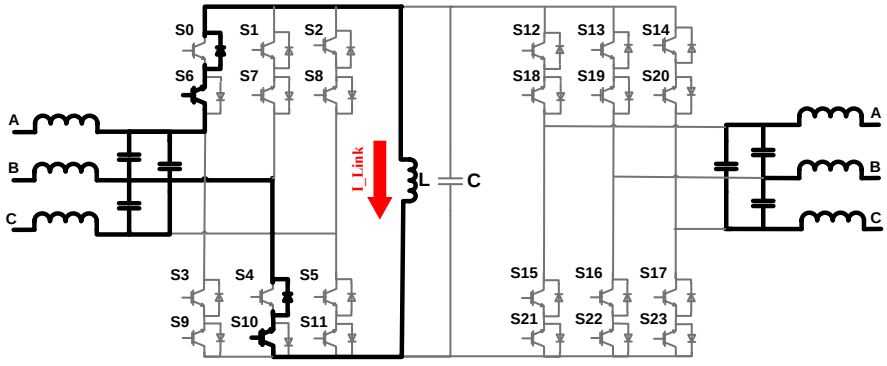
***Mode 6 (Partial resonance)*:** The link is allowed to swing to the voltage of the other output phase-pair chosen during mode 4; for the case shown in Figure 15 and Figure 16, the link voltage swings from V_{ACO} to V_{ABO}.

***Mode 7 (De-energizing)*:** During mode 7, the link is discharged into the selected output phase-pair until there is just sufficient energy left in the link to swing to a predetermined voltage (V_{max}), which is slightly higher than the maximum input and output line-to-line voltages. At the end of mode 7, all the switches are turned off allowing the link to resonate during mode 8.

***Mode 8 (Partial resonance)*:** The link voltage swings to $-V_{max}$ and then it starts to increase (because it is negative, its absolute value decreases). At this moment, the input switches that are supposed to conduct during modes 9 and 11 are turned on; however, they do not conduct immediately because they are reverse-biased. Once the absolute value of the link voltage becomes equal to $|V_{AB}|$, switches S1 and S3 will be forward-biased.

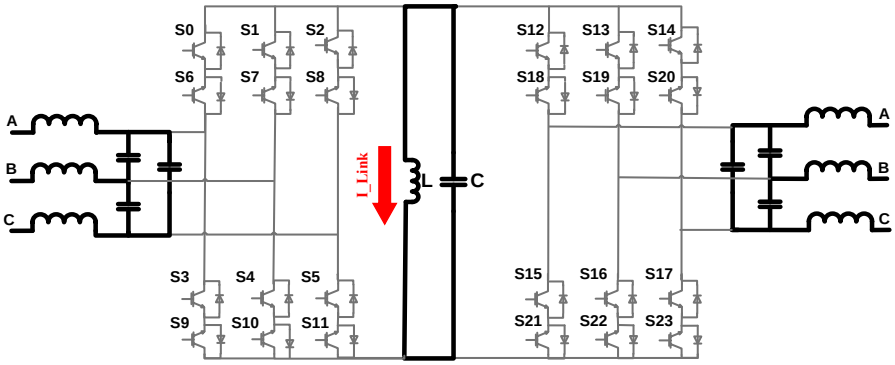
Modes 9 through 16 are similar to modes 1 through 8, except the link is charged and discharged in the reverse direction. For these modes, the complimentary switch in each leg is switched, when compared with the ones switched during modes 1 through 8.

Choosing the proper input-side switches during modes 8 and 16 is similar to choosing the proper output-side switches during modes 4 and 12. The sequence and the phase-pairs are selected in order to minimize the partial resonance times while meeting the desired harmonic levels. Therefore, first the two phase-pairs that can be involved in the energizing process must be determined. These are the phase-pairs formed by the phase with the maximum current and the two other phases. The switches connected to the input phase-pair that has the higher line-to-line voltage conduct during the first energizing mode (mode 1 or 9). Whereas, the switches connected to the output phase-pair that has the lower line-to-line voltage conduct during the first de-energizing mode (mode 5 or 13). This will result in minimized partial resonance time and guarantees the zero voltage turn-on of the switches.

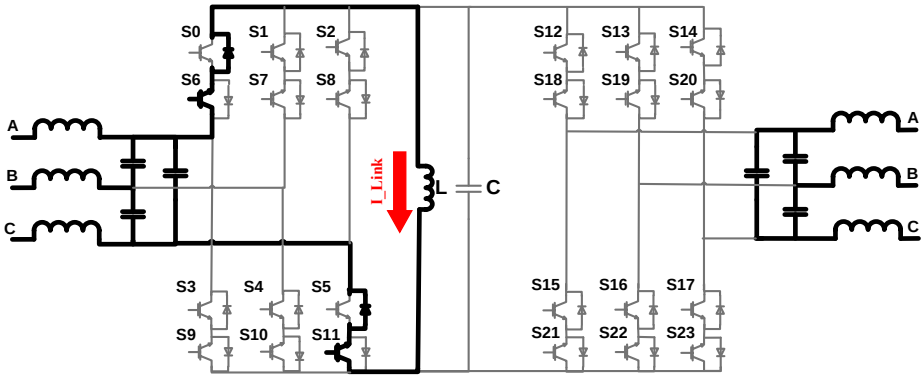


(a) Mode1

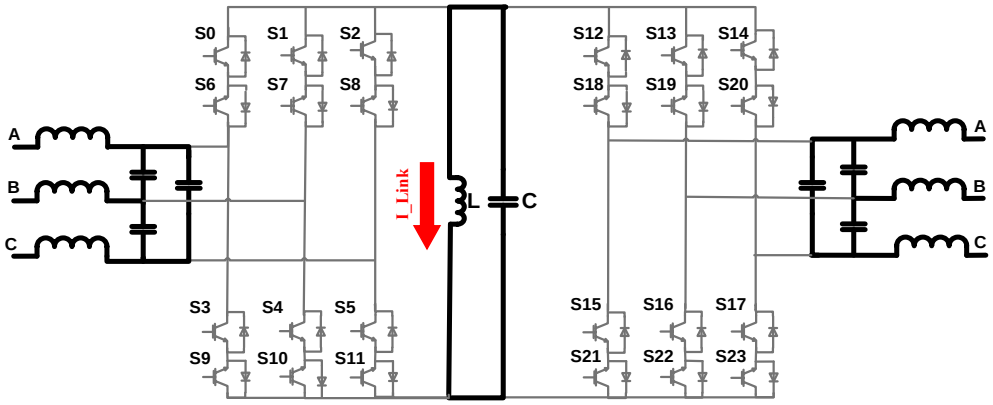
Figure 15 Circuit behavior in different modes of operation



(b) Mode 2

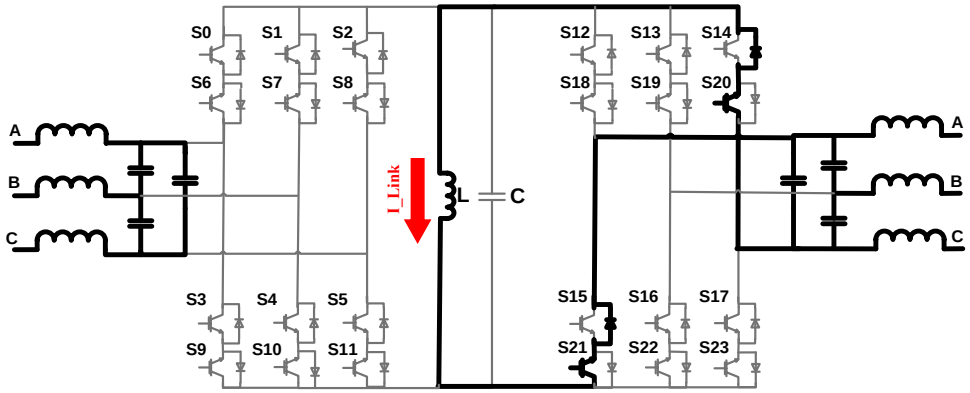


(c) Mode 3

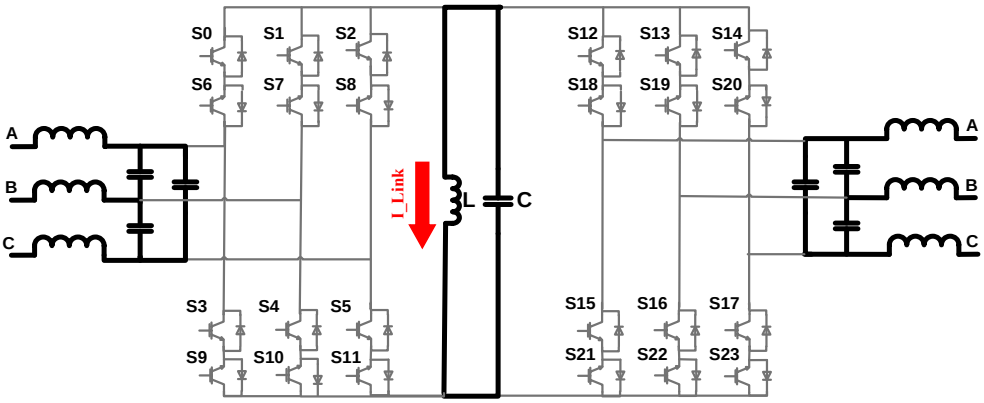


(d) Mode 4

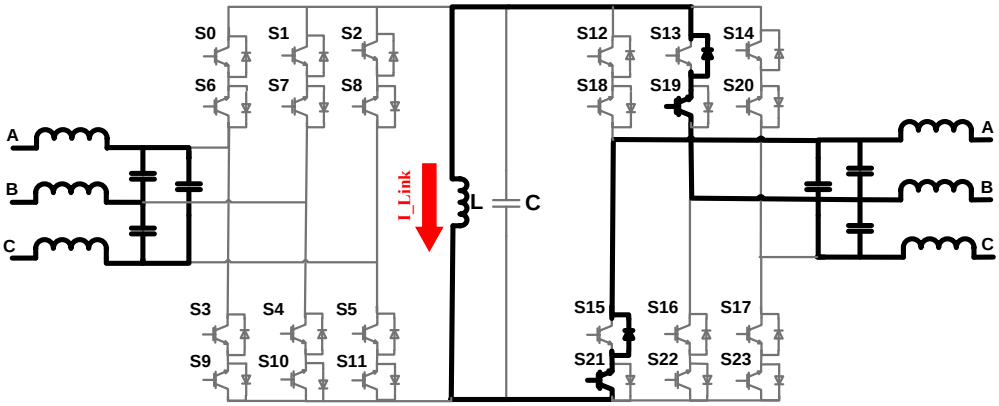
Figure 15 Continued.



(e) Mode 5

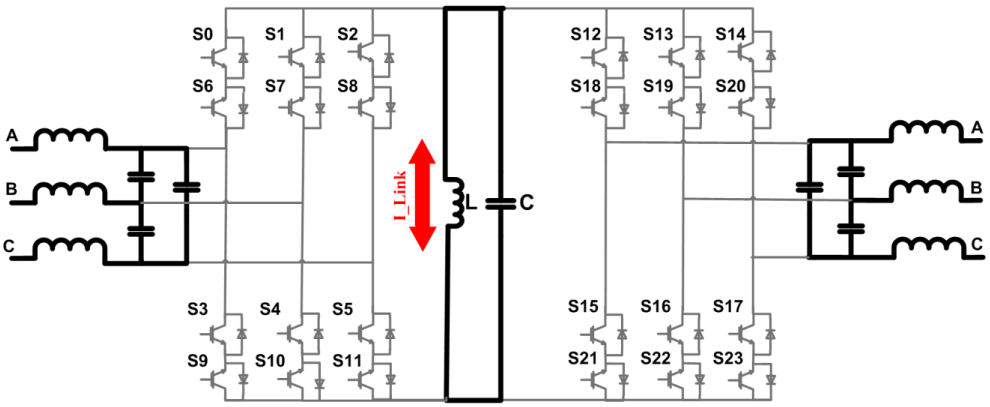


(f) Mode 6

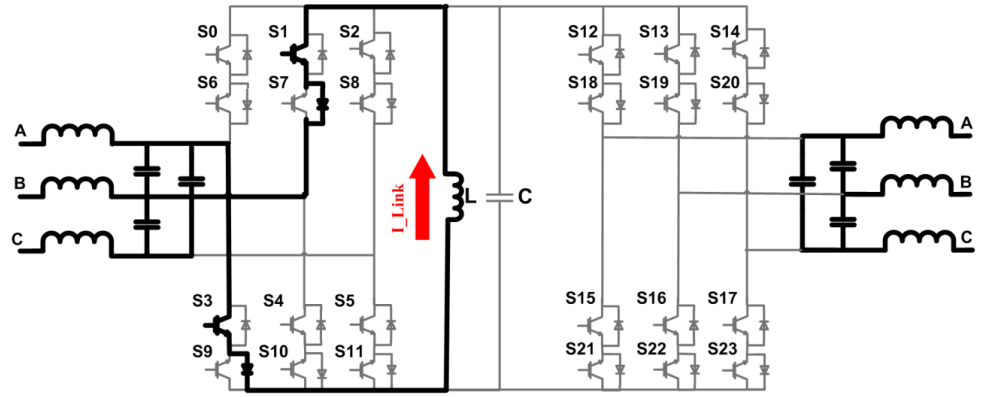


(g) Mode 7

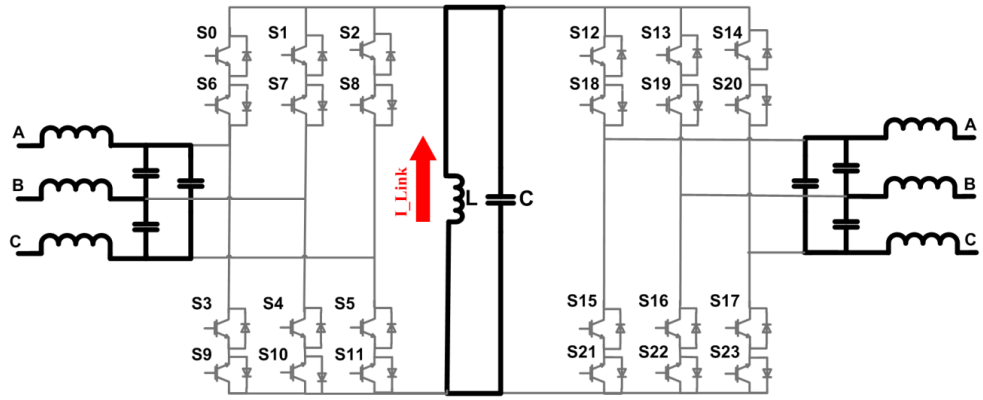
Figure 15 Continued.



(h) Mode 8

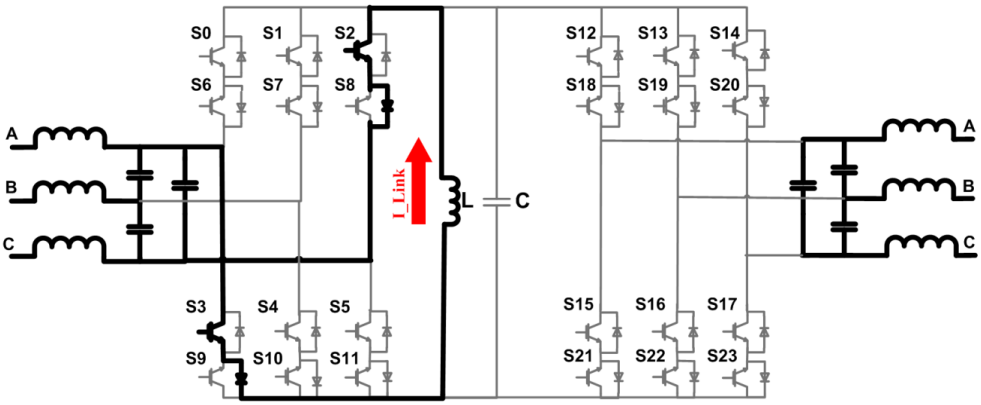


(i) Mode 9

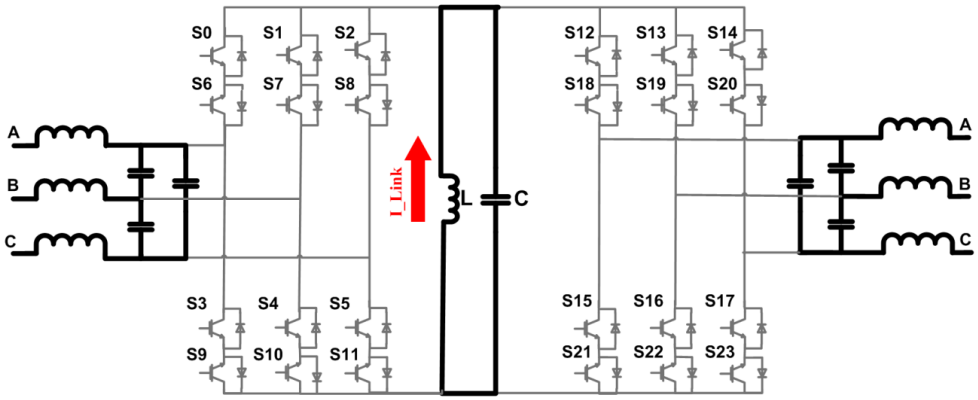


(j) Mode 10

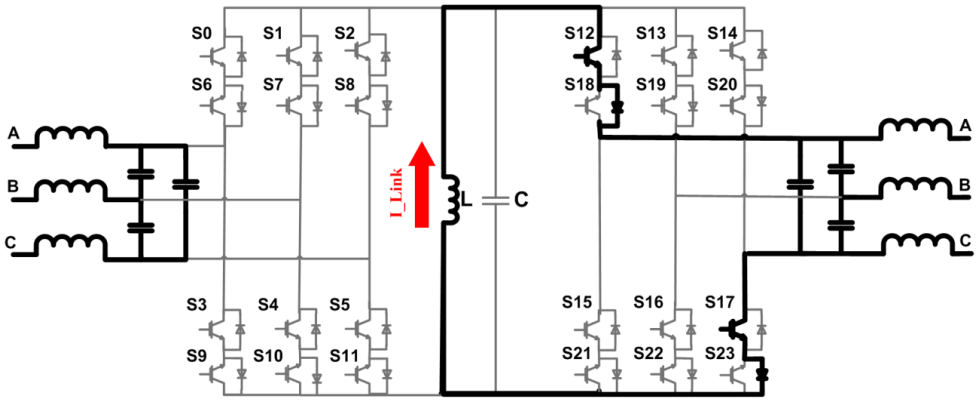
Figure 15 Continued.



(k) Mode 11

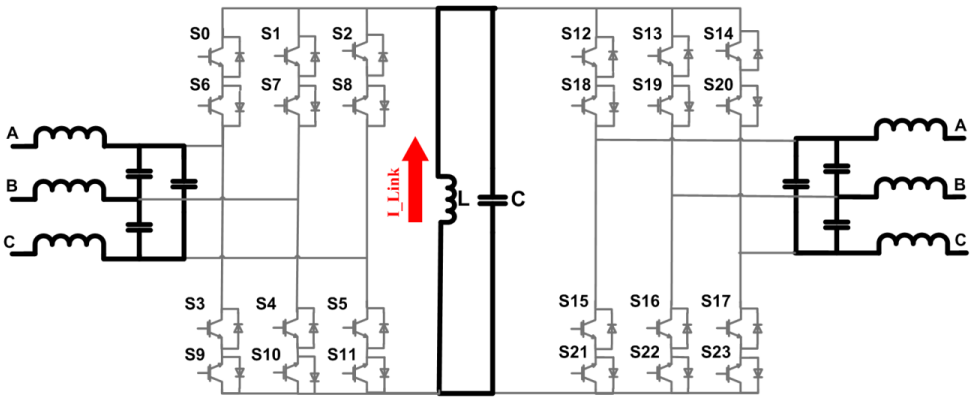


(l) Mode12

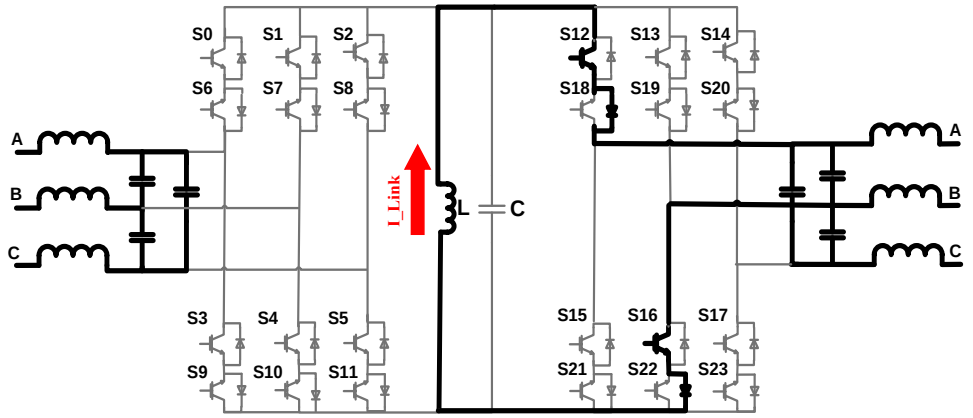


(m) Mode 13

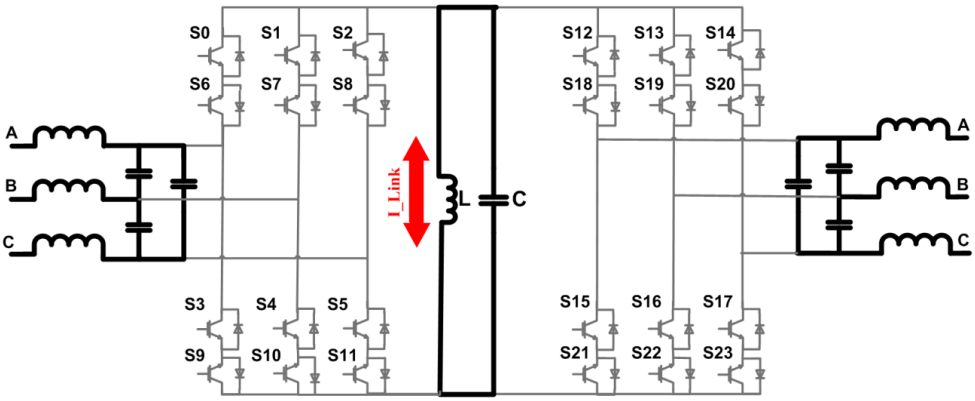
Figure 15 Continued.



(n) Mode 14



(o) Mode 15



(p) Mode 16

Figure 15 Continued.

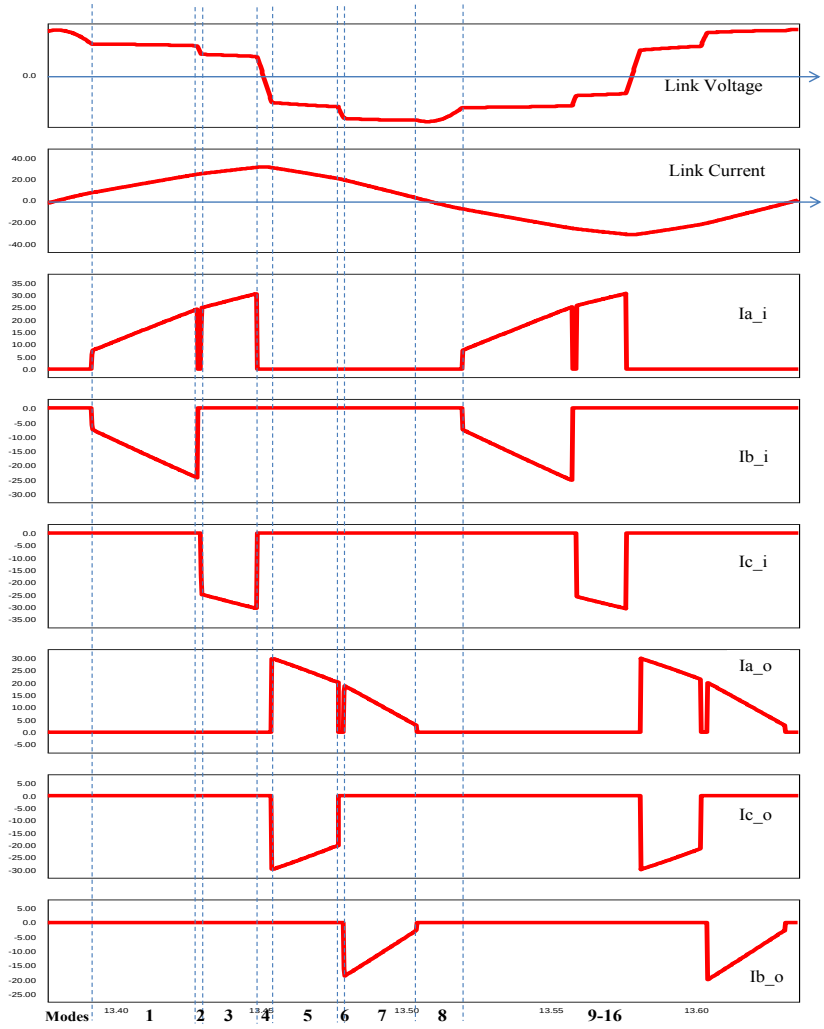


Figure 16 Voltage and current waveforms showing the behavior of the circuit during different modes of operation

As observed, the input-side and the output-side switches never conduct simultaneously, which implies that the input and output are isolated. However, if galvanic isolation is still required, a single-phase high-frequency transformer can be added to the link. In order to have a more compact converter, the transformer can be designed such that its magnetizing inductance plays the role of the link inductance, as depicted in Figure 17 [12]. In practice, the link capacitor must be split into two

capacitors that are placed at the primary and the secondary of the transformer. The principle of operation of the converter with galvanic isolation is similar to that of the original converter; therefore, it will not be studied here.

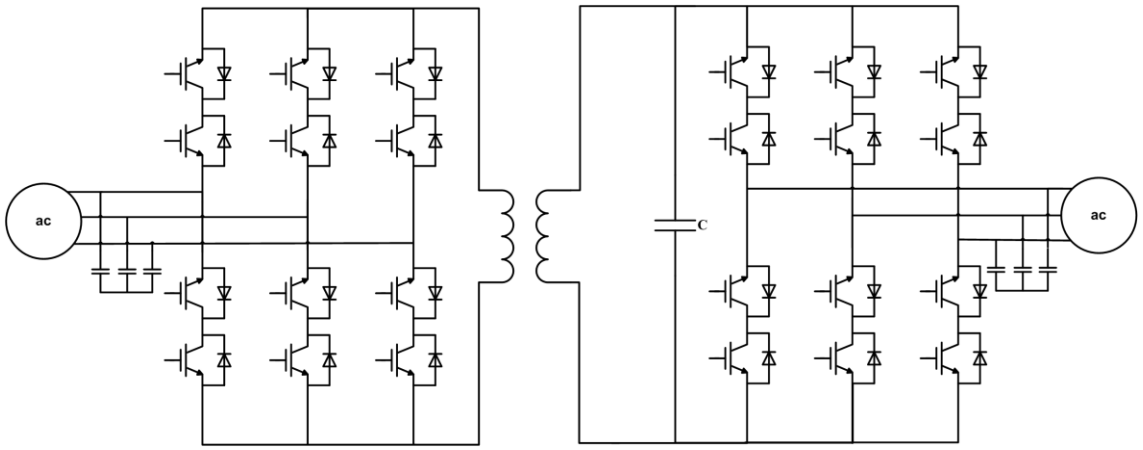


Figure 17 Parallel ac-link universal power converter with galvanic isolation

2.4. Design Procedure

To simplify the design procedure, the resonating time, which is much shorter than the power transfer time at full power, will be neglected. Moreover, charging and discharging are each assumed to take place in one equivalent mode, instead of two modes during each power cycle. For this, the link is assumed to be charged through a virtual source with the input equivalent current and voltage. In a similar manner, the link is assumed to be discharged into a virtual load with the output equivalent current and voltage. Because the phase carrying the maximum input current is involved in the energizing of the link during both modes 1 and 3 and similarly, the phase carrying the maximum output current is involved in the de-energizing of the link during both modes

5 and 7, the input and output equivalent currents in a three-phase ac-ac ac-link universal power converter can be calculated as follows:

$$I_{i-eq} = \frac{3I_{i,peak}}{\pi} \tag{5}$$

$$I_{o-eq} = \frac{3I_{o,peak}}{\pi} \tag{6}$$

where $I_{i,peak}$ and $I_{o,peak}$ are the input and output peak phase currents (filtered). It can be shown that the input and output equivalent voltages are equal to:

$$V_{i-eq} = \frac{\pi V_{i,peak}}{2}\cos\theta_i \tag{7}$$

$$V_{o-eq} = \frac{\pi V_{o,peak}}{2}\cos\theta_o \tag{8}$$

where $V_{i,peak}$, $V_{o,peak}$, $cos(\theta_i)$, and $cos(\theta_o)$ are the input peak phase voltage, output peak phase voltage, input power factor, and output power factor, respectively. It should be noted that for the dc-dc, dc-ac, or ac-dc cases, we do not need to consider any virtual sources or loads for the dc side. Design of these cases is similar to the ac-ac case, except the equivalent current and voltage of the dc side are simply the average current and voltage of that side.

Figure 18 represents one cycle of the link current. The following equations describe the behavior of the circuit during the charging and discharging of the link:

$$I_{Link,peak} = \frac{V_{i-eq}t_{charge}}{L} \tag{9}$$

$$I_{Link,peak} = \frac{V_{o-eq}t_{discharge}}{L} \tag{10}$$

In the above equations, the following parameters $I_{Link,peak}$, t_{charge}, and $t_{discharge}$ represent the peak of the link current, the total charge time during modes 1 and 3, and the total discharge time during modes 5 and 7, respectively.

Equations (9) and (10) determine the relationship between the charge time and discharge time as follows:

$$t_{charge} = \frac{V_{o-eq} t_{discharge}}{V_{i-eq}} \tag{11}$$

Consequently, the ratio of the total duration of modes 1 and 3 to the period of the link current, which is twice the sum of the charging time and discharging time, is:

$$\frac{t_{charge}}{T} = \frac{1}{2} \frac{V_{o-eq}}{V_{i-eq} + V_{o-eq}} \tag{12}$$

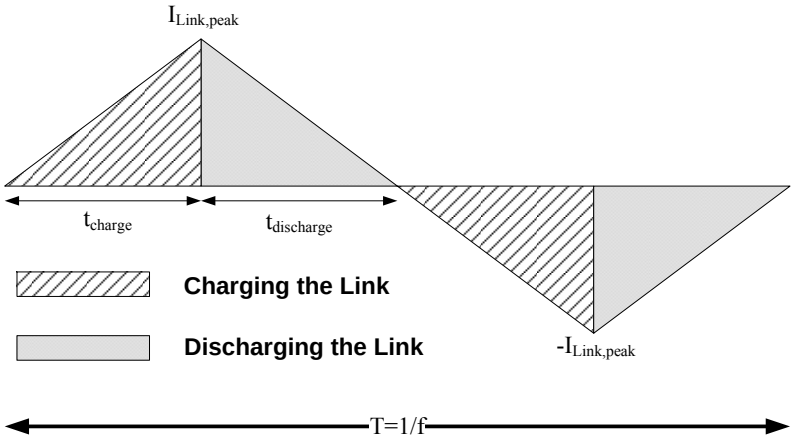


Figure 18 Link current when the resonating time is negligible

On the other hand, the equivalent input current can be calculated based on the link peak current, the energizing time, and the link current period, as follows:

$$I_{i-eq} = 2 \times \frac{1}{T} \times \frac{1}{2} \times t_{charge} \times I_{Link,peak} \tag{13}$$

Using (12) and (13) the following equation is derived for determining the link peak current:

$$I_{Link,peak} = 2 \times I_{i-eq} \times \left(1 + \frac{V_{i-eq}}{V_{o-eq}}\right) = 2 \times \left(I_{i-eq} + I_{o-eq}\right) \tag{14}$$

This implies that the peak of the filtered input and output currents determine the link peak current. The frequency of the link at full power, *f*, can be chosen based on the power rating of the system and the characteristics of the available switches. Once the link frequency is chosen, the following equation determines the inductance of the link:

$$L = \frac{P}{f\left(I_{Link,peak}^2\right)} \tag{15}$$

where P is the rated power. Figure 19 shows the relationship between the link frequency and link inductance. It is observed that choosing a higher link frequency results in a lower link inductance.

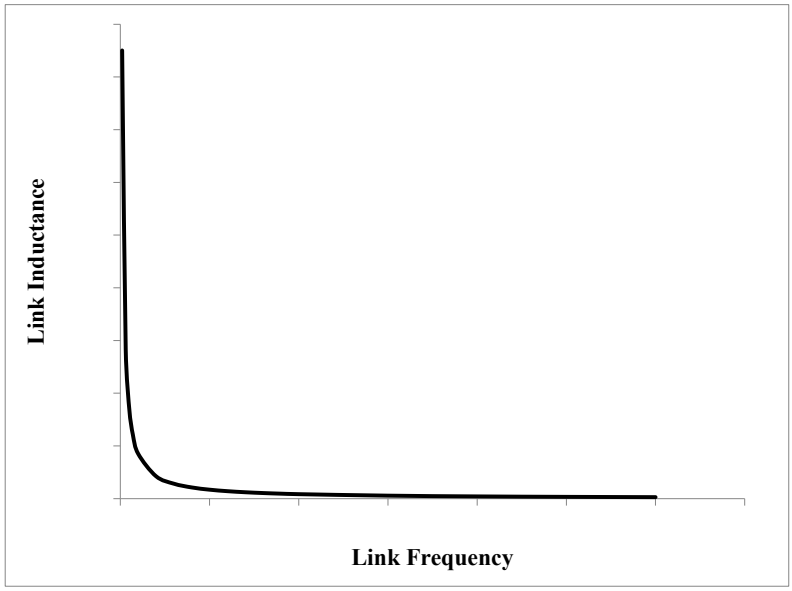


Figure 19 Link inductance vs. link frequency

Link capacitance is chosen such that the resonating periods are retained within a small percentage of the link cycle:

$$\frac{1}{2\pi\sqrt{LC}} \gg f \tag{16}$$

Since no power is transferred during the resonating modes, it is preferred to keep these modes as short as possible.

In order to design the converter, the current and voltage rating of the switches must be determined, as well. It can be shown that the maximum voltage each switch on the input-side switch bridge tolerates is:

$$V_{SW-Input} = \frac{1}{2}V_{\max} + V_{i,peak} \tag{17}$$

where V_{max} is the maximum link voltage. Similarly the maximum voltage each switch on output-side switch bridge tolerates is:

$$V_{SW-Output} = \frac{1}{2}V_{\max} + V_{o,peak} \tag{18}$$

The maximum voltage the switches block in this converter is slightly higher than that of the dc-link converter.

The peak current of each switch in this converter is equal to the link peak current and the average current of the input and output switches are as follows:

$$I_{SW-Input} = \frac{1}{2\pi}I_{i,peak} \tag{19}$$

$$I_{SW-Output} = \frac{1}{2\pi}I_{o,peak} \tag{20}$$

Therefore, the average current of the switches in this converter are half the average current of the switches in the dc-link converter.

2.5. Analysis

As mentioned earlier, the resonating time is normally negligible at full power. However, at lower power levels, the power transfer time (energizing and de-energizing time) is usually shorter than the power transfer time at full power, whereas the resonating time is almost constant. Therefore, the resonating time cannot be neglected at lower power levels. Figure 20 shows the link voltage and current over one cycle, assuming the resonating time is not negligible.

If the resonating time is negligible, then (14) and (15) may be used to calculate the link peak current and the link frequency at different power levels. However, when the resonating time cannot be neglected, the analysis will become more complicated.

Considering the principles of operation, the link current at the end of the de-energizing mode (I_4) can be calculated by:

$$I_4 = \sqrt{\frac{C}{L}\left(V_{max}^2 - V_{o,eq}^2\right)} \tag{21}$$

Solving the resonant LC circuit during the time period t_1 (resonating time after the de-energizing mode and before the energizing mode), I_1 (Link current at the beginning of the energizing mode) and t_1 can be calculated as follows:

$$I_1 = \sqrt{\left(I_4^2 + \left(\frac{V_{o,eq}}{L\omega_r}\right)^2 - \left(\frac{V_{i,eq}}{L\omega_r}\right)^2\right)} \tag{22}$$

$$t_1 = \frac{1}{\omega_r}\left(\pi + \tan^{-1}\left(\frac{I_1 L\omega_r}{V_{i,eq}}\right) - \pi + \tan^{-1}\left(\frac{I_4 L\omega_r}{V_{o,eq}}\right)\right) = \frac{1}{\omega_r}\left(\tan^{-1}\left(\frac{I_1 L\omega_r}{V_{i,eq}}\right) + \tan^{-1}\left(\frac{I_4 L\omega_r}{V_{o,eq}}\right)\right) \quad (23)$$

In the above equations, ω_r is the resonant angular frequency, which can be calculated by:

$$\omega_r = \frac{1}{\sqrt{LC}} \quad (24)$$

In order to find the link peak current and the link frequency, the current at the end of the energizing mode (I_2), the current at the beginning of the de-energizing mode (I_3), the resonating time after the energizing mode and before the de-energizing mode (t_2), and the total energizing and de-energizing time should be determined first. Five other equations should be solved in order to determine I_2, I_3, t_2, t_{charge}, and $t_{discharge}$. These equations are as follows:

$$V_{i,eq} = L\frac{I_2 - I_1}{t_{charge}} \quad (25)$$

$$V_{o,eq} = L\frac{I_3 - I_4}{t_{discharge}} \quad (26)$$

$$I_{i,eq} = \frac{t_{charge}}{2(t_{charge}+t_{discharge}+t_1+t_2)}(I_2+I_1) \quad (27)$$

$$I_{o,eq} = \frac{t_{discharge}}{2(t_{charge}+t_{discharge}+t_1+t_2)}(I_3+I_4) \quad (28)$$

$$t_2 = \frac{1}{\omega_r}\left(\pi - \tan^{-1}\left(\frac{I_3 L\omega_r}{V_{o,eq}}\right) - \tan^{-1}\left(\frac{I_2 L\omega_r}{V_{i,eq}}\right)\right) \quad (29)$$

Once these equations are solved, $I_{Link,peak}$ and f can be calculated as follows:

$$I_{Link,peak} = \sqrt{\left(I_2^2 + \left(\frac{V_{i,eq}}{L\omega_r}\right)^2\right)} \quad (30)$$

$$f = \frac{1}{2(t_{charge}+t_{discharge}+t_1+t_2)} \quad (31)$$

It can be shown that by decreasing the power level, the link peak current decreases, whereas the link frequency increases. It should be noted that in this converter the maximum link frequency, which occurs at zero power, is equal to the resonant frequency. Figure 21 and Figure 22 represent the link peak current and the link frequency variations vs. power, respectively.

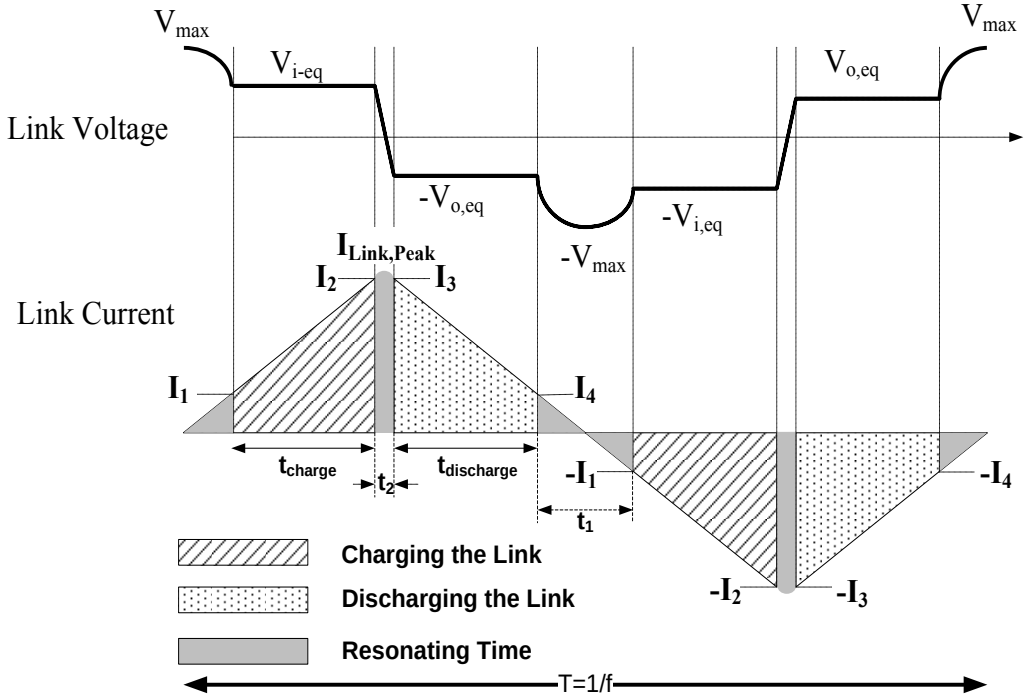


Figure 20 Link voltage and current when resonating time is not negligible

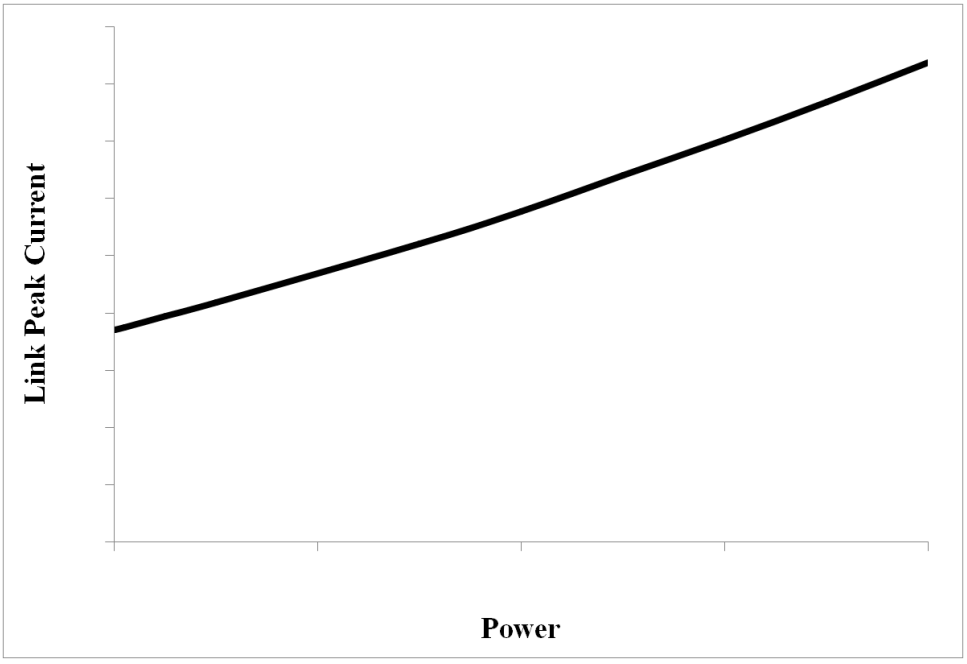


Figure 21 Link peak current variations vs. power

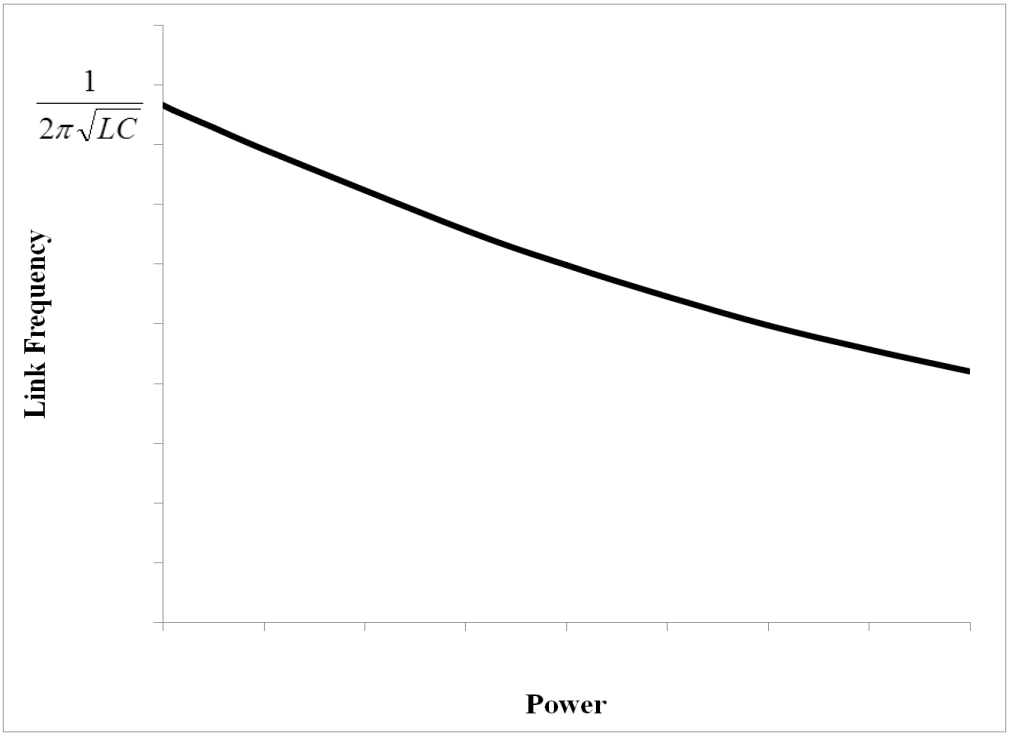


Figure 22 Link frequency variations vs. power

2.6. Low Voltage Ride Through (LVRT)

Another important issue to study is the behavior of the parallel ac-link universal converter during the grid fault. Although this converter does not have a dc link, it can inject reactive power into the grid during the voltage sags. The principles of operation of the converter during the grid fault are slightly different than that of the normal operation. For the dc-ac configuration the principles of operation during a voltage dip are as follows:

During mode 1, the link will be charged through the dc source up to a certain level. Then, similar to the normal operation, it will be discharged into the output phases; however, no net energy is taken from the link in this case. The second discharging mode is over once the current of the output phase having maximum current meets its reference. After the output-side switches are turned off, the energy remained in the link inductor is discharged into the input. In this case, the dc-side filter capacitor absorbs the energy discharged into the input. Once the link is completely discharged, it will be re-charged from the dc source with current flowing in the opposite direction.

This method of control can also be used for normal operation to control the currents of two output phases instead of one phase. In the case of normal operation, the energy remained in the link after turning off the output-side switches, which must be discharged into the dc-side capacitor, is much lower than that of the low-voltage case.

For an ac-ac configuration, the principles of operation during the low-voltage fault are similar to those of the dc-ac configuration, except both energizing from the input and de-energizing to the input are split into two modes. The same phase-pairs

involved in charging of the link will be charged from the link. The behavior of the circuit at different modes along with the unfiltered phase currents are shown in Figure 23.

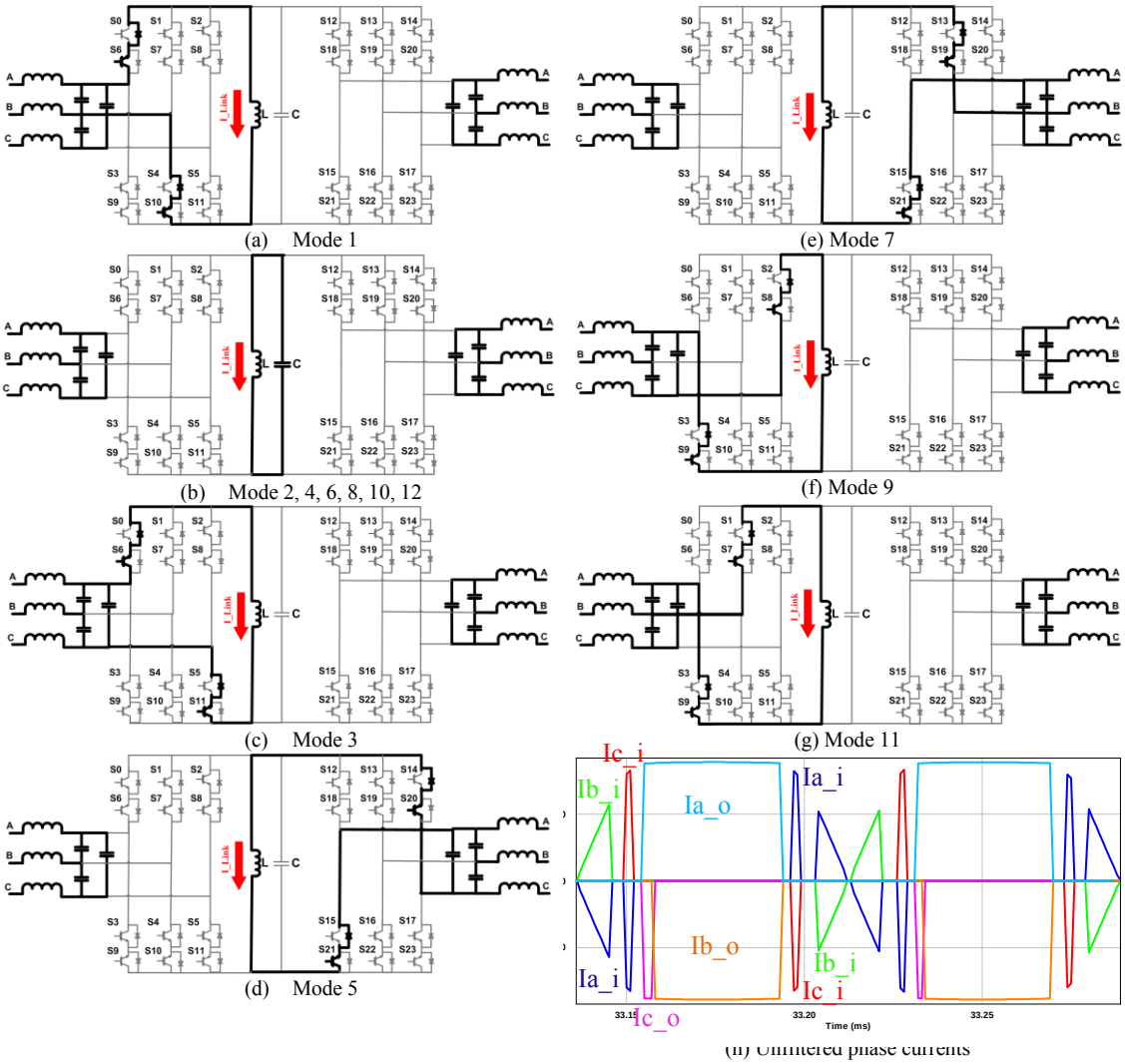


Figure 23 Different modes of operation in the ac-ac parallel ac-link universal converter during a voltage drop

2.7. Load Power Factor Limitation and an Improved Control Algorithm

For the case shown in Figure 15 and Figure 16, the reference currents of the output phases A, B, and C are positive, negative, and negative, respectively. During modes 1–8 the link current is positive. The positive direction in the link is defined from

top to bottom and the positive direction in the output phases is defined from left to right. In this converter the currents are regulated such that they meet their references. Therefore, during mode 4, the output-side switches are turned on such that the unfiltered currents formed during modes 5 and 7 have the same direction as their references. Considering the polarity of the output current references and the link current, for the case shown in Figure 15 and Figure 16 switches S19, S20, and S21 are turned on. In these figures the line-to-line voltages that will be seen across the link during modes 5 and 7 are both negative, which result in discharging the link inductor. However, if the output power factor is lower than a certain value, the line-to-line voltages seen across the link may be positive. In this case if the output line-to-line voltages are lower than the input line-to-line voltages, we still may have soft switching, assuming the delay of the microcontroller is short and the output-side switches are turned on at the end of mode 3. However, if the output line-to-line voltage seen across the link during mode 5 is higher than the input line-to-line voltage seen across the link during mode 3, the output-side switches will not be turned on at zero voltage. In this case once the incoming switches are turned on they are forward-biased and the link voltage changes instantaneously. This results in the hard switching of the switches, which is not desirable in this converter.

To find the condition that results in hard switching, first the minimum link voltage during mode 3 must be estimated. If the input-side power factor is unity, the minimum voltage across the link during mode 3 is as follows:

$$V_{ll\_in\_min} = \frac{\sqrt{3}V_{i,peak}}{2} \tag{32}$$

where $V_{i,peak}$, is the input peak voltage. The output currents and voltages are as follows:

$$I_{a\_o} = I_m \sin(\omega t + \theta_o) \tag{33}$$

$$I_{b\_o} = I_m \sin\left(\omega t + \theta_o - \frac{2\pi}{3}\right) \tag{34}$$

$$I_{c\_o} = I_m \sin\left(\omega t + \theta_o - \frac{4\pi}{3}\right) \tag{35}$$

$$V_{a\_o} = V_{o,peak} \sin(\omega t) \tag{36}$$

$$V_{b\_o} = V_{o,peak} \sin\left(\omega t - \frac{2\pi}{3}\right) \tag{37}$$

$$V_{c\_o} = V_{o,peak} \sin\left(\omega t - \frac{4\pi}{3}\right) \tag{38}$$

In the above equations $V_{o,peak}$, I_m and θ_o are the output voltage amplitude, amplitude of the fundamental component of the unfiltered output current, and the phase shift between the output voltage and the unfiltered current, respectively. The line-to-line voltages seen across the link during modes 5 and 7 for the case shown in Figure 15 and Figure 16 are as follows:

$$V_{ba\_o} = -\sqrt{3} V_{o,peak} \cos\left(\omega t - \frac{\pi}{3}\right) \tag{39}$$

$$V_{ca\_o} = -\sqrt{3} V_{o,peak} \cos\left(\omega t - \frac{2\pi}{3}\right) \tag{40}$$

To satisfy soft switching, the following conditions should be valid:

$$V_{ba\_o} < V_{ll\_in\_min} \tag{41}$$

$$V_{ca\_o} < V_{ll\_in\_min} \tag{42}$$

which can be expressed as follows:

$$-\sqrt{3} V_{o,peak} \cos\left(\omega t - \frac{\pi}{3}\right) < \frac{\sqrt{3} V_{i,peak}}{2} \tag{43}$$

$$-\sqrt{3} V_{o,peak} \cos\left(\omega t - \frac{2\pi}{3}\right) < \frac{\sqrt{3} V_{i,peak}}{2} \tag{44}$$

On the other hand, for the case that the current of phase A is positive (and maximum) and the currents of phases B and C are negative, $\omega t+\theta_o$ varies between $\frac{\pi}{3}$ and $\frac{2\pi}{3}$. Hence, it can be shown that to guarantee soft switching of the output-side switches, the following condition should be met:

$$\frac{\pi}{3}+\theta_o < \omega t < \frac{2\pi}{3}+\theta_o \quad \& \quad -\frac{1}{2}\frac{V_{i,peak}}{V_{o,peak}} < \cos\left(\omega t-\frac{\pi}{3}\right) \tag{45}$$

Or in other words:

$$-\frac{1}{2}\frac{V_{i,peak}}{V_{o,peak}} < \cos\left(\theta_o+\frac{\pi}{3}\right) \tag{46}$$

In the above equations I_{a_o}, I_{b_o}, and I_{c_o} are the fundamental components of the unfiltered output currents, or in other words the references of the unfiltered output currents. If the references of the filtered currents are given, the peak and the phase shift of the unfiltered currents, (I_m and θ_o) can be calculated from the peak and the phase shift of the filtered currents (I_{mf} and θ_{of}) as follows:

$$I_m = \sqrt{\left(I_{mf}\cos\theta_{of}\right)^2+\left(I_{mf}\cos\theta_{of}-V_{o,peak}C_f\omega\right)^2} \tag{47}$$

$$\theta_o = \tan^{-1}\left(\frac{I_{mf}\cos\theta_{of}-V_{o,peak}C_f\omega}{I_{mf}\sin\theta_{of}}\right) \tag{48}$$

In the above equations C_f is the output filter capacitance. In order to extend the load power factor range, an improved control scheme is proposed in this section. This method is very similar to the previous control method, except the input-side and the output-side switches are all turned on at the same time; this approach allows the proper switches to conduct as they become forward-biased regardless of being placed at the input side or at the output side. Therefore, the switches at the output side might conduct

during modes 1 or 3 if the load power factor is low. Figure 24 represents the waveforms employing this control method in case of a low power factor. As seen in this figure, during mode 1, the output phase-pair “ab” charges the link, and during modes 3 and 5 the input phase-pairs charge the link. Finally, the link is discharged into the output phase-pair “bc” during mode 7.

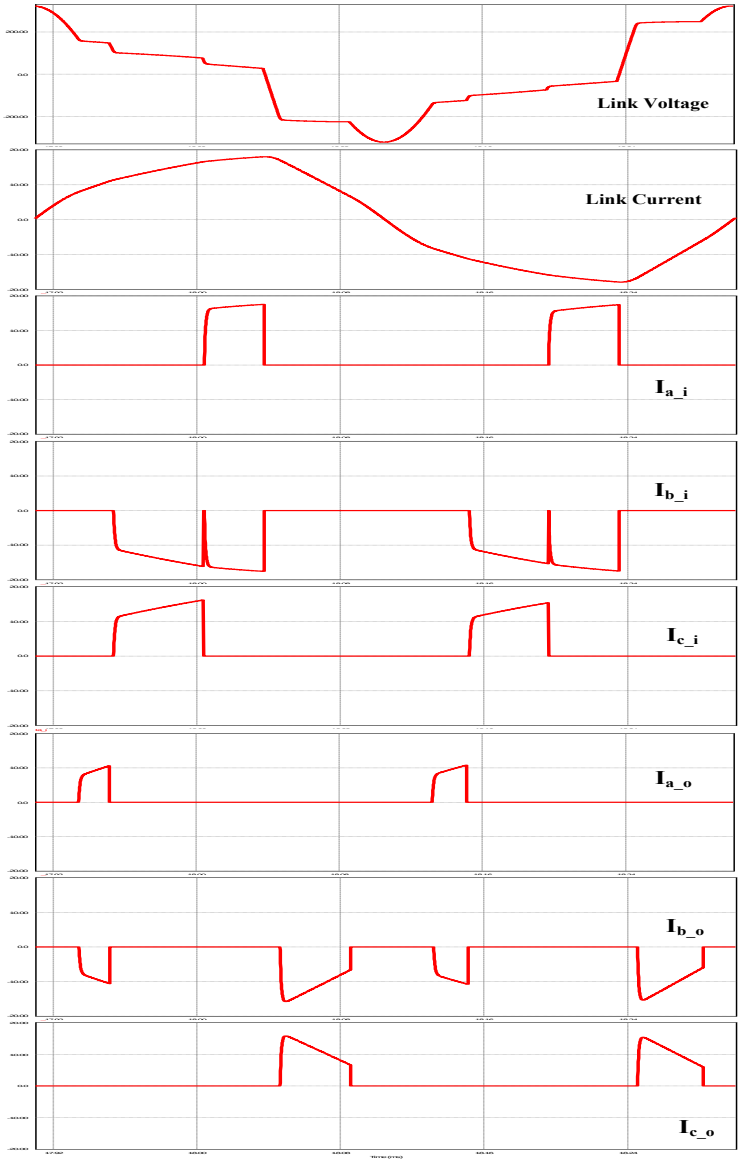


Figure 24 Link voltage, link current, and unfiltered input/output currents with the improved control algorithm

2.8. Hybrid Parallel AC-Link Universal Power Converter

As mentioned earlier, the parallel ac-link universal power converters are an excellent candidate for renewable energy systems. However, renewable energy sources are usually intermittent in nature. Therefore, it is not practical to rely on one source of renewable energy. Usually, energy storage is employed along with PV arrays or wind turbines. Considering the necessity of using more than one source of energy, it is essential to investigate the power electronics required for hybrid energy systems. One solution is to use two (or more) separate power converters. A more efficient and more reliable method is to use a hybrid (multi-port) converter to interface several energy sources and the grid. A good example for such systems is a hybrid PV/battery inverter. In this section, we will focus on this example to show the possibility of extending the number of inputs or outputs of the parallel ac-link universal power converter. Of course, any combination of dc, ac, single phase and multi-phase sources and loads may interface in the hybrid converter.

Two common inverter configurations exist for hybrid PV/battery systems. The first system is formed by a hybrid inverter that consists of two inverters operating in parallel, whose outputs are tied to the grid through a multi-winding, step-up transformer [9]. The main drawback of this scheme is that a low-frequency, and thus bulky, transformer is required [9, 39-42]. The other configuration is a multi-input dc–dc converter with an additional dc/ac inverter stage for feeding the ac loads. This configuration offers high boosting capability and galvanic isolation; however, it consists

of multiple power processing stages [9]. Moreover, electrolytic capacitors are required at the dc link.

In this section the hybrid parallel ac-link universal converter interfacing the PV modules, the battery, and the load is proposed. This single-stage converter overcomes the above mentioned problems associated with the currently available hybrid PV/battery inverters.

Figure 25 represents the schematic of the proposed converter. There are three switch bridges in this configuration: one bridge connected to the PV modules; a second bridge connected to the battery; and a third bridge connected to the load. As seen in Figure 25, the PV switch bridge contains only unidirectional switches, while the battery switch bridge contains bi-directional switches to allow bi-directional flow of power. Since PV cells cannot absorb electrical energy, the corresponding switch bridge is formed by unidirectional switches.

Depending on the power generated by the PV modules, the battery State Of Charge (SOC), and the load requirements, there are four possible power flow scenarios in this converter, i.e. power flow

1. From the PV modules to the load
2. From the battery to the load
3. From the PV modules to the load and the battery
4. From the PV modules and the battery to the load

If the grid-connected configuration is considered, there will be another scenario in which power flows from the grid to the battery. Here the stand-alone application is

considered. Similar to the dc-ac configuration, the hybrid converter transfers power entirely through the link inductor. Again, the link is charged through the input phases and then discharged into the output phases. Between each charging and discharging there is a resonating mode. Depending on the power-flow scenario, there might be more than one input phase-pair to charge the link (fourth power flow scenario) or more than one output phase-pair to which the link is discharged. Therefore, the link charging or discharging mode can be split into two or more modes.

Figure 26, Figure 27, and Figure 28 represent one cycle of the link current in each power-flow scenario. In the first and second power-flow scenarios, the converter behaves as an inverter. In this case the link cycle is divided into 12 modes, with 6 power transfer modes and 6 resonating modes. The link is energized from the battery (in the second power flow scenario) or PV modules (in the first power flow scenario) during modes 1 and 7 and is de-energized into the load during modes 3, 5, 9 and 11. Modes 2, 4, 6, 8, 10, and 12 are the resonating modes.

In the third power-flow scenario, the converter converts dc to three-phase ac and dc (dc/ac+dc). In this scenario, the link cycle is divided into 16 modes, with 8 power transfer modes and 8 resonating modes. The link is energized from the PV during modes 1 and 9 and is de-energized to the load and the battery during modes 3, 5, 7, 11, 13 and 15.

In the fourth power-flow scenario, power flows from two dc sources to a three-phase ac load (dc+dc/ac). In this case, the link cycle is divided into 16 modes including 8 power transfer modes and 8 resonating modes. The link is energized from the PV and the

battery during modes 1, 3, 9 and 11 and is de-energized into the load during modes 5, 7, 13 and 15.

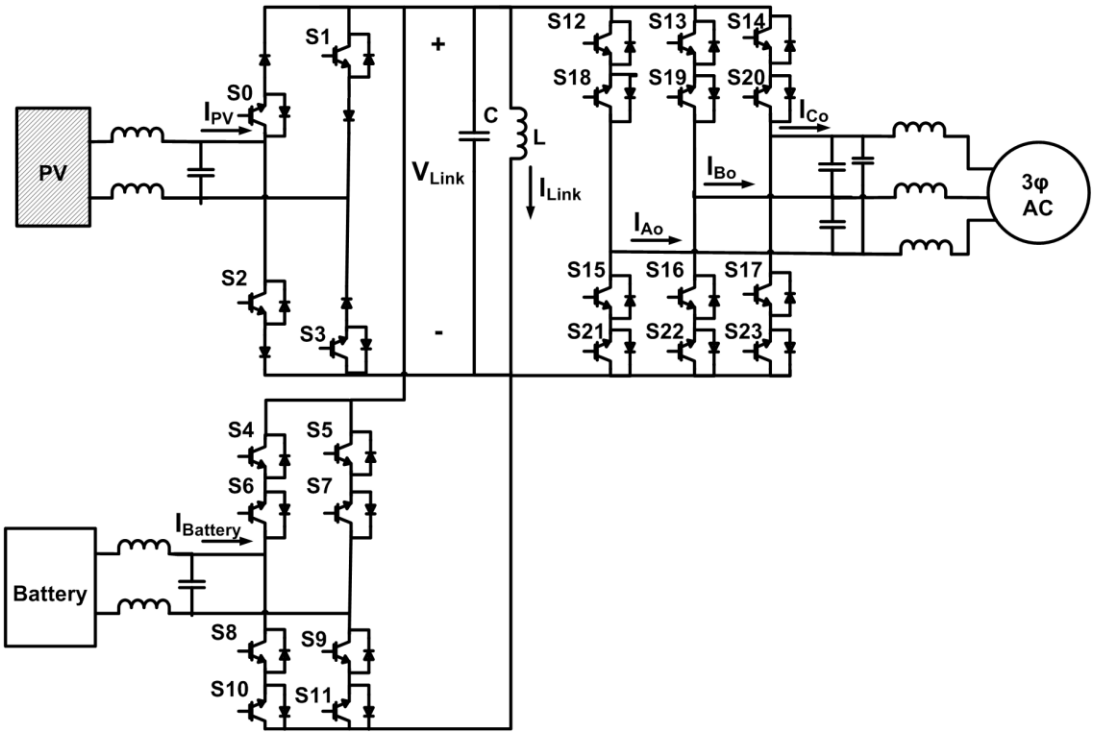


Figure 25 Hybrid parallel ac-link universal power converter interfacing PV, battery, and a three-phase load

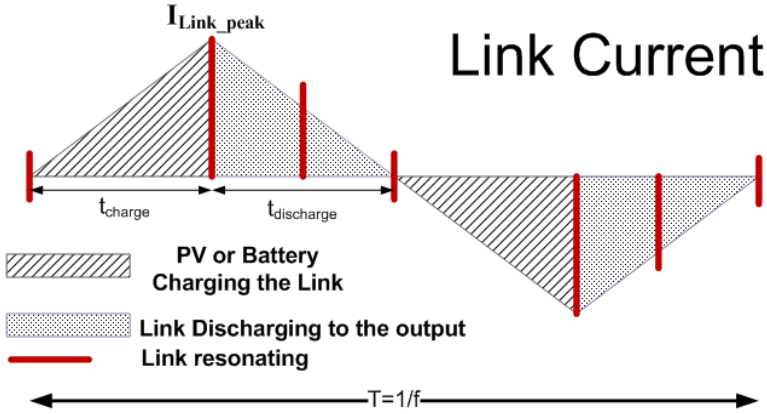


Figure 26 Link current of the hybrid inverter during the first and second power-flow scenarios

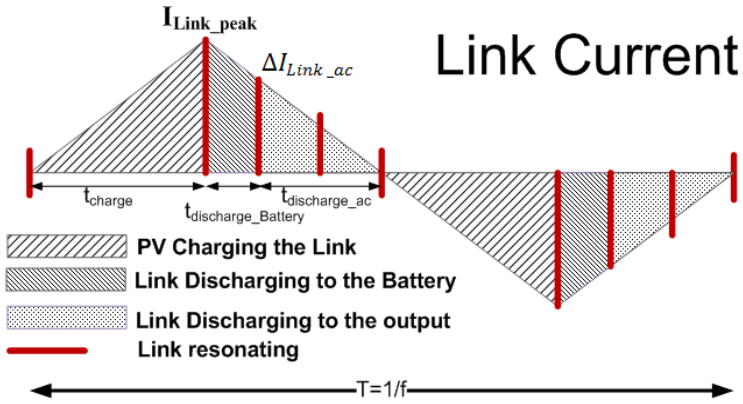


Figure 27 Link current of the hybrid inverter during the third power flow

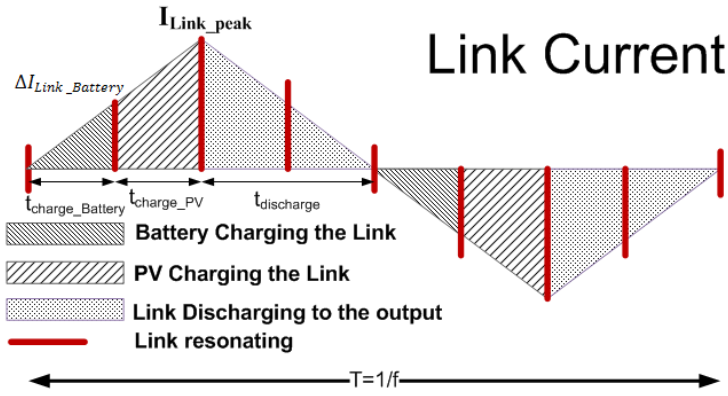


Figure 28 Link current of the hybrid inverter during the fourth power-flow scenario

Section 2.3 studied in detail different modes of operation in the single-input/single-output ac-link universal power converter. Therefore, the first and the second power-flow scenarios, which are simple dc-ac cases, will not be discussed here. Only the third and the fourth power-flow scenarios will be explained. The basic operating modes and the relevant waveforms of these two cases are represented in Figure 29 and Figure 30, respectively.

2.8.1. Principles of Operation & Analysis for the Third Power Flow Scenario (PV to the Battery and the Load)

Various modes of operation in the third power-flow scenario, which is from the PV toward the battery and the load, are as follows:

Mode 1 (Energizing): Before the start of mode 1, proper switches on the PV switch bridge which are supposed to conduct during mode 1, are turned on (S0 and S3 in Figure 29 and Figure 30). However, they do not immediately conduct, since they are reverse-biased. Once the link voltage, which is resonating before mode 1, becomes equal to the voltage across the PV modules, proper switches (S0 and S3) are forward-biased, thereby initiating mode 1. This results in zero voltage turn on of S0 and S3. During this mode, the link voltage is equal to the PV voltage, as shown in Figure 30.

The link is charged until the PV current, averaged over a power cycle time, meets its reference value. Switches located on the PV switch bridge are then turned off.

Mode 2 (Partial resonance): During this mode, none of the switches conduct and the link resonates. The link voltage decreases and once it becomes negative, the battery and load phase-pairs may be sorted by voltage absolute value. The one with minimum absolute value will be charged first (in mode 3). The one having the second highest value will be charged in mode 5. The one having the maximum value will be charged in mode 7. As discussed earlier, in a three-phase system, only two phase-pairs can provide paths for the current. One phase-pair is formed by the phase having the highest current and the phase having the second highest current. The second phase-pair is formed by the phase having the highest current and the phase having the lowest current. In this model,

the currents are identified as highest, second highest, and lowest in terms of magnitude alone. During mode 2 proper switches which are supposed to conduct during modes 3, 5 and 7 are turned on (switches S10, S7, S18, S22 and S23 in Figure 29 and Figure 30). However, they do not immediately conduct, as they are reverse-biased. In Figure 29 and Figure 30, it is assumed that the link will be discharged into the battery, V_{ABO} and V_{ACO} during modes 3, 5 and 7, respectively.

Mode 3 (De-energizing): Once the absolute value of the link voltage is equal to the voltage across the battery, switches S10 and S7 are forward-biased and initiate mode 3, during which the link is discharged into the battery. S10 and S7 are turned on at zero voltage to allow the link to be discharged to the battery until the battery current averaged over a power cycle time meets its reference. At this point S10 and S7 will be turned off and initiate another resonating mode.

Mode 4 (Partial resonance): During mode 4, the link voltage decreases. When it reaches V_{ABO} (Assuming phase A carries the maximum ac-side current and $|V_{ABO}|$ is lower than $|V_{ACO}|$), switches S18 and S22 will be forward-biased; they start to conduct and initiate mode 5.

Mode 5 (De-energizing): The output switches (S18 and S22) are turned on at zero voltage to allow the link to be discharged to the chosen phase-pair until the current of phase B averaged over a power cycle time meets its reference. At this point, S22 will be turned off and initiate another resonating mode.

Mode 6 (Partial resonance): the link is allowed to swing to the voltage of the other output phase-pair chosen during Mode 2. For the case shown in Figure 29 and Figure 30 the link voltage swings from V_{ABO} to V_{ACO}.

Mode 7 (De-energizing): During mode 7, the link discharges into the selected output phase-pair until there is just sufficient energy left in the link to swing to a predetermined voltage (V_{max}). At the end of mode 7 all the switches are turned off allowing the link to resonate during mode 8.

Mode 8 (Partial resonance): The link voltage swings to $-V_{max}$ and then its absolute value starts to decrease.

Modes 9-16 are similar to modes 1- 8, except the link charges and discharges in the reverse direction. For these modes, the complimentary switch on each leg is switched, when compared to the ones switched during modes 1 through 8.

Similar to the single-input/single-output configuration, it is important to find the link peak current and the link frequency at different power levels. As shown in Figure 27 for the third power-flow scenario, the link will be energized in mode 1 and it will be de-energized into the battery and into the three-phase load in modes 3, 5 and 7. As discussed earlier, the order and sequence of charging the battery and the ac load depend on the ac-side and the battery voltage values and here it is assumed that the link is discharged into the battery during mode 3. The following equations describe the behavior of the circuit in each mode:

$$I_{Link,Peak} = \frac{V_{PV} \times t_{charge}}{L} \tag{49}$$

$$\Delta I_{Link\_ac} = \frac{V_{o-eq} \times t_{discharge\_ac}}{L} \tag{50}$$

$$I_{Link,Peak} - \Delta I_{Link\_ac} = \frac{V_{Battery} \times t_{discharge\_Battery}}{L} \quad (51)$$

In these equations $I_{Link,peak}$, ΔI_{Link_ac}, t_{charge}, $t_{discharge\_ac}$, $t_{discharge\_Battery}$, $V_{Battery}$, V_{PV} and V_{o_eq} are the link peak current, the link current change during modes 5 and 7, duration of mode 1 (energizing from PV), duration of modes 5 and 7 (de-energizing to the load), duration of mode 3 (de-energizing to the battery), battery voltage, PV voltage and, the equivalent load voltage, respectively.

The average of the PV current and the battery current can be calculated using the following equations:

$$I_{PV} = \frac{1}{T}\left(I_{Link,Peak} \times t_{charge}\right) \quad (52)$$

$$I_{Battery} = \frac{1}{T}\left(\left(I_{Link,Peak} + \Delta I_{Link\_ac}\right) \times t_{discharge\_Battery}\right) \quad (53)$$

It can be shown that:

$$P_{PV} = I_{Link,Peak}^2 Lf \quad (54)$$

$$P_{bat} = \left(I_{Link,Peak}^2 - \Delta I_{Link\_ac}^2\right)Lf \quad (55)$$

$$\frac{\Delta I_{Link\_ac}}{I_{Link,Peak}} = \sqrt{\frac{P_{PV} - P_{bat}}{P_{PV}}} \quad (56)$$

where P_{PV}, P_{bat}, and f are power generated by the PV, power needed for charging the battery, and the frequency of the link, respectively. The link peak current and the link frequency can be determined using the following equations:

$$I_{Link,Peak} = 2P_{PV}\left(\frac{1}{V_{PV}} + \frac{1 - \sqrt{\frac{P_{PV} - P_{bat}}{P_{PV}}}}{V_{bat}} + \frac{\sqrt{\frac{P_{PV} - P_{bat}}{P_{PV}}}}{V_{o\_eq}}\right) \quad (57)$$

$$f = \frac{1}{2 \times L \times I_{Link,Peak} \left(\frac{1}{V_{PV}} + \frac{1 - \sqrt{\frac{P_{PV} - P_{bat}}{P_{PV}}}}{V_{bat}} + \frac{\sqrt{\frac{P_{PV} - P_{bat}}{P_{PV}}}}{V_{o\_eq}} \right)} \quad (58)$$

In these equations the resonating modes have been neglected. If the resonating modes are not negligible, a more accurate method similar to the method proposed in 2.5 should be used.

2.8.2. Principles of Operation & Analysis for the Fourth Power-Flow Scenario (PV and Battery to the Load)

Various modes of operation in the fourth power-flow scenario are similar to those of the third power-flow scenario, except mode 3 is an energizing mode in the fourth power scenario. These modes of operation are explained as follows:

Mode 1 (Energizing): Similar to the third power-flow scenario, in this mode the link will be charged. However since there are two sources to charge the link, before the start of mode 1, it should be decided which one to charge the link during mode 1 and which one to charge the link during mode 3. This will be determined based on the absolute value of the voltage across the PV modules and the battery. The source having a higher voltage will charge the link during mode 1 and the other source will charge the link during mode 3. Before the start of mode 1, switches which are supposed to conduct during modes 1 and 3 will be turned on; however, they do not conduct immediately as they are reverse-biased. In Figure 29 and Figure 30 it is assumed that the voltage across the battery is higher than the voltage across the PV module. Consequently, during mode 1 the battery will charge the link and once the battery current averaged over a power

cycle meets its reference value, switches S6 and S11, which were turned on at zero voltage, will be turned off.

Mode 2 (Partial resonance): Similar to the third power-flow scenario during this mode none of the switches conduct and the link resonates until its voltage becomes equal to that of the PV modules, which are supposed to charge the link during mode 3.

Mode 3 (De-energizing): Once the link voltage is equal to the voltage across the PV, switches S0 and S3 are forward-biased initiating mode 3, during which the link continues being charged through the PV. When the PV current averaged over a power cycle meets its reference; S0 and S3 will be turned off, initiating another resonating mode.

During mode 4 the switches which are supposed to conduct during modes 5 and 7 are turned on; however, they do not conduct because they are reverse-biased. Modes 5-8 are similar to those of the third power-flow scenario.

The behavior of the circuit during modes 1, 3, and 5 in the first power-flow scenario is the same as its behavior during modes 3, 5, and 7 of the fourth power-flow scenario, respectively. Similarly, modes 1, 3, and 5 in the second power-flow scenario are the same as modes 1, 5 and 7 in the fourth power-flow scenario, respectively. The input current reference can be derived using the output reference currents and the estimated efficiency of the converter at that power level. A more accurate method, as mentioned for the single-input/single-output configuration, is to charge the link from the input up to a certain level, then discharge it to the output and control the output currents during the de-energizing modes. Once the output currents meet their references, the

energy left in the link is discharged into the input-side capacitor. In this case, even the PV side switches need to be bi-directional. This method does not need the input current reference and is more accurate.

As mentioned earlier, the PV voltage is considered to be lower than the battery voltage. The following equations describe the behavior of the circuit in each power transfer mode of the fourth power flow scenario:

$$\Delta I_{Link\_Battery} = \frac{V_{Battery} \times t_{charge\_Batttery}}{L} \tag{59}$$

$$I_{Link,Peak} - \Delta I_{Link\_Battery} = \frac{V_{PV} \times t_{charge\_PV}}{L} \tag{60}$$

$$I_{Link,Peak} = \frac{V_{o-eq} \times t_{discharge}}{L} \tag{61}$$

In these equations $I_{Link,peak}$, $\Delta I_{Link\_Battery}$, $t_{charge\_Battery}$ and t_{charge_PV} are the link peak current, the link current change during mode 1, duration of mode 1 (energizing from the battery), and duration of mode 3 (energizing from the PV), respectively.

It can be shown that the link peak current and the link frequency are determined by the following equations:

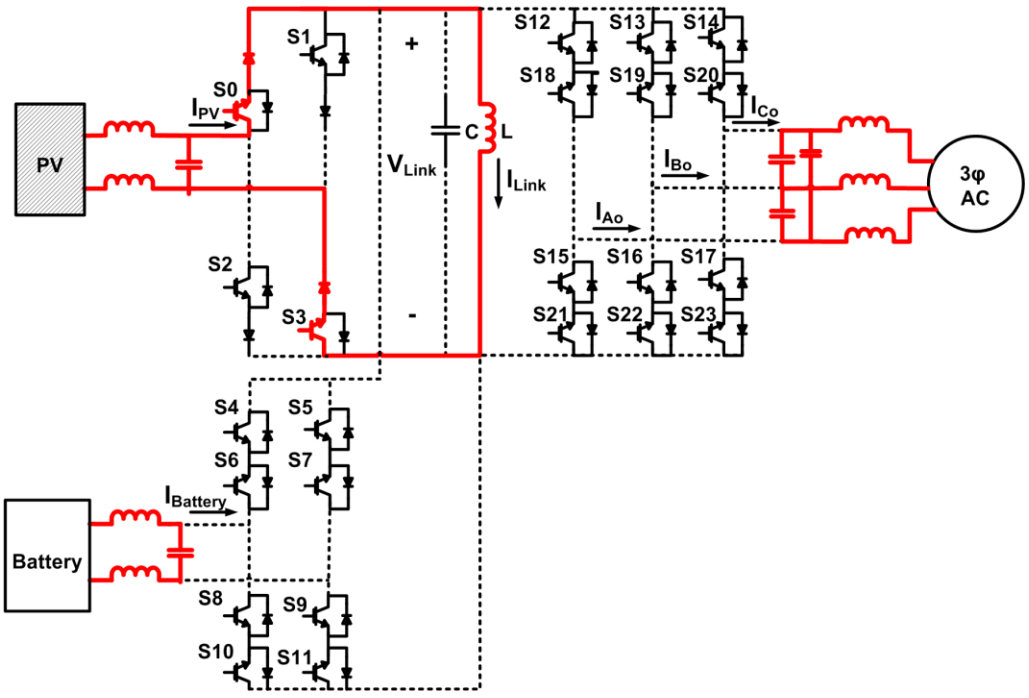
$$I_{Link,Peak} = 2(P_{PV} + P_{bat})\left(\frac{\sqrt{\frac{P_{bat}}{P_{PV}+P_{bat}}}}{V_{bat}} + \frac{1-\sqrt{\frac{P_{bat}}{P_{PV}+P_{bat}}}}{V_{PV}} + \frac{1}{V_{o_{eq}}}\right) \tag{62}$$

$$f = \frac{1}{2 \times L \times I_{Link,Peak}\left(\frac{\sqrt{\frac{P_{bat}}{P_{PV}+P_{bat}}}}{V_{bat}} + \frac{1-\sqrt{\frac{P_{bat}}{P_{PV}+P_{bat}}}}{V_{PV}} + \frac{1}{V_{o_{eq}}}\right)} \tag{63}$$

where P_{PV} and P_{bat} are the power generated by the PV and the power generated by the battery, respectively.

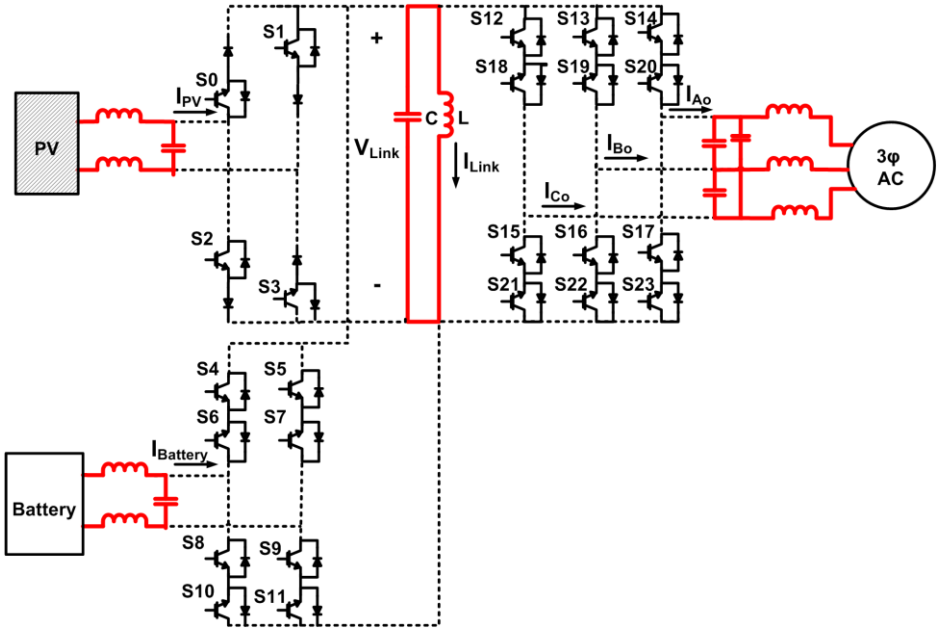
Again, if the resonating time is short enough, the link peak current and the link frequency can be determined by the above equations. Otherwise, the resonating time should be taken into consideration and more accurate values for the link peak current and the link frequency should be achieved.

It is observed that the PV modules are never directly connected to the load, thereby resulting in proper isolation. Fully galvanic isolation can be achieved by using a single phase high-frequency transformer in place of the link inductor.

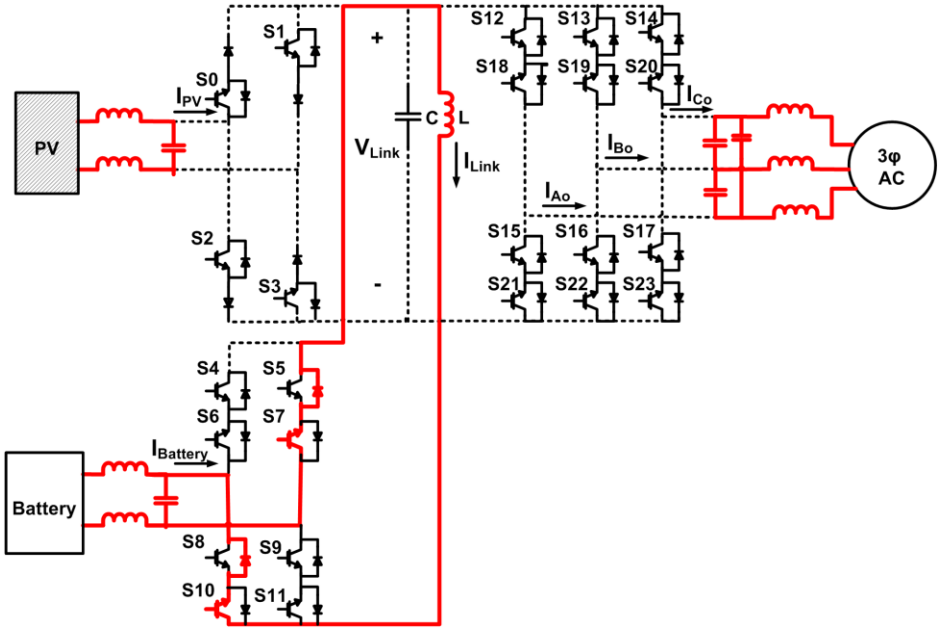


(a) Mode 1 of the third power-flow scenario and mode 3 of the fourth power-flow scenario

Figure 29 Circuit behavior during different modes of operation

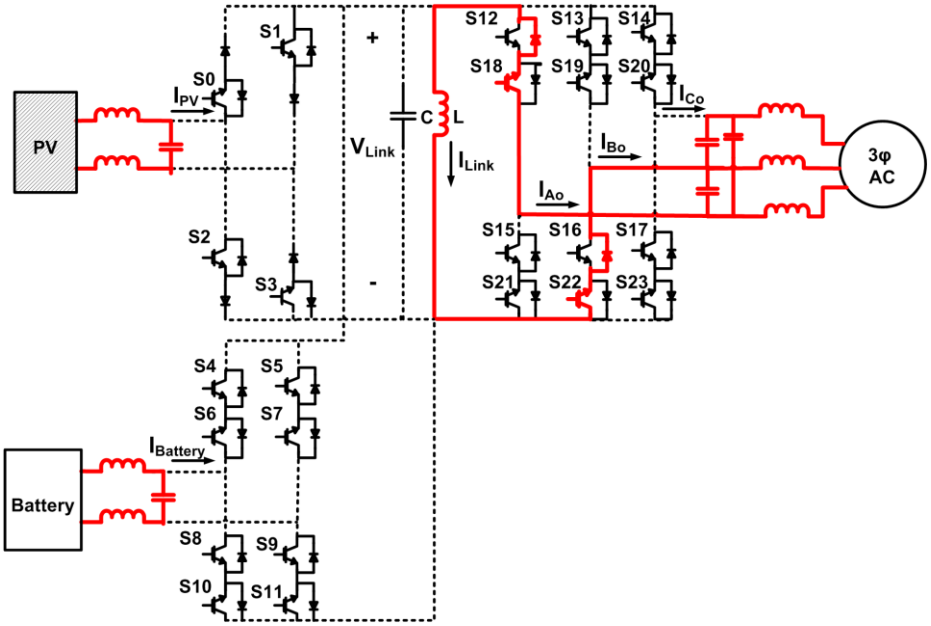


(b) Modes 2,4,6 and 8 of the third & fourth power-flow scenarios

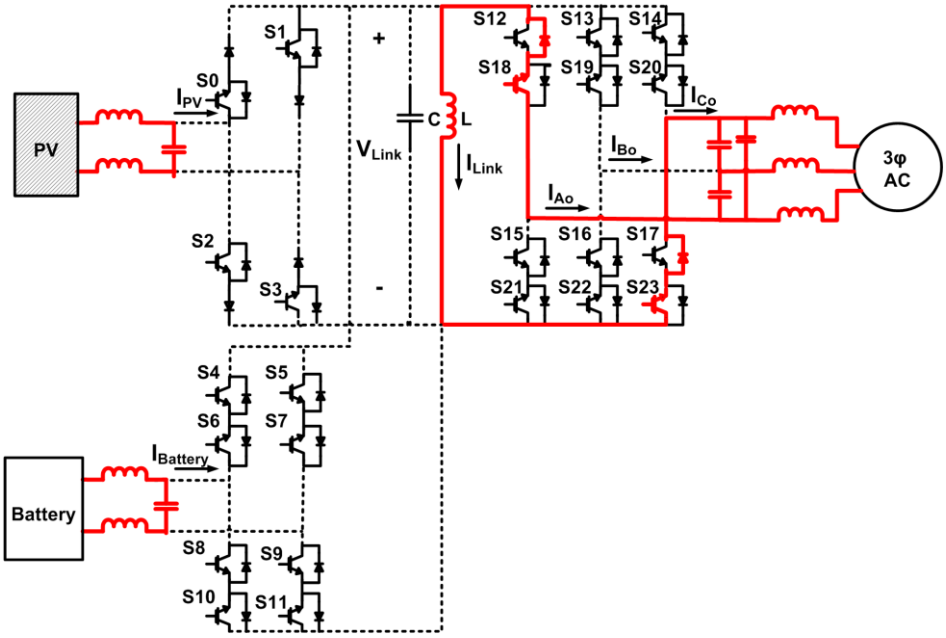


(b) Mode 3 of the third power-flow scenario

Figure 29 Continued.

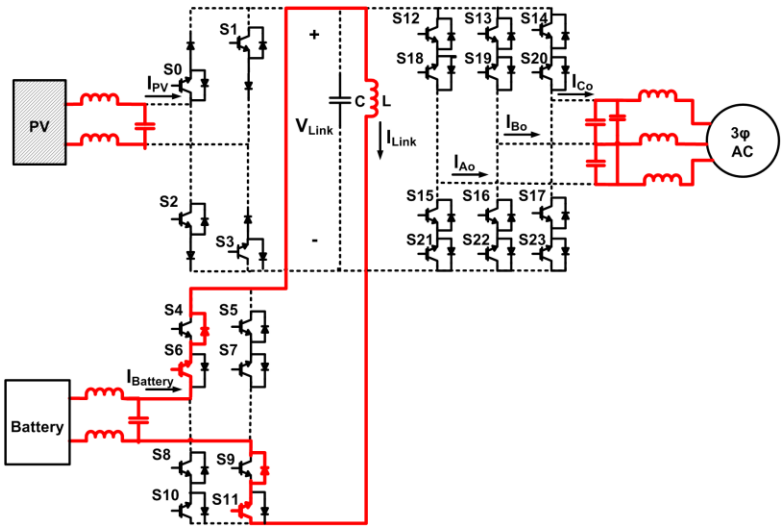


(d) Mode 5 of the third and fourth power-flow scenarios



(e) Mode 7 of the third and fourth power-flow scenario

Figure 29 Continued.



(f) Mode 1 of the fourth power-flow scenario

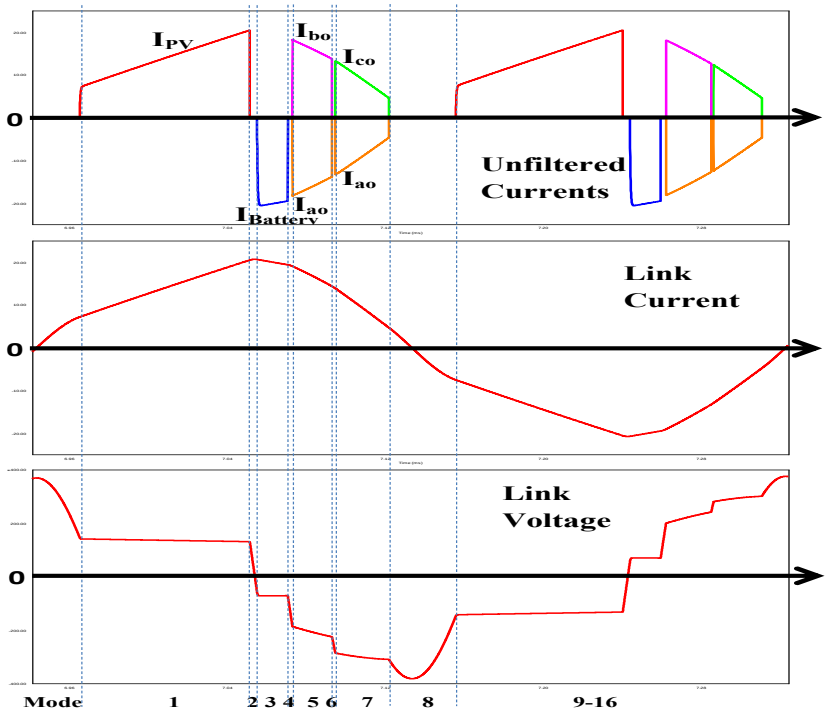
Figure 29 Continued.

2.9. Simulation and Experimental Results

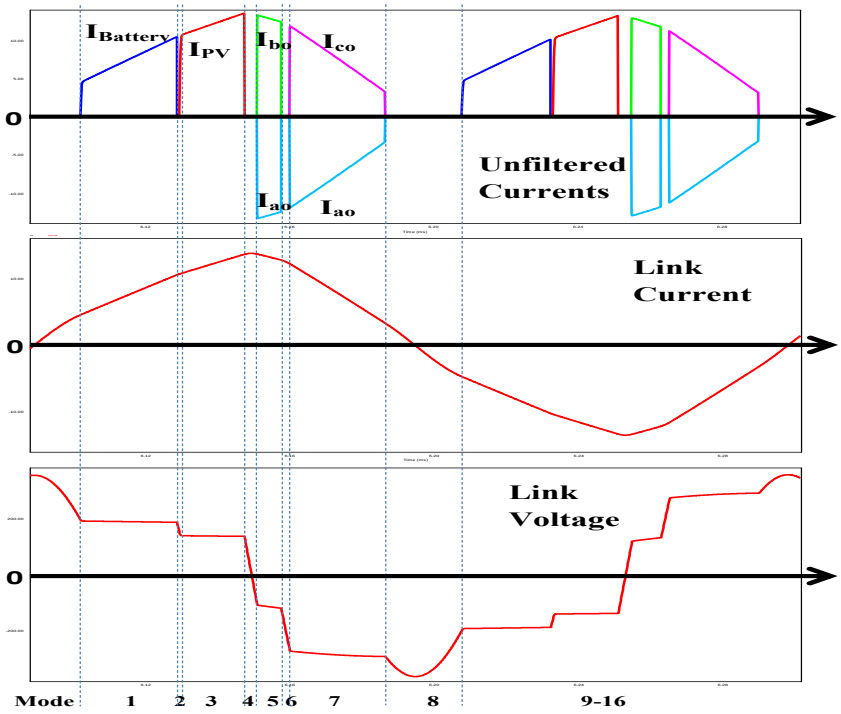
The parallel ac-link universal converter may be employed at low-power, medium-power and high-power applications. The performance of this converter has been evaluated through simulation for all three categories. However, the experimental evaluation in this dissertation is limited to low-power and medium-power categories.

2.9.1. Low Power Tests

In order to evaluate the ac-link universal power converters (parallel, series, sparse, and ultra-sparse) a multi-purpose and modular prototype was designed and fabricated with which different configurations were tested. For this purpose the whole system was divided into four boards:



(a) Third power-flow scenario



(b) Fourth power-flow scenario

Figure 30 Current and voltage waveforms

- *Input-side switch board*

Three legs, each containing two bidirectional or four unidirectional switches, have been considered on the input switch board. If this board is connected to a dc or to a single-phase ac source; one of the legs will be unused. Pictures of the fabricated switch boards are shown in Figure 31. Proper filters, current sensors, and voltage sensors are also included on these boards.

- *Output-side switch board*

The output switch board is similar to the input switch board. Again, when connected to dc or to a single phase ac load, one leg will be unused.

- *Link board*

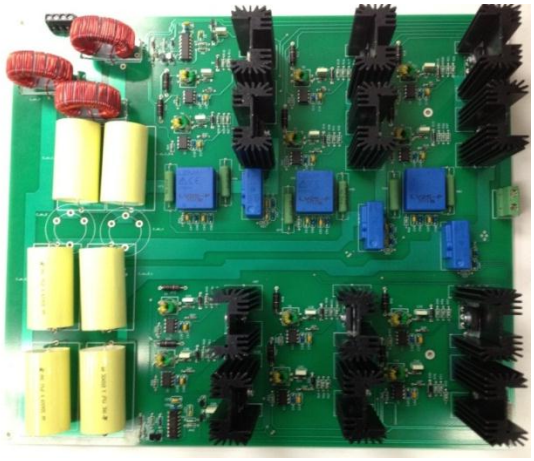
This link board contains the link inductor, the link capacitor, proper sensors for measuring the link current and voltage, and a circuit for turning off the converter. The picture of the fabricated link board is represented in Figure 32.

- *Control board*

This control board contains a microcontroller, the proper analog-to-digital converter (ADC) interface, and the required buffers as shown in Figure 33.

2.9.1.1. Three-phase AC-AC Configuration

In this part the performance of the three-phase ac-ac parallel ac-link universal power converter will be evaluated through simulation and experiments. The parameters of the designed, simulated and tested prototype are tabulated in Table 1.



(a) Switch board for three-phase ac source or load

(b) Switch board for dc source or load

Figure 31 Fabricated input/ output switch board

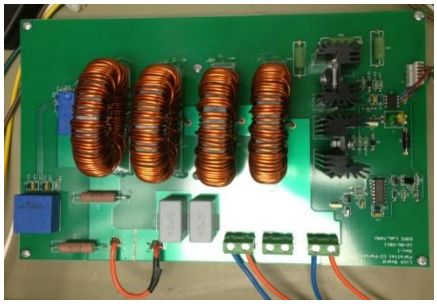


Figure 32 Fabricated link board

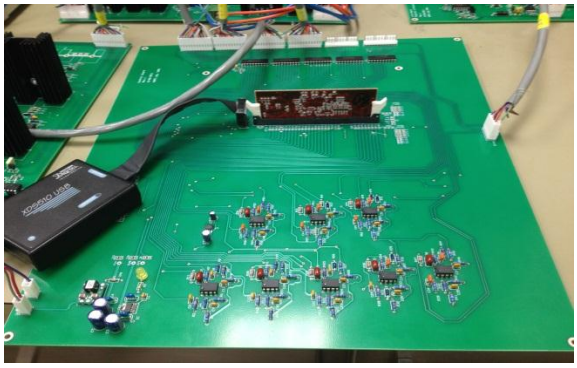


Figure 33 Fabricated control board

This converter was simulated in PSim. Figure 34–Figure 38 represent the results. Figure 34 shows the input current and voltage when the converter operates at 450 W. As seen in this figure the input current and voltage are about 25 degrees apart. As mentioned earlier, one of the advantages of this converter is the possibility of controlling

the input power factor. In this simulation, the currents are regulated such that the unfiltered currents are in phase with the phase voltages. However, the input-side filter capacitor, the capacitance of which is 40 μF, causes the filtered current to be phase shifted from the unfiltered current. To show that the input power factor can be controlled, in Figure 35 the simulation is repeated, but this time the input current is regulated such that the filtered current is in phase with the voltage. Figure 36 represents the output voltage and current. Because the load is resistive, the output power factor is unity, too.

TABLE 1 PARAMETERS OF THE DESIGNED, SIMULATED AND FABRICATED AC-AC PARALLEL AC-LINK UNIVERSAL POWER CONVERTER

Parameter	**Value**
Input Voltage	Step-down operation: 140 V Step-up operation: 70 V
Output Voltage	Step-down operation: 92 V Step-up operation: 120 V
Link inductance	880 μH
Link Capacitance	700 nF
Input side filter inductance	Simulation:1 mH Experiment: 15 mH
Input side filter capacitance	40 μF
Output side filter inductance	556 μH
Output side filter capacitance	20 μF

Figure 37 depicts the link current and voltage. The link peak current varies between 14 and 14.7 A. Therefore, the average of the link peak current is about 14.3 A. This value is much higher than the value calculated by (14). This is due to the high link capacitance. A lower link capacitance is always more desirable in this converter. Since no power is transferred during the resonance, the resonating time should be kept as short as possible. However, in practice we have to make sure the proper switches are turned on before they are forward-biased; otherwise the switches will have hard switching. By

optimizing the control code and using a faster microcontroller a lower link capacitance can be chosen. Figure 38 shows the link current and voltage when the link capacitance is decreased to 20 nF. The link peak current in this case has dropped to 11.55 A. This value is very close to the value calculated by (14), which is 11.74 A.

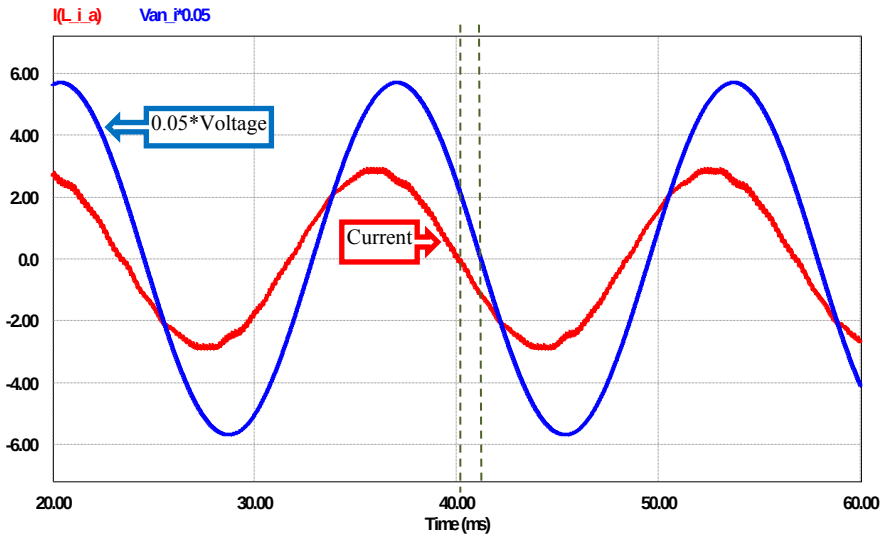


Figure 34 The input-side current and scaled voltage in the ac-ac parallel ac-link universal converter when the current is regulated such that the unfiltered current is in-phase with the input voltage

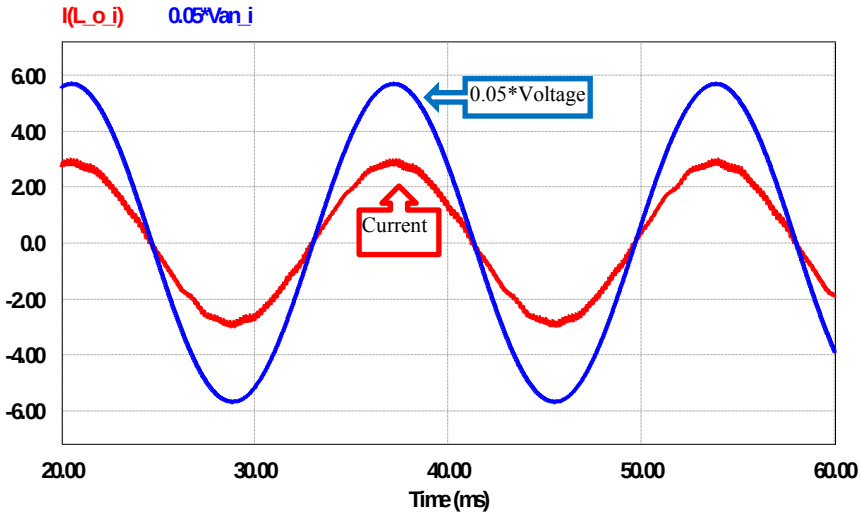


Figure 35 The input-side current and scaled voltage in the ac-ac parallel ac-link universal converter when the current is regulated such that the filtered current is in-phase with the input voltage

A low power prototype, shown in Figure 39, with the same specifications as listed in Table 1 was tested. Figure 40 shows how different boards are connected to test the prototype as a three-phase ac-ac converter. Figure 41 represents the input current and voltage when the converter is operating at 450 W. As seen in this figure the input current and voltage are not in phase. Again, the converter is controlled such that the unfiltered current is in phase with the voltage.

Considering that the frequency of the unfiltered currents is twice the frequency of the link (as shown in Figure 16), the cut-off frequency of the filters can be very high and the filter inductance and capacitance can be small in this converter. However, the three-phase ac voltage source used in this test was distorted by low-frequency harmonics. In order to attenuate the low-frequency harmonics of the input current, which are generated by low-frequency harmonics of the source voltage, a high-inductance filter was chosen. The input filter components are listed in Table 1.

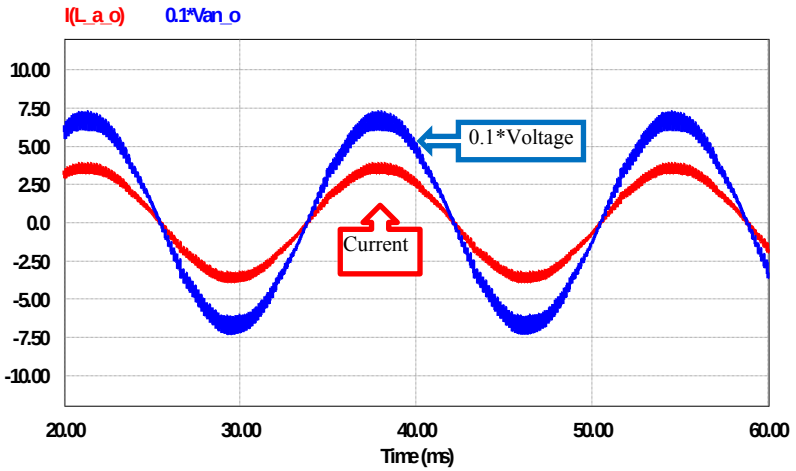


Figure 36 The load current and scaled voltage in the ac-ac parallel ac-link universal converter

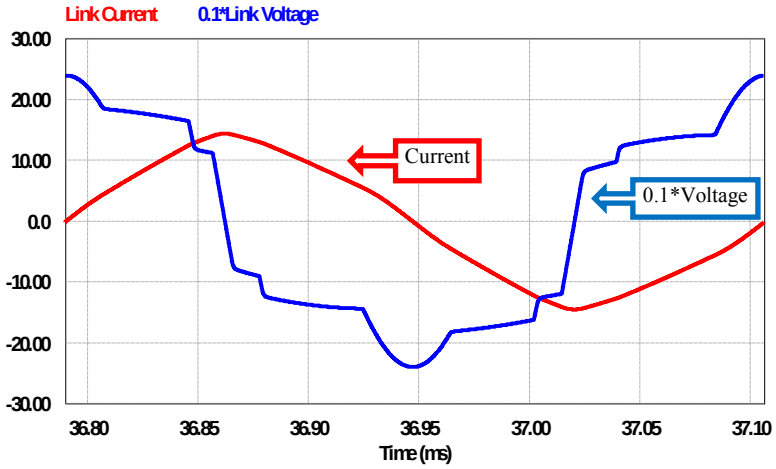


Figure 37 The link current and scaled voltage in the ac-ac parallel ac-link universal converter with 700 nF link capacitance

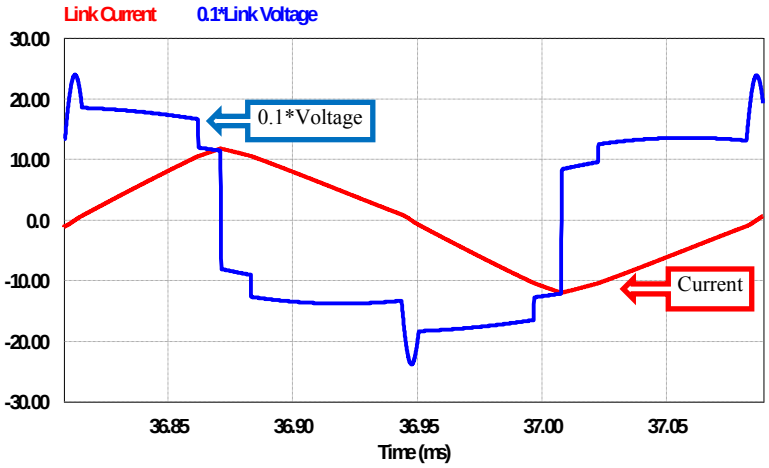


Figure 38 The link current and scaled voltage in the ac-ac parallel ac-link universal converter with 20 nF link capacitance

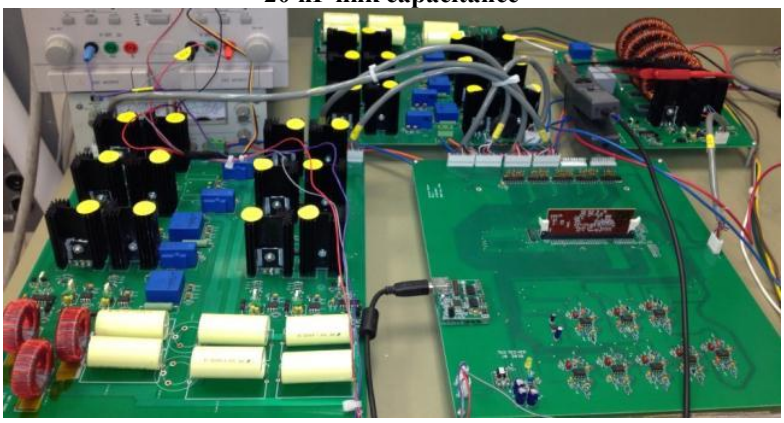


Figure 39 Fabricated and tested three-phase ac-ac parallel ac-link universal converter

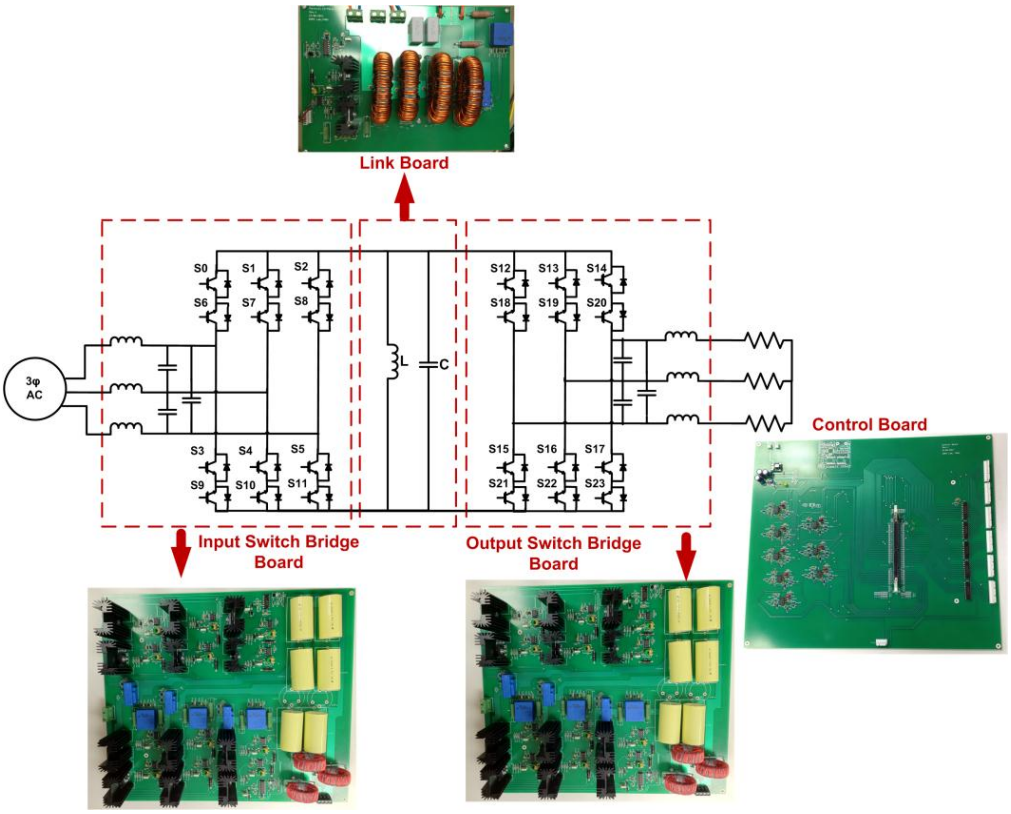


Figure 40 Different parts of the prototype for testing the ac-ac configuration

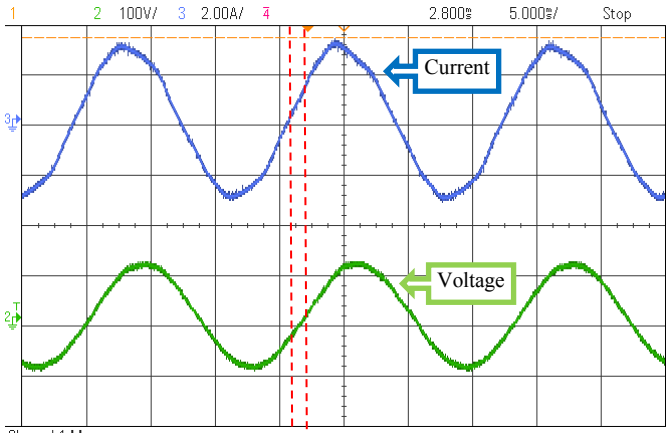


Figure 41 The input current and voltage in the ac-ac parallel ac-link universal converter (experimental results)

Figure 42 represents the load current and load voltage. Similar to the simulations, a three-phase resistive load is used. In this test both the input and output frequencies are

60 Hz. To show the capability of the converter in changing the frequency, the test is repeated and the output frequency is set at 30 Hz while the frequency of the input voltage/current is still 60 Hz. Figure 43 shows the output current/voltage corresponding to this case.

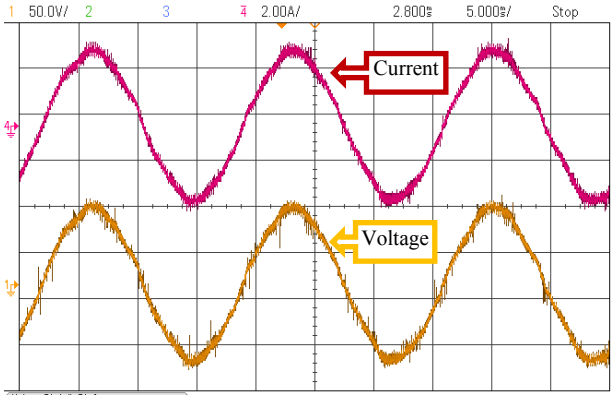


Figure 42 The load current and voltage in the ac-ac parallel ac-link universal converter (experimental results)

The link current and voltage are depicted in Figure 44. The link peak current and the link frequency are 14.2 A and 3.1 kHz, respectively. These values are very close to the values achieved through the simulation. Using the method introduced in section 2.5 for calculating the accurate values of the link peak current and the link frequency, these parameters are determined as 14.3 A and 3.1 kHz, respectively. This verifies the accuracy of the method proposed in section 2.5.

In Figure 41–Figure 44 the peak of the input voltage is higher than the peak of the output voltage. The converter is stepping down the voltage. Figure 45–Figure 47 illustrate the experimental results corresponding to the step-up operation of the converter with 70 V input and 120 V output voltages. The input current/voltage, the output current/voltage, and the link current/voltage corresponding to this case are shown in these figures. When the converter operates in the step-up mode, the principles of the

operation may be slightly changed such that the link voltage does not swing to a maximum voltage. In this case the link will be fully discharged during mode 7, and once the link current reaches zero all of the switches will be turned off. Therefore, the absolute value of the link voltage decreases right after turning off the output switches at the end of mode 7. This method improves the efficiency and reduces the resonating time.

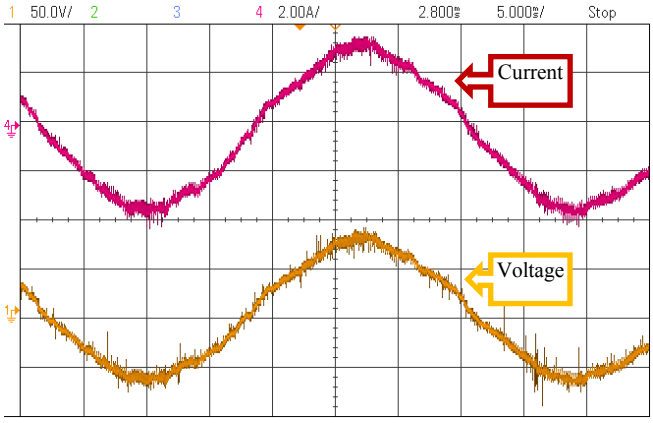


Figure 43 The load current and voltage in the ac-ac parallel ac-link universal converter when the output frequency is set at 30 Hz (experimental results)

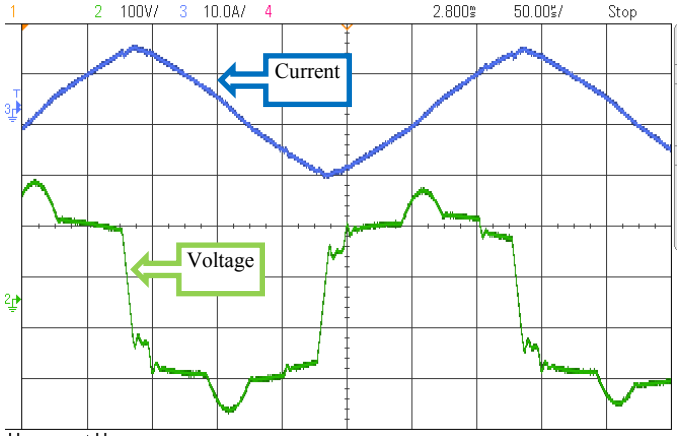


Figure 44 The link current and voltage in the ac-ac parallel ac-link universal converter

To validate the method proposed in section 2.5, the measured link peak current and frequency at two different power levels are compared with the values achieved

through the simulation and calculations. These values are compared in Table 2. As seen in this table, the proposed method is accurate with an error less than 3%.

The measured efficiency of the converter when operating at 450 W is 90%. Of course the efficiency will be higher when the converter operates at higher power levels. The main sources of power dissipation in this converter are conduction losses of the switches, the inductor core loss, and the inductor copper loss.

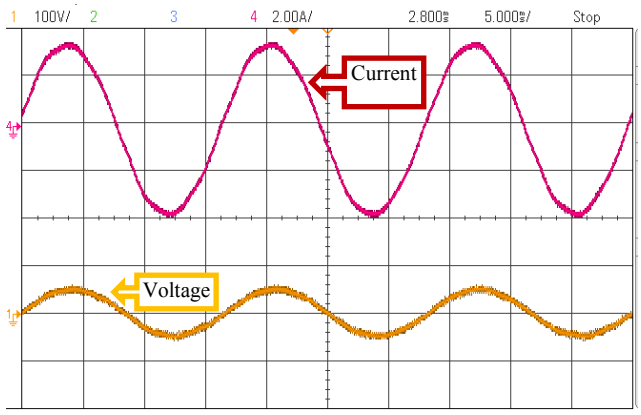


Figure 45 The input current and voltage of the ac-ac parallel ac-link universal converter in step-up operation (Experimental results)

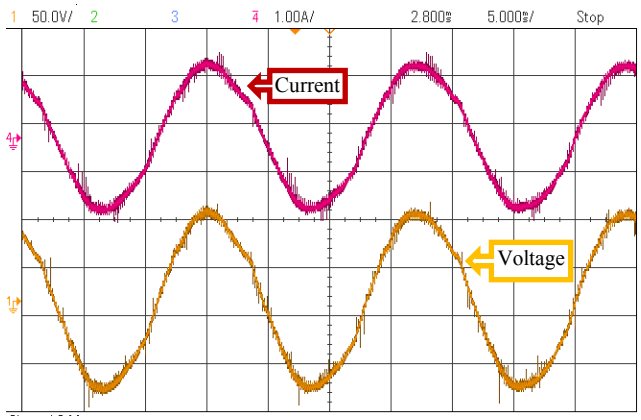


Figure 46 The load current and voltage of the ac-ac parallel ac-link universal converter in step-up operation (Experimental results)

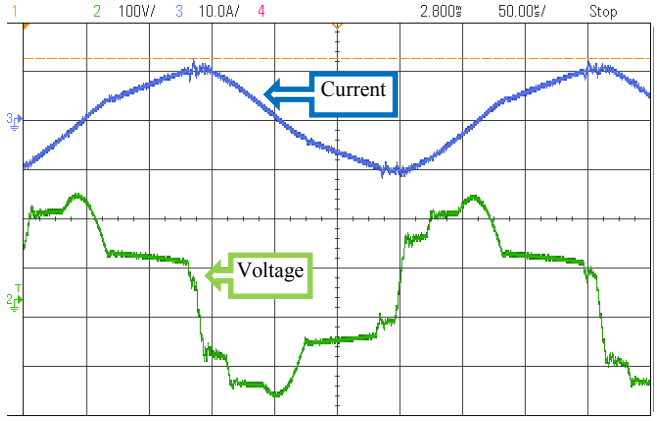


Figure 47 The link current and voltage of the ac-ac parallel ac-link universal converter in step-up operation (Experimental results)

TABLE 2 COMPARISON OF THE ANALYSIS, SIMULATION AND EXPERIMENT

Case	Parameter	Calculation	Simulation	Experiment
P_{in}=450 W, V_{in}=140 , V_o=92	$I_{Link,peak}$	14.3 A	14.3 A	14.2 A
	F_{Link}	3.1 kHz	3.1 kHz	3.1 kHz
P_{in}=250 W, V_{in}= 140, V_o=92	$I_{Link,peak}$	10.3 A	10.2 A	10.7 A
	F_{Link}	4.4 kHz	4.5 kHz	4.4 kHz

In order to evaluate the improved control method proposed in section 2.7, the ac-ac parallel ac-link universal converter with the specifications listed in Table 3 has been simulated. The load power factor is about 0.46 in this case and it is lower than the limit determined by (46) to satisfy soft switching. Figure 48–Figure 50 demonstrate the simulation results corresponding to this system when the improved control method has been used. Figure 48 represents the input current and scaled voltage. The input power factor is close to unity. Figure 49 depicts the load current and scaled voltage. Link current and voltage along with the unfiltered currents are shown in Figure 50. As seen, during the time span shown in this figure the output phase-pair “bc” has charged the link during mode 1.

TABLE 3 PARAMETERS OF THE SIMULATED CONVERTER WHEN THE IMPROVED CONTROL METHOD IS USED

Parameter	Value
Input Voltage	140 V
Output Voltage	675 V
Power Level	1000
Load	Three-phase (RL): R=100 Ω L= 0.5 H
Link inductance	880 µH
Link Capacitance	700 nF
Input side filter inductance	1 mH
Input side filter capacitance	40 µF
Output side filter inductance	556 µH
Output side filter capacitance	50 µF

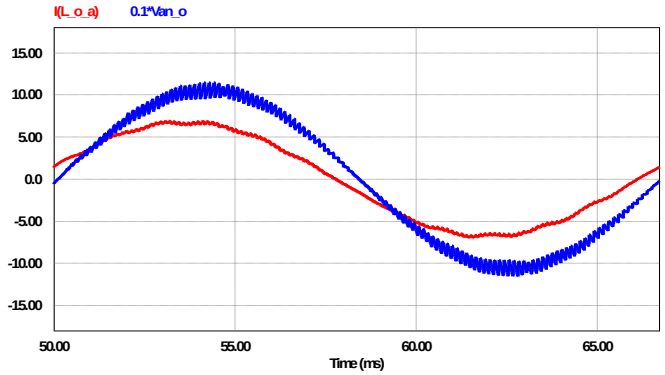


Figure 48 Input current and scaled voltage in the ac-ac parallel ac-link universal converter using the improved control method

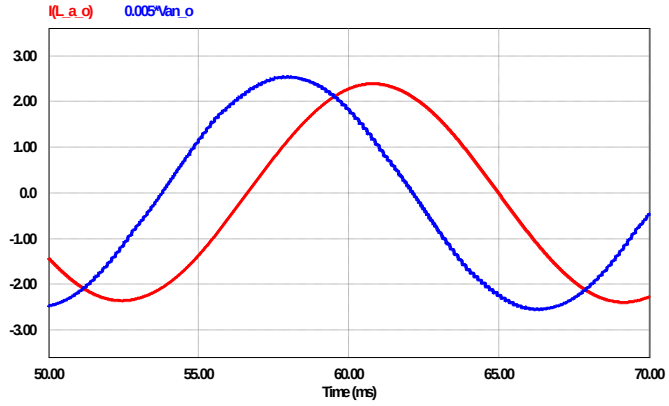


Figure 49 Load current and scaled voltage in the ac-ac parallel ac-link universal converter using the improved control method

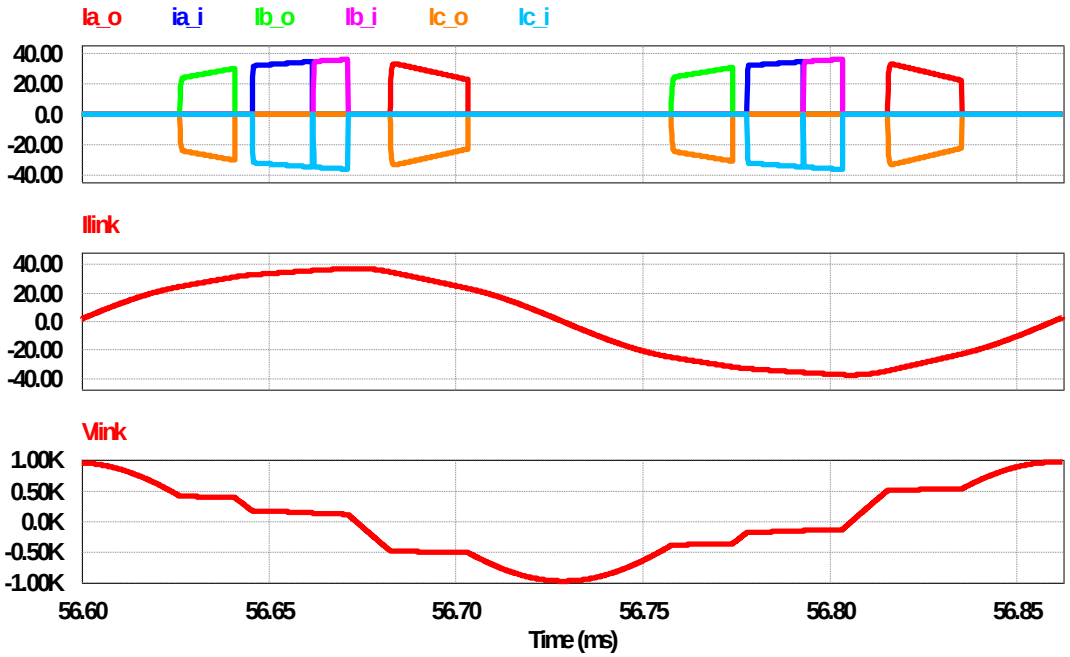


Figure 50 Unfiltered phase currents, link current and link voltage in the ac-ac parallel ac-link universal converter using the improved control method

2.9.1.2. DC-AC Configuration

In this part the performance of the parallel ac-link universal power converter when operating as an inverter is evaluated. Table 4 summarizes the parameters of the simulated and tested converter. Figure 51–Figure 54 show the simulation results of this converter when operating at 800 W. Figure 51 shows dc-side current and voltage. Figure 52 and Figure 53 show the ac-side currents and the link current/voltage, respectively.

As illustrated in Figure 53, the peak of the link current and the maximum voltage to which the link swings during mode 6 are 17.5 A and 322 V, respectively. The frequency of the link is 3.79 kHz in this case. Equations (21)–(31) determine the link peak current and the link frequency as 17.5 A and 3.77 kHz, which are very close to the simulation results. It should be noted that the input power is more than 800 W in this

case, as the efficiency is 94.5%. Conduction losses of the switches and the copper losses of the inductors have been modeled in the simulations. The link current and voltage when using 200 µH and 20 nF link inductance and capacitance are shown in Figure 54. As seen in this figure, the peak of the link current is 15.41 A. The value achieved by (14) is 15.25 A.

TABLE 4 PARAMETERS OF THE SIMULATED AND TESTED DC-AC PARALLEL AC-LINK UNIVERSAL POWER CONVERTER

Parameter	Value
Dc side Voltage	200 V
ac side Voltage	208 V
Load characteristics	Three-phase, resistive, 54 Ω
Power level	800 W
Link inductance	880 µH
Link Capacitance	400 nF

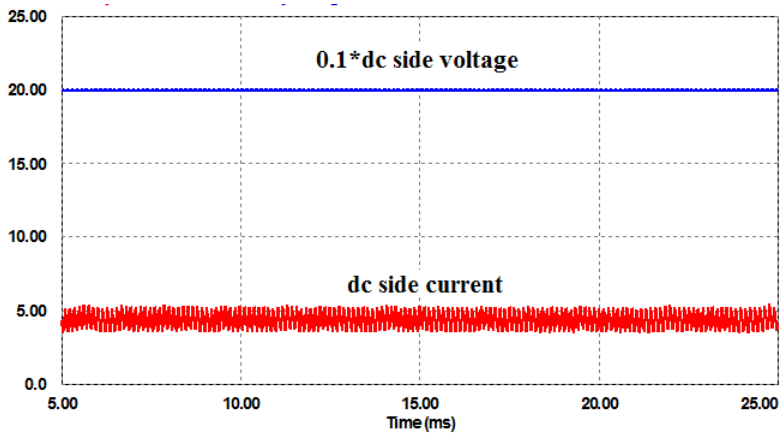


Figure 51 Dc side current and scaled voltage in the dc-ac parallel ac-link universal converter

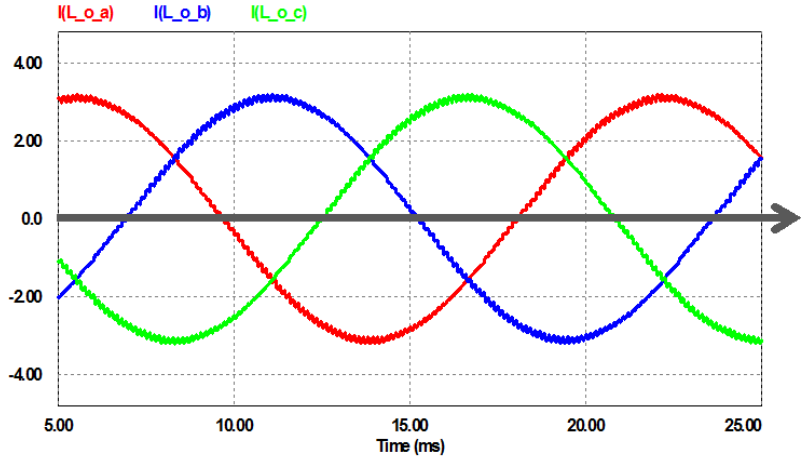


Figure 52 Ac-side currents in the dc-ac parallel ac-link universal converter

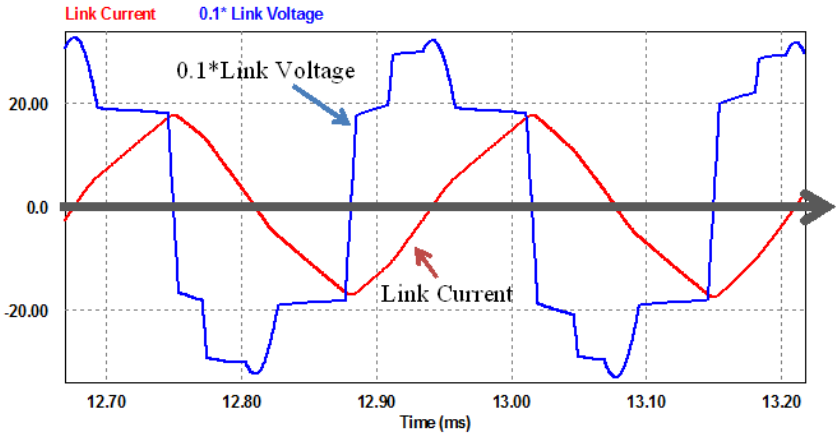


Figure 53 Link current and scaled link voltage in the dc-ac parallel ac-link universal converter with 880 µH link inductance and 400 nF link capacitance

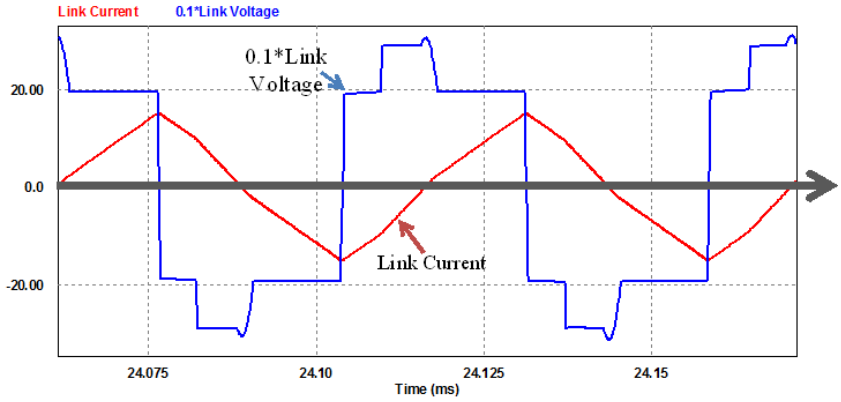


Figure 54 Link current and scaled link voltage in the dc-ac parallel ac-link universal converter with 200 µH link inductance and 20 nF link capacitance

Figure 55 shows how different parts of the prototype are connected to form the dc-ac parallel ac-link universal power converter. Figure 56–Figure 58 represent the experimental results when the prototype is operating at 800 W. Figure 56 shows the dc-side voltage/current. Similar to the simulation, the input voltage is 200 V. The ac-side current is represented in Figure 57. A three-phase resistive load has been used in this test; however, this inverter does not have any limitations on the type of load. Link current and voltage are illustrated in Figure 58. The peak of the link current is 17.39 A,

which is very close to the simulation. The maximum link voltage is 326 V and the link frequency is 3.75 kHz in this case.

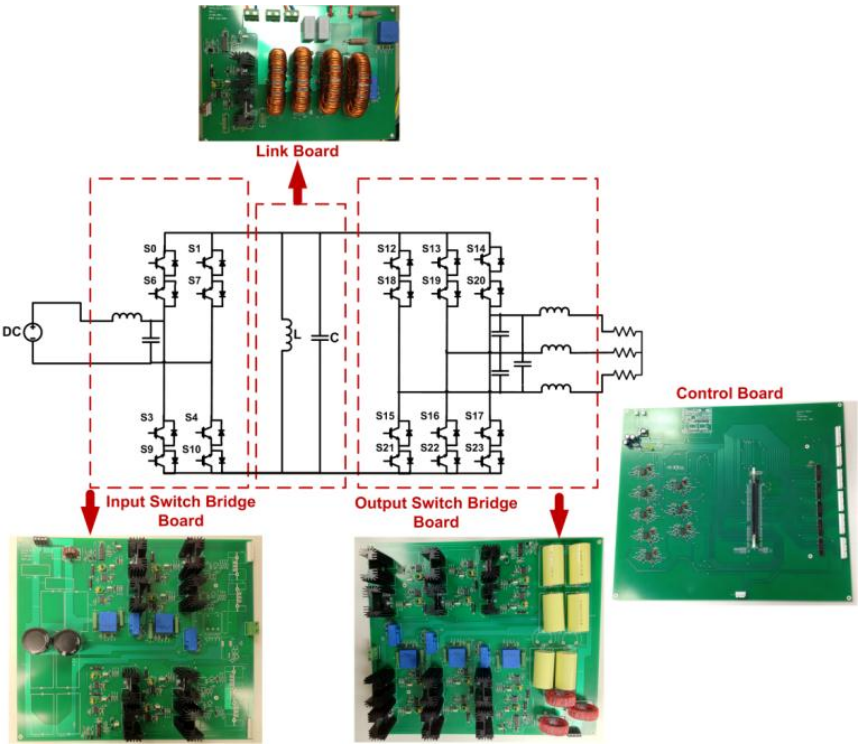


Figure 55 Different parts of the prototype for testing the dc-ac parallel ac-link universal converter

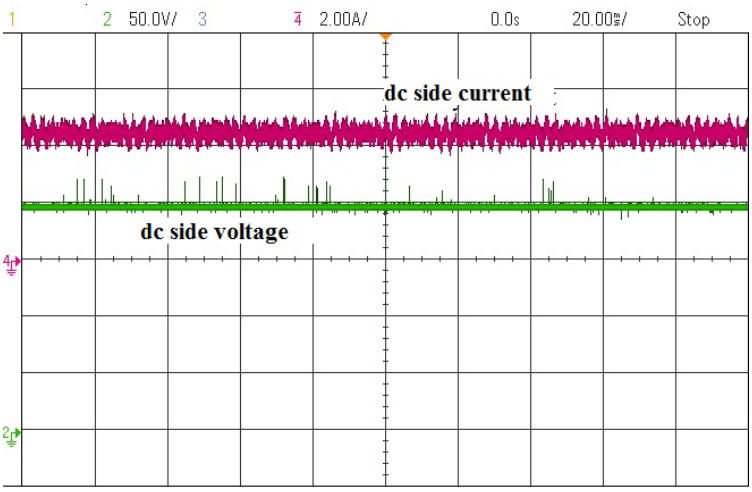


Figure 56 Dc-side current (2 A/div) and voltage (50 V/div) in the dc-ac parallel ac-link universal converter (experimental results), time scale: 20 ms/div

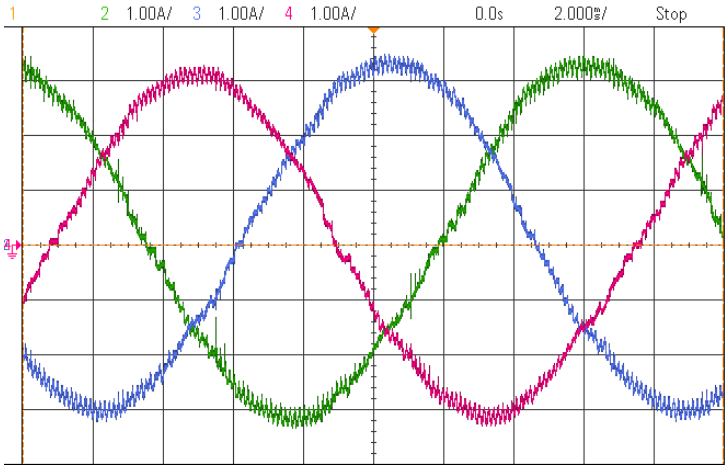


Figure 57 Ac side currents (1 A/div) in the dc-ac parallel ac-link universal converter (experimental results), time scale: 2 ms/div

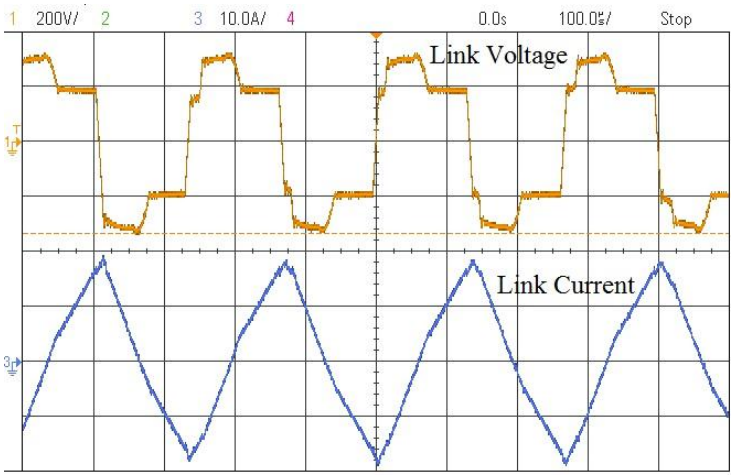


Figure 58 Link voltage (200 V/div) and current (10 A/div) in the dc-ac parallel ac-link universal converter (experimental results), time scale: 100 µs/div

2.9.1.3. AC-DC Configuration

This part evaluates the performance of the converter as a rectifier. Figure 59–Figure 61 show the simulation results for this case. The parameters of the converter are similar to those of the dc-ac case studied in the previous part, and the converter is tested at 800 W.

To test the multi-purpose prototype in the ac-dc mode of operation, boards are connected as shown in Figure 62. The ac-side is connected to a three-phase ac source through an autotransformer, and the dc-side is connected to a resistive load.

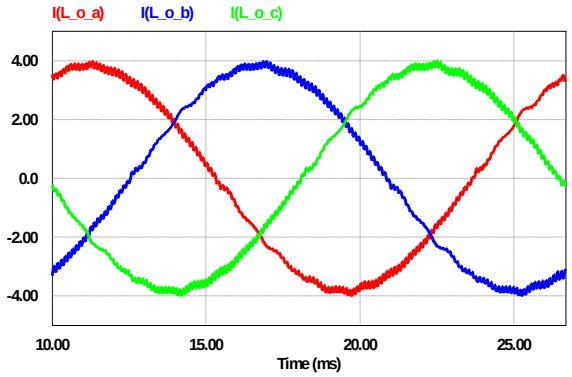


Figure 59 Ac-side currents in the ac-dc parallel ac-link universal converter

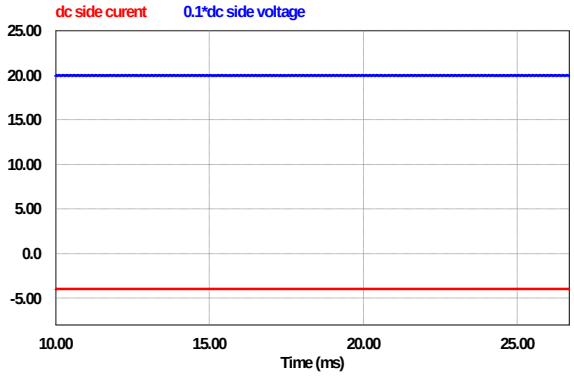


Figure 60 Dc-side current and scaled voltage in the ac-dc parallel ac-link universal converter

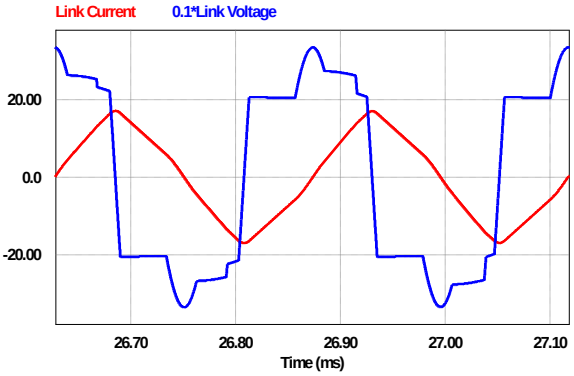


Figure 61 Link current and scaled voltage in the ac-dc parallel ac-link universal converter

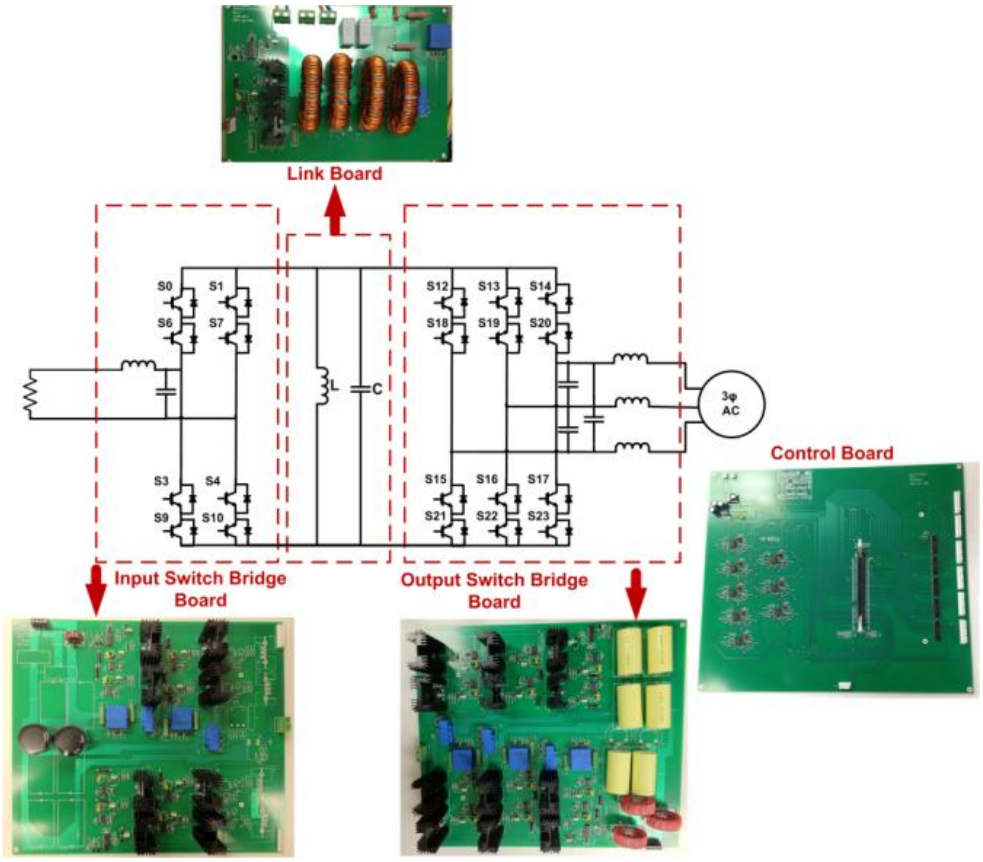


Figure 62 Different parts of the tested ac-dc parallel ac-link universal power converter

Figure 63–Figure 65 show the experimental results corresponding to this converter operating at 200 W. The ac-side voltage is 120 V and the dc-side is connected to a resistive load with 50 ohms resistance. The ac-side current/voltage are represented in Figure 63. The three-phase ac voltage source used in this experiment contains low-frequency harmonics which generate the same low-frequency harmonics in the current. To attenuate these harmonics, large filter components were used. The result was a noticeable phase difference between the phase current and voltage. The dc-side current and voltage are shown in Figure 64. Figure 65 depicts the link current and voltage. The peak of the link current and the link frequency are 8.6 A and 6.13 kHz, respectively.

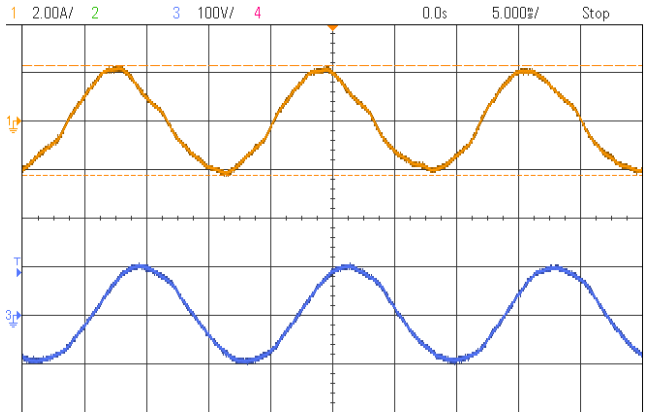


Figure 63 Ac-side current (top) and voltage (bottom) in the ac-dc parallel ac-link universal converter operating at 200 W (Experiment)

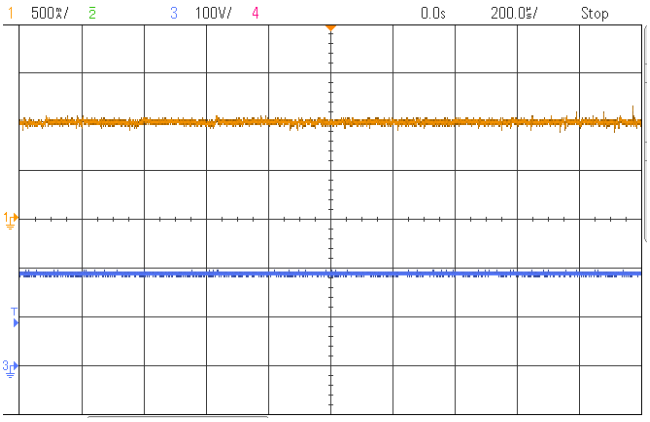


Figure 64 Dc-side current (top) and voltage (bottom) in the ac-dc parallel ac-link universal converter operating at 200 W (Experiment)

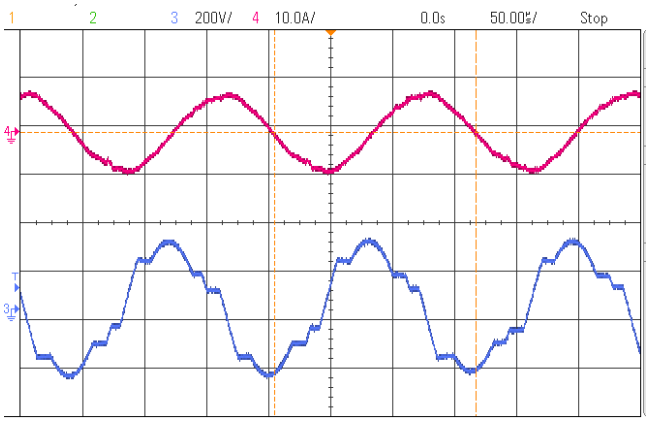


Figure 65 Link current (top) and voltage (bottom) in the ac-dc parallel ac-link universal converter operating at 200 W (Experiment)

2.9.1.4. Hybrid PV/Battery Inverter

This part verifies the performance of the hybrid parallel ac-link universal converter. Again, the PV/battery hybrid inverter is considered. Both the battery, when being discharged, and the PV are modeled by dc voltage sources. The battery, when being charged, is modeled by a resistor.

Table 5 summarizes the system specifications and the designed parameters. The performance of the converter during the first and second power-flow scenarios are similar to that of the dc-ac configuration, which was evaluated in part 2.9.1.2. Therefore, here we have only to focus on the third and the fourth power-flow scenarios.

TABLE 5 THE SPECIFICATIONS OF THE HYBRID PARALLEL AC-LINK UNIVERSAL POWER CONVERTER

Parameter	Value
PV voltage	150 V
Battery voltage	200 V
ac-side voltage	208 V
Link inductance	880 μH
Link capacitance	400 nF

Figure 66–Figure 68 verify the performance of the simulated converter during the third power-flow scenario. In this simulation it is assumed that the power generated by the PV is 600 W and the battery is charged with 1 A current. Figure 66 depicts the PV current, PV voltage, battery current, and battery voltage. Load current and link current/voltage are illustrated in Figure 67 and Figure 68, respectively. Negative battery current implies the battery is being charged. Link peak current is 16.8 A in this case. The link frequency is 3.8 kHz, and hence, the frequency of the unfiltered output current is 7.6 kHz. Considering that the cut-off frequency of the ac-side filter is 1.2 kHz, the

harmonics are mostly attenuated. The THD of the output current is 1.9% which is compatible with the corresponding standards.

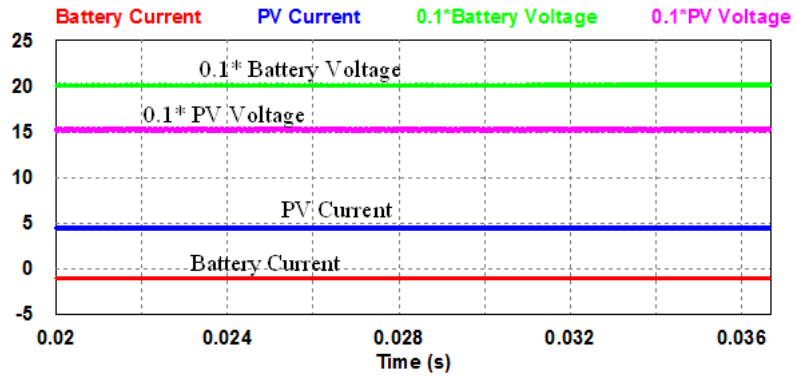


Figure 66 Scaled battery voltage, scaled PV voltage, PV current, and battery current in the hybrid parallel ac-link universal converter during the third power-flow scenario

Figure 69–Figure 71 illustrate the simulation results corresponding to the fourth power-flow scenario. In this simulation the battery and the PV are each assumed to provide 50% of the power required by the load, which is 800 W. Load currents are represented in Figure 69. The PV current, PV voltage, battery current, and battery voltage are represented in Figure 70. Figure 71 depicts the link current and voltage. The peak of the link current and the frequency of the link are 18.4 A and 3.34 kHz, respectively. The maximum voltage to which the link swings during mode 8 is, again, 330V.

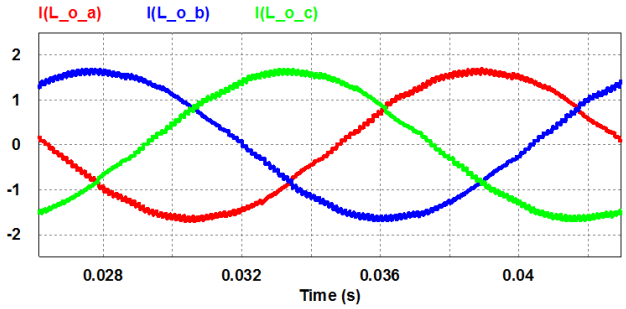


Figure 67 Ac-side currents in the hybrid parallel ac-link universal converter during the third power-flow scenario

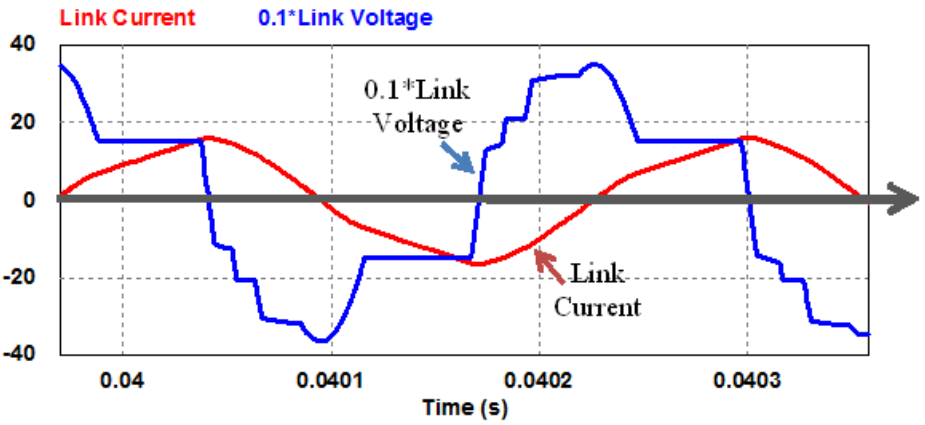


Figure 68 Link voltage and current in the hybrid parallel ac-link universal converter during the third power-flow scenario

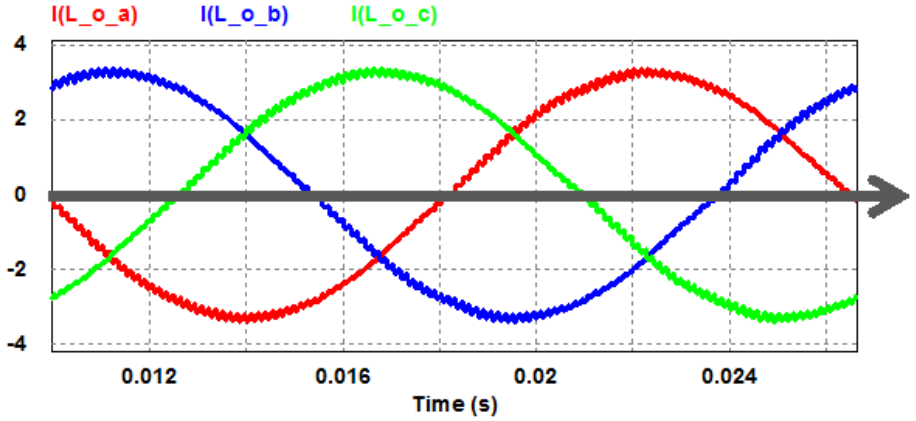


Figure 69 Ac-side currents in the hybrid parallel ac-link universal converter during the fourth power-flow scenario

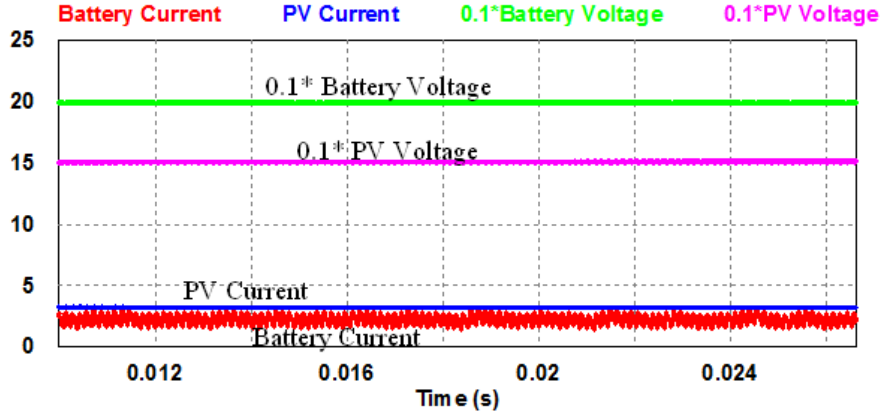


Figure 70 Scaled battery voltage, scaled PV voltage, PV current, and battery current in the hybrid parallel ac-link universal converter during the fourth power-flow scenario

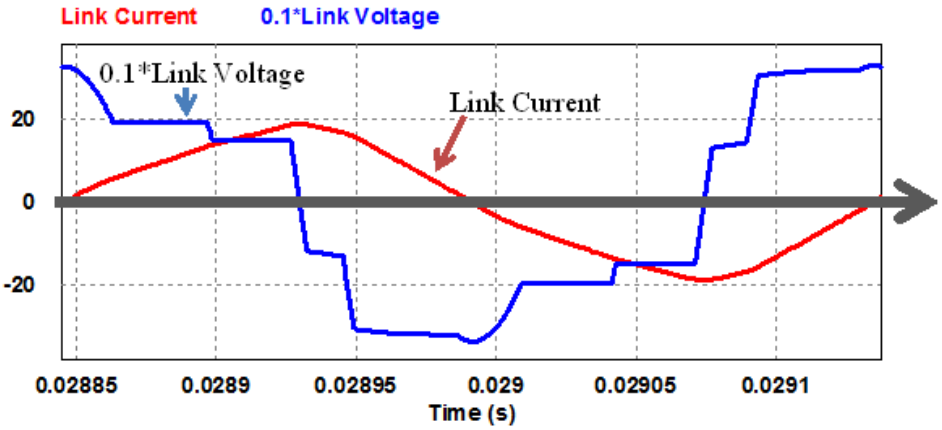


Figure 71 Link voltage and current in the hybrid parallel ac-link universal converter during the fourth power-flow scenario

Again, the multi-purpose prototype is used to experimentally evaluate the hybrid parallel ac-link converter. Figure 72 depicts different parts of the prototype. This prototype was tested at different power-flow scenarios using dc power supplies and resistive loads.

Figure 73–Figure 76 represent the experimental results corresponding to the third power-flow scenario. Similar to the simulation, it is assumed that the power generated by the PV is 600 W and the battery charge current is 1 A. Figure 73 represents the PV current and voltage. Battery current/voltage, load currents, and the link current/voltage are illustrated in Figure 74–Figure 76, respectively.

Similarly, Figure 77–Figure 80 verify the performance of the converter during the fourth power-flow scenario. The PV and battery each provide 50% of the required power, which is assumed to be 800 W in this case. Figure 77 and Figure 78 represent the PV current, the PV voltage, the battery current, and the battery voltage. Figure 79 and Figure 80 show ac-side currents and link current/voltage, respectively.

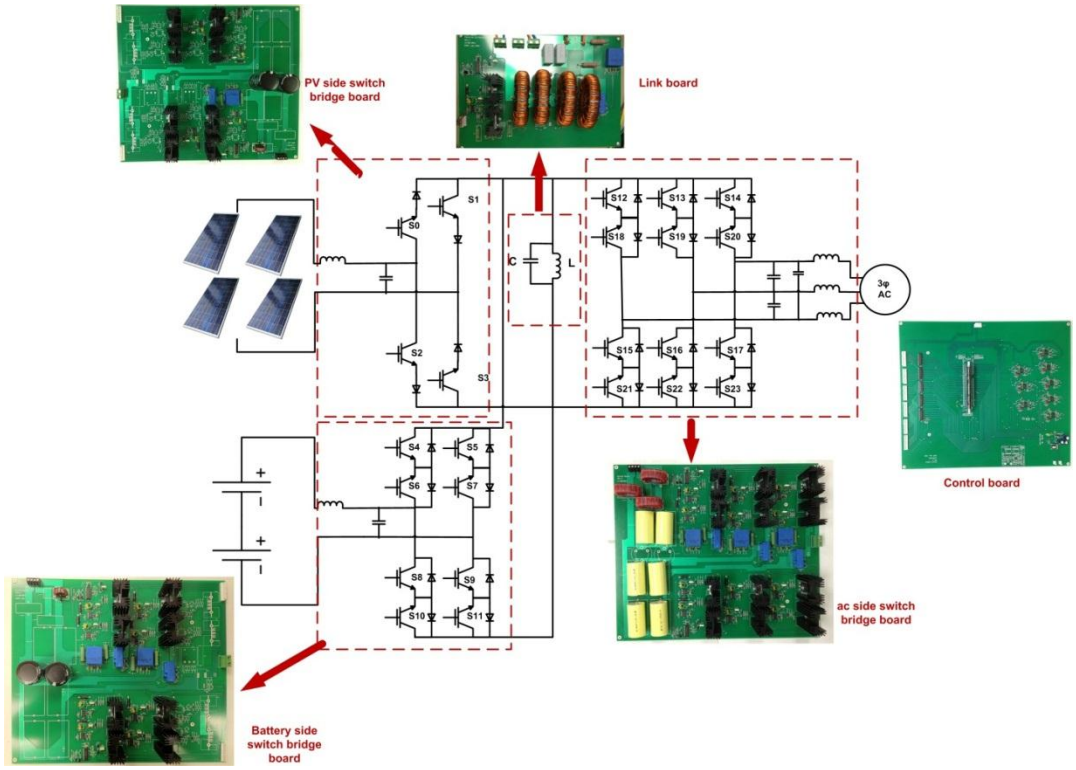


Figure 72 Different parts of the tested hybrid parallel ac-link universal converter

Table 6 summarizes the simulation and experimental results corresponding to different power-flow scenarios and compares them with theoretical values. For the 2nd power flow, the accurate analysis method introduced in part 2.5 has been used and the calculation results are very close to the simulation and experiment values. For the 3rd and 4th power-flow scenarios, equations derived in part 2.8, which neglect the resonating modes, have been employed, and hence, the theoretical values are not close to the experiment and simulation values when the link capacitance is 400 nF. Link capacitance of 400nF results in considerable resonating time. However, when the link capacitance is 40 nF, the resonating time is negligible; the aforementioned equations can accurately calculate the link frequency and link peak current.

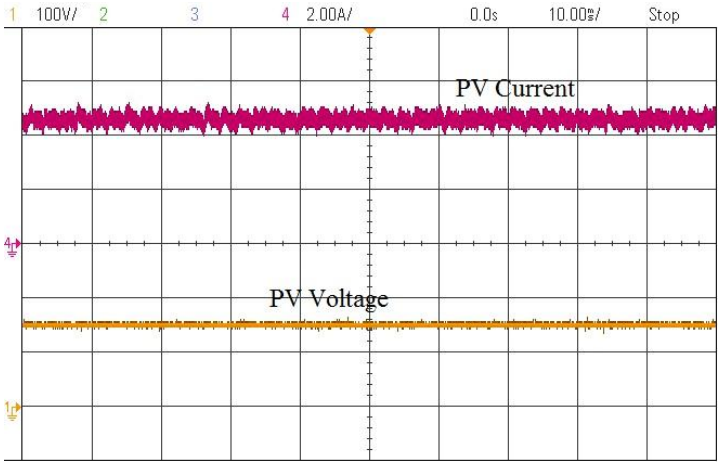


Figure 73 PV current (2 A/div) and voltage (100 V/div) in the hybrid parallel ac-link universal converter during the third power-flow scenario (experimental results), time scale: 10 ms/div

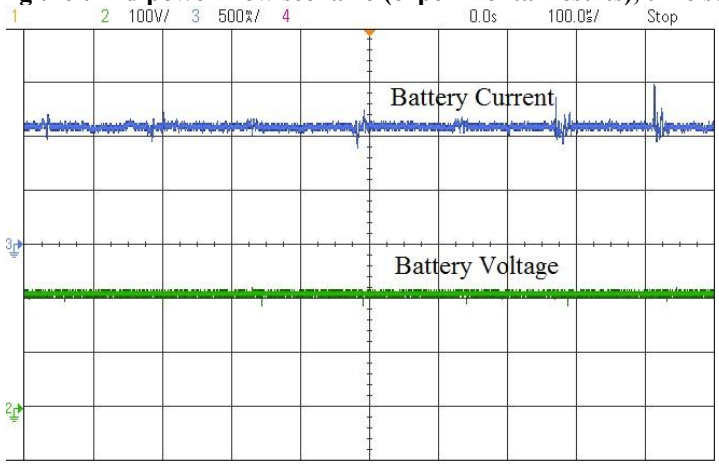


Figure 74 Battery current (0.5 A/div) and voltage (100 V/div) in the third power flow scenario (experimental results), time scale: 100 µs/div

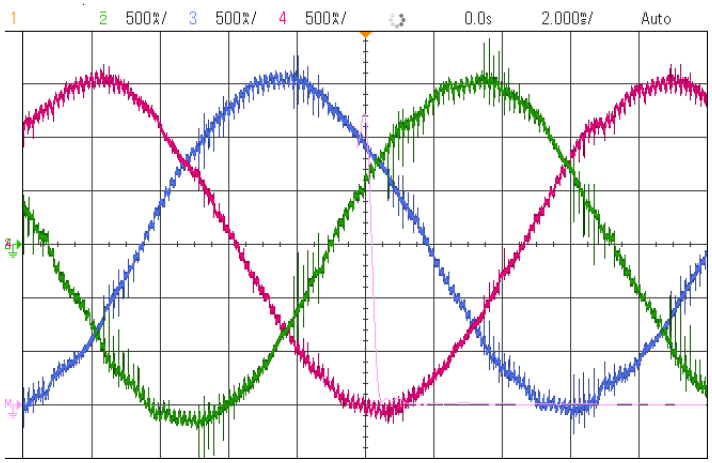


Figure 75 Ac-side current (0.5 A/div) in the hybrid parallel ac-link universal converter during the third power-flow scenario (experimental results), time scale: 2 ms/div

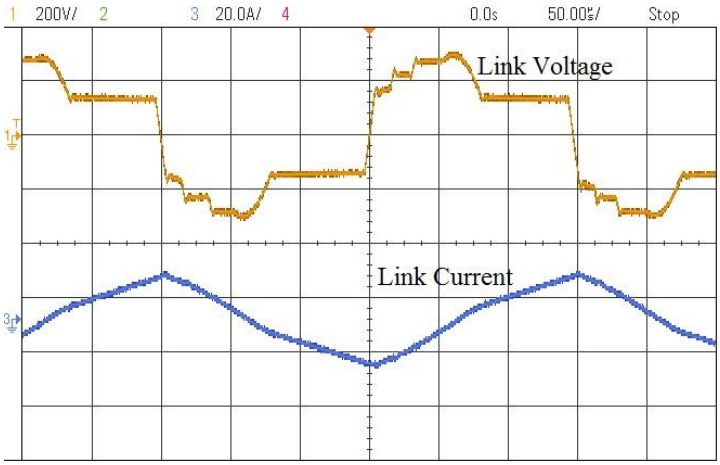


Figure 76 Link voltage (200 V/div) and current (20 A/div) in the hybrid parallel ac-link universal converter during the third power flow scenario (experimental results), time scale: 50 µs/div

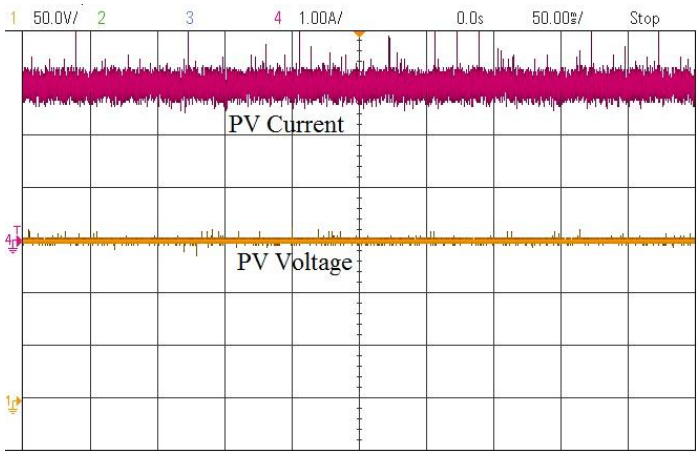


Figure 77 PV current (1 A/div) and voltage (50 V/div) in the hybrid parallel ac-link universal converter during the fourth power-flow scenario (experimental results), time scale: 50 ms/div

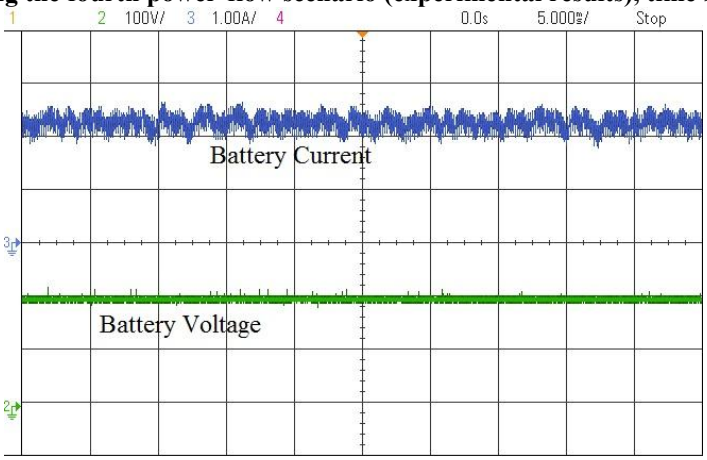


Figure 78 Battery current (1 A/div) and voltage (100 V/div) in the hybrid parallel ac-link universal converter during the fourth power-flow scenario (experimental results), time scale: 5 ms/div

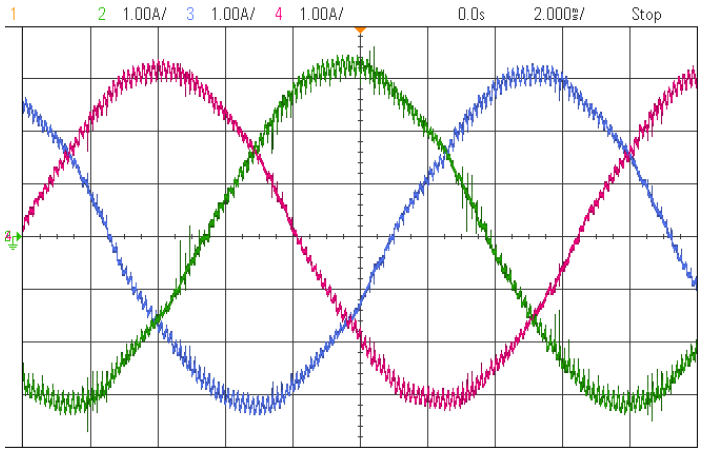


Figure 79 Ac-side current (1 A/div) in the hybrid parallel ac-link universal converter during the fourth power flow scenario (experimental results), time scale: 2 ms/div

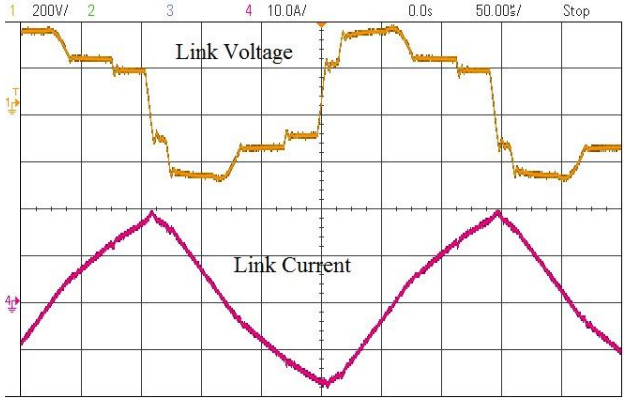


Figure 80 Link voltage (200 V/div) and current (10 A/div) in the hybrid parallel ac-link universal converter during the fourth power-flow scenario (experimental results), time scale: 50 µs/div

2.9.1.5. DC to Single-Phase AC Configuration

The dc to single phase ac inverters are among the most common types of power converters. They are mostly used in residential applications. The main difficulty in the dc to single-phase ac inverters is that the instantaneous input and output power cannot match. The input-side power must be dc, whereas the instantaneous output power is alternating with a frequency that is twice the output voltage/current frequency. The average ac-side power is equal to the dc-side power; however, a capacitor is required to consume or to provide the alternating part of the power.

TABLE 6 SUMMARY OF THE ANALYSIS, SIMULATION, AND EXPERIMENTAL EVALUATION OF THE HYBRID PARALLEL AC-LINK UNIVERSAL CONVERTER

	Link Peak Current (A)			Link Frequency (Hz)			Eff.	THD
	Cal.	Sim.	Exp.	Cal.	Sim.	Exp.		
2nd Power Flow Scenario	17.77	17.5	17.39	3750	3790	3759	90.48%	1.9%
3rd Power Flow Scenario C_{Link}=400 nF	13.92	16.8	17	4060	3816	3493	89.28%	1.6%
3rd Power Flow Scenario C_{Link} =40 nF		14.05	-		4043	-	-	-
4th Power Flow Scenario C_{Link}=400 nF	16.3	18.4	18.7	4010	3348	3482	89.38%	0.75%
4th Power Flow Scenario C_{Link} =40 nF		16.6	-		3905	-	-	-

Cal.: Calculation, Sim.: Simulation, Exp.: Experiment, Eff.: Efficiency

There are two solutions to implement the dc to single-phase ac parallel ac-link universal converter. The first solution is to use a large dc-side capacitor. The other solution is to use the hybrid ac-link universal power converter as an interface between the dc source, load, and a capacitor that consumes or provides the alternating part of the ac power. In this part simulation results corresponding to both solutions are presented.

Figure 81 represents the system configuration for the first solution. The parameters of the simulated system are listed in Table 7.

The frequency of the ac-side current and voltage is 60 Hz. Therefore, the frequency of the alternating part of the instantaneous power is 120 Hz. Given this, the reference input current (unfiltered current) includes a dc part and a 120 Hz alternating part. The cut-off frequency of the dc-side filter must be below 120 Hz to attenuate the alternating part and to generate a dc filtered current. Figure 82 represents the dc-side current (filtered) and voltage. The ac-side current and voltage are illustrated in Figure

83. In this case a resistive load is used. However, there is no limitation in the type of the load.

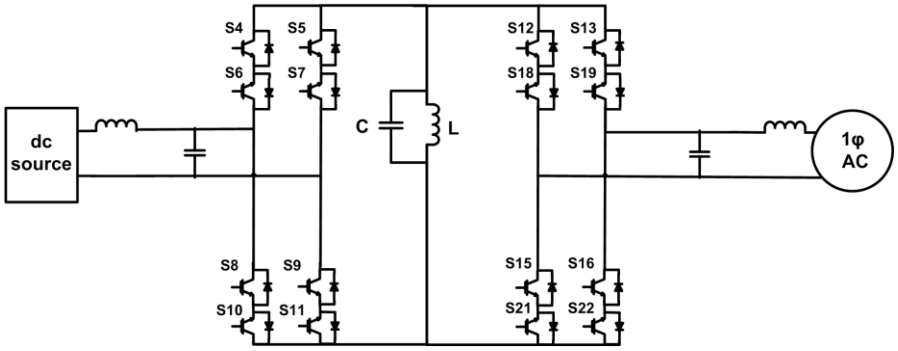


Figure 81 Dc to single-phase ac parallel ac-link universal converter (first solution)

The link current and voltage are shown in Figure 84. In this configuration, the link peak current changes by the instantaneous power of the load. As depicted in Figure 85, its lowest and highest link peak current values are 3.25 A and 75.84 A, respectively. Clearly, the lowest link peak current occurs at zero crossing of the load current. Figure 86 shows the link current and voltage at a point close to the zero crossing. At that point the link is mostly resonating as the duration of the power transfer modes are very short. The current of the dc-side capacitor is shown in Figure 87. The 120 Hz harmonic can be seen in this waveform.

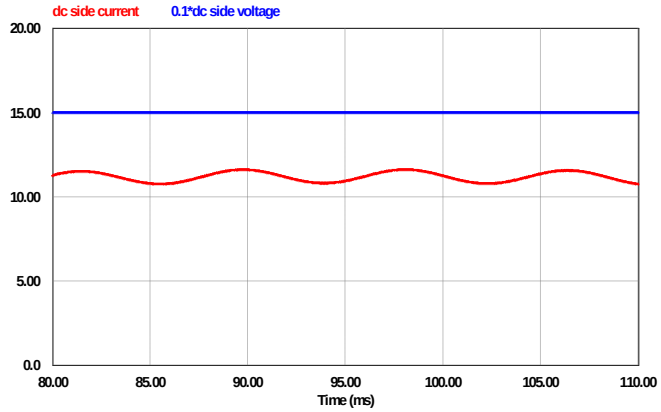


Figure 82 Dc-side current and scaled voltage in the dc to single-phase ac parallel ac-link universal converter (first solution)

TABLE 7 PARAMETERS OF THE DC-SINGLE PHASE AC CONVERTER (FIRST SOLUTION)

Parameter	Value
dc voltage	150 V
ac voltage	120 V
Link inductance	111 µH
Link capacitance	20 nF
dc-side filter inductance	4 mH
dc-side filter capacitance	100 mF
ac-side filter inductance	1 mH
ac-side filter capacitance	30 µF

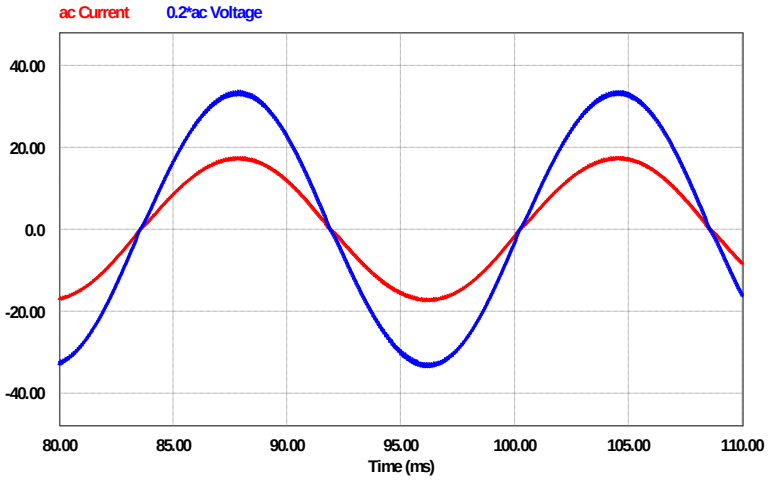


Figure 83 Ac-side current and scaled voltage in the dc to single-phase ac parallel ac-link universal converter (first solution)

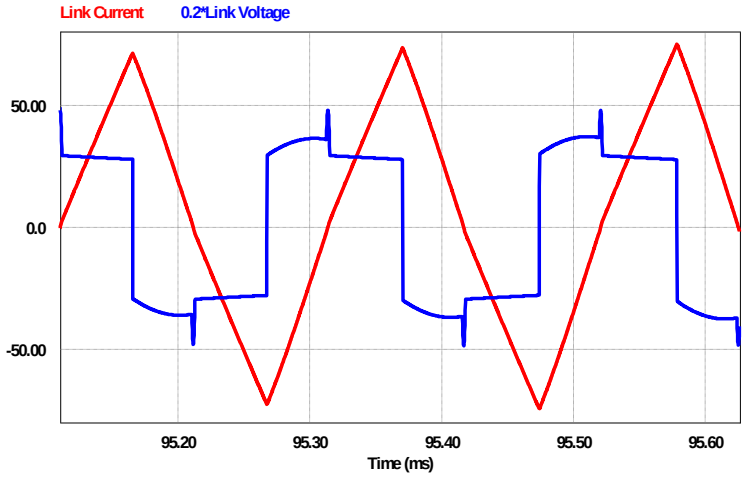


Figure 84 Link current and scaled voltage in the dc to single-phase ac parallel ac-link universal converter (first solution)

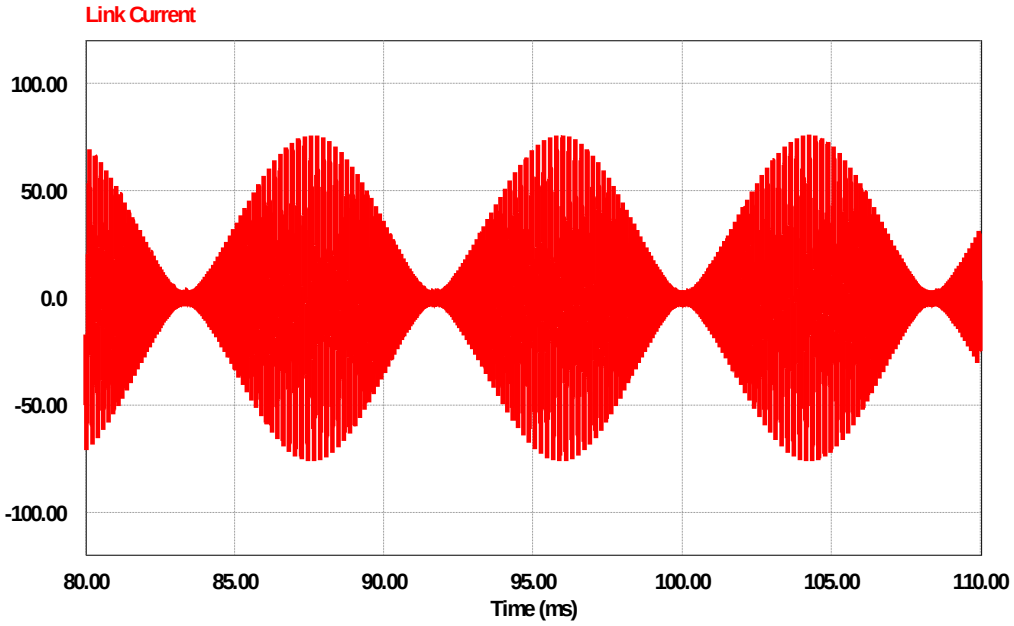


Figure 85 Link current in the dc to single-phase ac parallel ac-link universal converter (first solution)

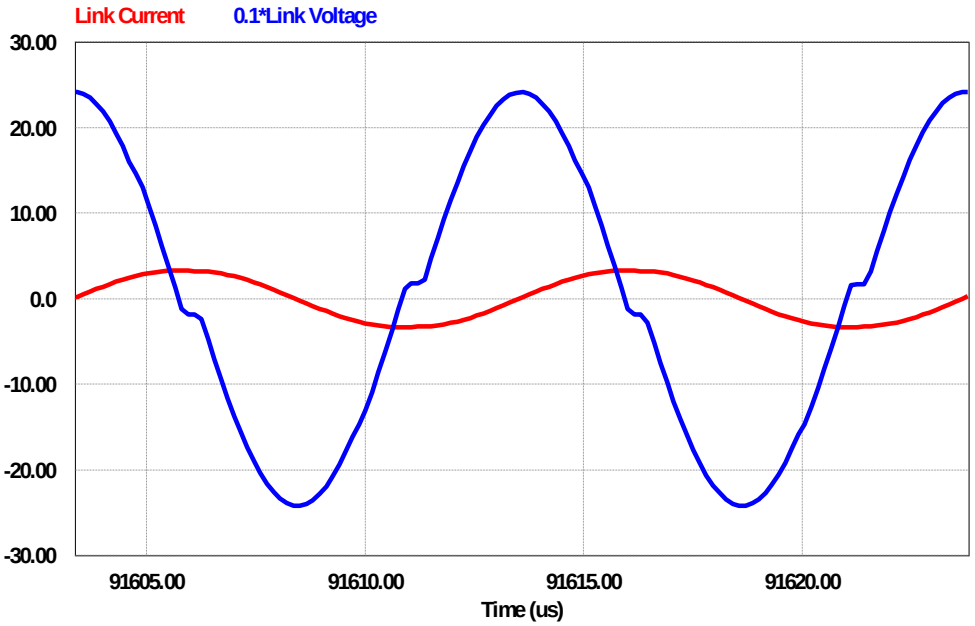


Figure 86 Link current and scaled voltage in the dc to single-phase ac parallel ac-link universal converter (first solution) when the load current is close to zero

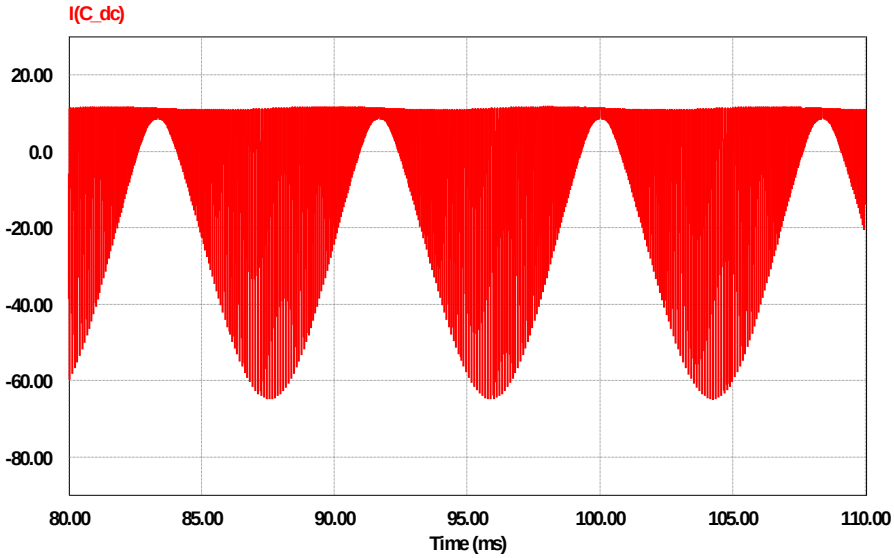


Figure 87 Current of the dc-side filter capacitor in the dc to single-phase ac parallel ac-link universal converter (first solution)

The system configuration using the second solution is illustrated in Figure 88. The parameters of the simulated system are summarized in Table 8. A 5 mF capacitor is placed across one of the terminals of this converter to provide or to consume the alternating part of the power. The voltage of this capacitor is 166 V. This converter operates similar to the hybrid PV/battery inverter introduced in the previous section. Whenever the instantaneous ac-side power is higher than the average power, which is equal to the dc-side power, the capacitor behaves as a source and along with the dc source provides the ac-side with the power it needs. In this case the operation of the converter is similar to the fourth power-flow scenario in the hybrid PV/battery inverter. When the instantaneous ac-side power is lower than the power generated by the dc source, the extra power will be fed into the capacitor and in this case the performance of the converter is similar to the third power-flow scenario in the hybrid PV/Battery inverter.

Figure 89 shows the dc source current and voltage. The current does not contain any low-frequency harmonics. The ac-side current and voltage are depicted in Figure 90. Again, a resistive load is used. Figure 91 and Figure 92 show the link current/voltage at two different points. In Figure 91, the capacitor acts as a load because the alternating power is lower than the average power. However, in Figure 92 the alternating power is higher than the average power and the capacitor acts as a source. The link peak current varies in a much narrower range in this case. The highest and lowest link peak currents are 38 A and 67 A, respectively.

The capacitor current and voltage are shown in Figure 93. The frequency of the current is 120 Hz.

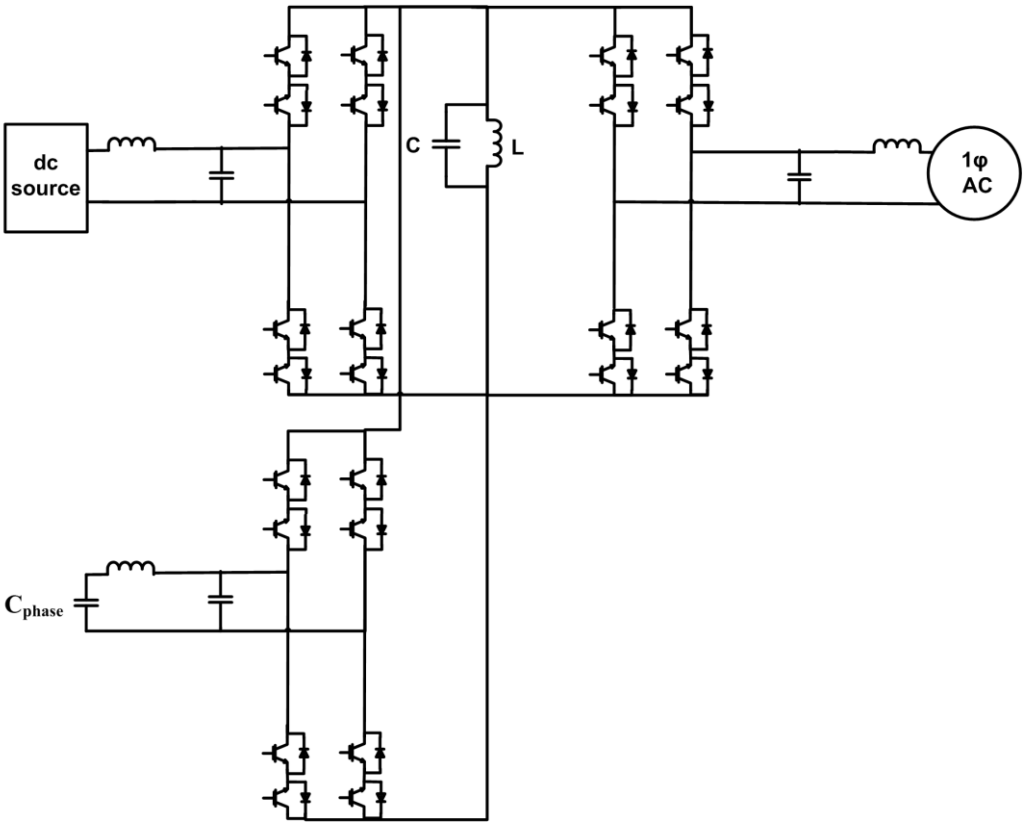


Figure 88 Dc to single-phase ac parallel ac-link universal converter (second solution)

TABLE 8 PARAMETERS OF THE SIMULATED DC-SINGLE PHASE AC PARALLEL AC-LINK UNIVERSAL CONVERTER (SECOND SOLUTION)

Parameter	Value
dc Voltage	150 V
ac Voltage	120 V
Capacitor's voltage	166 V
Capacitance of the capacitor added as a new source/load (C_{phase})	5 mF
Link inductance	111 µH
Link Capacitance	20 nF
Input side filter inductance	100 µH
Input side filter capacitance	2 mF
Output side filter inductance	1 mH
Output side filter capacitance	30 µF

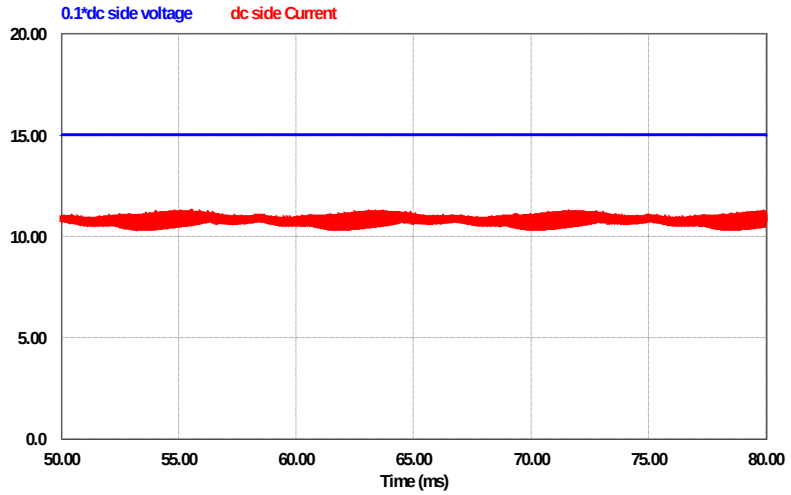


Figure 89 Dc-side current and scaled voltage in the dc to single-phase ac parallel ac-link universal converter (second solution)

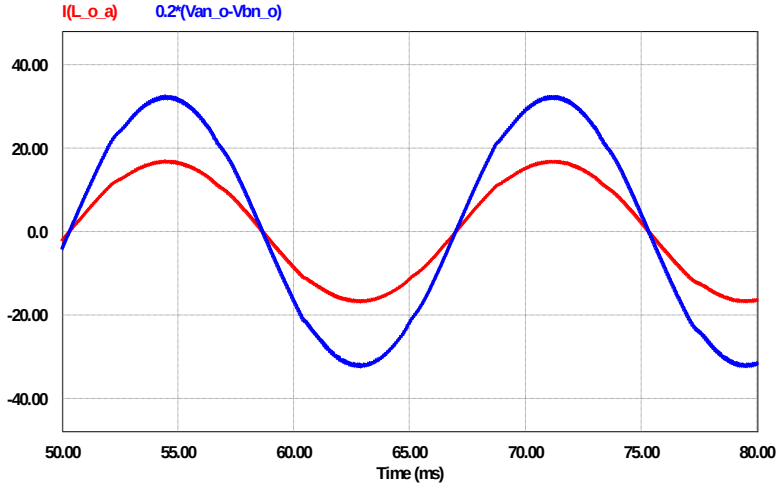


Figure 90 Load current and scaled voltage in the dc to single-phase ac parallel ac-link universal converter (second solution)

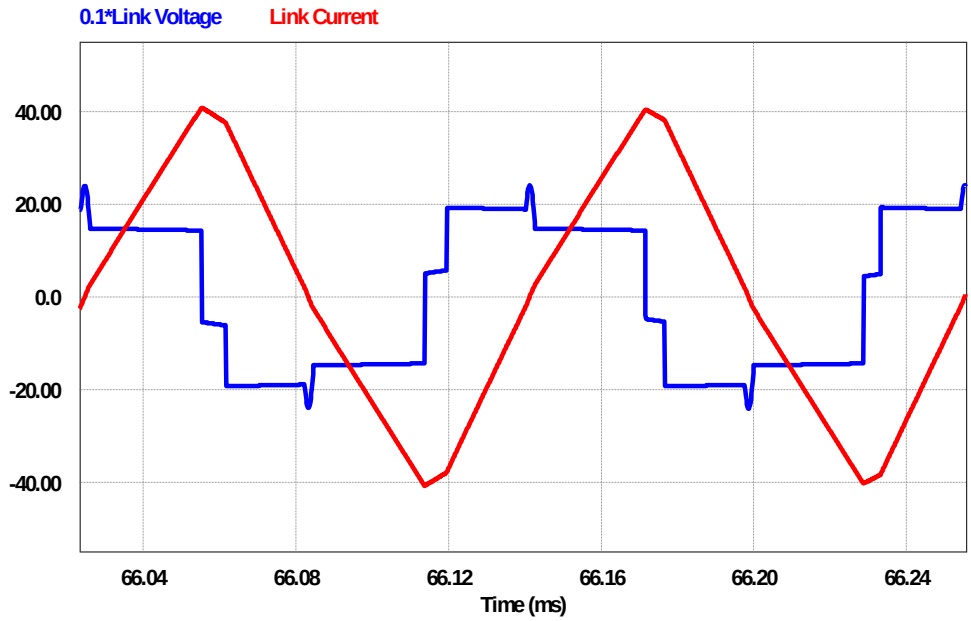


Figure 91 Link current and scaled voltage in the dc to single-phase ac parallel ac-link universal converter (second solution) when the capacitor acts as a load

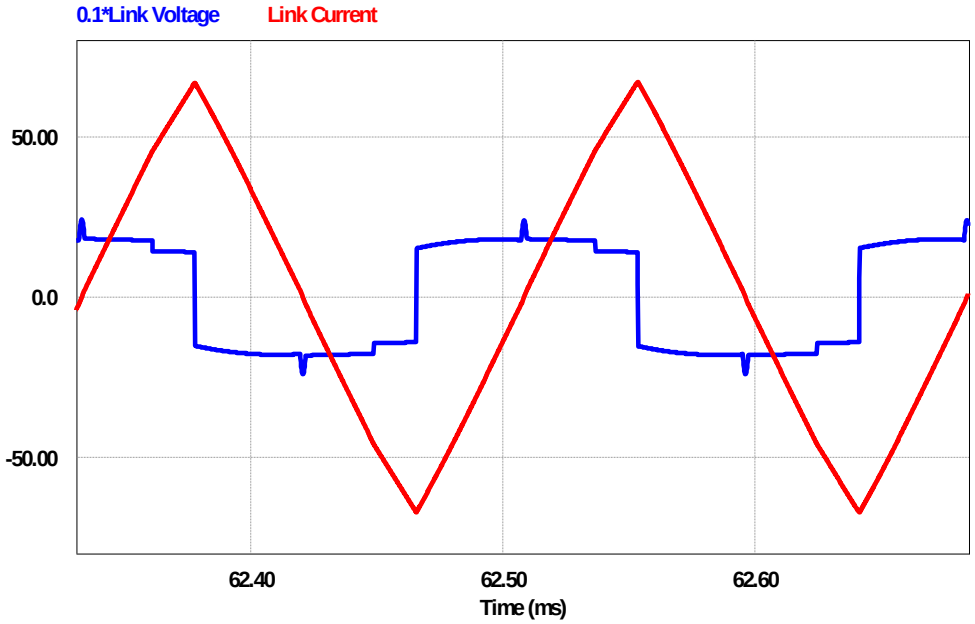


Figure 92 Link current and scaled voltage in the dc to single phase ac parallel ac-link universal converter (second solution) when the capacitor acts as a source

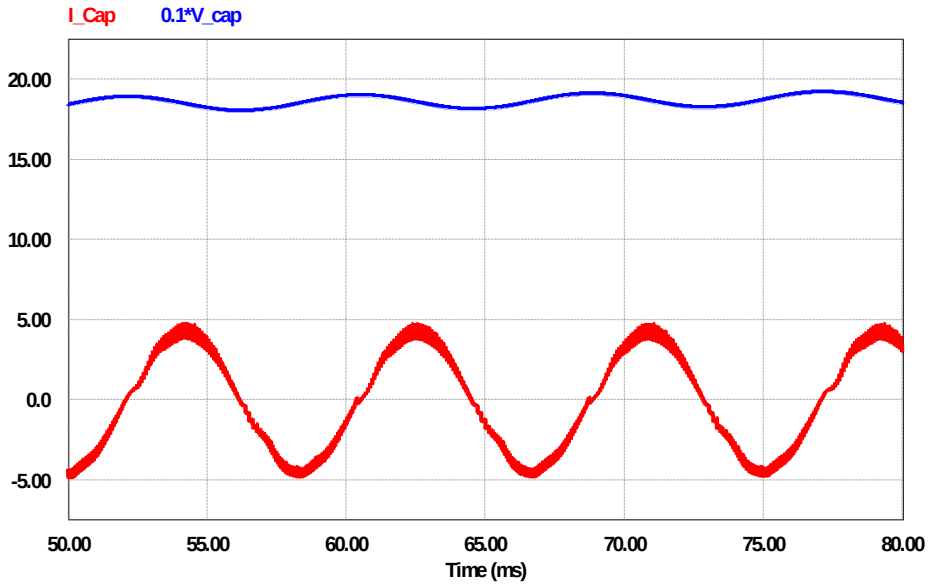


Figure 93 Capacitor current and scaled voltage in the dc to single-phase ac parallel ac-link universal converter (second solution)

2.9.2. Medium Power Tests

The medium power tests evaluate the performance of a 30 kW parallel ac-link universal power converter as a PV inverter and a variable frequency drive.

2.9.2.1. 30 kW Three-phase PV Inverter

In this part the simulation and experimental results of a 30 kW dc to three-phase ac parallel ac-link universal converter used for PV application are presented. For the experimental results a 30 kW dc-ac parallel ac-link universal power converter developed and manufacture by Ideal Power Converters Co. is used. Several of these inverters are currently mounted in the Austin Convention center and have been working continuously for more than a year. The parameters of this 30 kW system are summarized in Table 9. Figure 94–Figure 103 represent the simulation results. Figure 94 represents the input voltage and current at full power. The input voltage is 700 V and the input current is 43

A. The output current along with the output voltage are illustrated in Figure 95. In this case the power factor is close to unity and the frequency is 60 Hz.

Figure 96 and Figure 97 represent the link voltage and current, respectively. The link current and voltage are both alternating. Since the frequency of the link (7200 Hz) is much higher than the frequency of the line (60 Hz), the link voltage and current are illustrated in these figures over a short time interval. As seen in these figures, the predetermined voltage to which the link resonates during mode 6 is set at 850V. Moreover, the peak of the link current is 200A, although during mode 1 the link current increases by 180 A. During mode 2, when the link resonates, its peak current reaches 200 A. as mentioned earlier, at lower power levels the peak of the link current will be lower than that of the full power. Figure 98 represents the link voltage and current at 15 kW. As seen in this figure the predetermined voltage to which the link resonates during mode 6 is still set at 850V. Although the PV voltage has dropped to 350 V, the maximum output line-to-line voltage is still 679 V. The peak of the link current in this case is about 147 A. Again, the resonating time is noticeable due to using 0.8 μF link capacitance.

As mentioned earlier, one of the merits of this inverter is the possibility of both stepping up and stepping down the voltage. In Figure 94–Figure 97, the peak of the line-to-line output voltage is lower than the input voltage ; therefore, the inverter is stepping down the voltage; whereas in Figure 98, the input voltage is lower than the peak of line-to-line output voltage and thus the inverter is stepping up the voltage.

Maximum Power Point Tracking (MPPT) is essential in PV inverters. Similar to other PV inverters, this inverter can perform MPPT, as it can follow any references within its range. Figure 99 represents the ac-side current/voltage when the irradiance drops from 850 w/m^2 to 650 w/m^2 (at t=20 ms). The temperature is assumed to be 25 °C. Figure 100 depicts the ac-side current/voltage when the temperature increases from 25°C to 50°C (at t=20 ms). Although a change in the temperature usually takes place gradually, in order to see the effect of this change on the behavior of the inverter, a sharp change is considered in this simulation. For the case shown in Figure 100, the irradiance is 850 w/m^2.

TABLE 9 PARAMETERS OF THE 30 KW DC-AC PARALLEL AC-LINK UNIVERSAL POWER CONVERTER USED AS A PV INVERTER

Parameter	**Value**
Nominal PV voltage	700 V
Output voltage	480 V (rms, line to line)
Link inductance	110 µH
Link capacitance	0.8 µF
Peak of link Current	200 A
Link frequency	7.2 kHz
PV-side filter	Inductance: 200 µH Capacitance: 150 µF
ac-side filter	Inductance: 50 µH Capacitance: 72 µF (line to line)

Another important issue to study is the behavior of the proposed inverter during the grid fault. As mentioned earlier this inverter can inject reactive power into the grid during voltage sags. To provide the low voltage ride through (LVRT) feature, the PV-side switches should be replaced by bidirectional switches, as illustrated in Figure 101. Figure 102 depicts the ac-side current/voltage when the output voltage drops to 10% of its nominal value (at t=0.016 s). As seen, the power factor is almost zero in this case. PV

current and voltage are represented in Figure 103. The active power drawn from the PV in this case is equal to the losses of the inverter.

The 30 kW inverter fabricated by Ideal Power Converters Co., which has the same specifications as the simulated inverter, is shown in Figure 104. This inverter, which interfaces the PV modules and the grid, was installed in the Austin Convention Center more than a year ago by Ideal Power Converters Co. [43]. Figure 105 represents the input voltage and current at full power. The input voltage at full power is 700V and the input current is set at 45 A. The difference between this current and the input current in simulation (43 A) is due to the power losses which could not be modeled in the simulation. The output current and voltage are depicted in Figure 106. Similar to the simulation, the peak of the output current is regulated at 51 A. Figure 107 represents the link voltage and current waveforms while the inverter is running at full power. Peak current is almost 200 A, which is the same as the simulation result.

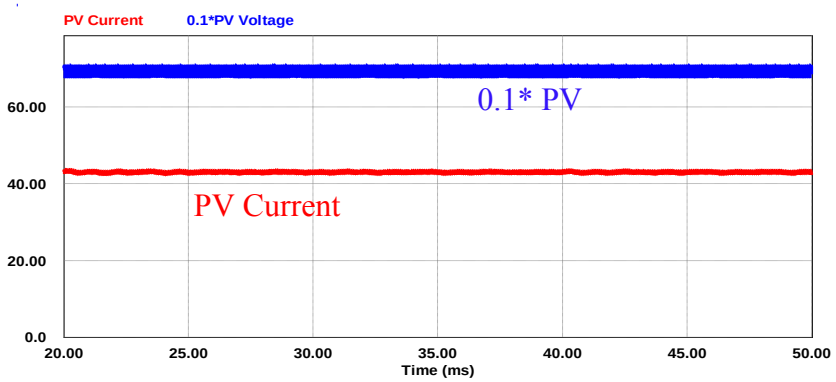


Figure 94 PV current and scaled voltage in the 30 kW dc-ac parallel ac-link universal power converter at full power

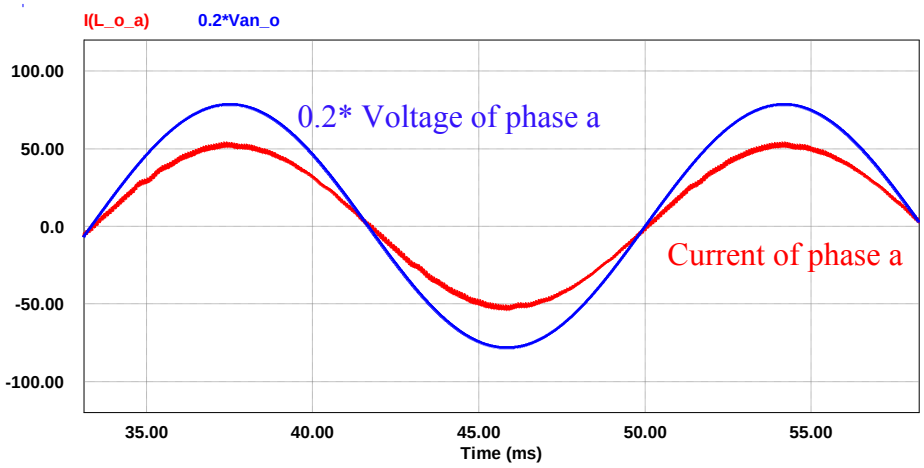


Figure 95 Ac-side current and scaled voltage in the 30 kW dc-ac parallel ac-link universal power converter at full power

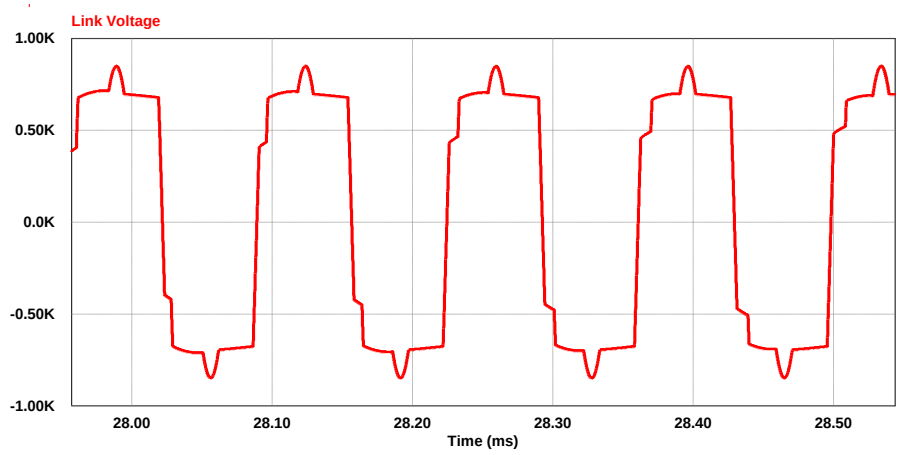


Figure 96 Link voltage in the 30 kW dc-ac parallel ac-link universal power converter at full power

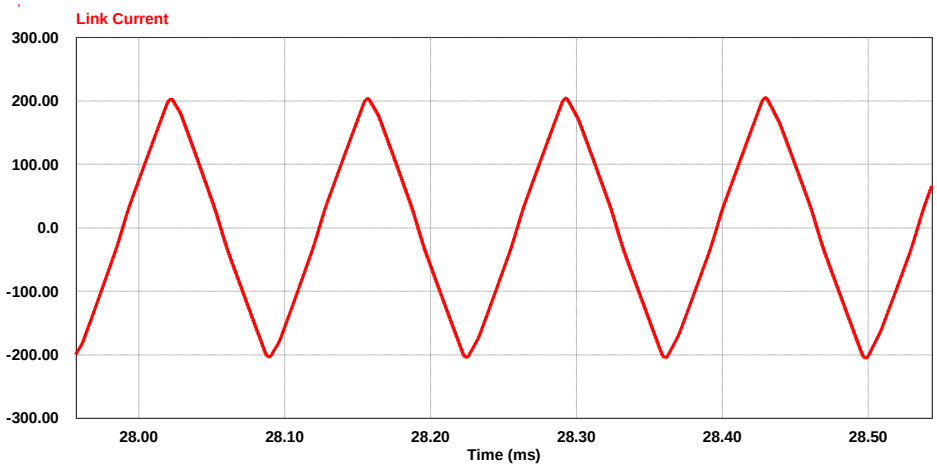


Figure 97 Link current in the 30 kW dc-ac parallel ac-link universal power converter at full power

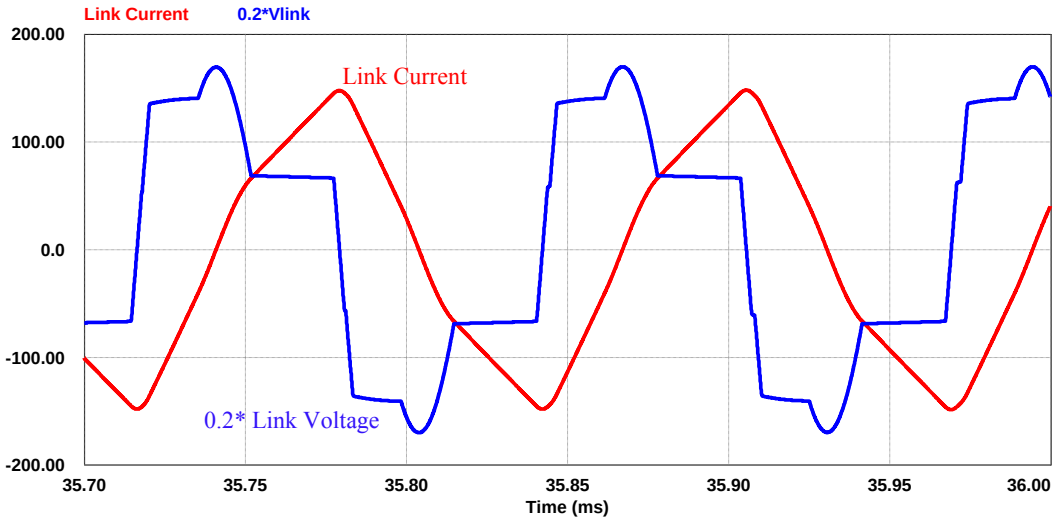


Figure 98 Link current and voltage in the dc-ac parallel ac-link universal power converter operating at 15 kW

Figure 108 represents the ac-side current and voltage when the inverter is operating at 25 kW. As seen in Figure 106 and Figure 108, the ac-side current contains low-frequency harmonics that are related to low-frequency components of the grid voltage. Due to the existence of nonlinear loads, the grid voltage is distorted by harmonics. Figure 109 shows the fast Fourier transform (FFT) of the line to neutral voltage when the inverter is turned off. To better show the low-frequency harmonics the zoomed-in image of the FFT is represented. Regardless of the type of the inverter employed, these low-frequency voltage harmonics generate low-frequency current harmonics. Figure 110 depicts the FFT of the load current corresponding to Figure 108. As seen in this figure, the line current contains the same harmonics as the grid voltage.

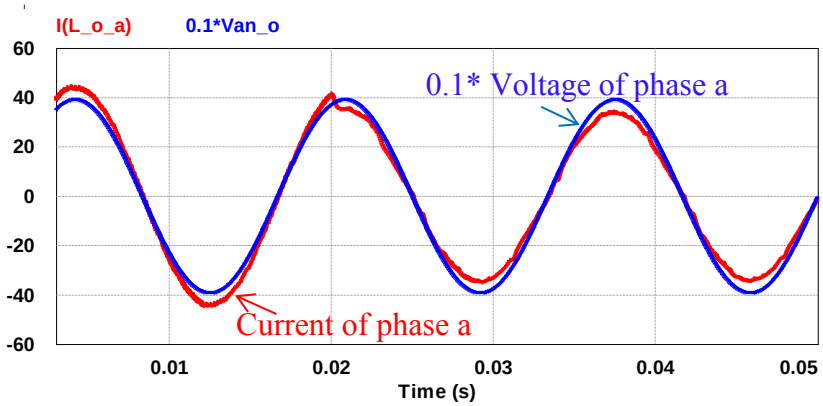


Figure 99 Ac-side current and scaled voltage in the 30 kW dc-ac parallel ac-link universal power converter when the irradiance drops from 850 w/m^2 to 650 w/m^2

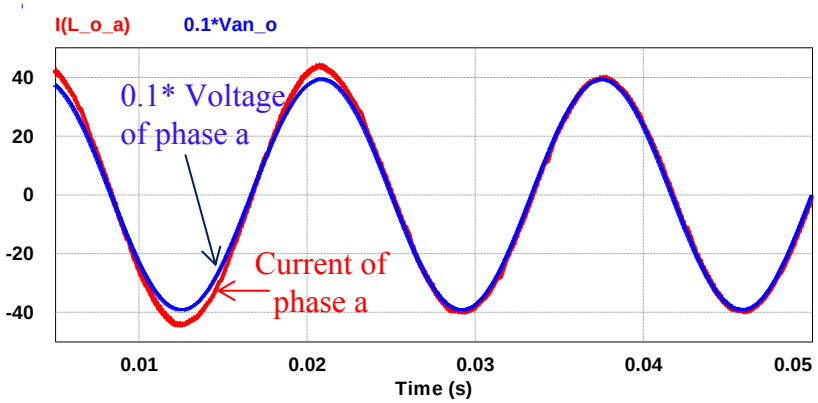


Figure 100 Ac-side current and voltage in the 30 kW dc-ac parallel ac-link universal power converter when the temperature changes from 25 °C to 50 °C

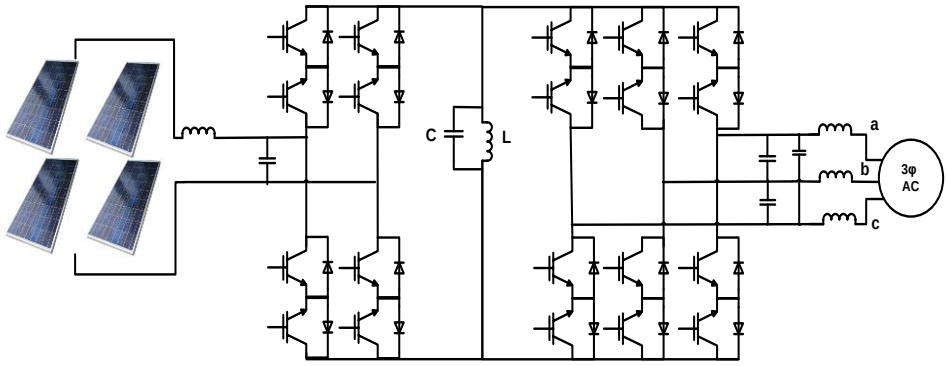


Figure 101 Dc-ac parallel ac-link universal power converter in case LVRT feature is needed

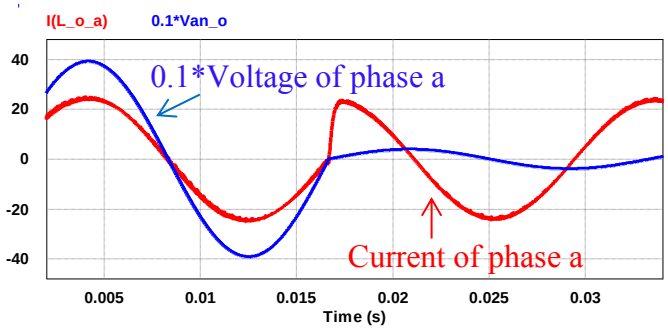


Figure 102 Ac-side current and voltage in the 30 kW dc-ac parallel ac-link universal power converter when the ac-side voltage drops to 10% of its nominal value (at t=0.016 s)

The link current and voltage when the prototype is operating at 15 kW and the PV voltage is 350 V are represented in Figure 111. As shown in this figure, the peak of the link current is 144 A, which is very close to the simulation results. This inverter is capable of operating at very low power levels as well. Figure 112 represents the link current and voltage at 3.75 kW (12.5% of the rated power). As seen in this figure, at this power level the resonating time is longer than the power transfer time. Figure 113 depicts the PV current and voltage at almost 20% of the rated power. The ac-side current and voltage when the inverter is operating at this power level are shown in Figure 114. Similar to the full-power operation the ac-side current contains 5th, 7th, 11th and 13th harmonics, which are generated by the low-frequency components of the grid voltage. In the case of low power, the fundamental component of the current is smaller as compared to the case of full power; however, the low-frequency harmonics are the same in both cases. Hence, the THD is higher in the case of low power.

Figure 115 represents the measured California Energy Commission (CEC) efficiency of this inverter. As shown in this figure, the efficiency of the inverter varies between 94% and 96.5% throughout the whole power range [43].

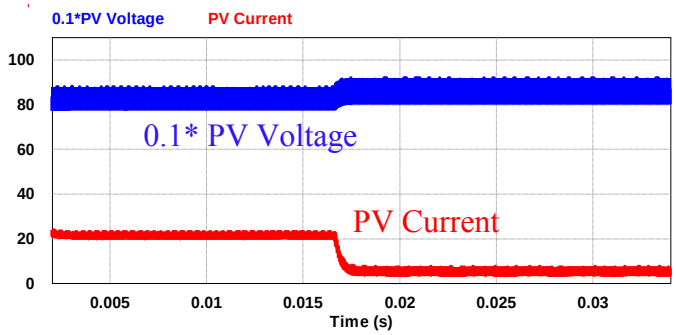


Figure 103 PV current and voltage in the 30 kW dc-ac parallel ac-link universal power converter when the ac-side voltage drops to 10% of its nominal value (at t=0.016 s)

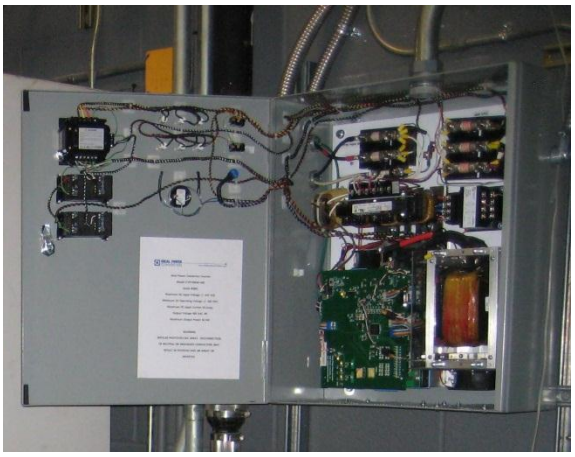


Figure 104 30 kW inverter developed and manufactured by Ideal Power Converters Co.

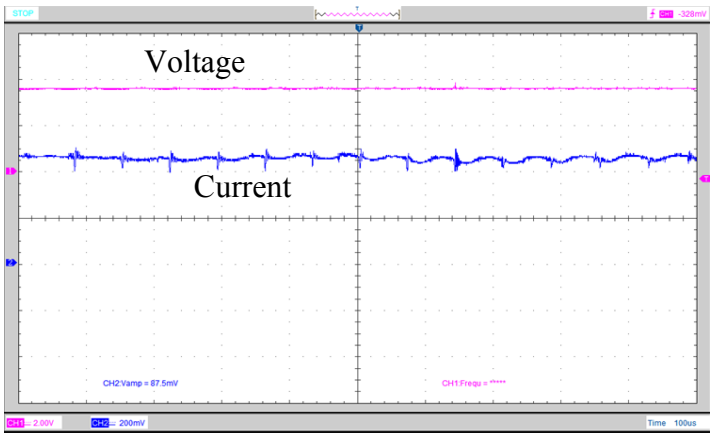


Figure 105 Dc-side current (20A/division) and dc-side voltage (400V/division) in the 30 kW dc-ac parallel ac-link universal power converter (experiment)

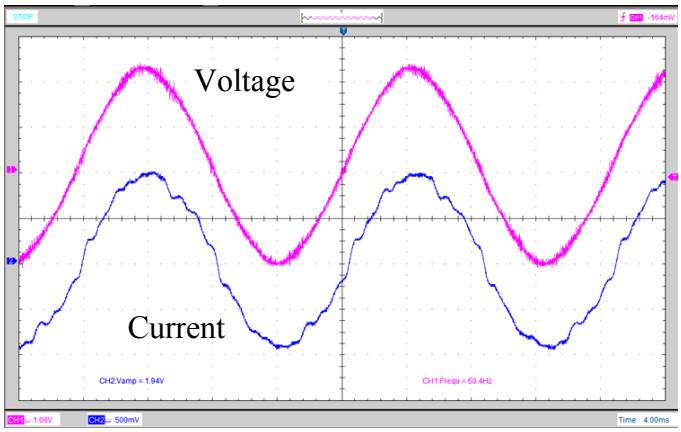


Figure 106 Ac-side voltage (200V/division) and ac-side current (30A/division) in the 30 kW dc-ac parallel ac-link universal power converter (experiment)

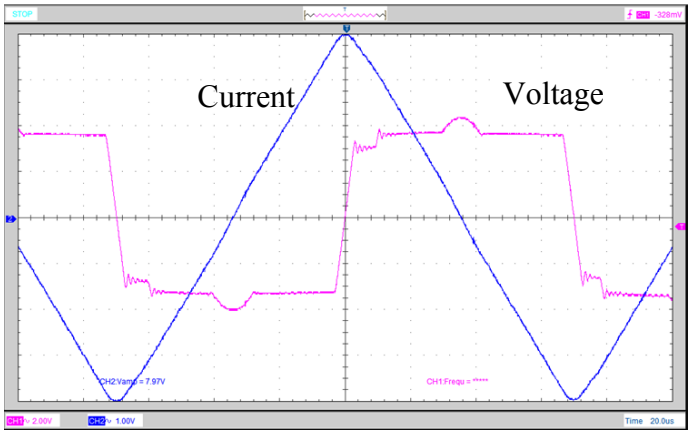


Figure 107 Link current (50A/division) and link voltage (400V/division) in the 30 kW dc-ac parallel ac-link universal power converter at full power (experiment)

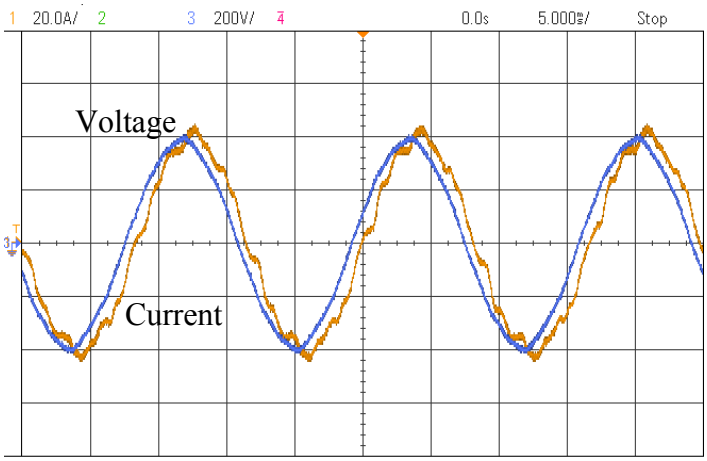


Figure 108 Ac-side current (20 A/ division) and voltage (200 V/division) in the 30 kW dc-ac parallel ac-link universal power converter running at 25 kW (experiment)

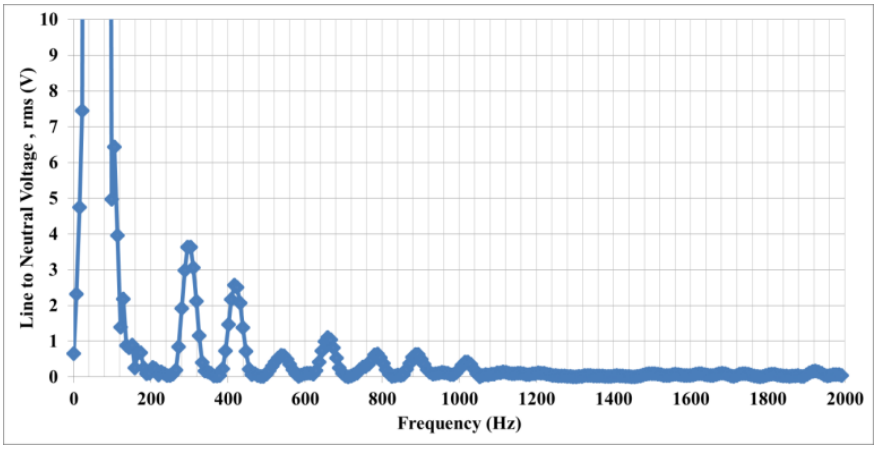


Figure 109 FFT of the line to neutral grid voltage (experiment)

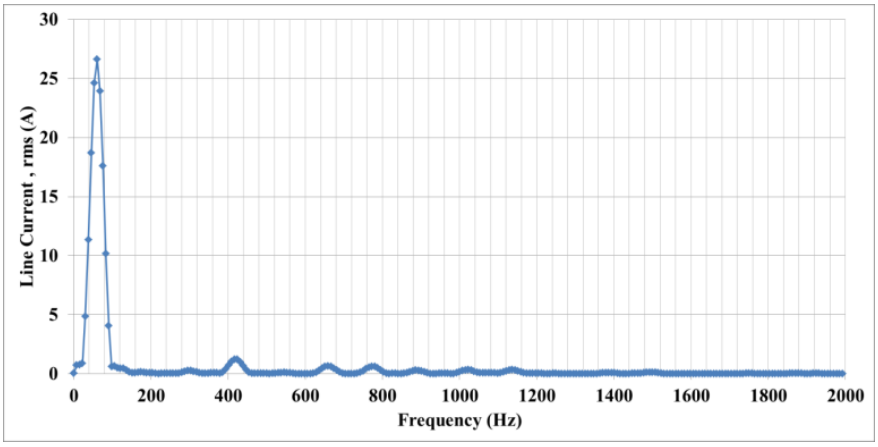


Figure 110 FFT of the load current in the dc-ac parallel ac-link universal power converter operating at 25 kW (experiment)

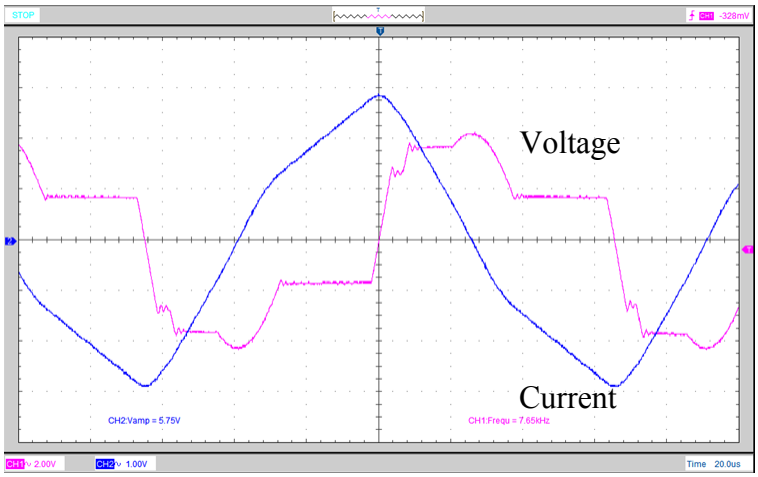


Figure 111 Link current (50A/division) and link voltage (400V/division) in the dc-ac parallel ac-link universal power converter operating at 15 kW (experiment)

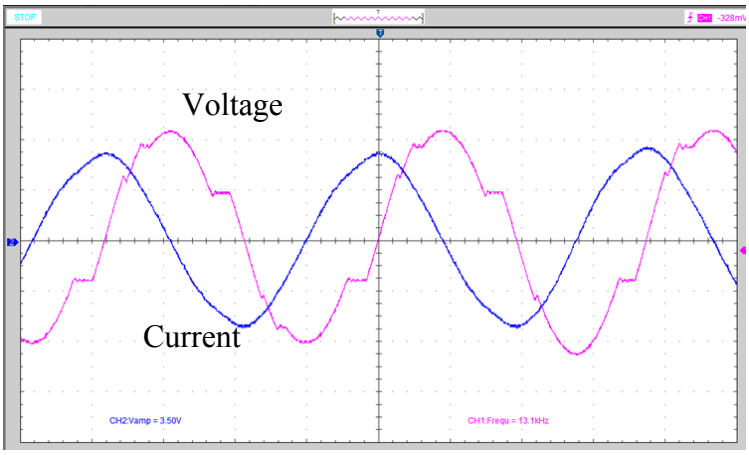


Figure 112 Link current (50A/division) and link voltage (400V/division) in the dc-ac parallel ac-link universal power converter operating at 3.75 kW (experiment)

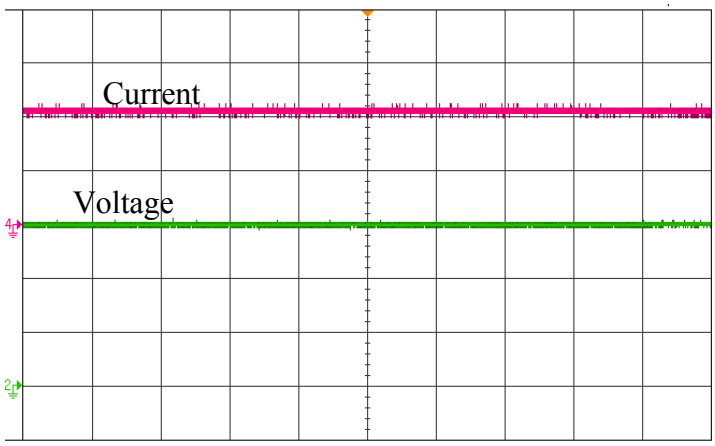


Figure 113 PV current (5A/division) and PV voltage (200V/division) in the dc-ac parallel ac-link universal power converter operating at 6.2 kW (experiment)

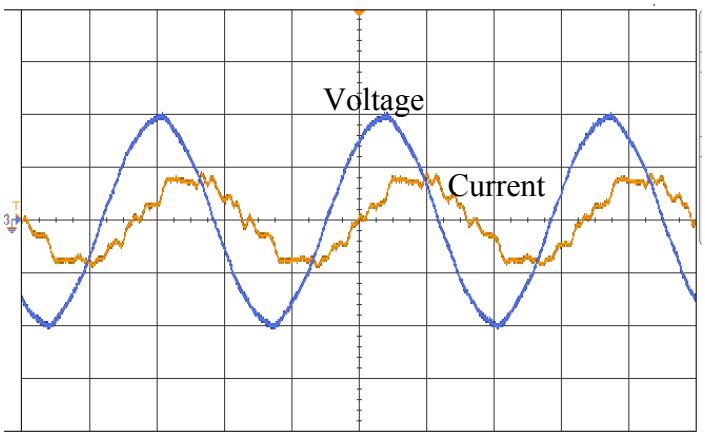


Figure 114 Ac-side current (20A/division) and ac-side voltage (200V/division) in the dc-ac parallel ac-link universal power converter operating at 6.2 kW (experiment)

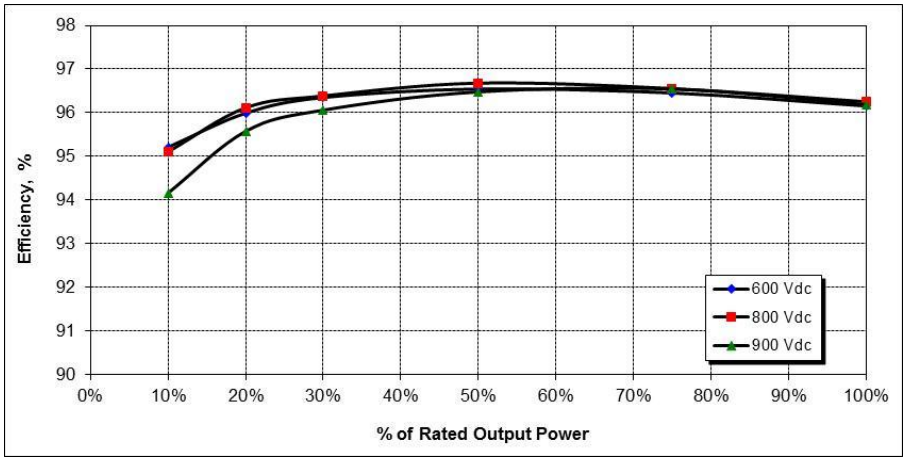


Figure 115 CEC Efficiency Curve of the 30 kW dc-ac parallel ac-link universal power converter (experiment) [43]

2.9.2.2. 30 kW Variable Frequency Drive

In this part the application of parallel ac-link universal converter in variable frequency drive (VFD) using the vector control scheme is studied.

The field oriented control method is widely used for controlling the speed and torque of induction machines. Here the indirect field orientation is considered. This method makes use of the fact that satisfying the slip relation is a necessary and sufficient condition to produce field orientation [44].

As illustrated in Figure 116, the field oriented control block determines the stator reference current, which is the output reference current of the converter. The flux is assumed to be constant. The q-axis stator reference current in the synchronous reference frame is calculated based on the reference speed and the actual speed of the motor using a Proportional-Integral (PI) controller. The electrical angular velocity (ω_e) can be calculated by:

$$\omega_e = S.\omega_e + \omega_r \tag{64}$$

Where S is the slip and ω_r is the electrical speed of the rotor and can be calculated using the following expression:

$$\omega_r = \frac{P}{2}\omega_m \tag{65}$$

In the above equation ω_m is the mechanical speed of the rotor and P is the number of the poles. $S.\omega_e$ in (64) can be determined using the following equation:

$$S.\omega_e = \frac{r_r}{L_r} * \frac{i_{qs}^e}{i_{ds}^e} \tag{66}$$

In the above equation, r_r is the rotor resistance and L_r is the rotor winding inductance. Since the flux has been considered constant, (66) does not contain any transient terms. In case the flux is not constant, the following equation should be used instead of (66):

$$S.w_e = \frac{r_r}{L_r} * \frac{i_{qs}^e}{\left(1+\frac{L_r}{r_r}*\frac{d}{dt}\right)*i_{ds}^e} \tag{67}$$

Finally, θ_e can be calculated by integrating ω_e. The stator three-phase reference currents can be easily calculated using the d-q reference currents and the electrical angle (θ_e).

The input reference current of the converter is derived based on the input power which can be estimated using the following equation:

$$Input\ Power = Output\ Power + Losses = \frac{3*I_r^2*r_r}{S} * (1-S) + 3 * I_s^2 * r_s + 3 * I_r^2 * r_r \tag{68}$$

In the above equation I_s, I_r and r_s are the stator rms current, the rotor rms current, and the stator resistance, respectively. The controller can control the currents of the

converter to meet their references and hence the desire speed can be achieved. A more accurate method is similar to the method explained for the LVRT. In this case the input reference currents are not needed.

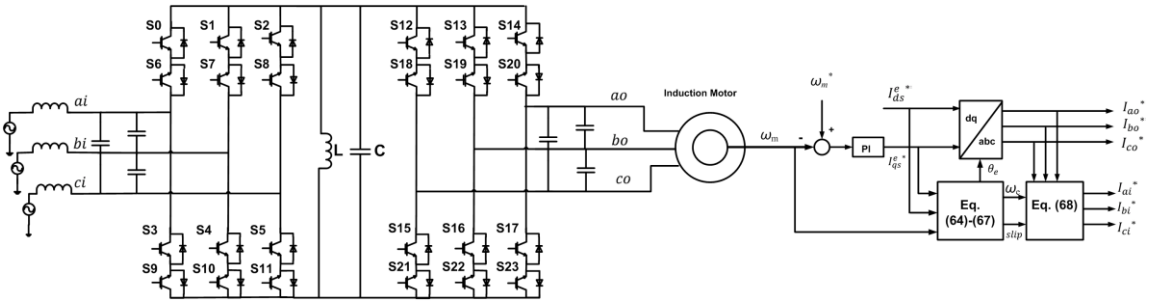


Figure 116 ac-ac parallel ac-link universal converter as a VFD

A 30 kW system was designed and simulated in PSim. The parameters of the motor and the converter are listed in Table 10 [45].

TABLE 10 PARAMETERS OF THE 30 KW AC-AC PARALLEL AC-LINK UNIVERSAL CONVERTER AND THE 20 HP INDUCTION MACHINE

Parameter	Value
Converter	
Link Frequency	3 kHz
Link Inductance	110 µH
Link Capacitance	0.9 µF
Peak of link current at full power	225 A
Induction machine (20 hp, 220 V, three phase, 60 Hz)	
r_s	0.1062 Ω
r'_r	0.0764 Ω
x_m	5.834 Ω
$x_{ls}=x'_{lr}$	0.2145 Ω
Number of poles	4

The nominal speed of the induction machine is 1750 rpm. As a case study, a change in the reference speed from 0 to its nominal value and then a reduction in the speed to 780 rpm is considered. The reference motor speed and the actual motor speed are represented in Figure 117. As seen, the motor speed can follow its reference and the error is very small.

For this case study the load torque is 15 Nm as illustrated in Figure 118. Figure 119 depicts the stator current and voltage while the speed of the machine is 1750 rpm. Current and voltage of the input-side of the converter when the induction machine is rotating at 1750 rpm are illustrated in Figure 120. The amplitude of the input current is 20 A. The input current and voltage are in phase. The stator current and voltage when the speed of the machine is 780 rpm are represented in Figure 121. In this case the frequency of the current/voltage is 28 Hz. Figure 122 and Figure 123 represent the link voltage and the link current, respectively.

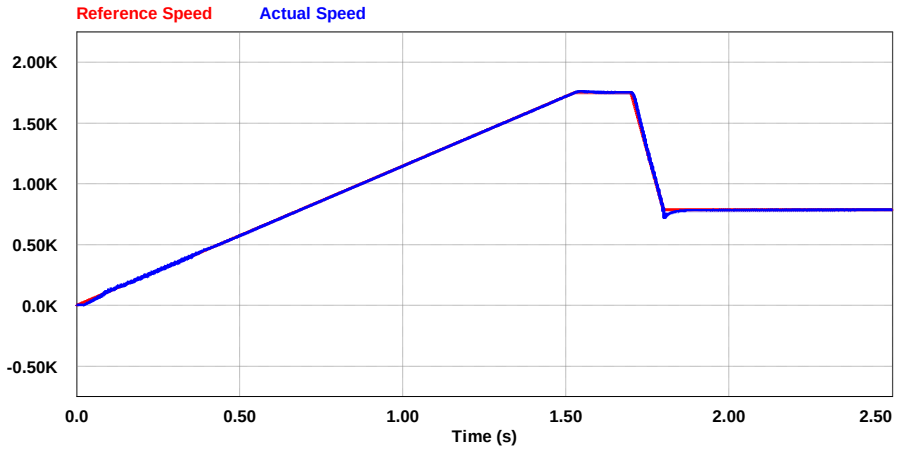


Figure 117 The reference speed and the actual speed of the motor (in rpm) derived by the ac-ac parallel ac-link universal converter

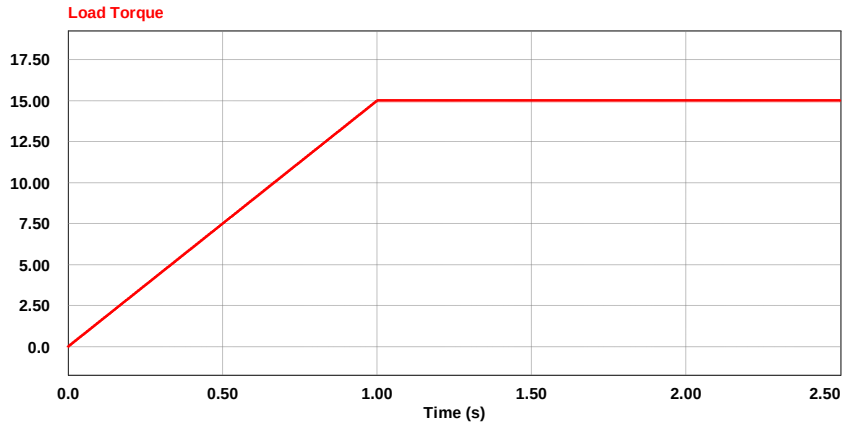


Figure 118 Load torque of the motor derived by the ac-ac parallel ac-link universal converter

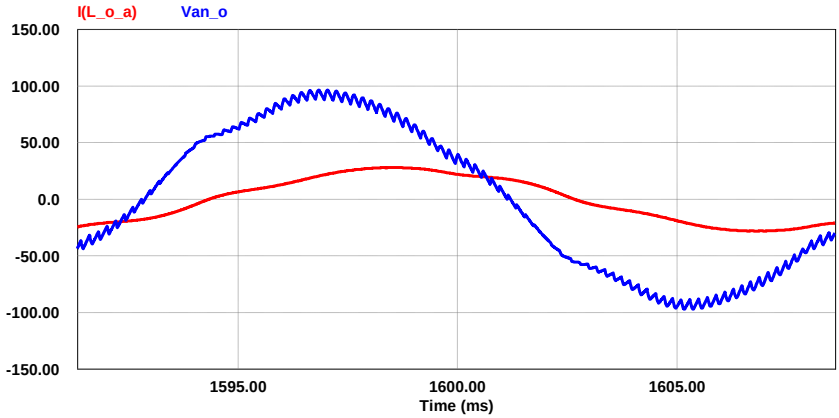


Figure 119 Stator current and voltage of the motor derived by the ac-ac parallel ac-link universal converter, operating at 1750 rpm

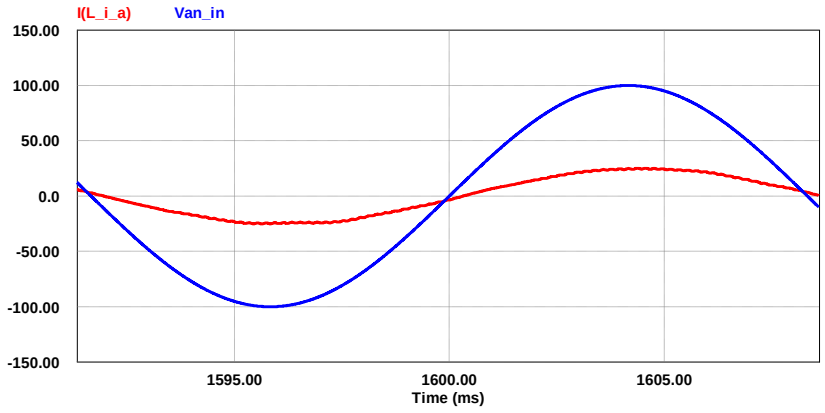


Figure 120 Input current and voltage in the ac-ac parallel ac-link universal converter

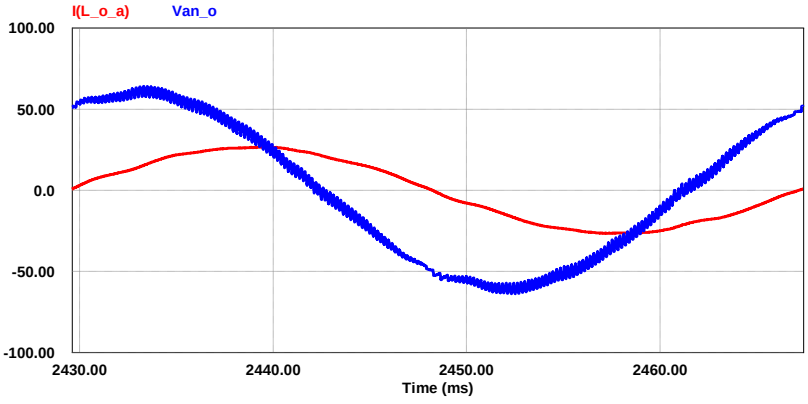


Figure 121 Stator current and voltage of the motor derived by the ac-ac parallel ac-link universal converter, operating at 780 rpm

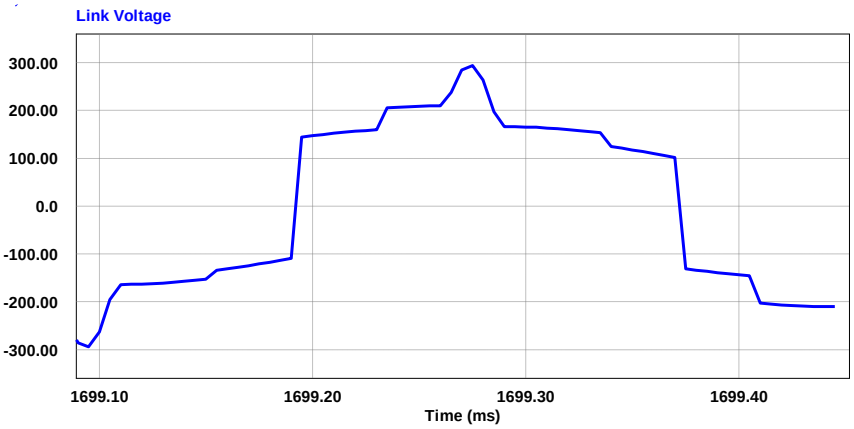


Figure 122 Link Voltage of the ac-ac parallel ac-link universal converter used as a VFD

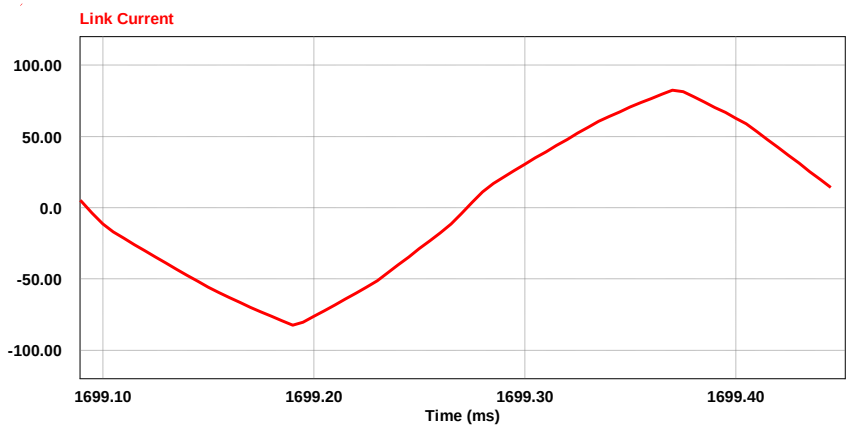


Figure 123 Link Current of the ac-ac parallel ac-link universal converter used as a VFD

2.10. Summary

In this section the parallel ac-link universal power converter was introduced. This converter is an extension of the buck-boost converter. By applying several modifications the link current becomes alternating, which eliminates the need for dc-electrolytic capacitors and the low-frequency transformers. This converter is a soft-switching converter in which all the switches turn on at zero voltage and they have a soft turn off.

In this section the principles of the operation of the parallel ac-link universal converter were studied, and the design procedures and a detailed analysis method were

introduced. Moreover, the hybrid parallel ac-link universal power converter was proposed to interface several sources/loads.

Finally, this converter was evaluated through several simulations and experiments, which verified its performance as the three-phase ac-ac, dc to three-phase ac, three phase ac-dc, hybrid inverter, and dc to single-phase ac parallel ac-link universal converters.

3. SERIES AC-LINK UNIVERSAL POWER CONVERTER*

3.1. Introduction

In this section the series ac-link universal power converter will be proposed. This converter is a dual of the parallel ac-link universal power converter. Therefore, an ac capacitor is the main energy storage component in this converter. An inductor is added in series with the link capacitor to facilitate the zero current turn-off and the soft turn-on of the switches. Similar to the parallel ac-link universal power converter, switching losses are negligible in this converter. Devices are subject to minimum current and voltage stress. Therefore, no snubber circuit is needed in the series ac-link universal power converter.

In this converter the link current and link voltage are both alternating. Their frequency can be very high. This results in the elimination of the dc capacitors and the low-frequency transformers.

This converter is named Series Partial Resonant Converter (SEPARC). Although it is a dual of the parallel ac-link universal power converter, it has a significant advantage over that converter. Since the switches are turned off at zero current in the SEAPRC, SCRs with natural commutation may be used instead of the metal-oxide semiconductor field-effect transistors (MOSFETs) or IGBTs. SCRs have several

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1. " A Highly Reliable Converter for Wind Power Generation Application " by M. Amirabadi and H. Toliyat, in Applied Power Electronics Conference and Exposition (APEC), 2013, pp. 1117-1123. Copyright 2013 by IEEE.
2. " A New Class of PV Inverters: Series Partial Resonant Converters " by M. Amirabadi and H. A. Toliyat, in Energy Conversion Congress and Exposition (ECCE), 2012 IEEE, 2012, pp. 3125-3132. Copyright 2012 by IEEE.

advantages over the other types of switches. They have low losses, are available at both high current and high voltage ratings, and are inexpensive and reliable. These characteristics make them an excellent candidate for high power applications and reliability demanding applications. The SEPARC can operate without the link inductor as well. However, in this case the converter will be a hard-switching converter and switches cannot have natural commutation.

3.2. Principles of Operation

Being universal, the series ac-link universal converter can appear as dc-dc, dc-ac, ac-dc, or ac-ac. Figure 124 represents the schematic of the three-phase ac-ac series ac-link universal power converter. This converter includes 12 unidirectional (or 6 bi-directional) switches on the input-side switch bridge (S1-S11) and 12 unidirectional (or 6 bi-directional) switches on the output-side switch bridge (S12-S23). The link is formed by a series LC pair placed in series with the input and output switch bridges. The main energy storage component is the capacitor, the current and voltage of which are alternating. Hence, a film capacitor can be used instead of the dc electrolytic capacitor, which is commonly used in ac-ac converters. The elimination of the electrolytic capacitors results in a more reliable converter. Link inductor, L, is a small inductor added to facilitate the zero current turn off of the switches. Since the switches are all turned off at zero current, naturally commutated thyristors may be employed in this converter, as shown in Figure 125. This converter needs current sources at the input and output terminals, which can be formed by placing an inductor in series with each voltage source. However, the link capacitor forms a voltage source at the link.

If galvanic isolation is required, a single phase high-frequency transformer can be added to the link, as shown in Figure 126 and Figure 127. In this case the leakage inductance of the transformer may play the role of the link inductance.

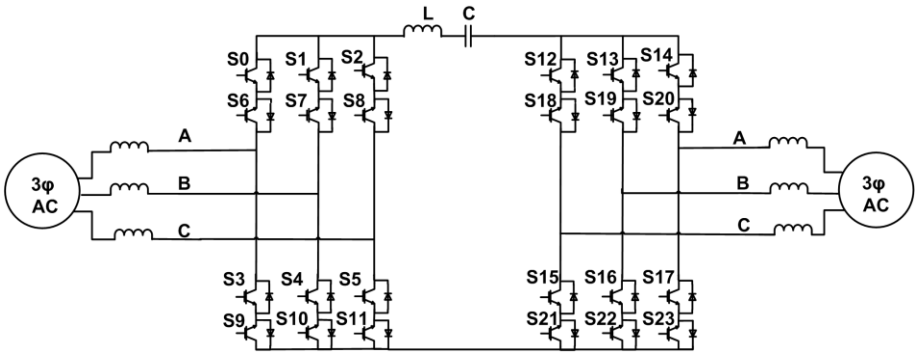


Figure 124 Three-phase ac-ac series ac-link universal power converter

The operation of this converter is similar to a Cuk converter in which the link capacitor is first charged through input phase-pairs and then discharged into the output phase-pairs. Bidirectional switches makes it possible for the capacitor to have both positive and negative voltage. In order to have lower THDs and desired input power factor, similar to the method proposed in [12] for the parallel ac-link universal converters, each charging and discharging mode can be divided into two modes. Between each charging and discharging, a resonating mode, in which the inductor and capacitor are shorted to resonate, occurs. One cycle of the link voltage is represented in Figure 128. As seen, the link cycle is divided into 16 modes with 8 power transfer modes and 8 resonating modes. The link capacitor is charged in the positive direction through the input phase currents during modes 1 and 3 and charged in the negative direction during modes 9 and 11. It is discharged in the positive direction into the output during modes 5 and 7 and discharged in the negative direction during modes 13 and 15.

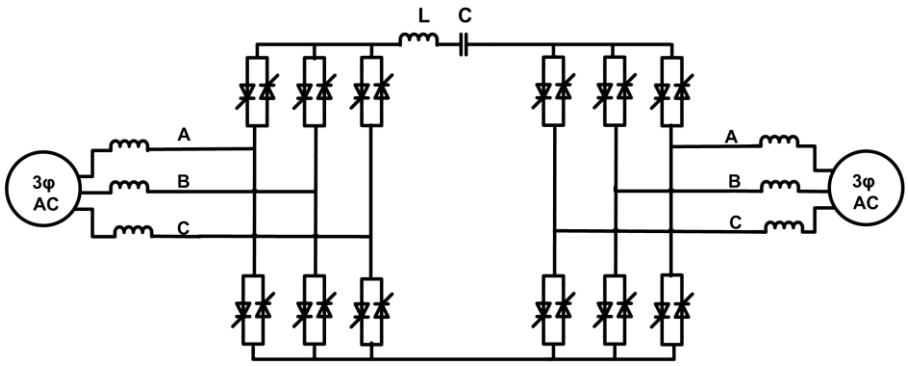


Figure 125 Three-phase ac-ac series ac-link universal power converter using SCRs

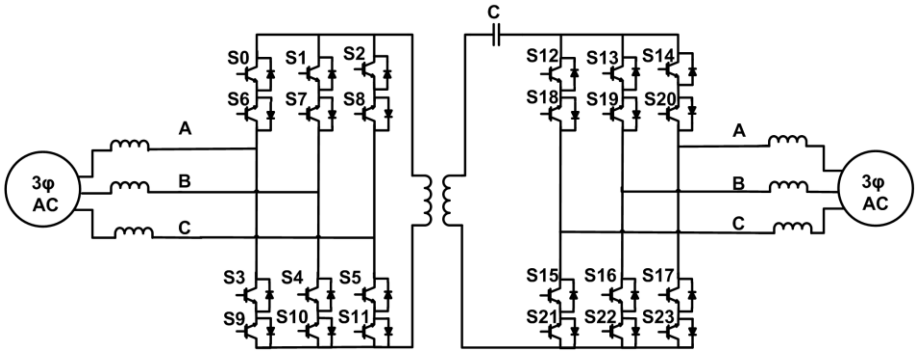


Figure 126 Three-phase ac-ac series ac-link universal power converter with galvanic isolation

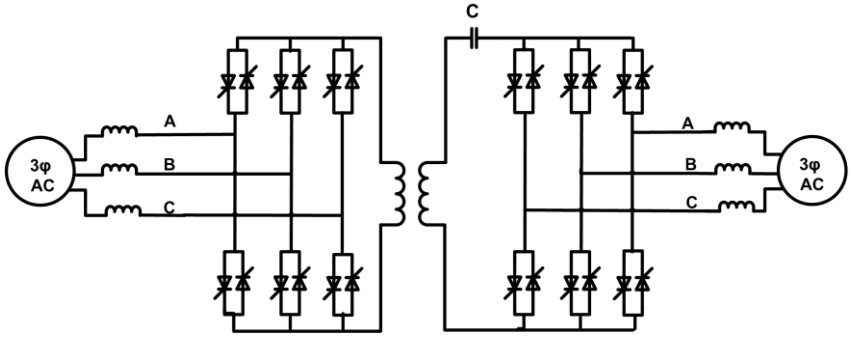


Figure 127 Three-phase ac-ac series ac-link universal power converter using SCRs with galvanic isolation

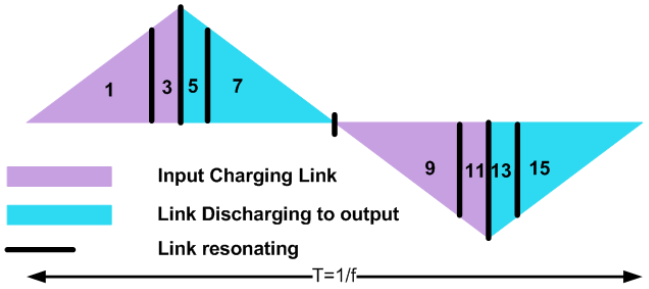


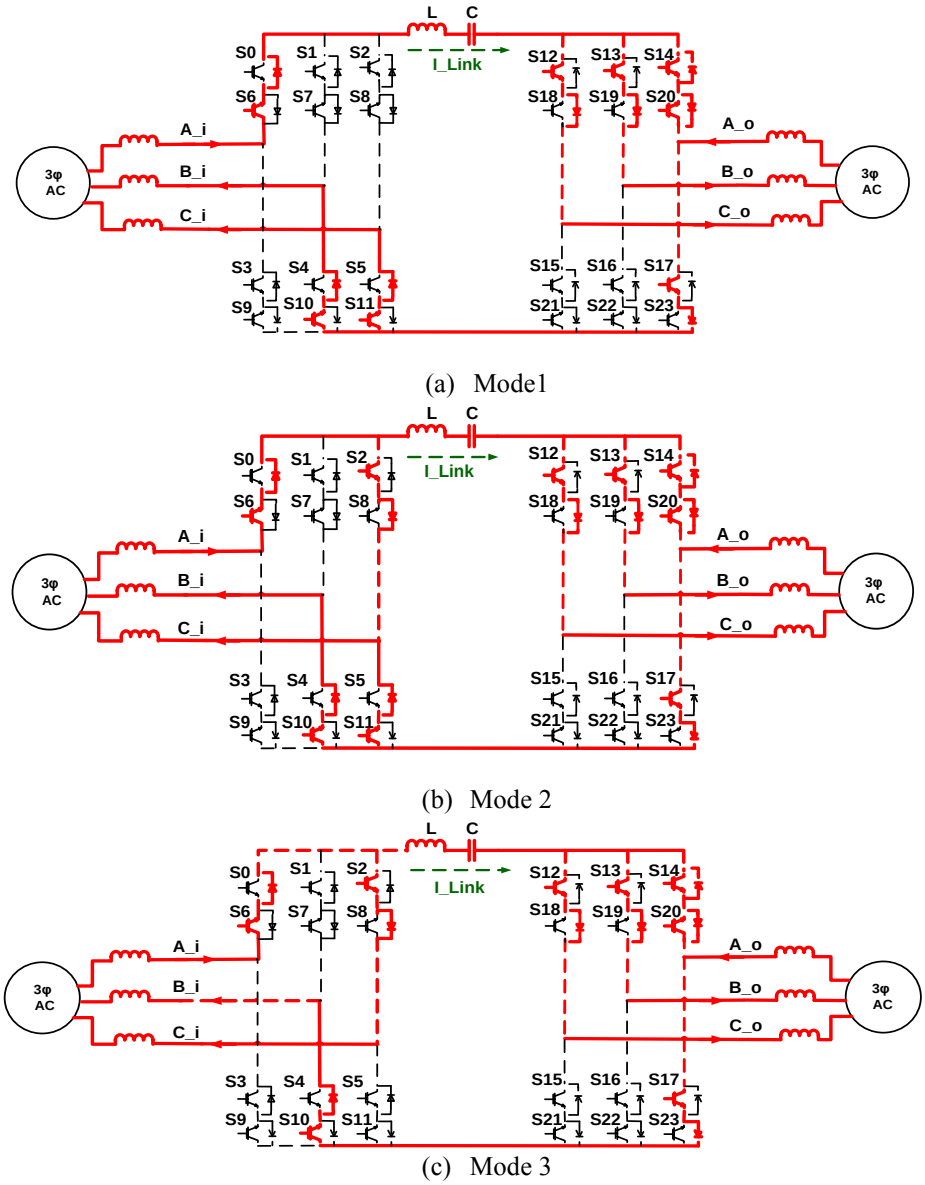
Figure 128 One cycle of the link voltage in the three-phase ac-ac series ac-link universal power converter

Figure 129 and Figure 130 illustrate the principles of operation in more detail. The behavior of the circuit during each mode of the operation is depicted in Figure 129. It is assumed that at this time the voltage across the input phase-pair AB is higher than the voltage across the input phase-pairs BC and CA ($|V_{AB\_i}|>|V_{BC\_i}|>|V_{CA\_i}|$). Similarly, the voltage across the output phase-pair AB is higher than the voltage across the output phase-pairs BC and CA ($|V_{AB\_o}|>|V_{BC\_o}|>|V_{CA\_o}|$). Moreover, it will be assumed that the current of phase A at the input side is higher than the current of phase B at that side and that current of phase A at the output side is higher than the current of phase B at the output side ($|I_{A\_i}|>|I_{B\_i}|$ and $|I_{A\_o}|>|I_{B\_o}|$). It is obvious that the phase carrying the highest instantaneous current and the phase-pair carrying the maximum instantaneous voltage continually shift during the operation and that the same input and output phases do not need to carry maximum current or the voltage at the same time. As shown in Figure 129 (a) during mode 1, the input phase A charges the link capacitor; therefore the link current is equal to I_{A_i}. Leg "A" at the output switch bridge provides a path for the link current flow. The output switch bridge must also provide a path for the output phase currents. It is assumed that the sum of the output phases currents is zero ($I_{A\_o}=I_{B\_o}+I_{C\_o}$). Once the voltage across the input phase-pair AC meets its reference, mode 2, which is a resonating mode, begins by turning on switch S2. During mode 2 the link is shorted and therefore its current decreases. Once the link current becomes equal to the current of phase B, Switch S11, which is carrying zero current at this time, is turned off. By turning off this switch, mode 3 is initiated during which time phase B charges the link capacitor. Once the voltage across the input phase-pair AB meets its reference, a resonating mode,

mode 4, which includes two stages, starts by turning on switch S11 and shorting the link. This results in decreasing the link current. After the link current and the current passing through switches S10, S11 and S17 reaches zero, these switches are turned off. Then, the second stage of mode 4 starts, by turning on S3 and S22. This operation allows the polarity of the link current to be reversed. The link current continues to decrease during the second stage of mode 4. Once its absolute value becomes equal to the absolute value of the current of phase B at the output side, mode 5 starts by turning off S13, which carries no current at this moment ($I_{A\_o}=I_{B\_o}+I_{C\_o}$).

During mode 5, the current of the link is equal to the current of phase B at the output side, which is negative. Therefore, the link voltage decreases and the link capacitor is discharged into the output. As soon as the voltage across the output phase-pair BC meets its reference, mode 6, another resonating mode, is initiated by turning on S21. During mode 6, the link current decreases until its absolute value becomes equal to the absolute value of phase A current at the output side. Since the link current is negative, while it is decreasing its absolute value is increasing. At this time S12, which is carrying zero current, is turned off. During mode 7, the remainder of the energy stored in the capacitor is discharged into the output; the link current is equal to the phase A current at the output side. Finally, when the energy remained in the link is sufficient for the link current to reach to a predetermined value, which is slightly higher than the peak of the input and output currents, mode 8 starts by shorting the link. During this mode the link resonates until its current becomes equal to that of the phase A at the input side. Modes 9-16 are similar to modes 1-8, except the polarity of the link voltage/current is

reversed. For this set of operations, the complimentary switch on each leg is switched when compared to the ones switched during modes 1 through 8. As discussed, all the switches are turned off at zero current and they have soft turn on, which results in negligible switching losses and higher efficiencies.

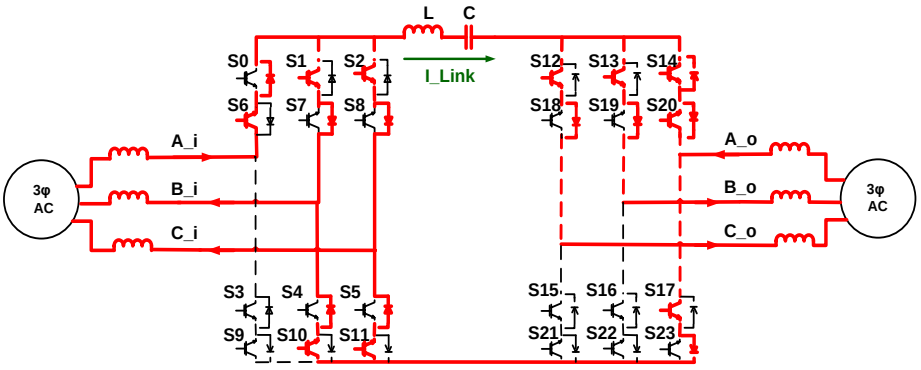


(a) Mode1

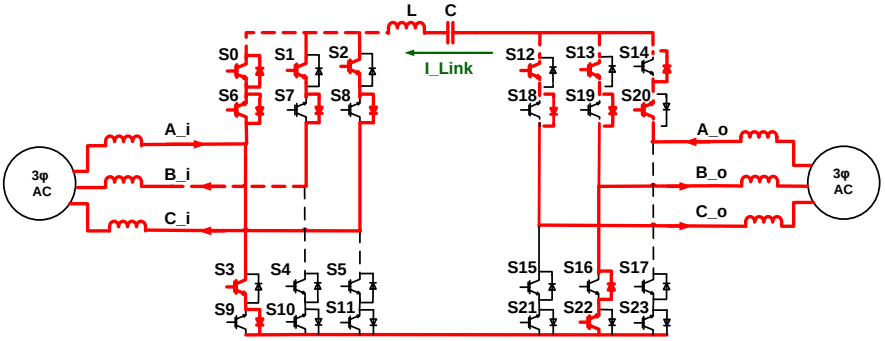
(b) Mode 2

(c) Mode 3

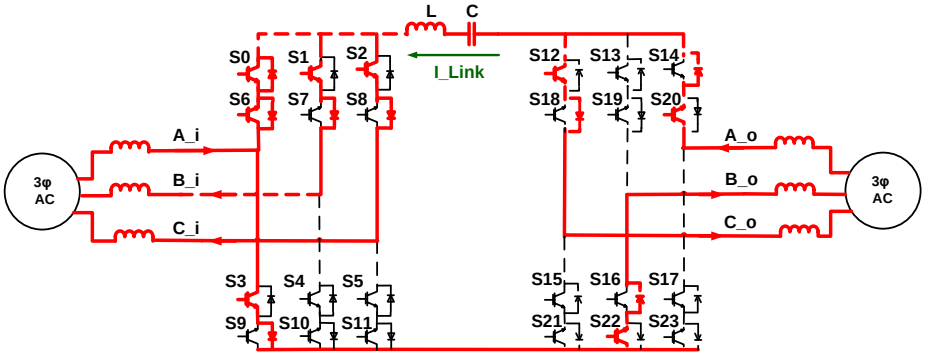
Figure 129 Behavior of the series ac-link universal power converter during different modes of operation



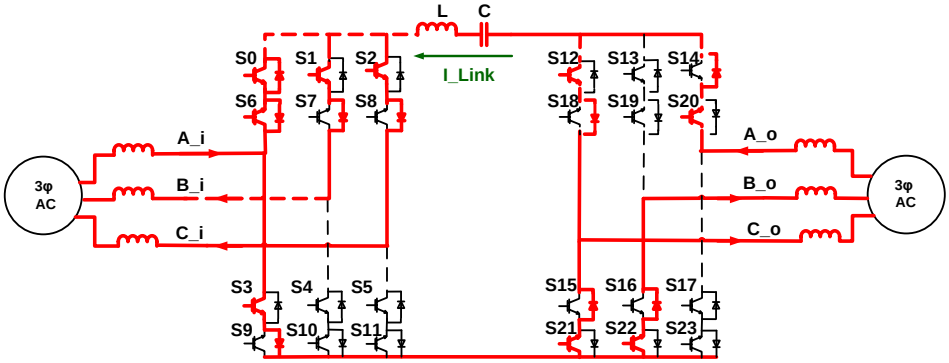
(d) Mode 4-first stage



(e) Mode 4-second stage

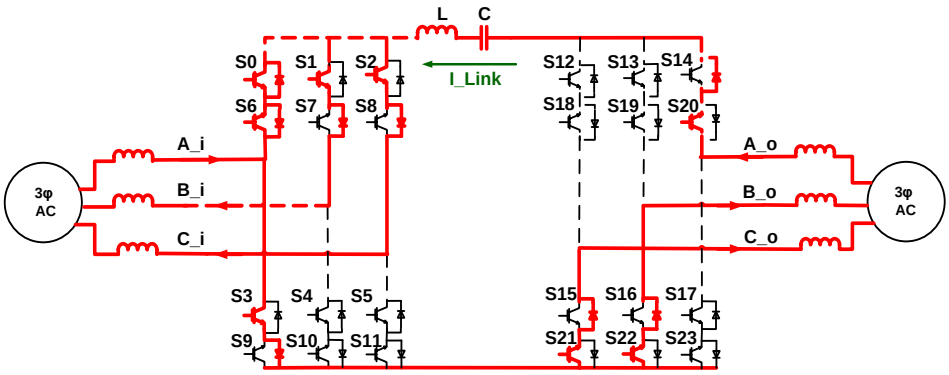


(f) Mode 5

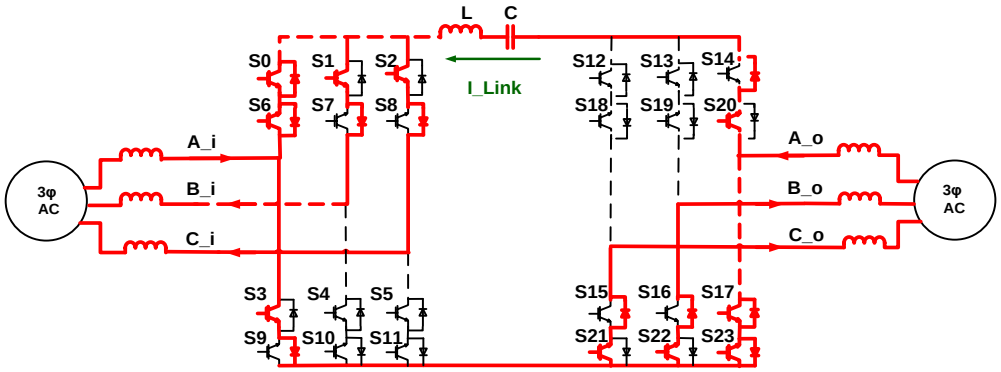


(g) Mode 6

Figure 129 Continued.



(h) Mode 7



(i) Mode8

Figure 129 Continued.

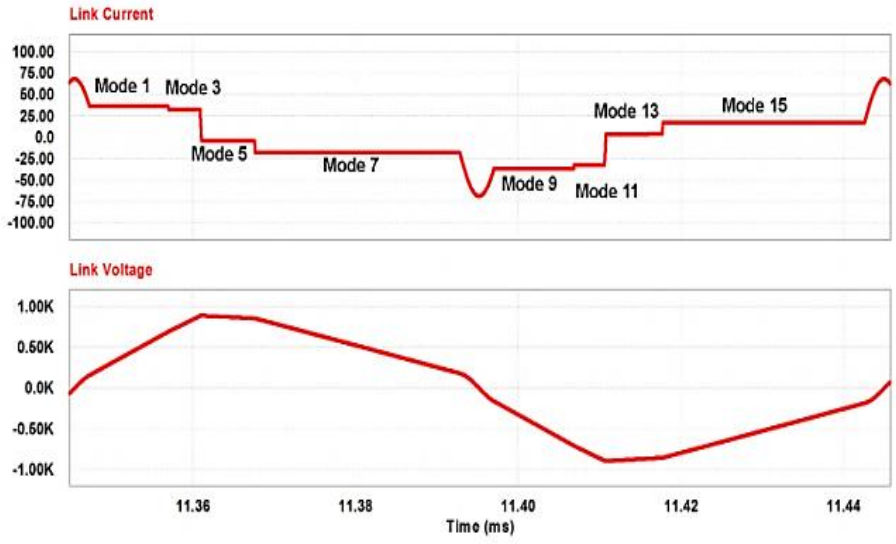


Figure 130 Link current and voltage in the series ac-link universal power converter

3.3. Design Procedure and Analysis

In this part the design procedure of the SEPARC will be presented. To simplify the design procedure, similar to the parallel ac-link universal power converter, the resonating time which is much shorter than the power transfer time, will be neglected. Moreover, charging and discharging are each assumed to take place in one equivalent mode instead of two modes during each power cycle. For this operation, the link is assumed to be charged through virtual source with input equivalent current and then discharged into a virtual load with output equivalent current.

Considering the principle of the operation, it can be shown that the input equivalent voltage, which is the voltage across the virtual source, is:

$$V_{i,eq} = \frac{3\sqrt{3}}{\pi} \times V_{i,peak} \tag{69}$$

Similarly, the output equivalent voltage is:

$$V_{o,eq} = \frac{3\sqrt{3}}{\pi} \times V_{o,peak} \tag{70}$$

In the above equations, $V_{i,peak}$ and $V_{o,peak}$ are the filtered input and output peak voltages, respectively. The input and output equivalent currents can then be calculated as:

$$I_{i,eq} = \frac{\pi}{2\sqrt{3}} \times I_{i,peak} \times \cos\theta_i \tag{71}$$

$$I_{o,eq} = \frac{\pi}{2\sqrt{3}} \times I_{o,peak} \times \cos\theta_o \tag{72}$$

where $I_{i,peak}$, $I_{o,peak}$, $cos(\theta_i)$ and $cos(\theta_o)$ are the input peak current, the output peak current, the input power factor and the output power factor, respectively.

As shown in Figure 129, during the equivalent charging mode (modes 1 and 3), the input equivalent current charges the link capacitor and the voltage across this capacitor increases linearly. During the equivalent de-energizing mode (modes 5 and 7), the charged link capacitor is discharged into the virtual load. Figure 131 shows one cycle of the link voltage (simplified for the design procedure). The following equations describe the behavior of the circuit during the charging and discharging modes, respectively:

$$V_{Link,Peak} = \frac{I_{i,eq} \times t_{charge}}{C} \tag{73}$$

$$V_{Link,Peak} = \frac{I_{o,eq} \times t_{discharge}}{C} \tag{74}$$

In the above equations, $V_{Link,peak}$, t_{charge} and $t_{discharge}$ represent the peak of the link capacitor voltage, total energizing time during modes 1 and 3, and total de-energizing time during modes 5 and 7, respectively.

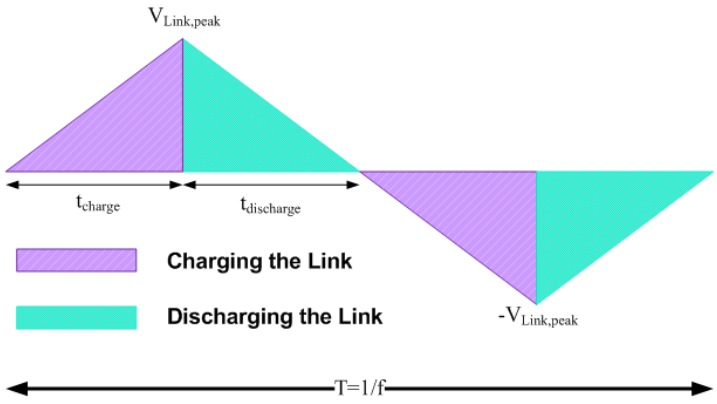


Figure 131 One cycle of the link voltage in the series ac-link universal converter simplified for the design procedure

Equations (73) and (74) determine the relationship between the charge time and discharge time as follows:

$$t_{charge} = \frac{I_{o,eq} \times t_{discharge}}{I_{i,eq}} \tag{75}$$

Using the above equations, the link peak voltage can be calculated based on the input and output peak voltages:

$$V_{link,peak} = \frac{6\sqrt{3}}{\pi} \times \left(V_{i,peak} + V_{o,peak}\right) \tag{76}$$

For the grid-tied converters the peak of the output voltage is fixed and the peak of the link voltage varies by changing the input voltage. Figure 132 depicts the link peak voltage vs. the input voltage variation for a 1.5 kW system with 208 V output voltage.

The frequency of the link at full power (f) can be chosen based on the power rating of the system and the characteristics of the available switches. Once the link frequency is chosen the following equation determines the link capacitance:

$$C = \frac{P}{\left(V_{link,peak}\right)^2 f} \tag{77}$$

where P is the rated power. This equation shows that by choosing a higher link frequency, a smaller link capacitor can be used. Figure 133 shows the link capacitance vs. the link frequency for a 1.5 kW system with 208 V and 134 V output and input voltages.

Link inductance should be chosen so as to minimize the resonating periods at full power. Similar to the parallel ac-link universal power converters, the resonating modes in the series ac-link universal power converters should be kept as short as possible.

Eq. (77) can be rewritten as:

$$f = \frac{\pi^2 P}{72 \times \left(V_{i,peak} + V_{o,peak}\right)^2 C} \tag{78}$$

This equation calculates the link frequency at different power levels. Figure 134 shows the frequency variation vs. the power level. As seen in this figure, the frequency of the link decreases by decreasing the power level.

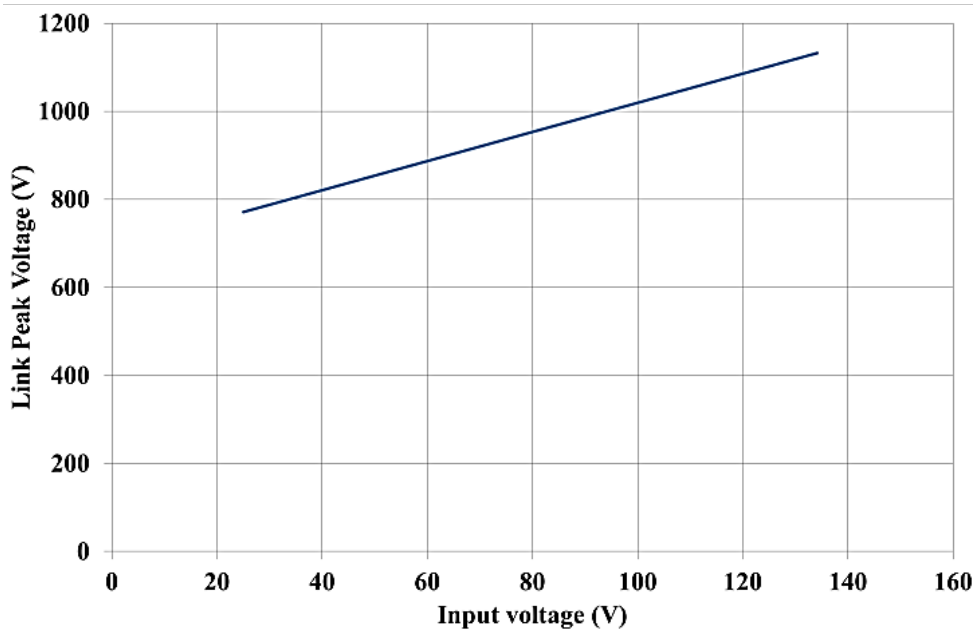


Figure 132 Link peak voltage vs. the input voltage in the series ac-link universal converter

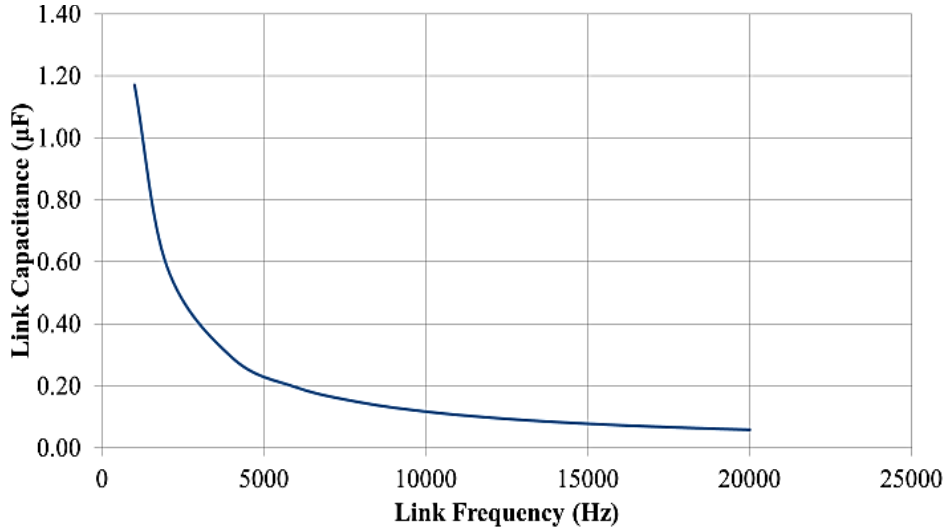


Figure 133 Link capacitance vs. the link frequency in the series ac-link universal converter

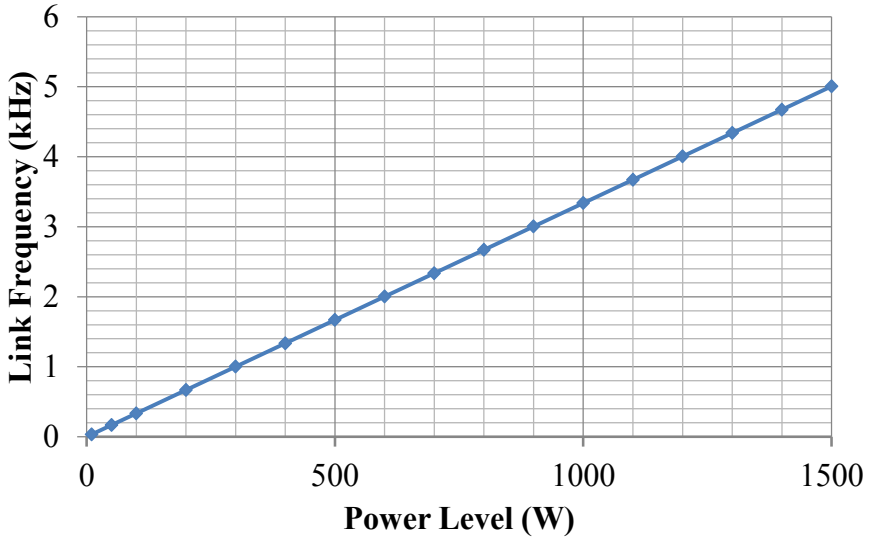


Figure 134 Link frequency vs. the power level in the series ac-link universal converter

Unlike the parallel ac-link universal power converter, in the series ac-link converter the power transfer modes become longer at lower power levels. Therefore, in this converter, the resonating modes can be neglected at lower power levels. Consequently, there is no need for more accurate analysis of the converter.

The series ac-link universal power converters may also appear as shown in Figure 135. However, in this case the switching scheme is slightly different.

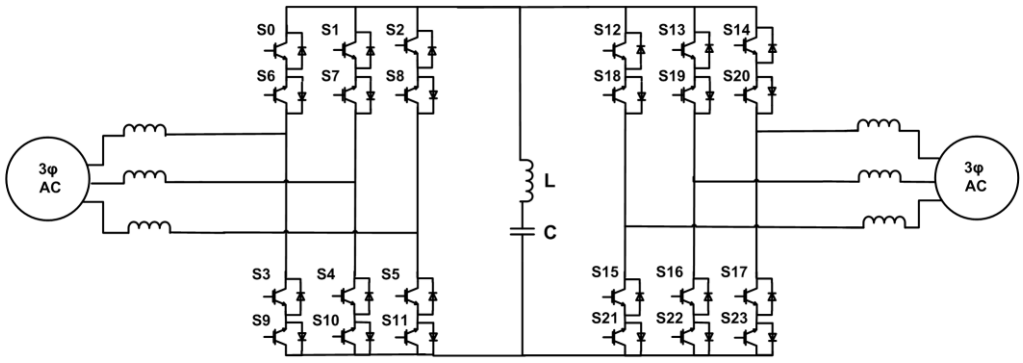


Figure 135 Another form of series ac-link universal power converter

3.4. Simulation and Experimental Results

In this part the performance of the dc-dc, dc-ac and ac-ac series ac-link universal power converters will be evaluated.

3.4.1. DC-DC Configuration

This part evaluates the performance of the dc-dc series ac-link universal converter through simulations and experiments. This converter is depicted in Figure 136. The parameters of the designed and simulated system are listed in Table 11.

Figure 137 depicts the dc voltage and current. The input current source is formed by placing an inductor in series with the dc voltage source. The output current and voltage are represented in Figure 138. The link current and scaled voltage are illustrated in Figure 139. As seen in this figure, the peak of the link voltage is 442 V, and the link frequency is 22 kHz. The maximum current to which the link resonates is 20 A.

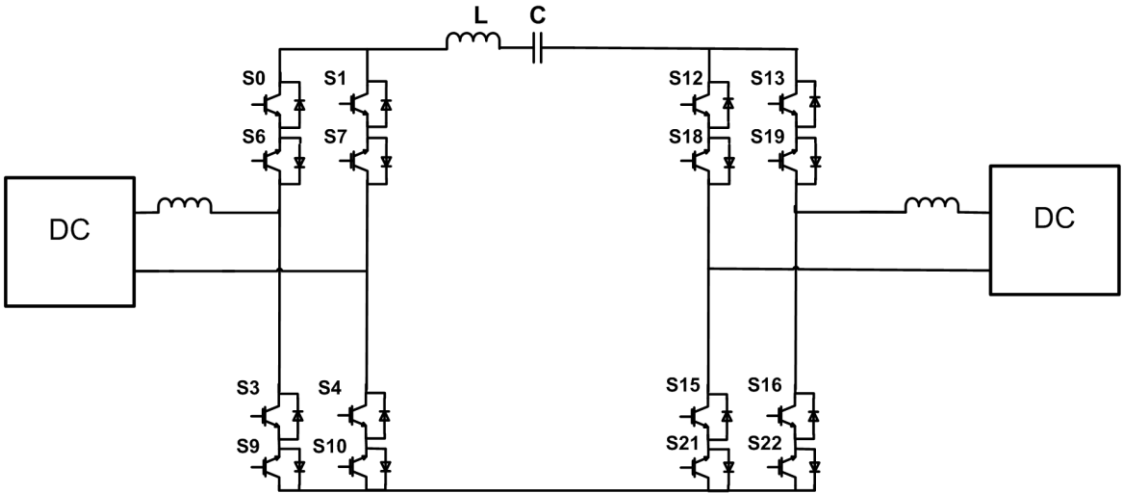


Figure 136 Dc-dc series ac-link universal converter

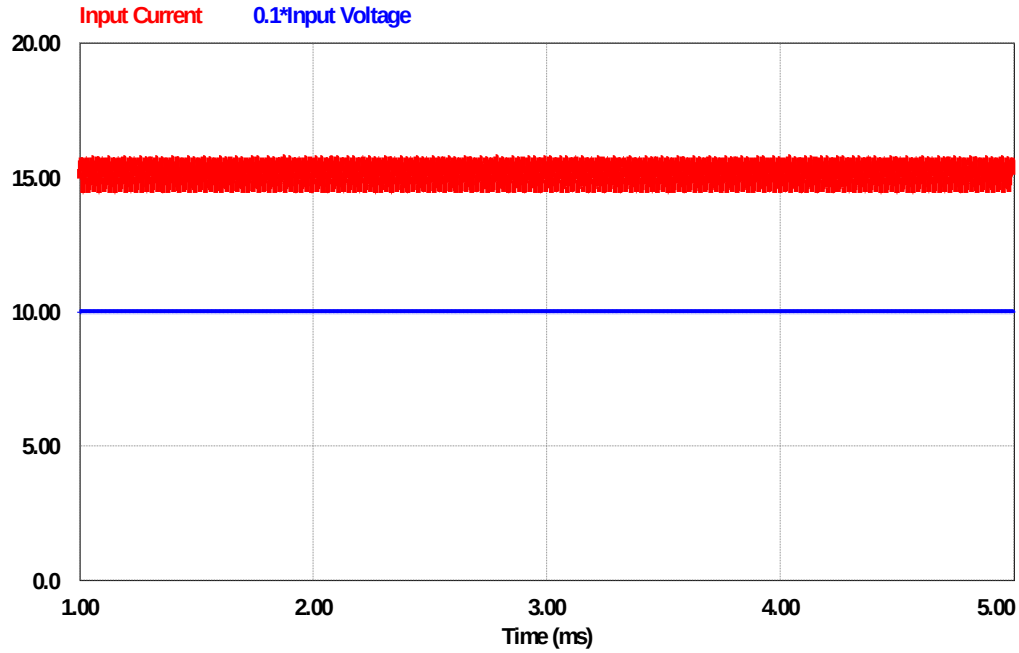


Figure 137 Input current and scaled voltage in the dc-dc series ac-link universal converter

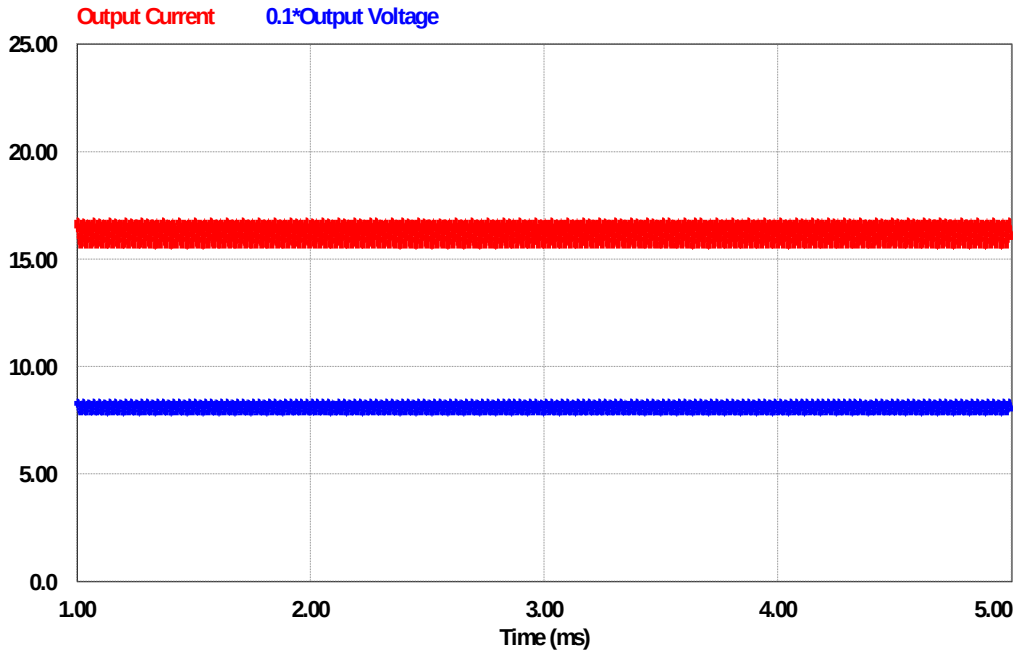


Figure 138 Output current and scaled voltage in the dc-dc series ac-link universal converter

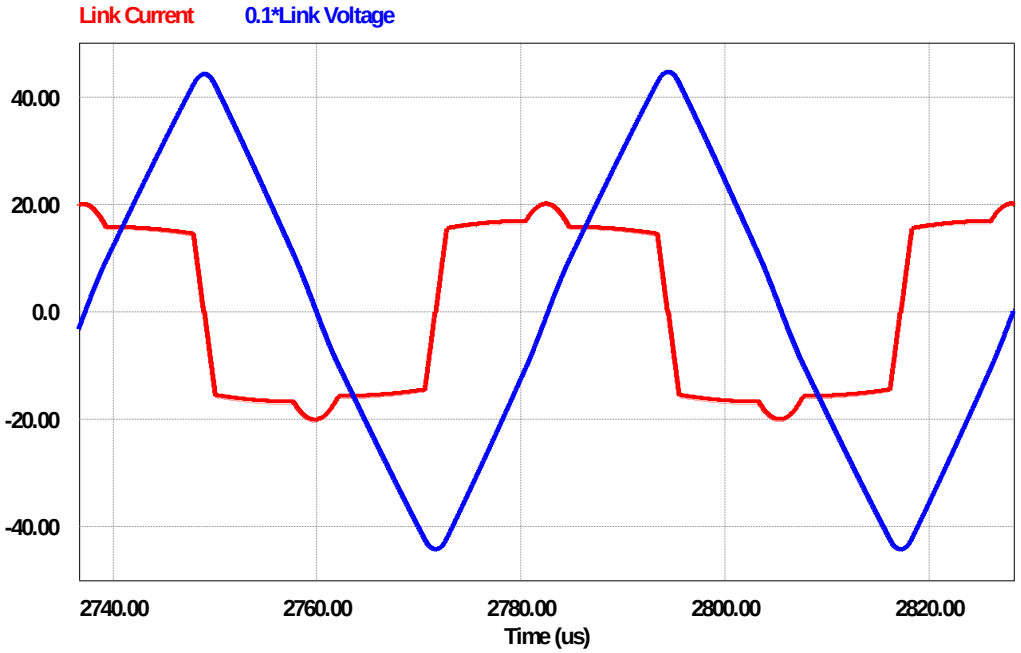


Figure 139 Link current and scaled voltage in the dc-dc series ac-link universal converter

TABLE 11 PARAMETERS OF THE DESIGNED AND SIMULATED DC-DC SERIES AC-LINK UNIVERSAL CONVERTER

Parameter	**Value**
Power rating	1.5 kW
Input voltage	100 V
Output voltage	86 V
Link inductance (L)	30 µH
Link capacitance (C)	0.4 µF
Inductance of the input side inductor	1 mH
Inductance of the output side inductor	1 mH

The dc-dc series ac-link universal power converter has been experimentally evaluated as well. Again, the multi-purpose prototype was used to test this configuration. Table 12 shows the parameters of this converter.

TABLE 12 PARAMETERS OF THE TESTED DC-DC SERIES AC-LINK UNIVERSAL CONVERTER

Parameter	Value
Power rating	100 W
Input voltage	45 V
Ro	22 Ω
Link inductance (L)	24 µH
Link capacitance (C)	0.4 µF

The input current and unfiltered voltage are shown in Figure 140. The input current is about 2 A. The output current and unfiltered voltage are illustrated in Figure 141. The output is connected to a resistive load. Since the converter is tested at a very low power level, its efficiency is low. The efficiency of the converter will be higher at higher power levels. The link current and voltage are shown in Figure 142. The link frequency and the link peak voltage are 8 kHz and 150 V, respectively.

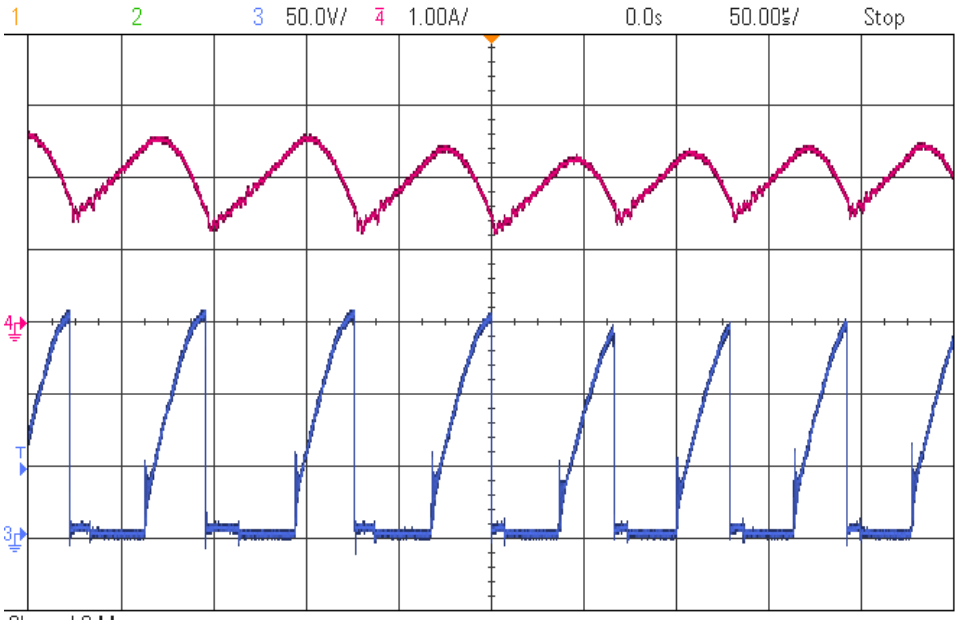


Figure 140 Input current (top) and unfiltered voltage (bottom) of the tested dc-dc series ac-link universal power converter (Experiment)

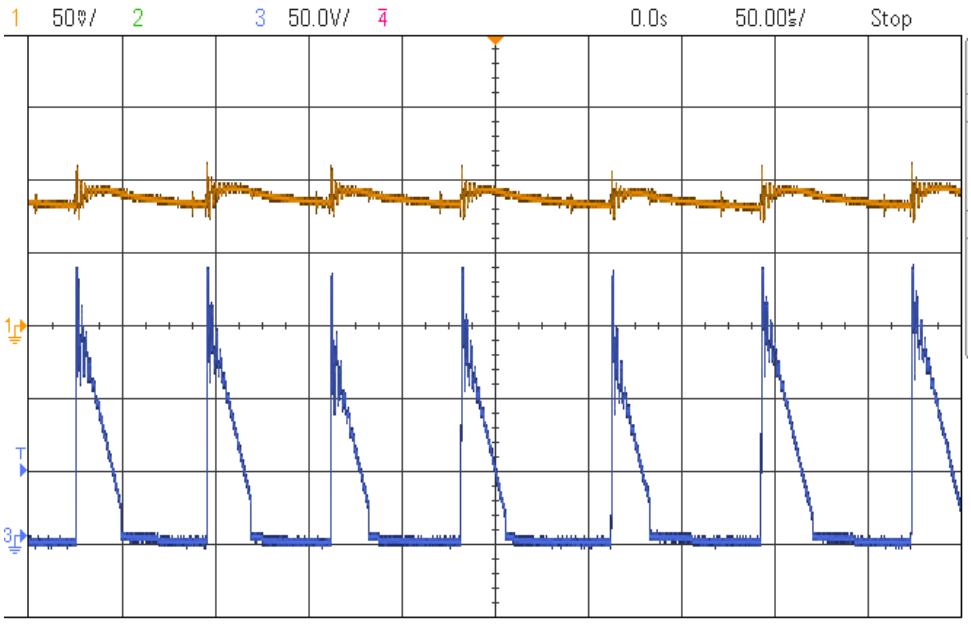


Figure 141 Output current (top) and unfiltered voltage (bottom) of the tested dc-dc series ac-link universal power converter (Experiment)

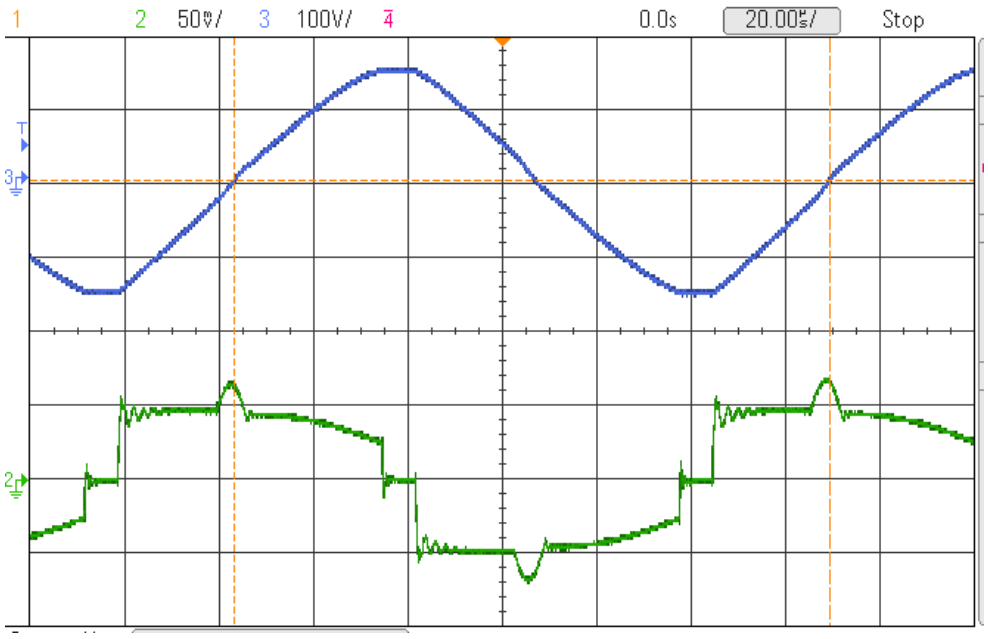


Figure 142 Link voltage (top) and current (bottom) of the tested dc-dc series ac-link universal power converter (Experiment)

3.4.2. DC to Three-Phase AC Configuration

This part evaluates the performance of the dc-ac series ac-link universal converter, which is shown in Figure 137. A good application for this inverter may be PV power generation. Table 13 summarizes the parameters of the designed and simulated system.

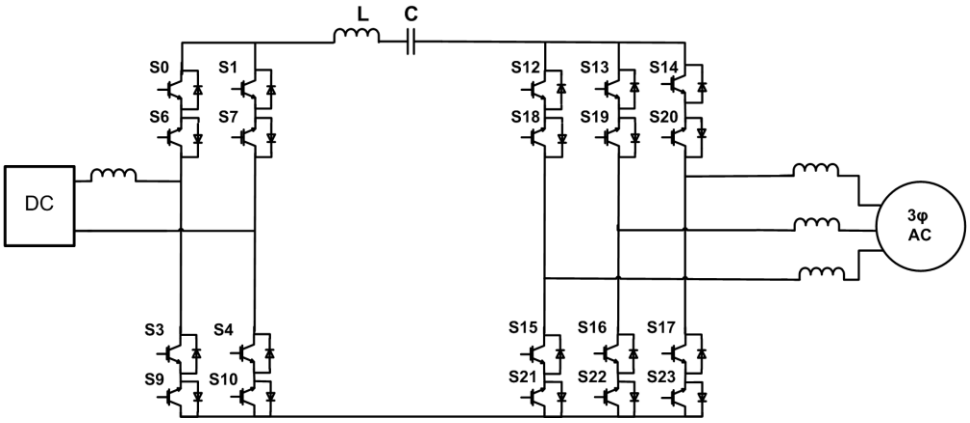


Figure 143 Dc-ac series ac-link universal converter

TABLE 13 PARAMETERS OF THE DESIGNED AND SIMULATED DC-AC SERIES AC-LINK UNIVERSAL CONVERTER

Parameter	**Value**
Power rating	1.5 kW
Input current	7.5 A
Output voltage	208 V
Link frequency (f)	5 kHz
Link inductance (L)	20 μH
Link capacitance (C)	0.344 μF

Simulations are performed in PSim. Figure 144 shows the output current, which is very smooth with THD less than 5%. In these simulations a dc current source (7.5 A) is used at the dc side. Figure 145 and Figure 146 illustrate the link voltage and current, respectively. The link current and voltage are both alternating and their frequency is 5

kHz. The peak of the link voltage is 933 V. It can be shown that in the dc-to-three phase ac series ac-link universal converter the link peak voltage is calculated by:

$$V_{link,peak} = (2 \times V_{dc}) + \left(\frac{6\sqrt{3}}{\pi} \times V_{o,peak}\right) \quad (79)$$

Where V_{dc} is the dc-side voltage. Since the link peak voltage is a function of the input voltage and the output peak voltage, high-current and low-voltage sources and loads are more appropriate for this converter, as it results in lower link peak voltage. Figure 147 represents the unfiltered line-to-line voltages.

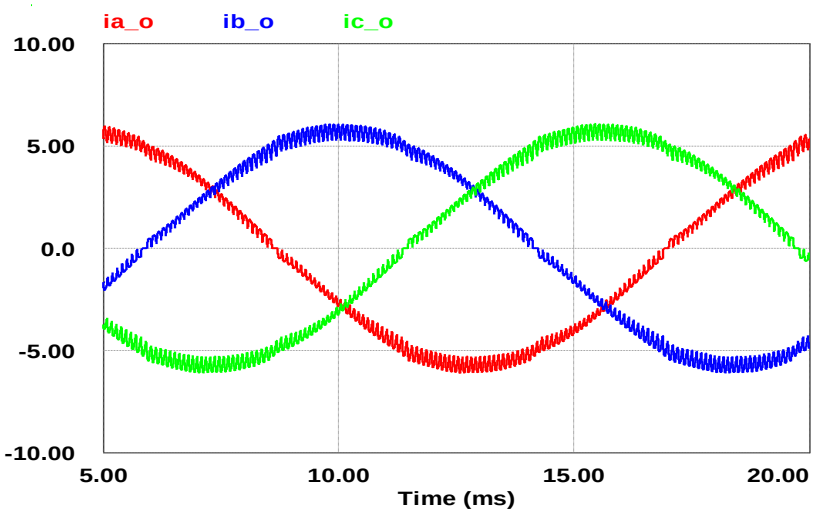


Figure 144 Output currents of the simulated 1.5 kW dc-ac series ac-link universal converter

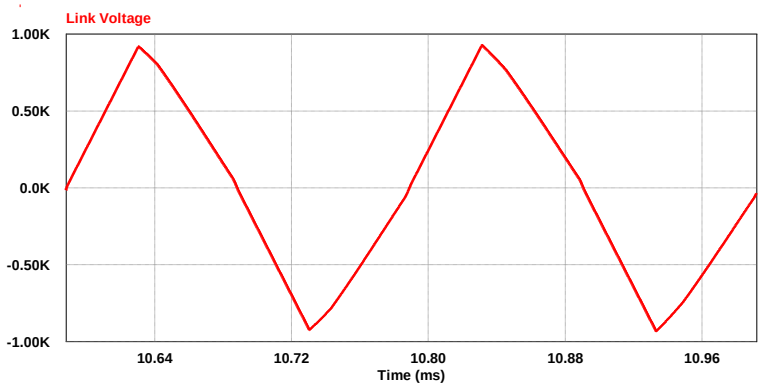


Figure 145 Link voltage of the simulated 1.5 kW dc-ac series ac-link universal converter

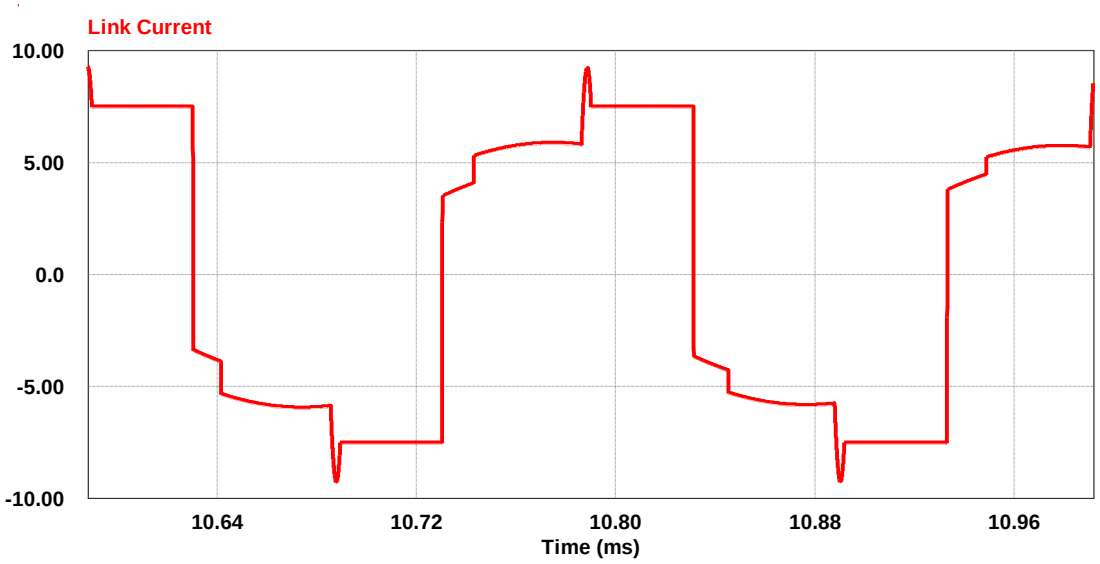


Figure 146 Link current of the simulated 1.5 kW dc-ac series ac-link universal converter

Figure 148 depicts the current and the gate command of switch S10. As shown in this figure, the switch is turned off after its current reaches zero, which results in zero current turn-off of switch S10. Other switches are turned off at zero current as well.

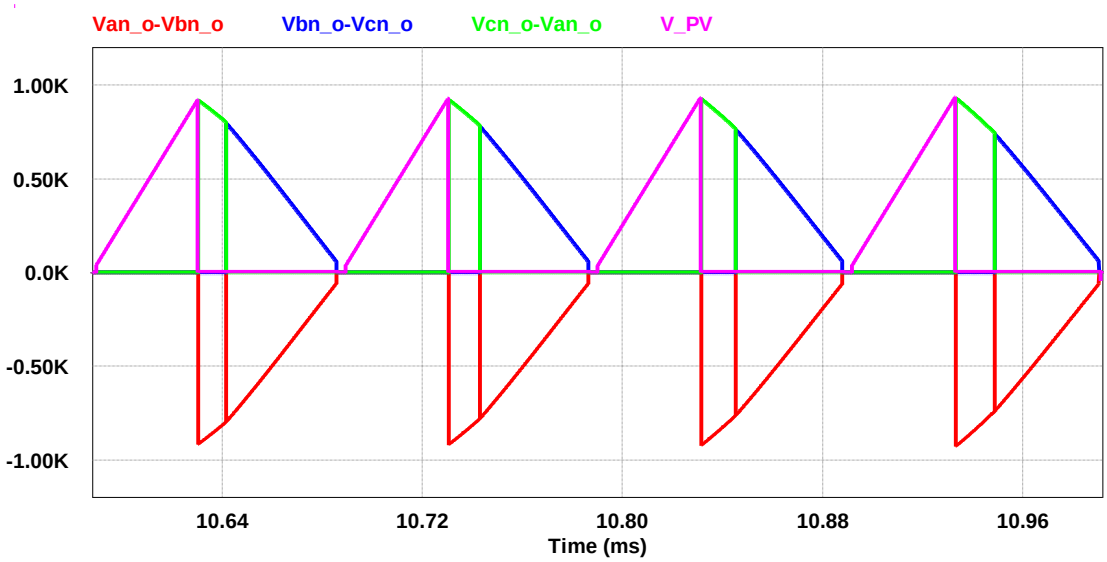


Figure 147 Unfiltered line-to-line voltages of the simulated 1.5 kW dc-ac series ac-link universal converter

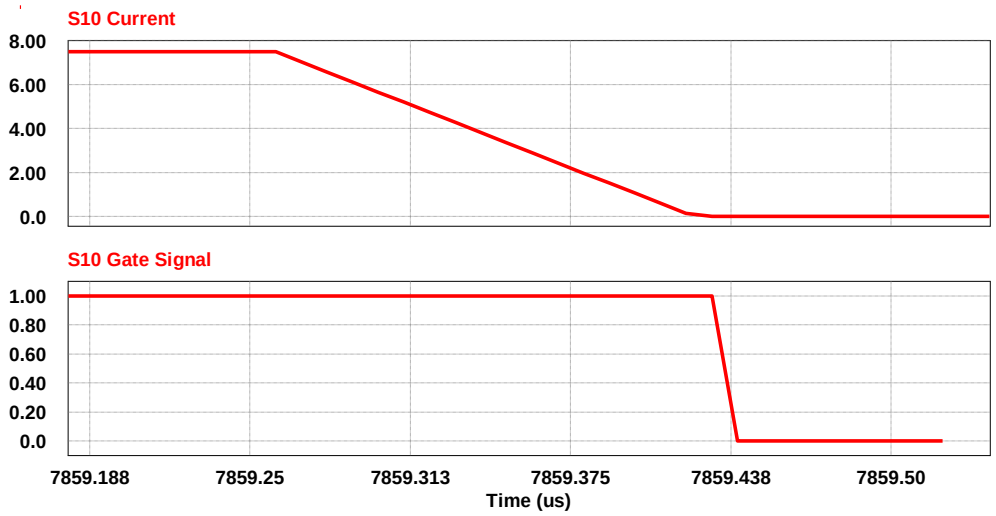


Figure 148 Current and gate command of switch S10 in the simulated 1.5 kW dc-ac series ac-link universal converter

3.4.3. AC-AC Configuration

A 5 kW three-phase ac-ac SEPARC was designed and simulated in PSim. Table 14 summarizes the parameters of this converter. The load is assumed to be RL with 0.85 power factor. Because it is a Cuk converter, this converter can both step up and step down the current. In this simulation, the voltage is stepped up and the current is stepped down. Figure 149 represents the input and output currents. In this case, both the input and the output frequencies are 60 Hz. Figure 150 and Figure 151 represent the link voltage and link current, respectively. The frequency of the link is 15 kHz. The link frequency may be increased by choosing a smaller capacitor. The link peak voltage is 850 V in this case.

In order to show that the converter is capable of changing the frequency, the simulation was repeated with the input frequency set to 30 Hz, whereas the output

frequency is 60 Hz. Figure 152 shows the input and output currents for this case. The capability to change the frequency is essential in the ac-ac converters used for wind power generation.

The gate command and the current passing though switch S0 are shown in Figure 153. As seen in this figure, the switch is turned off after its currents reaches zero.

TABLE 14 PARAMETERS OF THE DESIGNED AND SIMULATED AC-AC SEPARC

Parameters	**Value**
Power rating	5 kW
Input voltage	72
Output voltage	245
Load	R=9.45 Ω L=15.5 mH
Link capacitance	0.66 µF
Link inductance	100 µH

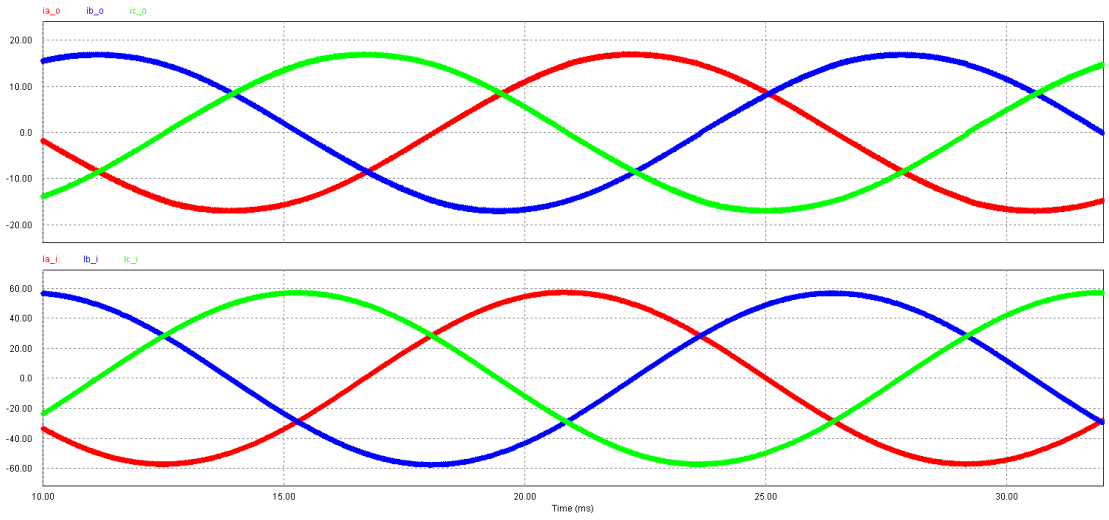


Figure 149 Output currents (top) and input currents (bottom) of the ac-ac SEPARC operating at full power

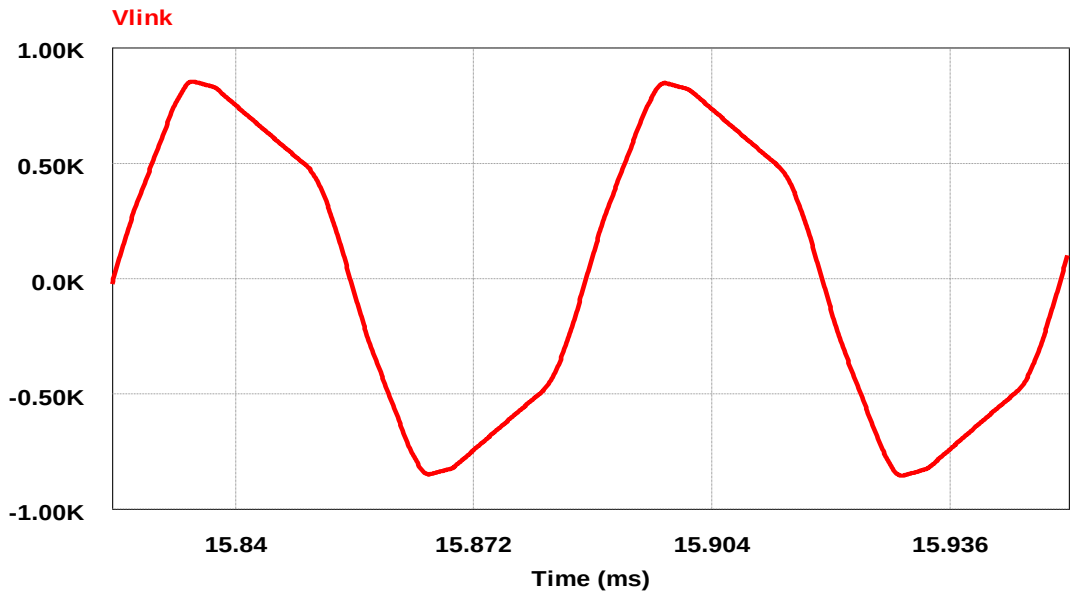


Figure 150 Link voltage of the ac-ac SEPARC operating at full power

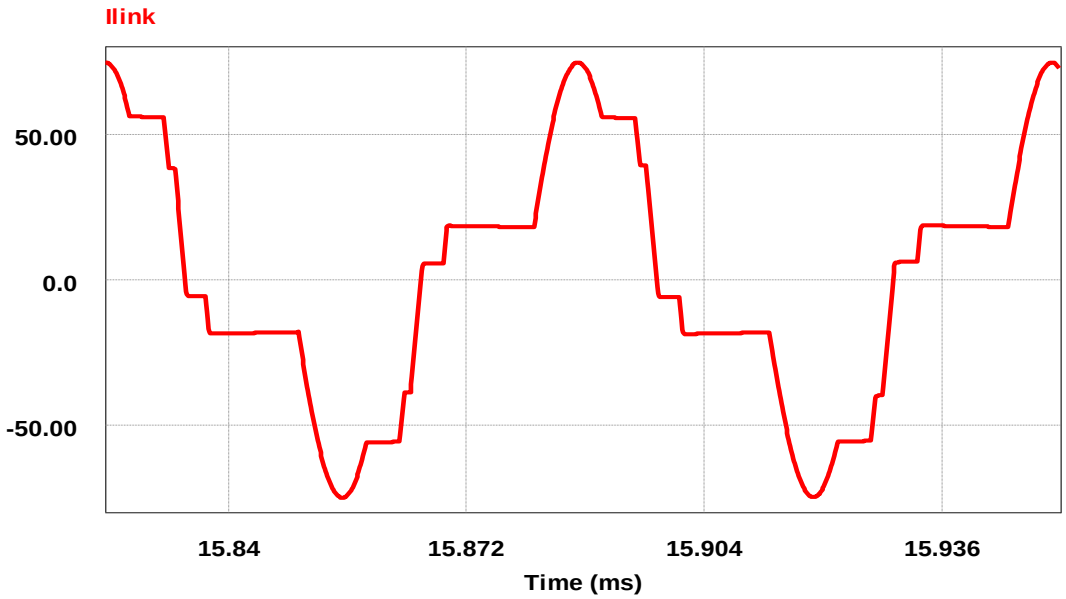


Figure 151 Link current of the ac-ac SEPARC operating at full power

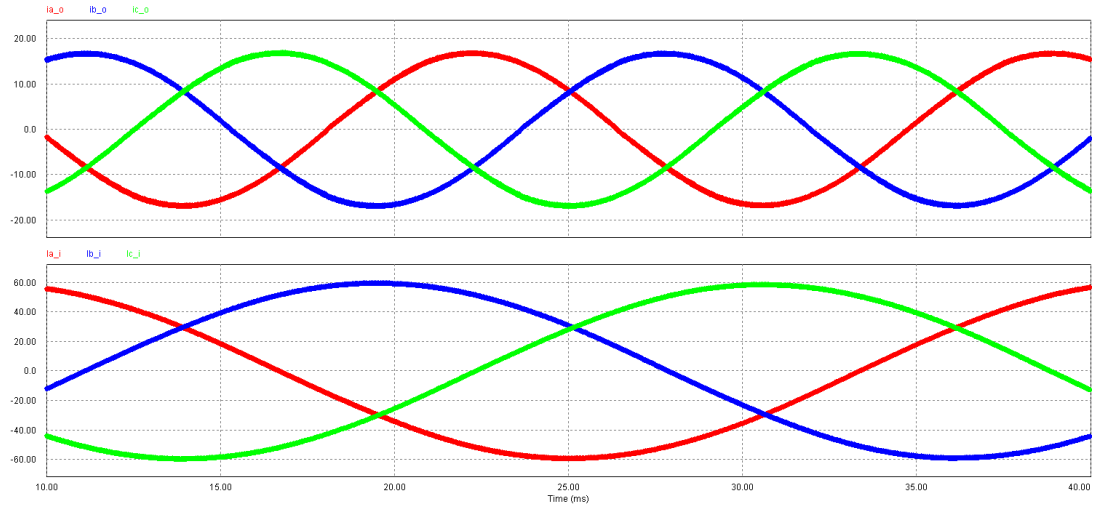


Figure 152 Output currents (top) input currents (bottom) of the ac-ac SEPARC operating at full power when the input frequency is 30 Hz

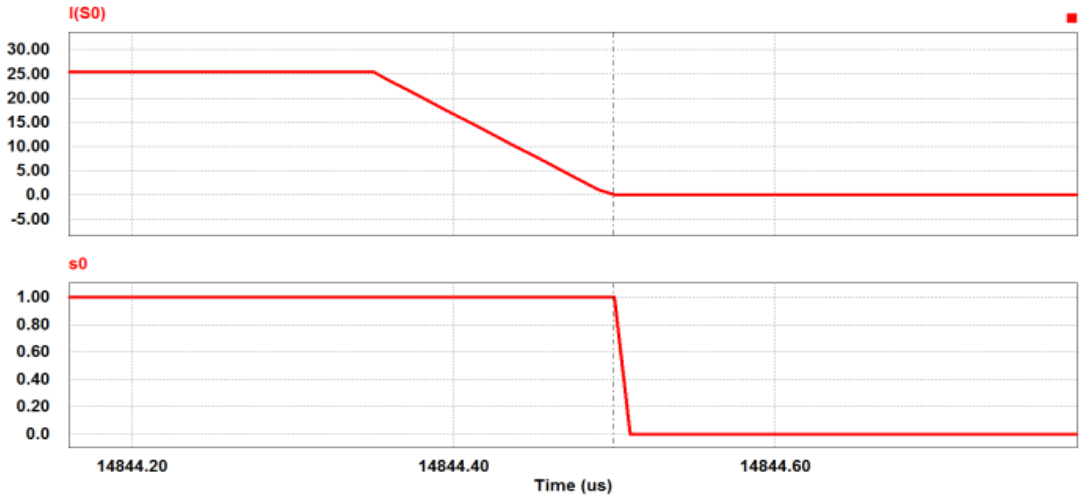


Figure 153 Current (top) and the gate command (bottom) of switch S0 in the ac-ac SEPARC

3.5. Summary

In this section the series ac-link universal power converter, which is an extension of the Cuk converter, was proposed. Being universal, the input and output of this converter can be dc, ac, single phase or multi-phase. In this converter the link is formed by a series LC pair having alternating current and voltage. The frequency of the link

current and voltage can be high. This configuration eliminates the need for the dc electrolytic capacitor and the low-frequency transformers.

In this converter, all the switches are turned off at zero current and their turn-on is soft. Therefore, in case of using SCRs, switches can have natural commutation Moreover, the current and voltage stress over devices are minimized.

In this section the principles of the operation in the series ac-link universal converters along with its design and analysis were presented. Finally, the performance of the converter was evaluated through simulation and experiment.

4. SPARSE AND ULTRA-SPARSE AC-LINK UNIVERSAL POWER CONVERTERS*

4.1. Introduction

Owing to their remarkable merits, the ac-link universal power converters have received noticeable attention during the last few years. These converters are compact, reliable and efficient. In addition, they offer longer life time compared to the other types of converters. However, they require more switches, which make the control process more complicated. In this section, a modified configuration that has all the advantages of the parallel and series ac-link universal power converters but requires fewer switches is proposed. Despite reducing the number of switches, the principles of operation of the proposed converter, which is named the sparse ac-link universal power converter, is the same as the original converter. The sparse ac-link universal power converters, which can appear as parallel or series, offer higher reliability compared to the parallel and series ac-link universal power converters. Another important feature of the sparse configuration is that due to using unidirectional switches, it can be fabricated by switch modules. These modules are more compact and more cost-effective, compared to the discrete devices. Hence, the sparse ac-link universal power converter is expected to be less expensive, less complicated, and more compact compared to the parallel and series ac-link universal

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* Part of this section is reprinted with permission from:
1. "Bi-Directional Sparse Parallel Partial Resonant ac-Link Inverter " by M. Amirabadi, J. Baek, and H. Toliyat, in Applied Power Electronics Conference and Exposition (APEC), 2013, pp. 136-143. Copyright 2013 by IEEE.
2. and from " Bi-Directional Partial Resonant Converters with Reduced Number of Switches " by M. Amirabadi, H. Hussain and H. A. Toliyat, in Energy Conversion Congress and Exposition (ECCE), 2012 IEEE, 2012, pp. 1024-1031. Copyright 2012 by IEEE.

power converters. Despite using unidirectional switches, the sparse ac-link universal power converters can support bidirectional flow of power. However there are several applications that do not require bidirectional flow of power. For these applications the ultra-sparse ac-link universal power converter is proposed in this section. The ultra-sparse ac-link universal power converter requires fewer switches than the sparse ac-link universal power converter. Therefore, it is more reliable, more compact, less expensive, and less complicated compared to the sparse and conventional ac-link universal power converters.

4.2. Sparse AC-Link Universal Power Converter

As mentioned in section 2, in the ac-link universal power converters, the complementary switches are added to provide the link with alternating current. In the sparse ac-link universal converter, the complementary switches are removed; however, the link current is still alternating. Figure 154 represents this configuration, and as seen in this figure, the number of switches is reduced from 24 to 20 in the three-phase ac-ac case. The input and output switch bridges mainly contain unidirectional switches, and, in order to provide the link with alternating current, the intermediate cross-over switching circuits have been added to both the input side and the output side. Switches Si7, Si8, Si9 and Si10, which form the input-side intermediate cross-over switching circuit, and switches So7, So8, So9 and So10, which form the output-side intermediate cross-over switching circuit, permit the partially resonant circuit to operate bi-directionally, which affords the advantages discussed earlier. The performance of the proposed configurations is similar to that of the original ac-link universal power converter. The

link current and voltage are exactly the same as those of the original configuration and the partial resonance time is as short as in the original converter. As seen in Figure 154, there is a diode in series with each IGBT. Since conventional IGBTs cannot block the reverse voltage, these diodes are connected in series with the IGBTs. In case reverse-blocking IGBTs are used, the sparse configuration can be simplified further, as represented in Figure 155.

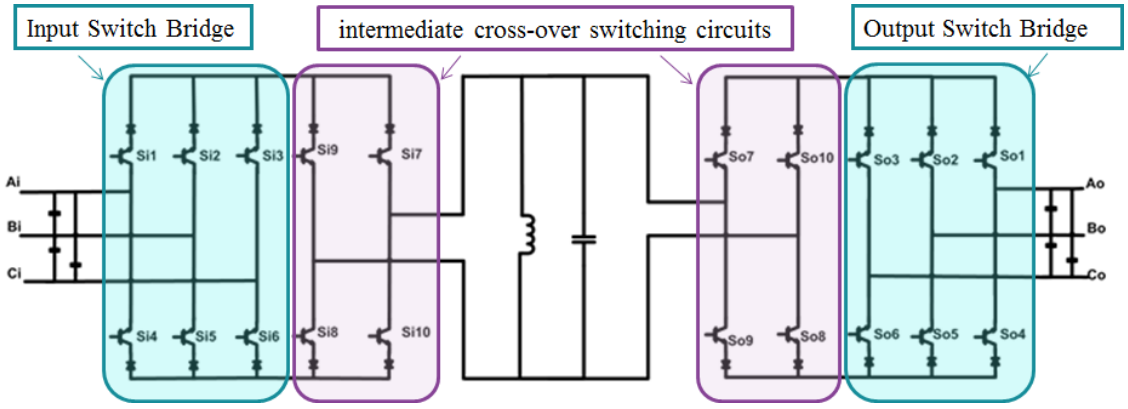


Figure 154 Sparse parallel ac-link universal power converter with conventional IGBTs

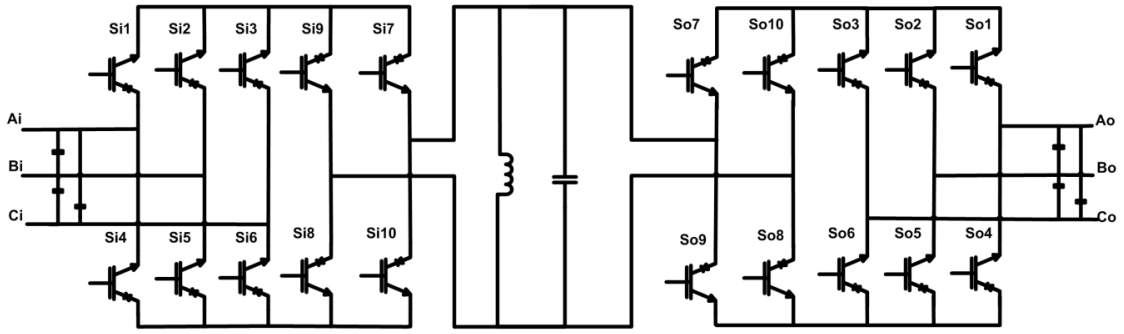
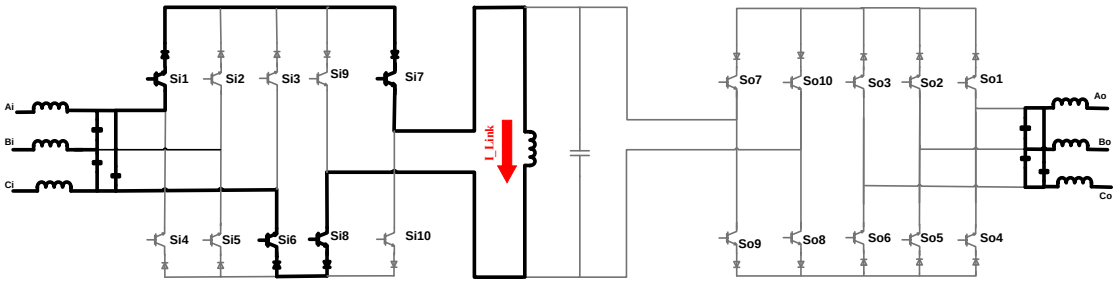


Figure 155 Sparse parallel ac-link universal power converter with reverse blocking IGBTs

Figure 156 and Figure 157 represent the behavior of the proposed configuration and the current/voltage waveforms at different modes, respectively. Modes 1-8 in the modified configuration are similar to those of the original converter, except other than turning on the proper switches on the input/output switch bridges; Si7 and Si8, on the

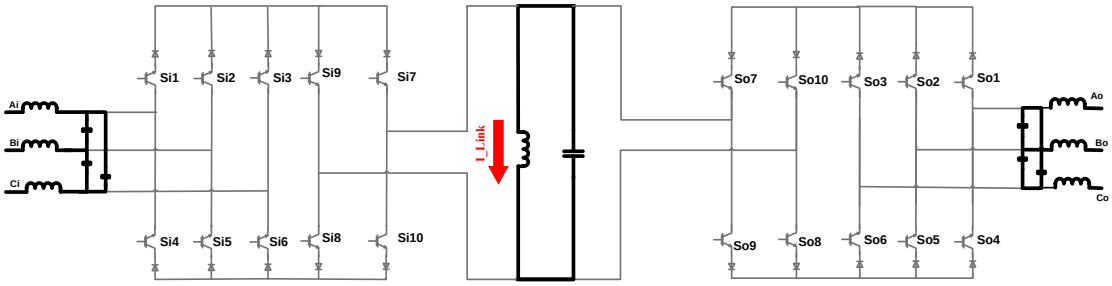
input-side intermediate cross-over switching circuit, should be turned on during modes 1-4; and, So7 and So8, on the output-side intermediate cross-over switching circuit, should be turned on during modes 5-8. Although the input and output switch bridges contain unidirectional switches, Si7–Si10 and So7–So10 (referenced above as intermediate cross-over switching circuits) enable the link to conduct both positive and negative currents. Therefore during modes 9-16, the same input/output switches as modes 1-8 will be conducting; however, instead of Si7 and Si8, switches Si9 and Si10 conduct during modes 9-12. Instead of So7 and So8, switches So9 and So10 conduct during modes 13-16.

Similar to the parallel and series ac-link universal power converters, the sparse configuration is universal and therefore, it can appear as dc-dc, dc-ac, ac-dc, ac-ac, or even hybrid converters. Figure 158 and Figure 159 represent the dc-ac sparse parallel ac-link converter. Since the proposed configuration does not lead to any switch count reduction at the dc side, the dc side is kept similar to the original configuration. As seen in these figures, the number of switches is reduced from 20 in original configuration to 18 in the sparse configuration. Behavior of the converter during different modes of operation is depicted in Figure 160 and Figure 161.

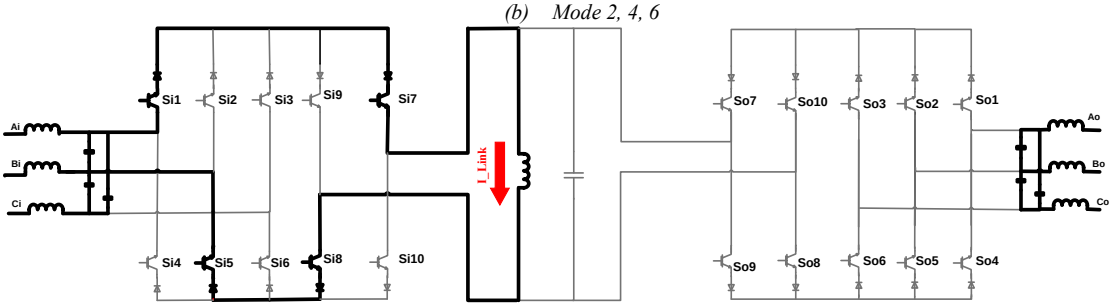


(a) Mode 1

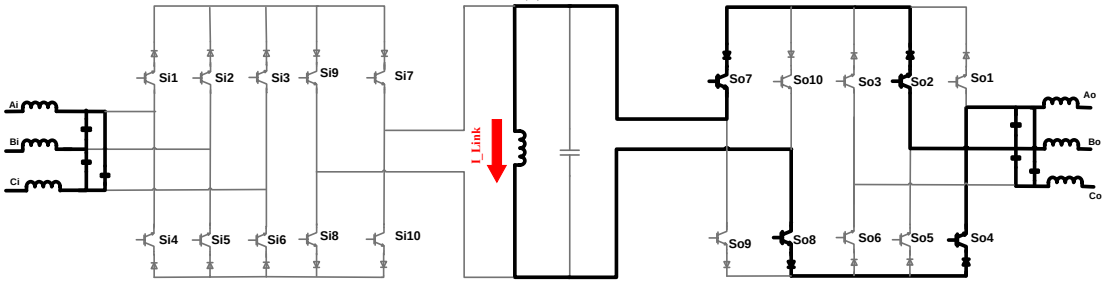
Figure 156 Behavior of the ac-ac sparse parallel ac-link universal converter during different modes of operation



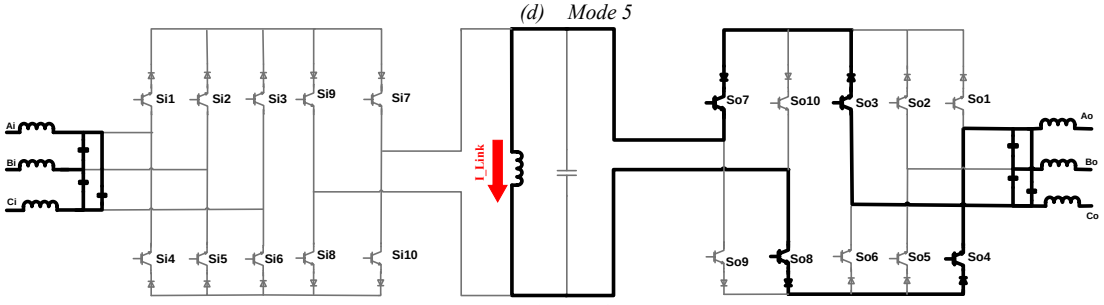
(b) Mode 2, 4, 6



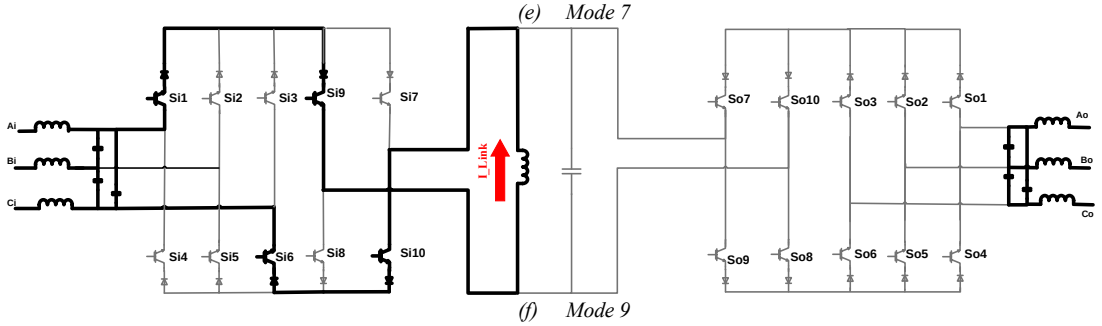
(c) Mode 3



(d) Mode 5



(e) Mode 7



(f) Mode 9

Figure 156 Continued.

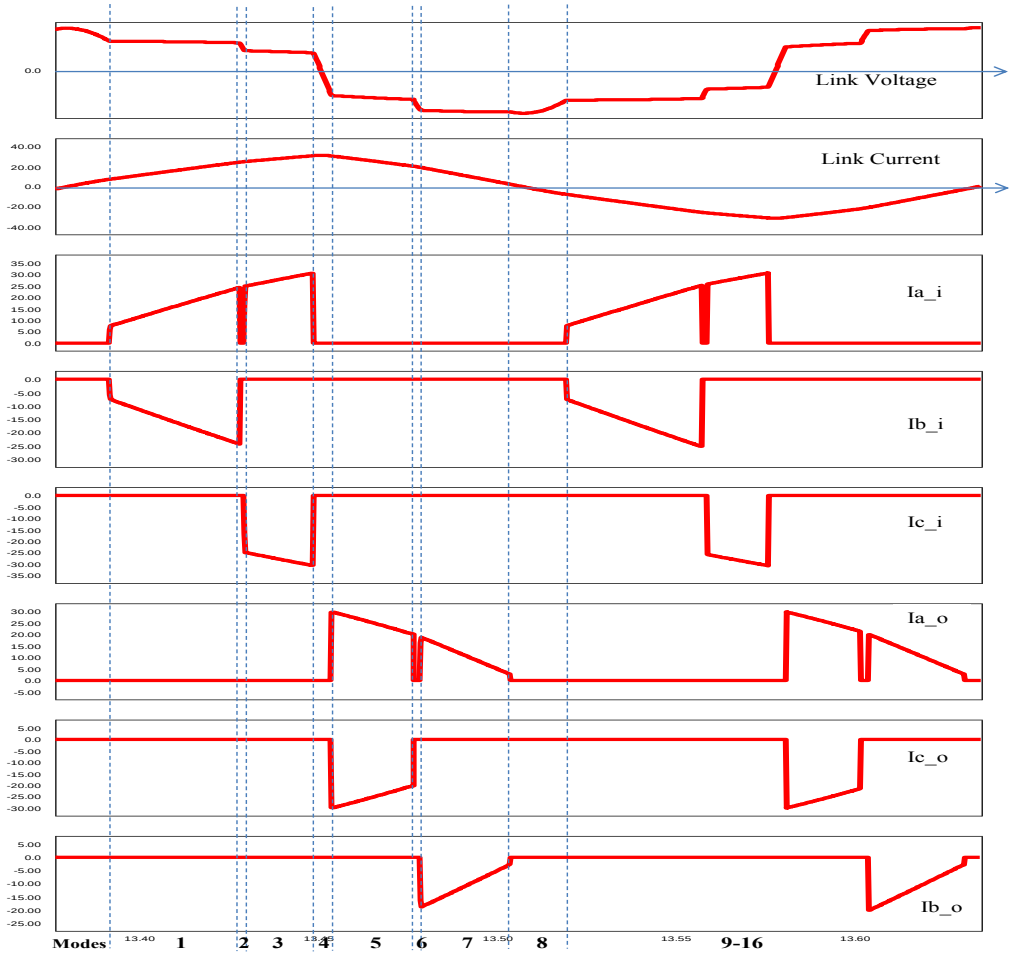


Figure 157 Voltage and current waveforms showing the behavior of the ac-ac sparse parallel ac-link universal converter during different modes of operation

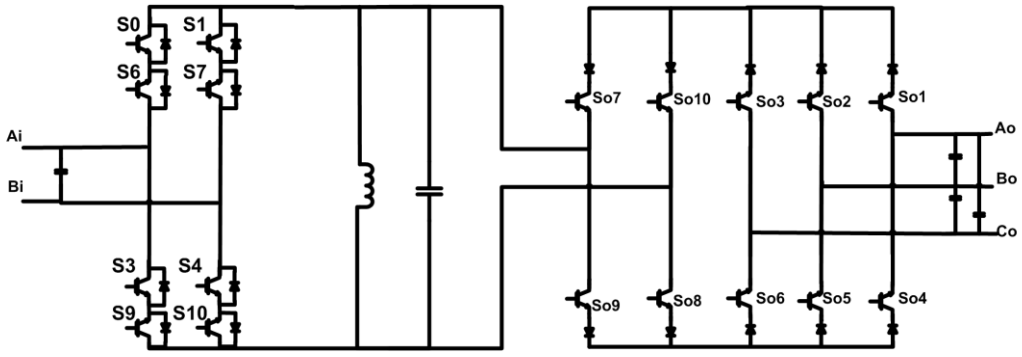


Figure 158 Dc-ac sparse parallel ac-link universal converter with regular IGBTs

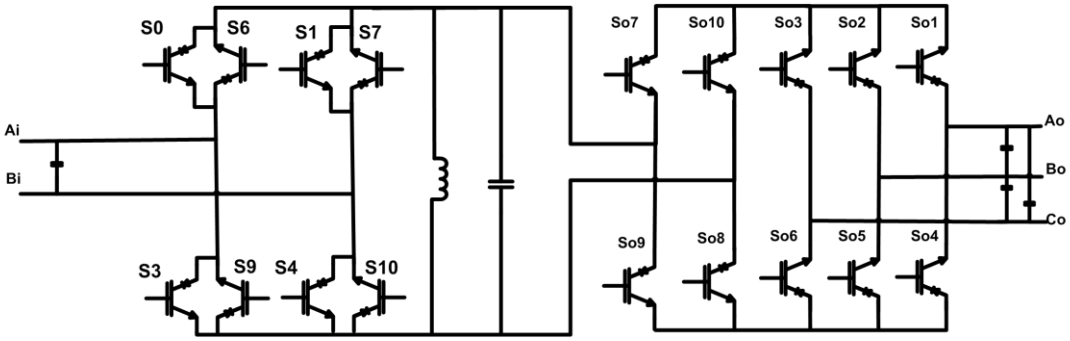


Figure 159 Dc-ac sparse parallel ac-link universal converter with Reverse Blocking IGBTs

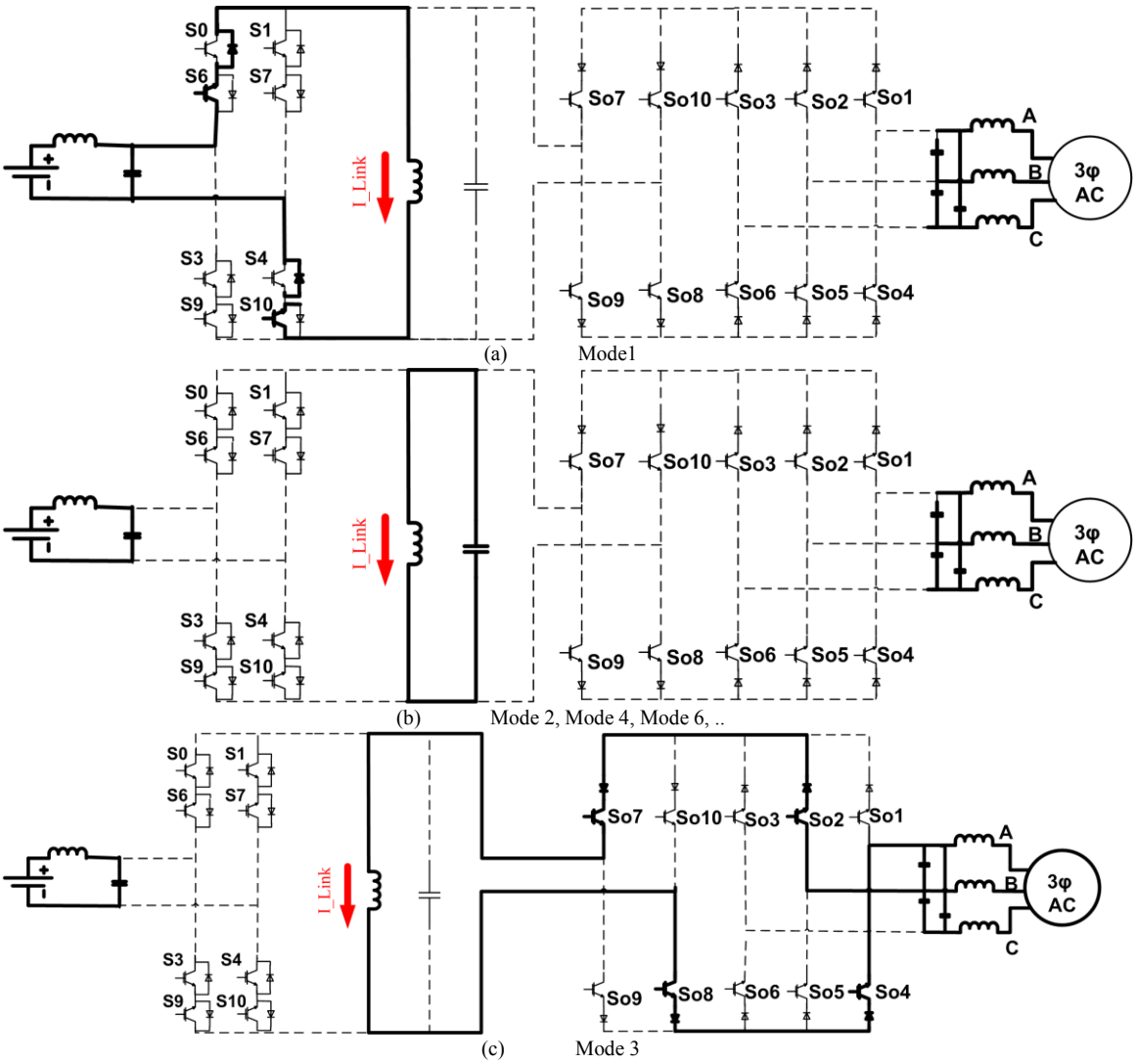
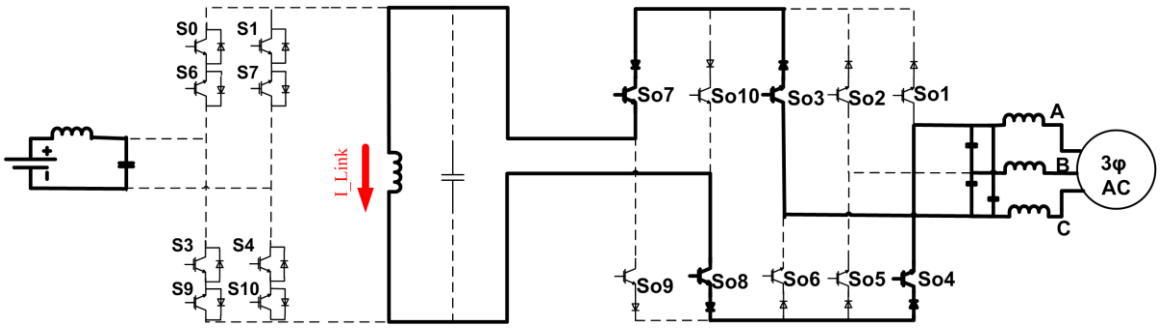
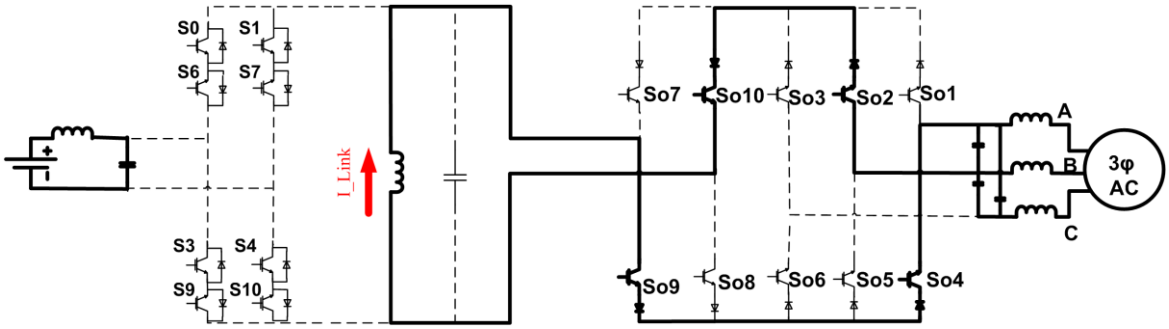


Figure 160 Behavior of the dc-ac sparse parallel ac-link universal power converter during different modes of operation



(d) Mode 5



(e) Mode 9

Figure 160 Continued.

As mentioned earlier, the sparse configuration may also be extended to the series ac-link universal power converter. Figure 162 shows the ac-ac sparse series ac-link universal power converter.

Both the parallel and series sparse ac-link universal power converters can provide galvanic isolation by adding a single phase high-frequency transformer to the link, as shown in Figure 163. Moreover, it is possible to have hybrid sparse ac-link universal power converters, as shown in Figure 164. This figure represents a hybrid sparse parallel ac-link universal power converter interfacing to a wind generator, PV, battery, and grid.

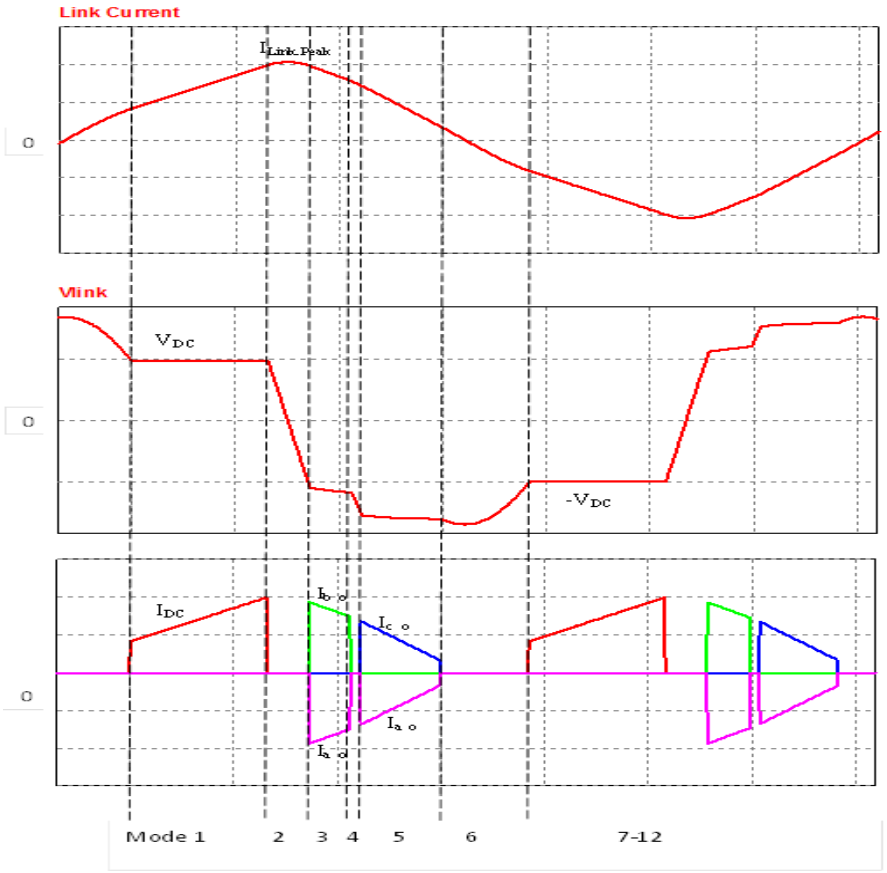


Figure 161 Link current, link voltage and unfiltered input and output currents in the dc-ac sparse parallel ac-link universal power converter

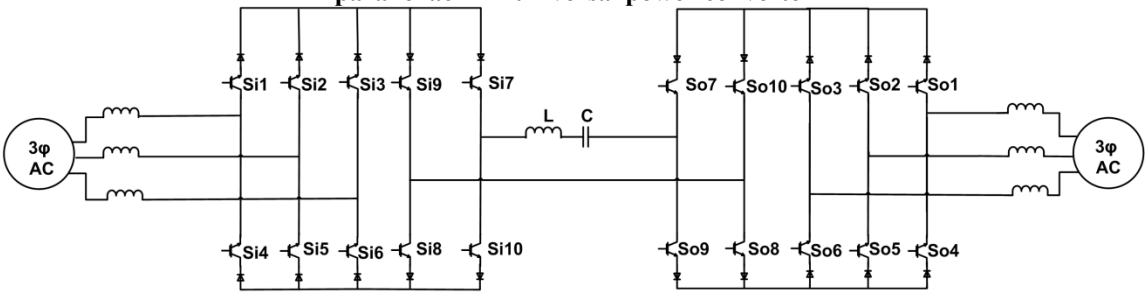


Figure 162 Ac-ac sparse series ac-link universal power converter

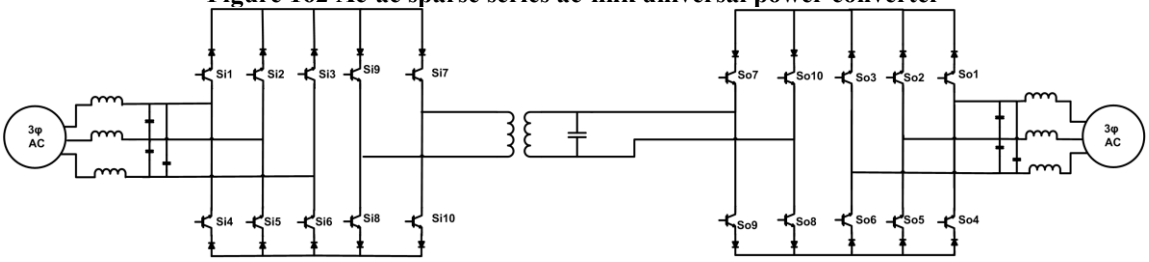


Figure 163 Ac-ac sparse parallel ac-link universal converter with galvanic isolation

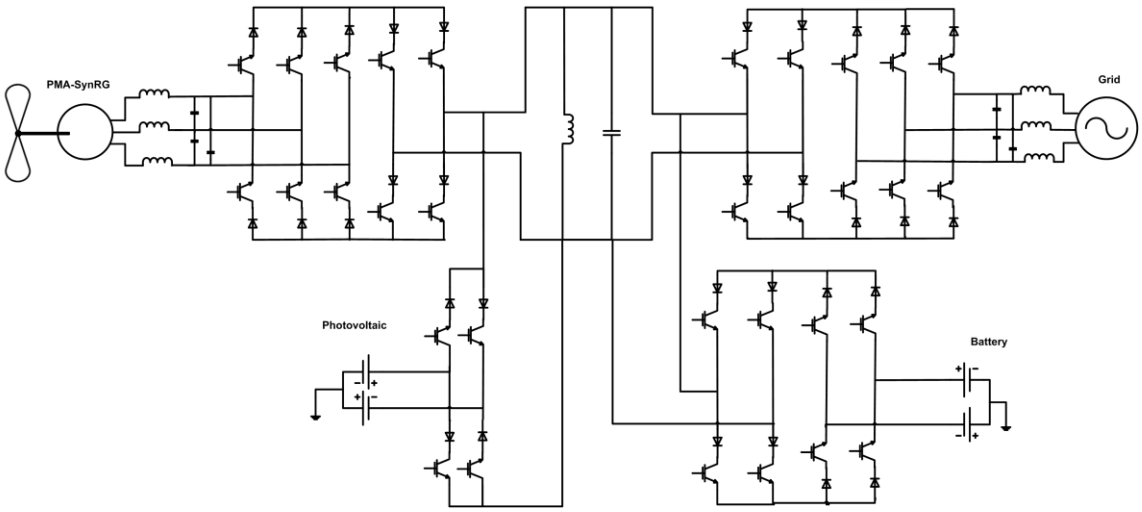


Figure 164 An example of the hybrid sparse parallel ac-link universal converter

4.3. Ultra-Sparse AC-Link Universal Power Converter

As mentioned earlier, the sparse ac-link universal power converters are bi-directional. However, there are several applications that do not require bi-directional flow of power, including wind power generation (ac-ac) and PV power generation (dc-ac). In order to further simplify the converter for these applications, another modified configuration, named ultra-sparse ac-link universal power converter, is proposed in this part. This configuration, as shown in Figure 165, contains 16 switches in the case of three-phase ac-ac conversion. Considering the unidirectional flow of power, the reverse blocking diodes placed in series with Si7, Si8, Si9, and Si10 can be removed and instead IGBTs with anti-parallel diodes may be employed. Moreover, reverse blocking IGBTs may be employed at the input and output switch bridges. Therefore, the configuration may be simplified as represented in Figure 166. As shown in Figure 167, Si7, Si8, Si9, and Si10 can be replaced with reverse blocking IGBTs, as well. The performance of the

proposed configurations is similar to that of the sparse parallel and parallel ac-link universal power converters. The link current and voltage are exactly the same as those of the original configuration and the partial resonant time is as short as in the original converter.

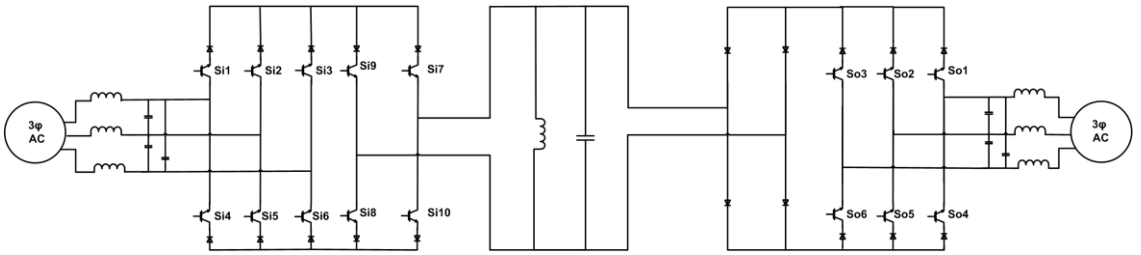


Figure 165 Ac-ac ultra sparse parallel ac-link universal converter

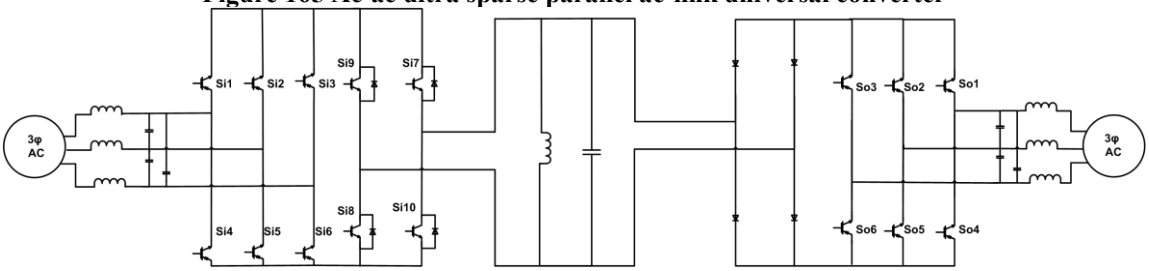


Figure 166 Ac-ac ultra-sparse parallel ac-link universal power converter with reverse-blocking IGBTs at both input and output switch bridges

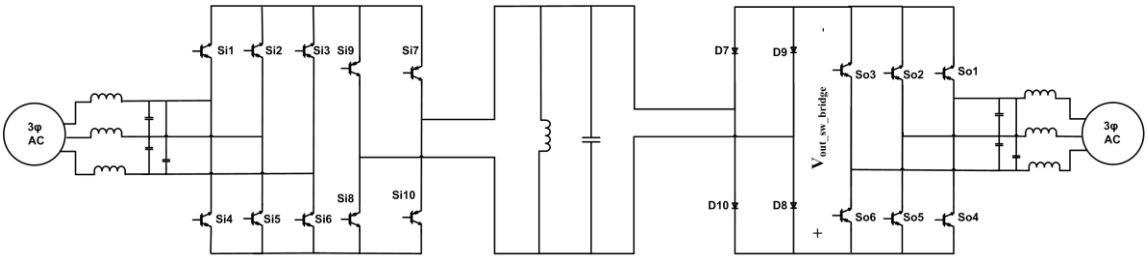


Figure 167 Ac-ac ultra-sparse ac-link universal power converter with reverse-blocking IGBTs at input and output switch bridges and the input-side intermediate cross-over switching circuits

In the sparse parallel ac-link universal power converter, shown in Figure 154, when the power flows from the input side to the output side, the output intermediate

cross-over switching circuit, which is formed by switches So7, S08, So9, and So10, acts like a rectifier. In the ultra-sparse parallel ac-link universal power converter, these switches are removed and the output intermediate cross-over switching circuit is formed by using only diodes. These diodes start to conduct as they become forward-biased; and, the diodes are not forward-biased when they are not supposed to conduct. Considering that the power is unidirectional and therefore, the link voltage is positive when Si7 and Si8 conduct, and it is negative when Si9 and Si10 conduct, the reverse blocking diodes in the input-side intermediate cross-over switching circuit can be removed and replaced by anti-parallel diodes. This configuration reduces the conduction losses of the switches. By using reverse blocking IGBTs the reverse blocking diodes on the input and output switch bridges may also be removed.

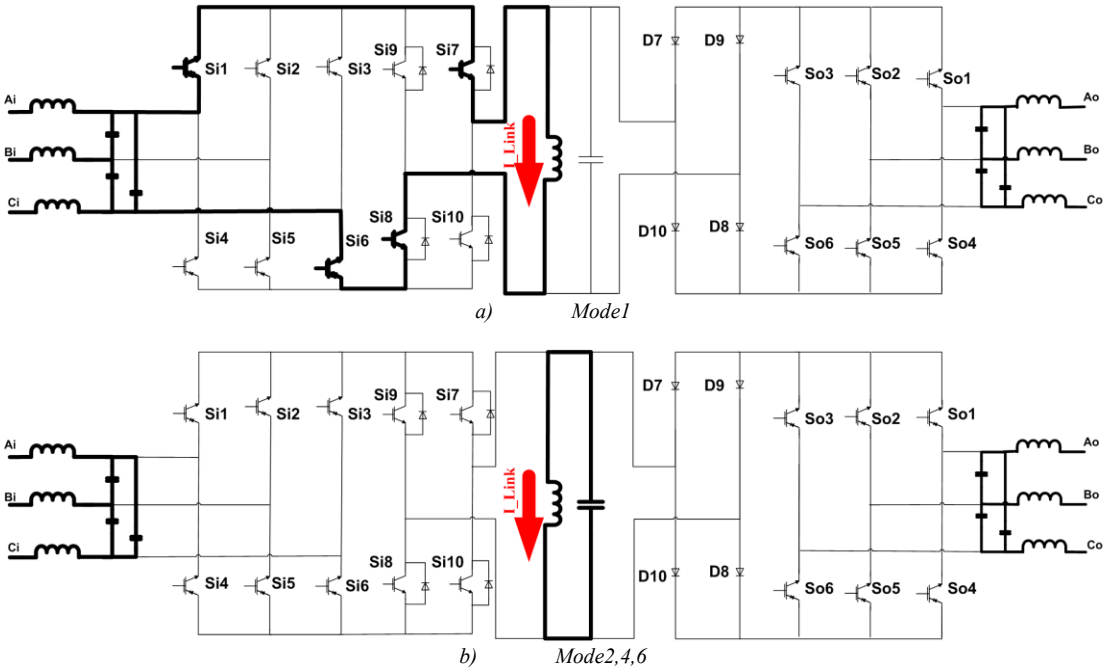


Figure 168 Behavior of the ultra-sparse parallel ac-link universal power converter during different modes of operation

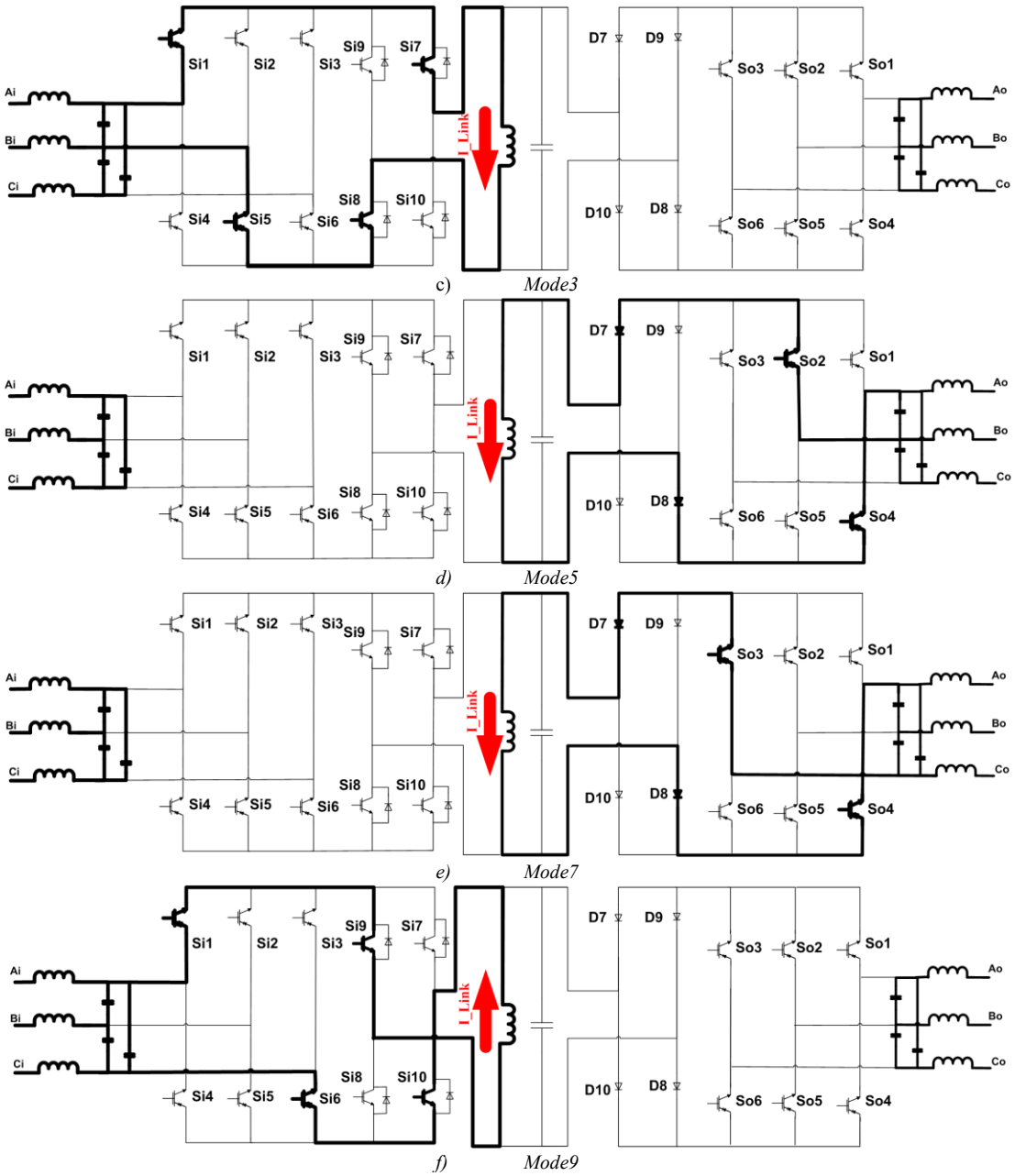
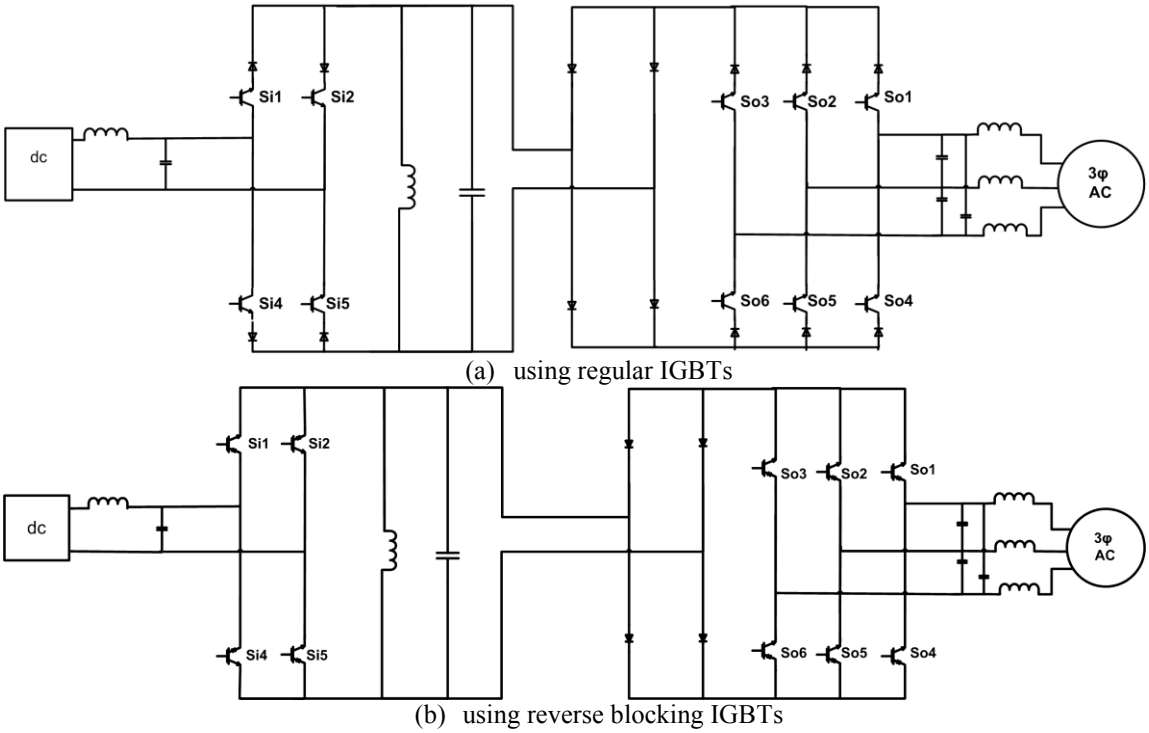


Figure 168 Continued.

Figure 168 represents the behavior of the ac-ac ultra-sparse configuration in different modes. The link voltage, the link current, and the input and output currents in

the ac-ac ultra-sparse parallel ac-link universal power converter are similar to those of the parallel ac-link universal power converter.

The ultra-sparse configuration is a universal converter as well. The dc-ac ultra-sparse ac-link universal converter is shown in Figure 169. Similar to the sparse configuration, the dc-side is kept the same as the original converter.



(a) using regular IGBTs

(b) using reverse blocking IGBTs

Figure 169 Dc-ac ultra-sparse ac-link universal converter

The ultra-sparse parallel ac-link universal converters (both dc-ac and ac-ac configurations) have some restrictions on the load power factor. When the switches on the output switch bridge are turned on, diodes D7 and D10 must not be forward-biased at the same time—otherwise, the load will be shorted. Similarly, diodes D8 and D9 must not be forward-biased at the same time. To satisfy this condition, the voltage seen across the output switch bridge, $V_{out\_sw\_bridge}$ in Figure 167, should be negative when the link is being discharged into the output.

Using the equations derived in section 2.7, when the current of phase A is positive and higher than the currents of phases B and C, V_{ba_o} and V_{ca_o} should be negative:

$$V_{ba\_o} = -\sqrt{3}V_{o,peak}\cos\left(\omega t - \frac{\pi}{3}\right) < 0 \tag{80}$$

$$V_{ca\_o} = -\sqrt{3}V_{o,peak}\cos\left(\omega t - \frac{2\pi}{3}\right) < 0 \tag{81}$$

which can be expressed as follows:

$$0 < \cos\left(\omega t - \frac{\pi}{3}\right) \tag{82}$$

$$0 < \cos\left(\omega t - \frac{2\pi}{3}\right) \tag{83}$$

On the other hand, $\omega t+\theta_o$ may vary between $\frac{\pi}{3}$ and $\frac{2\pi}{3}$ to have positive current on phase A, and negative currents on phases B and C. It can be shown that to avoid shorting the load the following condition should be valid:

$$\cos(\theta_o) > \frac{\sqrt{3}}{2} \tag{84}$$

Therefore, in order for the ultra-sparse parallel ac-link universal converter to operate properly, the load power factor should be higher than 0.86. It should be noted that θ_o is the angle between the voltage and the unfiltered current. Therefore, the actual power factor may be lower than 0.866.

4.4. Comparison of the Parallel, Sparse Parallel, and Ultra-Sparse Parallel AC-Link Universal Power Converters

Designing the link parameters is the same in the parallel, sparse parallel, and ultra-sparse parallel ac-link universal power converters. However, due to the unequal

number of switches, and consequently different switch conduction periods in these converters, the switch ratings will be different.

The link current is the same in all these converters. Therefore, the peak current each switch should tolerate is the same, whereas, the average current passing through the switches in the conventional, sparse, and ultra-sparse ac-link universal converters are different. The average current that the switches/diodes located on the switch bridges in the sparse and ultra-sparse parallel configurations should withstand is twice the average current passing through the switches in the parallel ac-link universal converter. The average current that the switches/diodes located at the intermediate cross–over switching circuits in the sparse and ultra-sparse configurations tolerate is three times the current passing through the switches in the parallel ac-link universal converter. However, the peak current of the switches is usually much higher than their average currents for parallel, sparse parallel and ultra-sparse parallel ac-link universal power converters. Consequently, peak current may become the limiting factor in choosing the switches. Therefore, the higher average current of the switches in the sparse and ultra-sparse ac-link universal power converters may not play any roles in choosing high current rating and consequently, more expensive switches.

In order to show the advantages and the disadvantages of the sparse and ultra-sparse configurations, their failure rates and efficiencies will be compared with those of the parallel ac-link universal power converter.

4.4.1. Efficiency

In this part the efficiency of the parallel, sparse parallel, and ultra-sparse parallel ac-link universal power converters will be estimated and compared. We will start with the parallel ac-link universal power converter, as shown in Figure 170. In this converter switches S0–S5 at the input side and S12–S17 at the output side, may conduct only during the half cycles that that the link current is negative. Switches S6–S11 and S18–S23 may conduct during the half cycles that the link current is positive. Therefore, the conduction loss of each switch at the input side and at the output side may be estimated as follows:

$$P_{Si\_m} = V_{TO,S} I_{Si,avg} + r_{T,S} I_{Si,rms}^2 = \frac{1}{2\pi} I_{i,peak} V_{TO,S} + \frac{1}{4} r_{T,S} I_{in,unfiltered,rms}^2 \quad (85)$$

$$P_{So\_m} = V_{TO,S} I_{So,avg} + r_{T,S} I_{So,rms}^2 = \frac{1}{2\pi} I_{o,peak} V_{TO,S} + \frac{1}{4} r_{T,S} I_{out,unfiltered,rms}^2 \quad (86)$$

In the above equations, $V_{TO,S}$, $r_{T,S}$, $I_{Si,rms}$, $I_{So,rms}$, $I_{in,unfiltered,rms}$, $I_{out,unfiltered,rms}$, $I_{si,avg}$, and $I_{so,avg}$ are the IGBT threshold voltage, IGBT series resistance, the input-side switch rms current, the output-side switch rms current, the rms of the unfiltered input-side phase current, the rms of the unfiltered output-side phase current, the average of the input-side switch current, and the average of the output-side switch current, respectively. Given that the current passing each IGBT is equal to the current passing the anti-parallel diode of the IGBT placed in series with that IGBT, the total conduction loss in the parallel ac-link universal power converter is equal to:

$$P_{Conduction\_parallel} = \frac{6}{\pi}\left(I_{i,peak} + I_{o,peak}\right)\left(V_{TO,S} + V_{TO,D}\right) + 3\left(I_{in,unfiltered,rms}^2 + I_{out,unfiltered,rms}^2\right)\left(r_{T,S} + r_{T,D}\right) \quad (87)$$

Where, $V_{TO,D}$, $r_{T,D}$ are the diode threshold voltage and the diode series resistance, respectively.

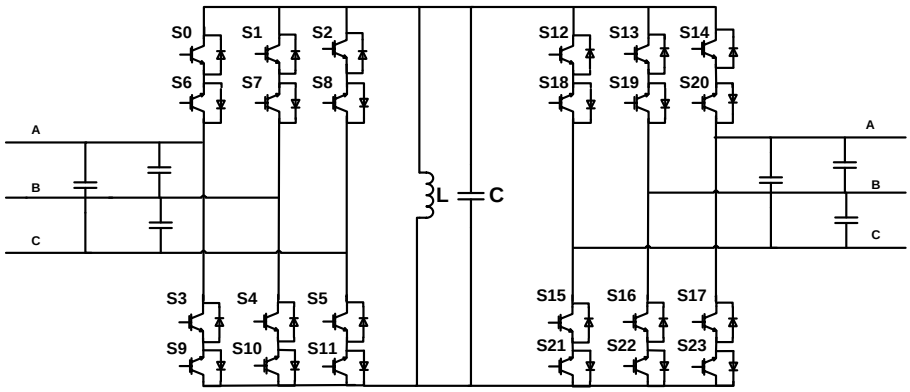


Figure 170 Ac-ac parallel ac-link universal converter

Of course, when using reverse blocking IGBTs, the conduction losses in the parallel ac-link universal converter may become almost half, as the bidirectional switches may be formed by placing two IGBTs in parallel instead of series. This configuration is represented in Figure 171. In this case the conduction losses may be estimated by the following equation:

$$P_{Conduction\_parallel\_RB} =$$

$$\frac{6}{\pi}\left(I_{i,peak} + I_{o,peak}\right)V_{TO,S} + 3\left(I^2_{in,unfiltered,rms} + I^2_{out,unfiltered,rms}\right)r_{T,S} \quad (88)$$

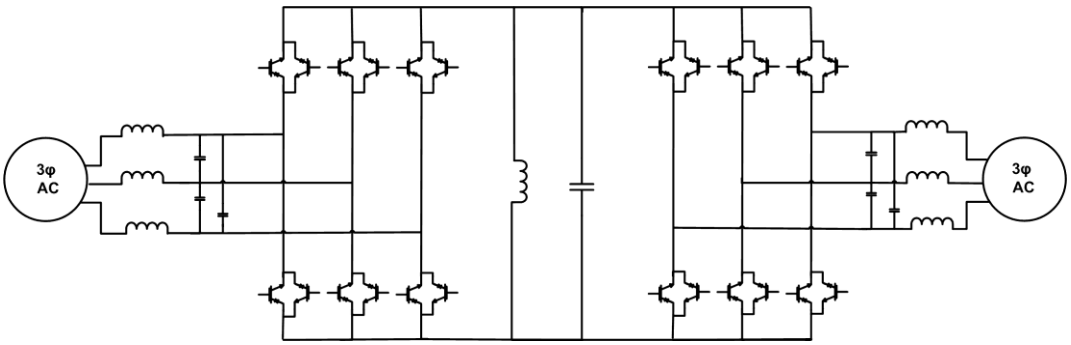


Figure 171 Ac-ac parallel ac-link universal converter using reverse blocking IGBTs

In a similar manner, conduction loss in the sparse ac-link universal converter, shown in Figure 154, can be calculated. The conduction losses of each switch located at the input and output switch bridges are as follows:

$$(1\leq m\leq 6) \quad P_{Si\_m} = \frac{1}{\pi} I_{i,peak} V_{TO,S} + \frac{1}{2} r_{T,S} I^2_{in,unfiltered,rms} \tag{89}$$

$$(1\leq m\leq 6) \quad P_{So\_m} = \frac{1}{\pi} I_{o,peak} V_{TO,S} + \frac{1}{2} r_{T,S} I^2_{out,unfiltered,rms} \tag{90}$$

During each half cycle of the link the current passing through the conducting switches located at the input and output intermediate cross-over switching circuits are equal to the maximum input and output currents, respectively. Of course half of these switches conduct during the first half cycle of the link and the other half conduct during the second half cycle of the link. Therefore, the conduction losses of the switches located at the input and output intermediate cross-over switching circuits are as follows:

$$(7\leq m\leq 10) \quad P_{Si\_m} = \frac{3}{2\pi} I_{i,peak} V_{TO,S} + \frac{3}{4} r_{T,S} I^2_{in,unfiltered,rms} \tag{91}$$

$$(7\leq m\leq 10) \quad P_{So\_m} = \frac{3}{2\pi} I_{o,peak} V_{TO,S} + \frac{3}{4} r_{T,S} I^2_{out,unfiltered,rms} \tag{92}$$

It can easily be shown that total conduction loss in the sparse parallel ac-link universal converter, shown in Figure 154, is as follows:

$$P_{Conduction\_sparse\_parallel} = \frac{12}{\pi}\left(I_{i,peak} + I_{o,peak}\right)\left(V_{TO,S} + V_{TO,D}\right) + 6\left(I^2_{in,unfiltered,rms} + I^2_{out,unfiltered,rms}\right)\left(r_{T,S} + r_{T,D}\right) \tag{93}$$

This loss is twice the conduction loss in the parallel ac-link universal converter. If the reverse blocking IGBTs are used, as shown in Figure 155, the conduction loss will be:

$$P_{Conduction\_sparse\_parallel\_RB} = \frac{12}{\pi}\left(I_{i,peak} + I_{o,peak}\right)V_{TO,S} + 6\left(I^2_{in,unfiltered,rms} + I^2_{out,unfiltered,rms}\right)r_{T,D} \quad (94)$$

It can easily be shown that in the ac-ac ultra-sparse parallel ac-link universal power converter, shown in Figure 166, the conduction loss is as follows:

$$P_{Conduction\_ultra\_sparse\_parallel} = \frac{12}{\pi}\left(I_{i,peak}V_{TO,S} + \frac{1}{2}I_{o,peak}V_{TO,S} + \frac{1}{2}I_{i,peak}V_{TO,D} + I_{o,peak}V_{TO,D}\right) + 6\left(I^2_{in,unfiltered,rms}r_{T,S} + \frac{1}{2}I^2_{out,unfiltered,rms}r_{T,S} + \frac{1}{2}I^2_{in,unfiltered,rms}r_{T,D} + I^2_{out,unfiltered,rms}r_{T,D}\right) \quad (95)$$

If reverse blocking IGBTs are used, as depicted in Figure 167, the conduction loss of the ac-ac ultra–sparse parallel ac-link universal power converter is:

$$P_{Conduction\_ultra\_sparse\_parallel\_RB} = \frac{12}{\pi}\left(I_{i,peak}V_{TO,S} + \frac{1}{2}I_{o,peak}V_{TO,S} + \frac{1}{2}I_{o,peak}V_{TO,D}\right) + 6\left(I^2_{in,unfiltered,rms}r_{T,S} + \frac{1}{2}I^2_{out,unfiltered,rms}r_{T,S} + \frac{1}{2}I^2_{out,unfiltered,rms}r_{T,D}\right) \quad (96)$$

Other important sources of power dissipation in these converters are inductor copper loss and inductor core loss. In the fabricated low-power prototype, Magnetics Molypermalloy Powder (MPP) cores are used for the link inductors. For the selected cores, the copper loss and the core loss are calculated as follows [46]:

$$P_{Copper} = 0.0376 * I^2_{Link,Peak} \quad (97)$$

$$P_{Core} = 8.57 * 10^{-6} * f_{Link}^{1.65} \quad (98)$$

Because the link behavior is the same for all of these converters, the copper loss and the core loss in the parallel, sparse parallel, and ultra-sparse parallel ac-link universal converters will be the same. The copper loss increases by increasing the power level; whereas the core loss decreases by increasing the power level.

The conduction losses of the dc-ac parallel ac-link universal converter, dc-ac sparse parallel ac-link universal converter (as shown in Figure 158 and Figure 159), and dc-ac ultra-sparse parallel ac-link universal converter (as shown in Figure 169) are estimated as follows:

$$P_{Conduction\_dc\_ac\_parallel} = \left(2I_{dc} + \frac{6}{\pi} I_{o,peak}\right)\left(V_{TO,S} + V_{TO,D}\right) + \left(2I^2_{in,unfiltered,rms} + 3I^2_{out,unfiltered,rms}\right)\left(r_{T,S} + r_{T,D}\right) \quad (99)$$

$$P_{Conduction\_dc\_ac\_parallel\_RB} = \left(2I_{dc} + \frac{6}{\pi} I_{o,peak}\right)\left(V_{TO,S}\right) + \left(2I^2_{in,unfiltered,rms} + 3I^2_{out,unfiltered,rms}\right)\left(r_{T,S}\right) \quad (100)$$

$$P_{Conduction\_dc\_ac\_sparse\_parallel} = \left(2I_{dc} + \frac{12}{\pi} I_{o,peak}\right)\left(V_{TO,S} + V_{TO,D}\right) + \left(2I^2_{in,unfiltered,rms} + 6I^2_{out,unfiltered,rms}\right)\left(r_{T,S} + r_{T,D}\right) \quad (101)$$

$$P_{Conduction\_dc\_ac\_sparse\_parallel\_RB} = \left(2I_{dc} + \frac{12}{\pi} I_{o,peak}\right)\left(V_{TO,S}\right) + \left(2I^2_{in,unfiltered,rms} + 6I^2_{out,unfiltered,rms}\right)\left(r_{T,S}\right) \quad (102)$$

$$P_{Conduction\_dc\_ac\_ultra\_sparse\_parallel} = \left(2I_{dc}V_{TO,S} + \frac{6}{\pi} I_{o,peak}V_{TO,S} + I_{dc}V_{TO,D} + \frac{12}{\pi} I_{o,peak}V_{TO,D}\right) +$$

$$\left(2I_{in,unfiltered,rms}^{2}r_{T,S} + 3I_{out,unfiltered,rms}^{2}r_{T,S} + I_{in,unfiltered,rms}^{2}r_{T,D} + 6I_{out,unfiltered,rms}^{2}r_{T,D}\right) \quad (103)$$

$$P_{Conduction\_dc\_ac\_ultra\_sparse\_parallel\_RB} = \left(2I_{dc}V_{TO,S} + \frac{6}{\pi}I_{o,peak}V_{TO,S} + \frac{6}{\pi}I_{o,peak}V_{TO,D}\right) + \left(2I_{in,unfiltered,rms}^{2}r_{T,S} + 3I_{out,unfiltered,rms}^{2}r_{T,S} + 3I_{out,unfiltered,rms}^{2}r_{T,D}\right) \quad (104)$$

In order to compare the three topologies from the efficiency point of view, ac-ac parallel, sparse parallel, and ultra-sparse parallel ac-link universal power converters were designed, and the parameters are listed in Table 15. Figure 172 shows the efficiency of each of these converters over a range of power. As seen in this figure, the efficiency of the ultra-sparse parallel ac-link universal converter with reverse blocking IGBTs is as high as the efficiency of the parallel ac-link universal converters with regular IGBTs. As expected, the efficiency of the conventional parallel ac-link universal converter with the reverse blocking IGBTs is higher than the other converters.

In Figure 172, the efficiency of a 1.5 kW dc-link converter with the same input and output specifications as the designed parallel, sparse parallel, and ultra-sparse parallel ac-link universal converters is shown as well. Two different switching frequencies (4 kHz and 8 kHz) are considered. The efficiency of the dc-link converter with 8 kHz switching frequency is lower than the parallel ac-link converter, mainly due to the switching losses. Similar to the ac-ac configuration, the efficiencies of the dc-ac parallel, sparse parallel, and ultra-sparse parallel ac-link universal power converters with the specifications listed in Table 16 are compared. Figure 173 shows this comparison.

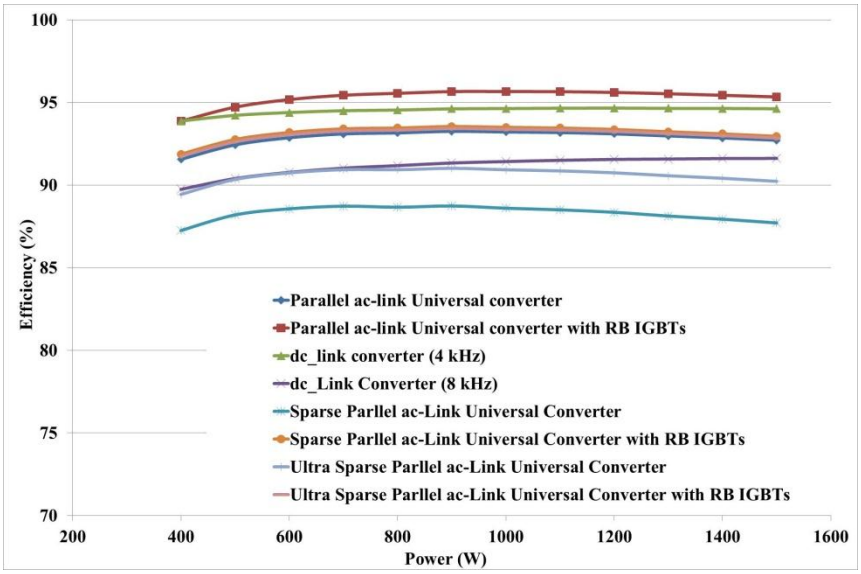


Figure 172 Efficiency of the ac-ac parallel, sparse parallel, and ultra-sparse parallel ac-link universal power converters and the ac-ac dc-link converter

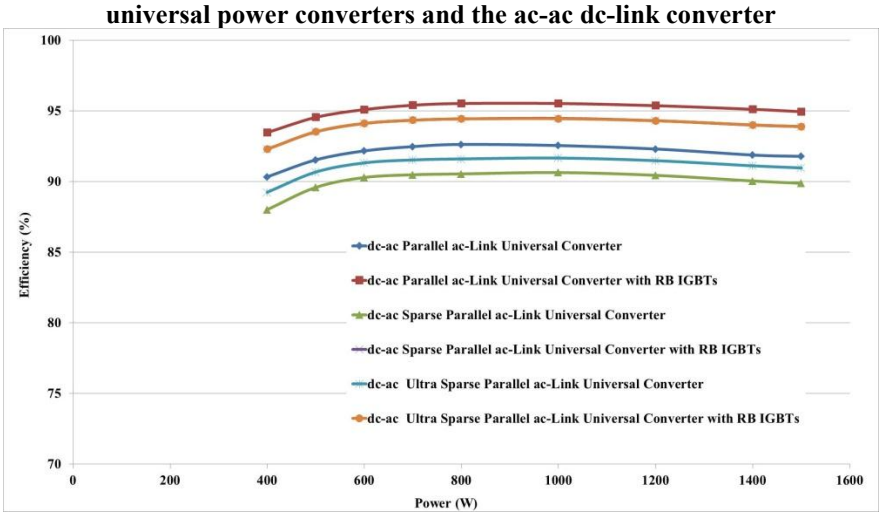


Figure 173 Efficiency of the dc-ac parallel, sparse parallel, and ultra-sparse parallel ac-link universal power converters

TABLE 15 PARAMETERS OF THE AC-AC CONVERTERS

Parameter	**Value**
Power rating	1.5 kW
Input voltage (three-phase ac)	150 V
Output voltage (three-phase ac)	208 V
Link inductance (L)	884 µH
Link capacitance (C)	400 nF

TABLE 16 PARAMETERS OF THE DC-AC CONVERTERS

Parameter	**Value**
Power rating	1.5 kW
Input voltage (dc)	200 V
Output voltage (three-phase ac)	208 V
Link inductance (L)	884 µH
Link capacitance (C)	400 nF

4.4.2. Reliability

Reliability is another important criterion on which power electronics converters can be compared. To predict the reliability of a converter, it is necessary to first calculate each component's failure rate (λ_p), which is estimated by multiplying the listed base failure rate values (λ_b) by the π factors that take into account the stresses [47]:

$$\lambda_p = \lambda_b(\prod_{i=1}^{n} \pi_i) \tag{105}$$

where n is the number of π factors for each component. MIL-HDBK 217 handbook lists the base failure rates for electronic devices [47-49].

Using [48], the failure rates of the parallel ac-link universal power converter, sparse parallel ac-link universal power converter (as shown in Figure 154), and ultra-sparse parallel ac-link universal power converter (as shown in Figure 165), with the parameters listed in Table 15, are estimated over a temperature range. The results are shown in Figure 174.

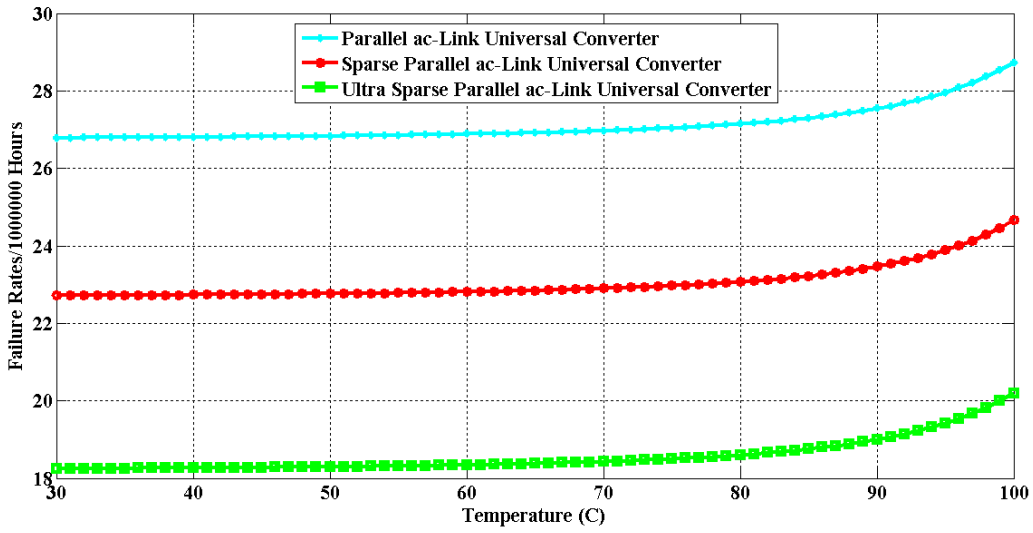


Figure 174 Failure rates of different ac-ac configurations

As seen in this figure, the failure rate of the sparse parallel ac-link universal converter is 15% less than the failure rates of the parallel ac-link universal power converter. The failure rate of the ultra-sparse parallel ac-link converter is 32% less than that of the parallel ac-link universal converter. This implies that the life time of the ultra-sparse configuration is 47% higher than that of the parallel ac-link converter.

4.5. Simulation and Experimental Results

4.5.1. DC-AC and AC-DC Sparse Parallel AC-Link Universal Power Converter

In this part, the performance of the bidirectional dc-ac sparse parallel ac-link universal power converters will be evaluated. The parameters of the simulated and tested converter are listed in Table 16.

Figure 175–Figure 177 depict the simulation results corresponding to the dc-ac sparse parallel ac-link universal converter operating at 800 W, when the power flows from the dc side to the ac side. These results can be compared with Figure 51–Figure 53, which show the simulation results corresponding to the dc-ac parallel ac-link universal power converter operating at 800 W. Figure 175 represents the dc-side current and scaled voltage in the sparse parallel ac-link universal converter. The dc-side current is slightly higher than that of the parallel ac-link universal converter, as the efficiency of the sparse configuration is lower than the conventional configuration. The ac-side currents are depicted in Figure 176. The link current and voltage are represented in Figure 177. As seen in this figure, the peak and frequency of the link current are 17.75 A and 3.77 kHz, respectively. These values are very close to those of the parallel ac-link

universal converter. Similar to the dc-ac parallel ac-link universal converter, the sparse configuration can provide bi-directional power flow.

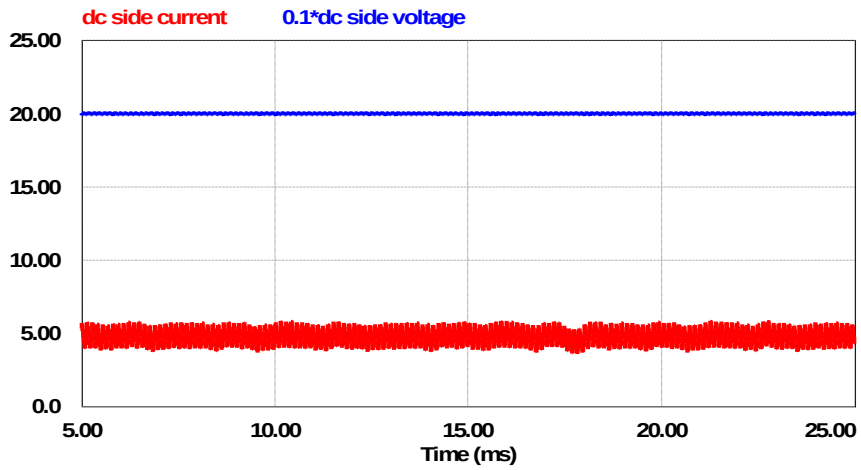


Figure 175 Dc-side current and scaled voltage in the dc-ac sparse parallel ac-link universal converter (simulation, dc-ac power flow)

Figure 178–Figure 180 show the behavior of the dc-ac sparse ac-link universal power converter for the case that power flows from the ac-side to the dc-side. These figures may be compared with Figure 59–Figure 61 which show the same scenario for the parallel ac-link universal power converter. Figure 178 shows the dc-side current and scaled voltage. The ac-side currents and the link current/voltage are depicted in Figure 179 and Figure 180, respectively. These results are similar to the simulation results corresponding to the parallel ac-link universal converter, which implies the parallel and sparse parallel ac-link universal power converters have the same principles of operation and performance.

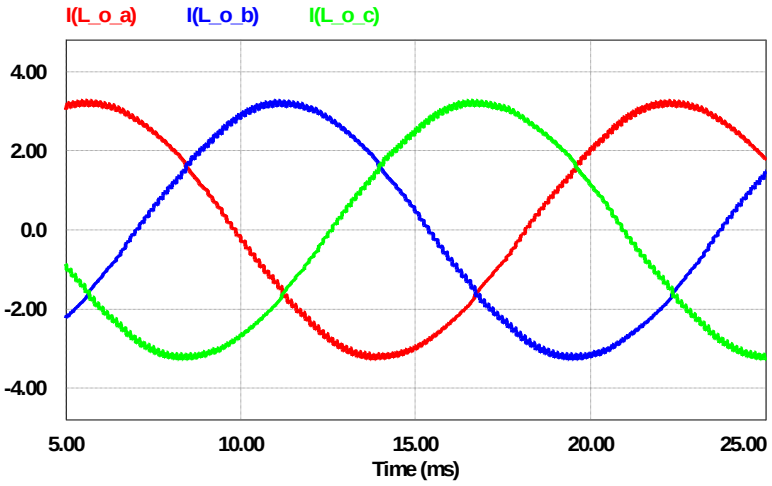


Figure 176 Ac-side currents in the dc-ac sparse parallel ac-link universal converter (simulation, dc-ac power flow)

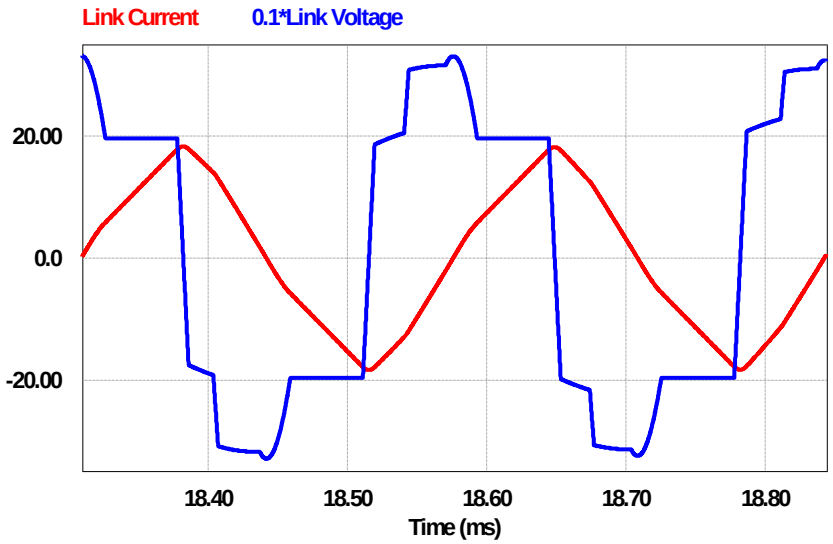


Figure 177 Link current and scaled voltage in the dc-ac sparse parallel ac-link universal converter (simulation, dc-ac power flow)

The dc-ac sparse parallel ac-link converter has been experimentally evaluated, as well. Again, the multi-purpose and modular prototype has been used to test this converter. Figure 181 shows how different boards were connected to test the dc-ac sparse parallel ac-link converter. As seen in this figure, a switch bridge board is used as the output intermediate cross-over switching circuit of the sparse configuration when

half of the switches on this board are disabled. Moreover, half of the switches on the output switch bridge are disabled. Figure 182–Figure 185 represent the experimental results corresponding to the dc-ac operation of this converter. Figure 182 shows the dc-side current and voltage. The ac-side currents are illustrated in Figure 183. Figure 184 depicts the link current and voltage. The link peak current and the link frequency are 18.7 A and 3.56 kHz, respectively. Figure 185 shows the current flowing in the ac-side switch bridge, the current flowing in the intermediate cross-over switching circuit, and the link current. As seen in this figure, the intermediate cross-over switching circuit has made it possible for the link current to be alternating, despite having unidirectional switches at the output switch bridge.

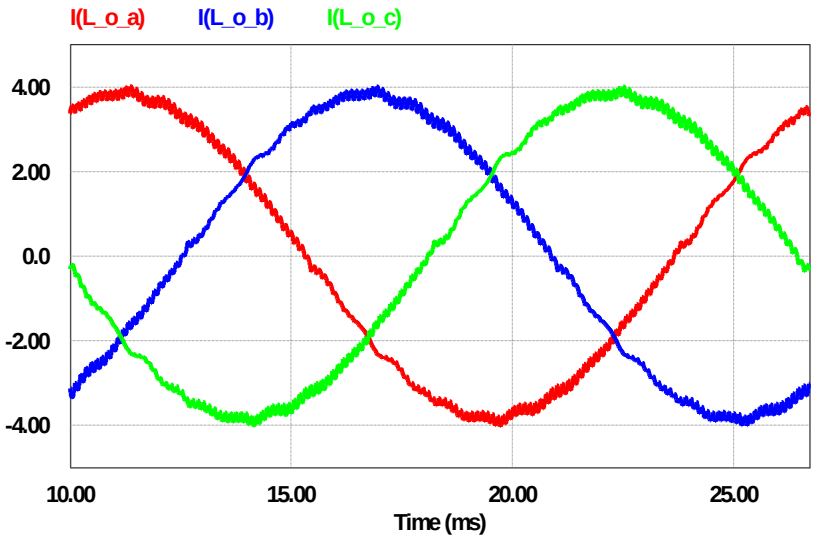


Figure 178 Ac-side currents in the dc-ac sparse parallel ac-link universal converter (simulation, ac-dc power flow)

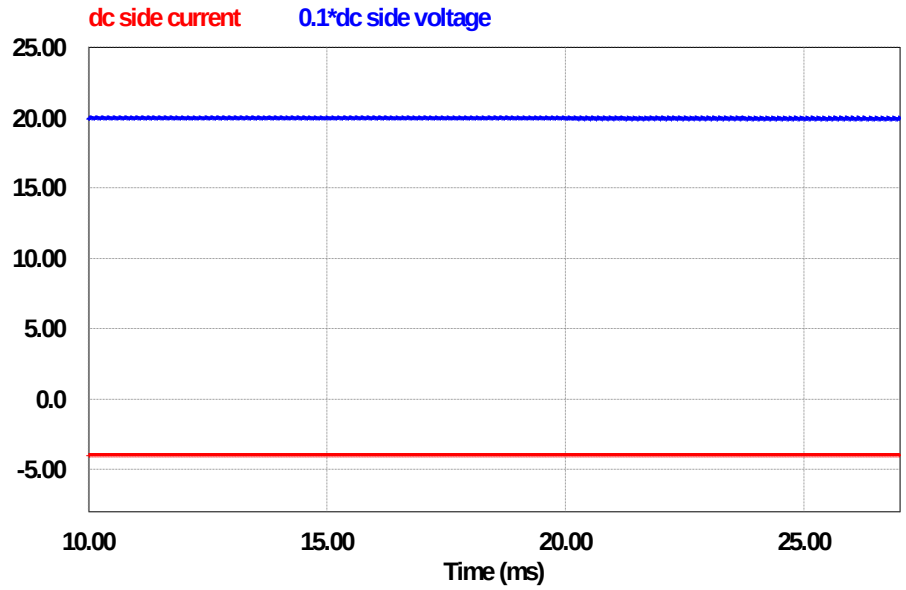


Figure 179 Dc-side current and scaled voltage in the dc-ac sparse parallel ac-link universal converter (simulation, ac-dc power flow)

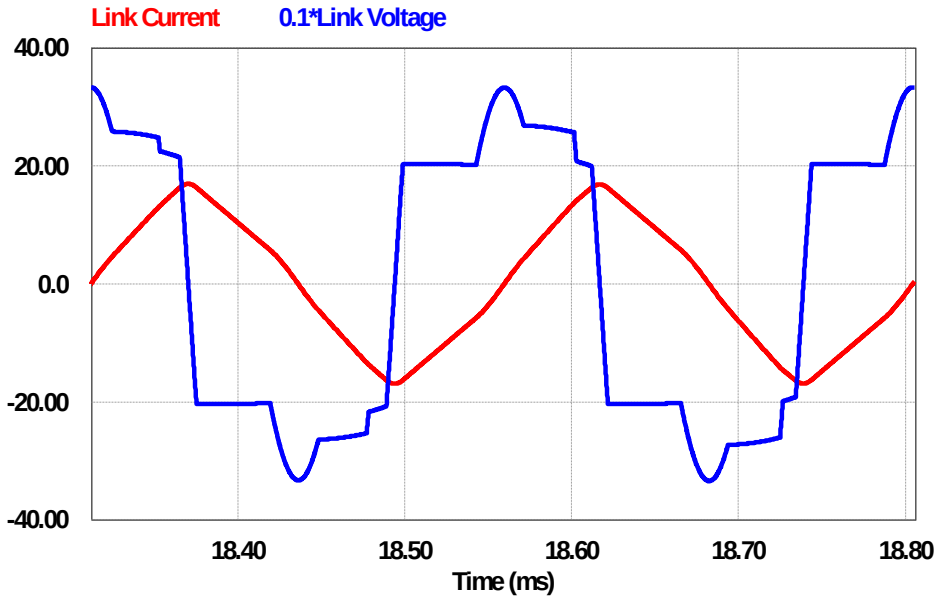


Figure 180 Link current and scaled voltage in the dc-ac sparse parallel ac-link universal converter (simulation, ac-dc power flow)

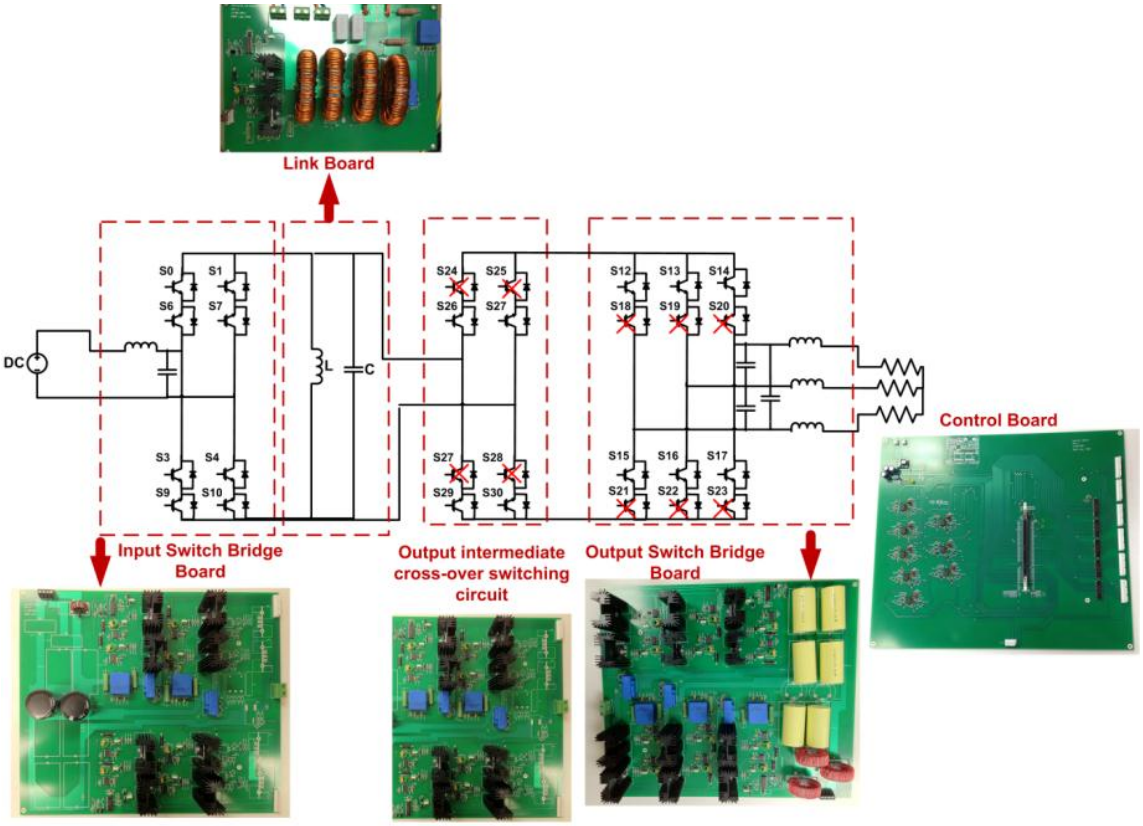


Figure 181 Different parts of the prototype for testing the dc-ac sparse parallel ac-link universal converter

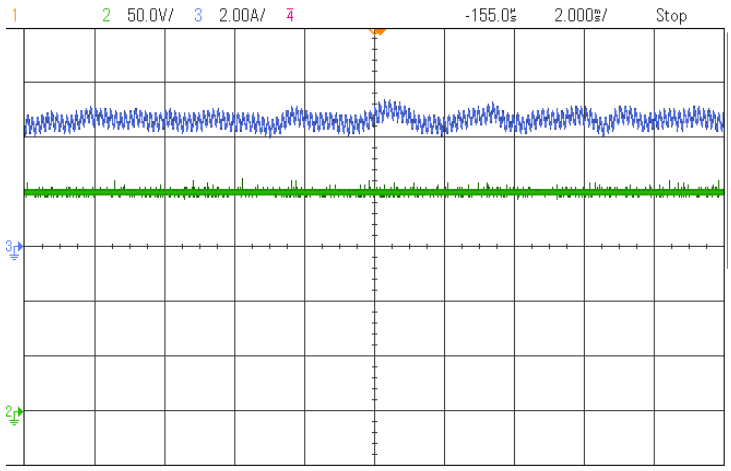


Figure 182 Dc-side current and voltage in the dc-ac sparse parallel ac-link universal converter (experiment, dc-ac power flow)

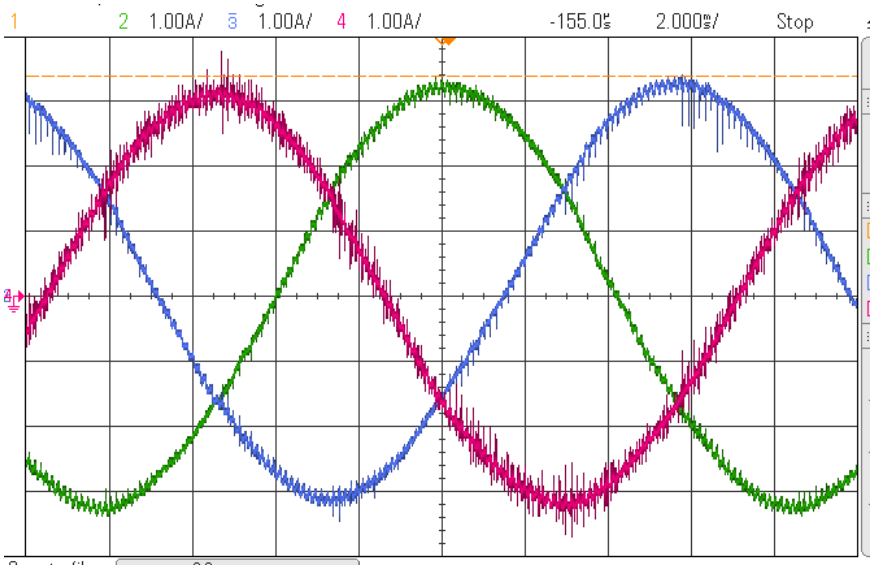


Figure 183 Ac-side currents in the dc-ac sparse parallel ac-link universal converter (experiment, dc-ac power flow)

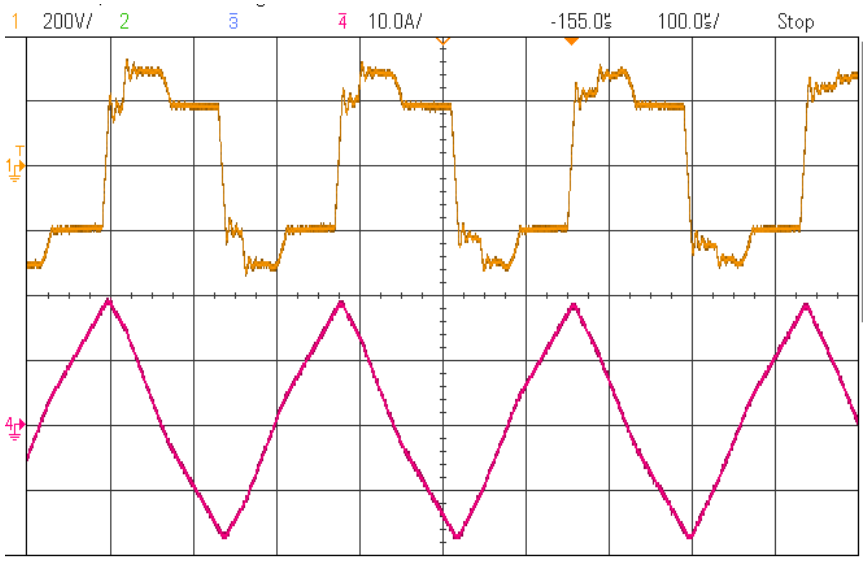


Figure 184 Link current and voltage in the dc-ac sparse parallel ac-link universal converter (experiment, dc-ac power flow)

Finally, Figure 186–Figure 187 show the experimental results corresponding to the ac-to-dc mode of operation of the sparse parallel ac-link universal converter operating at 200 W. The ac-side voltage is 120 V and the dc side is a 50 ohms resistive

load. Figure 186 shows the link current and voltage in this converter. The link peak current is 8.4 A in this case and the link frequency is 5.93 kHz. The dc-side current, which is regulated at 1 A, is represented in Figure 187.

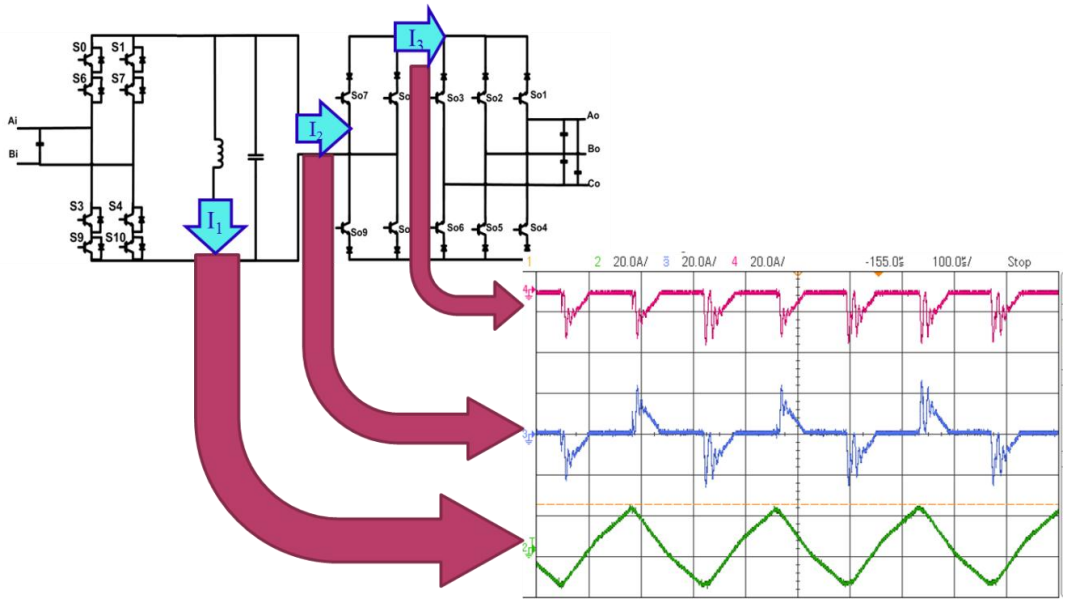


Figure 185 Current flowing the ac-side switch bridge (top), current flowing the intermediate cross-over switching circuit (middle), and the link current (bottom) in the dc-ac sparse parallel ac-link universal converter (experiment, dc-ac power flow)

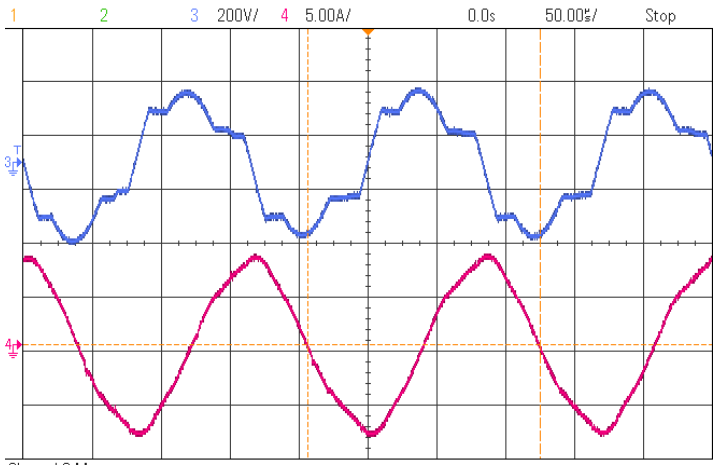


Figure 186 Link voltage and current in the dc-ac sparse parallel ac-link universal converter (experiment, ac-dc power flow)

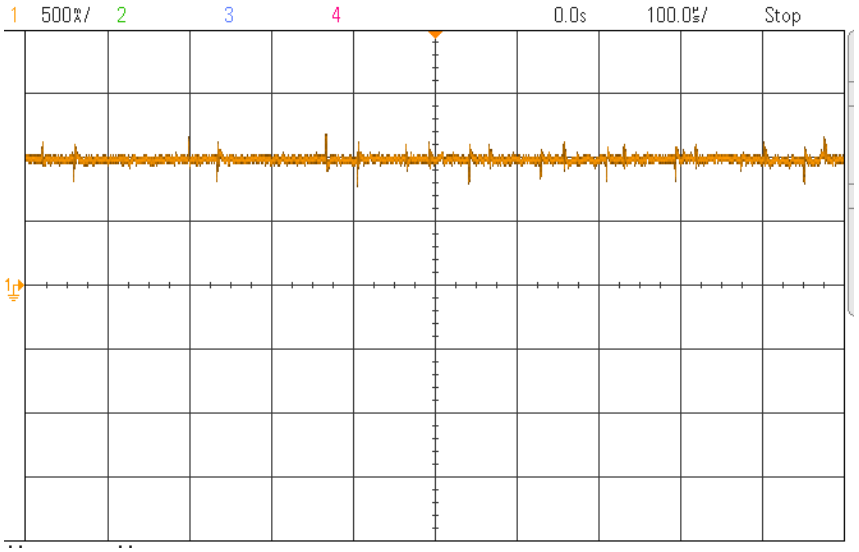


Figure 187 Dc-side current in the dc-ac sparse parallel ac-link universal converter (experiment, ac-dc power flow)

4.5.2. DC-AC Ultra Sparse Parallel AC-Link Universal Power Converter

The dc-ac ultra-sparse parallel ac-link universal power converter was experimentally evaluated as well, and the results are presented in this part. Figure 188 shows different parts of the converter. Similar to the dc-ac sparse parallel ac-link universal power converter, one of the switch boards is used as the output intermediate cross-over switching circuit. However, all the switches on this board are disabled and half of them are shorted as well. Therefore, only four diodes from this board are operating. This converter is tested at 800 W and Figure 189–Figure 192 represent the results. The parameters of the tested system are similar to the parameters listed in Table 16. The dc-side current and voltage are shown in Figure 189. The converter is tested at 800 W and the dc-side voltage is 200 V. The load currents are illustrated in Figure 190. Similar to the experimental evaluation of the dc-ac parallel and sparse parallel converters, a three-phase resistive load is used. The link current and voltage are shown

in Figure 191. The link current and voltage in this converter look similar to those of the parallel and sparse parallel configurations, as the performance of all three converters are the same.

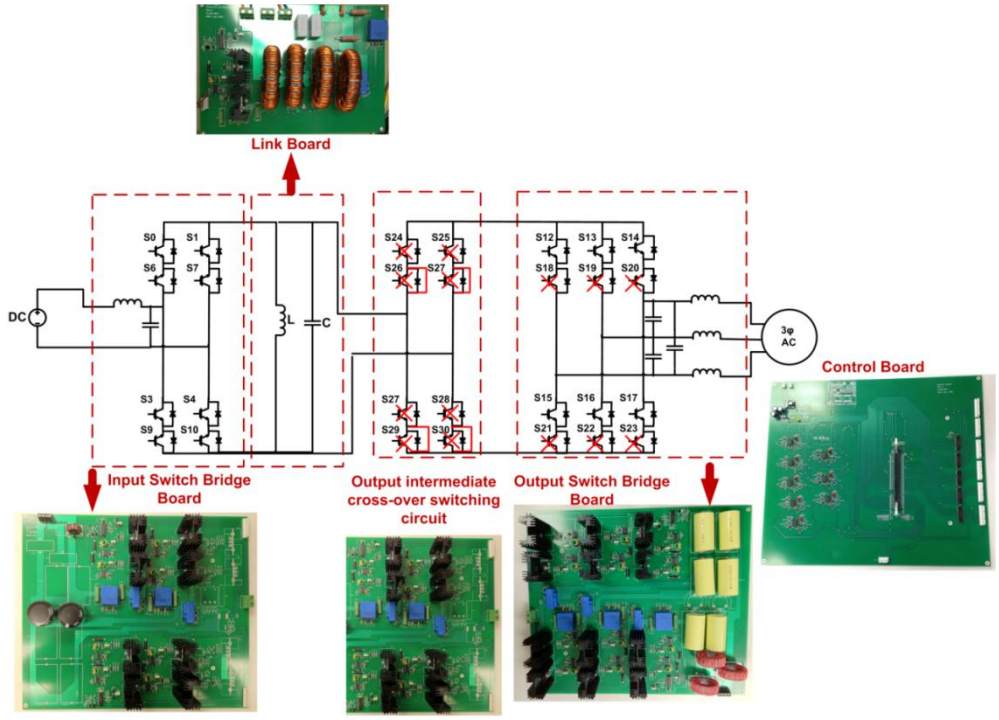


Figure 188 Different parts of the prototype for testing the dc-ac ultra-sparse parallel ac-link universal converter

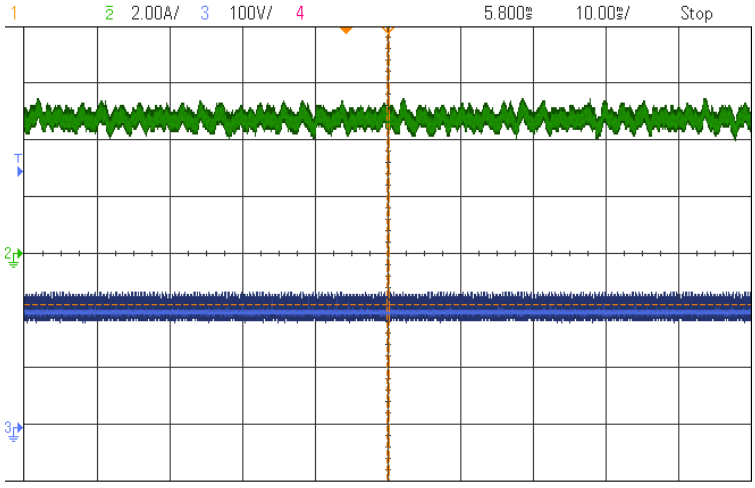


Figure 189 Dc-side current and voltage in the dc-ac ultra-sparse parallel ac-link universal converter (experiment)

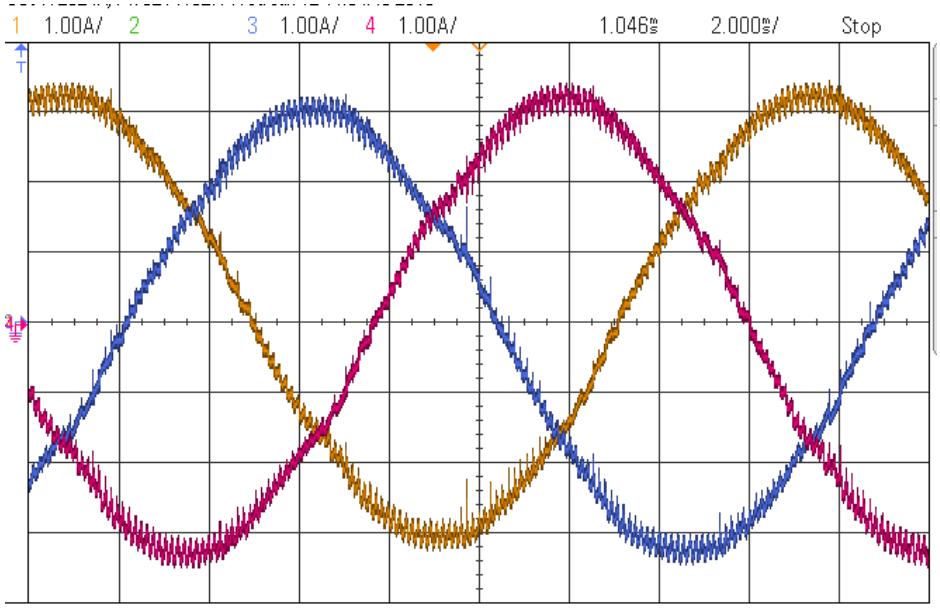


Figure 190 Ac-side currents in the dc-ac ultra-sparse parallel ac-link universal converter (experiment)

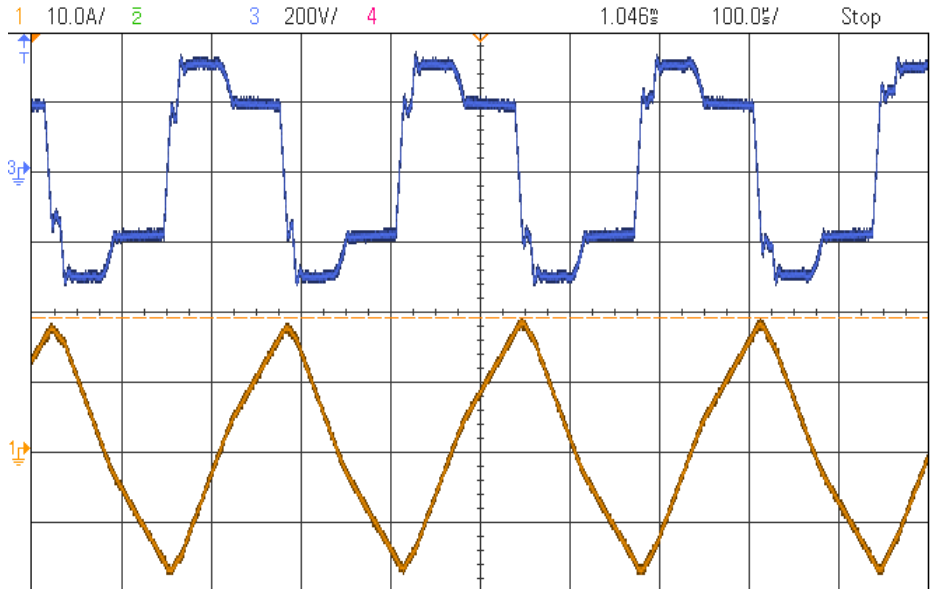


Figure 191 Link current and voltage in the dc-ac ultra-sparse parallel ac-link universal converter (experiment)

Figure 192 shows the link current, the current passing the diode bridge, and the current passing the output switch bridge.

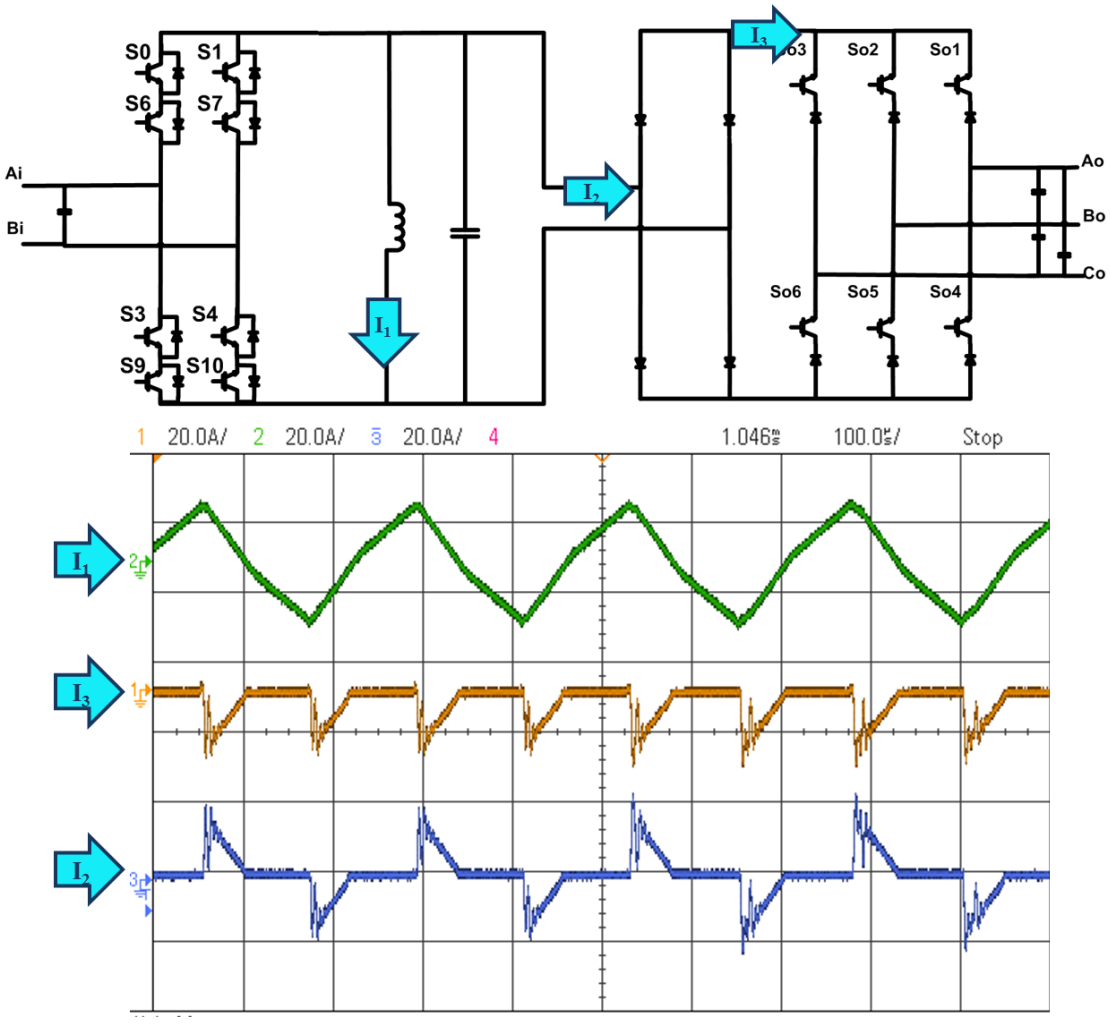


Figure 192 The link current (top), the current flowing the ac-side switch bridge (middle), and current flowing the diode bridge (bottom) in the dc-ac sparse parallel ac-link universal converter (experiment, dc-ac power flow)

4.5.3. AC-AC Configuration

In this section, simulation results corresponding to the ac-ac parallel, sparse parallel, and ultra-sparse parallel ac-link universal converters will be presented and compared. Parameters of the simulated converters are summarized in Table 17. The input of the converter is assumed to be 150V, three-phase and the load is assumed to be

three-phase RL with 0.75 power factor and 208 V line-to-line voltage. It should be noted that the phase shift between the filtered output current and the voltage in this case is 41.4˚. Using 30 μF filter capacitance, the phase shift between the unfiltered current and the voltage will be 29˚, which is within the range determined for ultra-sparse configuration in section 4.3.

TABLE 17 PARAMETERS OF THE SIMULATED AC-AC PARALLEL, SPARSE PARALLEL, AND ULTRA-SPARSE PARALLEL AC-LINK UNIVERSAL CONVERTERS

Parameter	**Value**
Power rating	1.5 kW
Input voltage	150 V
Output voltage	208 V
Link inductance (L)	443 μH
Link capacitance (C)	100 nF

Figure 193 and Figure 194 represent the filtered input and output currents in the parallel ac-link universal converter. The same waveforms for the sparse and ultra-sparse ac-link universal converters are illustrated in Figure 195–Figure 198. As seen in these figures, the current waveforms are the same for all three converters. Link current and voltage along with the current waveform passing S20 and S17 in the parallel ac-link converter are shown in Figure 199. It is clear that S20 conducts during the first half cycle of the link whereas S17 conducts during the second half cycle of the link.

In Figure 200 the link current and voltage along with the current passing switches So1 (at the output switch bridge), So7 and So9 (both located at the output intermediate cross-over switching circuit) in the sparse parallel ac-link universal converter, are depicted. As seen in this figure switch So1 conducts during both the first and second half cycles of the link. Switch So7 conducts during the first half cycle of the link and switch So9 conducts during the second half cycle of the link.

Figure 201 represents the link current, link voltage, the current passing switch So1, and the current passing diodes D7 and D9 in the ultra-sparse parallel ac-link universal converter. It is clear that diodes D7–D10 in the ultra-sparse configuration have been able to fulfill the task of the switches So7–So10 in the sparse configuration.

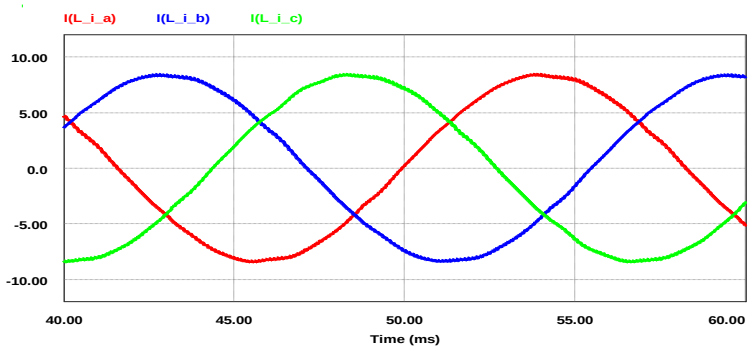


Figure 193 Filtered input currents in the ac-ac parallel ac-link universal converter

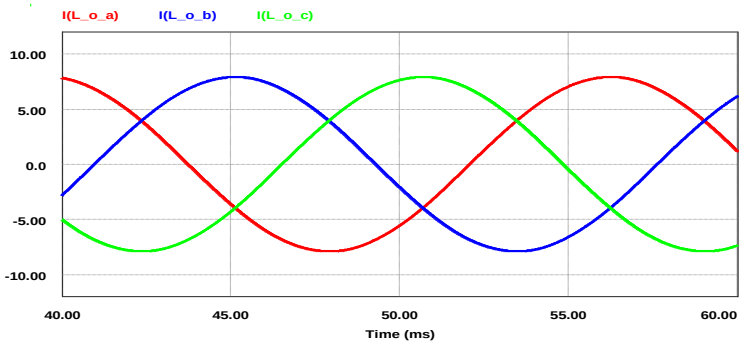


Figure 194 Filtered output currents in the ac-ac parallel ac-link universal converter

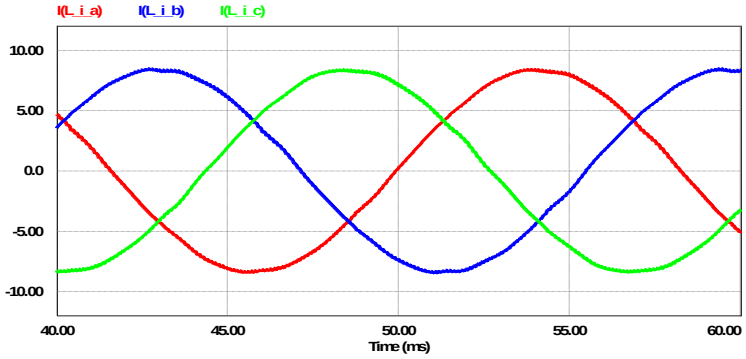


Figure 195 Filtered input currents in the ac-ac sparse parallel ac-link universal converter

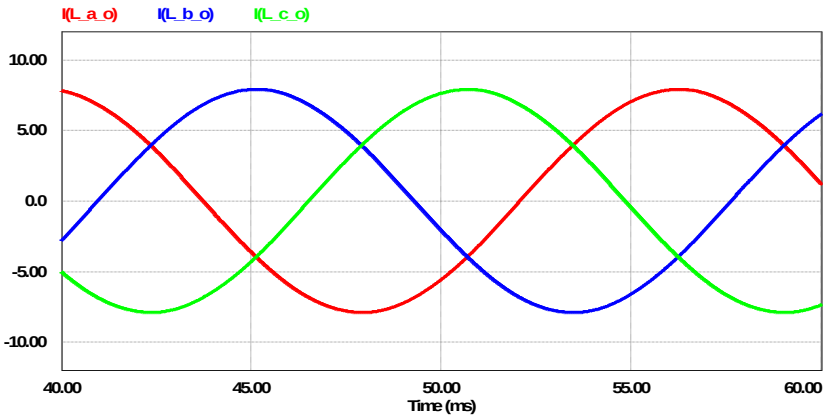


Figure 196 Filtered output currents in the ac-ac sparse parallel ac-link universal converter

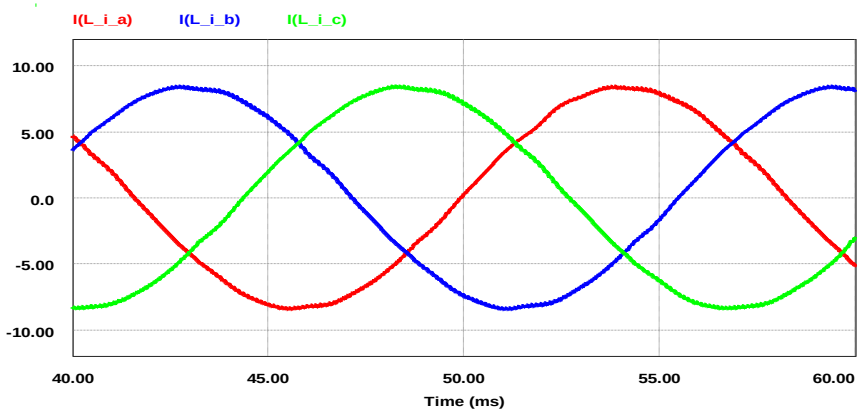


Figure 197 Filtered input currents in the ac-ac ultra-sparse parallel ac-link universal converter

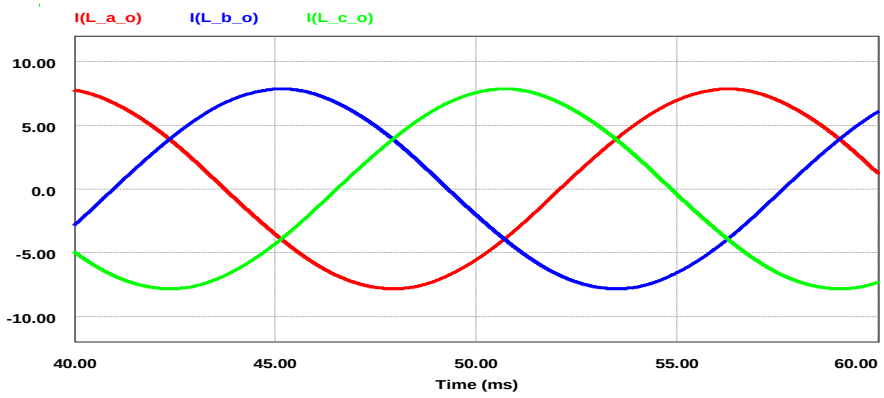


Figure 198 Filtered output currents in the ac-ac ultra-sparse parallel ac-link universal converter

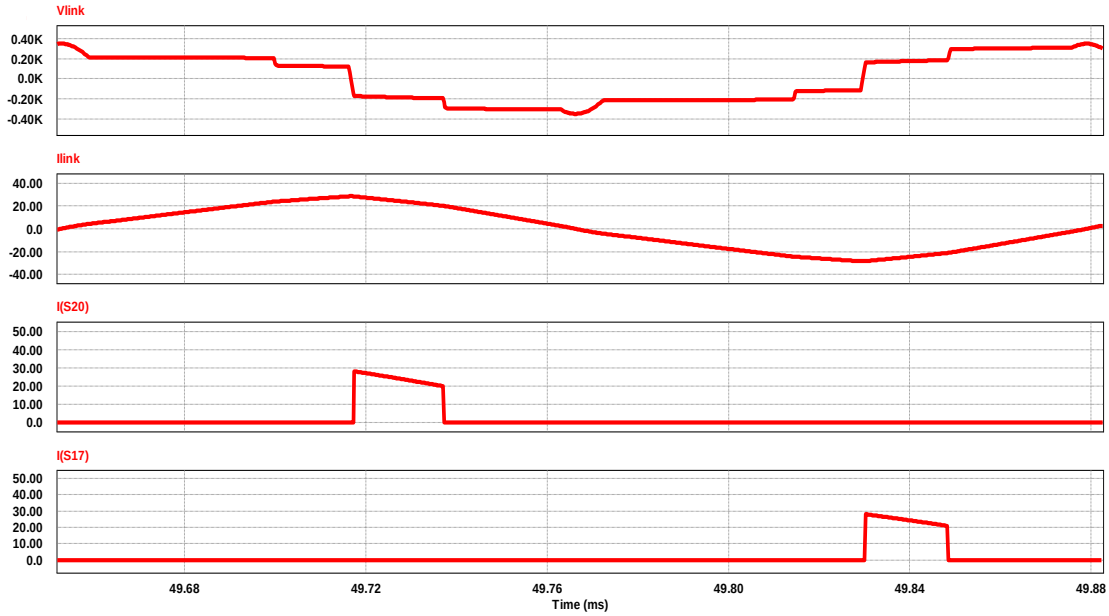


Figure 199 Link voltage, link current, current of switch S20 and current of switch S18 in the ac-ac parallel ac-link universal power converter

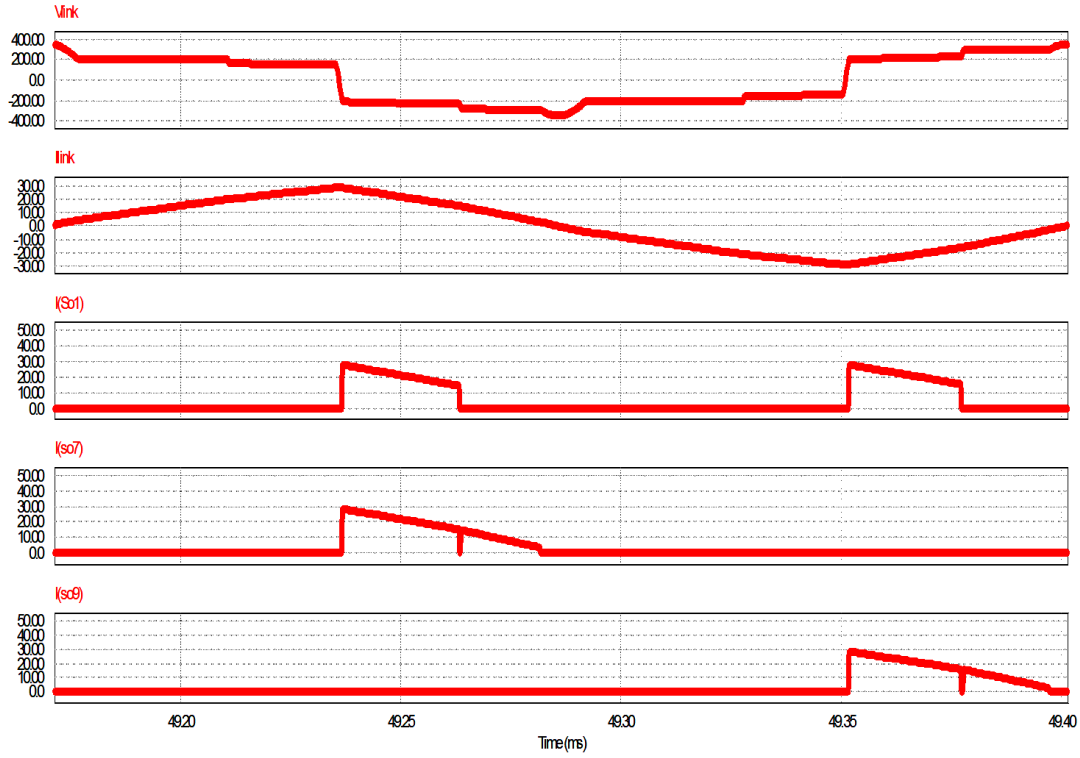


Figure 200 Link voltage, link current, current of switch So1, current of switch So7 and current of switch So9 in the ac-ac sparse parallel ac-link universal power converter

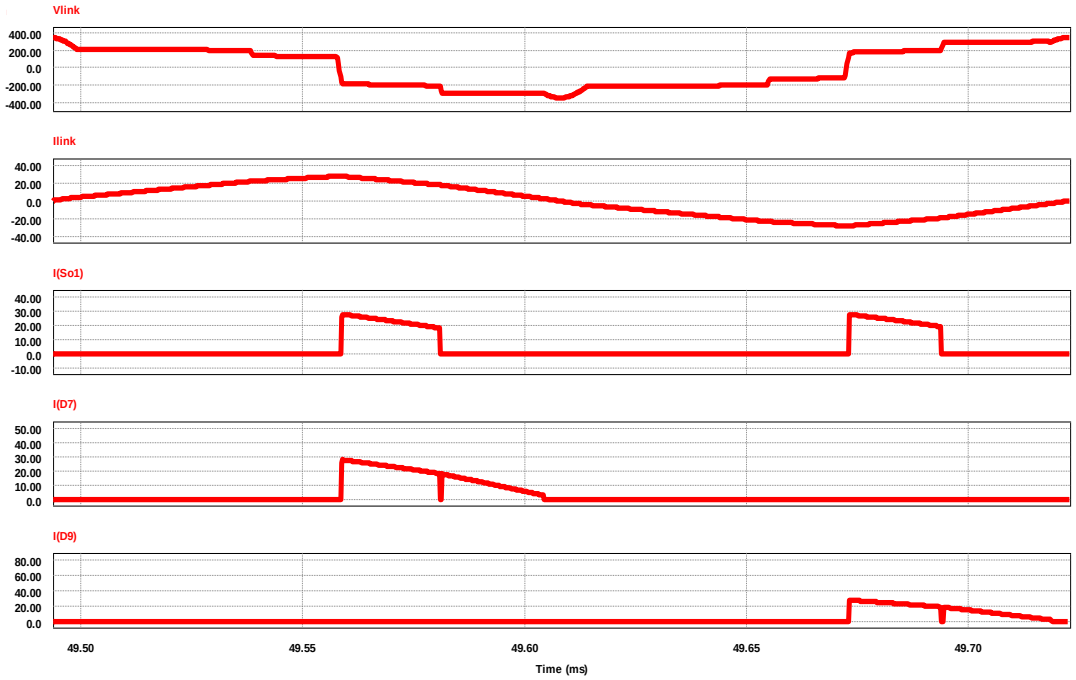


Figure 201 Link voltage, link current, current of switch So1, current of diode D7 and current of diode D9 in the ac-ac ultra-Sparse parallel ac-link universal power converter

4.6. Summary

In this section the sparse and ultra-sparse ac-link universal power converters were proposed. These converters have the advantages of conventional ac-link universal power converters but contain fewer switches. The ultra-sparse configuration is merely applicable to the applications with unidirectional flow of power.

Due to using fewer switches, the sparse and ultra-sparse configurations are more compact, less expensive, and more reliable compared to the parallel and series ac-link universal converters. The efficiency of the sparse and ultra-sparse ac-link universal

power converters are slightly lower than the original configuration; however, by using the reverse blocking IGBTs their efficiencies increase.

In this section the principles of the operation of the sparse and ultra-sparse parallel ac-link universal power converters were studied, and their efficiency and reliability were compared with those of the parallel ac-link universal converter. Moreover, the performance of these converters was evaluated through simulations and experiments.

5. SUMMARY AND FUTURE WORK

This dissertation introduced a new class of power converters, named ac-link universal power converters. These converters have several merits over the other types of converters which make them an excellent candidate for renewable energy systems.

The main advantage of the ac-link universal power converters is that their inputs and outputs may be dc, ac, single phase, or multi-phase. Therefore, they can be used in a variety of applications including renewable energy systems, variable frequency drives, and electric and hybrid electric vehicles. In these converters, the link current and voltage are both alternating, and their frequency can be high, which leads to the elimination of the dc electrolytic capacitors and the bulky low frequency transformers. Regardless of the topology, in these converters galvanic isolation may be provided by adding a single-phase high frequency transformer to the link.

The parallel ac-link universal power converter is an extension of the dc-dc buck-boost converter. Therefore, the main energy storage in this converter is the inductor, and a small capacitor is placed in parallel with the inductor to facilitate the soft switching. In this converter, the switches are all turned on at zero voltage and their turn-off is capacitance buffered, which results in negligible switching losses and minimized current and voltage stress over devices. Hence, the link frequency can be as high as permitted by the available switches and microcontroller. Clearly, by choosing a higher link frequency a smaller link inductor may be used. The link frequency and the link peak current vary by changing the power level. It was shown that in the parallel ac-link universal converter, by decreasing the power level the link peak current decreases and the link

frequency increases. The frequency of the unfiltered input and output currents are twice the link frequency. Due to the high frequency of the link, the frequency of the unfiltered currents is high, resulting in small filter elements. This converter may be used as an interface between several loads and sources and still remain a single stage converter.

The series ac-link universal power converter is an extension of the dc-dc Cuk converter. In this converter, an ac capacitor is the main energy storage element and an inductor is added to facilitate the zero-current turn-off and soft turn-on of the switches. Due to zero current turn-off of the switches in the series ac-link universal converters, the use of SCRs with natural commutation is possible as well. Similar to the parallel ac-link universal power converter, the link current and voltage in the series ac-link universal power converter are both alternating and their frequency can be as high as permitted by the switches and the microcontroller. By choosing a high link frequency, the link capacitance will be small. It was shown that in this converter, the frequency of the link decreases by decreasing the power level. Moreover, the link peak voltage is a function of the input and output filtered voltages.

The sparse ac-link universal converter, which can appear as parallel or series, has the advantages of the parallel and series ac-link universal converter; however, it contains fewer switches. The number of switches in a three-phase ac-ac configuration is reduced from 24 to 20. This results in lower cost, smaller size, and higher reliability. The efficiency of the sparse configuration is slightly lower than the original configuration. However, by using reverse blocking IGBTs its efficiency can be increased. The flow of power may be bidirectional in the sparse ac-link universal power converters. For the

applications that require unidirectional flow of power, the number of switches may be further reduced. The resultant configuration, which is named ultra-sparse parallel ac-link universal power converter, reduces the number of switches to 16 in a three-phase ac-ac configuration. The ultra-sparse parallel ac-link universal power converter is more compact, less costly, and more reliable than the parallel and sparse parallel ac-link universal power converters. The efficiency of this converter is higher than the sparse parallel configuration and lower than the parallel ac-link universal converter.

All these configurations were evaluated through simulations and experiments in this dissertation.

Suggested future works include:

- Extending the number of phases in the ac-link universal power converters to investigate the application of this converter in driving multi-phase electrical machines
- Developing the hybrid sparse parallel ac-link universal power converter for interfacing several sources/loads
- Improving the control scheme and applying new control techniques to the proposed converters
- Studying the effect of switch failure in the proposed converters and propose new methods to allow the converter to continue operation, despite the failure
- Optimizing the design by improving the efficiency and reducing the size of the converter

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