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# PARAMETER VARIATION SENSING AND ESTIMATION IN NANOSCALE FABRICS

A Thesis Presented

by

JIANFENG ZHANG

Submitted to the Graduate School of the
University of Massachusetts Amherst in partial fulfillment
of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL AND COMPUTER ENGINEERING

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Department of Electrical and Computer Engineering

# PARAMETER VARIATION SENSING AND ESTIMATION IN NANOSCALE FABRICS

A Thesis Presented

by

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Finally, I would like to thank my family for their support and encouragement.

## ABSTRACT

## PARAMETER VARIATION SENSING AND ESTIMATION IN NANOSCALE FABRICS

SEPTEMBER 2013

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Parameter variations introduced by manufacturing imprecision are becoming more influential on circuit performance. This is especially the case in emerging nanoscale fabrics due to unconventional manufacturing steps (e.g., nano-imprint) and aggressive scaling. These parameter variations can lead to performance deterioration and consequently yield loss.

Parameter variations are typically addressed pre-fabrication with circuit design targeting worst-case timing scenarios. However, this approach is pessimistic and much of performance benefits can be lost. By contrast, if parameter variations can be estimated post-manufacturing, adaptive techniques or reconfiguration could be used to provide more optimal level of tolerance. To estimate parameter variations during run-time, on-chip variation sensors are gaining in importance because of their easy implementation.

In this thesis, we propose novel on-chip variation sensors to estimate variations in physical parameters for emerging nanoscale fabrics. Based on the characteristics of systematic and random variations, two separate sensors are designed to estimate the extent of systematic variations and the statistical distribution of random variations from

measured fall and rise times in the sensors respectively. The proposed sensor designs are evaluated through HSPICE Monte Carlo simulations with known variation cases injected. Simulation results show that the estimation error of the systematic-variation sensor is less than 1.2% for all simulated cases; and for the random-variation sensor, the worst-case estimation error is 12.7% and the average estimation error is 8% for all simulations.

In addition, to address the placement of on-chip sensors, we calculate sensor area and the effective range of systematic-variation sensor. Then using a processor designed in nanoscale fabrics as a target, an example for sensor placement is introduced. Based on the sensor placement, external noises that may affect the measured fall and rise times of outputs are identified. Through careful analysis, we find that these noises do not deteriorate the accuracy of the systematic-variation sensor, but affect the accuracy of the random-variation sensor.

We believe that the proposed on-chip variation sensors in conjunction with post-fabrication compensation techniques would be able to improve system-level performance in nanoscale fabrics, which may be an efficient alternative to making worst-case assumptions on parameter variations in nanoscale designs.

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# CHAPTER 1

# INTRODUCTION AND MOTIVATION

Emerging nanoscale computing systems have been proposed as an alternative to scaled CMOS with potential performance and density benefits. These nanoscale computing systems are based on novel nanostructures, such as nanowires [1], [2], carbon nanotubes [3], graphene [4], [5], magneto electric devices [6], [7], [8], etc. Their manufacturing approaches incorporate unconventional (e.g., self-assembly, nano-imprint) and conventional (e.g., deposition, etching, and lithography) process steps. As their feature sizes shrink into deep nanoscale, the manufacturing process may cause a significant level of variations in physical parameters. For example, during ion implantation, there exists some randomness in the distribution of dopants, which can result in the fluctuation of total number of dopants in the specified region (e.g., drain, source).

Parameter variations are usually classified into systematic variations and random variations based on the characteristics of their manufacturing process. Systematic variations are typically spatial correlated, which can lead to similar characteristics of parameter variations in devices that are close to each other. In contrast to systematic variations, random variations have no spatial correlation, which means even neighboring devices may have completely different variation characteristics. Details on the types and sources of both systematic and random variations in these emerging nanoscale fabrics will be introduced later with emphasis on Nanoscale Application Specific Integrated Circuits (NASICs) fabric [9], [10], [11], [12], [13].

Their influence on circuit performance for these emerging nanoscale computing fabrics, including both systematic and random variations, has been extensively characterized

through 3-D physics based simulations using Synopsys Sentaurus tools [14]. For example, simulation results in [14] show the non-linear influence of variations in different physical parameters (e.g., channel length, gate oxide thickness, source-drain doping and underlap) on the on-current of devices. The system level performance was shown to degrade considerably as a result of parameter variations, with 67% of simulated chips operating at less than their nominal frequency [14]. As a result, these parameter variations could lead to performance deterioration such as timing errors and consequently yield loss in the integrated circuits.

Parameter variations are traditionally addressed pre-fabrication by circuit design, often targeting various worst-case variation scenarios. However, this pre-fabrication approach is pessimistic and much of the performance benefits can be lost especially for emerging nanoscale computing fabrics where the extent of variability can be high. Alternatively, if parameter variations could be estimated post-fabrication, some compensation techniques, such as redundant intermediate bitslices [15] and body biasing [16], could be used to adjust circuit timing and reduce leakage power during run-time, leading to area and performance benefits.

To estimate parameter variations post-fabrication, two popular methods exist: I-V curve measurement and sensor-based estimation. I-V curve measurement is a conventional approach to obtain characteristics for each transistor [17], [18]. However, in order to measure I-V curve, an analog voltage and current measurement equipment is required. It is a very precise approach, but not adaptive for estimating parameter variations for each chip targeting chip-by-chip performance compensation. By contrast, on-chip variation sensors can be easily implemented on a chip and can obtain variability

information at run-time since sensor outputs can be easily measured. Traditionally, ring oscillator (RO) is chosen as on-chip variation sensor for variability sensing by measuring RO frequency. However, some problems exist in RO-based on-chip variation sensor design. First of all, a large area overhead will be introduced by RO-based on-chip variation sensors. It is mainly because RO stages in these on-chip sensors are usually more than 100 to make RO frequency measurable. Secondly, RO is unsuitable for random variation sensing. Because of the averaging effect [19], RO frequency will average parameters of all stages. So it does not permit the characterization of random variations on individual devices. As a result, in order to enable accurate variation estimation in these emerging nanoscale fabrics, novel on-chip variation sensor design and the corresponding variability sensing methodology become necessary.

In this thesis, we propose novel on-chip variation sensor designs for quantifying variations in physical parameters (e.g., channel length, underlap and gate oxide thickness) in NASIC fabric. Based on the different characteristics of systematic and random variations, two separate sensor circuits are designed for estimating systematic and random variations respectively. It is necessary because: 1) spatial correlation is the foundation of systematic-variation sensing, but random variation has no spatial correlation; and 2) in order to estimate random variations accurately, the averaging effect must be avoided in the random-variation sensor design, but it does not affect the systematic-variation sensor design.

With respect to systematic variations, a new resilience sensor design is presented, which can estimate the extent of systematic variations in neighboring regions from its own variations. This correspondence is possible because: 1) spatially correlated or 'systematic'

behavior is well-known for several parameters (e.g., gate oxide [20], transistor channel and gate linewidth [21]); and 2) the uniform array-based organization of these fabrics with identical devices and no arbitrary sizing or doping implies that sensor circuits designed using the same devices and circuit/logic styles can be representative of the fabric as a whole. In this sensor design, signal fall times are used to extract the extent of physical parameter variations for different spatially correlated parameters. HSPICE Monte Carlo circuit simulations are used to evaluate this sensor design. Simulation results show that in 100% of simulated cases, the relative error between the injected and estimated extent of systematic variations in physical parameters is less than 1.2%. In addition, to address the aspect of sensor distribution across a wafer, sensor effective range is defined based on spatial correlation. In conjunction with well-characterized experimental data shown in [22], the sensor effective range is calculated with respect to different values of permissible error. Our results show that the sensor design can estimate the extent of systematic variation in the gate diameter to within 20% of its actual values inside a 3.3mm radius based on the given experimental data.

By contrast, a novel on-chip sensor design for quantifying the statistical distribution and impact of random variations in physical parameters (e.g., channel doping density, drain/source doping density) in the NASIC fabric is proposed. In this sensor, signal fall and rise times are used to extract the statistical distribution of random variations. Further, a methodology for evaluating and validating this sensor design using HSPICE Monte Carlo circuit simulations is presented. The simulation results show that the relative error between the injected and estimated standard deviation of physical parameters is 12.7% in the worst case and 8% on average scenarios with as low as 150 sensor instances used.

Finally, to introduce the application of the proposed on-chip variation sensors in real chip scenario, WISP-0 processor, which is designed on NASIC fabric with all NASIC design principles and optimizations applied, is used as a target to show examples of sensor placement. The principles of sensor placement are discussed and the sensor area that may be treated as the area overhead is calculated with the projected technology parameters. External noises that may affect the estimation accuracy of the proposed sensors are identified. Through careful analysis, we find that these external noises only affect the estimation accuracy of the random-variation sensor, but their effect can be reduced by sensor placement.

The proposed sensor designs for both systematic and random variations are also directly applicable to the Nanoscale 3-D Application Specific Integrated Circuits ($N^3$ASIC) [23], [24], and the variability sensing methodology can be extended to other regular nanoscale computing fabrics in general.

The rest of this thesis is organized as follows: Chapter 2 briefly presents the NASIC fabric with emphasis on physical parameter variations; Chapter 3 illustrates the new systematic-variation sensor design and describes the Monte Carlo simulation methodology for evaluating the sensor design; Chapter 4 discusses the random-variation sensor design and its evaluation; Chapter 5 introduces the principles of sensor placement and analyzes the impact of external noises on the estimation accuracy; and Chapter 6 concludes the thesis.

# CHAPTER 2

# NASIC FABRIC OVERVIEW

Nanoscale Application Specific Integrated Circuits (NASICs) is a nanoscale computational fabric that relies on 2-D grids of semiconductor nanowires with crossed nanowire field-effect transistors (xnwFETs) at certain crosspoints (Figure. 1). In this fabric, in order to ease manufacturing requirements, a regular grid layout is used where all transistors on the crosspoints are identical with no arbitrary doping or sizing requirements. This semiconductor nanowire grid includes some peripheral micro wires to carry VDD, GND and control signals. Dynamic circuit styles without the requirement of complementary devices or arbitrary placement/sizing are used for logic implementation. Several extensions exist to NASICs and there are other circuit styles also proposed but the approach for variability estimation applies across all of them.

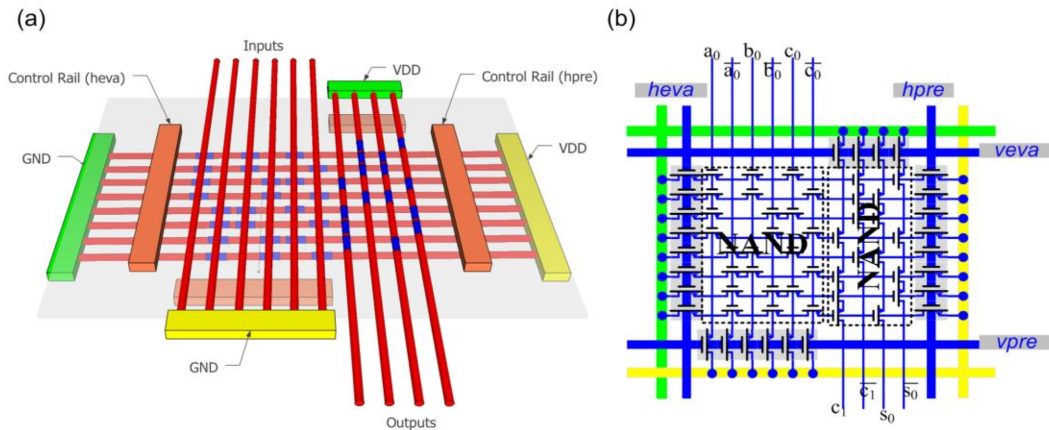


Figure. 1 Nanoscale Application Specific Integrated Circuits (NASIC) with regular semiconductor nanowire grids, xnwFET devices and peripheral microscale control a) 3-D fabric view b) circuit schematic

The xnwFET structure and dynamic circuit style are shown in Figure. 2 and Figure. 3. Figure. 3 shows an N-input dynamic NAND gate with xnwFETs as active devices. The pre and eva signals in this NAND gate are used to precharge and discharge the output (out)

respectively depending on inputs ($in_1$, $in_2$, …, $in_N$). Multiple stages of logic can be achieved by cascading multiple such dynamic NAND gates. The proposed sensors follow the same dynamic circuit style.

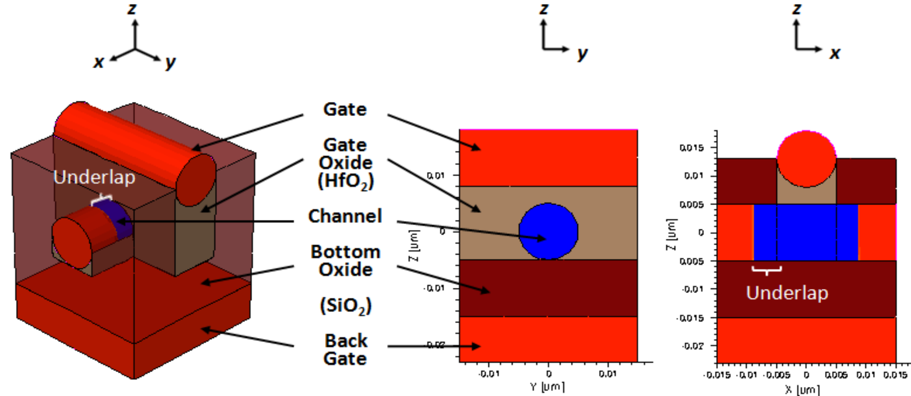


Figure. 2 n-type xnwFET device structure with orthogonal gate and channel nanowires

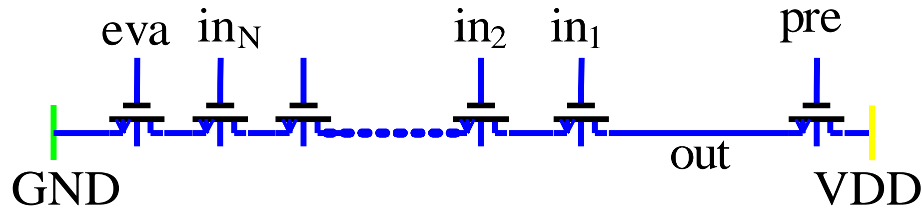


Figure. 3 N-input NASIC dynamic NAND gate

The assumed xnwFET device operating principle is similar to that of inversion mode devices; the current through the channel nanowire is modulated by the potential applied on the orthogonal gate. In this xnwFET structure, key physical parameters are identified, which include channel diameter ($C_{diam}$), gate diameter ($G_{diam}$), gate oxide thickness ($G_{ox}$), bottom oxide thickness ($B_{ox}$), channel doping density (CD), source-drain doping density (SDD) and underlap length (U). Based on the characteristics of their manufacturing process, they are classified into systematic variations and random variations.

In NASIC fabric, physical parameters varying systematically include channel diameter ($C_{diam}$), gate diameter ($G_{diam}$), gate oxide thickness ($G_{ox}$) and bottom oxide thickness ($B_{ox}$).

Diameters of nanowires in NASIC fabric are strongly correlated to the size of the seed catalysts used in Vapor-Liquid-Solid (VLS) growth [25], [26]. Nanoimprint lithography is usually used to pattern substrates with these seed catalysts. During this process, a variety of sources, such as mold errors and lens aberrations, may cause variations in the size of these seed catalysts. This implies that at the circuit level, the channel and gate diameters of all transistors along a same nanowire will be systematically affected. On the other hand, Atomic-Layer Deposition (ALD) is a process step commonly used for creating $HfO_2$ gate and bottom dielectric that also exhibits strong spatial correlation [20].

By contrast, channel doping density, drain-source doping density and underlap length are the main types of random variations in NASIC fabric. As the feature sizes continue to shrink, the total number of dopant atoms inside the channel, source and drain regions decreases drastically. Hence, there exists some randomness in the distribution of dopant atoms in these regions during ion implantation. On the other hand, source and drain junction underlap regions are formed by spacer technology [27], which is similar to what is used to form highly doped drain and source (HDD) in CMOS devices. The formation of the drain and source underlap is shown in Figure. 4. An initial device structure is shown in Figure. 4a, and then the spacer material is conformally deposited as shown in Figure. 4b. During the anisotropic etching step, the spacer is etched incompletely owing to higher

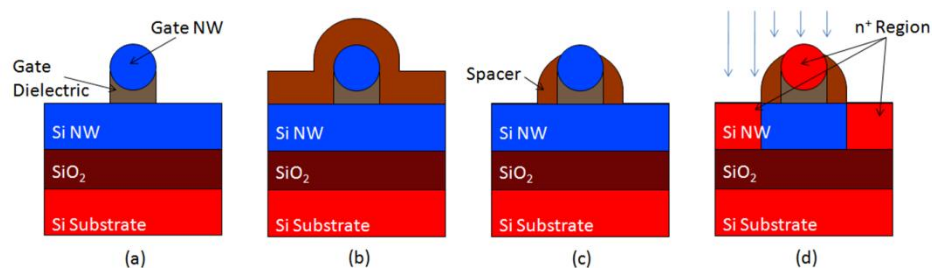


Figure. 4 Front view of the xnwFET during the formation of the source and drain underlap

thickness above the underlap region in Figure. 4c. During the subsequent ion implantation, some dopant atoms may be implanted into the underlap region due to the thinner spacer above the boundary of underlap, leading to random variation in underlap length.

Based on the discussion above, the variations in these physical parameters come from different manufacturing process. So we assume that they are independent to each other in this thesis.

# CHAPTER 3

# ON-CHIP VARIATION SENSOR DESIGN FOR SYSTEMATIC VARIATION ESTIMATION

## 3.1 Introduction

A key motivation for on-chip variation sensing is the capability to adjust circuit behavior post-manufacturing without pessimistic over-compensation at design time. While designing for the worst case could guarantee that there are no timing faults in the design, this approach would likely eliminate benefits of nanoscale computing fabrics. For example, previous circuit simulations of parameter variations in NASIC processor designs [14] have shown that while worst-case delays can be 2X – 2.5X of the nominal, this occurs in less than 1% of simulated cases. Also, the distribution of delays is such that 85% of samples fall within 30% deviation from the nominal frequency, which implies that most fabricated chips would not need worst-case resilience.

If the extent of variations in fabricated chips can be estimated, body-biasing (to lower the threshold voltage), or reconfiguration schemes can be used to meet circuit timing requirements and retain performance benefits. Variation sensors can also be used for process feedback (i.e., to determine, based on device parameters, which process steps need to be more carefully controlled).

In this chapter, we first present a new on-chip sensor design for the NASIC fabric, which can be used to estimate the extent of systematic variations in physical parameters based on the measurement of fall time (1-to-0 transitions) in dynamic NAND gate, and then describe a methodology for evaluating the accuracy of the sensor design based on HSPICE Monte Carlo circuit simulations injecting known variation cases into the sensor

circuits. The simulation results for the sensor accuracy are shown subsequently. Finally, based on the spatial correlation of systematic variations, an experimental model for systematic variations in gate diameter is used to derive sensor effective range for different permissible errors.

### 3.2 Notations

All the notations that will be used in this chapter are summarized in Table. 1.

Table. 1 Summary of Notations

| Notation | Description |
|---|---|
| N | Number of inputs for the NAND gate |
| $V_{DS}$ | Drain-source voltage |
| $t_{f,out}$ | Fall time of the output |
| K | Number of time constants to discharge output |
| $C_{Load}$ | Output loading capacitance |
| $R_i$ | xnwFET equivalent resistance |
| $h(x_i)$ | Polynomial function of individual parameter $x_i$ |
| M | Number of systematic parameters |
| P | Vector representing the extent of variations in individual parameters |
| S | Sensitivity matrix of systematic parameters |
| T | Vector containing the difference in fall times of one functional unit |
| $C_{diam}$ | Channel diameter |
| $G_{diam}$ | Gate diameter |
| $G_{ox}$ | Gate oxide thickness |
| $B_{ox}$ | Bottom oxide thickness |
| $x^j_i$ | Injected value of parameter $x_i$ |
| $x^e_i$ | Estimated value of parameter $x_i$ |
| EE | Estimation error of one parameter |
| MEE | Maximum estimation error across all parameters |

| | for each Monte Carlo case |
|---|---|
| D | Sensor effective range |
| $e_{max}$ | Maximum allowed imprecision |

### 3.3 On-Chip Systematic-Variation Sensor Design

Figure. 5 shows the new sensor circuit, which uses the same circuit styles as logic portions of the design. It consists of a pair of dynamic NAND gates with fan-in N and N+1. In principle, if the switching characteristics of a single device can be isolated, then information on the extent of variation in the device can be extracted using physics-based device models.

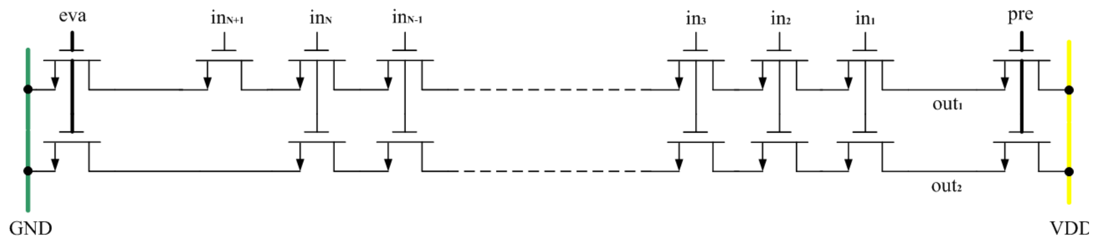


Figure. 5 Sensor dynamic circuit pair using N, N+1 fan-in NAND gates

The sensor operates as follows: outputs are initially precharged by asserting the pre signal. During this time the input $in_1$ is switched off ensuring that intermediate capacitances are not charged. All other inputs are asserted. Subsequently, $in_1$ and eva signals are asserted, leading to 1-to-0 transitions on both output nodes. The difference in the fall times of the two output signals in this circuit pair can be directly attributed to the behavior of the single ‘additional’ xnwFET if transient effects are near identical. This is made possible through careful sensor design. Firstly, the output load capacitance is made much larger than the device parasitics related capacitances, eliminating their effect. Secondly, N must be large enough such that the net $V_{DS}$ drop across the N+1 FETs in the second dynamic NAND gate is very small. This N will be determined by HSPICE

simulations of sensor circuits employing accurate physics-based device models.

Ignoring transient effects, fall times are given by Eq. (1) and (2),

$$t_{f,out_1} = K*(R_1^{'} + R_2^{'} + \cdots\cdots + R_N^{'} + R_{N+1}^{'} + R_{eva}^{'})*C_{Load} \tag{1}$$

$$t_{f,out_2} = K*(R_1 + R_2 + \cdots\cdots + R_N + R_{eva})*C_{Load} \tag{2}$$

where K is the number of time constants to discharge the output and $C_{Load}$ is the output loading capacitance. $R_1 \ldots R_{N+1}$ are xnwFET equivalent resistances. Subtracting Eq. (1) – (2), we get Eq. (3).

$$t_{f,out_1} - t_{f,out_2} = K*R_{N+1}^{'}*C_{Load} \tag{3}$$

Next, $R^{'}_{N+1}$ can be expressed as a function of the individual variation parameters. Assuming independent variations in M different parameters (since each parameter is dependent on a separate process step as discussed in chapter 2), the resistance function can be decomposed into polynomial functions $h_i(x_i)$ of the individual parameter $x_i$, as shown in Eq. (4).

$$\frac{t_{f,out_1} - t_{f,out_2}}{K*C_{Load}} = R_{N+1}^{'} = h_1(x_1) + h_2(x_2) + \cdots + h_M(x_M) \tag{4}$$

The above equation establishes a single relationship between measurable fall times and the extent of physical variations to be estimated. Considering different values of N and N+1, a linear system of equations can be established and solved for the individual parameters. For example, if there are 4 systematic parameters being varied (M=4), then four different sensor pairs are used to establish 4 fall-time difference equations. Figure. 6 shows such a sensor, with 8 dynamic NAND gates, and (N, N+1) pairs will be determined by circuit simulations.

For simplicity, the next set of equations consider first-order (linear) relationships for

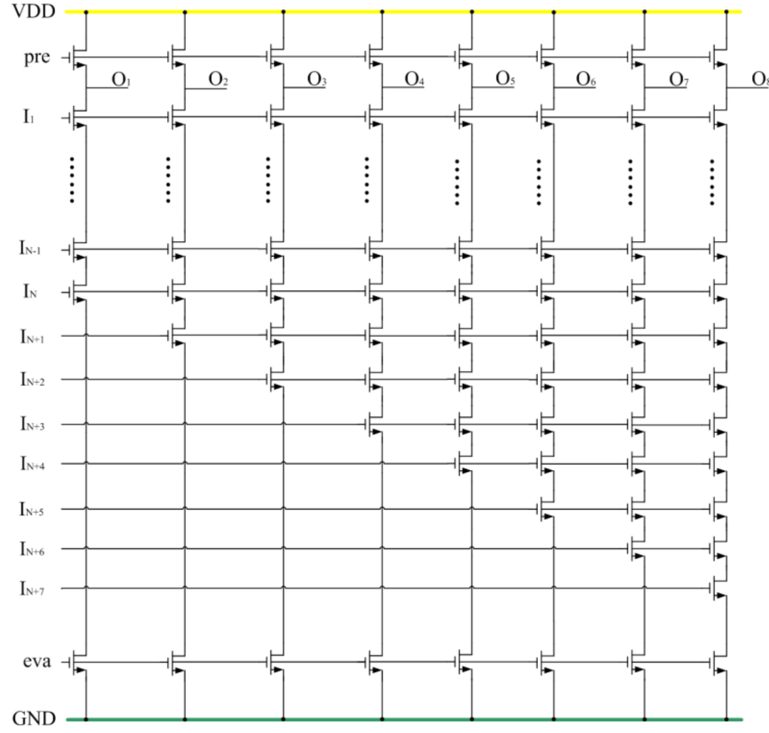


Figure. 6 4-pair sensor circuit to determine variation in four systematic variation parameters

$h_i(x_i)$ polynomials. Results for 1st, 2nd, 3rd and 4th order polynomials will be discussed in the following sections. Eq. (5) shows the matrix representation for the linear system of equations that needs to be solved.

$$\vec{P} = \vec{S}^{-1} * \vec{T} \tag{5}$$

$$\vec{P} = \begin{pmatrix} x_1 \\ x_2 \\ \vdots \\ \vdots \\ x_{M-1} \\ x_M \end{pmatrix} \quad \vec{S} = \begin{pmatrix} k_{1,1} & k_{1,2} & \cdots & \cdots & k_{1,M-1} & k_{1,M} \\ k_{2,1} & k_{2,2} & \cdots & \cdots & k_{2,M-1} & k_{2,M} \\ \vdots & \vdots & \ddots & & \vdots & \vdots \\ \vdots & \vdots & & \ddots & \vdots & \vdots \\ k_{M-1,1} & k_{M-1,2} & \cdots & \cdots & k_{M-1,M-1} & k_{M-1,M} \\ k_{M,1} & k_{M,2} & \cdots & \cdots & k_{M,M-1} & k_{M,M} \end{pmatrix} \quad \vec{T} = \begin{pmatrix} g(\Delta t_{f,1}) \\ g(\Delta t_{f,2}) \\ \vdots \\ \vdots \\ g(\Delta t_{f,M-1}) \\ g(\Delta t_{f,M}) \end{pmatrix}$$

P is the vector representing the extent of variation in individual parameters that needs to be determined, S lists the sensitivity coefficients of each parameter, and T contains measured differences in fall times. For M systematic variation parameters, M pairs of

sensor circuits are needed to establish M different linear equations. By solving this system of equations, the extent of variation in individual parameters is estimated. This process is abstracted in Figure. 7.

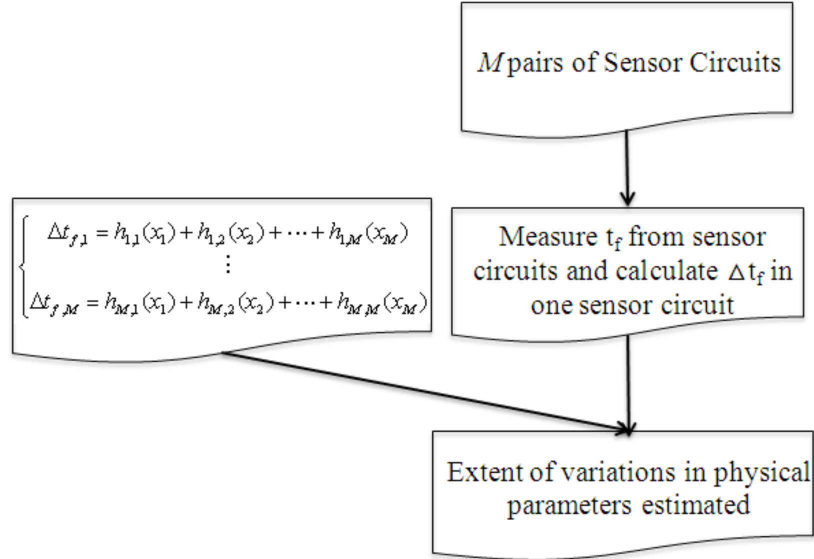


Figure. 7 Flowchart of systematic-variation estimation

### 3.4 Methodology for Evaluating the Sensor Design

In this section, we describe a methodology for evaluating the accuracy of the sensor design based on HSPICE Monte Carlo circuit simulations injecting known variation cases into the sensor circuit.

xnwFET structures are characterized through variation-aware 3-D physics based simulations using Synopsys Sentaurus [14]. Individual parameters considered include channel and gate diameters ($C_{diam}$, $G_{diam}$), and gate-oxide and bottom-oxide thicknesses ($G_{ox}$, $B_{ox}$). Device I-V and C-V characteristics were obtained for up to $3\sigma=\pm30\%$ variation in all parameters. The device characterization data was then used to build SPICE-compatible behavioral models using regression analysis. These behavioral models represent the xnwFET resistance as a function of gate-source voltage, drain-source

voltage and extent of variation in physical parameters.

Using these device behavior models, an initial circuit simulation step is used to populate the sensitivity matrix S. Circuit simulations are carried out for the sensor shown in Figure. 6 with parameters varied one at a time. Sensitivity coefficients for all parameters are calculated from the measured fall times by curve fitting.

To test if the sensor design provides accurate estimates of physical parameter variations, a Monte Carlo based simulation framework (Figure. 8) is used. Fan-in N will be varied to evaluate its effect on the estimation accuracy. Then for each N, HSPICE circuit simulations are carried out with known variation cases injected into the sensor. Based on the measured fall times, the extent of variation in physical parameters is estimated using the theoretical framework described in the previous section. The relative error in estimated vs. injected variation in physical parameters can then be determined. This process will be iterated 100 times to achieve sufficient estimates.

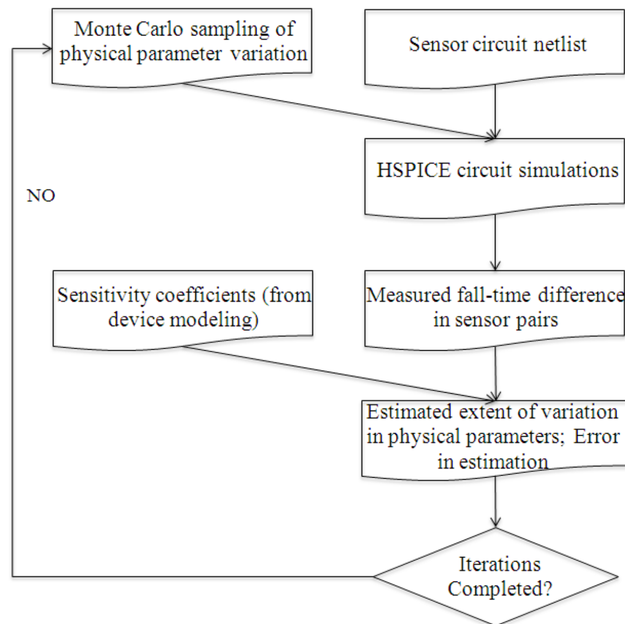


Figure. 8 Methodology for evaluating sensor designs based on HSPICE Monte Carlo circuit simulations

### 3.5 Results

3.5.1 Sensor Accuracy

Circuit simulations were carried out to determine the accuracy of the sensor design in estimating the extent of variation in physical parameters. The metric used is the Estimation Error (EE) for parameter $x_i$, defined as:

$$EE = 100 * \left|(x_i^e - x_i^j)\right| / x_i^j \tag{6}$$

here $x^j_i$ is the injected value of parameter $x_i$, $x^e_i$ is the value of the parameter $x_i$ estimated by the sensor. The Maximum Estimation Error (MEE) across all M parameters for each Monte Carlo case is then defined as:

$$MEE = MAX(EE_1, EE_2, \cdots, EE_M) \tag{7}$$

An example for the calculation of MEE is shown in Table. 2. In Case 1, the $C_{diam}$ parameter has the maximum estimation error of 0.212%. In Case 2, the maximum estimation error is for the $B_{ox}$ parameter (0.695%).

Table. 2 Examples of Variation Cases and *MEE* Calculation

| ($C_{diam}$, $G_{ox}$, $B_{ox}$, $G_{diam}$) | Estimated Variation | Injected Variation (normalized) | *MEE* |
|---|---|---|---|
| Case 1 | (-0.10, 0.06, 0.09, 0.08) | (-0.11, 0.06, 0.09, 0.09) | 0.212%($C_{diam}$) |
| Case 2 | (0.11, -0.16, -0.07, 0.03) | (0.10, -0.17, -0.06, 0.03) | 0.695%($B_{ox}$) |

To evaluate the impact of fan-in N on the estimation accuracy, N is varied in the HSPICE simulations, and for each N, in order to eliminate the impact of other factors on the estimation accuracy, 4th-order polynomial functions (i.e., sufficient to model relationships between fall times and systematic parameters and proved later) are used to model Eq. (4). Based on the evaluation methodology, 100 variation cases are injected into

the sensor circuit and then estimated. The average estimation error among these 100 variation cases for each N is calculated. The relationship between fan-in N and the estimation accuracy is shown in Figure. 9. From this figure, we can see that both the maximum estimation error and the average estimation error decrease gradually as the number of fan-in (N) increases. When N increases to 49, the average estimation error decreases to 1.07% and the maximum estimation error becomes 1.2% across these 100 different variation cases.

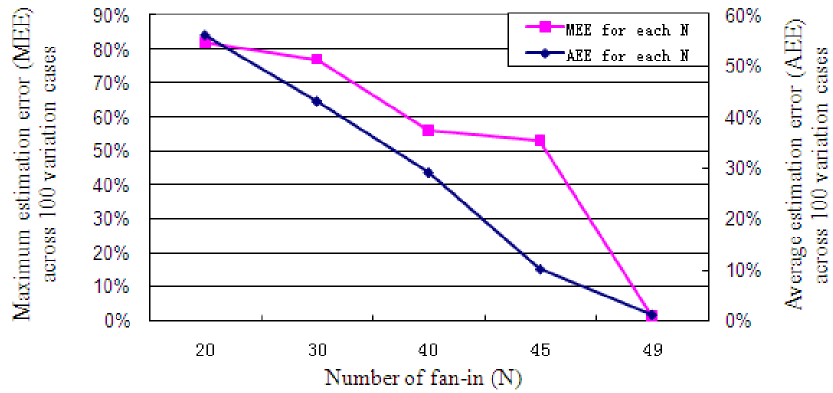


Figure. 9 Relationship between fan-in (N) and the estimation error

When fan-in N is 49, Figure. 10 shows the cumulative distribution function (CDF) for the MEE across 100 Monte Carlo simulations. The graphs consider first, second, third and fourth-order polynomial relationships between individual parameters and the measured fall times. From these results, third-order polynomials are accurate enough to model the relationships between individual parameters and the measured fall times, with less than 1% MEE for 90% of simulations, and less than 1.2% MEE for all cases considered. Even with linear approximations, the MEE is within 1.4% for 100% of samples. This implies that sensor design and methodology provides an accurate estimation of extent of variation in individual parameters. An important caveat is the requirement for populating the sensitivity matrix from accurate models based on extensive experimental

characterizations.

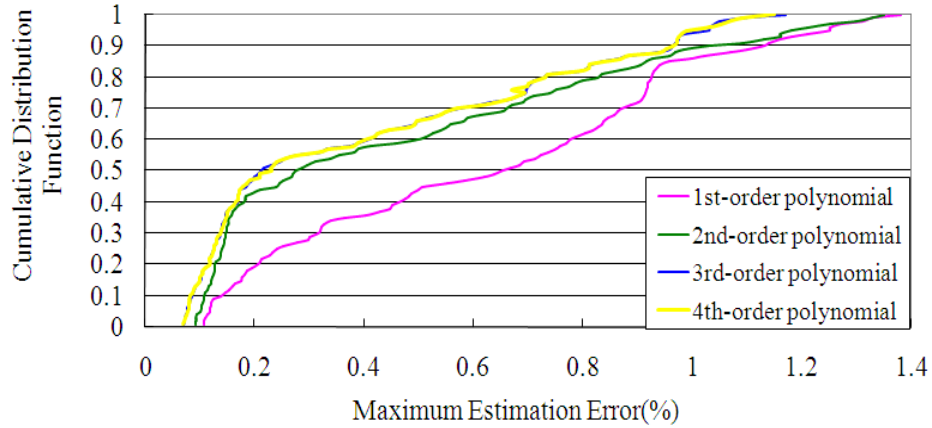


Figure. 10 CDF function of Maximum Estimated Error across 100 Monte Carlo Simulations

3.5.2 Sensor Effective Range

The problem of sensor effective range seeks to address the placement of sensors on a wafer, chip or small region given a model for trends in systematic variation across this region. For example, initial wafer lots could have a high density of sensors and as processes become more tightly controlled and extent/trends in variation better quantified, it may be possible to achieve a more optimal placement of sensors.

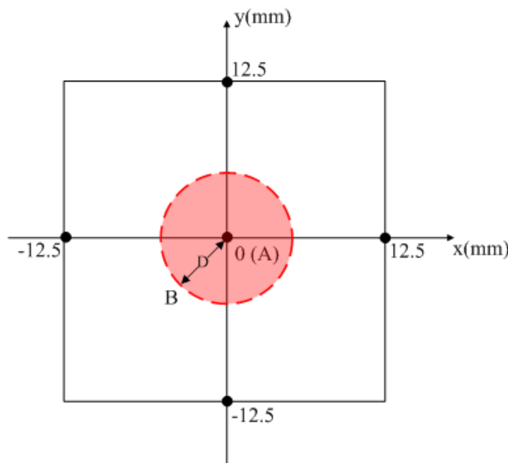


Figure. 11 Example of sensor effective range calculation within the effective field (25mm*25mm) of systematic-variation model

Consider two locations A and B in a region separated by a distance D (Figure. 11). A sensor placed at A is able to determine the extent of systematic variation at position A to within MEE (i.e., the sensor accuracy). Now, considering a suitable model for the distribution of systematic variation in this region, we wish to estimate the error in the sensor estimation with respect to the actual extent of systematic variation at location B. Conversely, the sensor range D for which the sensor accuracy is below a pre-defined permissible estimation error can be estimated. This is demonstrated below.

Considering error in estimation at point A,

$$\left|(x_A^e - x_A^a)\right| / x_A^a \le e_A \tag{8}$$

where for simplicity the metric MEE has been replaced by estimation error at point A, '$e_A$'. $x^e_A$ represents the sensor estimation value; $x^a_A$ represents the actual variation at point A. Two cases are possible depending on whether the sensor overestimates or underestimates the value of $x^a_A$,

$$x_A^a \le x_A^e / (1 - e_A) \tag{9}$$

or

$$x_A^a \ge x_A^e / (1 + e_A) \tag{10}$$

Consider an experimental model for systematic variations in gate diameter [22] that describes the distribution of systematic variations across a region,

$$\Delta G_{diam} = f(x, y) = 0.027 * y^2 - 0.093 * x - 0.079 * y + 0.008 * x * y + 4.043 \tag{11}$$

In this model, the systematic variation in gate diameter ($\Delta G_{diam}$) is modeled as a function of its coordinates (x, y) in a region (25mm*25mm). By employing this model, the systematic variation in gate diameter at every point in this region can be calculated.

Now, based on the two cases outlined above, and given a maximum allowed

imprecision $e_{max}$ at point B,

$$x_B^a = x_A^e / (1 - e_{\max}) \tag{12}$$

or

$$x_B^a = x_A^e / (1 + e_{\max}) \tag{13}$$

Solving the inequalities (9) – (13) for the two cases, we get many possible positions for point B that match our equations. Then the distances between point A and these possible points for point B can be calculated. Since the information on whether the sensor overestimated or underestimated the actual value of the parameter is unknown, the smallest of these D values needs to be selected. With respect to different values of permissible errors ($e_{max}$), the calculated sensor effective range (D) is shown in Table. 3.

Table. 3 Sensor Range vs. Permissible Estimation Error ($e_{max}$)

| $e_{max}$ | Sensor Range ($D$), in mm |
|---|---|
| 2% | 0.18 |
| 4% | 0.6 |
| 6% | 1 |
| 10% | 1.7 |
| 15% | 2.5 |
| 20% | 3.3 |

These results show that for an estimation error between 2% - 20%, the sensor range varies from 0.18mm to 3.3mm. As expected, sensor effective range increases if more imprecision can be tolerated. Similarly, the model for the distribution of systematic variations in each parameter can be established and the sensor effective range would then be determined by employing these models.

A key challenge in determining sensor distribution is that the distance D depends on the estimated parameter value and the variation distribution model, which may only be

available post-manufacturing. In nanoscale computing fabrics supporting reconfiguration, it may be possible to progressively design sensors based on estimated values, since the sensor logic and circuit style are identical to other functional blocks in the design. Otherwise, estimations based on previous experimental characterizations need to be used to determine sensor spacing pre-manufacturing.

### 3.6 Summary

In this chapter, a new on-chip variation sensor for the NASIC fabric was shown. A methodology for extracting the extent of systematic variation in physical parameters from the measured sensor fall times was presented. Using physics-based device models and HSPICE Monte Carlo simulations, sensor accuracy was quantified. Results show less than 1.2% error in estimation of physical parameters for 100% of the samples considered. Sensor effective range was calculated by employing an experimental model for systematic variations in gate diameter. With respect to different values of permissible estimation error, the sensor range was shown to be up to 3.3mm considering a permissible estimation error of 20% in gate diameter.

# CHAPTER 4

# ON-CHIP VARIATION SENSOR DESIGN FOR RANDOM VARIATION ESTIMATION

## 4.1 Introduction

Conventional variation estimation methods [28], [29] assume that large circuits are not affected by random variations because of an averaging effect; i.e., the influence of random variations is assumed to be nullified if the number of transistors in the critical path is large [30]. However, at nanoscale the impact of random variations cannot be neglected, since the influence is non-linear on circuit performance. For example, in [14] it was shown that there exists non-linear relationship between the on-current of devices and random variations in certain parameters (e.g., channel doping, source-drain doping and underlap). The system level performance was shown to degrade considerably as a result of random variations, with 67% of simulated chips operating at less than their nominal frequency [14]. Therefore, we believe that in order to estimate parameter variations accurately, random variations should be explicitly taken into consideration.

In this chapter, we discuss a new on-chip sensor design in the context of the NASIC fabric. The sensor can be used to estimate the statistical distribution of random variation in physical parameters based on the measured fall time (1-to-0 transitions) and rise time (0-to-1 transitions) from the sensor circuit. Further, a methodology for evaluating this sensor design using HSPICE Monte Carlo simulation is presented. The simulation results obtained from 150 sensor instances show that the relative error between the injected and estimated standard deviation of physical parameters is 12.7% in the worst-case and 8% on average scenarios.

## 4.2 Notations

All the notations that will be used in the following sections are summarized in Table. 4.

Table. 4 Summary of Notations

| | Notation | Distribution | |
|---|---|---|---|
| | | Mean ($\mu$) | Standard Deviation ($\sigma$) |
| Rise Time | $t_r$ | $\mu_{tr}$ | $\sigma_{tr}$ |
| Fall Time | $t_f$ | $\mu_{tf}$ | $\sigma_{tf}$ |
| Channel Doping | $CD$ | _ | $\sigma_{CD}$ |
| Source/drain Doping | $SDD$ | _ | $\sigma_{SDD}$ |
| Underlap | $U$ | _ | $\sigma_U$ |
| Complete Sensor Set | $n$ | $\mu_C$ | $\sigma_C$ |
| Current Sensor Set | $m$ | _ | _ |
| Log-likelihood Function | $L$ | _ | _ |
| Estimation Error | $EE$ | _ | _ |
| Average Estimation Error | $AEE$ | _ | _ |

## 4.3 On-Chip Random-Variation Sensor Design

Figure. 12a shows the new sensor circuit with only two xnwFETs. Two control signals pre and eva are used. When pre signal is '1' and eva signal is '0', the output is charged to '1' at first, and then discharged to '0' by inversing pre and eva signals. A load capacitance is connected to the output, designed to be much larger than device parasitics related capacitances. There are two reasons for using a large load capacitance: 1) this load capacitance can amplify fall and rise times of the output, making them easier to measure; 2) it can also eliminate the effect of device parasitic capacitances and thus simplify the complexity of theoretical analysis, as shown in subsequent sections. As a result, deviations of fall and rise times in the output can be attributed to variations in eva and pre xnwFETs respectively. To determine the distribution of random variations in physical

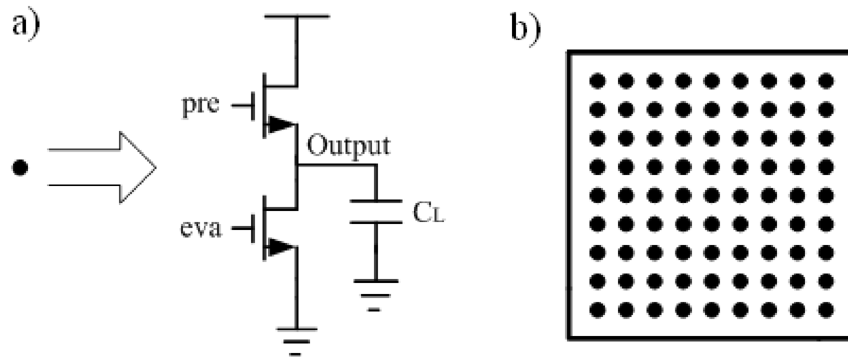


Figure. 12 a) Random-variation sensor; b) Sensor set

parameters, by statistical methods, a large number of such sensors are used, defined as the sensor set (as shown in Figure. 12b).

Using this variation sensor and the sensor set, a variability sensing methodology is developed, which can estimate the distribution of random variations in physical parameters based on the measured fall and rise times of outputs from the sensor set.

4.3.1 MLE-based Variability Sensing Methodology

A general framework of Maximum Likelihood Estimation (MLE) based variability sensing methodology is shown in Figure. 13. A sensor set containing n distributed sensors can be used for variation sensing. We use MLE to calculate the mean and standard deviation of measured parameters. Variations in physical parameters will result in fluctuations of rise ($t_r$) and fall ($t_f$) times in each sensor. A set of $t_r$ and $t_f$ can be measured from the sensor set – marked as $\{t_{r,1}, t_{r,2}, \ldots, t_{r,n}\}$ and $\{t_{f,1}, t_{f,2}, \ldots, t_{f,n}\}$. Assuming that $t_r$ and $t_f$ follow normal distributions ($N(\mu_{tr}, \sigma_{tr})$, $N(\mu_{tf}, \sigma_{tf})$) with unknown mean ($\mu$) and unknown standard deviation ($\sigma$), MLE can be employed to calculate mean and standard deviation. Eq. (14) and (15) shows both mean ($\mu$) and standard deviation ($\sigma$) calculations, given the sample set $\{t_{r,1}, t_{r,2}, \ldots, t_{r,n}\}$ and $\{t_{f,1}, t_{f,2}, \ldots, t_{f,n}\}$.

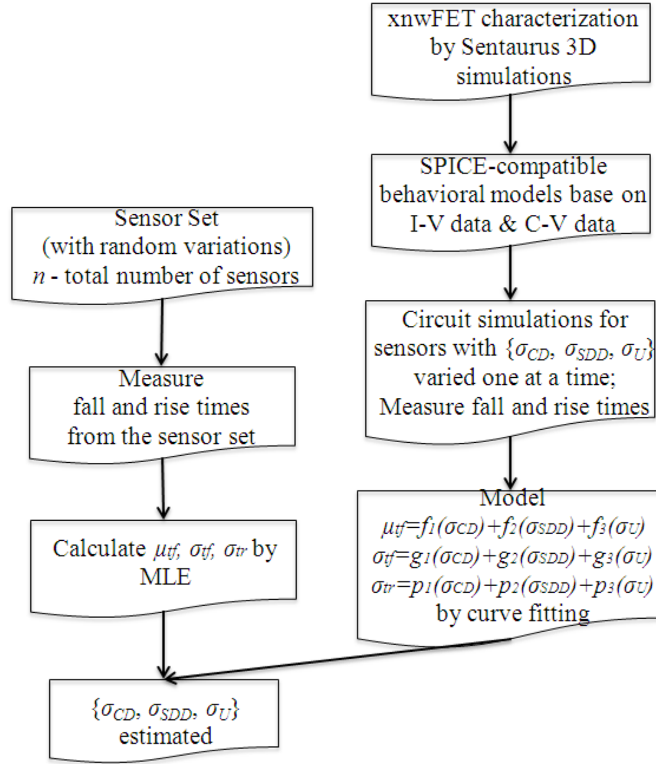


Figure. 13 Maximum Likelihood Estimation (MLE) based variability sensing methodology

$$\mu_{tf/tr} = \frac{1}{n}\sum_{i=1}^{n} t_{f/r,i} \tag{14}$$

$$\sigma_{tf/tr}^2 = \frac{1}{n}\sum_{i=1}^{n}(t_{f/r,i} - \mu_{tf/tr})^2 \tag{15}$$

The fluctuations in rise and fall times in each sensor are directly correlated to the variations in pre and eva xnwFET transistors. We can assume mean and standard deviation of $t_r$ and $t_f$ as functions of standard deviations of random parameters, as expressed by set of equations in (16).

$$\begin{cases} \mu_{t_f} = f(\sigma_{X_1}, \sigma_{X_2}, \cdots, \sigma_{X_N}) \\ \sigma_{t_f} = g(\sigma_{X_1}, \sigma_{X_2}, \cdots, \sigma_{X_N}) \\ \mu_{t_r} = h(\sigma_{X_1}, \sigma_{X_2}, \cdots, \sigma_{X_N}) \\ \sigma_{t_r} = p(\sigma_{X_1}, \sigma_{X_2}, \cdots, \sigma_{X_N}) \end{cases} \tag{16}$$

In (16), f(σ), g(σ), h(σ) and p(σ), respectively, are shown as polynomial functions of standard deviations of physical parameters $\{X_1, X_2, \ldots, X_N\}$.

Specifically, for random parameter variation estimation in the NASIC fabric we mainly focus on three physical parameters: channel doping (CD), source-drain doping (SDD) and underlap (U). To estimate the distributions of these random parameters, we use the equation set (17), based on (16)

$$\begin{cases} \mu_{t_f} = f(\sigma_{CD}, \sigma_{SDD}, \sigma_U) \\ \sigma_{t_f} = g(\sigma_{CD}, \sigma_{SDD}, \sigma_U) \\ \mu_{t_r} = h(\sigma_{CD}, \sigma_{SDD}, \sigma_U) \\ \sigma_{t_r} = p(\sigma_{CD}, \sigma_{SDD}, \sigma_U) \end{cases} \tag{17}$$

Since each of the parameters is mainly dependent on a separate process step, variations in these parameters are independent from each other. As a result, (17) can thus be decomposed into functions of the individual parameters, as shown in (18).

$$\begin{cases} \mu_{t_f} = f_1(\sigma_{CD}) + f_2(\sigma_{SDD}) + f_3(\sigma_U) \\ \sigma_{t_f} = g_1(\sigma_{CD}) + g_2(\sigma_{SDD}) + g_3(\sigma_U) \\ \mu_{t_r} = h_1(\sigma_{CD}) + h_2(\sigma_{SDD}) + h_3(\sigma_U) \\ \sigma_{t_r} = p_1(\sigma_{CD}) + p_2(\sigma_{SDD}) + p_3(\sigma_U) \end{cases} \tag{18}$$

To derive the coefficients of polynomial functions in equation set (18), a device behavioral model encompassing parameter variations is built first. The xnwFET device structure is extensively characterized through variation-aware 3-D physics based simulations using Synopsys Sentaurus tools [14]. Device I-V and C-V characteristics were obtained for up to $3\sigma=\pm30\%$ variations in all parameters; standard deviation, $\sigma=\pm10\%$, was conservatively treated as worst-case scenario such as in [14]. The device characterization data was then used to build SPICE-compatible behavior models using

regression analysis. These behavioral models represent the xnwFET resistance and capacitance as a function of gate-source voltage, drain-source voltage and extent of variation in physical parameters.

Using this device model, the equation set shown in (18) is populated in an initial circuit simulation step. Circuit simulations are carried out for the sensor shown in Figure. 12a – in this, standard deviations of random parameters are varied one at a time. Then, the relationship between {$\mu_{tf}$, $\sigma_{tf}$, $\mu_{tr}$, $\sigma_{tr}$} and {$\sigma_{CD}$, $\sigma_{SDD}$, $\sigma_U$} is built from the measured fall and rise times by curve fitting. Based on the circuit simulation results, $\mu_{tr}$ is almost constant with only 0.14% deviation as {$\sigma_{CD}$, $\sigma_{SDD}$, $\sigma_U$} increasing from 0 to 15%, which means $\mu_{tr}$ is redundant. Finally, the equation set is reduced as shown in (19) with known polynomial functions {$f_1$, $f_2$, $f_3$, $g_1$, $g_2$, $g_3$, $p_1$, $p_2$, $p_3$}.

$$\begin{cases} \mu_{t_f} = f_1(\sigma_{CD}) + f_2(\sigma_{SDD}) + f_3(\sigma_U) \\ \sigma_{t_f} = g_1(\sigma_{CD}) + g_2(\sigma_{SDD}) + g_3(\sigma_U) \\ \sigma_{t_r} = p_1(\sigma_{CD}) + p_2(\sigma_{SDD}) + p_3(\sigma_U) \end{cases} \tag{19}$$

Combining with the calculated {$\mu_{tf}$, $\sigma_{tf}$, $\sigma_{tr}$} from MLE, standard deviations of random parameters are estimated by solving these equations as shown in Figure. 13.

There are two factors that can affect estimation accuracy: the precision of deriving equation set (19) and the accuracy of calculated {$\mu_{tf}$, $\sigma_{tf}$, $\sigma_{tr}$}. Since (19) is derived by curve fitting in an initial circuit simulation step, it can be made increasingly more accurate by choosing more data points (i.e., {$\sigma_{CD}$, $\sigma_{SDD}$, $\sigma_U$} and their corresponding {$\mu_{tf}$, $\sigma_{tf}$, $\sigma_{tr}$}) in the simulations. But the accuracy of calculated {$\mu_{tf}$, $\sigma_{tf}$, $\sigma_{tr}$} depends on the size of sample set, corresponding to the size of the sensor set. In order to reduce the area overhead introduced by on-chip sensors, the sensor set is usually made as small as possible. As a

result, the accuracy of the calculated $\{\mu_{tf}, \sigma_{tf}, \sigma_{tr}\}$ is constrained in practice, which may contribute to a large part of the estimation error. In the next section, we show how the mean and standard deviation calculations can be improved with reduced sample set using Expectation Maximization (EM) technique [31], [32].

### 4.3.2 EM-based Variability Sensing Methodology

The Expectation Maximization (EM) algorithm [31], [32] is an efficient alternative to MLE in the calculation of $\{\mu_{tf}, \sigma_{tf}, \sigma_{tr}\}$. It is an iterative method for estimating the values of some unknown parameters in a statistical model. It can enable more accurate parameter estimation in a statistical model even with incomplete samples. The EM algorithm includes two main steps: the Expectation step and the Maximization step. A general process of EM algorithm for an incomplete sample set is shown as follows.

- Initialize the distribution parameters for the sample set
- Repeat until convergence:
    1) Expectation step: calculate the expected value of the sample set and fill the missing samples with this expected value, given the current distribution parameters.
    2) Maximization step: re-estimate the distribution parameters to maximize the likelihood of the known samples, given the current expected estimates of the missing samples.

The core of the Expectation step is to rebuild the complete sample set, based on the given distribution parameters. Since the known samples really exist, we try to maximize their likelihood with the rebuilt complete sample set during the subsequent Maximization step. Because the results calculated by the Expectation step and Maximization step depend

on each other, the EM algorithm is iterated sufficient times until the likelihood of the known samples is converged, treated as its maximization. At this time, the estimated distribution parameters are closest to the actual distribution parameters of this incomplete sample set. To estimate the mean and standard deviation in the normal distribution, a framework of EM algorithm is shown in Figure. 14.

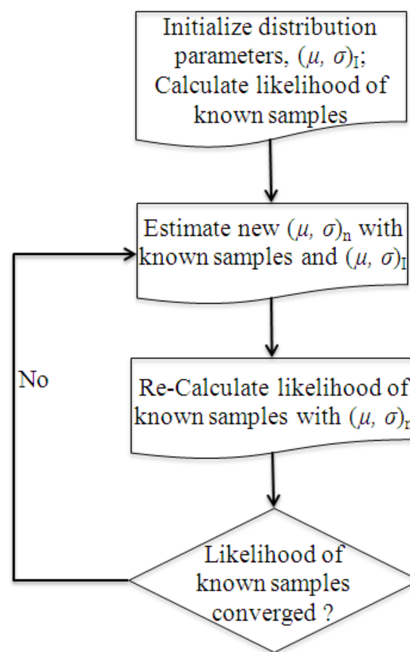


Figure. 14 Flowchart of Expectation Maximization algorithm for normal distribution

Based on Figure. 14, the EM algorithm is iterated enough times until the convergence of the likelihood of the known samples is reached, treated as the maximum of this likelihood. In this algorithm, the initial values of ( μ, σ) affect the estimation accuracy and overall run-time, and should be therefore chosen carefully.

In our case, the known samples in the incomplete sample set correspond to the sensors we use, and the unknown samples represent the sensors removed from our sensor set. So an insight can be achieved that the area overhead introduced by our random-variation sensors can be reduced by employing EM algorithm. In order to explain the usage of EM

algorithm in our random-variation sensing methodology clearly, we define two sensor sets: the complete sensor set (i.e., an imaginary sensor set that can provide sufficient samples to achieve converged estimates) and the current sensor set employed. Because EM algorithm is a modified MLE algorithm, the size of the complete sensor set can be determined by MLE algorithm. Then the number of missing samples equals to the difference in the sizes of these two sensor sets.

Here we assume the size of the complete sensor set is n and the size of current sensor set employed is m, the number of missing sensors equals n-m. Let $\{t_{r,1}, t_{r,2}, \ldots, t_{r,m}\}$ and $\{t_{f,1}, t_{f,2}, \ldots, t_{f,m}\}$ denote the measured rise and fall times from the current sensor set, and $\{t_{r,m+1}, t_{r,m+2}, \ldots, t_{r,n}\}$, as well as $\{t_{f,m+1}, t_{f,m+2}, \ldots, t_{f,n}\}$, denote the unknown measurements from the missing sensors. As the part of the process of EM in the calculation of the mean and standard deviation of $t_r$ and $t_f$ is completed in a similar manner, we only use fall times ($t_f$) to illustrate how EM algorithm calculates the mean and standard deviation from an incomplete sensor set. This is as follows.

1 Estimate an initial $(\mu, \sigma)_C$ for the complete sensor set, $\{t_{f,1}, t_{f,2}, \ldots, t_{f,m}, t_{f,m+1}, t_{f,m+2}, \ldots, t_{f,n}\}$;

2 Calculate the log-likelihood function, given known $\{t_{f,1}, t_{f,2}, \ldots, t_{f,m}\}$ under this initial $(\mu, \sigma)_C$ by Eq. (20);

$$L(t_f) = -0.5n * \log(2\pi * \sigma_C^2) - 0.5\sum_{i=1}^{m}(t_{f,i} - \mu_C)^2 / \sigma_C^2 \tag{20}$$

3 Re-estimate $(\mu, \sigma)_C$ by Eq. (21) and (22);

$$\mu_{C,i} = \frac{1}{n}\sum_{i=1}^{m} t_{f,i} + \frac{n-m}{n}\mu_{C,i-1} \tag{21}$$

$$\sigma_{C,i}^2 = \frac{1}{n}[\sum_{i=1}^{m} t_{f,i}^2 + (n-m) * (\mu_{C,i-1}^2 + \sigma_{C,i-1}^2)] - \mu_{C,i}^2 \quad (22)$$

4 Re-calculate the log-likelihood function given known $\{t_{f,1}, t_{f,2}, \ldots, t_{f,m}\}$ under the new $(\mu, \sigma)_C$ by Eq. (20);

5 Repeat until the convergence of the log-likelihood function is reached.

The condition of convergence is expressed as Eq. (23),

$$\left| L(t_f)_{new} - L(t_f)_{old} \right| < \varepsilon \quad (23)$$

where ε is very small and depends on the required accuracy.

Figure. 15 shows our random variation sensing methodology, which uses EM algorithm for mean and standard deviation calculation. Compared with the previous MLE-based estimation methodology, the main difference is that in the estimation flow we replaced MLE (for the calculation of mean and standard deviation of fall and rise times) by the EM

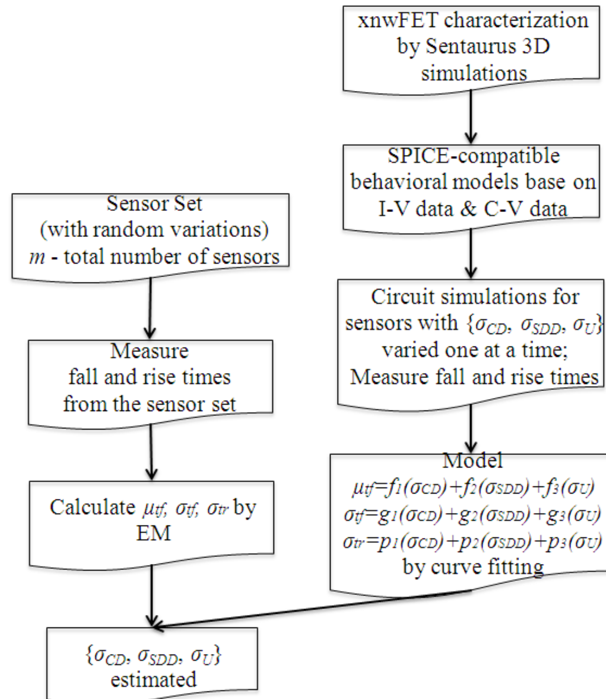


Figure. 15 Expectation Maximization (EM) based variability sensing methodology

algorithm.

### 4.4 Evaluation of the Proposed Sensor Design

In this section we detail a framework for evaluating the accuracy of our sensor design based on HSPICE Monte Carlo simulations. The framework is shown in Figure. 16.

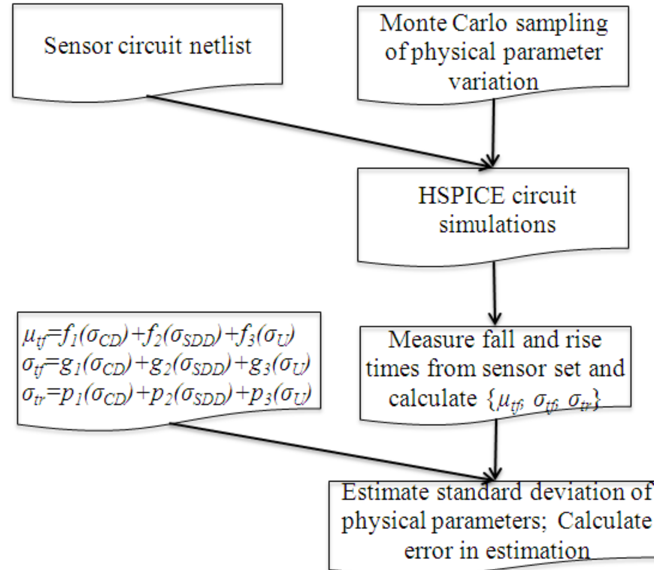


Figure. 16 Framework for evaluating sensor design based on Monte Carlo circuit simulations

As shown in Figure. 16, HSPICE circuit simulations need to be carried out with known variation cases injected into the sensor circuits. These simulations assume normal distributions of individual device parameters with a known standard deviation. Based on the measured fall and rise times from the sensor circuits, the standard deviation of random parameters is estimated using the theoretical framework described in the previous sections. As statistical methods are used in the proposed methodology, the number of samples becomes very important to the estimation accuracy. The number of sensors in the sensor set is varied to demonstrate how it affects the estimation accuracy. HSPICE circuit simulations on the sensor set are iterated 1,000 times to achieve sufficient estimates for

{$\sigma_{CD}$, $\sigma_{SDD}$, $\sigma_U$}. The probability density functions (PDF) of these estimated standard deviations are built to check the degree of convergence. Then the relative errors in estimated vs. injected standard deviations of random parameters are calculated. This iterative flow is abstracted in Figure. 17.

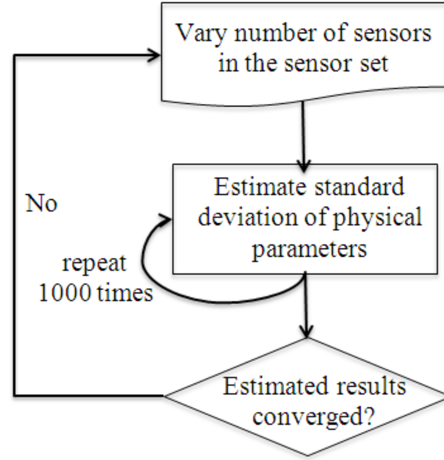


Figure. 17 HSPICE Monte Carlo circuit simulation flow

**4.5 Results**

Following the evaluation framework described in the previous section, circuit simulations were carried out to determine the accuracy of the sensing method for random variation estimation. In the equation set (19), f(σ) was populated as a fifth-order polynomial; g(σ) and p(σ) were populated as third-order polynomials. The simulations were iterated for 1,000 times to estimate {$\sigma_{CD}$, $\sigma_{SDD}$, $\sigma_U$} sets. The metrics used are Estimation Error (EE) and Average Estimation Error (AEE) for the parameter $X_i$ across 1,000 iterations. We defined these as:

$$EE = \left|(\sigma^e_{X_i} - \sigma^i_{X_i})\right| / \sigma^i_{X_i} \tag{24}$$

$$AEE = (EE_1 + EE_2 + \cdots + EE_{1000}) / 1000 \tag{25}$$

wherein $\sigma^{e}_{Xi}$ is the estimated standard deviation of parameter $X_i$, and $\sigma^{i}_{Xi}$ is the injected standard deviation of parameter $X_i$ in the simulations; $EE_j$ represents the jth estimation error for one parameter across 1,000 iterations.

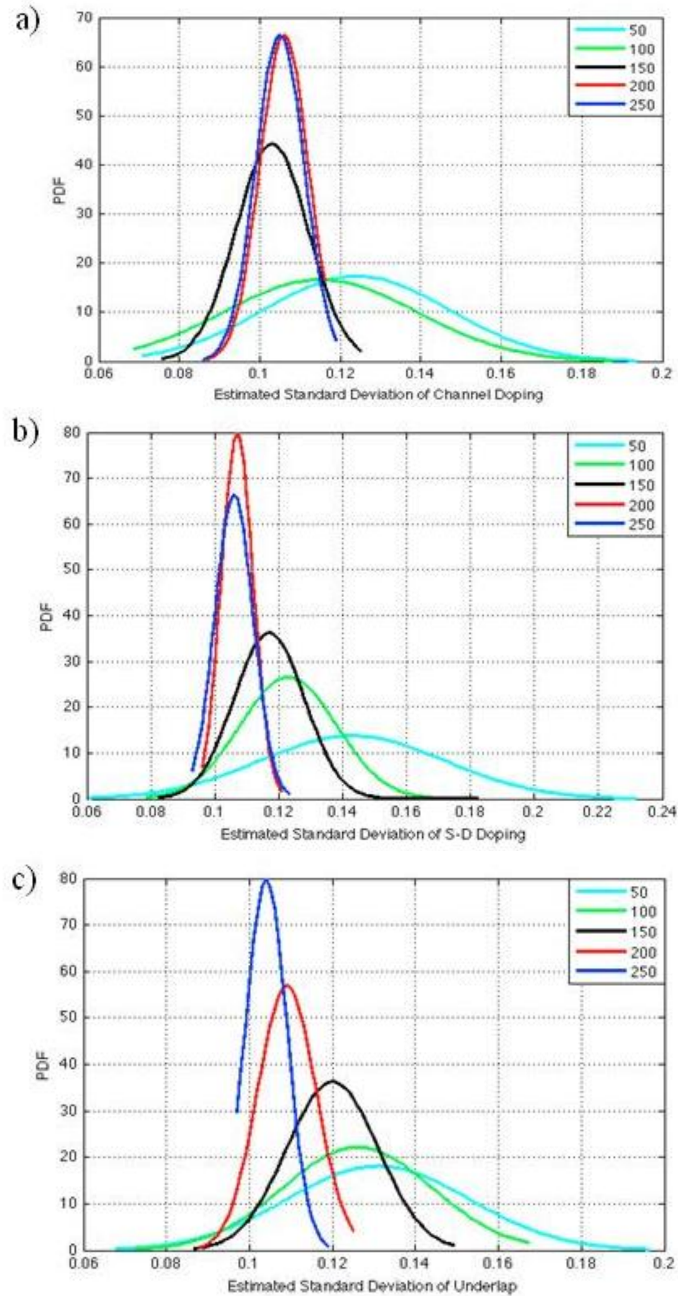


Figure. 18 Probability density function (PDF) of estimated standard deviation for varying number of sensors in the sensor set; a) Channel doping; b) Source-Drain doping; and c) Underlap

4.5.1 Simulation Results of MLE-based Sensing Methodology

Figure. 18 shows the probability density function (PDF) of estimated standard deviations for varying number of sensors in the sensor set. The estimated standard deviations gradually converge and approach the injected value (0.1) as the number of sensors in the sensor set (n) increases. For example, when n increases from 50 to 200, σ in PDF of estimated $\sigma_U$ decreases from 0.022 to 0.007, which means the degree of convergence in $\sigma_U$ is increased by 3X. However, when n increases from 200 to 250, the improvement in the convergence of estimated $\{\sigma_{CD}, \sigma_{SDD}, \sigma_U\}$ becomes less significant; a less than 10% decrease in σ of PDFs of the estimated $\{\sigma_{CD}, \sigma_{SDD}, \sigma_U\}$ is in fact achieved. This means that 200 sensors in the sensor set are sufficient to estimate $\{\sigma_{CD}, \sigma_{SDD}, \sigma_U\}$ such that they are less than or equal to 0.1.

For the sensor set containing 200 sensors, the estimation error for every parameter was calculated. The corresponding cumulative distribution function (CDF) of estimation error across 1,000 estimated results is shown in Figure. 19. From this figure, we can note that the estimation error is largest for the underlap variation; however, this error is still less than 15% for 90% of simulations and smaller than 25% for all simulated cases. Estimation

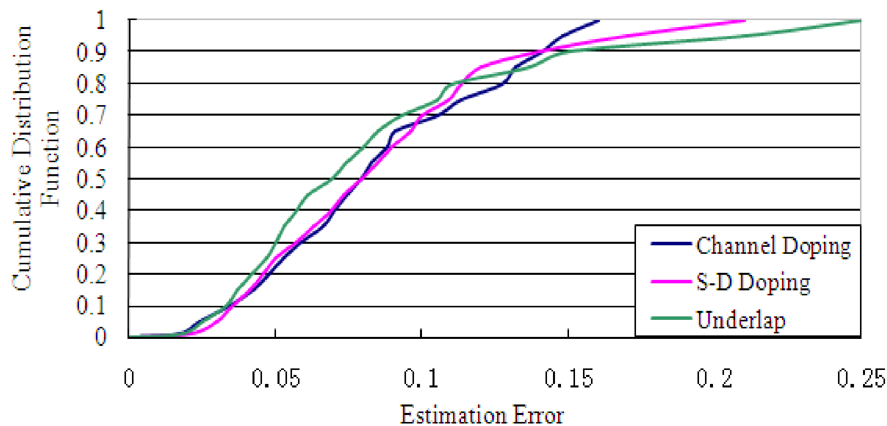


Figure. 19 Cumulative distribution function (CDF) of estimation error across 1,000 estimated standard deviations

errors of all three parameters for worst-case scenarios are summarized in Table. 5.

Table. 5 Estimation Error for MLE-Based Sensing Methodology

| | Underlap | Channel doping | SD doping |
|---|---|---|---|
| *EE* in worst-case scenario | 25% (most sensitive) | 16% (least sensitive) | 20% |

4.5.2 Simulation Results of EM-based Sensing Methodology

Based on our simulation results achieved from MLE-based sensing methodology, 200

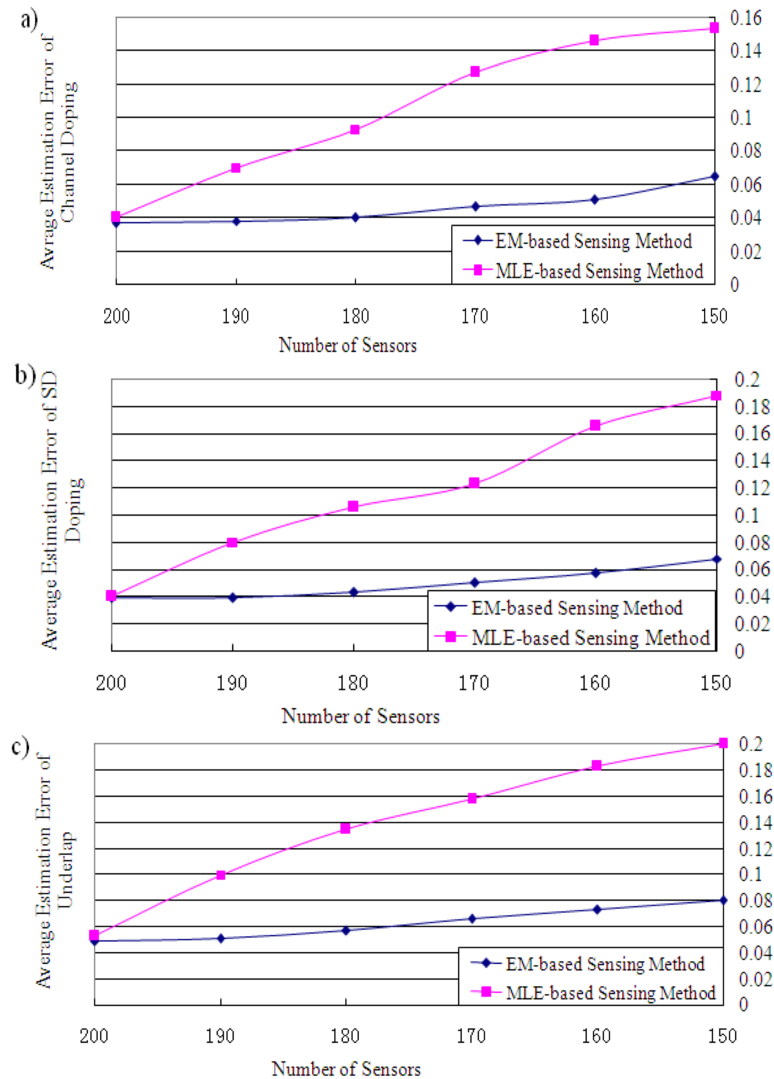


Figure. 20 Comparison of average estimation error (*AEE*) between EM-based and MLE-based sensing methods: a) Channel doping; b) Source-Drain doping; c) Underlap

sensors are sufficient to achieve converged estimates if the standard deviation of random parameters is less than or equal to 10%. For the EM-based sensing methodology, the size of the complete sensor set (n) was set to 200 and kept constant for simulations. Figure. 20 shows the comparison of AEE for MLE-based and EM-based sensing methods. AEE is much smaller for the EM-based sensing method than the MLE-based sensing method. For example, for underlap (U), if the number of sensors in the current sensor set (m) decreases from 200 to 150, AEE increases from 0.053 to 0.2 with the MLE-based sensing method, but only increases from 0.049 to 0.08 with the EM-based sensing method. As a result, the estimated results become more robust with decrease in number of sensors and the estimation accuracy is improved by at least 2X with the EM-based sensing method. The results are presented in Table. 6, which shows a range of AEEs due to varying number of sensors from 200 to 150.

Table. 6 Comparison of *AEE* between EM-based and MLE-based Methods

| | *m* decreased from 200 to 150 | | |
|---|---|---|---|
| | *AEE* of *CD* | *AEE* of *SDD* | *AEE* of *U* |
| EM-based method | [0.037,0.065] | [0.039,0.068] | [0.049,0.08] |
| MLE-based method | [0.04,0.153] | [0.04,0.188] | [0.053,0.2] |

For the EM-based sensing method, the number of sensors in the sensor set was gradually decreased to evaluate estimation accuracy. The relationship between AEE and the number of sensors in the sensor set is shown in Figure. 21. The estimated standard deviation of underlap has the largest AEE among the three random parameters. If AEE is required to be less than 10%, at least 150 sensors are needed in the sensor set.

For m=150, the cumulative distribution function of the estimation error is shown in Figure. 22. From these results, EE is largest for the underlap variation with 12.7% (for all

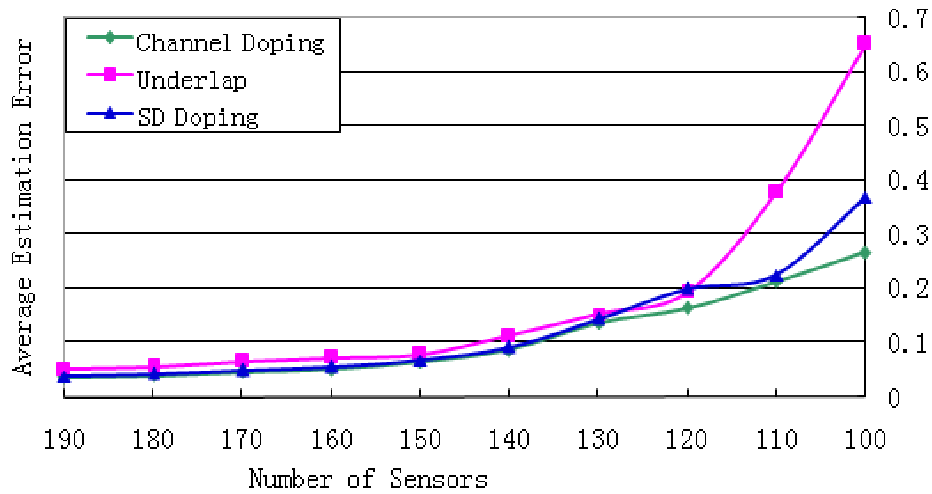

Figure. 21 Relationship between average estimation error and number of sensors

simulations), which can be treated as worst-case scenario. EEs in the worst-case scenario for all three parameters are listed in Table. 7. Compared with the EEs in Table. 5, the estimation accuracy is improved by 2X with the EM-based sensing method.

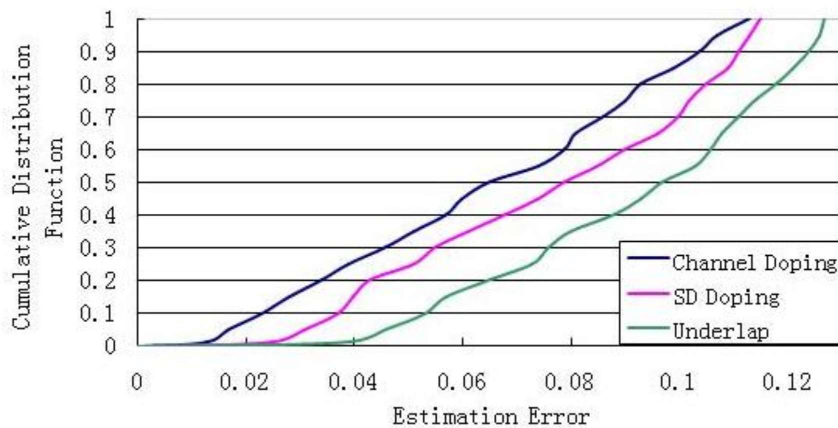

Figure. 22 Cumulative distribution function of estimation error for m=150 current sensor set

Table. 7 Estimation Error for EM-Based Sensing Method

| | Underlap | Channel doping | SD doping |
|---|---|---|---|
| *EE* in worst-case scenario | 12.7% (most sensitive) | 11.3% (least sensitive) | 11.5% |

In order to evaluate the proposed EM-based sensing method more extensively, the injected standard deviation of physical parameters was reduced gradually from 10% to 1% in the Monte Carlo simulations; we then re-estimated the error with the EM-based sensing method. Following the evaluation flow shown in Figure. 16, the worst-case estimation errors were calculated. Figure. 23 shows the relationship between worst-case estimation errors and injected standard deviations of physical parameters. For these simulations number of sensors in the sensor set was fixed to 150. From these results, the worst-case estimation error decreases slightly (as the injected standard deviation of physical parameters). The main reason for this slight decrease in the worst-case estimation error is the increase of the accuracy in the calculation of $\{\mu_{tf}, \sigma_{tf}, \sigma_{tr}\}$. As the standard deviation of a physical parameter decreases, the degree of fluctuation in the fall and rise times also decreases, which means the number of samples required to derive the distribution decreases. However, the number of sensors in all simulations remains constant, so the accuracy of calculated $\{\mu_{tf}, \sigma_{tf}, \sigma_{tr}\}$ improves. From Figure. 23, the worst-case estimation error is less than 13% with the EM-based sensing method for all standard deviations that are less than or equal to 10%.

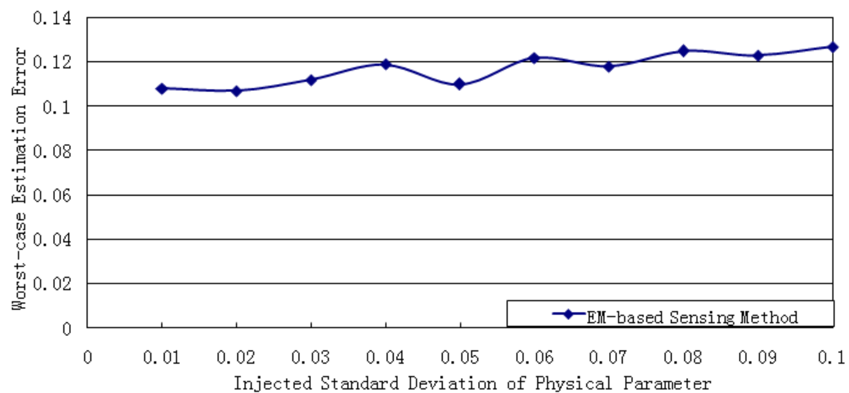

Figure. 23 Relationship between the worst-case estimation error and the injected standard deviation of physical parameter for $m$=150

### 4.6 Summary

In this chapter, a new on-chip variation sensor design for random variation estimation in the NASIC fabric was presented. A generic sensing methodology for extracting distributions of random variations in physical parameters from the measured fall and rise times was described. Using physics-based device models and Monte Carlo simulations, the estimation accuracy was quantified. Simulation results show that with the EM-based variability sensing methodology, an 8% average estimation error can be achieved with as low as 150 sensors in the sensor set. The estimation error in the worst-case scenario was 12.7% for all simulated cases. Compared with the ring-oscillator (RO) based sensor design in CMOS technology shown in [33], the worst-case estimation error is improved by 1.6X, and the total number of devices required in on-chip sensors is reduced by 40X.

# CHAPTER 5

# PLACEMENT OF ON-CHIP VARIATION SENSORS

## 5.1 Introduction

Recent technological developments have facilitated the widespread use of variation sensors in variation diagnosis. Due to the aggressive technology scaling and the drastic increase in chip density, it is often of great importance that the variation sensor configurations in use minimize area overhead while meeting some appropriate requirements. We develop two separate approaches for determining the placement of the proposed systematic-variation sensor and random-variation sensor respectively. Further, we introduce examples of sensor placements with WISP-0 processor as a target. Lastly, we identify and analyze external noises that may affect the accuracy of measured fall and rise times based on the sensor placement.

## 5.2 Placement of Systematic-Variation Sensor

As discussed in section 3.5.2, the sensor effective range is up to 3.3mm considering a permissible estimation error of 20% using an experimental model developed by the 180nm technology. In order to adjust to the emerging nanoscale fabrics, this sensor effective range needs to be scaled down based on the projected technology parameters. Sensor effective area can then be determined with respect to the sensor area and shape. Finally, the sensor placement can be developed with the help of sensor effective area.

### 5.2.1 Calculation of Sensor Area

NASIC fabric is a regular grid-based fabric with crossed nanowire field-effect transistors at certain crosspoints. Given the specified technology parameters, the circuit

area can be easily calculated based on the required number of vertical and horizontal nanowires. The layout of the systematic-variation sensor is shown in Figure. 24, where the light blue rectangles at the crosspoints represent xnwFETs in NASIC fabric. As a result, 58 horizontal nanowires and 8 vertical nanowires are used to build the sensor. Technology parameters used are listed in Table. 8. Then the sensor area is calculated, as shown in Eq. (26).

$$Area = (58*10 + 57*10)*(8*10 + 7*10) = 172500\ nm^2 \tag{26}$$

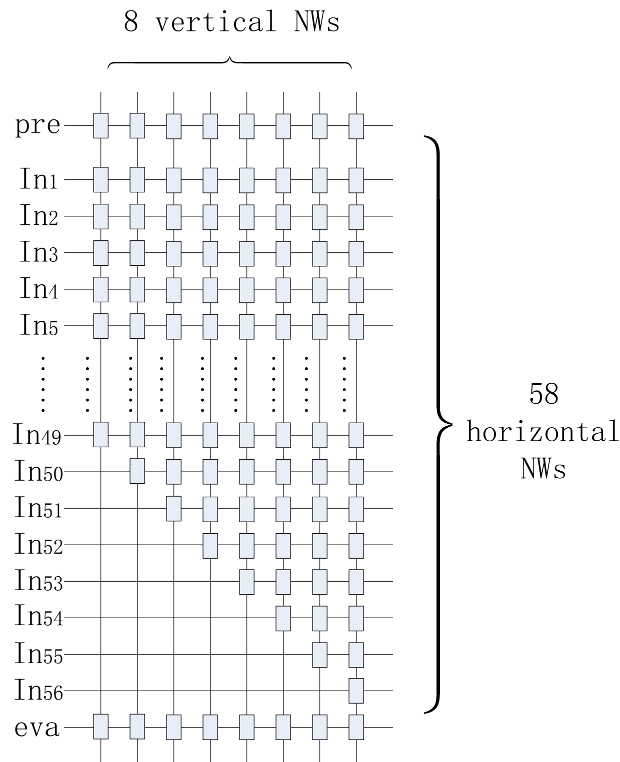


Figure. 24 The layout of the systematic-variation sensor

Table. 8 Parameter values for density calculation

| Parameter | Value |
|---|---|
| NW-pitch | 20nm |
| NW-width | 10nm |

### 5.2.2 Re-calculation of Sensor Effective Range

Based on the parameters listed in Table. 8, the projected technology node in this thesis is 10nm, which means the sensor effective range should be scaled down with respect to the technology node of 10nm.

With the aggressive scaling of technology nodes, parameter variations are increasing drastically. The statistical results between parameter variations and technology nodes are explored in [34]. Based on these statistical results, when the technology node is scaled down from 180nm to 10nm, percentage of parameter variations increases 40X. It means the sensor effective range needs to be scaled down 40X. So the new sensor effective range (R) with a permissible estimation error of 20% for the 10nm technology is shown in Eq. (27).

$$R = 3.3mm / 40 = 82.5um \tag{27}$$

Assuming all devices in the sensor share the same systematic variations, the sensor effective region with consideration of sensor shape is shown in Figure. 25. The area of this

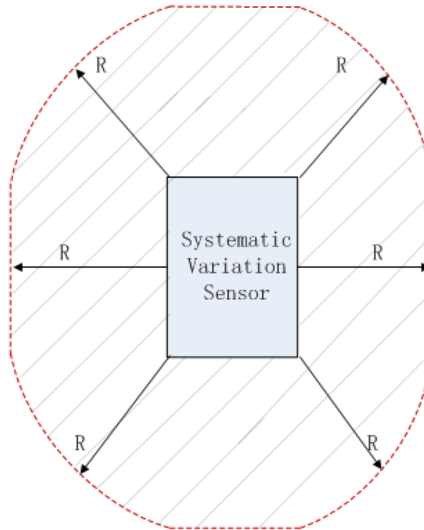


Figure. 25 Schematic diagram of sensor effective range with consideration of sensor shape

sensor effective region is calculated with the new sensor effective range, shown in Eq. (28).

$$Area_{Effective} = \pi R^2 + 2R(1.15 + 0.15) = 21597um^2 \quad (28)$$

5.2.3 Example of Sensor Placement

Based on the sensor effective range, the placement of systematic-variation sensor can then be introduced. The principle of sensor placement is to cover all regions implementing logic by the sensor effective range using the least number of sensors. Here we use WISP-0 processor [1], [2], [12], [13], [35] as an example to show the sensor placement and timing measurement architecture. WISP-0 is a NASIC processor design where NASIC design principles are applied. It implements a 5-stage pipeline architecture, which contains fetch, decode, register file, execute and write back. The floorplan of WISP-0, including program

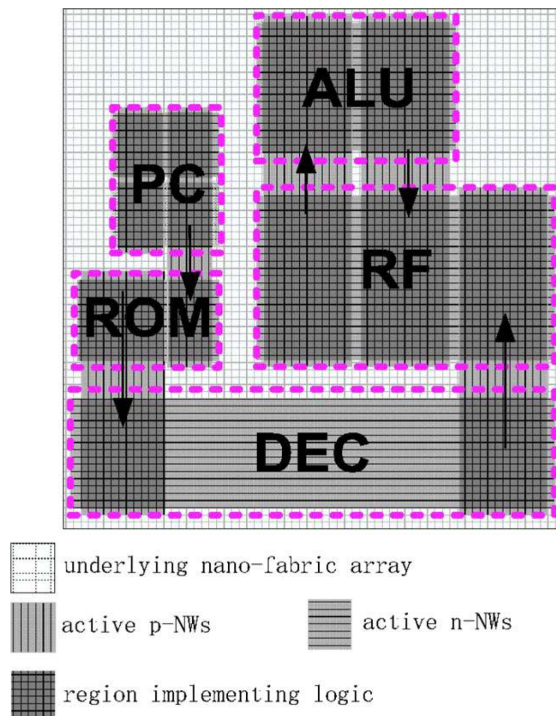

Figure. 26 Floorplan of the WISP-0 processor [35]

Table. 9 Area of WISP-0 in NAND-NAND style [35]

| | Nanoarray area ($nm^2$) |
|---|---|
| PC | 35200 |
| ROM | 26400 |
| DEC | 57600 |
| RF | 476000 |
| ALU | 59400 |
| Total | 654600 |

counter (PC), ROM, decoder (DEC), register files (RF) and ALU, is shown in Figure. 26. The area for each unit in WISP-0 is listed in Table. 9. Because the total area of WISP-0 is 654600nm$^2$, it is far more less than the sensor effective area. As a result, only one sensor is enough to cover all logic regions in WISP-0. Because RF takes more than 70% area of WISP-0, in order to balance the area of logic regions surrounding the systematic-variation sensor, an example of the sensor placement in WISP-0 processor with timing measurement architecture is shown in Figure. 27.

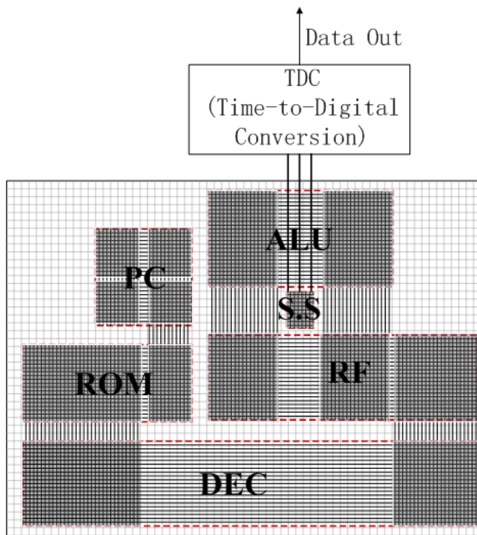


Figure. 27 Floorplan of the WISP-0 processor with systematic variation sensor and additional CMOS TDC (S.S represents systematic-variation

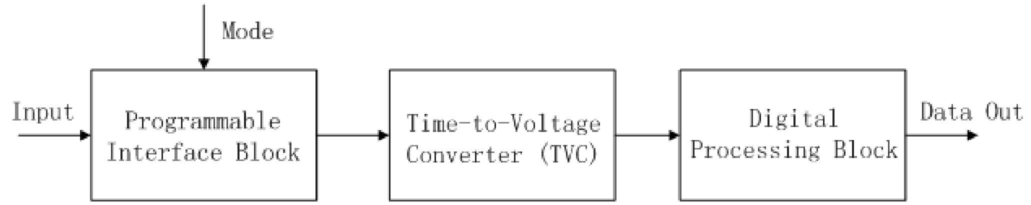


Figure. 28 Block diagram of timing measurement architecture [36]

In Figure. 27, the timing measurement architecture [36] is treated as an additional CMOS circuit. Its block diagram is shown in Figure. 28. The mode signal is used to configure the time measurement circuit. For example, if mode signal is '0', this circuit operates to measure rise time of the input signal. Finally, this circuit can convert rise or fall times into a digital form and generate an N-bit output code. By adding an N-to-1 multiplexer to the input, we can measure rise or fall times from N input signals by only one such time measurement architecture and output the measured results in series.

### 5.2.4 Impact of External Noise on the Estimation Accuracy

With respect to the sensor placement, several external noises may affect the values of measured fall times, leading to decrease in the estimation accuracy. These noises include wire delay, measurement error and environmental noise. Therefore, the measured fall time is represented by Eq. (29).

$$T_{f_measured} = T_{f_real} + T_{wire} + T_{measurement} + T_{environment} \tag{29}$$

Wire delay is conventionally dominated by a wire's resistance-capacitance product, or RC delay, which is a function of wire material and wire physical dimensions (e.g., length, width and thickness). With respect to the sensor placement shown in Figure. 27, the wire material and dimensions between outputs in the sensor and the time measurement

architecture are nearly identical, leading to the same wire delay for each output in the sensor.

As the same timing measurement architecture is used to measure fall times in the sensor, the measurement error for each output is also same. Finally, the environmental noise, such as the thermal noise, is mainly governed by environmental factors. Because fall times in the sensor are measured by the timing measurement architecture in a very short time interval, all the environmental factors can be assumed constant in this short time interval. As a result, this environmental noise can also be treated as constant for all outputs in the sensor.

Based on the analysis above, the difference in fall times in one functional unit can be expressed by Eq. (30).

$$\begin{aligned} & T_{f,2_measured} - T_{f,1_measured} = (T_{f,2_real} - T_{f,1_real}) + (T_{f,1_wire} - T_{f,2_wire}) + \\ & (T_{f,1_measurement} - T_{f,2_measurement}) + (T_{f,1_environment} - T_{f,2_environment}) \\ & = T_{f,2_real} - T_{f,1_real} \end{aligned} \tag{30}$$

From Eq. (30), we can see that these external noises have no or very little impact on the estimation accuracy of the proposed systematic-variation sensor.

## 5.3 Placement of Random-Variation Sensor

Similarly to the process for systematic-variation sensor, the area of random-variation sensor will be calculated at first. Then based on the characteristics of random variations, an example of the sensor placement will be introduced. The impact of external noises on the estimation accuracy will be finally discussed.

### 5.3.1 Calculation of Sensor Area

The layout of the random-variation sensor is shown in Figure. 29. Using the same method and technology parameters (i.e., 10nm NW and 20nm NW pitch) as for the systematic-variation sensor, the sensor area is calculated by Eq. (31).

$$Area = (2*10+10)*(150*10+149*10) = 89700\ nm^2 \tag{31}$$

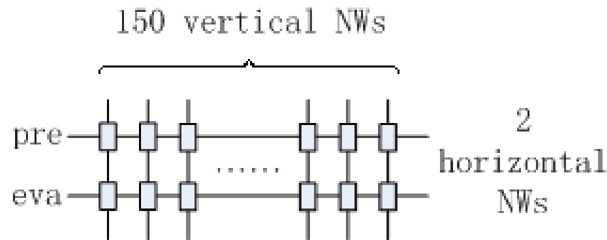


Figure. 29 The layout of the random-variation sensor

5.3.2 Example of Sensor Placement

Because of the randomness of random variations, the random-variation sensors can be placed anywhere in the chip to sample characteristics of random variations. Since the fall and rise times in the sensors are used to estimate random variations directly, the principle of the sensor placement is to reduce the impact of external noises on the measured fall and

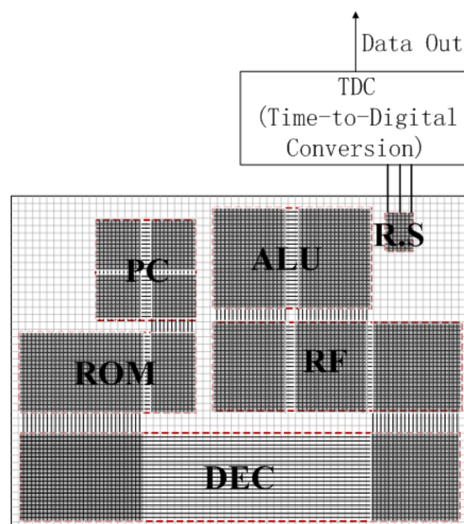


Figure. 30 Floorplan of the WISP-0 processor with random-variation sensor and additional CMOS TDC (R.S represents random-variation

rise times. In order to achieve this objective and share the timing measurement architecture with the systematic-variation sensor, an example of the sensor placement is shown in Figure. 30. Since the measured fall and rise times also follow Eq. (29), this sensor placement can reduce the wire delay by placing the random-variation sensor close to TDC (measurement error and environmental noise are independent on the sensor placement).

### 5.4 Summary

In this chapter, the sensor configuration was discussed. The sensor area was calculated at first, which could be treated as the area overhead introduced by on-chip sensors. Then using WISP-0 processor as a target, an example of the sensor placement was presented based on the sensor effective range. In addition, timing measurement architecture in CMOS was shown, which can be used to measure fall and rise times from multiple outputs in the sensors. With respect to the placement of on-chip variation sensors, several external noises were identified. By analyzing their sources, we found that the estimation accuracy of systematic-variation sensor is not deteriorated by these noises. However, the random-variation sensors are very sensitive to them. Since theoretically random-variation sensors can be placed anywhere in the chip, the placement of random-variation sensors tries to reduce the impact of these external noises on the measured fall and rise times.

# CHAPTER 6

# CONCLUSION

In this thesis, we proposed novel on-chip variation sensor designs for emerging nanoscale computing fabrics, which can estimate variations in physical parameters (e.g., channel diameter, gate oxide thickness and source-drain doping density) by employing a physical based device model. Based on the different characteristics of parameter variations, two separate sensor circuits were designed to estimate systematic variations and random variations respectively.

With respect to systematic variations, a pair of NAND gates with fan-in (i, i+1) formed a basic sensing unit that further composed our systematic-variation sensor, based on the number of physical parameters varying systematically. With careful sensor design, relationships between the difference in fall times in one functional unit and physical parameters varying systematically were extracted from our sensor circuits. With the measured fall times in the sensor circuit, the extent of systematic variations was estimated by solving those relationships. Through accurate HSPICE Monte Carlo simulations, our systematic-variation sensor was evaluated and the results show less than 1.2% error in estimation of the extent of systematic variations for 100% of the simulations. In addition, to address the sensor placement, sensor effective range was derived based on the distribution of systematic variations and a maximum allowed imprecision. By employing an experimental model for systematic variations in gate diameter, our sensor effective range was up to 3.3mm with respect to a 20% imprecision.

By contrast, a variation sensor design for estimating the statistical distribution of random variations was presented. To avoid averaging effect, the random-variation sensor

circuit was a very simple dynamic gate with only pre and eva xnwFETs. Therefore, the deviations of rise and fall times at output nodes were attributed to variations in pre and eva xnwFETs respectively without the impact of averaging effect. To estimate the standard deviation of random parameters, a variation sensing methodology was described, which could enable this estimation with measured fall and rise times in the sensors. Our random-variation sensor design was evaluated through HSPICE Monte Carlo simulations and the simulation results show an 8% average estimation error with as low as 150 sensors in the sensor set. The worst-case estimation error is 12.7% for all simulated cases. These results indicate the feasibility of our outlined approach.

Finally, an example of the sensor placement was introduced with WISP-0 processor as a target. We discussed the principles of sensor placement and presented timing measurement architecture. The area overhead introduced by on-chip sensors was also calculated with respect to the projected technology parameters (NW: 10nm; NW pitch: 20nm). Based on the sensor placement, the influence of external noises on the estimation accuracy was analyzed and we found that these noises do not affect the systematic-variation sensor, but deteriorate the accuracy of the random-variation sensor.

Furthermore, we believe that the proposed on-chip variation sensors when applied in conjunction with post-fabrication compensation techniques would be able to improve system-level performance in nanoscale computing fabrics, an alternative to making worst-case assumptions on parameter variations in nanoscale designs.

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