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TFT and ULSI technologies: The parallel evolution of the research and the higher education in France

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Olivier Bonnaud, "TFT and ULSI technologies: The parallel evolution of the research and the higher education in France" in "International Conference on Semiconductor Technology for Ultra-Large Scale Integrated Circuits and Thin Film Transistors VI (ULSIC vs TFT 6)", Yue Kuo (Texas A&M University, USA) Olivier Bonnaud (University of Rennes I, France) Eds, ECI Symposium Series, (2017). http://dc.engconfintl.org/ulsic_tft_6/19

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TFT and ULSI Technologies; the Parallel Evolution of the Research and the Higher Education in France

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This paper deals with the evolution since the early eighties of the microelectronics applied to integrated circuits and to large area electronics, in France. The evolution was resulting of the policy of the French government to support the development of the industry as well as the Higher Education in this field. The goal was to form the future technicians, engineers, masters and doctors with the knowledge and the know-how in this specialty. More recently, a new national plan was engaged in the frame of the French Large Investment Commissariat with the goal to adapt the new technologies to the emerging digital society. Connecting objects and Internet of Things are mainly mixing ULSI and large area technologies. After a synthetic presentation of the evolution of the two main technologies developed in R&D centers and in academic laboratories, the paper highlights the strategy developed by the French education community based on the innovation.

Introduction

This paper deals with the evolution since the early eighties of the microelectronics applied to integrated circuits and to large area electronics. The evolution in France was linked to a very strong effort of the French government (Microelectronics national plan) to improve the Higher Education in this field and to form with the knowledge and the know-how the future engineers, masters and doctors to the research and development and to the production. A way to help the growth of microelectronics companies mainly in France, but also in the world through multinational companies. More recently, a new national plan was engaged in the frame of the French Large Investment Commissariat [1] with the goal to improve the large area technology and the integrated technologies, which must be adapted to the emerging digital society. Connecting objects and Internet of Things are mainly mixing the different components of the electronics and microelectronics domains [2].

After a synthetic presentation of the evolution of the two main technologies developed in research and development centers and in academic laboratories, the paper highlights the strategy developed by the French community based on the innovation [3]. The interesting point is that, if at the beginning the two domains appeared independent, the evolution of the process and the fabulous evolution of the CAD tools made closer and closer the design and fabrication approaches by combining the two technologies. For example the FDSOI (Fully Depleted Silicon on Insulator) concept was in practice existing since many years in thin film transistor technology deposited at a relatively low temperature (<600°C) on glass substrates [4]. The arrival on the market of the first systems-on-chip (SOC) and systems-

in-package (SIP) with a wide spectrum of applications [5] confirms this interpenetration which has also a multidisciplinary aspect [6]. The new technologic process developed by French LETI laboratory, entitled Coolcub^{TM}, combines the classical VLSI technology with thin film technology in a three dimensional stacking at a relatively low temperature [7].

This evolution induces a huge change in the pedagogical approach in order to maintain a good background, skills and know-how for the research, development and fabrication activities [8-9]. The end of the paper will be devoted to the presentation of several examples of innovative projects, proposed to the students that must have this double competence of the thin film electronics and of the ultra-large scale-integration microelectronics moving to nanoelectronics. A way to prepare the evolution of this field that is the heart of most objects of the near future.

Explosion of the microelectronics activities in the eighty's

At the end of the seventy's, the French government tried to develop its own computer technologies with a special multiannual plan. Very fast, it was obvious that the development of computers passed through the control of the technologies and more especially of the fabrication of electronics devices and integrated circuits. Thus, similarly to the evolution of the USA in the Silicon Valley, a national strategy was set-up to create research, research and development structures, and to increase the industrial activities in France, in the field. In that time, for example, Eurotechnique [10], Sesco [11] in Aix-en-Provence, Thomson in Grenoble and Tours, and RTC Compelec in Caen (Normandy) were too small to insure the huge development of the integration semiconductor technologies.

This period corresponds to the creation of the LETI research center in Grenoble [12], the CNET (National Center for telecommunications studies) with three main sites in Brittany, in Paris, and in Grenoble, as well as companies like EFCIS in Grenoble (that became STMicroelectronics later with the association to Eurotechnique) or ES2 (European Silicon Structures) in Aix-en-Provence (South of France), that was bought later by ATMEL and then Global Foundries [13]. In parallel, initial US companies like Matra Harris, Fairchild (later SGS, and then STMicroelectronics), IBM (later ALTIS) increased their fabrication potentialities in France. As shown in the figure 1, we can notice that after several years, the historical companies were bought: Thomson-Sesco, Eurotechnique, and SGS became STMicroelectronics with EFCIS, RTC Compelec became successively Philips, NXP and IPDIA recently, for example.

These restructuration trends were the sign of the strong evolution and the change of the size of the facilities, the size of the plants, as a matter of fact of the investments. If more than ninety percent of the activities were devoted to the integrated silicon technologies in very large scale integration (VLSI), Thomson and CNET research centers worked on the III-V compound technologies and on the future large area electronics. On this last point, the goal was to move from the MINITEL developed by the French Communication company and involving cathode ray tubes (CRT) to flat panel displays (FPD) fabricated on glass substrates and involving thin film diodes and thin film transistors (TFT). The activities were shared in the technology and in the design. In this context, it was clear that the need of technicians and engineers became very high and that in parallel the government had to develop the higher education in the field. Knowing that the know-how is very important in this field, the policy was oriented towards the creation of common microelectronics centers with facilities in technology via cleanroom mainly devoted to education.

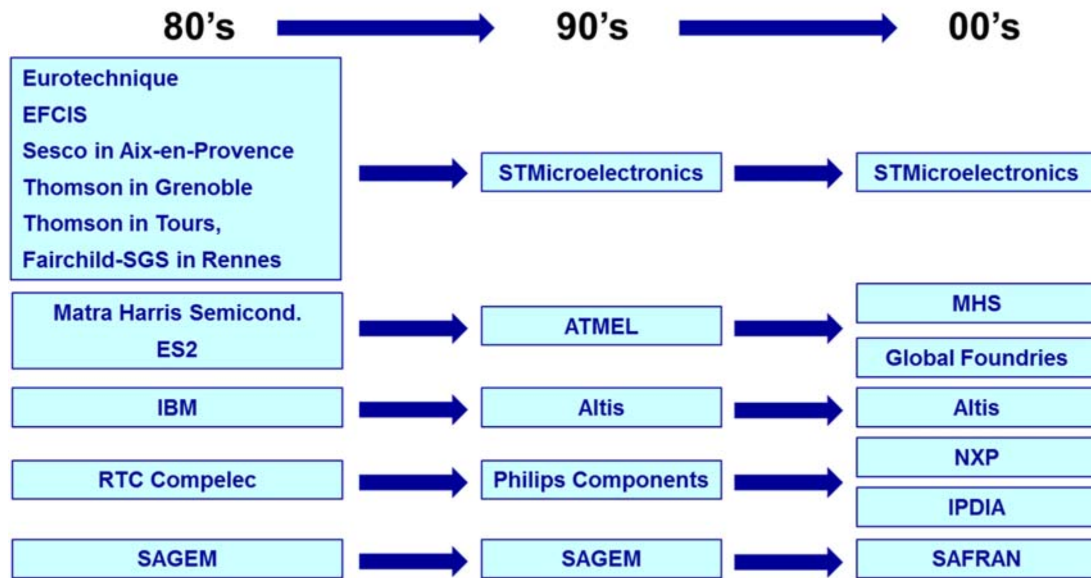

Figure 1. Evolution of French microelectronics companies during the last forty years. Grouping and restructuration governed the strategy in order to maintain a competitiveness in this very fast evolution industry.

National French education strategy to develop microelectronics

In 1981 a new national plan was launched to develop higher education and to train new engineers and masters in the field of microelectronics in both technology and computer-aided design. At this level, the problem was the dispersion of formations on the national territory. In order to achieve a critical mass and therefore effectiveness, the strategy was to create common centers between several institutions, a strategy strongly encouraged by the Ministry in charge of Higher Education.

In this context, the National Committee for Education in Microelectronics was created. It was composed of the members attached to 10 institutions that had in charge to create locally interuniversity structures in the frame of convention and of an industrial partner, the microelectronics industrial body. In this way, 10 centers were set-up in the main area of the activities of microelectronics as well in research as in production, with a strong financial support of the Ministry of Higher Education and the Ministry of Industry. The first objective was to gather and to share the competences and the skills as well the investments associated to the construction and starting of 5 cleanrooms opened mainly for education in which the students could be able to fabricate a simple microelectronics circuit, or specific devices like III-V compound semiconductor devices or thin film devices in function of the economic and industrial environment of the centers. To give an idea, today, about 4000 students have each year an experience in a cleanroom. They have some practice of fabrication process of simple circuits, from substrate cleaning step to final electrical characterizations of the wafers with a prober. Usually, the students spend with their teachers from 2 to 5 days in function of the level and of the pedagogical objectives. This

practice is considered mandatory in order to obtain solid knowledge and know-how in the field; this strategy is increasingly needed in the frame of development of educative tools available on internet but that do not give the know-how.

One of the centers was devoted to the computer aided design and played the role of national services. In charge of the negotiation to acquire software licenses with the suppliers, the national services manage the distribution to the users. Today, there are 90 institutions (universities, engineer schools, technician schools) using the design software as well as the 60 research laboratories associated to the national committee. As a result, about 14,000 students from the end to the secondary school to the doctorate levels are formed each year with the design tools distributed by the national services that are negotiated with the major companies of the field, such as Cadence, Synopsis, Mentor Graphics, Coventor, Silvaco, but also Altera and Xilinx for the software and cards devoted to the embedded electronics.

The evolution of the software was incredible during the last forty years, and associated to the huge increase of their complexity and of their calculation powerfulness also. Thus, the national services have to up-date permanently the CAD tools and they play a major role in the cohesion of the network.

The present situation of the national network (GIP-CNFM [14]) is shown on the Figure 2. The twelve present centers appear with their environment of research and industrial activities (ocher circles). The centers are usually localized in an area that contains many companies of the field. Students can have practice and labworks on the platforms in the close area but also in another faraway one, in function of the specialties. For example, the centers of Grenoble and Toulouse are majorly devoted to silicon-based integrated technologies towards nanotechnologies. Rennes and Bordeaux centers are more oriented towards thin film technologies (silicon and organic): Lille was specialized in III-V compound semiconductor technologies and more recently on graphene-based devices.

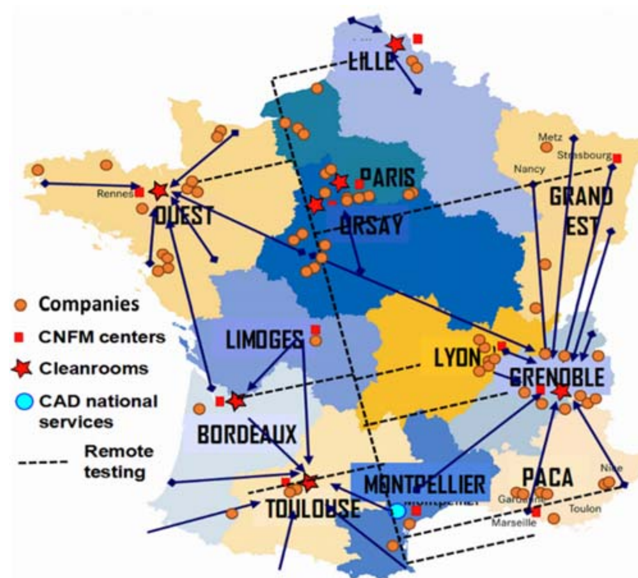

Figure 2. French national network for Higher education in microelectronics (GIP-CNFM). The twelve microelectronics centers are spread all over the territory and majorly in the area of the companies. Students can have practice on the platforms in the close area but also in another far one in function of the specialties.

Evolution of the technologies and associated studies

In this context, the conditions were favorable for contributing to the global effort to develop microelectronics and to fit the evolution predicted by G. Moore [15].

On VLSI side, the technologies moved progressively from silicon bipolar transistors to MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) based circuits, and to CMOS circuits (Complementary MOSFET). These devices have involved the self-aligned lithography and self-organization techniques, processes that have been the vectors of the fabulous decrease of the size of the elementary devices and that have allowed continuing to follow the Moore's Law. Moving towards the nanometric dimensions and in order to minimize the leakage current associated to the very thin insulator layers, new architectures were also proposed.

The use of insulating substrates (SOI for silicon on insulator) minimizing the bulk effects such as latch-up, the short channel effects, and the parasitic capacitances [16], lead to the creation of a new device family that also allows the back biasing of the channel. The creation of SOITEC Company in Grenoble that produces the SOI wafers was in agreement with this evolution that has converged recently towards the FDSOI technology (Fully depleted SOI). This technology is today the flagship of STMicroelectronics in Grenoble after many years of research and development with the LETI and several academics laboratories. Other international companies such as Samsung, RENESAS, Global Foundry, NXP, and Freescale have adopted recently this approach to develop the future circuits in the range of 10 nm for the smallest dimension of the channel length. The best advantage of this technology is the relative continuity with the planar technologies previously developed during more than forty years. For example, the addition of a high permittivity material in the very thin gate insulator such as HfO_2 in order to prevent tunnel leakage current does not over-complex the fabrication process.

In parallel, for a company like Intel, the challenge was to create a new architecture with vertical channel layer and involving by this way the third dimension. FinFET (Field Effect Transistor with a fin for the channel zone) was developed [17]. The potential improvement of the integration is thwarted by a much more complex process and a higher cost.

Figure 3 shows the schematic cross-section of the FDSOI and FinFET architectures [18]. The very thin fins with a relatively high aspect ratio and the vertical walls for the gate introduced several technological challenges.

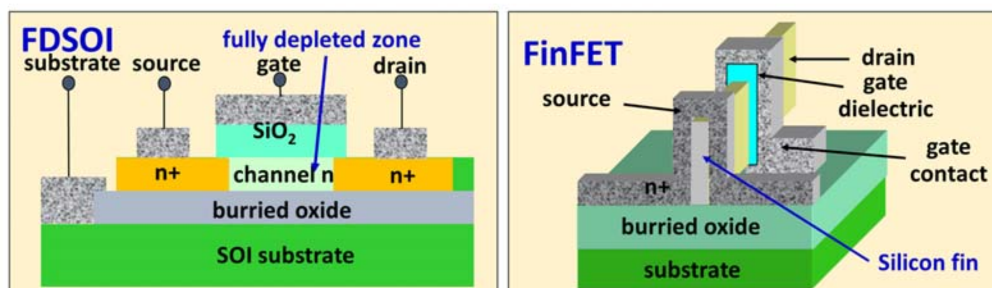

Figure 3. Schematic cross-section of the two technologies in strong competition today, FDSOI and FinFET. The FDSOI one seems to be more adapted for the expected applications in the connected objects [18].

The competition between these two recent technologies is strong. In France, the choice appears seriously oriented towards FDSOI. However, for the future, new architectures are studied in research and development by the LETI with the help of academic laboratories. Involving much more the third dimension and very small dimensions, two ways seem promising, the multi-nanowire based devices [19] and the very low temperature process structures involving the stacking of many device layers, the Coolcub^{TM} [7]. Figure 4 shows a schematic cross-section of an elementary stacking proposed by the LETI.

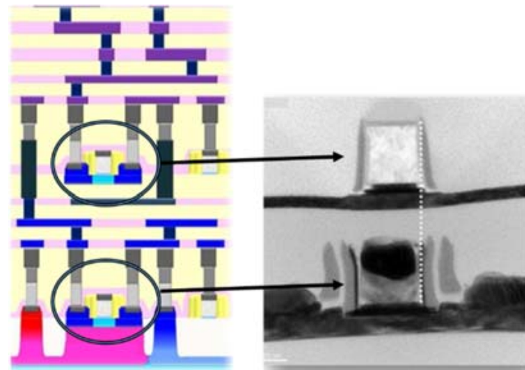

Figure 4. New tridimensional architecture developed by LETI, the Coolcub^{TM}. Many transistors layers are stacked thanks to depositions at very low temperature (*After* Batrude *et al.* [7]).

This process is a way to increase the integration while avoiding the reduction of the minimum dimensions lower than several nanometers.

The presence, close to the LETI of a cleanroom of the Grenoble CNFM center dedicated to education allows to prepare the students and future engineers to work in this field. Of course, the strategy is the same for all the CNFM centers.

On thin film technologies side, the first studies with CNET and Thomson were focused on thin film transistors for flat panel displays with active pixels. The first technologies were based on amorphous silicon thin film transistors with back-gating and deposited on glass substrates. Because the mobility of free carriers in amorphous silicon is very low in comparison with monocrystalline silicon, the main challenge was to increase the electrical properties of the material. Many studies were performed in collaboration with CNET and Thomson to deposit or reach polycrystalline layers with a reasonable thermal budget compatible with the substrate limitation. Several techniques were studied and have proved the feasibility such as *in-situ* doped LPCVD (Low Pressure Chemical Vapor Deposition) of amorphous silicon followed by solid phase thermal crystallization (SPC) [20-21] or in liquid phase crystallization by several types of lasers (excimer laser, cw YAG laser [22], or Very Large Excimer laser [23]). With laser beam radiations, the duration of the high energy heating is very short and affects only the deposited semiconductor layers thanks to a very short duration of the radiation, or thanks to a scanning of the beam at the surface. Figure 5 shows the principle of the polycrystalline CMOS like TFT [24] with, on the left hand side, a schematic cross-section and on the right hand side, a top view of a processed inverter involving one NMOS and one PMOS. Due to the lower mobility of the holes in the channel of the PMOS, the width of this TFT is higher.

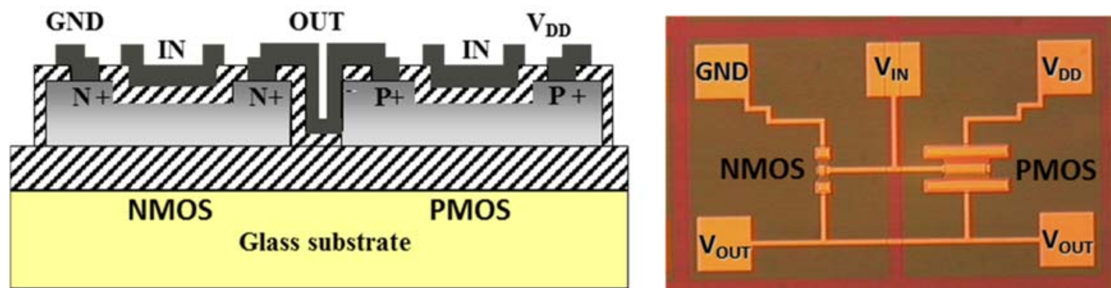

Figure 5. CMOS like TFT inverter involving solid phase crystallization of *in-situ* doped LPCVD amorphous silicon [24]. Schematic cross-section, on the left, and top-view from a microscope of the final device, on the right.

This process, developed in IETR, involving *in-situ* doped source and drain of both types (p and n) have proved the feasibility and the very good reproducibility. If many results were very good and promising, the industrialization could induce huge investment. The production mainly in the Far-East has however maintained during many years the amorphous-based technology with liquid crystal as optical switch. The development of the light emitting diode (LED) in thin film technology approach changed the strategy. Let us notice that the polycrytalline TFT had allowed the creation of new types of sensors, like the magnetic sensors [25] and airgap thin film transistors [26]. This last structure opens many applications and more especially physical, chemical, and biological sensors. Indeed, thanks to the presence of the airgap, a gap between the gate contact and channel region without any physical insulating layer, and thanks to the functionalization of the surface of the channel, a high selectivity combined to a high sensitivity can be achieved [27]. More recently, the flexible electronics involving microcrystalline silicon [28-29] or organics based devices [30] were developed. Several French laboratories are strongly involved in these activities such as IMS (Bordeaux) and IETR (Rennes), two laboratories having common facilities with their respective CNFM center. As it is already mentioned, the platforms of the national network for education are adapted to form the engineers, the masters, and also the doctors specialized in these technologies. The synergy between research and education is very high in this case.

Some common approaches between ULSI and TFT in the more recent evolutions

The fast overview of the evolution of the ULSI and TFT technologies could leave the feeling that the associated improvement occurred independently. It is in practice the contrary. For example, governed by the use of glass substrates and later by plastics substrates, the development of processes for flat panel displays have focused the researchers towards growth of materials at low temperature and increasingly the involvement of the third dimension. This need was progressively the same for the ultra large scale integration for which the thermal budget is very low in order to avoid any diffusion of species and more especially of doping atoms in the ultra-narrow junctions. The use of vacuum or airgap was also adopted in order to minimize the leakage current. In France, several studies were developed in this way. We highlight here-after the most significant studies.

The studies on the deposition of silicon and associated compound (for example Silicon-Germanium) lead to the deep understanding of LPCVD, PECVD (Plasma Enhanced

Chemical Vapor Deposition) and VLPCVD (Very Low Pressure CVD [31]) techniques. More recently, ALD (Atomic Layer Deposition) was developed and mainly applied to integrated technologies thanks to the very good control of the growth at atomic level and thanks to a good coverage factor of the layer when the surface is relatively hilly [32].

Another common evolution concerns the introduction of airgaps. The first results on thin film transistors were published in 2003 [26-27]. With a suspended gate (SGFET), they present very interesting sensor properties. Airgaps are also employed in the updated FinFET structures. Indeed, researchers from IBM and Global foundries have reported on the first use of “air-gaps” as part of the dielectric insulation around active gates of "10nm-node" FinFETs [33]. In fact it is used as interlayer dielectric and allows minimizing leakage current at the level of the gate. Figure 6 shows on the right hand side an airgap TFT and, on the left hand side, an airgap FinFET.

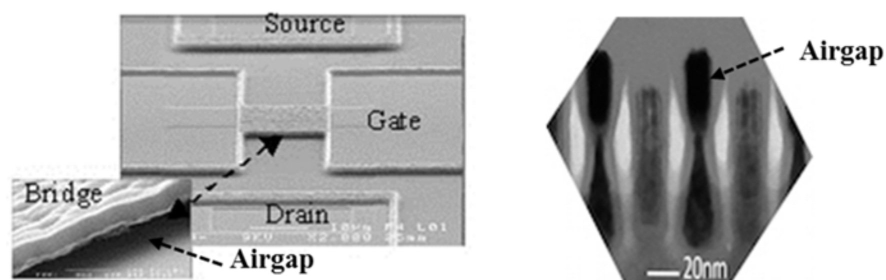

Figure 6. (left) Airgap TFT (*After* F. Bendriaa *et al.*) and (right) airgap FinFET (*After* Ed Korczynski). For both cases, the leakage current between gate contact and channel region is minimized. In the SGFET, the airgap zone can be functionalized and can act as a high sensitive sensor.

The concept of very-low temperature deposition techniques allowing the development of tridimensional architectures in ULSI technologies was first used to protect the power devices and circuits by stacking polysilicon diodes or thin film transistors in the early 90’s. A prototype was developed in cooperation between STMicroelectronics and academic laboratories [34].

All these common approaches indicate the trend of the technologies. The initial education as well as the life-long learning of industrial employees must be in agreement with this evolution.

Consequences on the training of engineers and doctors

It is clear that the processes are increasingly complex and involve process steps, which allows the growth of very thin layer with a low thermal budget. In terms of education, the difficulty comes from the large diversity of the knowledge and know-how. The graduate students must have a good background as well as some specialized skills. Somehow, the adaptation of students should be facilitated by the convergences occurring in technological evolutions.

However, the process steps combine many phenomena (chemical, physical, thermal, mechanical, electrical, optical, etc., and even at atomic scale), which implies an increasing multidisciplinarity [9]. The design of new architectures requires also a lot of competences in modeling, simulation, high level languages such as VHDL, multi-physic simulations,

and thus a widening of the spectrum of knowledge. It is more and more difficult to give a proper and comprehensive education to these students.

The proposed method consists of an intensive practice on dedicated platforms in initial education as well as in labworks, projects and internships. This is the approach that was included in the strategy of the French national network. Each year, the network management organizes a call for innovative practices that contains, obviously, the new fabrication process and design techniques [8]. The goal consists to create new platforms dedicated to the training on the new techniques and their applications.

In this strategy, we can give several examples of recent innovative practices set-up in the French microelectronics centers for education with the goal to prepare the students to the new processes and to the evolution towards the internet of things (IoT). Figure 7 shows two devices designed and fabricated by students on CNFM platforms: the flexible flat panel display at Rennes ("Ouest" center), and organic emitting diode at Bordeaux center.

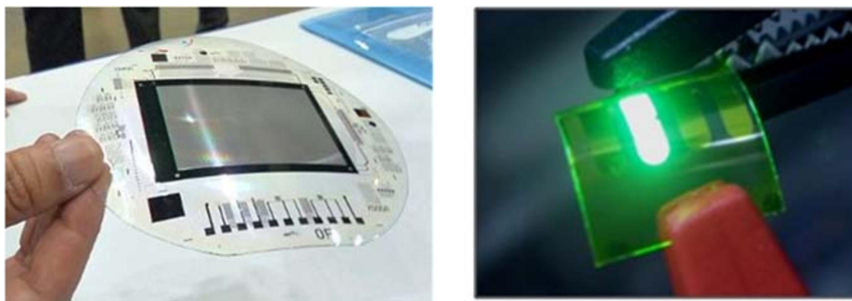

Figure 7. (left) Thin film circuit on flexible substrate (*After* West center activity report) and (right) organic emitting diodes on plastics (*After* Bordeaux center activity report.). These devices are fabricated by the students on the CNFM platforms.

Figure 8 shows on the left hand side a magnetic sensor and associated circuit designed and fabricated by students and involving polycrystalline thin film technology on the basis of the research activities [25]. It is based on Hall Effect in a thin film of *in-situ* doped polycrystalline silicon. On the right hand side, a wafer including membrane for pressure detection designed and fabricated on usual monocrystalline silicon wafers by students of the Grenoble center.

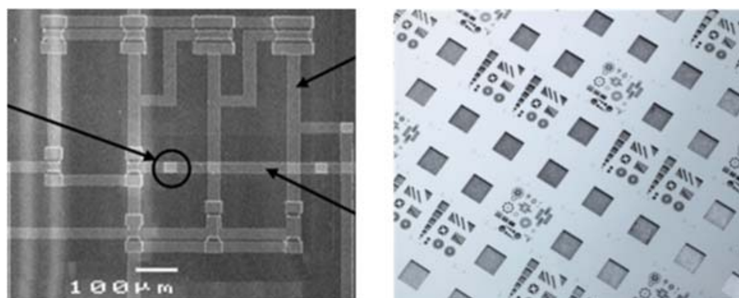

Figure 8. (left) Magnetic sensor involving polysilicon TFT (*After* "Ouest" center activity report) and (right) MEMS with suspended membranes (*After* Grenoble center activity report). All these devices are fabricated by the students on the CNFM platforms.

Figure 9 shows a super-capacity designed and fabricated by master students in the cleanroom of the Toulouse center. It can be a component of an energy harvesting device

integrated in connected objects. For these last objects, the electronics can be embedded through FPGA (Field Programmable Gate Aray), for example. Dedicated activities on embedded electronics are performed in all the centers. Figure 9, on the right hand side, shows a student designing a connected object on the Grenoble platform.

Figure 9. (left) Super-capacity for energy harvesting device integrated in connected objects (*After* Toulouse center activity report.) and (right) Embedded electronics for connected objects (*After* Grenoble center activity report). These devices and circuits are fabricated and designed by the students on the CNFM platforms.

To give an idea of the importance of the French network, 81 platforms including 7 cleanrooms are opened to students with these types of practice. Because the new objects are increasingly multidisciplinary, they drive the choice of the innovative practice. Many practices are thus oriented to sensors and actuators or to signal transmission electronics; platforms for MEMS, NEMS, BioMEMS, biosensors, physical and chemical sensors, are suitable for education in half of the centers. By this approach, the network hopes to maintain a high quality of diplomas in order to provide the companies and the research institutes of the field with technicians, masters, engineers, and doctors and to insure a high level of competitiveness.

Conclusion

During more or less forty years, the development of French and European microelectronics followed the unbelievable increasing of the performance of microelectronic circuits as well in integrated technologies as in thin film's ones. Many researches were performed and allowed to form doctors and engineers able to contribute to this evolution. This development has been made permanently turbulent due to the industrial strategies governed by the scale of the investments to be assumed. In parallel, the need of specialists has transformed the Higher education landscape with the creation of academic microelectronics centers devoted to Higher education in this field that might give the knowledge and the know-how to the future actors. This strategy needed also a permanent up-dating of the activities that are oriented today towards innovation and the future societal challenges. Thanks to strong links between education and industry in the frame of the national network, the strategy based on the innovation and on the multidisciplinary know-how seems to be well engaged in the global competition for the next years.

Acknowledgments

The author wants to thank the colleagues with IETR, department of sensors and microelectronics, and the colleagues with the GIP-CNFM. Special thanks to Lorraine Chagoya-Garzon, executive assistant of the GIP-CNFM, for the technical support in the redaction of this paper.

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