LARGE SCALE GRAPHENE INTEGRATION FOR SILICON TECHNOLOGIES

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The main guarantor of success for silicon based semiconductor research and industry was the availability and continuous improve of wafer fabrication processes for large scale integration. New material integration in a stable and reliable silicon process platform has to face several challenges. Graphene as a 2D material is considered as a material with formidable properties. This can enable new functionalities and performance improvements in a large variety of applications. Using graphene devices in microelectronics requires beside appropriate performances certain techniques for large scale fabrication of graphene which are currently not yet in place. In this paper we present recent progress of process platform developments to enable wafer scale integration in a silicon cmos platform. Synthesis of graphene on silicon cmos compatible substrates are considered to fulfill a basic request for the integration of graphene related devices in a silicon environment with no risk of metallic cross contamination. We present recent results of graphene synthesis on Ge(100) and Ge (110). Therefore chemical vapor deposition (CVD) methods are used to realize Ge/Si substrates followed by a CVD graphene synthesis at ~890°C (1,2). Due to silicon diffusion inside germanium certain germanium thickness is required to allow the subsequent graphene process. We present high quality graphene on a 200mm silicon wafers with high uniformity, a 2D/G ratio of ~3 and low D mode over the entire 200mm wafer measured by Raman spectroscopy (Figure 1). To enable a selective graphene synthesis on a 200mm wafer we discuss first approaches of graphene growth on patterned germanium island.

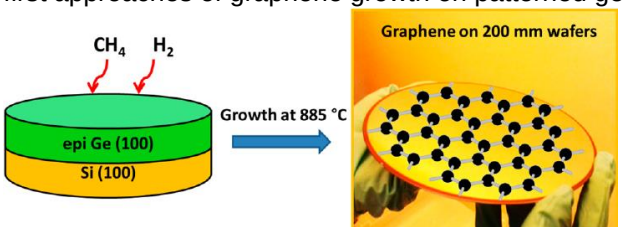

Figure 1: Germanium substrate realization and graphene synthesis on 200mm wafer (2).

Beside the synthesis a wide range of process steps is required to enable a sufficient graphene related device realization on a 200mm wafer. For this reason we consider a toolbox of processes dedicated to handling, cleaning, patterning as well as non-destructive deposition techniques of dielectric layers on graphene. Here, different approaches for the deposition of thin HfO_2 layers are reviewed (3) as well as the deposition of silicon nitride layers.

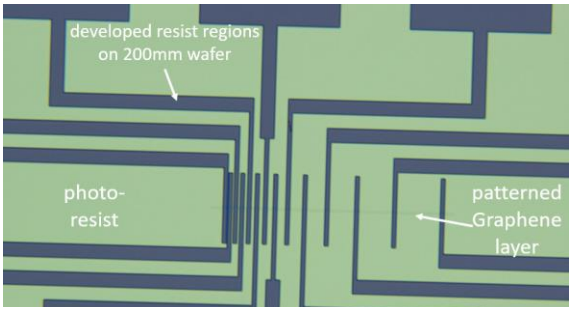

Figure 2: Patterned graphene test structure on 200mm wafer.

The latter appears to be a very valuable development offering not only a good quality insulating active layer on graphene but also an efficient protection of graphene against damages during device fabrication using standard manufacturing methods. All presented process developments are essential as a prerequisite to practical applications of this material in electronic and photonic devices (4). Finally sufficient techniques for process quality insurances like metrology methods are necessary to enable a realistic device process scenario. Usually Raman spectroscopy is used to ensure the quality of deposited and processed graphene. As a possible approach for a fast and reliable method to control graphene quality in a semiconductor process flow we consider spectroscopy ellipsometry measurements. We show that this high-throughput optical metrology method can be used to measure the thickness and uniformity of wafer scale graphene as well as to control the quality of cleaning steps during graphene patterning. We present recent results of these measurements, advantages and challenges in comparison to established characterization methods. In conclusion we present a closed loop of process steps of a silicon cmos platform used for the fabrication, patterning, and passivation of graphene layers. These investigation and developments are essential to enable a future graphene device realization in a microelectronic platform.

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