

BRAIN-LIKE SYNAPSE THIN-FILM TRANSISTORS USING OXIDE SEMICONDUCTOR CHANNELS AND SOLID ELECTROLYTIC GATE INSULATORS

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Human brain has astonishing advantages such as tolerance to system faults, low power consumption, and adaptive learning ability from pre-obtained data unlike conventional computer system with Von Neumann architecture. One of the most attractive benefits of human brain is an ability of parallel processing. Considering these advantages, new types of devices featured to emulate the human brain are quite demanding. These artificially designed systems are called neuromorphic systems, in which neurons are inspired by electronic signals applied to synapses. They can be useful components in artificial perception and action systems. Recently, many types of electronic devices mimicking the functions of human brain have been energetically studied [1-2]. However, these devices have following limitations. First, it needs additional external memories for storing synapse information because CMOS devices cannot work as nonvolatile memories. Second, conventional Si-based electronic technology is not compatible with large-area electronics implemented on glass or flexible substrates. In this work, we propose new type of synapse device with thin-film transistor (TFT) configuration for realizing simple device structure and operation for synaptic learning, in which oxide semiconductor In-Ga-Zn-O (IGZO) and solid electrolytes, such as poly(4-vinylphenol) - sodium β -alumina (PVP-SBA) and polypropylene carbonate (PPC), are employed as active channel and solid-electrolytic gate insulators for TFT operations, respectively. Solid electrolytes can be promising for controlling the synaptic weights by exploiting the movements of charged ions within the electrolytes. Lithium and sodium ions are transported in PPC and PVP-SBA, respectively. Synaptic weights can be determined as the modulated channel conductance and be estimated from the gradual variations in drain currents. Figs. 1(a) and 1(b) show cross-sectional view of fabricated synapse TFT using PVP-SBA gate insulator and schematic structures of biological synapse & neuron, respectively. Figs. 2(a) and 2(b) showed the variations in output drain currents as functions of two input pulse parameters, amplitude and width. First, the voltage pulses were repeatedly applied to the gate terminal one-hundred times with a fixed pulse width of 50 ms. The output drain current gradually increased with increasing the number of pulses [Fig. 2(a)]. When the pulse amplitude was varied to 10 and 20 V at ten-time applications, the value of obtained output drain current markedly increased and the current ratio for two conditions were calculated to be approximately 2.6. These results clearly suggest that the synaptic weights could be more fortified when larger voltage signals (20 V) were employed for synaptic operations. In other words, it means that the quantity of residual memory or response significantly increased with stronger stimuli. When pulse signals with a fixed amplitude of 10 V were applied with variations in pulse widths of 10, 50, and 100 ms. The output drain currents more quickly increased for longer pulses [Fig. 2(b)]. The obtained current ratios of 100-ms conditions to 10-ms condition at ten- and one-hundred-time applications were estimated to be approximately 3.1 and 2.1, respectively. These results emulate the changes in learning time at a single event. Our proposed synapse TFTs can be a suitable candidate for the next-generation low-power large-area electronics such as neuromorphic systems and flexible bio-mimicking devices.

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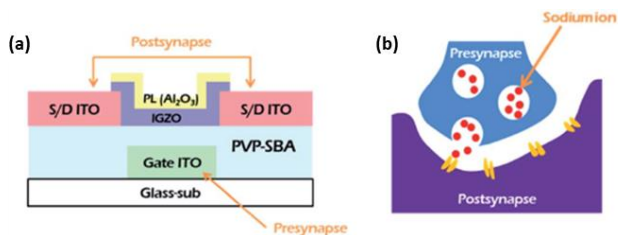


Figure 1(a) Cross-sectional view of the synapse TFT.
(b) Simplified schematic of a biological synapse.

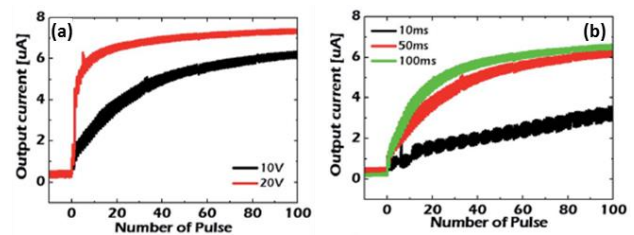


Figure 2 Output currents variations with modulating the input pulse (a) amplitudes and (b) widths.