OXIDE SEMICONDUCTOR BASED CHARGE TRAP DEVICE FOR VERTICALLY INTEGRATED NAND FLASH MEMORY

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Vertically integrated NAND flash memory (V-NAND) is the data storage component of modern hand-held electronic devices, which will also critically contribute to the futuristic devices for internet of things. The present V-NAND adopts thin poorly crystallized Si as the channel layer to minimize the cell-to-cell and device-to-device variability. However, the very low carrier (electron) mobility of such channel (only ~0.03 $cm^2/V\cdot sec$) deteriorates the device performance (write and read speed), which will eventually limit the maximum stackable number of device layers even if the various process-related issues for V-NAND fabrication are solved. An alternative channel material with amorphous structure and higher carrier mobility, therefore, is necessary for further development of V-NAND, and amorphous oxide semiconductor (AOS), such as $In_2Ga_2ZnO_7$ (IGZO) or $ZnSnO_3$ (ZTO), is an appealing contender for such application. Figure 1 shows a schematic diagram (left panel) and achieved memory performance (middle and right panels) of a double-layer stacked integrated charge trap flash (CTF) where the ZTO channel was grown by metal-organic chemical vapor deposition (MOCVD), and other Si-containing materials were grown by standard Si processes. Both top and bottom CTF devices showed feasible memory performances in the drain current – gate voltage sweep mode with sufficiently high memory window, which were also stable at 85°C guaranteeing the 10-year-retention time. However, the program time, estimated in pulse program/erase mode, was impractically long (order of sec.) suggesting that there must be significant improvements in material stack or process conditions. The relatively thick tunneling oxide (4nm SiO_2) may seriously limit the electron tunneling, but thinner SiO_2 could not guarantee sufficient retention time.
In the presentation, the material and integration strategies to improve such problem will be discussed. These strategies include AOS material variation (IGZO vs. ZTO), process method (sputtering vs. MOCVD), and integration schemes (tunneling oxide thickness and thermal treatments), of which details are dependent on the AOS material and process methods.

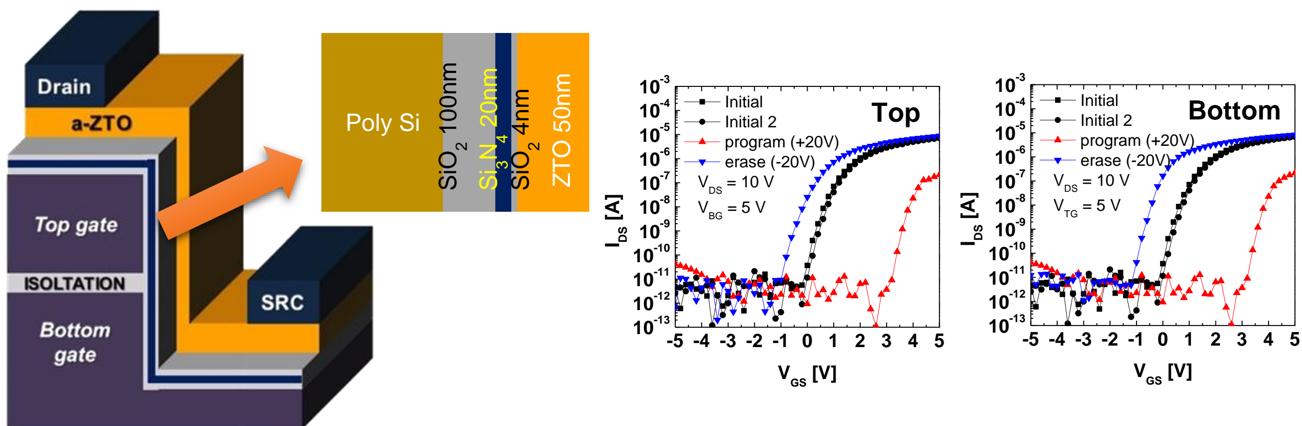

Figure 1 – Schematic diagram of double layer stacked CTF (Left panel), and I_{DS}-V_{GS} performance of top (middle panel) and bottom (right panel) devices