RECENT KEY DEVELOPMENTS IN NANOSCALE RELIABITY AND FAILURE ANALYSIS TECHNIQUES FOR ADVANCED NANOELECTRONIC DEVICES

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Last decade has witnessed an aggressive scaling of CMOS technology nodes pushing it all the way down to sub-10nm and this scaling trend looks positive for the next two-three nodes as well down to 5nm. This push for scaling of the technology node has created a need for using material characterization techniques with (sub)nanometer probe resolution to characterize these advanced nanoelectronic devices - to observe and understand the underlying thermodynamics and kinetics of the physical phenomenon at the nanometer scale in real-time. Among these advanced characterization techniques, transmission election microscopy (TEM) and scanning probe microscopy (SPM), as well as the techniques derived from these, have become critical and instrumental to failure analysis and for evaluation of key design metrics for reliability studies. In this work, we present the different case studies using these two techniques which we have employed for studying both advanced logic and memory devices.

High resolution TEM (HRTEM) has been used for both RRAM and gate oxide reliability studies due to its multiple compositional characterization capabilities with sub-nm resolution. TEM can routinely achieve a resolution around 0.1nm and thus can provide tremendous information related to structure (Diffraction Pattern) and composition (Electron Energy Loss Spectroscopy). *Ex-situ* TEM techniques (supported by Focused Ion Beam (FIB)) have allowed us to perform diverse electrical and thermal testing on devices. We have found concrete evidence of FinFET device degradation recently [1]. We have also employed *in-situ* TEM techniques (facilitated by scanning tunneling microscopy (STM) and the thermal holder) to observe the degradation behavior of metal-dielectric stacks in real-time [2]. The *in-situ* TEM technique has provided insight into the direct and solid time sequential evolution of failure behavior in RRAM devices. Additionally, 3D tomography characterization of the defect and failure spot has been acquired by tilting the sample and collecting the sequential images at different angles [3]. This technique of 3D tomography is a very powerful one for defect reorganization and for root cause analysis of failure mechanism.

Conductive atomic force microscopy (CAFM) and STM are two techniques, belonging to a large pool of available SPM tools, which we have used for breakdown studies in ultra-thin HfO_2 and other high-κ dielectrics as well as multi-layered fluorinated graphene (FG) stacks. With a resolution, down to ~10nm and ~0.1nm for CAFM and STM respectively under ultra-high vacuum (UHV) conditions, we have applied these tools to measure electrical properties (*I-V* and *dI/dV*) at grain and grain boundary spots in ultra-thin polycrystalline HfO_2 dielectrics [4] as well as to understand the breakdown mechanism in FG stacks [5]. We have also explored the local spectroscopy capabilities (of both STM and CAFM) for the measurement of random telegraph noise (RTN) in blanket HfO_2 films. Using bias dependent RTN measurements, it has been possible to quantify the position of the defect in the probed location of the dielectric. Interestingly, these dielectric breakdowns and RTN measurements at the nanoscale have also provided experimental evidence of defect clustering in polycrystalline dielectrics and possible existence of the metastable nature of oxygen vacancy (V_O) defect in HfO_2 respectively [6]. CAFM has also been explored to study the role of V_O in HfO_2 based RRAM stacks for ultra-low power memory applications where the signature of sub-quantum conductance based resistive switching has been experimentally observed [7].

We strongly believe that these tools and techniques would play an indispensable role in unveiling the underlying physics of the nanoscale physical phenomenon for existing as well as emerging materials and 2D/3D devices.

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