International Conference on Semiconductor Technology for Ultra-Large Scale Integrated Circuits and Thin Film Transistors VI (ULSIC vs TFT 6)

Proceedings

5-25-2017

Thin film transistor modeling: Frequency dispersion

Michael Shur
Rensselaer Polytechnic Institute, USA

Recommended Citation

Michael Shur, "Thin film transistor modeling: Frequency dispersion" in "International Conference on Semiconductor Technology for Ultra-Large Scale Integrated Circuits and Thin Film Transistors VI (ULSIC vs TFT 6)", Yue Kuo (Texas A&M University, USA) Olivier Bonnaud (University of Rennes I, France) Eds, ECI Symposium Series, (2017). http://dc.engconfintl.org/ulsic_tft_6/4

Thin film transistor modeling: frequency dispersion

Michael Shur

Rensselaer Polytechnic Institute
Troy, New York 12180-3590, USA

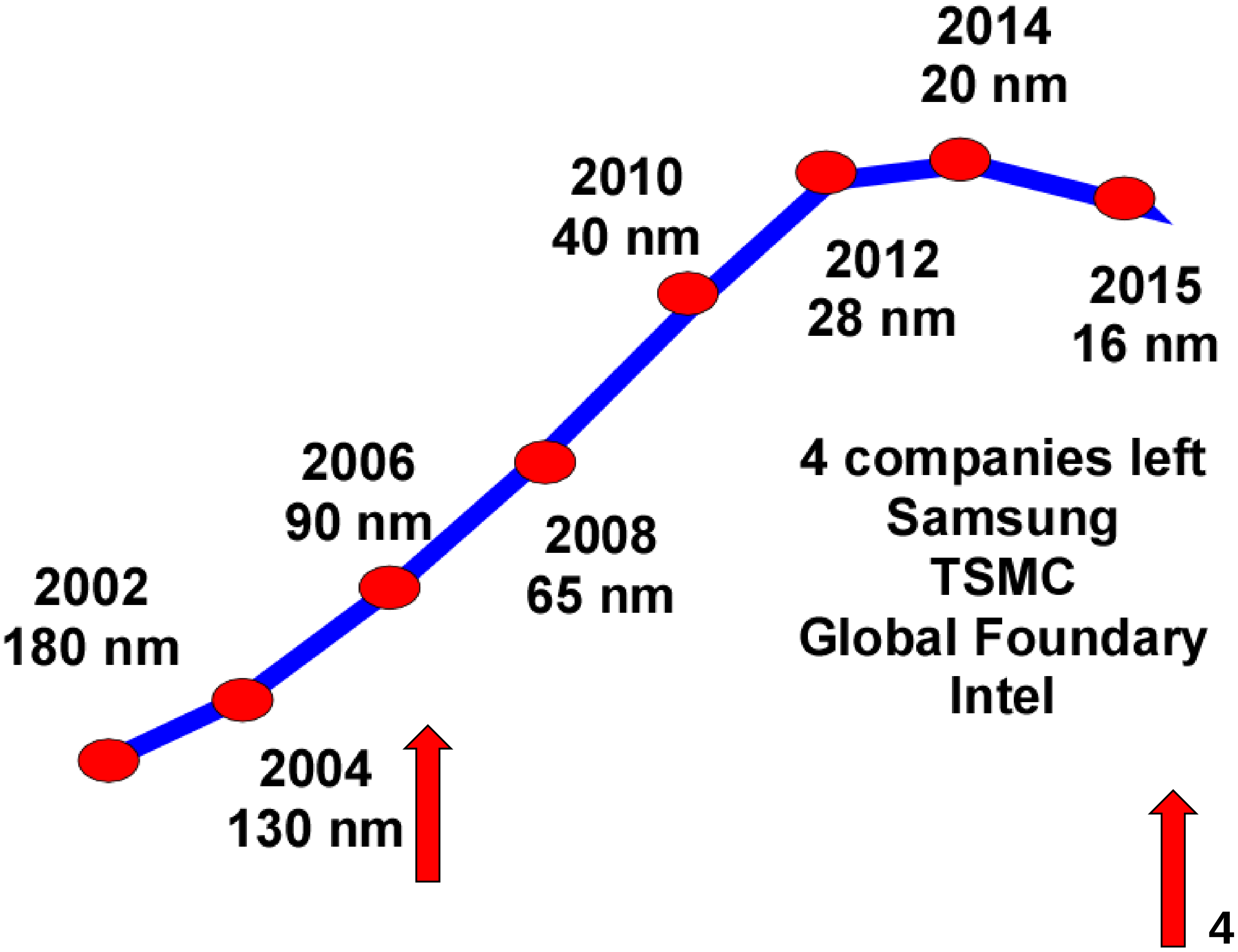
Presented at
International Conference on Semiconductor Technology
for Ultra Large Scale Integrated Circuits and Thin Film Transistors
Vienna, Austria
May 25, 2017

Outline

- Motivation
- Compact model challenges
- Effective medium approach
- Current-voltage characteristics
  - UCCM
  - Advanced (non-ideal and contact effects)
- Capacitance-voltage characteristics and Dispersion
- Sensing applictions
- Noise
- Conclusions

Michael Shur (shurm@rpi.edu)

Cost of x-Si transistors going up



4 companies left
Samsung
TSMC
Global Foundary
Intel

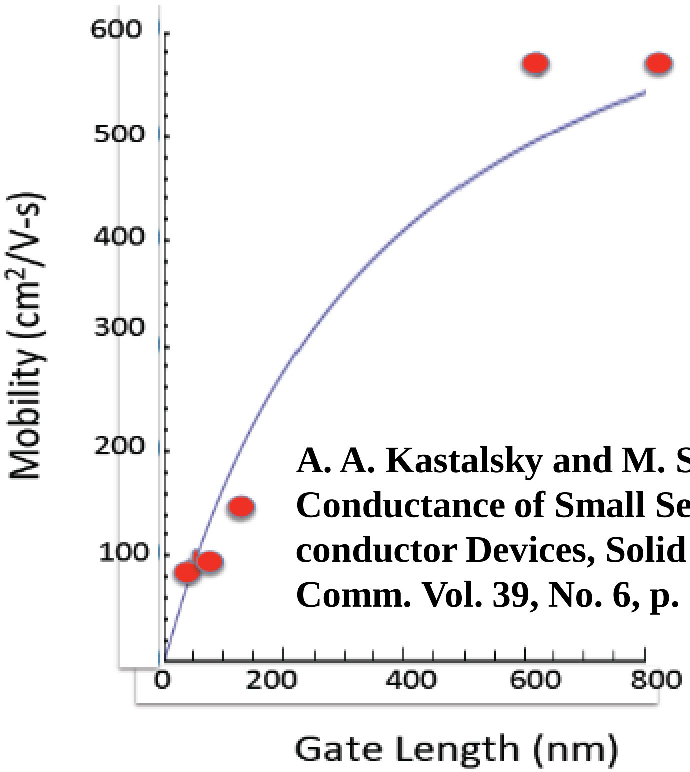
22 companies compete
($2B cost of entry)

4 companies
left ($7B cost of
entry)

Michael Shur (shurm@rpi.edu)

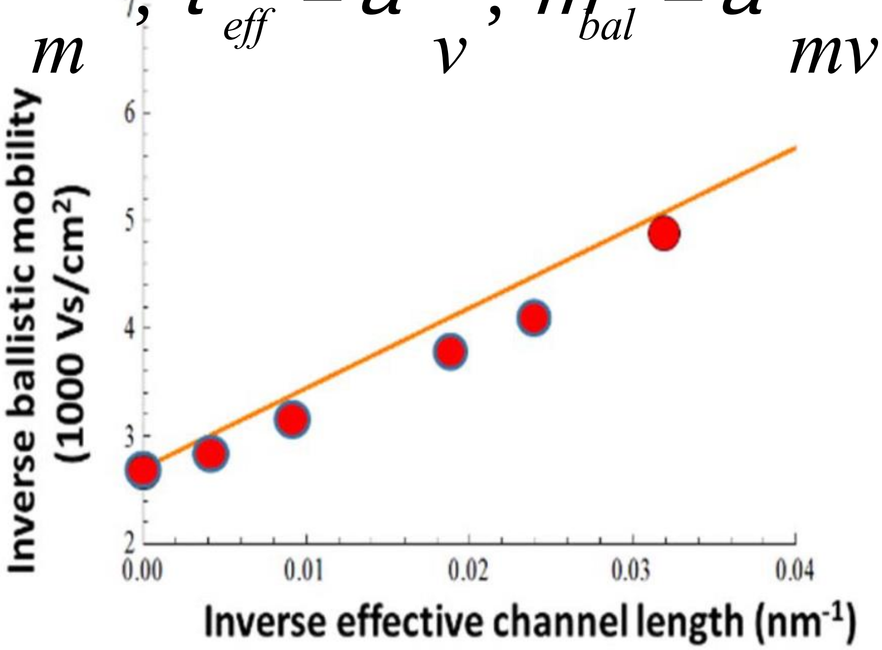
Ballistic mobility in Si

$$\mu_{bal} = \frac{e\tau_{eff}}{m};\ \tau_{eff} = a\frac{L}{v};\ \mu_{bal} = a\frac{eL}{mv}$$



A. A. Kastalsky and M. S. Shur, Conductance of Small Semi-conductor Devices, Solid State Comm. Vol. 39, No. 6, p. 715-718 (1981)

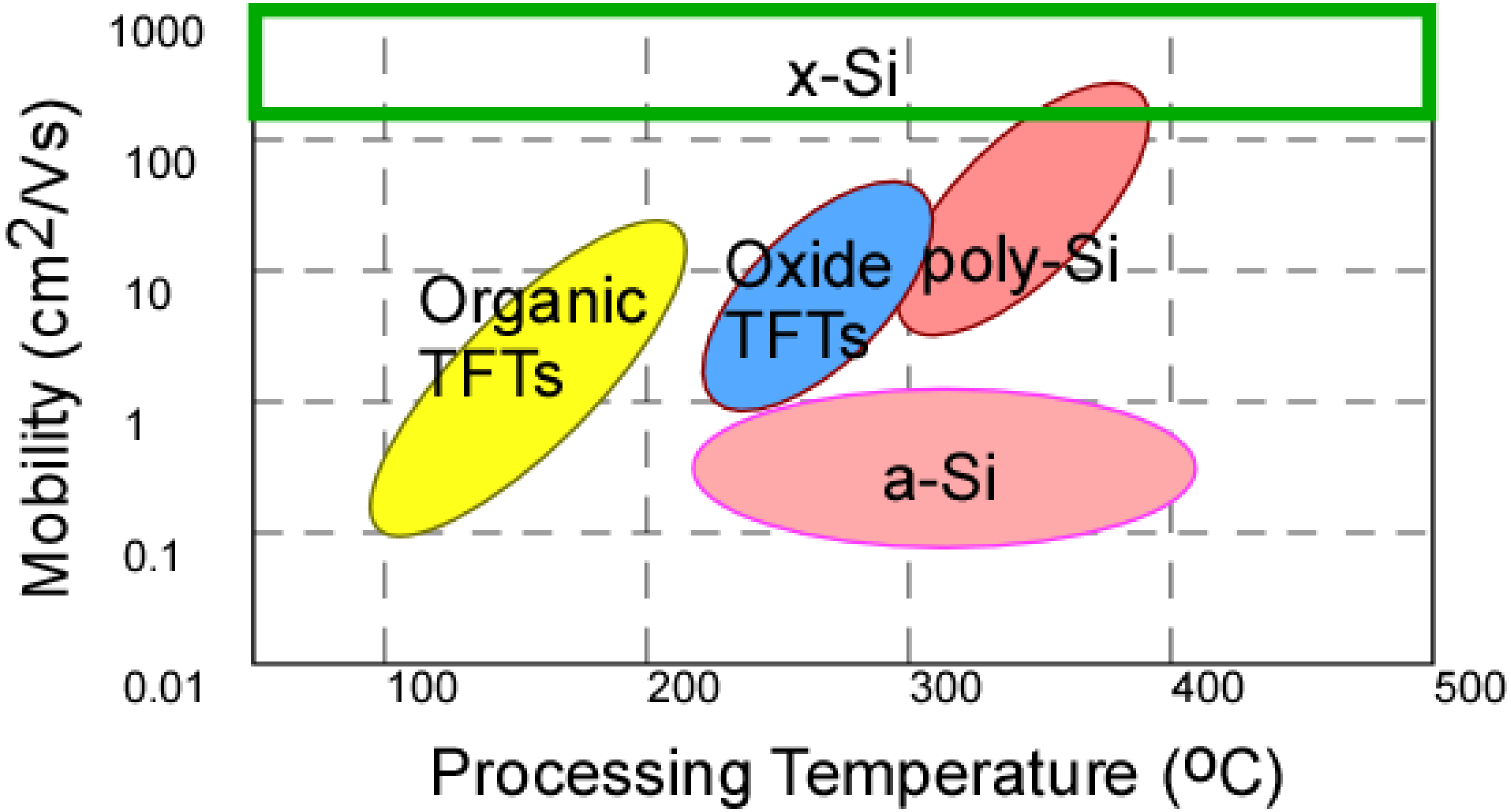
Data from W. Knap, F. Teppe, Y. Meziani, N. Dyakonova, J. Lusakowski, F. Bouef, T. Skotnicki, D. Maude, S. Rumyantsev and M. S. Shur, Appl. Phys. Lett, Vol. 85, No 4, pp. 675-677 (2004)



D. Antoniadis, IEEE Transactions on Electron Dev. Vol. 63, No 7, pp. 2650 – 2656 (2016) DOI: 10.1109/TED.2016.2562739

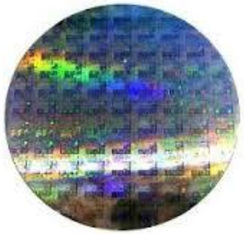
F. Ferdousi, R. Rios, and K. J. Kuhn, Solid-State Electron., vol. 104, pp. 44–46, Feb. 2015.

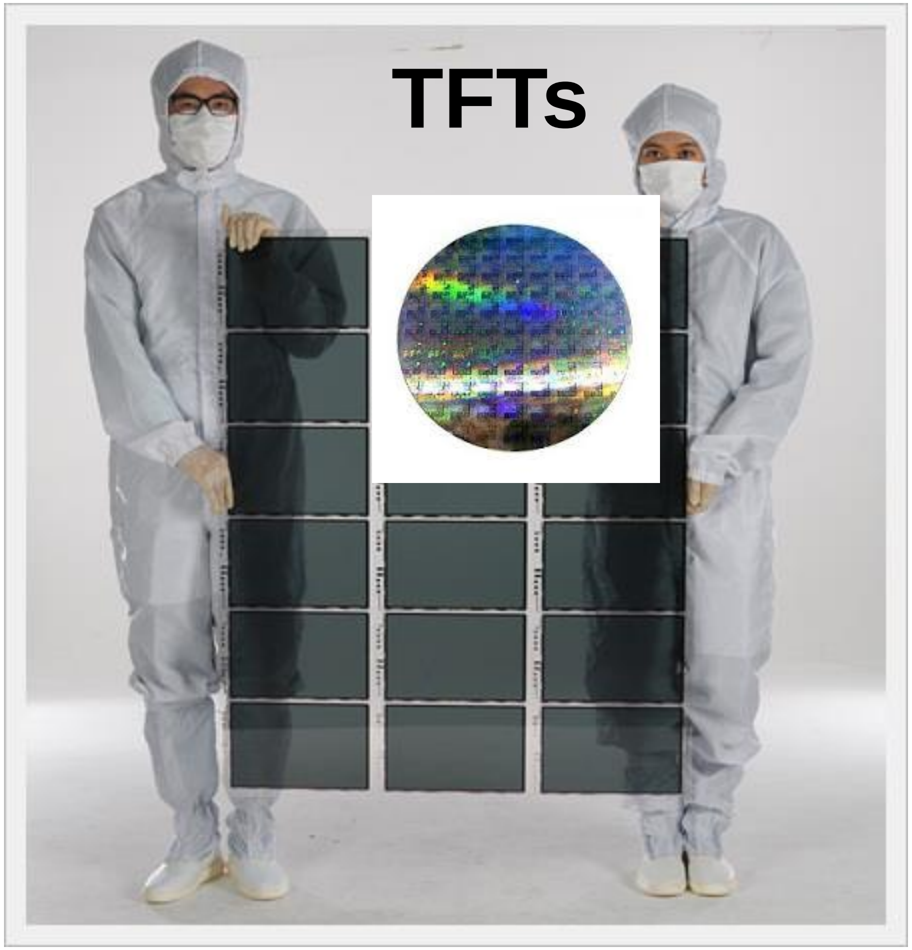
TFT Field Effect Mobility



FETs and TFTs

X-Si

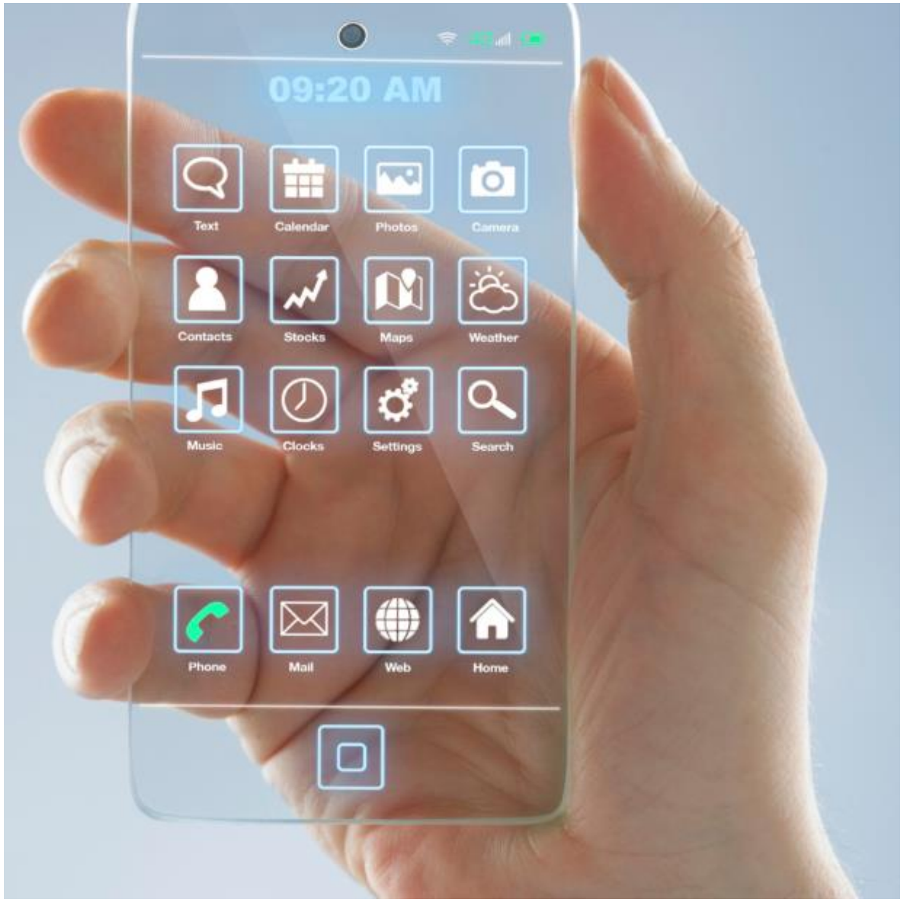




TFTs

From http://www.tradekorea.com/product/detail/P293787/TFT-LCD-Glass-Slimming.html

See-through $1 smart phone



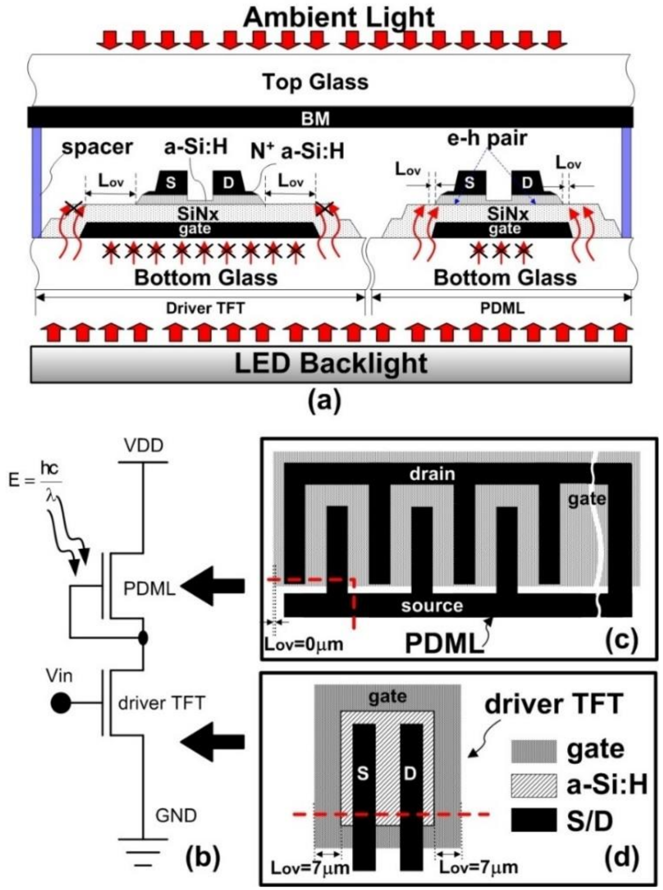
From https://futurephones2000.wordpress.com/

TFTs could be on flexible substrates for robotics applications

Michael Shur (shurm@rpi.edu)

Challenges to TFT Compact Modeling from Applications

- **Higher resolution, interactive displays**
- **Higher speed for RFIDs and sensors**
- **Low temperature processing for flexible electronics, and computers on glass**



PushingTFT designs to the limits with less ideal characteristics – challenge for compact modeling

S. H. Jin, M.-S. Park, and M. S Shur, Photosensitive Inverter and Ring Oscillator with Pseudo Depletion Mode Load for LCD Applications, IEEE Electron Device Letters, Vol. 30, Issue 9, pp. 943 – 945, September (2009)

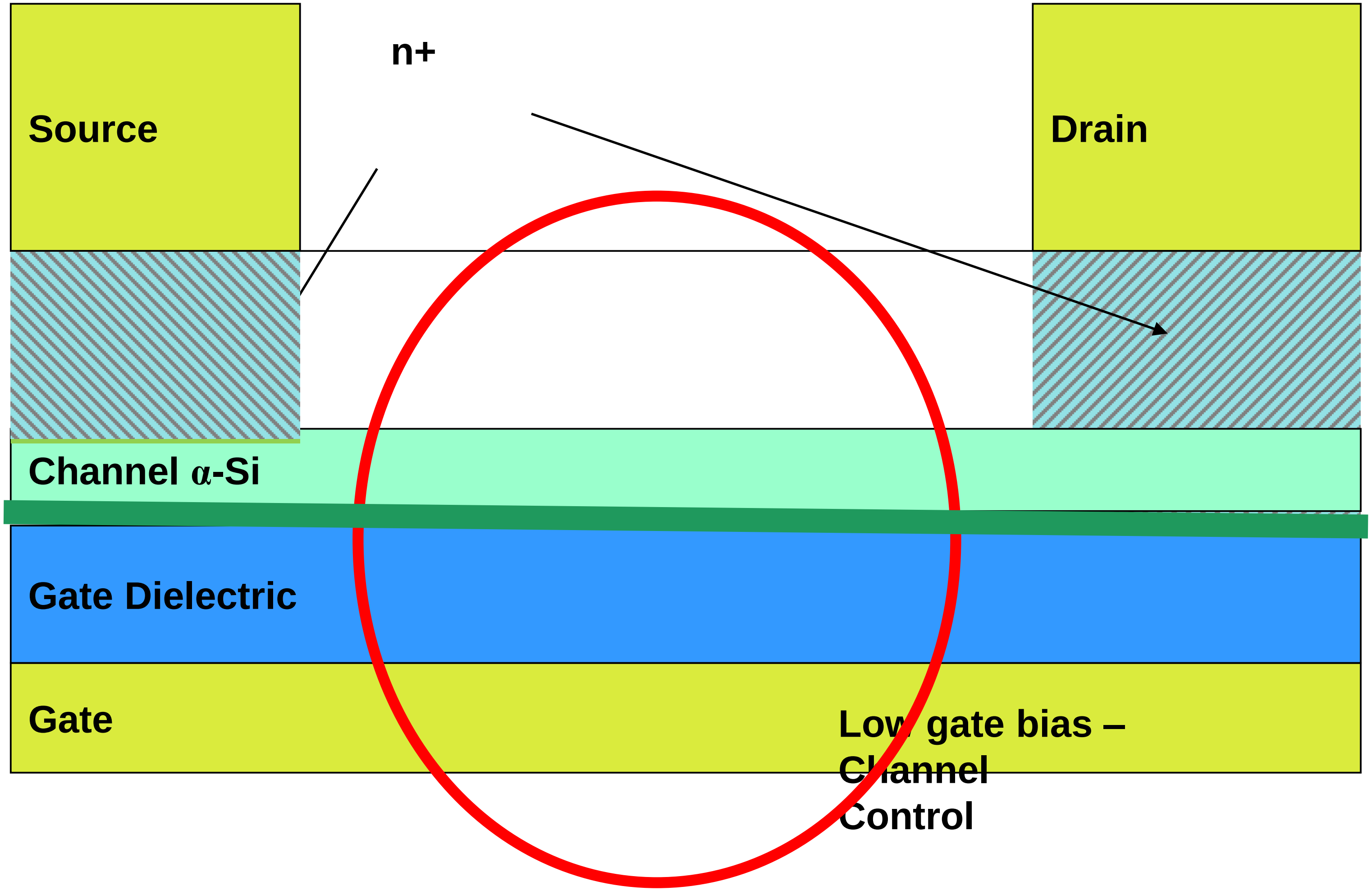
TFT Modeling: Challenges

- Different device sections (intrinsic channel versus contacts) dominate depending on bias and/or temperature
- Parameter variations from device to device
- Non trivial scaling
- **<u>Dispersion</u>**
- Noise

Effective medium approach and Unified Charge Control Model (UCCM)

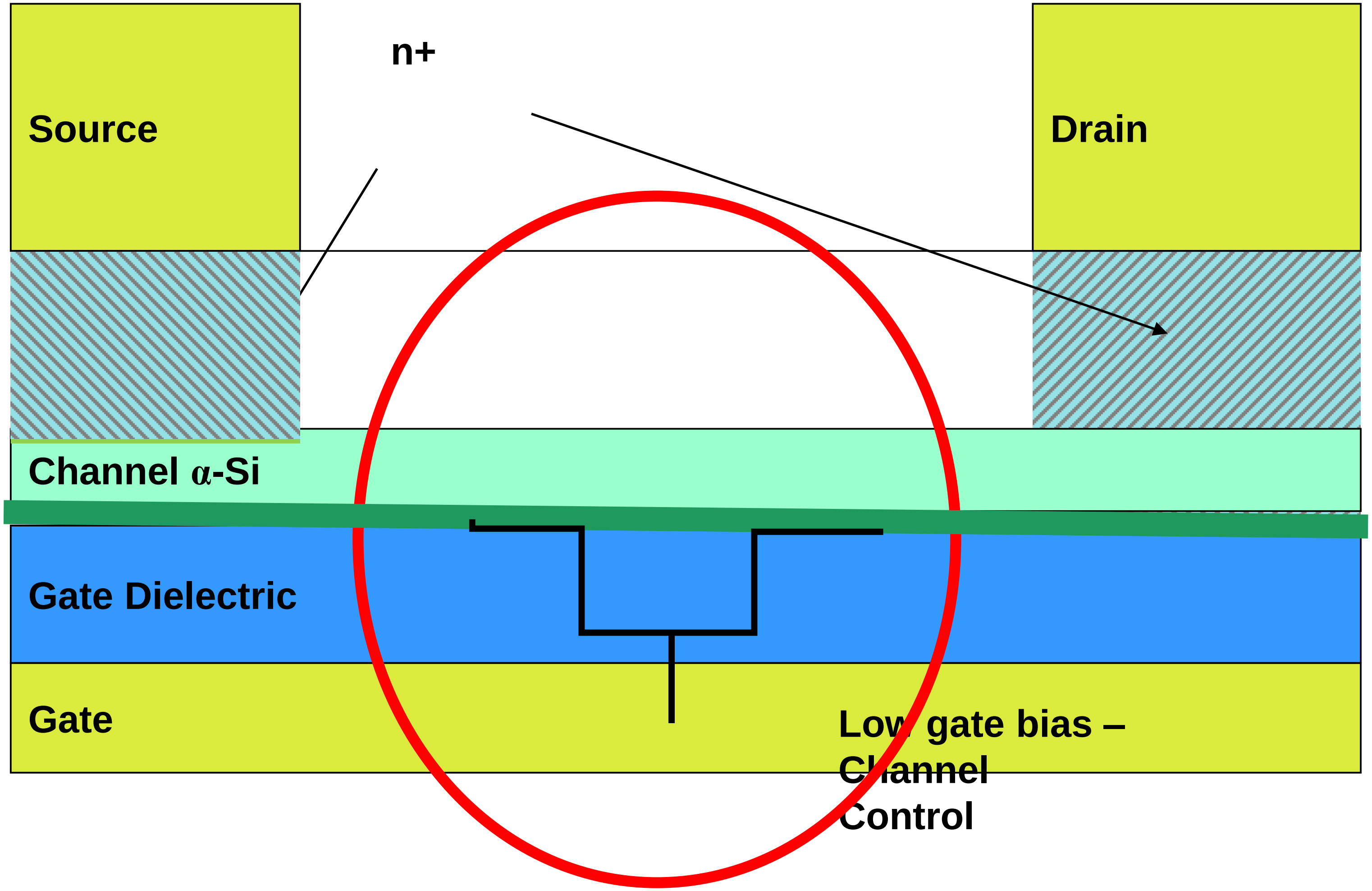
TFT layout and circuit elements

High gate bias –
Contact
Control



Low gate bias –
Channel
Control

TFT layout and circuit elements



n+

High gate bias –
Contact
Control

Source

Drain

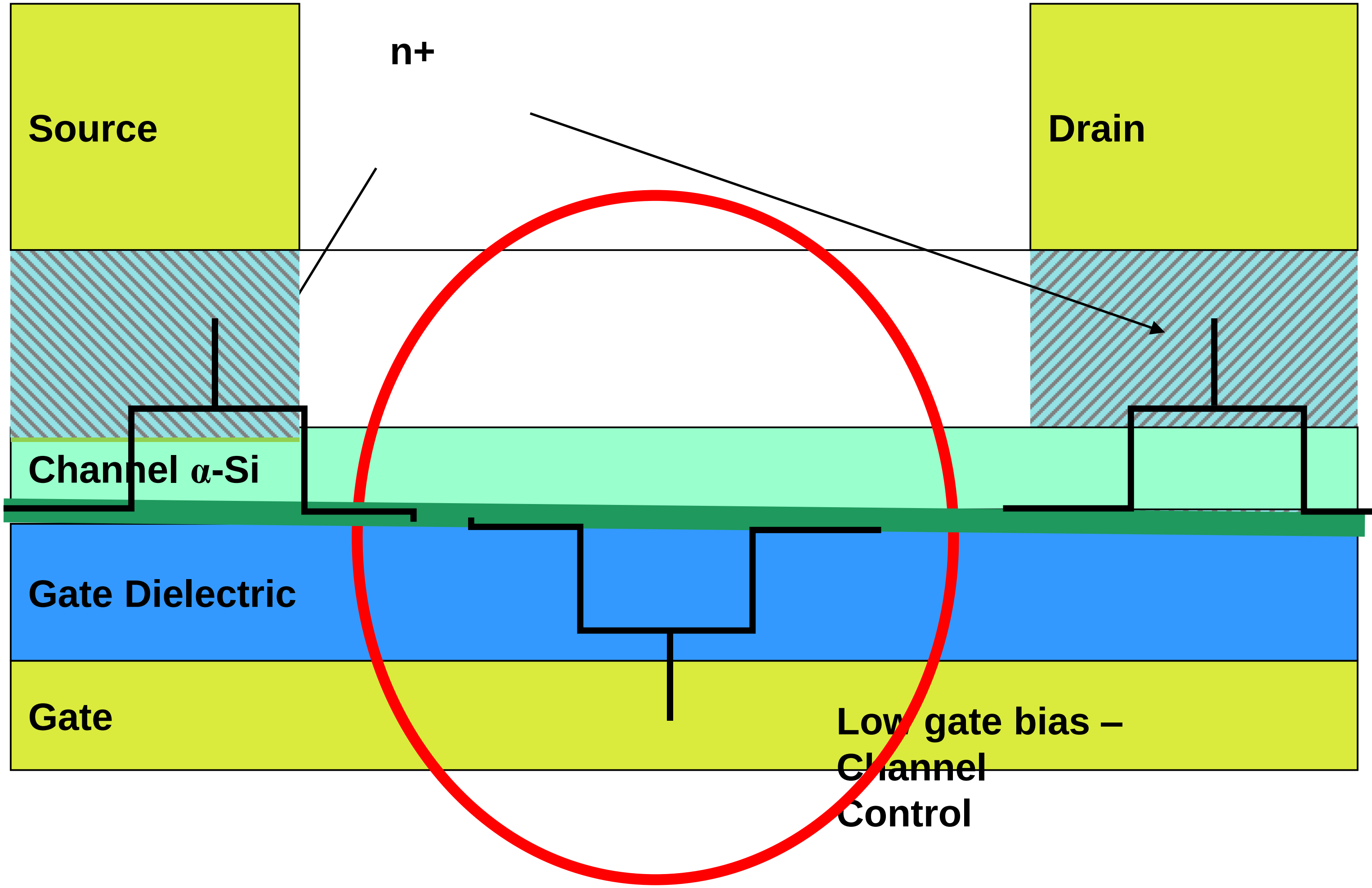
Channel α-Si

Gate Dielectric

Gate

Low gate bias –
Channel
Control

TFT layout and circuit elements



High gate bias – Contact Control

n+

Source

Drain

Channel α-Si

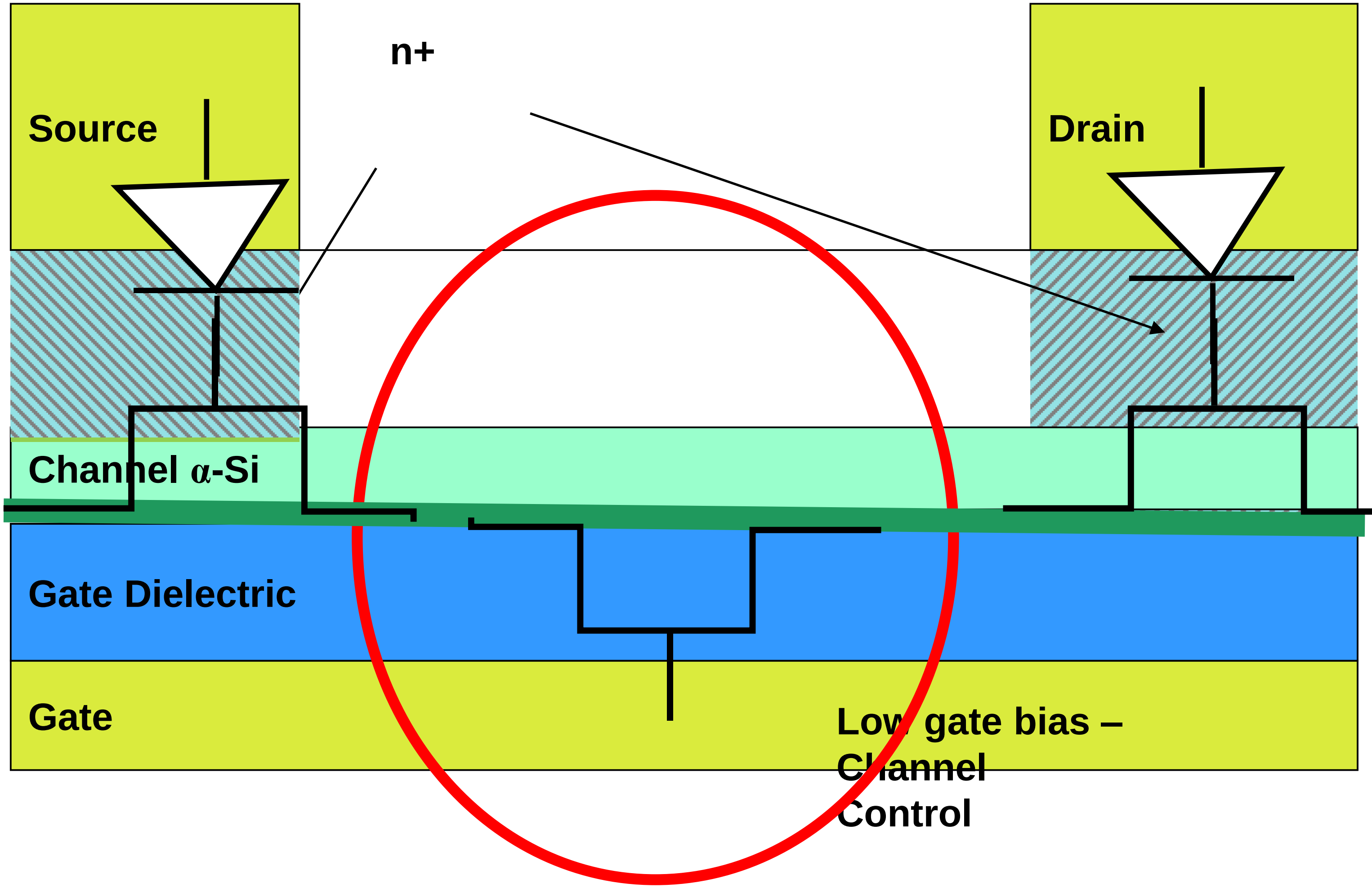
Gate Dielectric

Gate

Low gate bias – Channel Control

TFT layout and circuit elements

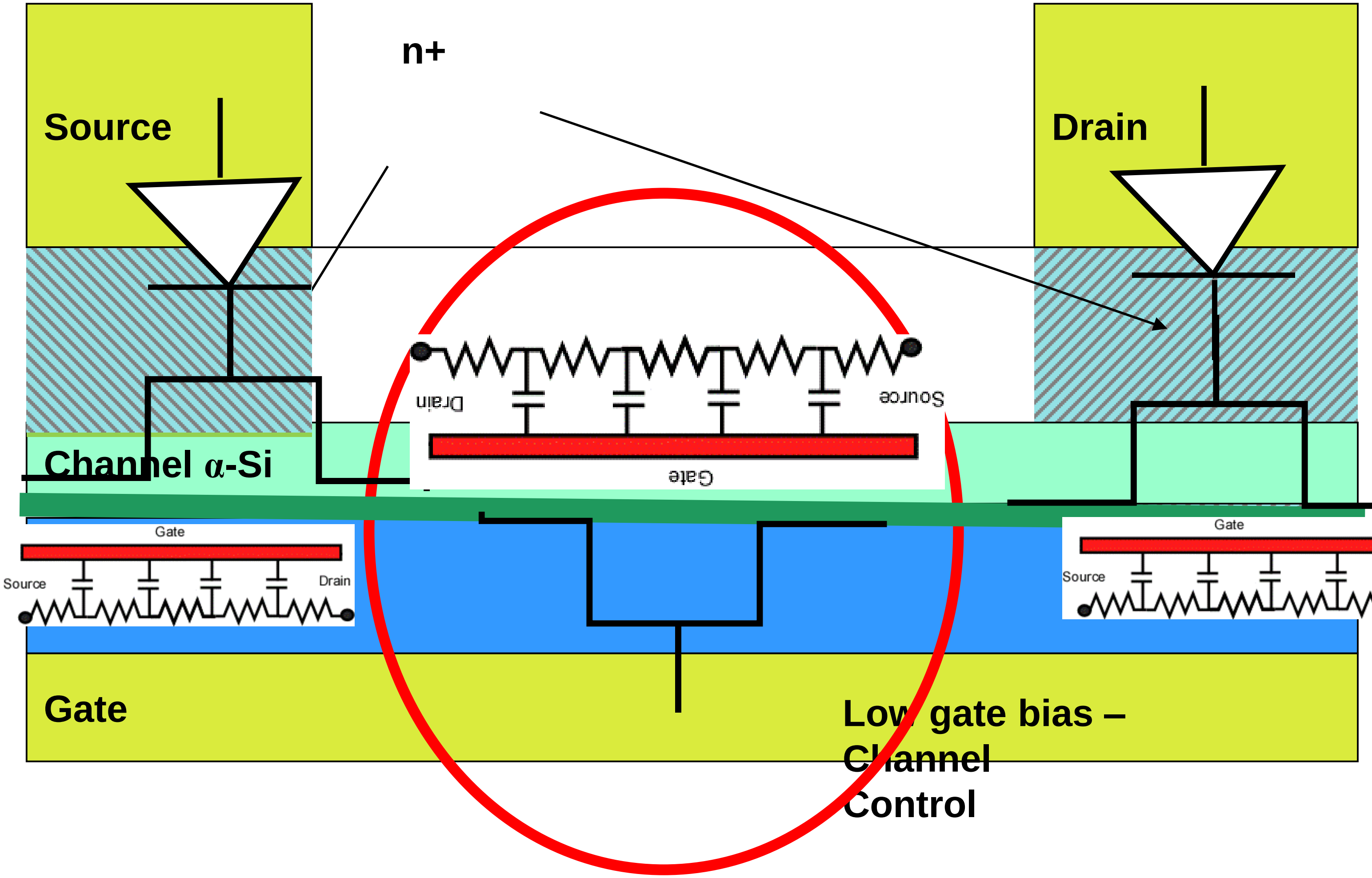
High gate bias –
Contact
Control



Low gate bias –
Channel
Control

TFT layout and circuit elements

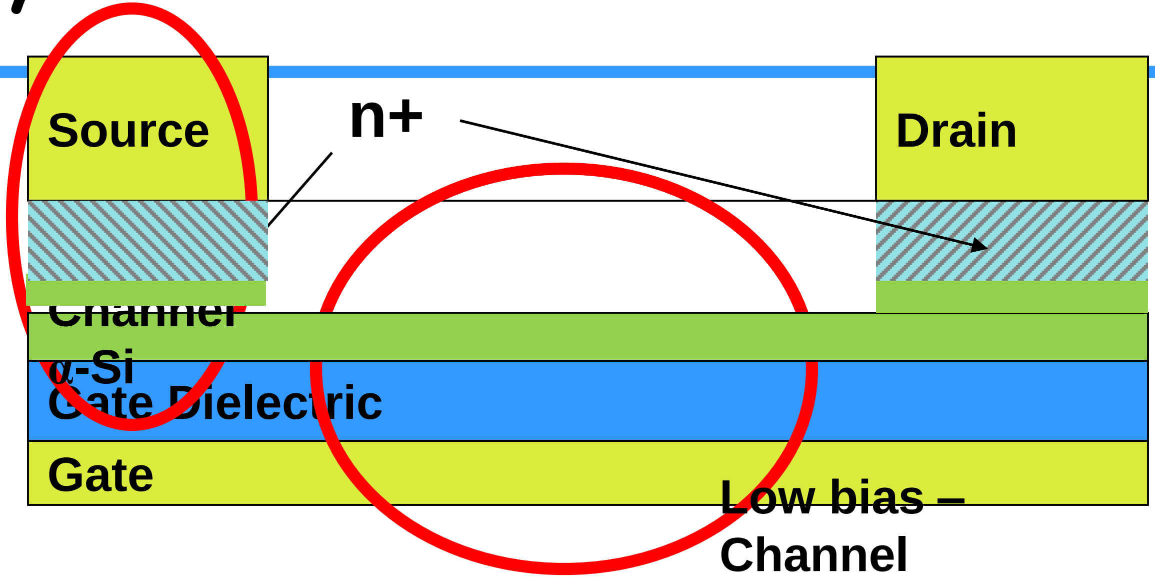
High gate bias –
Contact
Control



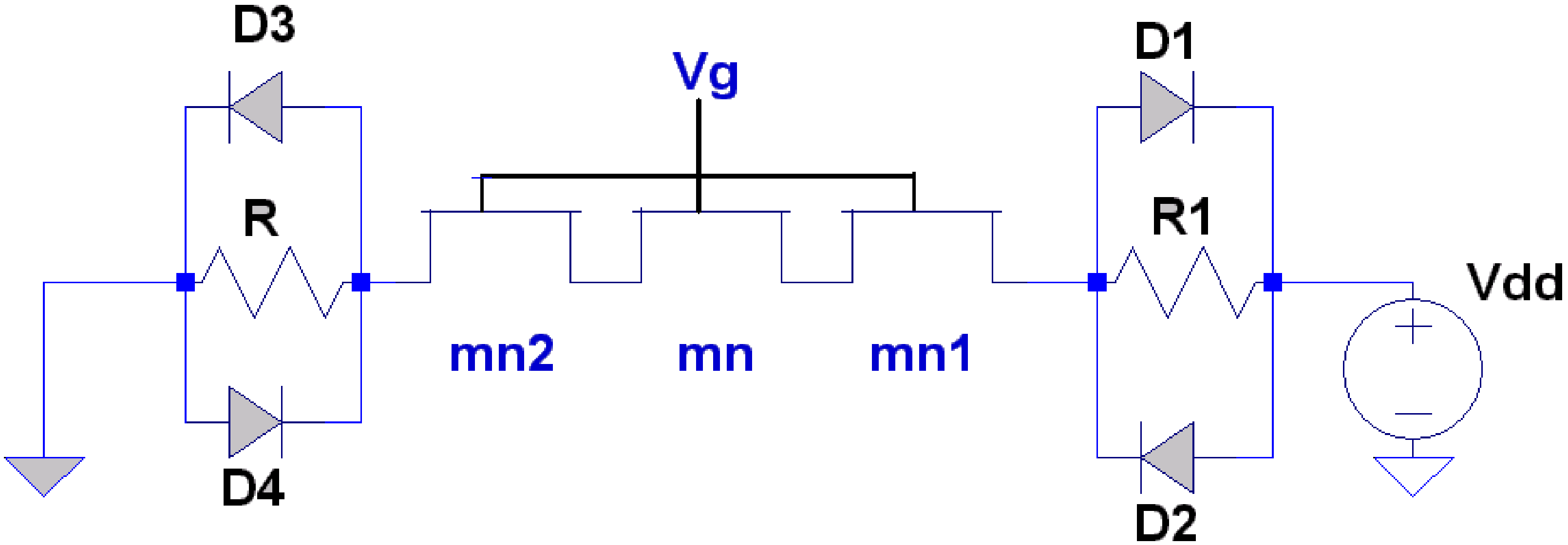
Low gate bias –
Channel
Control

TFT layout and circuit elements

High bias – Contact Control



Low bias – Channel Control

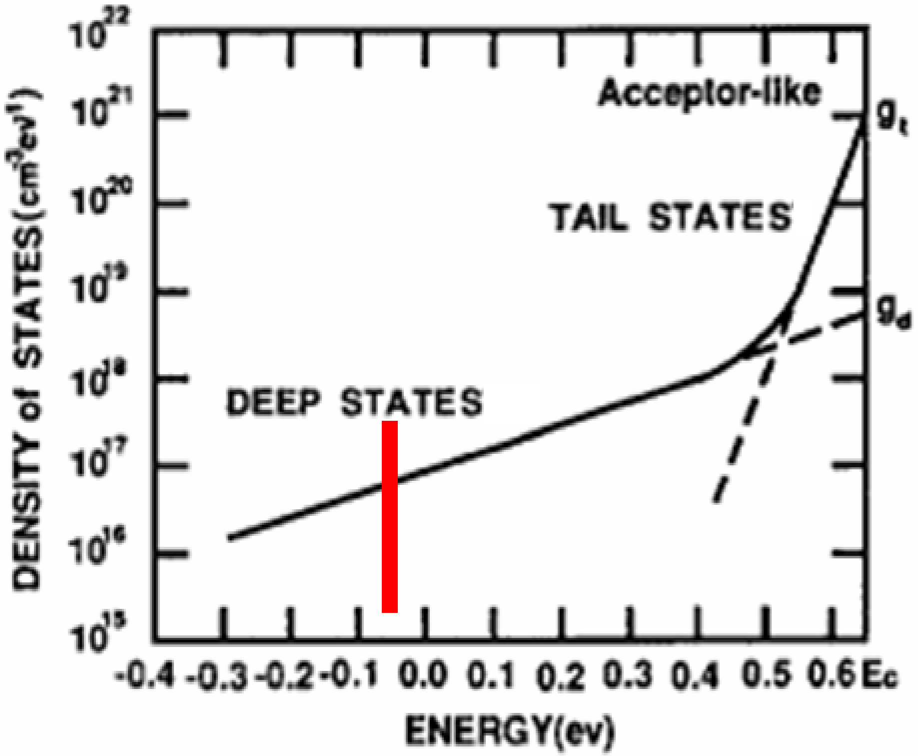


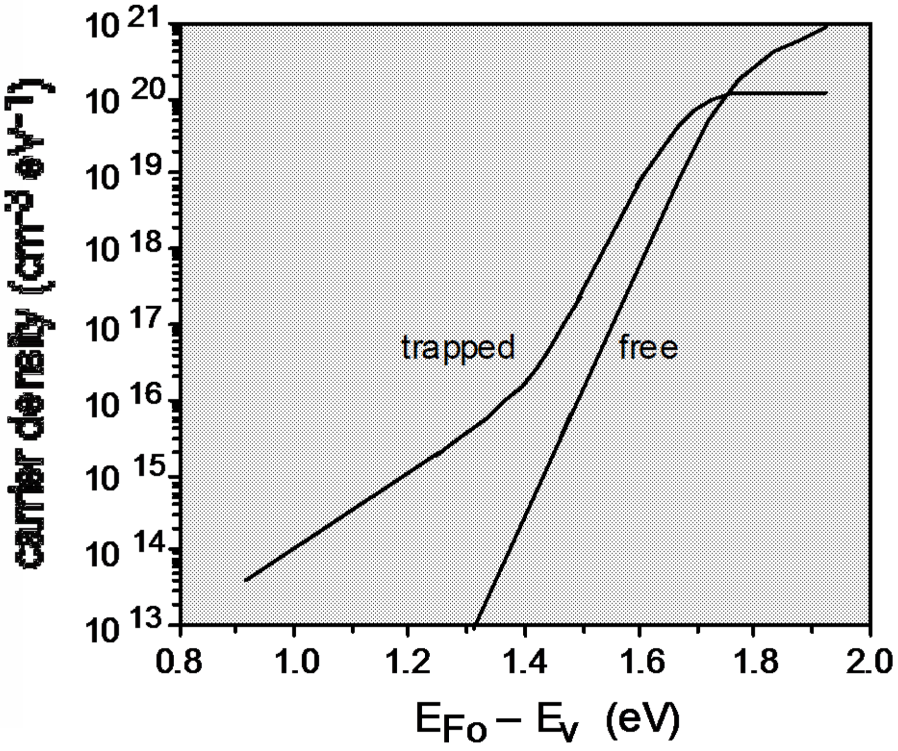
TFT Modeling: Goals

Good modelers

Michael Shur (shurm@rpi.edu)

Deep and tail localized states

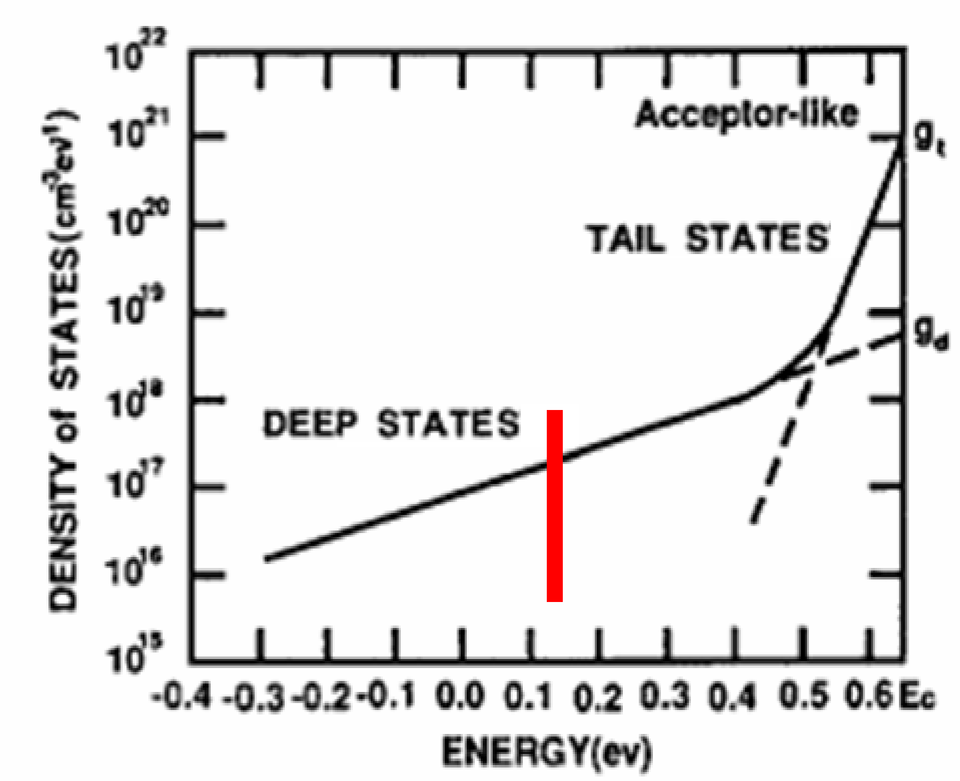


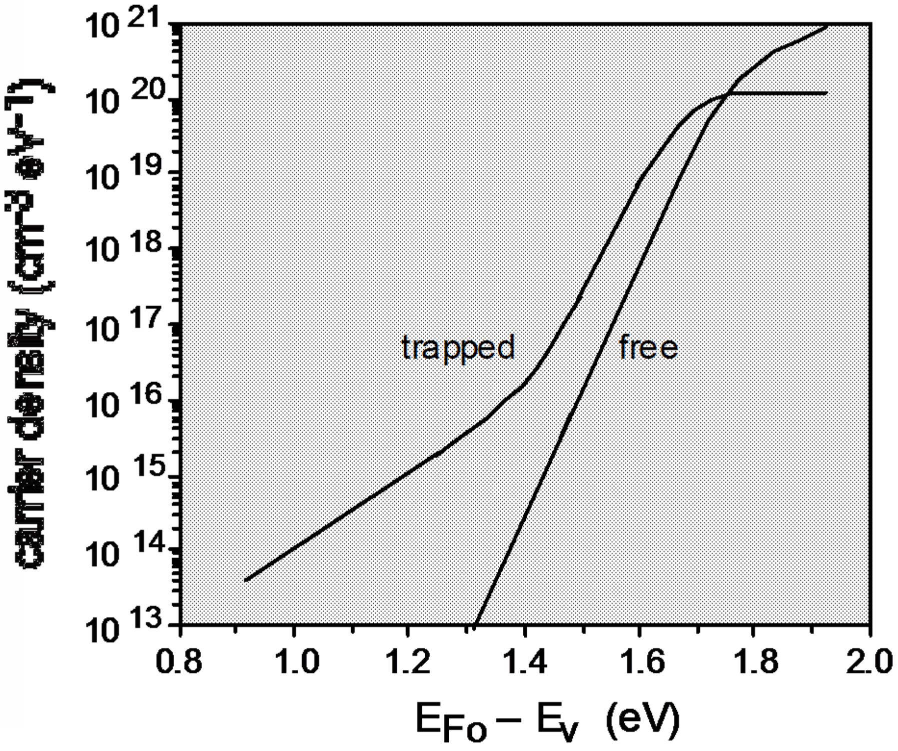


$$g(E) = g_d \exp\left(\frac{E - E_C}{kT_d}\right) + g_t \exp\left(\frac{E - E_C}{kT_t}\right)$$

M. Shur and M. Hack, "Physics of amorphous silicon based alloy field effect transistors," *J.* Appl. *Phys.,* vol. *55,* no. I I , pp. 3831-3842, May 1984.

Deep and tail localized states

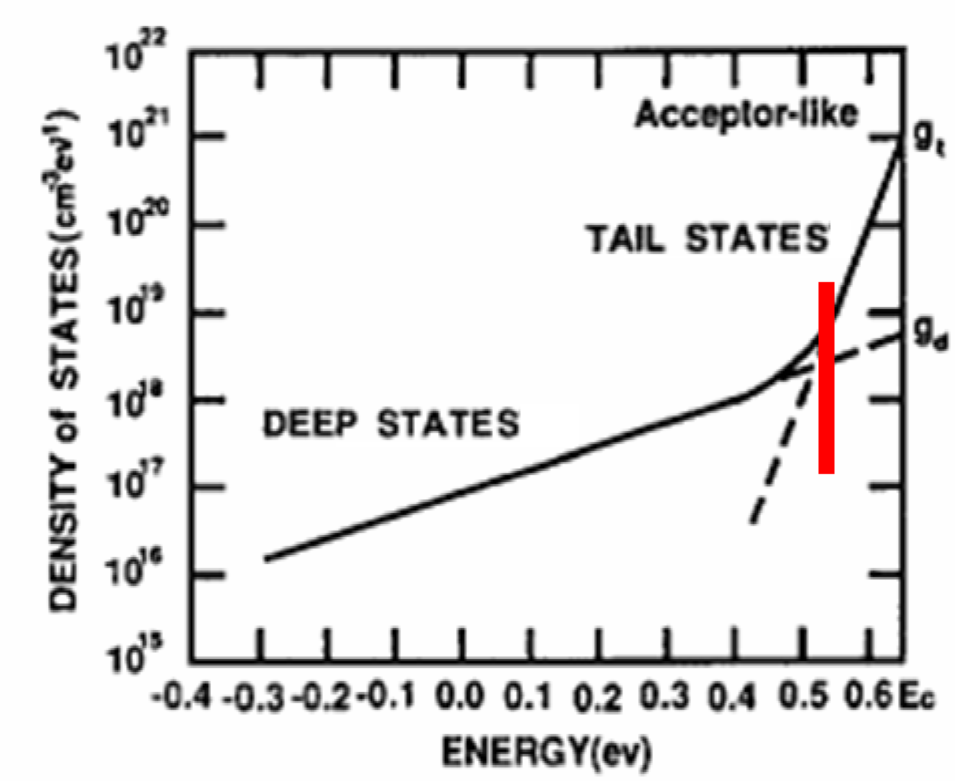


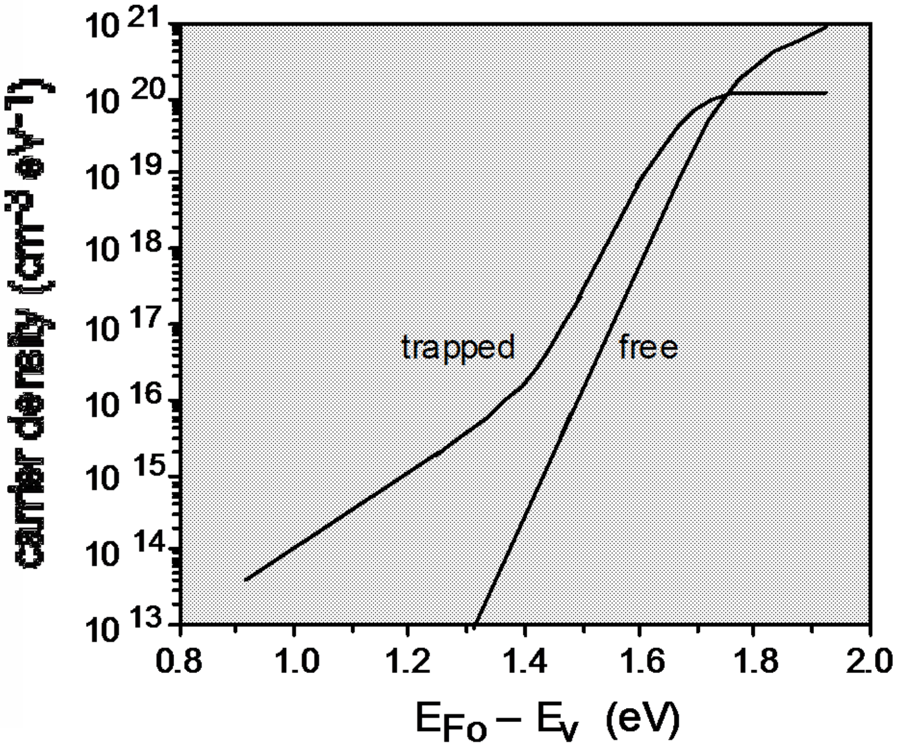


$$g(E) = g_d \exp\left(\frac{E - E_C}{kT_d}\right) + g_t \exp\left(\frac{E - E_C}{kT_t}\right)$$

M. Shur and M. Hack, "Physics of amorphous silicon based alloy field effect transistors," *J.* Appl. *Phys.,* vol. *55,* no. I I , pp. 3831-3842, May 1984.

Deep and tail localized states

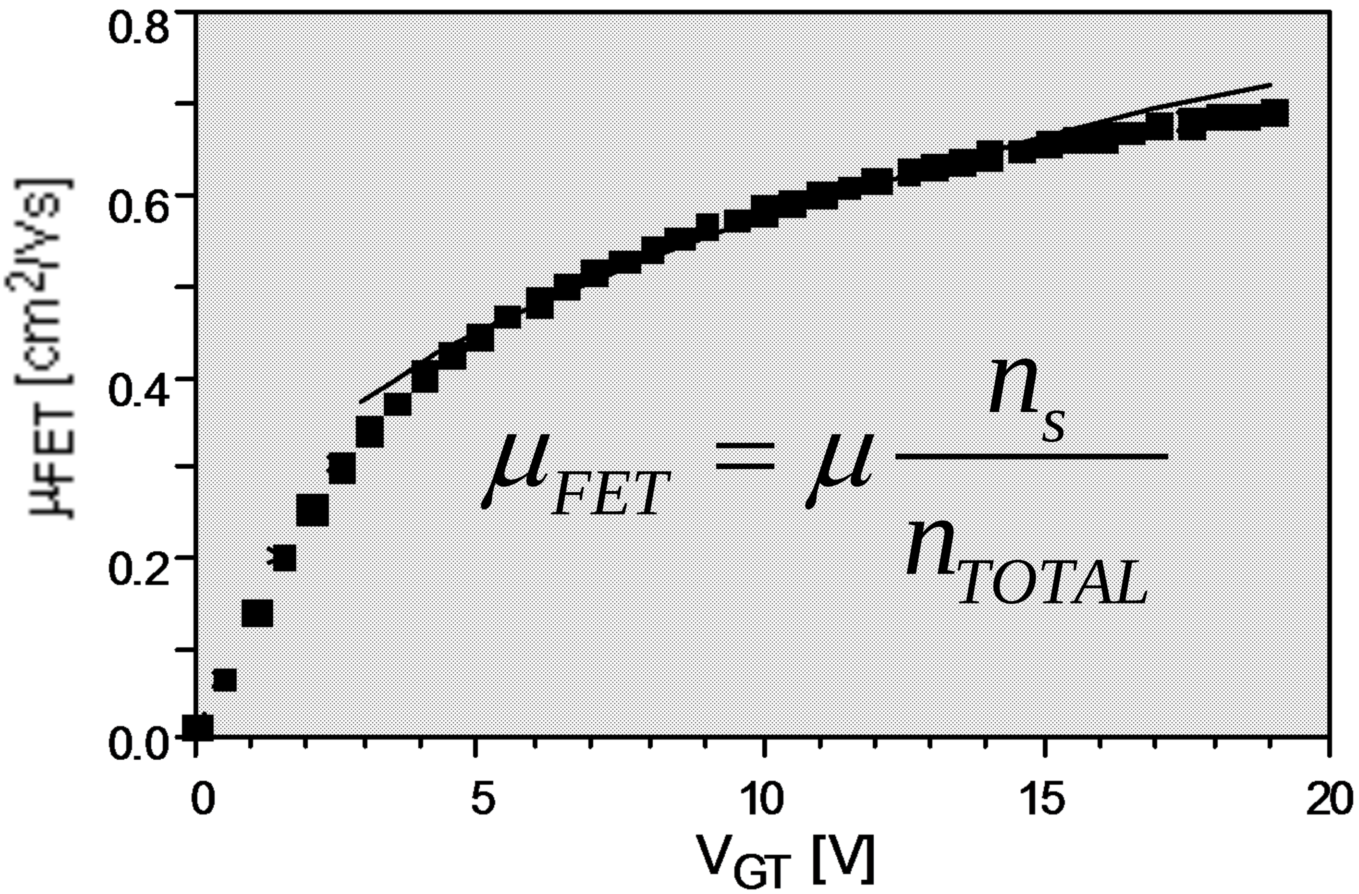




$$g(E) = g_d \exp\left(\frac{E - E_C}{kT_d}\right) + g_t \exp\left(\frac{E - E_C}{kT_t}\right)$$

M. Shur and M. Hack, "Physics of amorphous silicon based alloy field effect transistors," *J.* Appl. *Phys.,* vol. *55,* no. I I , pp. 3831-3842, May 1984.

Field Effect Mobility vs, Gate Voltage Swing



$$\mu_{FET} = \mu \frac{n_s}{n_{TOTAL}}$$

Field effect mobility vs gate bias

The field effect mobility is the effective mobility that links channel transport to the MOS capacitor properties:

$$\frac{\mu_{fet}}{\mu_0} = \frac{N_{free}}{N_{free} + N_{loc}}$$

$$\frac{1}{\mu_{fet}} = \frac{1}{\mu_0} + \frac{1}{\mu_1 \cdot \left(\frac{2qV_{gte}}{\eta_f kT} \right)^{m_\mu}}, \quad V_{gte} = \eta \frac{kT}{q} \left(1 + \frac{\alpha_{sat} q V_{gt}}{2\eta kT} + \sqrt{\Delta^2 + \left[\frac{\alpha_{sat} q V_{gt}}{2\eta kT} \right]^2} \right)$$

RPI TFT model

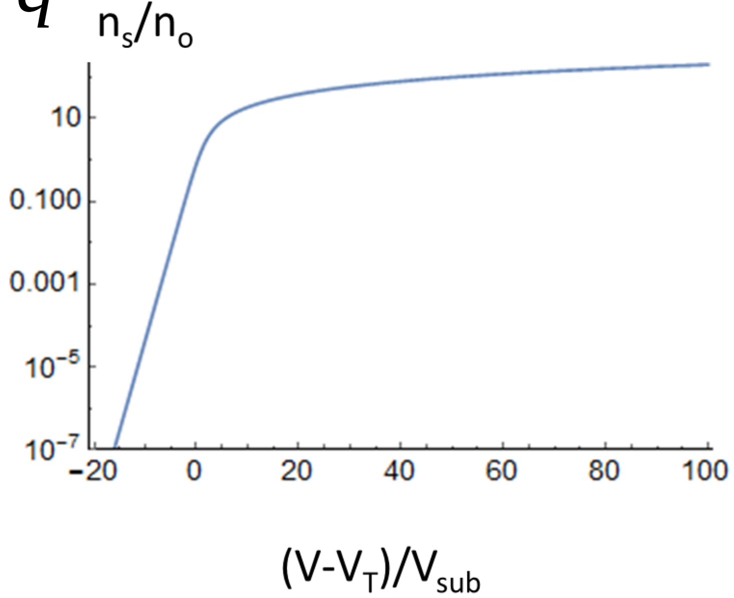
M. Shur and M. Hack, "Physics of amorphous silicon based alloy field effect transistors," *J.* Appl. *Phys.,* vol. *55,* no. I I , pp. 3831-3842, May 1984.

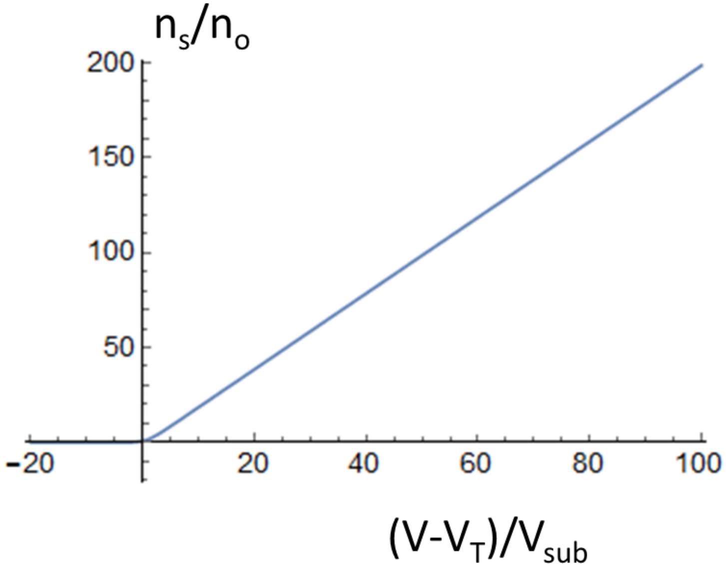
Unified Charge Control Model

$$V_{GS} - V_T = \boxed{q\left(n_s - n_o\right)/c_a} + V_{sub}\ln\left(\frac{n_s}{n_o}\right)$$

$$V_{sub} = \eta\frac{k_B T}{q}$$

ABOVE THRESHOLD



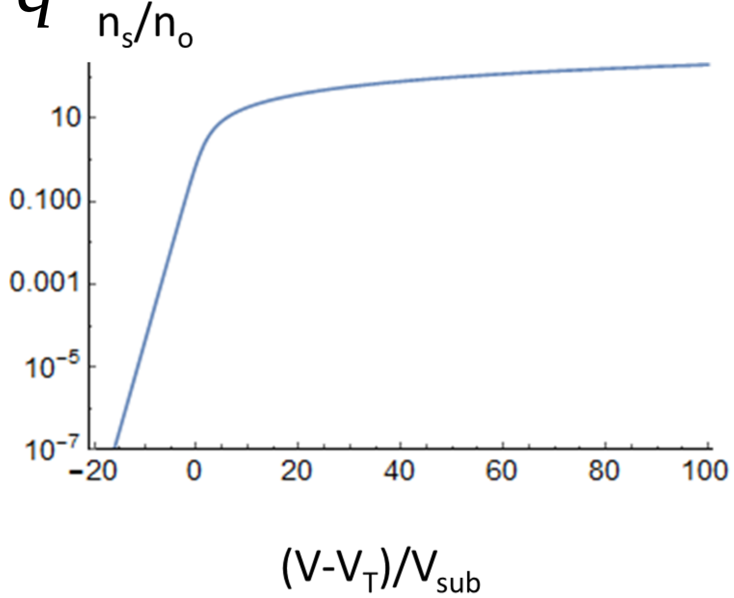


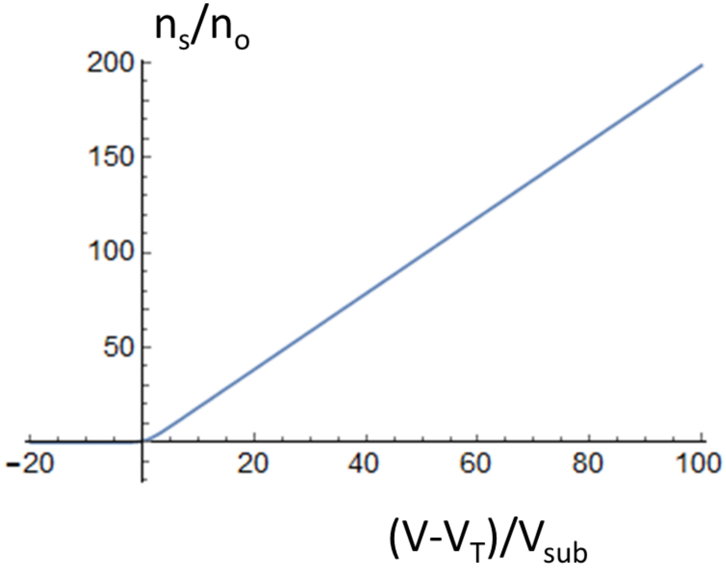
Unified Charge Control Model

$$V_{GS} - V_T = q\left(n_s - n_o\right)/c_a + V_{sub}\ln\left(\frac{n_s}{n_o}\right)$$

$$V_{sub} = \eta\frac{k_B T}{q}$$

Below threshold



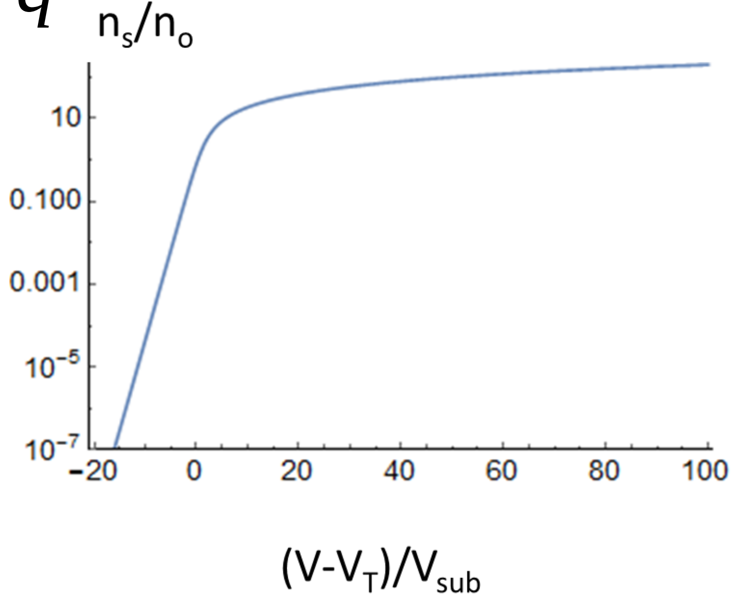


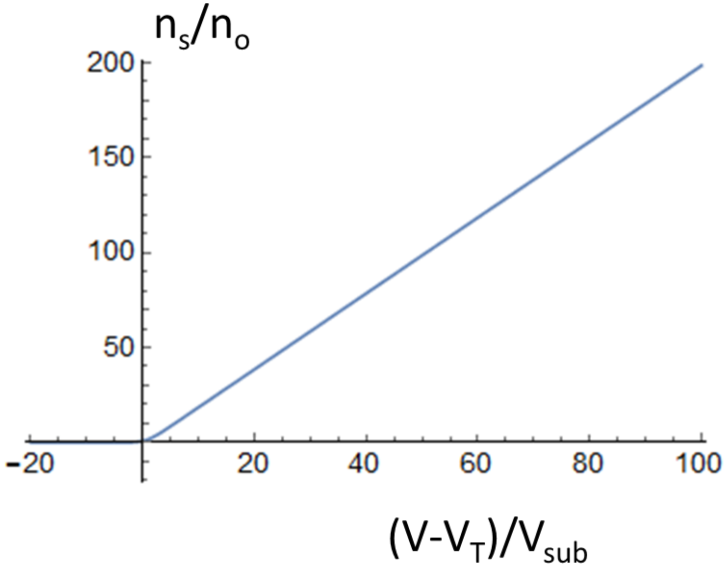
Unified Charge Control Model

$$V_{GS} - V_T = q\left(n_s - n_o\right)/c_a + V_{sub}\ln\left(\frac{n_s}{n_o}\right)$$

$$V_{sub} = \eta\frac{k_B T}{q}$$

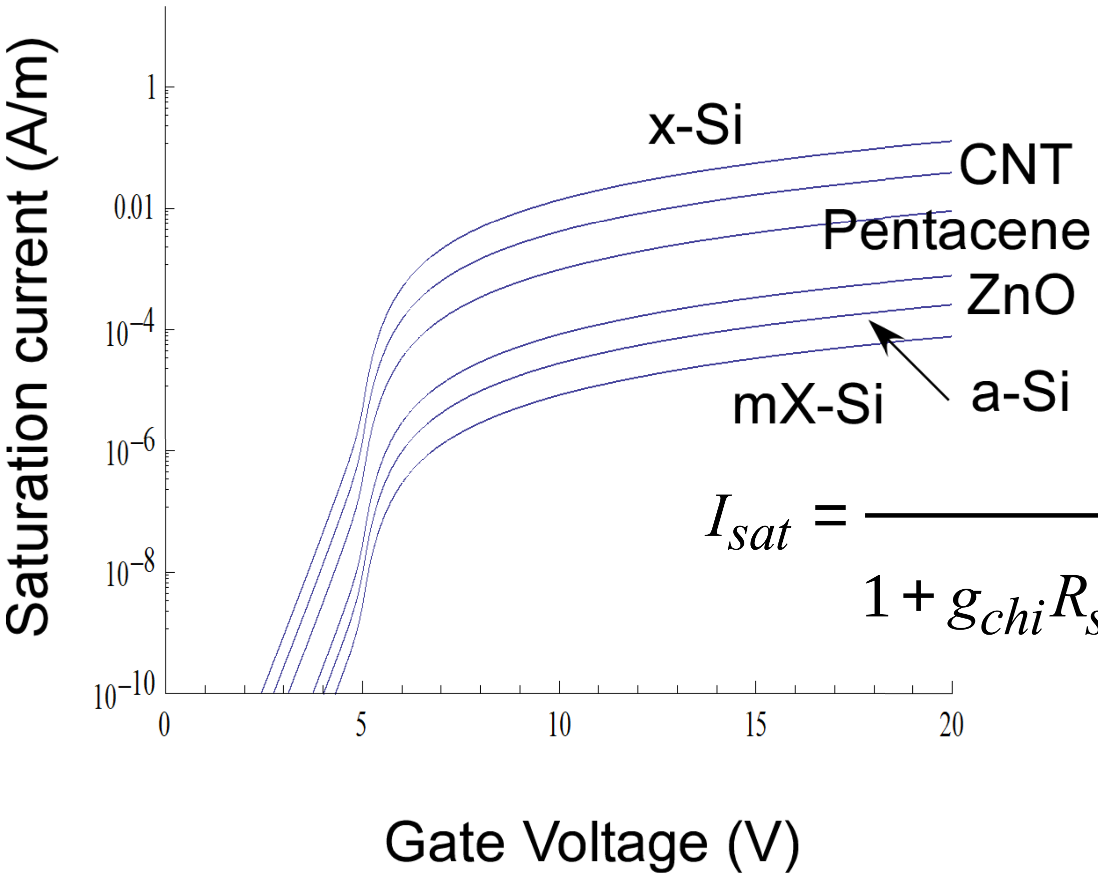
Unified





UCCM saturation current for different TFTs

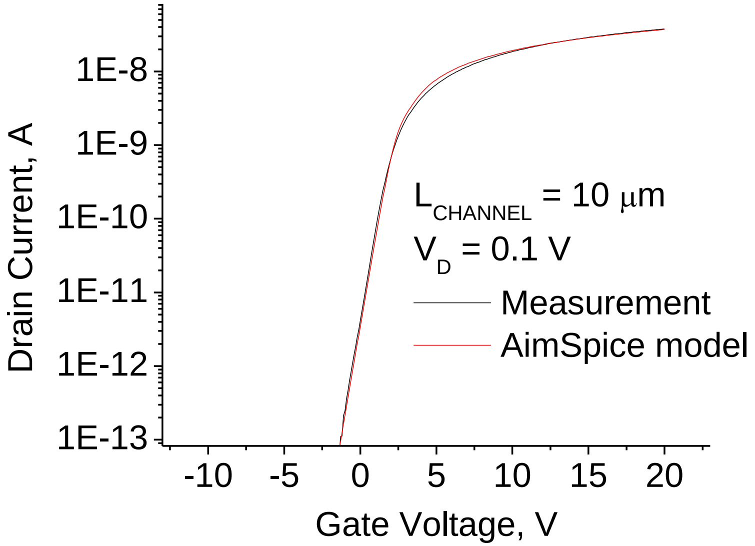
$$V_{gte} = V_{sub}\left[1+\frac{V_{GT}}{2V_{sub}}+\sqrt{\delta^2+\left(\frac{V_{GT}}{2V_{sub}}-1\right)^2}\right]$$

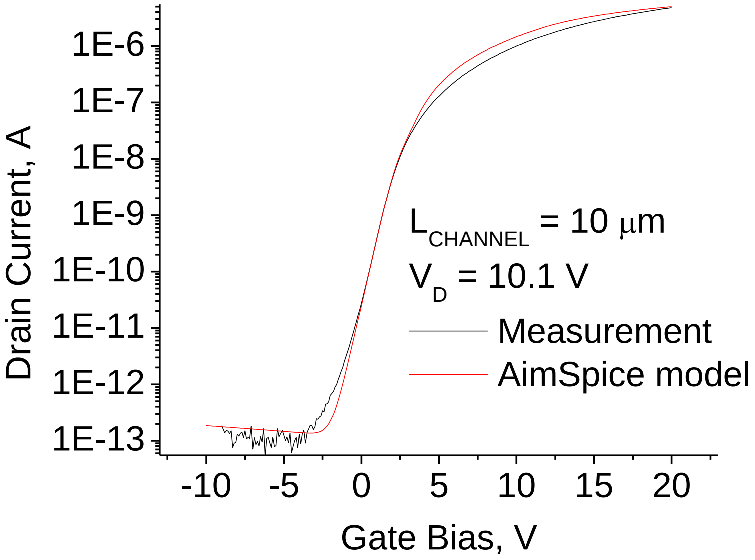


$$I_{ds}=\frac{g_{chi}V_{ds}}{\left[1+\left(g_{ch}V_{ds}/I_{sat}\right)^m\right]^{1/m}}$$

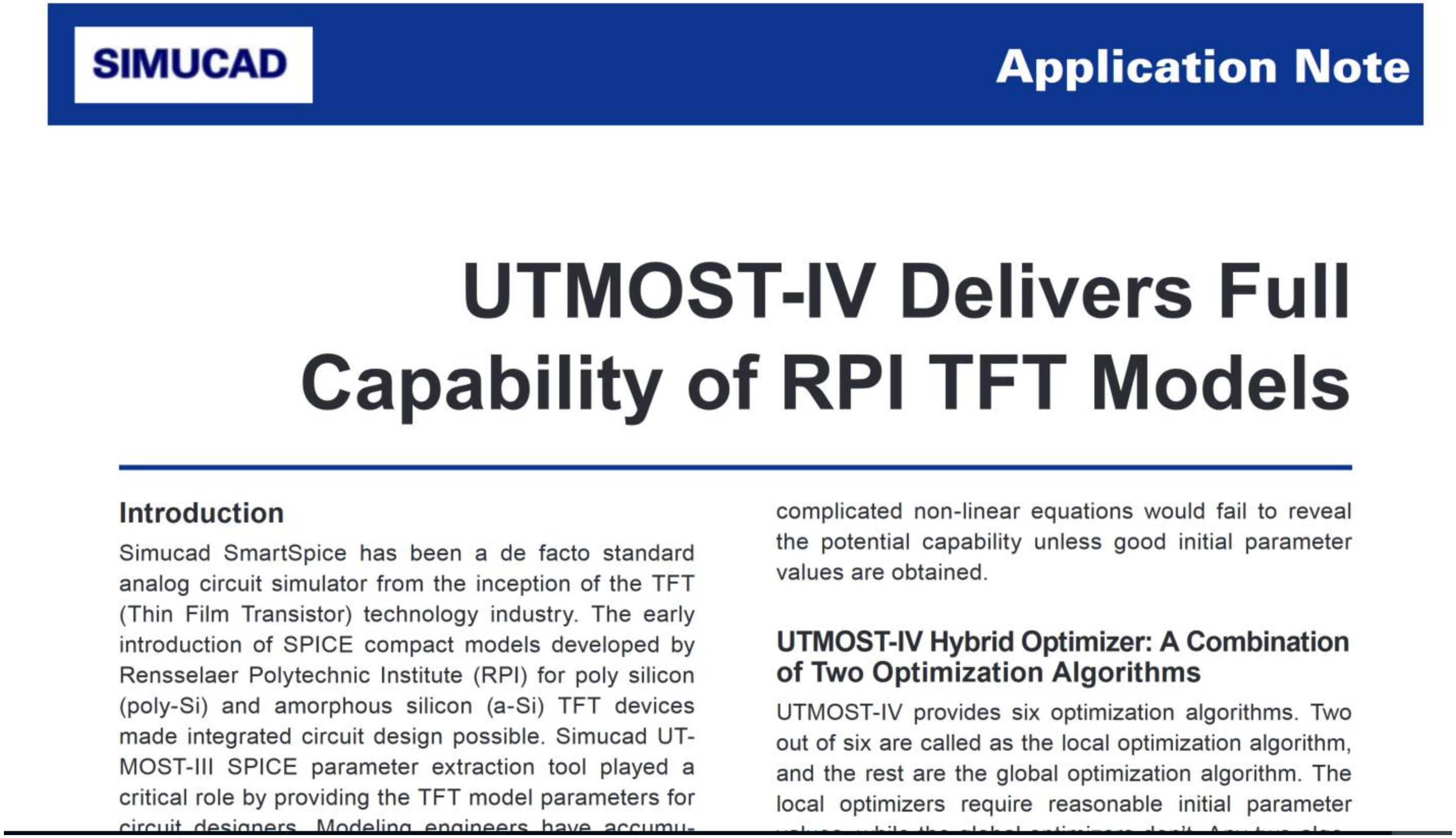
$$I_{sat}=\frac{g_{chi}V_{gte}}{1+g_{chi}R_s+\sqrt{1+2g_{chi}R_s+\left(V_{gte}/V_L\right)^2}}$$

Simulated I-Vs. L = 10 um





RPI TFT models



SIMUCAD

Application Note

UTMOST-IV Delivers Full Capability of RPI TFT Models

Introduction

Simucad SmartSpice has been a de facto standard analog circuit simulator from the inception of the TFT (Thin Film Transistor) technology industry. The early introduction of SPICE compact models developed by Rensselaer Polytechnic Institute (RPI) for poly silicon (poly-Si) and amorphous silicon (a-Si) TFT devices made integrated circuit design possible. Simucad UTMOST-III SPICE parameter extraction tool played a critical role by providing the TFT model parameters for circuit designers. Modeling engineers have accumu-

complicated non-linear equations would fail to reveal the potential capability unless good initial parameter values are obtained.

UTMOST-IV Hybrid Optimizer: A Combination of Two Optimization Algorithms

UTMOST-IV provides six optimization algorithms. Two out of six are called as the local optimization algorithm, and the rest are the global optimization algorithm. The local optimizers require reasonable initial parameter

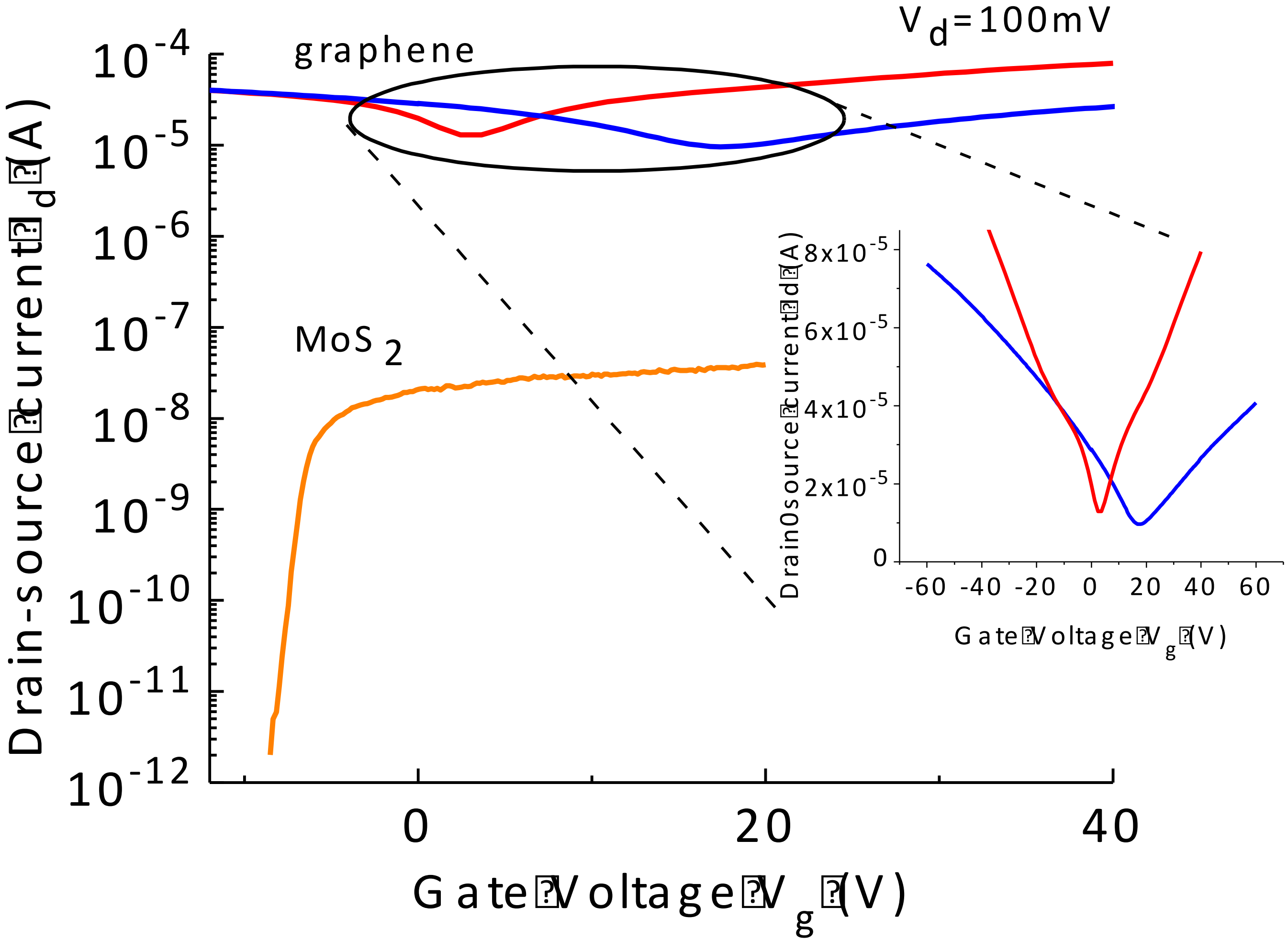
Non-ideal behavior (2D generation model)

Effective gate length and width for scaling design

$$L_{eff} = L - \Delta L(V_G, V_D)$$

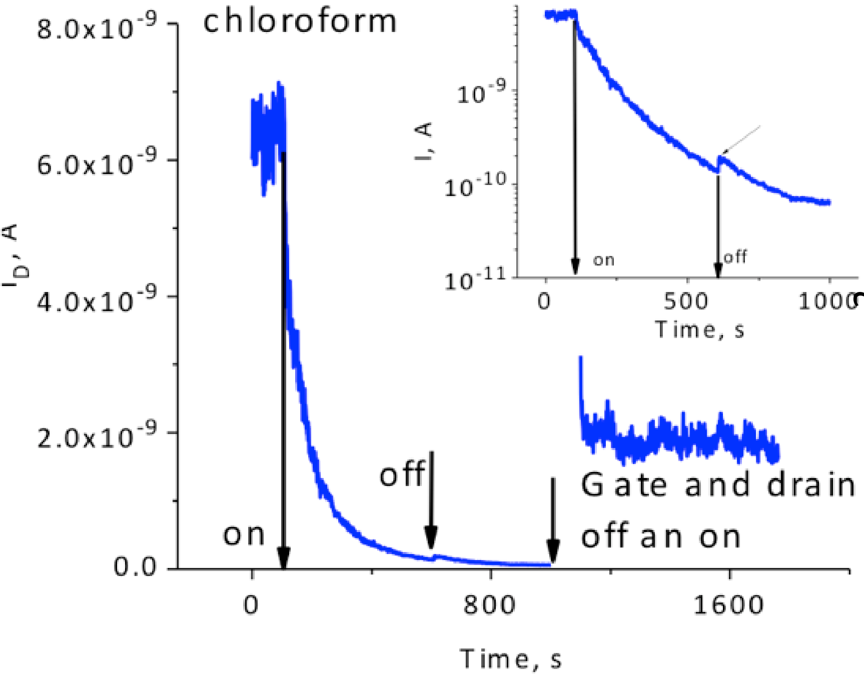
$$W_{eff} = W + \Delta W(V_G, V_D)$$

Graphene and MoS$_2$ FET I-Vs

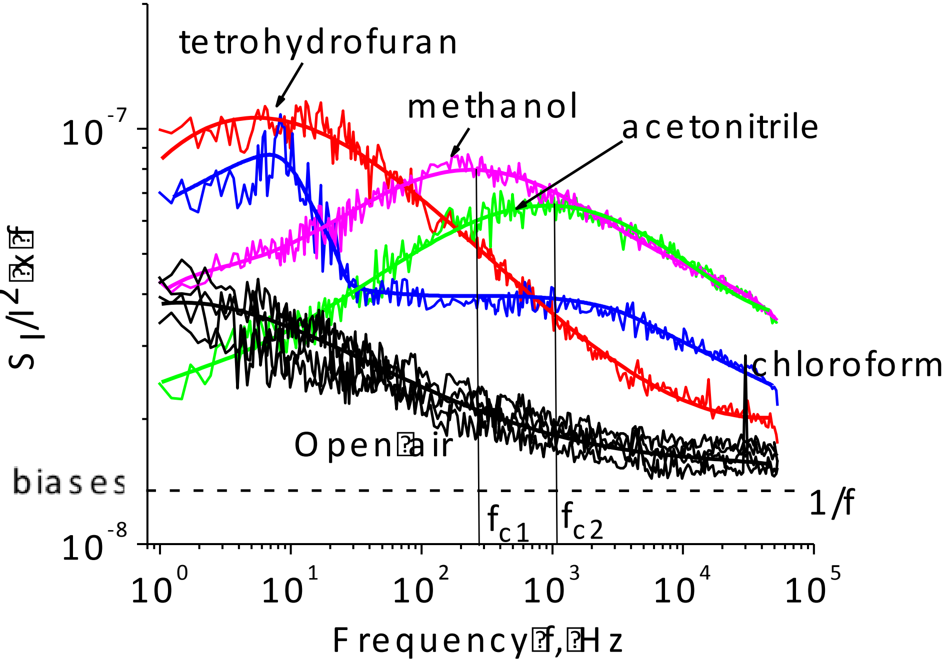


M. Shur, S. Rumyantsev, C. Jiang, R. Samnakay, J. Renteria, A. Balandin, Selective gas sensing with MoS2 thin film transistors, IEEE Sensors 2014 Proceedings., pp. 55-57 (2014)

Sensing Applications



Gas Gated Transistor
> 220 ºC

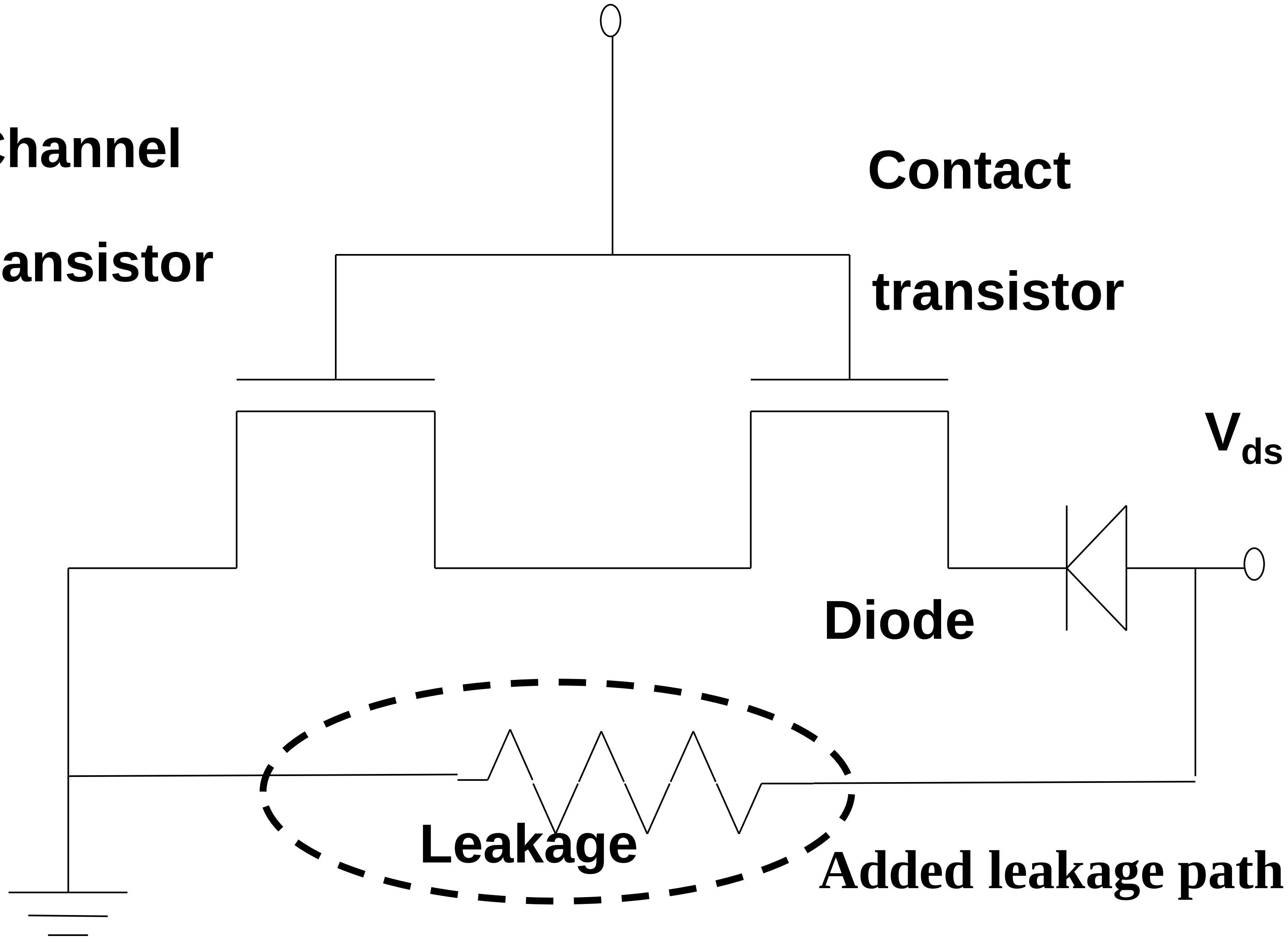


Selective Sensing with One Device

M. Shur, S. Rumyantsev, C. Jiang, R. Samnakay, J. Renteria, A. Balandin, Selective gas sensing with MoS2 thin film transistors, IEEE Sensors 2014 Proceedings., pp. 55-57 (2014)

S. Rumyantsev, G. Liu, R. A. Potyrailo, A. A. Balandin, and M. S. Shur, Selective Sensing of Individual Gases Using Graphene Devices, IEEE *Sensors Journal,* vol.13, no.8, pp. 2818 - 2822, Aug. 2013, doi: 10.1109/JSEN.2013.2251627

Equivalent Circuit: add leakage



Channel

transistor

Contact

transistor

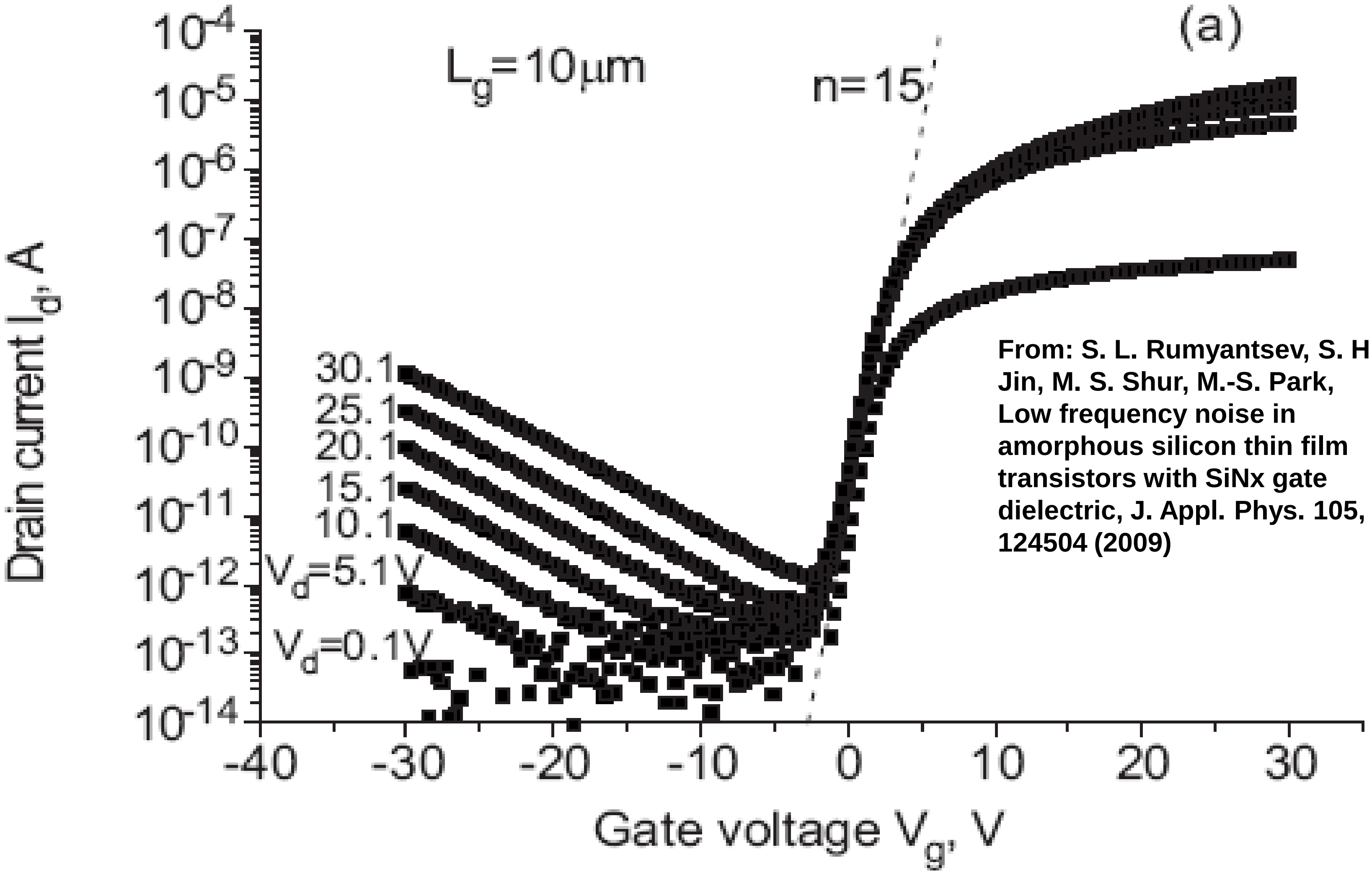
V_{ds}

Diode

Leakage

Added leakage path

TFT Transfer Characteristics: large, drain bias dependent leakage



From: S. L. Rumyantsev, S. H. Jin, M. S. Shur, M.-S. Park, Low frequency noise in amorphous silicon thin film transistors with SiNx gate dielectric, J. Appl. Phys. 105, 124504 (2009)

Threshold Voltage dependence on geometry for scaling

$$V_{TH} = V_{thx} - \frac{at \cdot V_{ds}^{2} + bt}{l \cdot \left(1 + e^{\left(\frac{V_{gs} - (V_{thx} - vsigmat)}{vsigma}\right)}\right)}$$

Michael Shur (shurm@rpi.edu)

Improved effective TFT mobility model

$$mueff = mus + \frac{mufet}{1 + \frac{theta}{tox} \cdot V_{gte}}$$

$$\frac{1}{mufet} = \frac{1}{mu0} + \frac{1}{\mu_1 \cdot \left(\frac{2 \cdot V_{gte}}{eta_f \cdot V_t} \right)^{mmu}}$$

where

$$V_t = k \cdot T / q$$

$$V_{gte} = eta \cdot V_t \cdot \left(1 + \frac{\alpha_{sat} \cdot V_{gt}}{2 \cdot eta \cdot V_t} + \sqrt{delta^2 + \left[\frac{\alpha_{sat} \cdot V_{gt}}{2 \cdot eta \cdot V_t} - 1 \right]^2} \right)$$

$$V_{gt} = V_{gs} - V_{th}$$

Unified Electron Sheet Charge Density Per Unit Area (2D generation model)

$$V_{dse} = \frac{V_{ds}}{\left(1 + \left(\frac{V_{ds}}{V_{dsat}}\right)^{mss}\right)^{1/mss}}$$

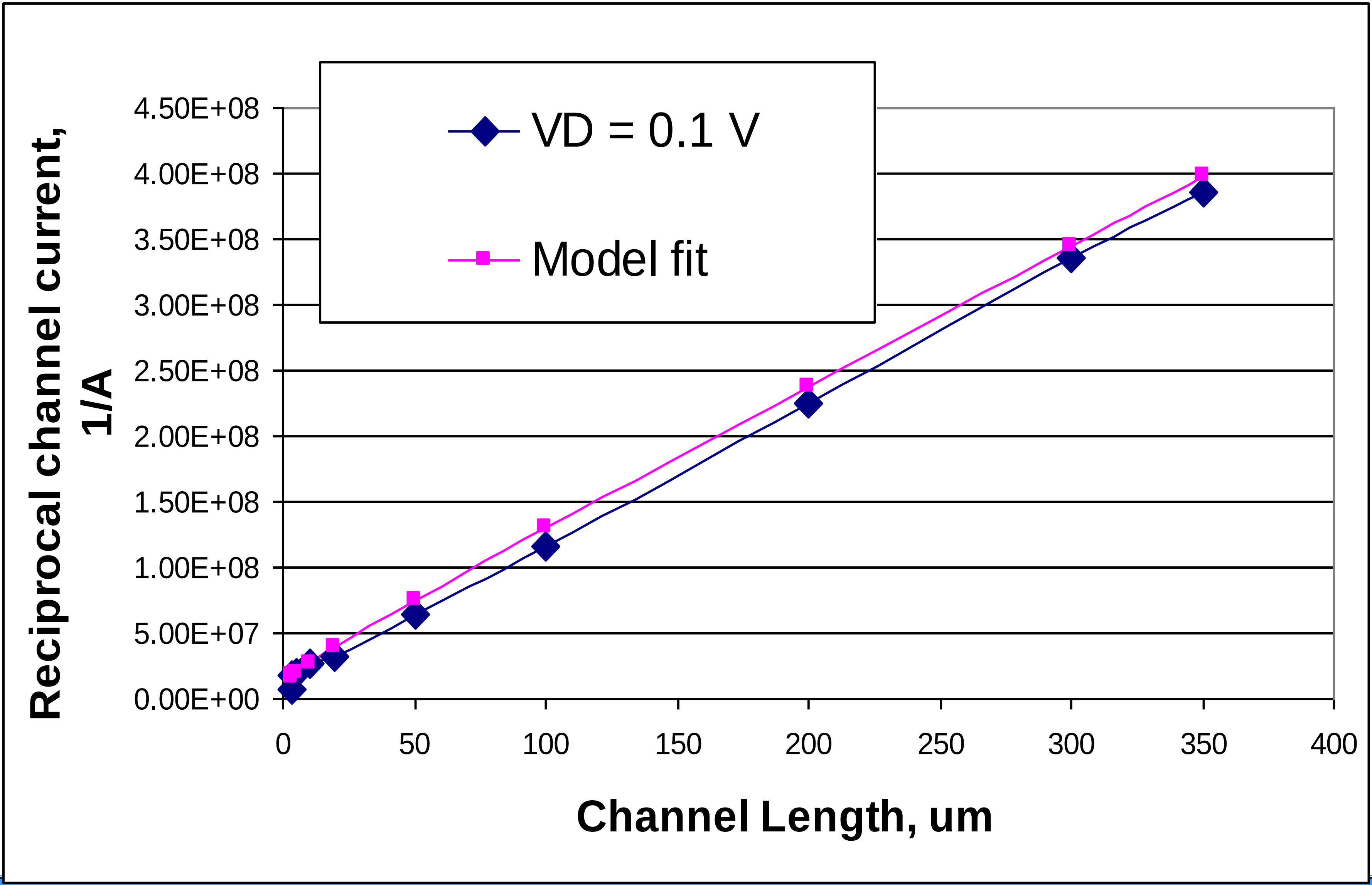
$$n_s = 2 \cdot n_0 \cdot \log\left(1 + \frac{1}{2} \cdot e^{\frac{V_{gt}}{etaf \cdot V_t}}\right)$$

$$eta_f = \frac{eta}{1 + meta \cdot reta \cdot \frac{i1}{1 + i1}}$$

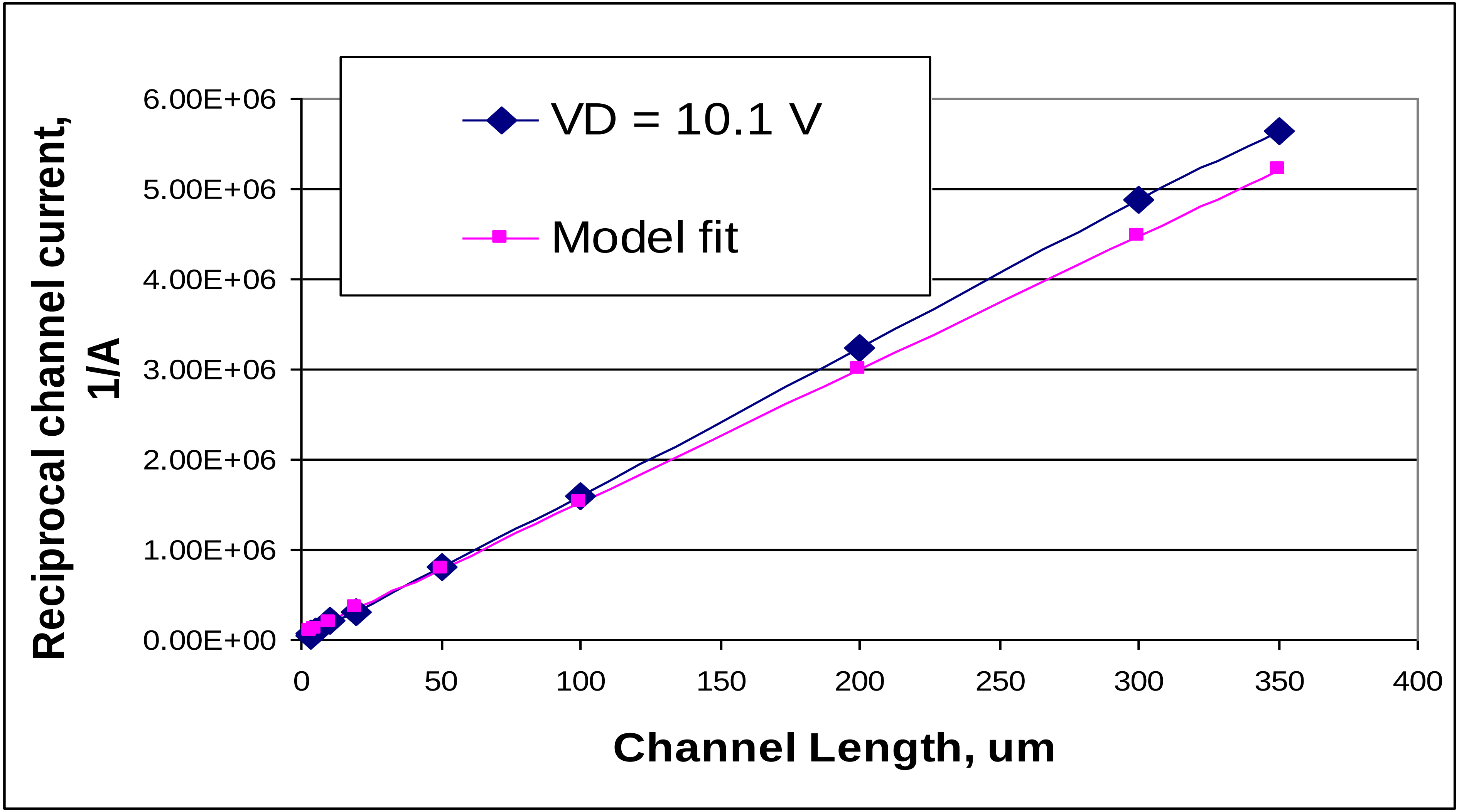
$$n_0 = \frac{\varepsilon_{SiO_2} \cdot eta \cdot V_t}{2 \cdot q \cdot tox}$$

Michael Shur (shurm@rpi.edu)

Scaling with RPI TFT model



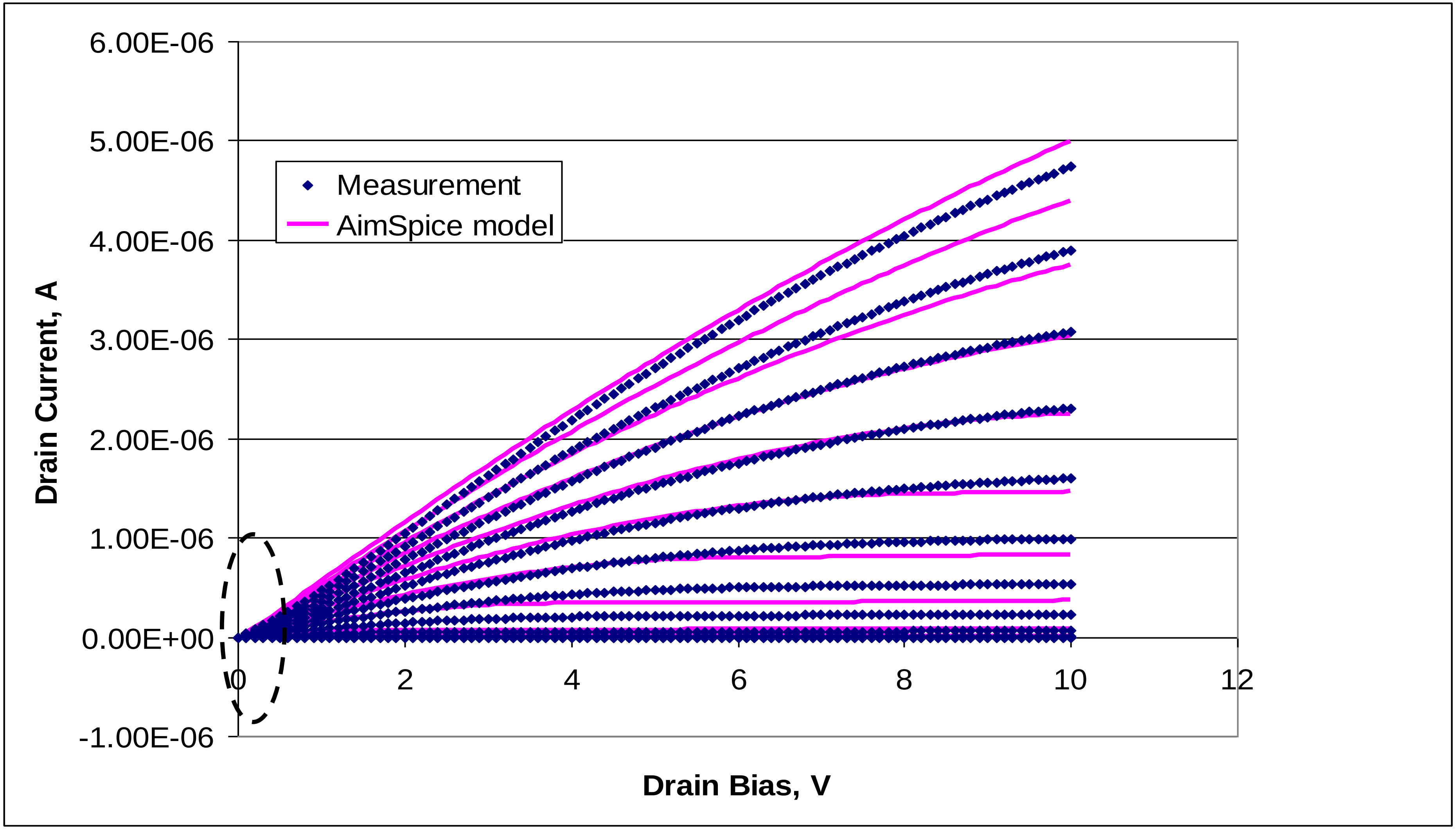
Scaling with RPI TFT model



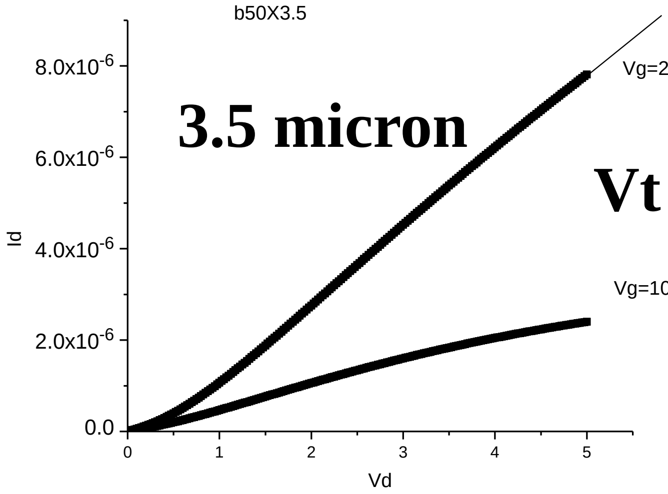
Michael Shur (shurm@rpi.edu)

CONTACT EFFECTS

The effect of contact non-linearity (diode). More pronounced for shorter channels



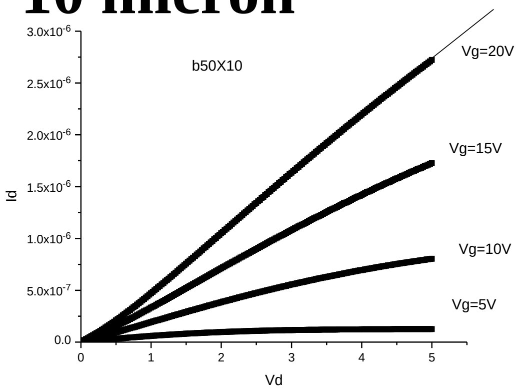
Contact Nonlinearity Affects Short Channel Devices



3.5 micron

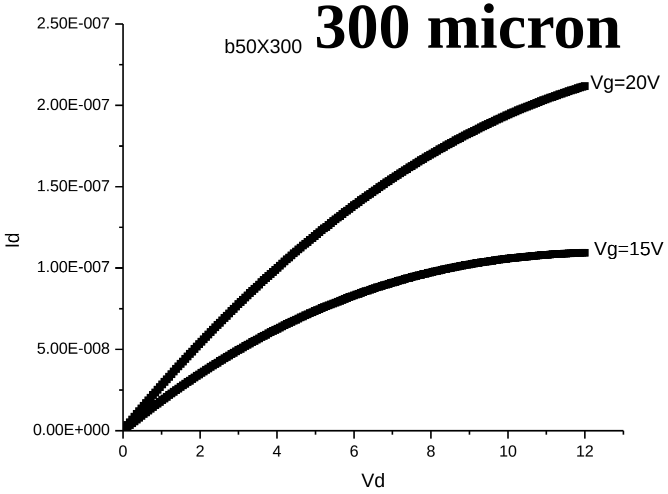
Vt = 1.4 V

10 micron



Vt = 2 V

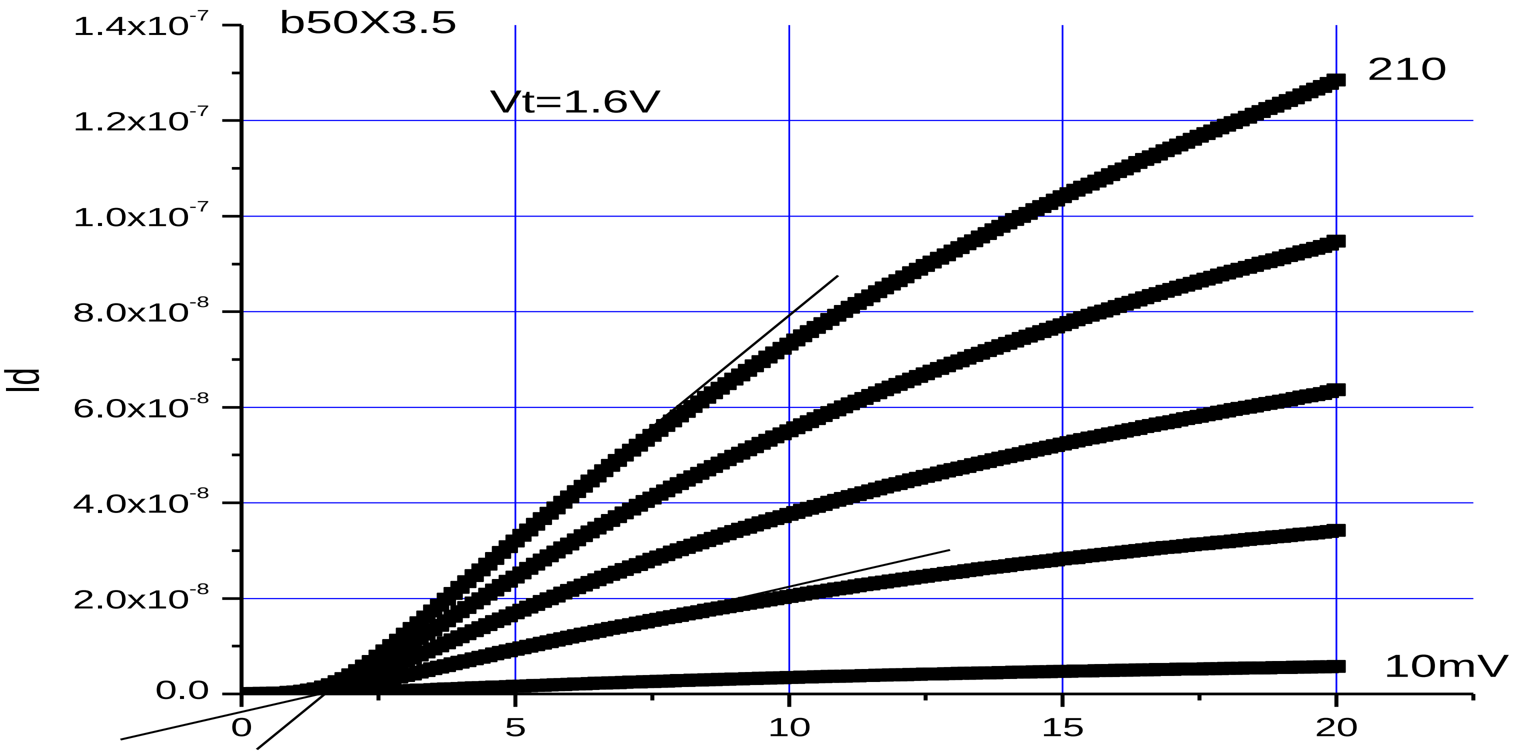
300 micron



Vt = 4 V

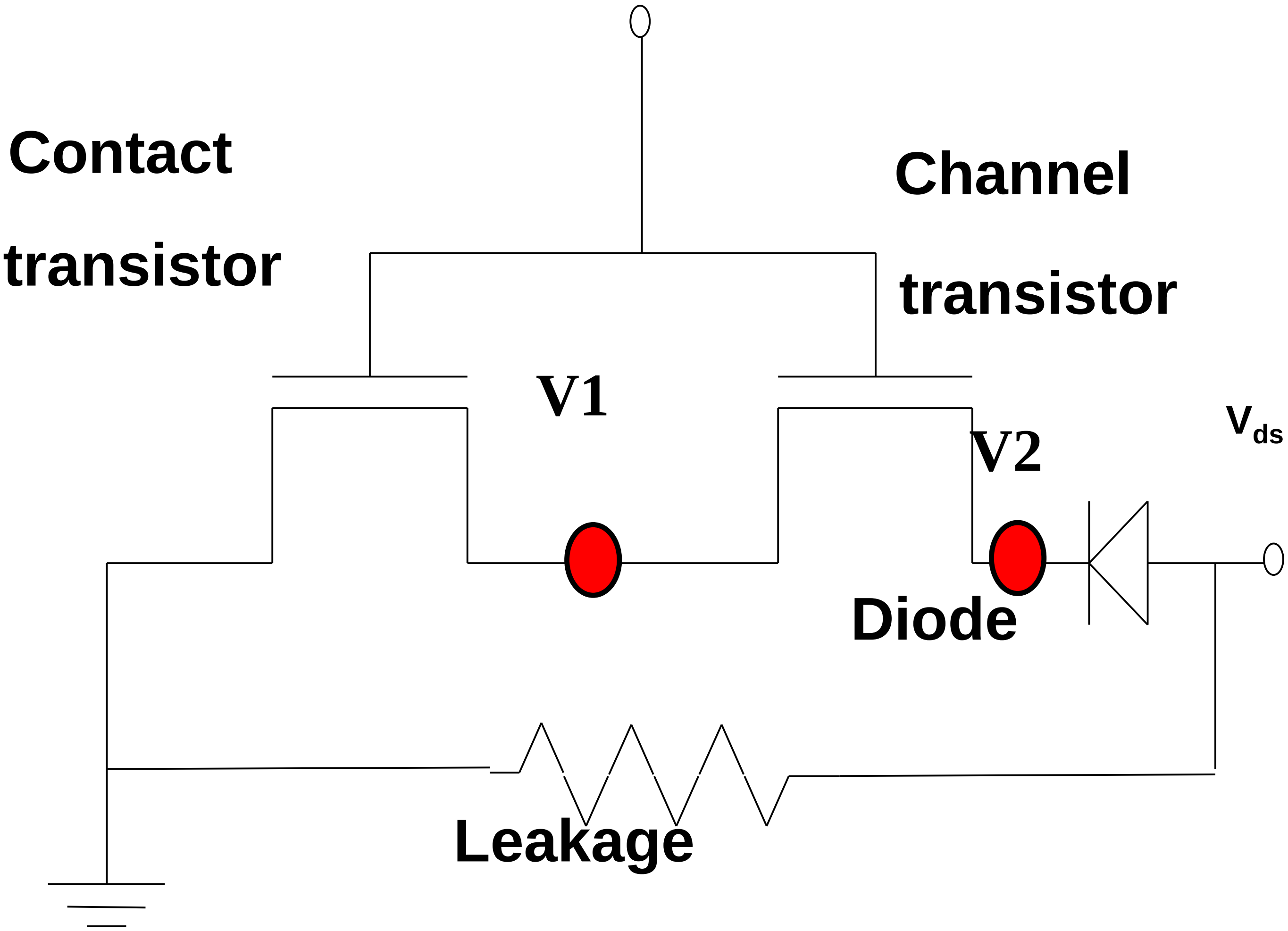
Contact non-linearity and threshold variation

Threshold Voltage Extraction

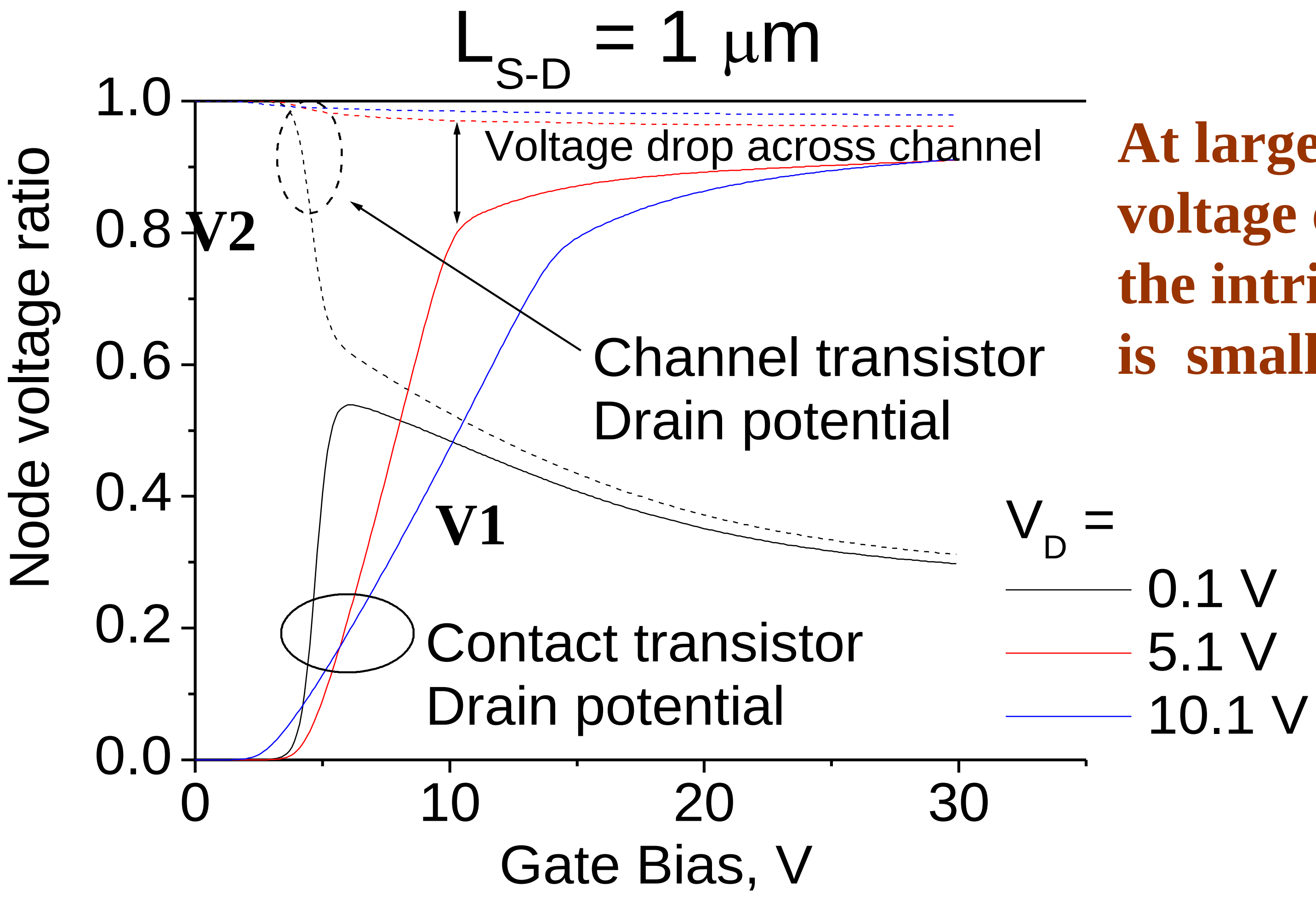


The effect of contact non-linearity is closely related to the threshold voltage variation. The contact section must be modeled separately.

Contact transistor model

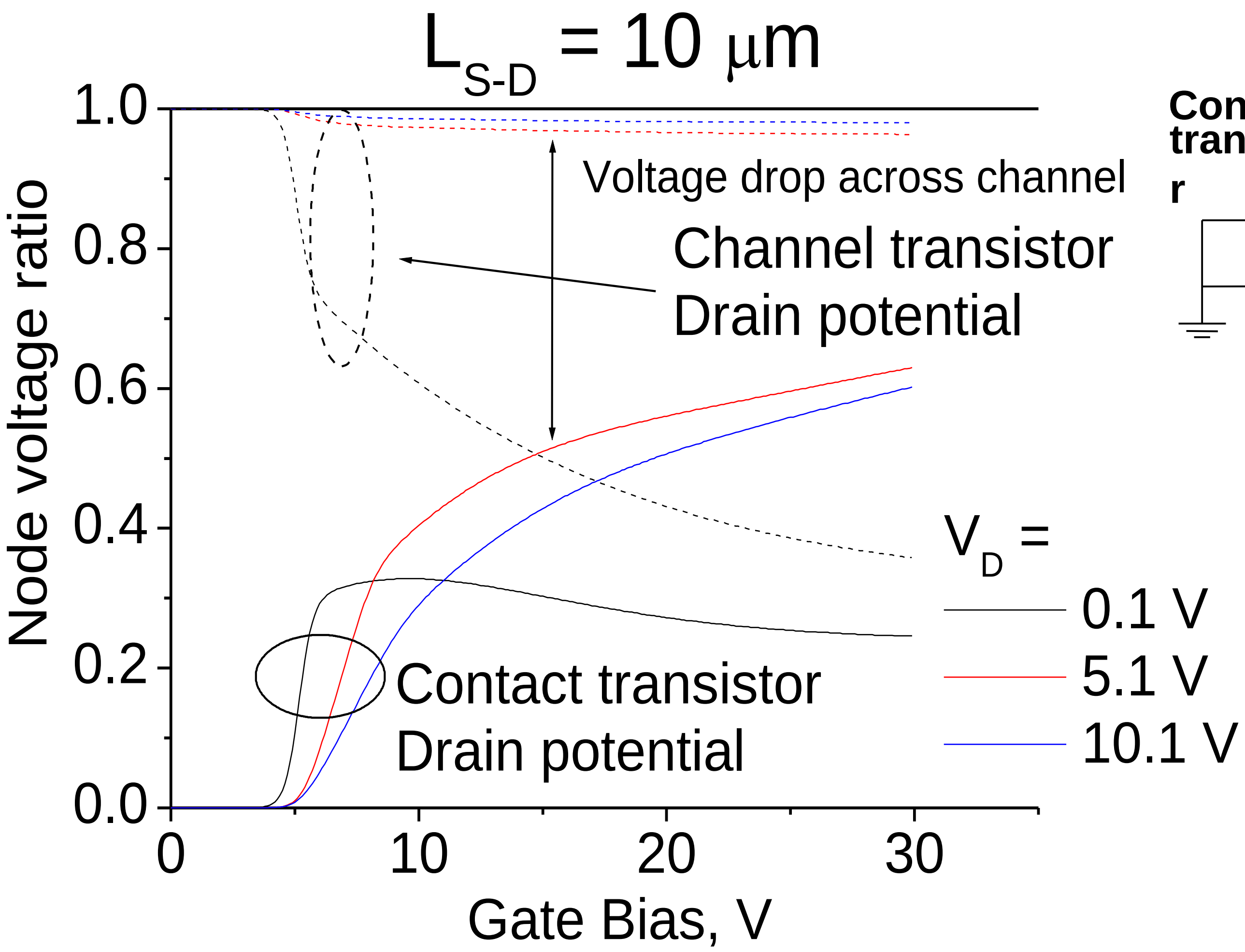


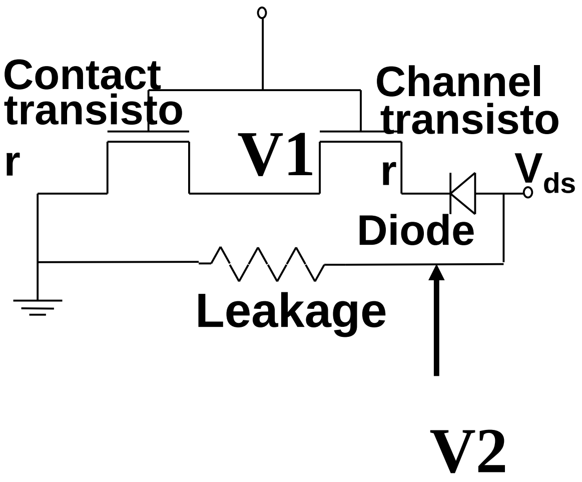
Node voltages. Solid – channel potential on the source side, dashed – on the drain side. L = 1 um



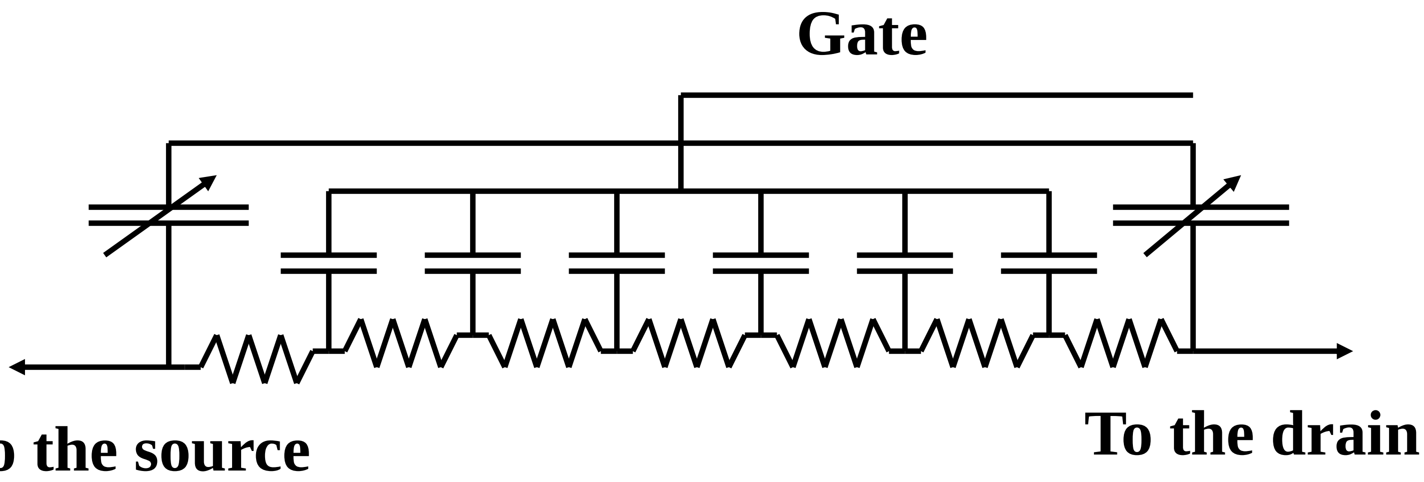
At large gate bias, the voltage drop across the intrinsic transistor is small

Node voltages. Solid – channel potential on the source side, dashed – on the drain side. L = 10 um



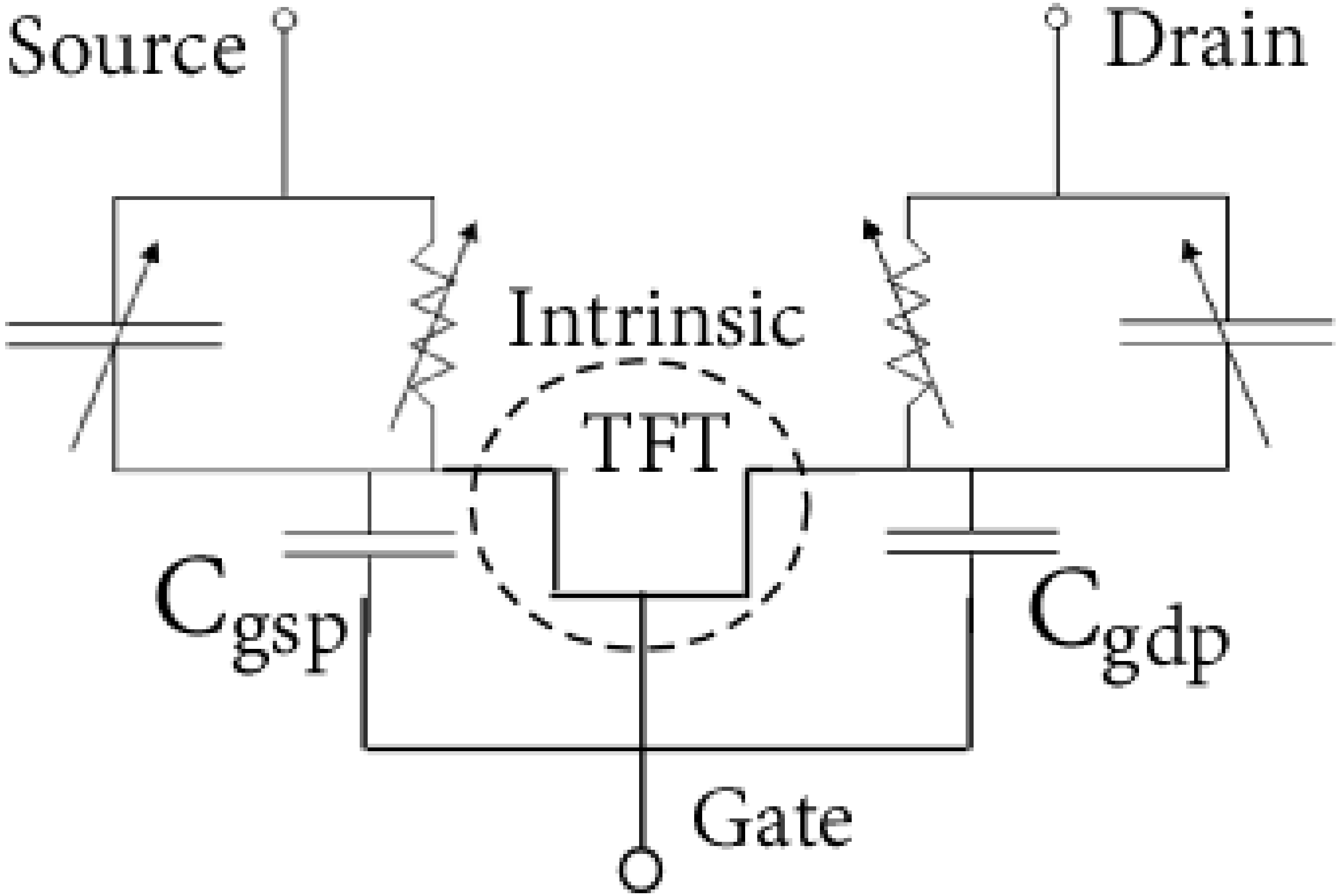


CV Model

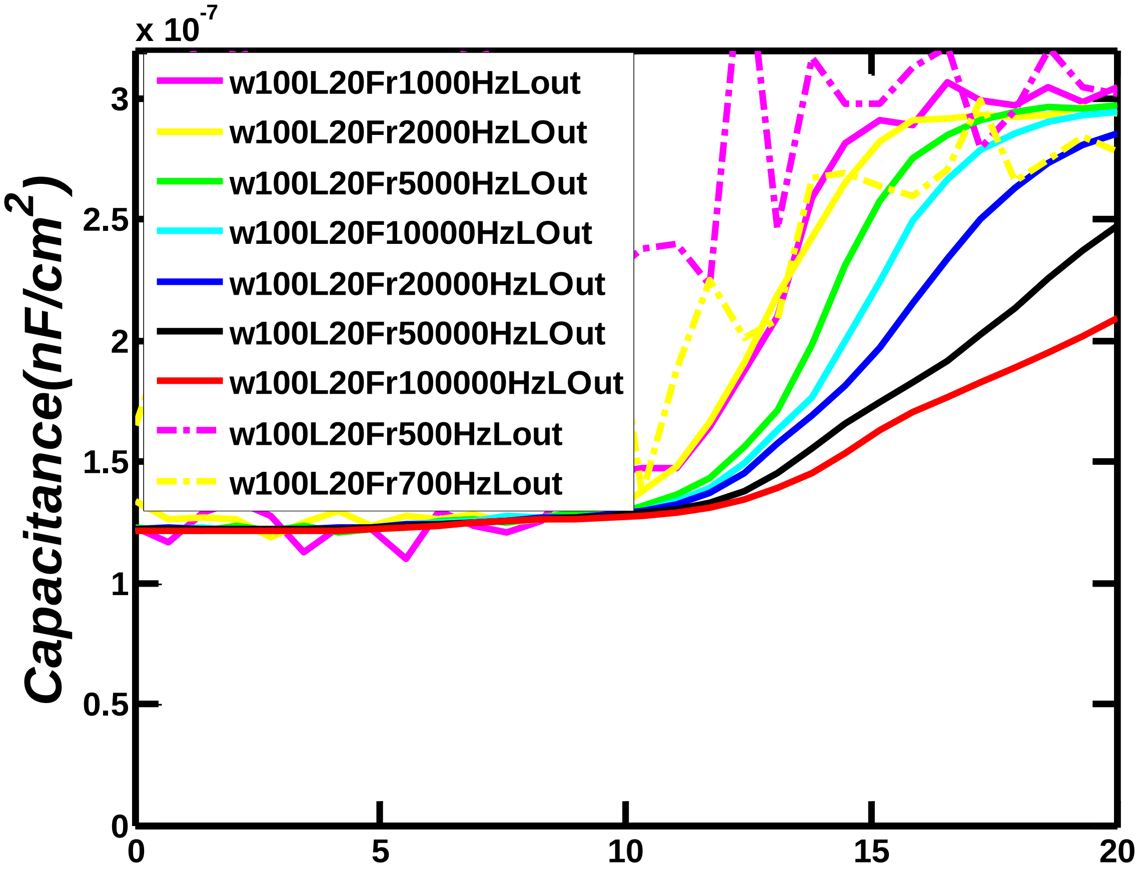


The channel of the transistor should be modeled as a distributed RC line with gate controlled resistances
Additional contact associated capacitances have significant dependence on the gate bias and should also be modeled as transistor capacitances

Capacitance model: Intrinsic and parasitic capacitances



Capacitance Dispersion



Capacitance Model: Equations

When capmod=0,

$$C_{gs} = C_f + \frac{2}{3} \cdot C_{gcs} \cdot \left[1 - \left(\frac{V_{dsat} - V_{dse}}{2 \cdot V_{dsat} - V_{dse}}\right)^2\right]$$

$$C_{gcs} = \frac{w \cdot l \cdot \varepsilon_{SiO_2} / tox}{1 + etac0 \cdot e^{\left(-\frac{V_{gt}}{etac0 \cdot V_t}\right)}}$$

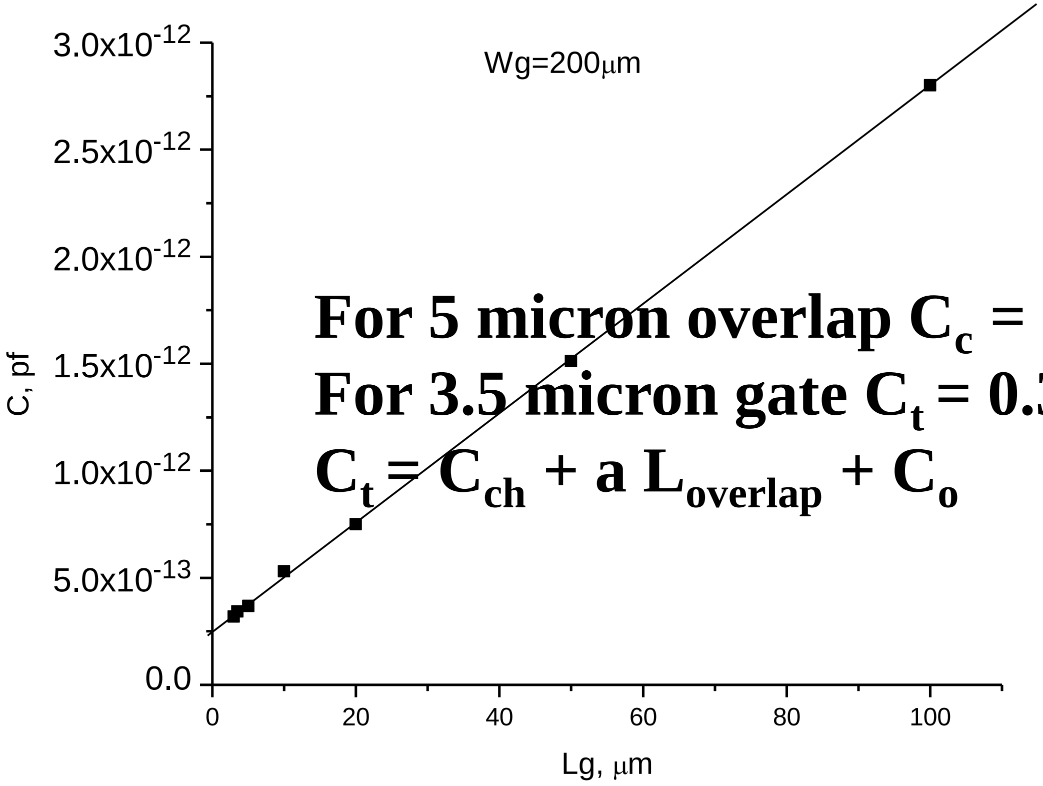
$$C_{gd} = C_f + \frac{2}{3} \cdot C_{gcd} \cdot \left[1 - \left(\frac{V_{dsat}}{2 \cdot V_{dsat} - V_{dse}}\right)^2\right]$$

$$C_{gcd} = \frac{w \cdot l \cdot \varepsilon_{SiO_2} / tox}{1 + \eta_{cd} \cdot e^{\left(-\frac{V_{gt} - V_{dse}}{\eta_{cd} \cdot V_t}\right)}}$$

$$C_f = \frac{1}{2} \cdot \varepsilon_{si} \cdot w$$

$$\eta_{cd} = etac0 + etac00 \cdot V_{dse}$$

Capacitance data



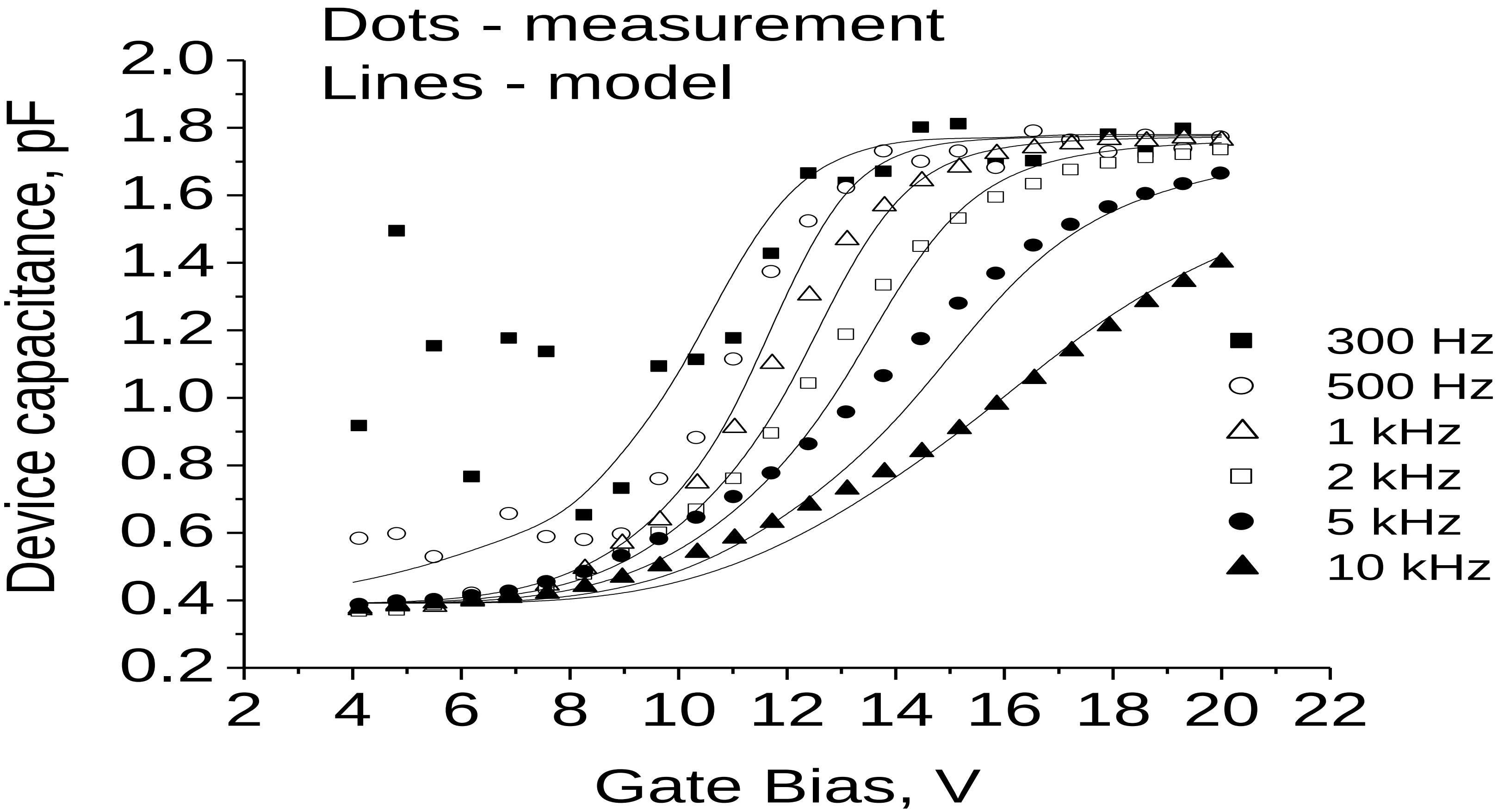
For 5 micron overlap $C_c = 0.125$ PF

For 3.5 micron gate $C_t = 0.34$ pF

$C_t = C_{ch} + a\,L_{overlap} + C_o$

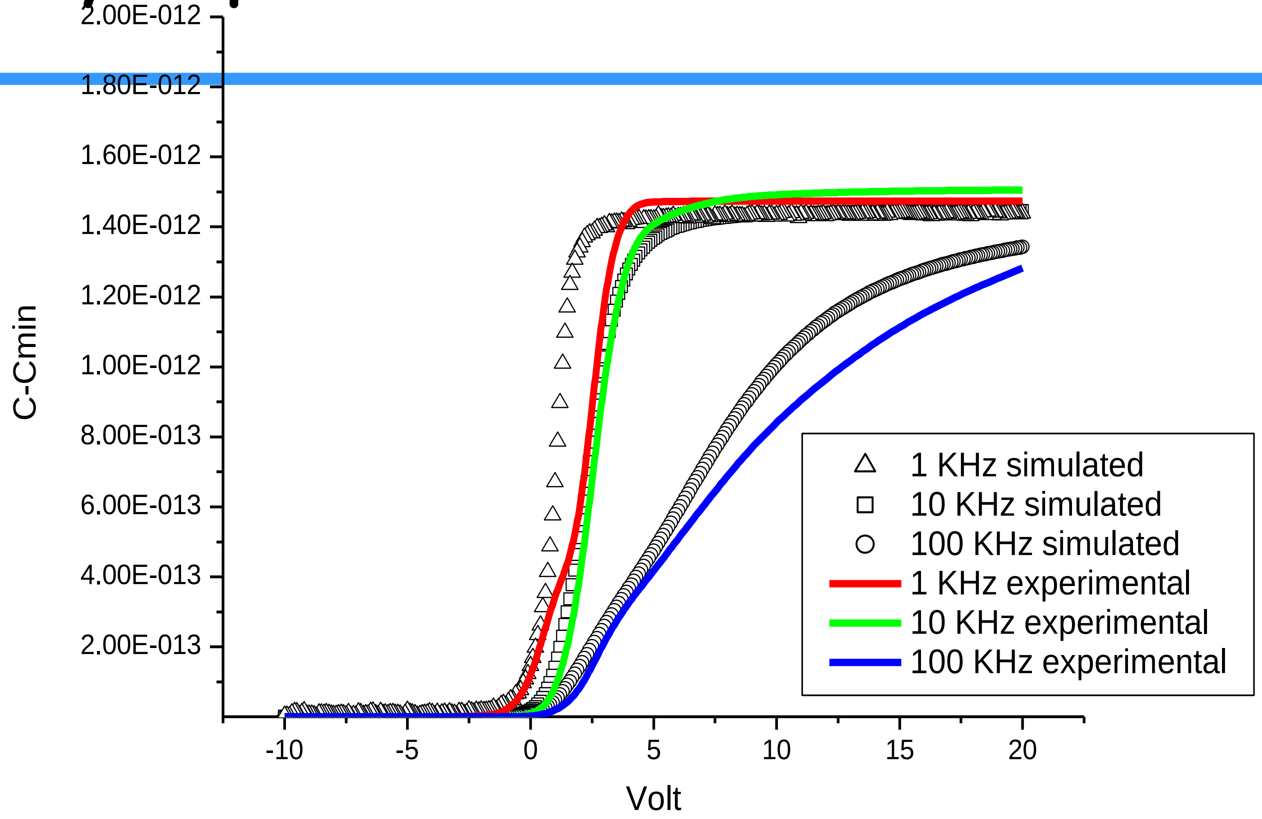
Gate oxide (ON state) capacitance scaling. The offset corresponds to contact capacitance

Frequency dispersion



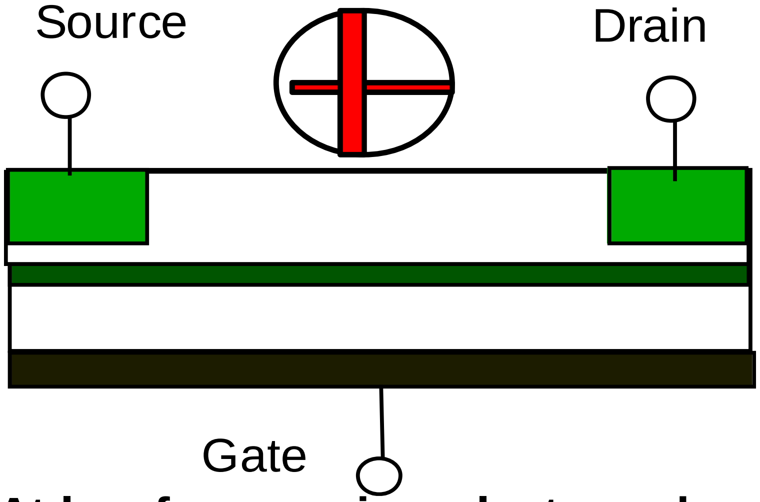
From S. Bhalerao, A. Koudymov, M. Shur, T. Ytterdal, W. Jackson, and C. Taussig, Compact capacitance model for printed thin film transistors with non-ideal contacts, International Journal of High Speed Electronics and System Vol. 20, No. 4, pp. 801-814, December 2011, B. Iniguez and M. Shur Editors

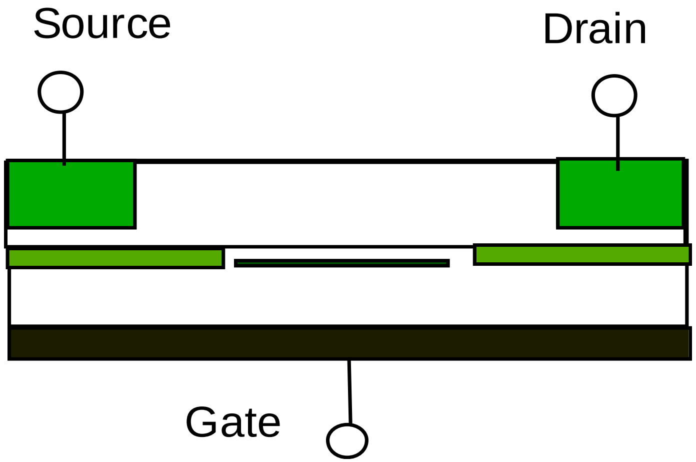
Frequency dispersion



The device channel was divided into 20 sub-regions in order to account for the distributed channel resistance. Good agreement with the experiment is obtained. The experimental threshold shift with frequency is trap-related.

Physics of capacitance Dispersion: Transit Time Mechanism





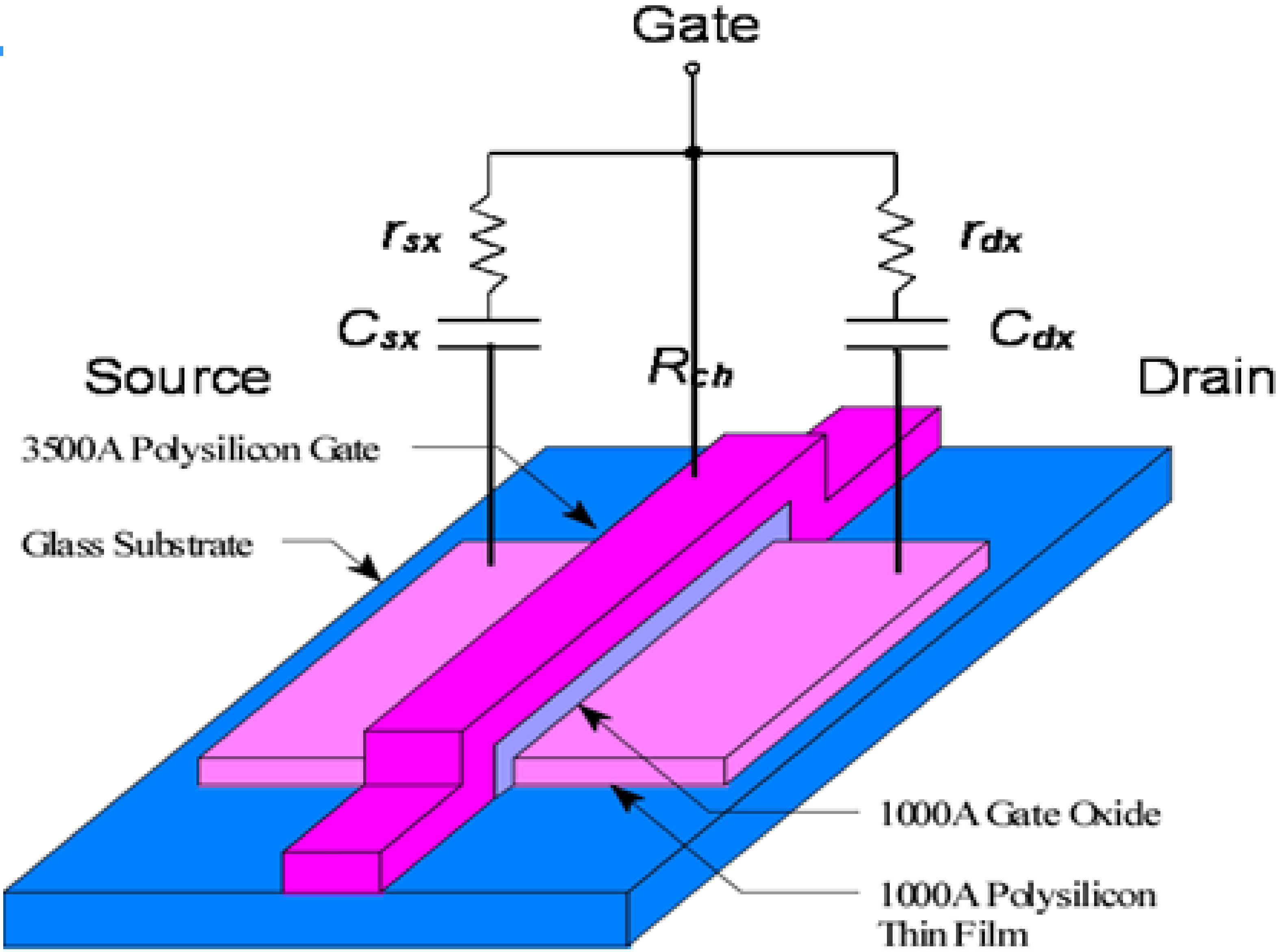
At low frequencies, electrons have time to travel to the middle of the channel establishing the second plate of for the parallel plate channel capacitance

At high frequencies, electrons DO NOT have time to travel to the middle of the channel and the capacitance is smaller

Since the field (and velocity driving electrons is proportional to 1/L, this dispersion is proportional to 1/L ^{2}

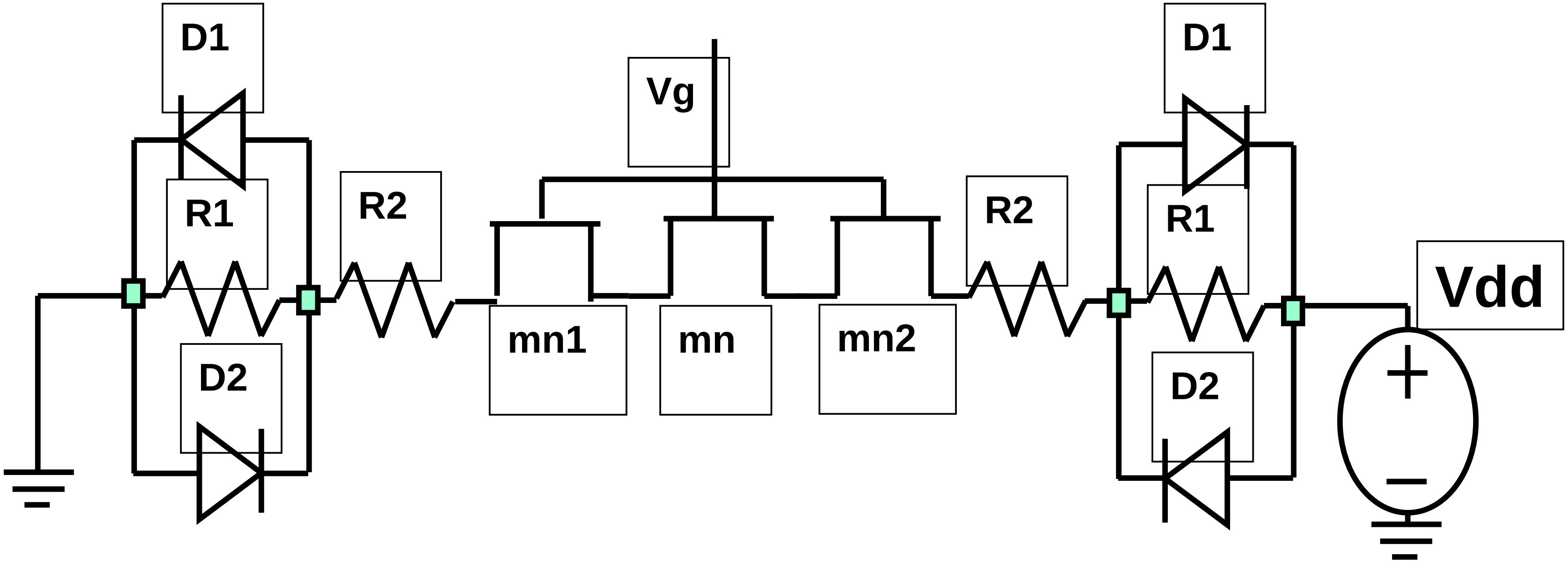
$$\tau_1 = \frac{L_g^{\ 2}}{\mu_{FET} * V_{eff}}$$

Elmore model



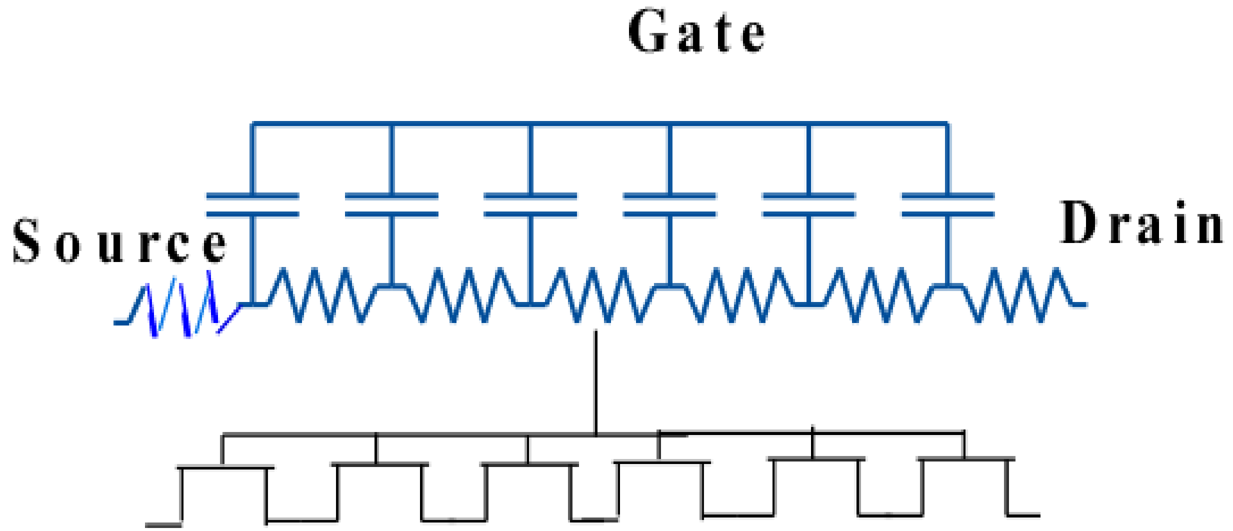
TFT dispersion circuit

Complete circuit

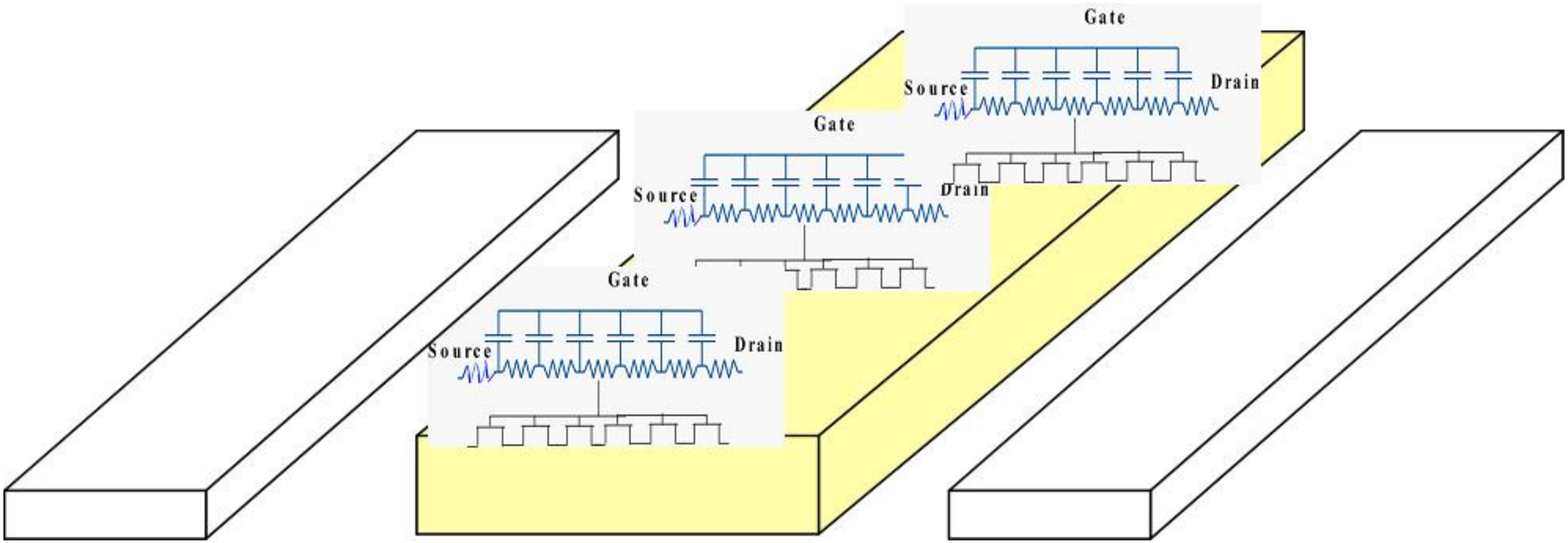


From M. S. Shur, D. Veksler, V. Chivukula, A. Koudymov, T. Ytterdal, B. Iñiguez, and W. Jackson, Modeling Of Thin Film Transistors With Non-Ideal Contacts, ECS Proceedings, vol. 8, No. 1, pp. 165-170 (2007)

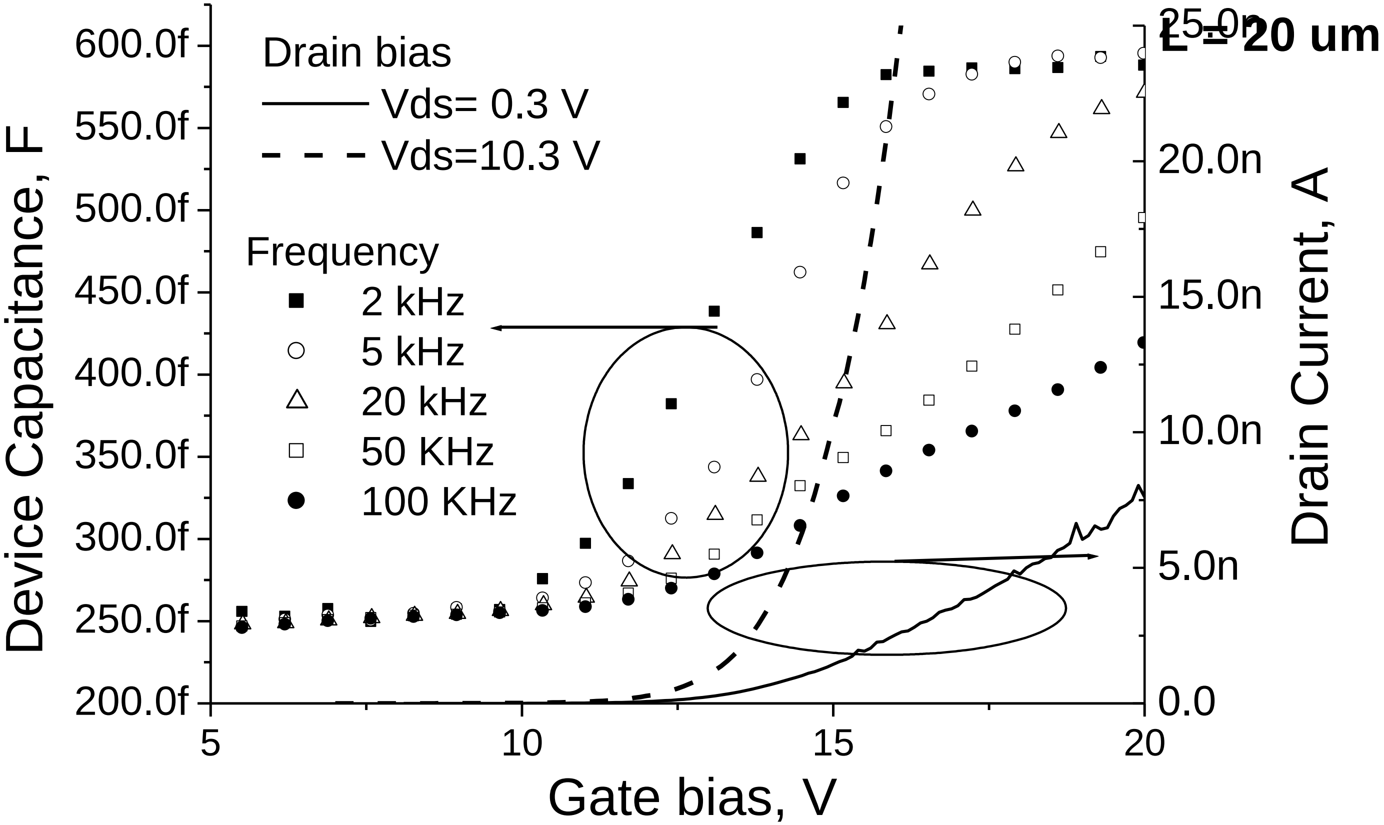
Transmission line model



2D model



Traps lead to a strong dispersion in C-V characteristics



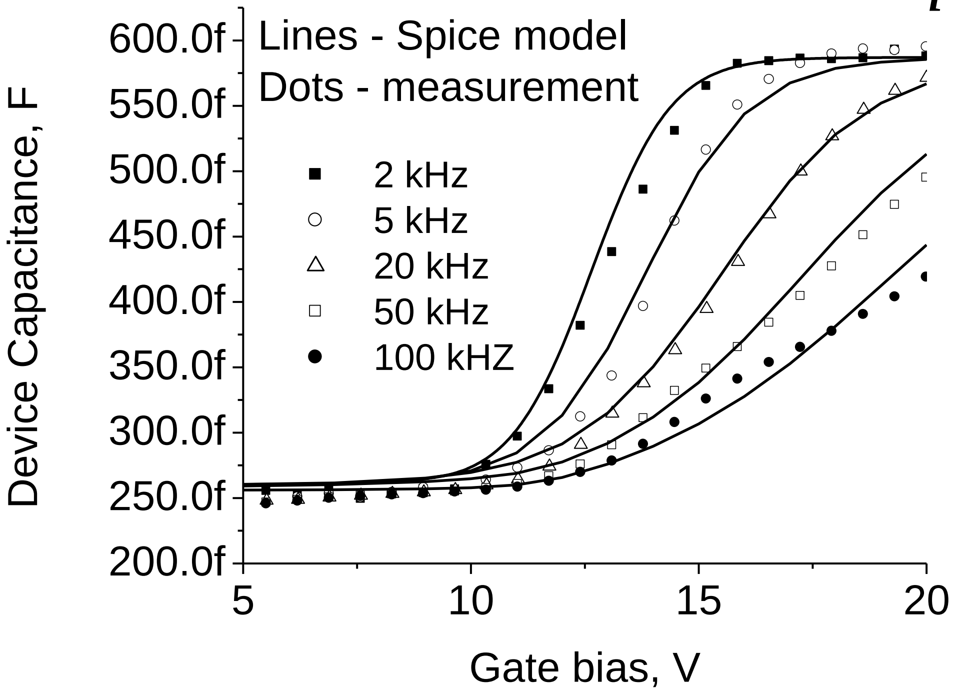
From S. Bhalerao, A. Koudymov, M. Shur, T. Ytterdal, W. Jackson, and C. Taussig, Compact capacitance model for printed thin film transistors with non-ideal contacts, International Journal of High Speed Electronics and System Vol. 20, No. 4, pp. 801-814, December 2011, B. Iniguez and M. Shur Editors

Role of traps

- ☐ Traps and contacts determine TFT I-V and C-V characteristics
- ☐ Traps cause noise and their density can be extracted from noise
- ☐ Frequency dispersion is determined by localized traps
  - ○ The rate of traps interaction with the states above mobility edge
  - ○ The trap-dominated speed of electron propagation along the channel
- ☐ Contacts are non-linear and dominant at higher currents and shorter channel lengths

Variable dispersion model

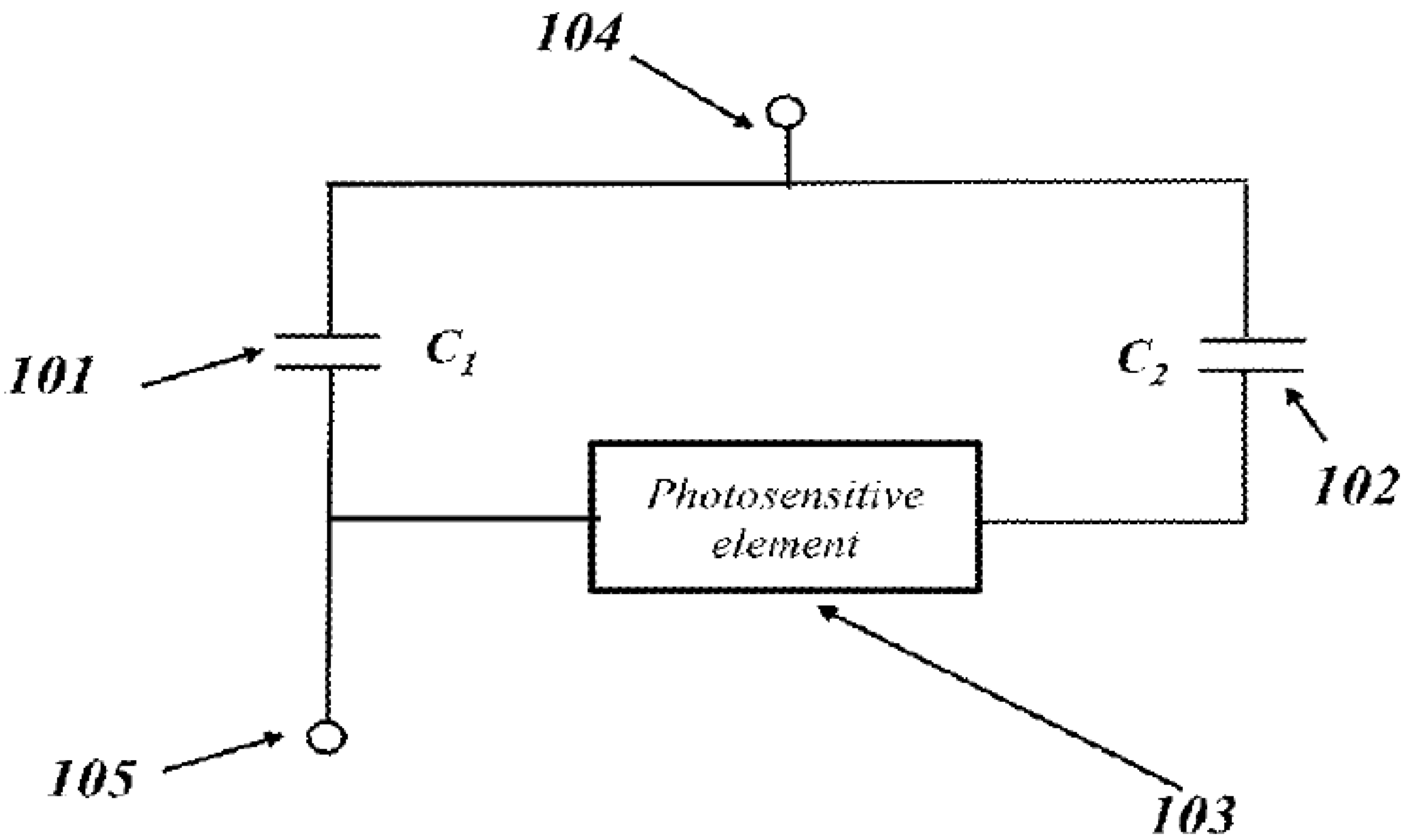
$$V_{th\_effective} = \frac{kT_{effective}}{q} = \frac{kT}{q}\left(1+\frac{f}{f_e}\right)^{mf}, \quad f_e = \frac{1}{\tau_e}$$



At low densities in the channel, traps take a longer time to exchange with extended states than the transit time

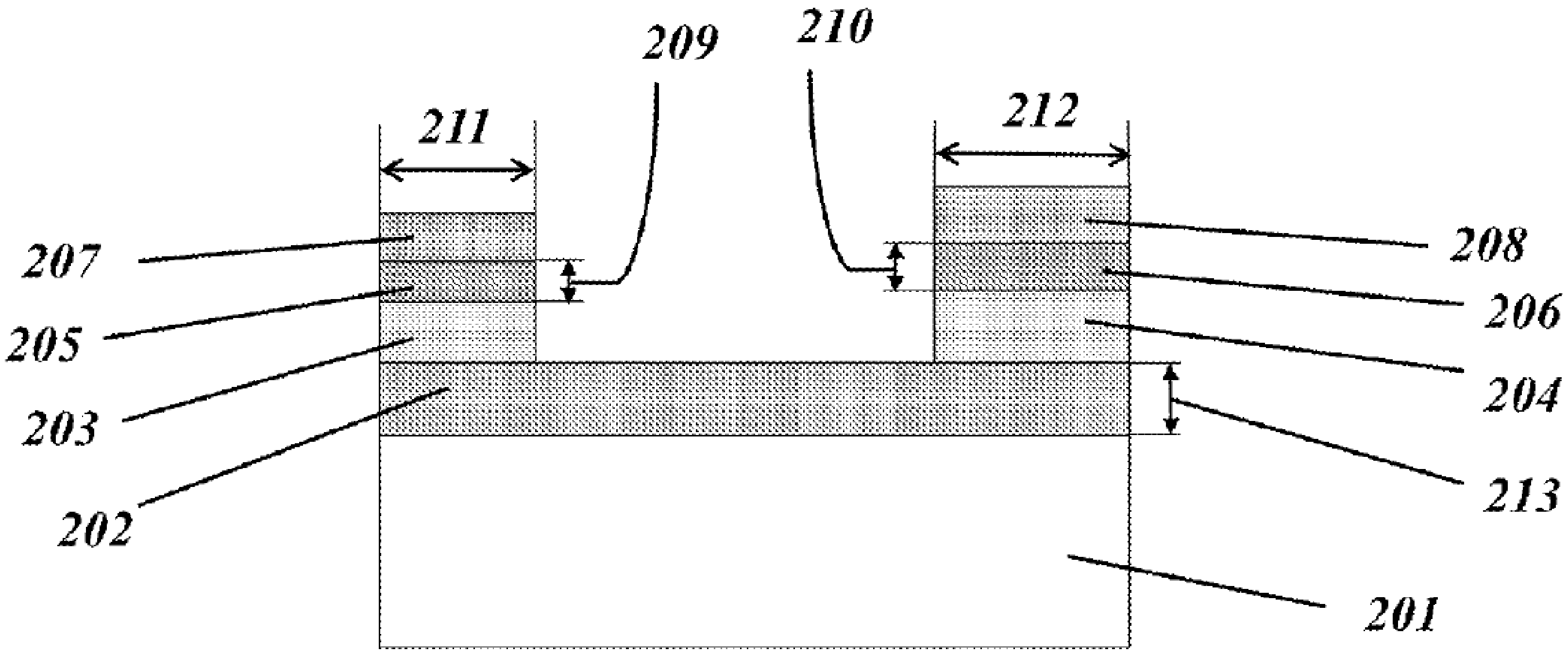
From S. Bhalerao, A. Koudymov, M. Shur, T. Ytterdal, W. Jackson, and C. Taussig, Compact capacitance model for printed thin film transistors with non-ideal contacts, International Journal of High Speed Electronics and System Vol. 20, No. 4, pp. 801-814, December 2011, B. Iniguez and M. Shur Editors

Application of dispersion for light sensing



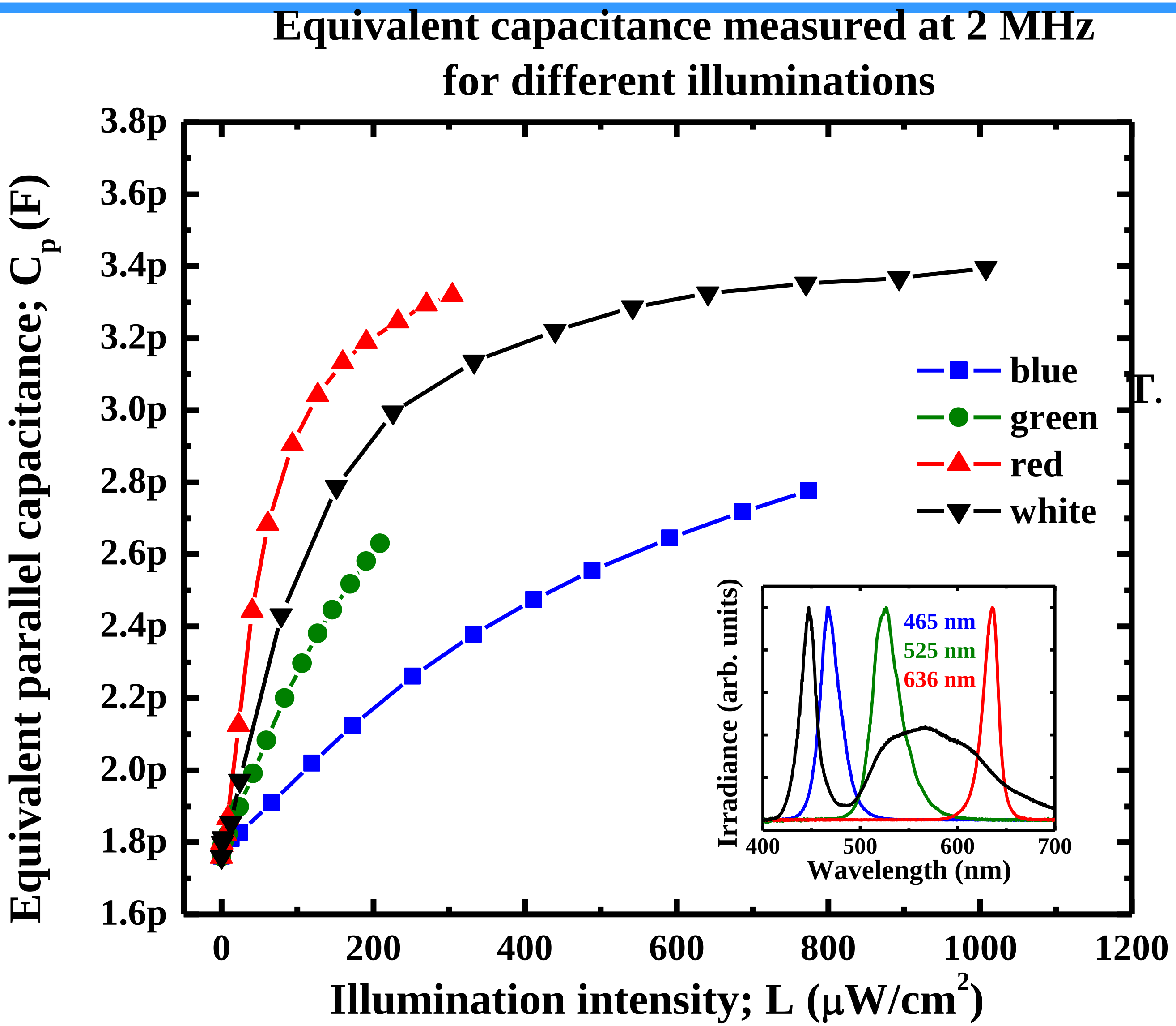
T. Saxena, P. S. Dutta, S. L. Roumiantsev, M. Shur Tunable photocapacitive optical radiation sensor enabled radio transmitter and applications thereof, US Patent Application 2016/0041030, Feb. 11 (2016)

Implementation



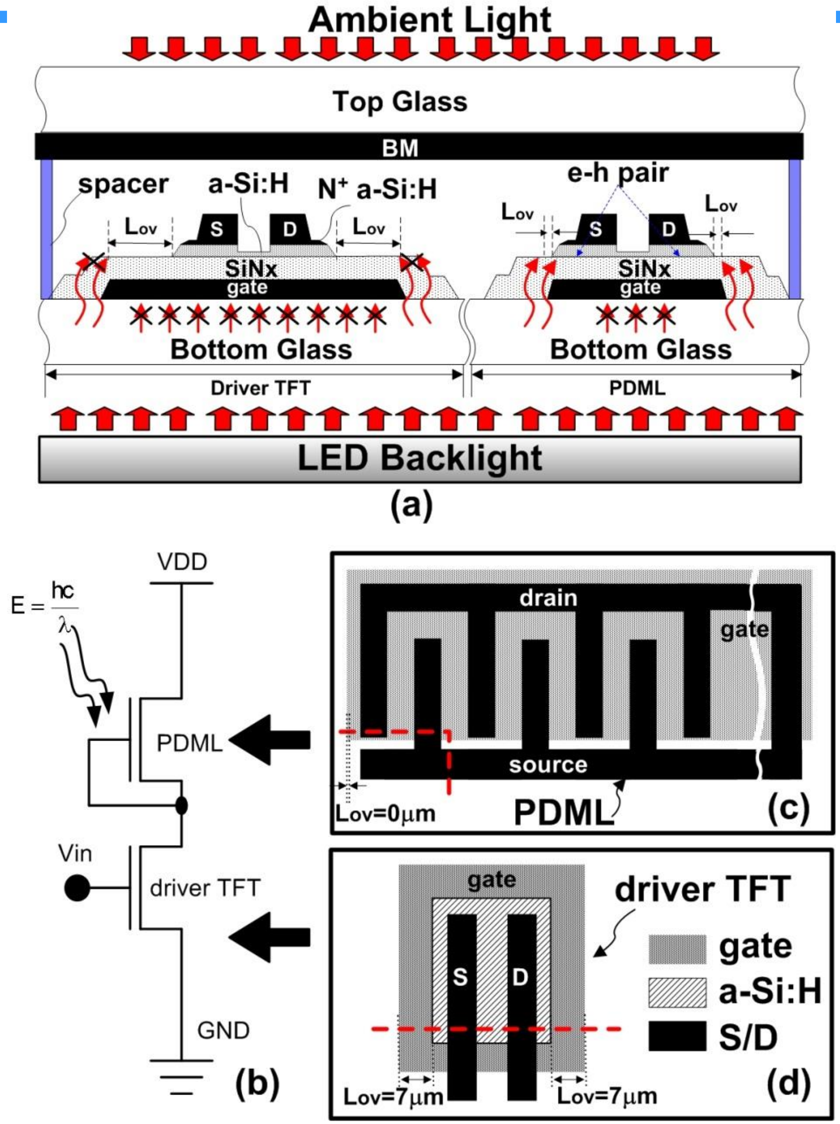
T. Saxena, P. S. Dutta, S. L. Roumiantsev, M. Shur Tunable photocapacitive optical radiation sensor enabled radio transmitter and applications thereof, US Patent Application 2016/0041030, Feb. 11 (2016)

Light sensor



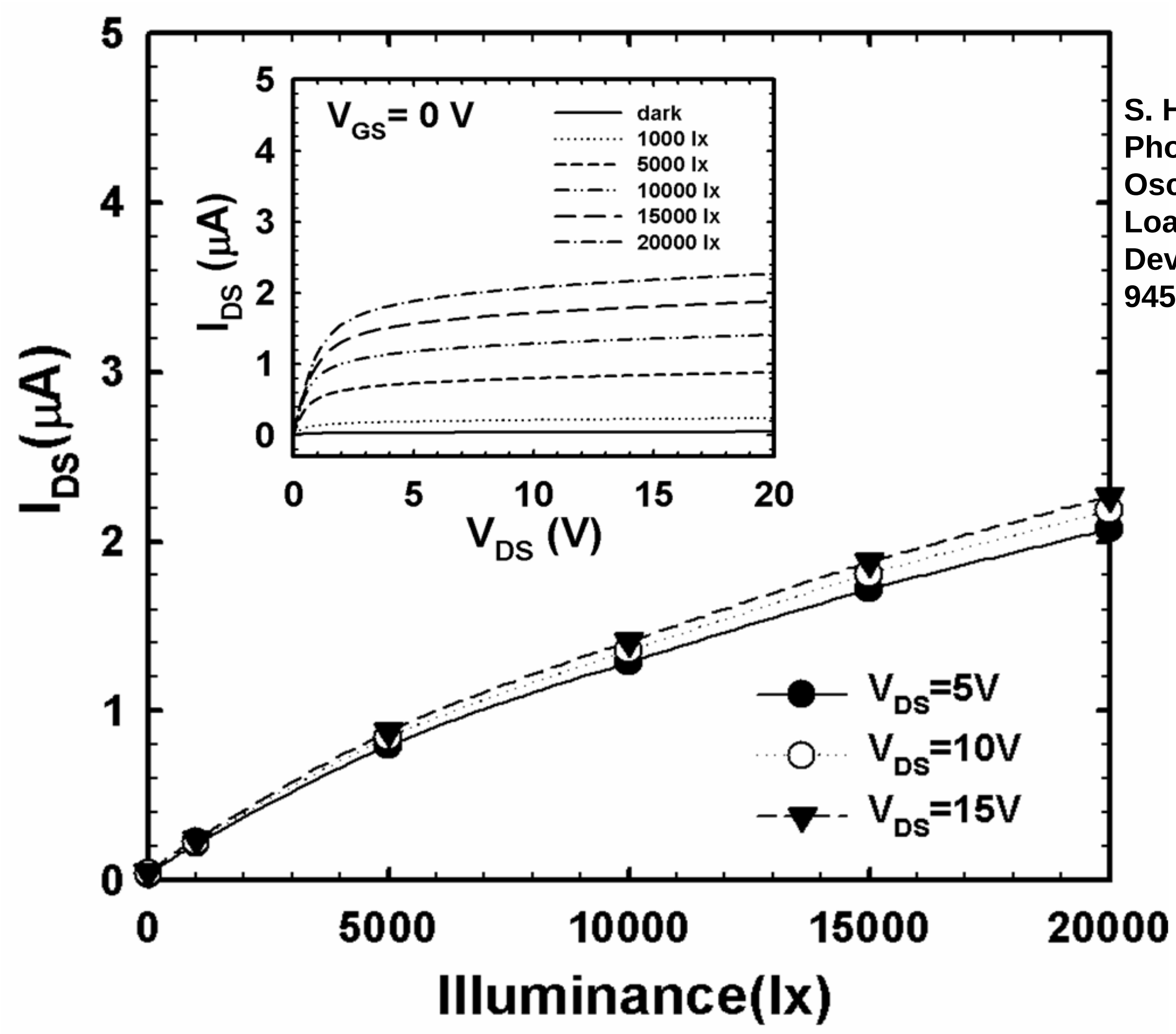
T. Saxena; M. Shur, "Silicon-on-Insulator Photoimpedance Sensor Using Capacitance Dispersion," in IEEE Transactions on Electron Devices , vol. PP, no.99, pp.1-5 June (2016)

Traps lead to TFT characteristics dependence on ambient light



S. H. Jin, M.-S. Park, and M. S Shur, Photosensitive Inverter and Ring Oscillator with Pseudo Depletion Mode Load for LCD Applications, IEEE Electron Device Letters, Vol. 30, Issue 9, pp. 943 – 945, September (2009)

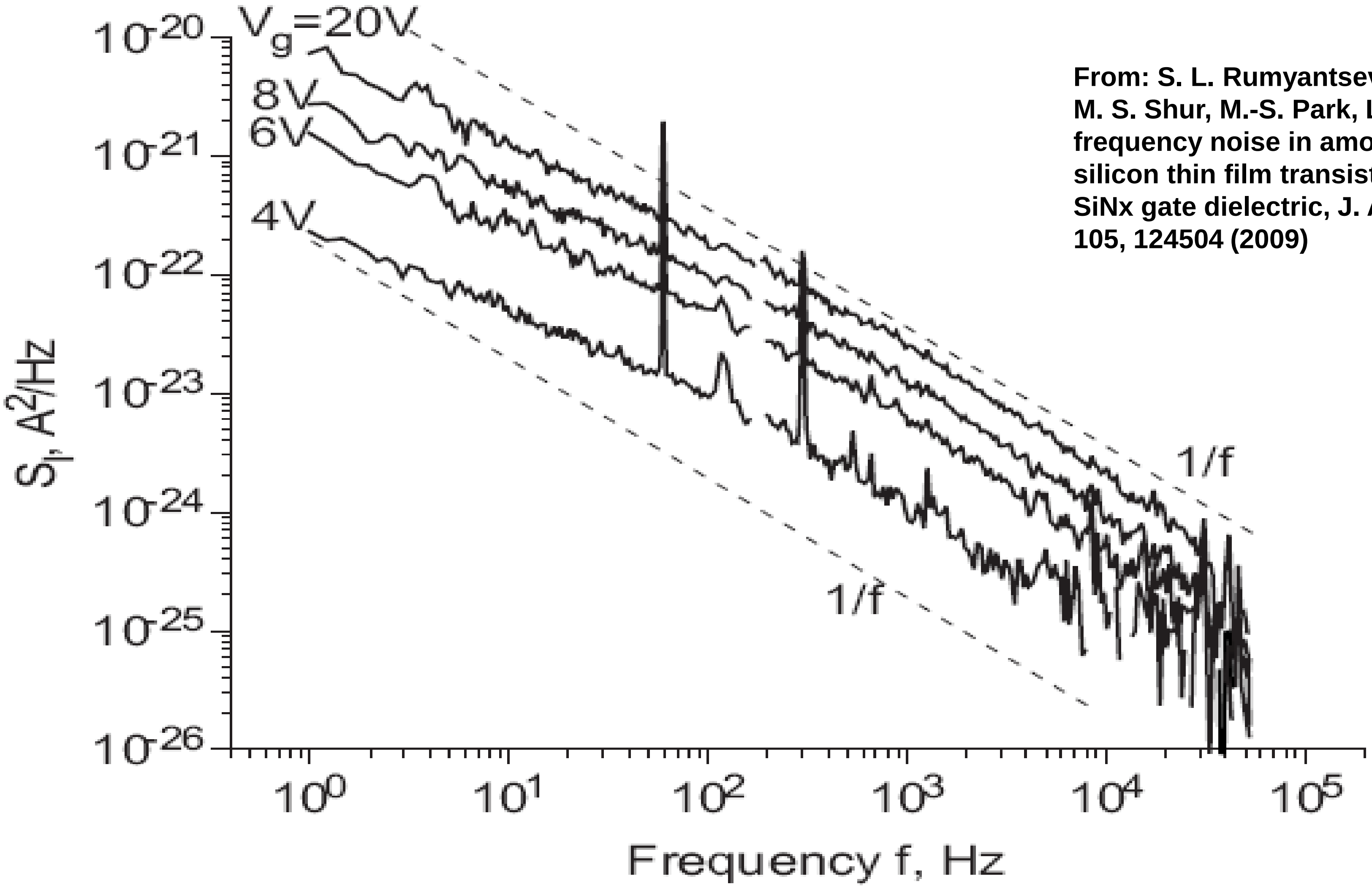
Non-linear dependence on illuminance



S. H. Jin, M.-S. Park, and M. S Shur, Photosensitive Inverter and Ring Oscillator with Pseudo Depletion Mode Load for LCD Applications, IEEE Electron Device Letters, Vol. 30, Issue 9, pp. 943 – 945, September (2009)

NOISE

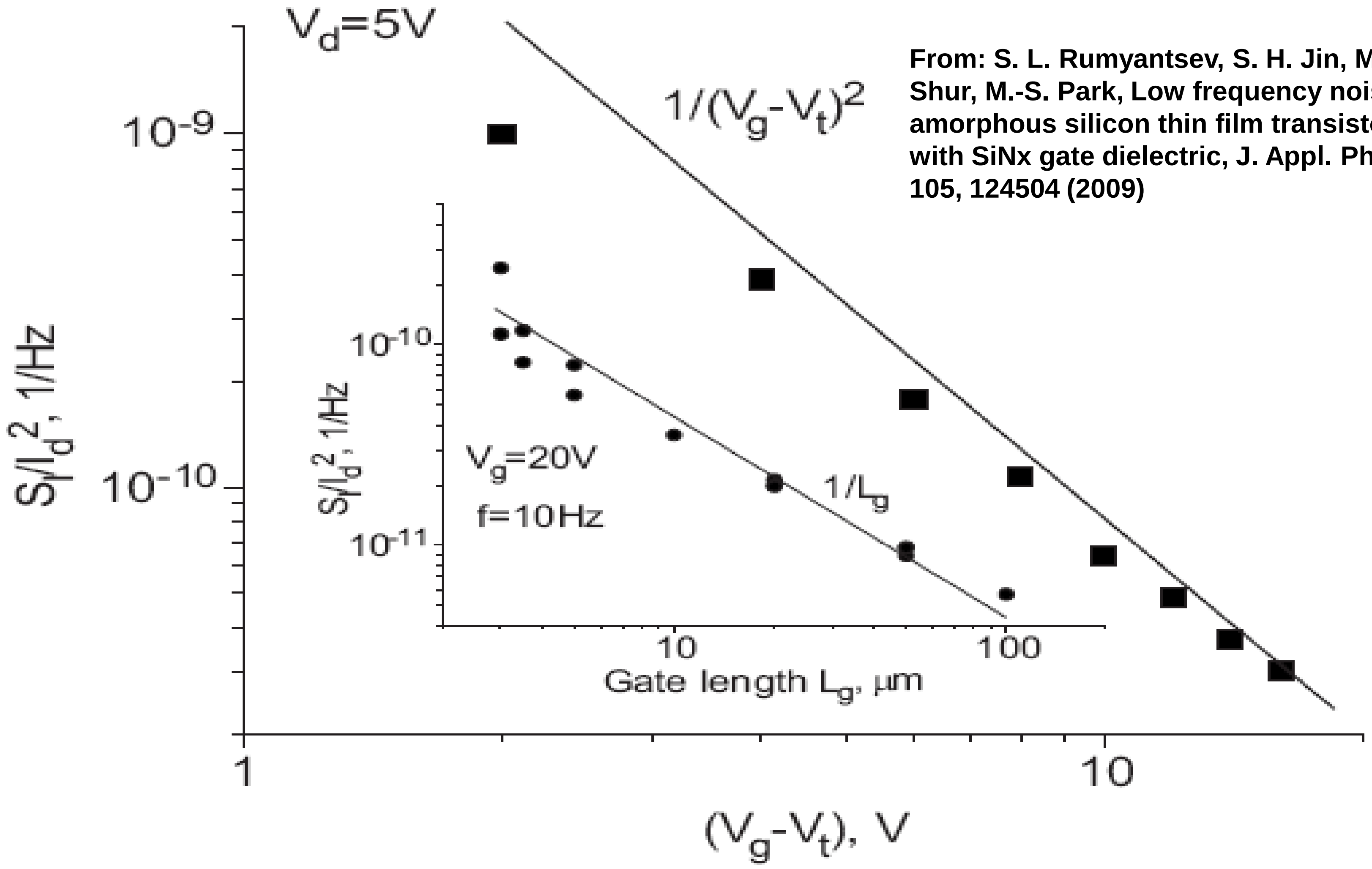
Gate voltage dependent 1/f noise



From: S. L. Rumyantsev, S. H. Jin, M. S. Shur, M.-S. Park, Low frequency noise in amorphous silicon thin film transistors with SiNx gate dielectric, J. Appl. Phys. 105, 124504 (2009)

Michael Shur (shurm@rpi.edu)

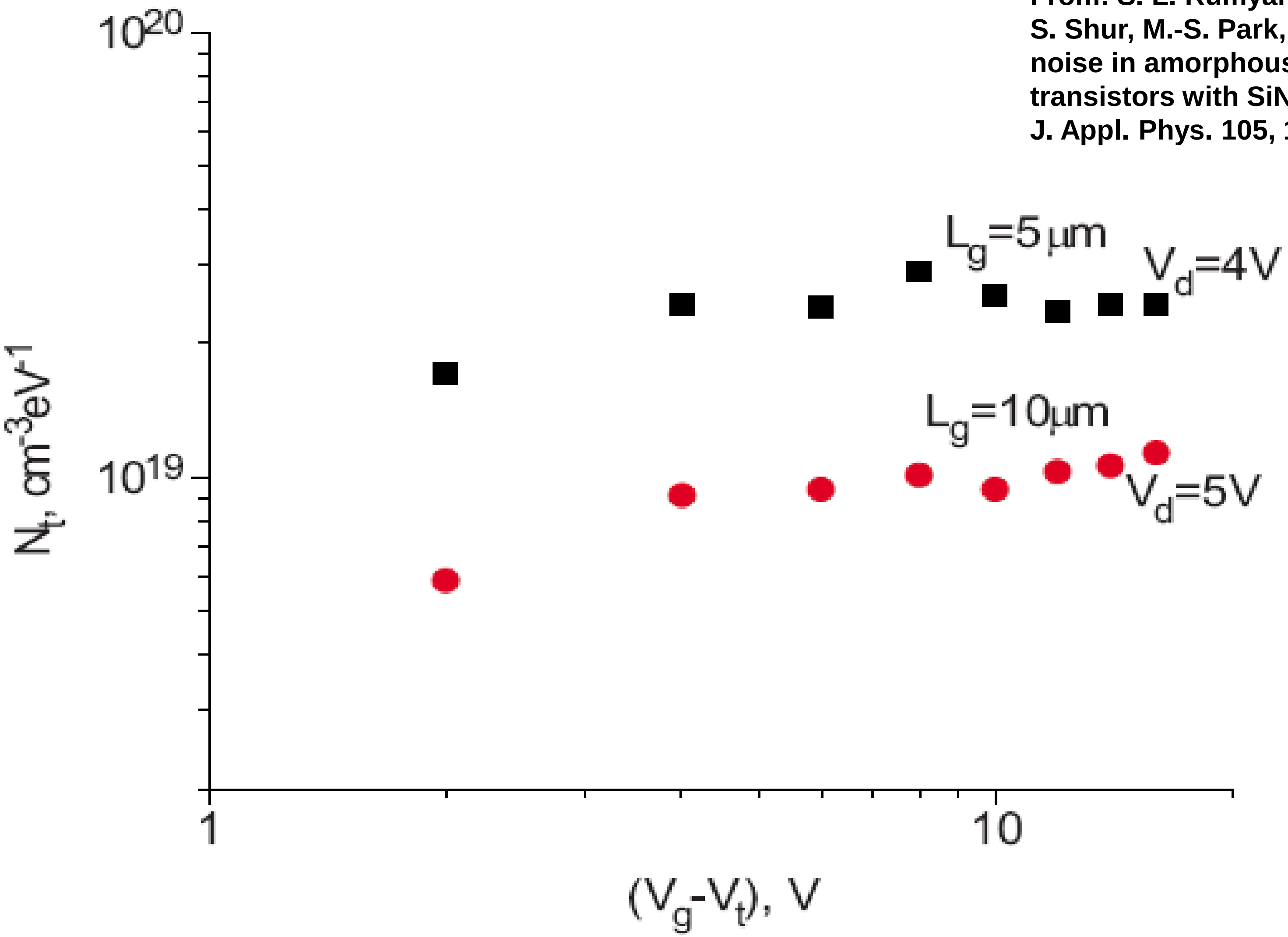
Noise much large in short channel devices



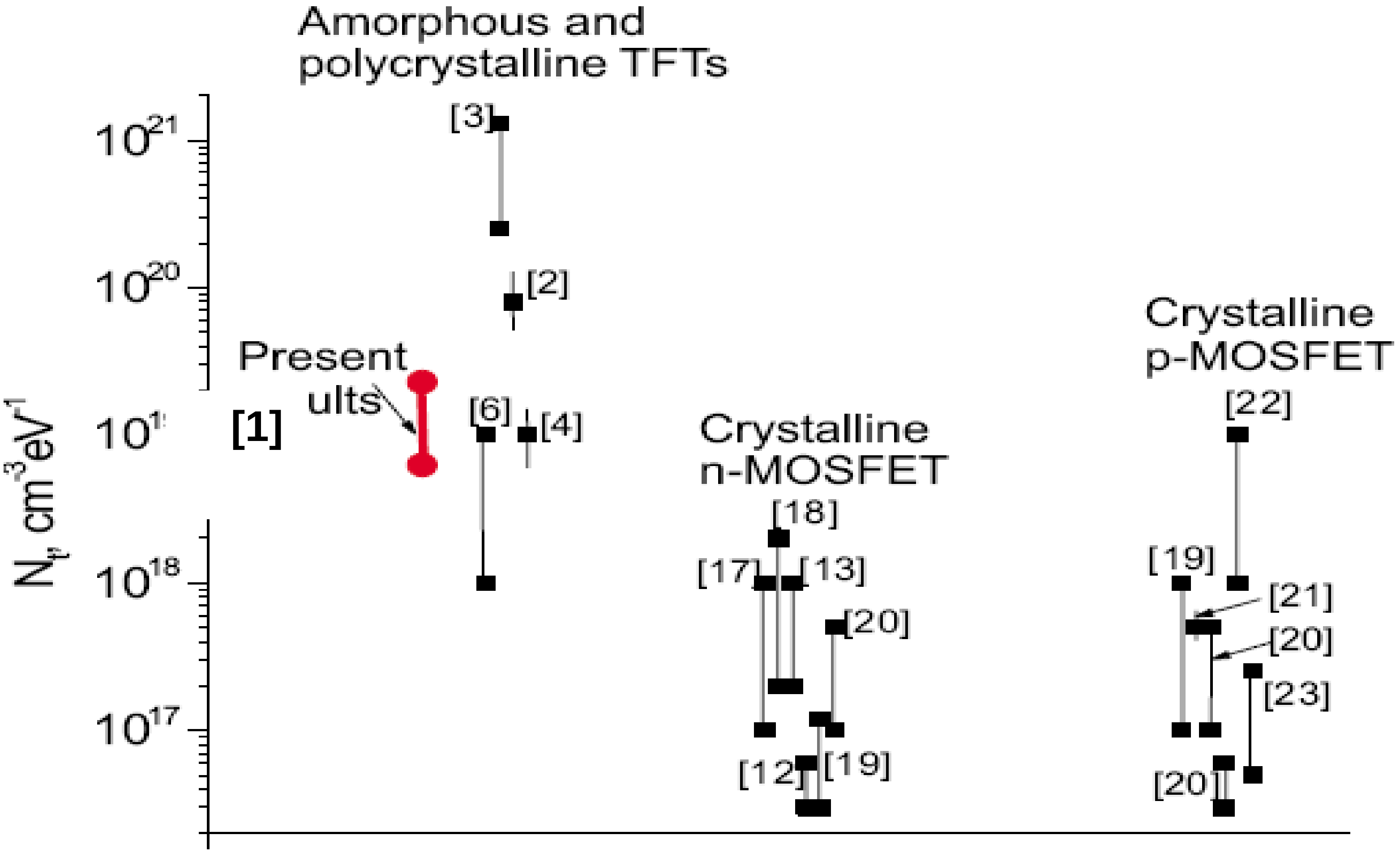
From: S. L. Rumyantsev, S. H. Jin, M. S. Shur, M.-S. Park, Low frequency noise in amorphous silicon thin film transistors with SiNx gate dielectric, J. Appl. Phys. 105, 124504 (2009)

Trap density can be extracted from noise data

From: S. L. Rumyantsev, S. H. Jin, M. S. Shur, M.-S. Park, Low frequency noise in amorphous silicon thin film transistors with SiNx gate dielectric, J. Appl. Phys. 105, 124504 (2009)



Noise: TFTs and Crystalline FETs (after [1])



From: S. L. Rumyantsev, S. H. Jin, M. S. Shur, M.-S. Park, Low frequency noise in amorphous silicon thin film transistors with SiNx gate dielectric, J. Appl. Phys. 105, 124504 (2009)

References

[1]JS. L. Rumyantsev, S. H. Jin, M. S. Shur, M.-S. Park, Low frequency noise in amorphous silicon thin film transistors with SiNx gate dielectric, J. App. Phys, J. Appl. Phys. 105, 124504 (2009)

[2]J. Rhayem, D. Rigaud, and M. Valenza, J. Appl. Phys. **87**, 2983 (2000).

[3]L. Pichon,_ A. Boukhenoufa, C. Cordier, and B. Cretu J. Appl. Phys. **100**, 054504 (2006).

[4]T. Hatzopoulos, N. Arpatzanis, D. H. Tassis, C. A. Dimitriadis, F. Templier, M. Oudwan, and G. Kamarinos, Solid-State Electronics **51**, 726 (2007).

[6]M. Rahal, M. Lee, and A. P. Burdett, IEEE Trans. Electron Devices **49**, 319(2002).

[12]Y. Allogo, M. Marin, M. de Murcia, P. Linares, D. Cottin, Solid-State Electronics **46**, 977 (2002).

[13]S. L. Rumyantsev, M. S. Shur, M. E. Levinshtein, P. A. Ivanov, J. W. Palmour, M. K. Das, and B. A. Hull**,** J. Appl. Phys. **104**, 094505 (2008).

[17]K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, IEEE Trans. Electron Devices, **37**, 654 (1990).

[19]Y. A. Allogo, M. Marin, M. de Murcia, P. Llinares, D. Cottin, Solid-State Electronics **46,** 977 (2002).

[20]M. von Haartman, Solid-State Electronics **51,** 771 (2007).

[21]M. Fadlallah, G. Ghibaudo, J. Jomaah, M. Zoaeter, G. Guegan, Microelectronics Reliability **42** 41 (2002).

[23]Jeong-Soo Lee, Daewon Ha, Yang-Kyu Choi, Tsu-Jae King, and Jeffrey Bokor, IEEE El. Dev. Lett. **24**, 31 (2003).

CONCLUSIONS

- **The challenge in the compact modeling of Thin Film Transistors (TFTs) is to accurately reproduce all regimes of operation (leakage, subthreshold, and above threshold)**

- **The developed models are suitable for the device characterization and parameter extraction even for the TFTs with non-ideal behavior**

- **These models account for non-ideal effects including gate-dependent mobility, contact effects and capacitance dispersion**

Acknowledgment

This work was supported in part by the U.S. Army Research Laboratory through the Collaborative Research Alliance (CRA) for Multi-Scale Modeling of Electronic Materials (MSME) (Project Monitor Dr. Meredith Reed).

Michael Shur (shurm@rpi.edu)