EMBEDDED OXIDE SEMICONDUCTOR MEMORIES: A KEY ENABLER FOR LOW-POWER ULSI

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Oxide semiconductor field-effect transistors (OSFETs) have been actively developed for display applications. The off-state current in an OSFET is more than ten orders of magnitude lower than that in a Si-FET [1]. Displays using OSFET backplanes achieve low power consumption through idling-stop (IDS) driving [2], which dramatically decreases the refresh rate when the flame image is static.

The extremely low off-state current of the OSFET is applicable not only to displays but to various other applications. Recently, OSFET technology has been applied to ULSI memory [3-6]. When used as a pass transistor connected to a storage node (SN), an OSFET allows the long-time retention of electric charge in the SN. Unlike conventional DRAM, the memory with OSFET eliminates the need for frequent refresh operations and reduces the refresh power. Furthermore, the memory can perform power gating (PG) in the idle state, solving the problem of leakage power observed in conventional SRAM. Thus, OSFETs enable low-power ULSI.

Figure 1 shows three types of OS memory with different features. DOSRAM (Dynamic Oxide Semiconductor RAM) [3] has a small number of elements (1T1C) and can achieve a small cell area. OSSRAM (Oxide Semiconductor Static RAM) [4] is a combined circuit that plays two roles. The normal-operation portion of the circuit operates as fast as conventional SRAM; however, it is volatile. The backup portion can retain data over a long period. In the idle state, the memory cell transfers data from the normal-operation portion to the backup portion and cuts the leakage power by performing PG. In the recovery operation, the memory cell restores the data from the backup portion to the normal-operation portion and immediately resumes its operation. The cell area and operation speed of NOSRAM (Nonvolatile Oxide Semiconductor RAM) [5] are between those of DOSRAM and OSSRAM. Multilevel NOSRAM [5] has also been proposed with the aim of reducing cost per bit. All kinds of OS memory can be simultaneously fabricated by the same process on the same substrate.

When embedded in computer architecture, OS memory enables normally-off (N-off) operation, wherein CPU processing and idle state are operated in the power-on and power-gate modes, respectively. The N-off operation effectively reduces the power consumption by reducing the leakage power to substantially zero. For the N-off operation, the embedded memory should operate at a high speed (or backup and restore data at a high speed) and has to retain data over a long period in PG. These requirements are met by DOSRAM, NOSRAM, and OSSRAM. Figure 2 shows a die photograph and specifications of a prototype microprocessor with embedded DOSRAM.

The performance of LSI devices will be further improved in the future by miniaturization, which increases the integration and leakage current of FETs. Therefore, lower power consumption will be particularly demanded. OS-LSI is a prospective candidate that achieves both higher performance and lower power consumption. In addition to memory devices, the OS technology will be adopted in global-shutter image sensors, nonvolatile FPGAs, analog circuits such as A/D convertors, neural networks, and other applications.

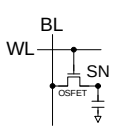
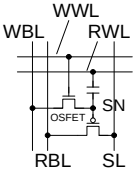
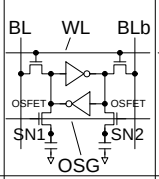
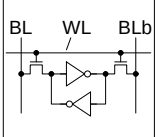
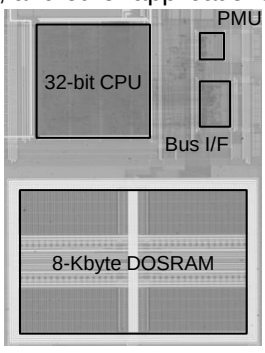
Type	DOSRAM	NOSRAM	OSSRAM	Conv. SRAM
Element	1Tr and 1Cap	2Tr and 1Cap	8Tr and 2Cap	6Tr
Circuit diagram				
Cell area	< 0.5	< 0.8 to 0.9	1.55	1 (Ref.)
Speed	Slower	Medium	~1	1 (Ref.)
Leakage	0nW	0nW	< nW @PG	~μW

Fig. 1. Pros/Cons of oxide semiconductor memories.



Technology	65nm CMOS 60nm OSFET 1P6M BEOL
Frequency	30MHz
Voltage	Core: 1.1V OSFET: 3.3V
Memory	DOSRAM (8KB)
Cell area	2.9 μm^2
Bus width	32bit
Chip size	1.05mm^2
Leakage	< 10nW @ PG
Power*	3.4 μW @ N-off

NOTE: *) Active/Sleep ratio = 1:100.

Fig. 2. Die photograph and specifications.

References [1] N. Kimizuka and S. Yamazaki, "Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Fundamentals" Wiley-SID Series in Display Technology (2016). [2] S. Amano et al., SID Symp. Dig. Tech. Pap. (2010). [3] T. Onuki et al., Symp. VLSI Circuits (2016). [4] H. Tamura et al., IEEE Micro 34 (2014). [5] T. Matsuzaki et al., ISSCC Dig. Tech. (2015). [6] S. H. Wu et al., Symp. VLSI Technology (2016)