CMOS VLSI Correlator Design for Radio-Astronomical Signal Processing

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Stepan Lapshev

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Abstract

Multi-element radio telescopes employ methods of indirect imaging to capture the image of the sky. These methods are in contrast to direct imaging methods whereby the image is constructed from sensor measurements directly and involve extensive signal processing on antenna signals. The Square Kilometre Array, or the SKA, is a future radio telescope of this type that, once built, will become the largest telescope in the world. The unprecedented scale of the SKA requires novel solutions to be developed for its signal processing pipeline one of the most resource-consuming parts of which is the correlator. The SKA uses the FX correlator construction that consists of two parts: the F part that translates antenna signals into frequency domain and the X part that cross-correlates these signals between each other. This research focuses on the integrated circuit design and VLSI implementation issues of the X part of a very large FX correlator in 28 nm and 130 nm CMOS. The correlator's main processing operation is the complex multiply-accumulation (CMAC) for which custom 28 nm CMAC designs are presented and evaluated. Performance of various memories inside the correlator also affects overall efficiency, and input-buffered and output-buffered approaches are considered with the goal of improving upon it. For output-buffered designs, custom memory control circuits have been designed and prototyped in 130 nm that improve upon eDRAM by taking advantage of sequential access patterns. For the input-buffered architecture, a new scheme is proposed that decreases the usage of the input-buffer memory by a third by making use of multiple accumulators in every CMAC. Because cross-correlation is a very data-intensive process, high-performance SerDes I/O is essential to any practical ASIC implementation. On the I/O design, the 28 nm full-rate transmitter delivering 15 Gbps per lane is presented. This design consists of the scrambler, the serialiser, the digital VCO with analog fine-tuning and the SST driver including features of a 4-tap FFE, impedance tuning and amplitude tuning.

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Contents

List of figures

List of tables

List of acronyms and abbreviations

AC	Alternating current
ASIC	Application-specific integrated circuit
CLA	Carry-lookahead adder
CMAC	Complex multiplier-accumulator
CML	Current-mode logic
CMOS	Complementary metal-oxide semiconductor
CSA	Carry-save adder
CV	Coefficient of variation
DAC	Digital-to-analog converter
DC	Direct current
DET	Dual-edge-triggered
DFT	Discrete Fourier Transform
DRAM	Dynamic random-access memory
DTSCR	Diode-triggered silicon controlled rectifier
EDA	Electronic design automation
eDRAM	Embedded dynamic random-access memory
ESD	Electrostatic discharge
FA	Full adder
FF	Flip-flop
FFE	Feed-forward equaliser
GF	GlobalFoundries
HA	Half adder
IC	Integrated circuit
IDDQ	Leakage current
I/O	Input/output
IP	Intellectual property

LFSR	Linear-feedback shift register
LVDS	Low-voltage differential signalling
MC	Monte Carlo
MOSFET	Metal-oxide-semiconductor field-effect transistor
MSB	Most significant bit
MUX	Multiplexer
PDP	Power-delay product
PFA	Partial full adder
PLL	Phase-locked loop
PRNG	Pseudorandom number generator
PVT	Process, voltage and temperature
RAM	Random-access memory
RSD	Relative standard deviation
SAM	Sequential-access memory
SCR	Silicon controlled rectifier
SD	Standard deviation
SerDes	Serialiser/deserialiser
SET	Single-edge-triggered
SI	Sub-integration
SST	Source-series termination
VCO	Voltage-controlled oscillator
VLSI	Very-large-scale integration