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A Novel Five-Level Semi-Bridgeless Power Factor Correction Topology

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***Abstract*—This paper proposes a novel topology of a multilevel converter for power factor correction (PFC) applications. The proposed topology, with a split dc-link, can produce five distinct voltage levels with a reduced number of power devices. Inherently, the proposed topology operates with unitary power factor, sinusoidal grid current, and controlled dc-link voltage. The functional principle of the proposed topology is described in detail to show its benefits compared to the classical PFC topologies. The current control methodology adopts the discrete-time nature of the topology to define the distinct states throughout a control period. A laboratorial prototype was developed to validate the proposed topology under real conditions of operation, and the hardware structure and the implemented control algorithm are presented in this paper. The experimental validation shows a grid current with reduced harmonic distortion, a controlled voltage in the split dc-link, and a unitary power factor operation.**

***Keywords*—Power Factor Correction, Five-Level, Power Quality, Smart Grid.**

I. Introduction

In the last decades, due to the nonlinear electrical appliances, power factor correction (PFC) topologies have gained more notoriety with the purpose of mitigating power quality issues associated with power factor and current harmonic distortion in smart grids [1][2][3][4]. PFC topologies are used in numerous industrial applications in order to accomplish with normative restrictions, as the international standards IEEE-519, IEC 61000 and EN 5016 [5][6]. For instance, PFC topologies can be employed in variable speed ac drives, high-power lighting systems, power supplies, and electric vehicle battery chargers [7][8][9][10].

Depending on the application and the desired amplitude for the output dc-link voltage, PFC topologies can be implemented, mainly, with converters based on buck- or boost-type structures [11][12][13][14][15]. The most applicable three-phase PFC topologies for industrial purposes are considered in [16] and [17], where a tradeoff between efficiency and power density is established. Regarding single-phase structures, a detailed review of the traditional PFC topologies is presented and discussed in [18] and [19], where buck- and boost-type structures of multilevel, isolated, bridgeless, and interleaved converters are highlighted. Since PFC topologies connected to the power grid produce a voltage according to the desired grid current, increasing the number of produced voltage levels will improve the grid current quality [20][21]. However, the required hardware will be directly affected, mainly in terms of gate-drivers, power semiconductors and voltage sensors [22]. As a contribution for multilevel PFC boost-type structures, this paper proposes a novel five-level semi-bridgeless PFC topology. The proposed topology, presented in Fig. 1, has a reduced number of power devices to state five voltage levels, operates with unitary power factor and sinusoidal grid current, as well as controlled voltage in the split dc-link.

A set of new efficient bridgeless PFC topologies operating in discontinuous conduction mode is proposed in [23]; however, it should be noted that the proposed topologies are based on the Cuk converter rather than multilevel topologies. An improved bridgeless PFC topology is proposed in [12], but due to its boost-double structure, the dc-link voltage is greater than the double of the grid peak voltage. A review about PFC converters based on the boost-type dc-dc converter is summarized in [24], where an evolution from the conventional boost converter is presented, but the voltage levels are limited to three. With the same limitation, a dual-boost bridgeless PFC topology is presented in [14]. A novel PFC topology of multilevel buck-boost-type converter with reduced number of power devices is proposed in [25], however, it has two independent dc-links, leading to difficulties in regulating the dc-link voltage with unbalanced loads, and the major disadvantage occurs when it operates as a boost-type converter, since each dc-link voltage value is greater than the grid peak voltage. A single-dc-source five-level PFC topology is proposed in [26], however, it requires a significant number of switching devices and it has two independent dc-links, which is limitative for specific applications. A five-level PFC topology with a split dc-link and reduced power devices is proposed in [27], however, it requires a dedicated dead-time control algorithm to avoid short-circuits

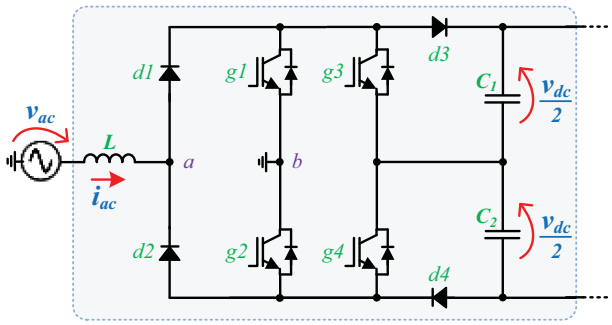

Fig. 1. Proposed five-level semi-bridgeless PFC topology.

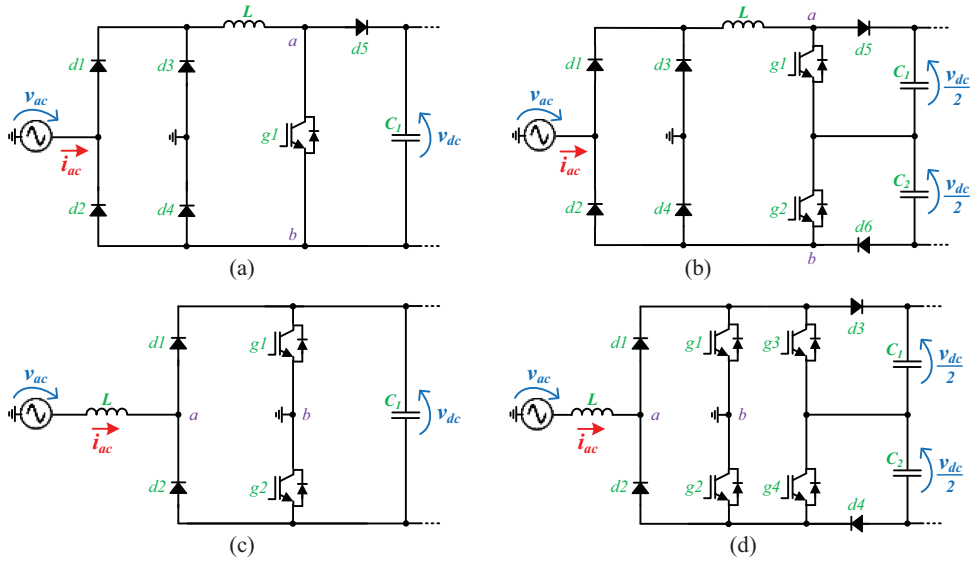

Fig. 2. Derivation of the proposed topology: (a) Traditional two-level PFC; (b) PFC employing a three-level dc-dc converter; (c) Three-level semi-bridgeless PFC; (d) Proposed five-level semi-bridgeless PFC.

in the split dc-link. A five-level VIENNA-type PFC topology with three switching devices is proposed in [28], but each dc-link capacitor should withstand the amplitude of the grid voltage, limiting this topology for specific applications. In summary, the proposed PFC topology has a single dc-link interface, which is the most convenient approach for industrial applications, and allows to establish five-levels with a reduced number of power devices.

The organization of the rest of this paper is as follows: The derivation of the proposed topology and a comparative analysis are described in Section II; The analytical modeling and control concepts for the proposed topology are given in Section III; The experimental system evaluation of the proposed topology is presented in Section IV; The main conclusions are presented in Section V.

II. Derivation of the Proposed Five-Level Semi-Bridgeless PFC Topology

The derivation of the proposed topology is presented in this section as a comparison with the traditional boost-type topologies employed in PFC circuits, as presented in Fig. 2. The topology presented in Fig. 2(a) is the best known and more employed in PFC applications. This topology is constituted by two converters, namely an ac-dc diode bridge connected in series with a dc-dc boost. It has a reduced number of power devices, but only allows to state two voltage levels. On the other hand, the topology presented in Fig. 2(b) allows to state three voltage levels. This topology is also constituted by an ac-dc converter in series with a dc-dc converter, however, the latter has a modified structure to take advantage of the split dc-link voltage. Comparing with the previous topology (cf. Fig. 2(a)), this one requires two additional power devices (a diode and a switching device), but the value of the coupling passive filter can be reduced for the same harmonic distortion in the grid current. A semi-bridgeless topology with a reduced number of power devices and able to state three voltage levels is presented in Fig. 2(c) [20]. Comparing with the previous one (cf. Fig. 2(b)), this topology has less power devices to obtain the same harmonic distortion when employing a coupling filter with the same value. By combining the advantages of the topologies presented in Fig. 2(b) and in Fig. 2(c), it is possible to obtain a novel boost-type PFC topology, as shown in Fig. 2(d). This converter has the same features as the previous one in terms of low harmonic distortion of the grid current, operation with unitary power factor, and controlled dc-link voltage. Moreover, comparing with the converter presented in Fig. 2(b), substituting the diodes *d3* and *d4* by two switching devices endows the proposed topology with five voltage levels, with the advantage of reducing the value of the coupling filter with the power grid. The essential comparison between the aforementioned topologies is summarized as follows: In terms of number of power devices (diodes and switching devices - IGBTs in this case), the traditional PFC boost-type is constituted by six devices, the PFC dc-dc three-level by eight, the PFC semi-bridgeless by four, and finally, the proposed topology by eight; Regarding the voltage levels produced by these topologies, the traditional PFC boost-type produces two voltage levels, the multilevel boost-type and the semi-bridgeless topologies produce three voltage levels, and the proposed topology produces five voltage levels; In terms of dc-link capacitors, the proposed PFC topology and the dc-dc three-level PFC have a split dc-link. As shown in Fig. 2(d), the proposed topology is constituted by four diodes (*d1*, *d2*, *d3*, and *d4*) and four IGBTs (*g1*, *g2*, *g3*, and *g4*). A relevant advantage of the proposed topology is related with the IGBTs switching, since they are not always switched along the positive and negative half-cycles. During the positive half-cycle, the IGBTs *g1* and *g2* are switched according to the state of the voltage levels (0, $+v_{dc}$, and $+v_{dc}/2$) and, during the negative half-cycle, the IGBTs *g3* and *g4* are also switched according to the state of the voltage levels (0, $-v_{dc}$, and $-v_{dc}/2$).

The different states assumed by the proposed topology during the positive and negative half-cycles are summarized in Fig. 3. As can be observable, at maximum, a single IGBT is ON during each state, representing a relevant advantage of the proposed PFC topology. Moreover, a single IGBT is switched

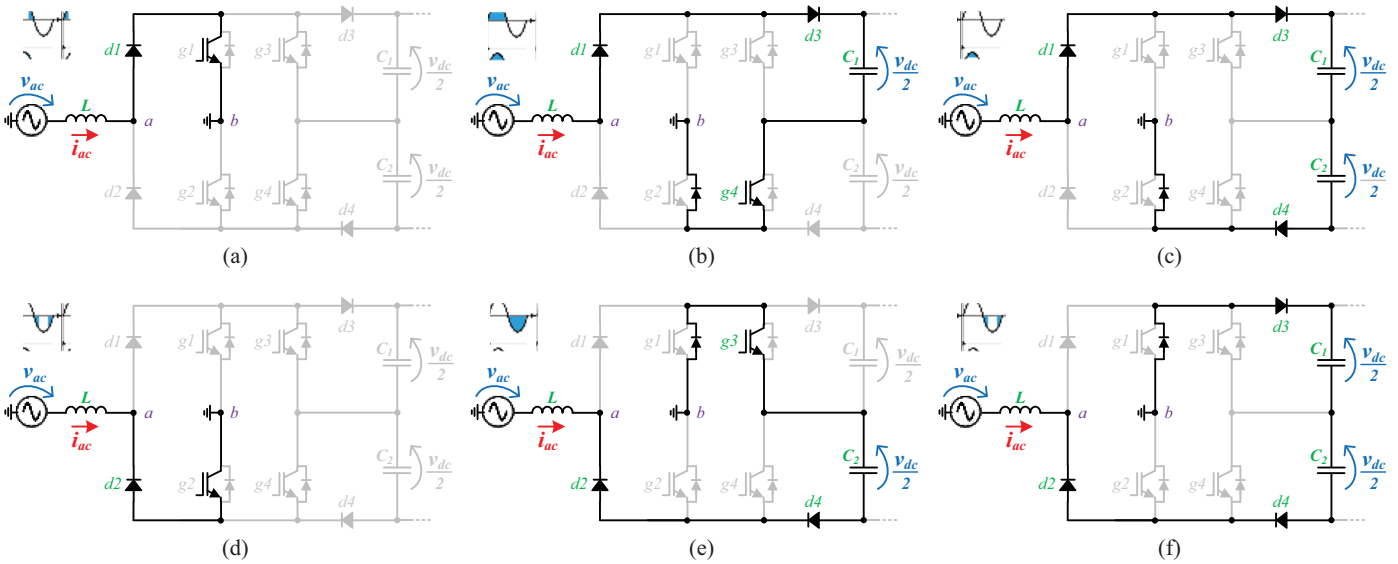

Fig. 3. Different states assumed by the proposed topology according to the positive and negative half-cycles: (a) $v_{ab} = 0$; (b) $v_{ab} = +v_{dc}/2$; (c) $v_{ab} = +v_{dc}$; (d) $v_{ab} = 0$; (e) $v_{ab} = -v_{dc}/2$; (f) $v_{ab} = -v_{dc}$;

ON when it is required to state the level 0 or $v_{dc}/2$ (or $-v_{dc}/2$). The level v_{dc} (or $-v_{dc}$) is stated using the diodes and the reverse diodes of the IGBTs during the OFF state.

III. Analytical Modeling and Control Concepts for the Proposed Topology

The control algorithm for the proposed topology is mainly based on three parts: dc-link voltage control; reference current generation; grid current control. Taking into account the split dc-link, two proportional-integral (PI) controllers are used to regulate both dc-link voltages. In the control algorithm, a PI controller is employed to regulate the voltage v_{dc1} (voltage between the positive output terminal and the middle of the dc-link) during the positive half-cycle (p_{PI1}) and another PI controller is employed during the negative half-cycle (p_{PI2}) to regulate the voltage v_{dc2} (voltage between the middle of the dc-link and the negative output terminal). By using this strategy, both voltages are regulated according to their references, which are selected to be greater than the grid peak voltage, since the proposed topology is of the boost-type. The output of each PI controller is summed with the dc operating power and, as the rms value of the grid voltage (V_{AC}) is constant, it is possible to define the theoretical grid current for the required dc operating power. The theoretical grid current, which is used as the reference current (i_{ac}^*), is established according to:

$$i_{ac}^*(t) = \frac{i_{dc}(t)\left(v_{dc1}(t) + v_{dc2}(t)\right) + p_{PI1} + p_{PI2}}{{V_{AC}}^2}\, v_{ac}, \qquad (1)$$

where i_{dc} is the output current. By analyzing (1), it is noticeable that the waveform of i_{ac}* is determined by the waveform of the grid voltage (v_{ac}). However, in the control algorithm, a phase-locked loop (PLL) strategy is used to avoid such influence and to synchronize the grid current only with the fundamental component of the grid voltage, i.e., for a unitary power factor operation. Taking into account that the control algorithm is digitally implemented, the current control methodology adopts the discrete-time nature of the proposed topology to define the distinct converter states throughout a control period. Therefore, throughout a control period [k, k+1], the state of the converter is selected to get the minimum error between the reference current established during the control period [k-1, k] and the measured current in the instant [k]. As the proposed topology has six valid states (three for each half-cycle), during each control period it can assume each one of such states. Consequently, the switching functions are described by:

$$S_{v_{ac}>0} = \begin{cases} 0,0,0,0 & if\ \ g_1 = 0,\ g_2 = 0,\ g_3 = 0,\ g_4 = 0; \\ 0,0,0,1 & if\ \ g_1 = 0,\ g_2 = 0,\ g_3 = 0,\ g_4 = 1; \\ 1,0,0,0 & if\ \ g_1 = 1,\ g_2 = 0,\ g_3 = 0,\ g_4 = 0; \end{cases} \qquad (2)$$

for the positive half-cycle, and by:

$$S_{v_{ac}<0} = \begin{cases} 0,1,0,0 & if\ \ g_1 = 0,\ g_2 = 1,\ g_3 = 0,\ g_4 = 0; \\ 0,0,1,0 & if\ \ g_1 = 0,\ g_2 = 0,\ g_3 = 1,\ g_4 = 0; \\ 0,0,0,0 & if\ \ g_1 = 0,\ g_2 = 0,\ g_3 = 0,\ g_4 = 0; \end{cases} \qquad (3)$$

for the negative half-cycle. The selection of each switching function is implemented in accordance with the grid voltage (v_{ac}) sign, which is also in accordance with the ac reference current sign, since the proposed topology operates with unitary power factor. The state variable equation describing the proposed topology dynamics is given as:

$$v_{ac}(t) = L\frac{di_{ac}(t)}{dt} + v_{ab}(t)\,, \qquad (4)$$

where L is the inductance value of the coupling filter and $v_{ab}(t)$ assumes one of the possibilities of the switching functions S, according to:

$$v_{ab}(t) = \begin{cases} v_{dc} & ,S_{v_{ac}>0} = 0,0,0,0 \\ v_{dc}/2 & ,S_{v_{ac}>0} = 0,0,0,1 \\ 0 & ,S_{v_{ac}>0} = 1,0,0,0 \\ 0 & ,S_{v_{ac}<0} = 0,1,0,0 \\ -v_{dc}/2 & ,S_{v_{ac}<0} = 0,0,1,0 \\ -v_{dc} & ,S_{v_{ac}<0} = 0,0,0,0 \end{cases}. \qquad (5)$$

From (4), the digital implementation using a forward Euler process results in:

$$v_{ac}[k] = \frac{L}{T_s}(i_{ac}[k+1] - i_{ac}[k]) + v_{ab}[k]\,, \tag{6}$$

which can be expressed as a function of the grid current in the instant [k] as:

$$i_{ac}[k+1] = i_{ac}[k] + \frac{T_s}{L}v_{ac}[k] - \frac{T_s}{L}v_{ab}[k]\,. \tag{7}$$

The obtained value from (7) is the desired ac current at the end of the control period, i.e., at the instant [k+1]. Since the voltage $v_{ab}[k]$ assumes the voltage of the dc-link ($+v_{dc}$, $+v_{dc}/2$, 0, 0, $-v_{dc}/2$, $-v_{dc}$), the variable $i_{ac}[k+1]$ can assume the values of:

$$i_{ac_{\{a,b,c,d,e,f\}}}[k+1] = \begin{cases} i_{ac}[k] + \frac{T_s}{L}v_{ac}[k] - \frac{T_s}{L}v_{dc}[k]\,. \\ i_{ac}[k] + \frac{T_s}{L}v_{ac}[k] - \frac{T_s}{L}\frac{v_{dc}}{2}[k]\,. \\ i_{ac}[k] + \frac{T_s}{L}v_{ac}[k]\,. \\ i_{ac}[k] + \frac{T_s}{L}v_{ac}[k]\,. \\ i_{ac}[k] + \frac{T_s}{L}v_{ac}[k] + \frac{T_s}{L}v_{dc}[k]\,. \\ i_{ac}[k] + \frac{T_s}{L}v_{ac}[k] + \frac{T_s}{L}\frac{v_{dc}}{2}[k]\,. \end{cases} \tag{8}$$

Therefore, the converter state is selected to obtain the minimum error by comparing the measured current with its reference, i.e., the state of the converter is selected according to:

$$i_{error_{\{a,b,c,d,e,f\}}} = \left\| i_{ac}{}^{*}[k] - i_{ac_{\{a,b,c,d,e,f\}}}[k+1] \right\|. \tag{9}$$

IV. Experimental System Evaluation

Fig. 4 shows the basic structure of the laboratorial setup used during the experimental validation. The digital control strategy was employed using a digital signal processor (DSP) from Texas Instruments (model F28335) with a clock frequency of 150 MHz. A sampling frequency of 40 kHz was assumed in the digital implementation, allowing a maximum switching frequency of 20 kHz according to the current control scheme. An external signal conditioning board and the internal 12-bit A/D converter of the DSP were used for signal acquisition. A total time of 1.62 µs is required for sampling five electrical signals and convert them into a digital value, i.e., to obtain $v_{ac}[k]$, $i_{ac}[k]$, $v_{dc1}[k]$, $v_{dc2}[k]$ and $i_{dc}[k]$. This task is performed at the beginning of each sampling period [k, k+1]. As presented in Section III, the values of these variables are used by the control algorithm to determine the state of the converter during each control period [k, k+1]. The whole digital control calculations are executed within a sampling period and the state of the converter can be updated also during such sampling period. In terms of the hardware implementation, current and voltage sensors with Hall-effect technology were used, namely model LTSR 15-NP and CYHVS5-25A, respectively. The input filter has an inductor of 5 mH (20 A) and the split dc-link has a capacitance of 2.24 mF (450 V) in each capacitor. The discrete IGBTs FGA25N120ANTD were used both as switching devices and as diodes in the different states assumed by the converter. The prototype was connected to a 115 V - 50 Hz power grid, and the

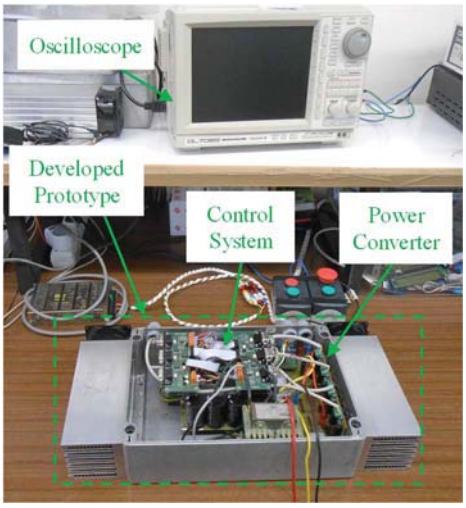

Fig. 4. Laboratorial setup used during the experimental validation.

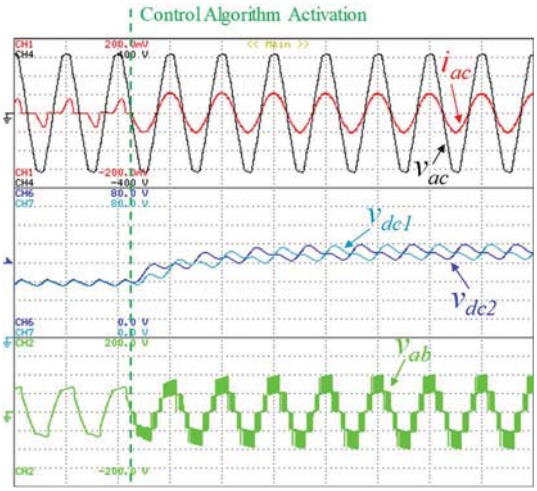

Fig. 5. Experimental results during a transient-state operation: Grid voltage (v_{ac}) and current (i_{ac}); Dc-link voltages of both capacitors (v_{dc1}, v_{dc2}); Voltage levels assumed by the converter ($+v_{dc}$, $+v_{dc}/2$, 0, $-v_{dc}/2$, $-v_{dc}$).

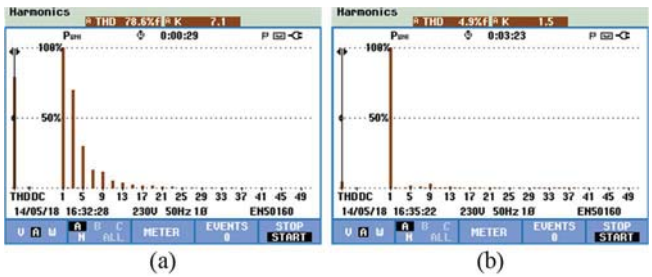

Fig. 6. Experimental results of the total harmonic distortion and spectral analysis of the grid current (i_{ac}): (a) Before the control algorithm activation; (b) After the control algorithm activation.

experimental results were registered with a digital oscilloscope Yokogawa model DL708E. Fig. 5 shows the operation of the proposed topology during a transient state. As shown, before the control algorithm activation, the grid current (i_{ac}) is non-sinusoidal, i.e., the converter operates as a traditional diode bridge rectifier. After the control algorithm activation, the grid current (i_{ac}) becomes sinusoidal and in phase with the grid voltage (v_{ac}). The measured total harmonic distortion of the grid current before and after the control algorithm activation is

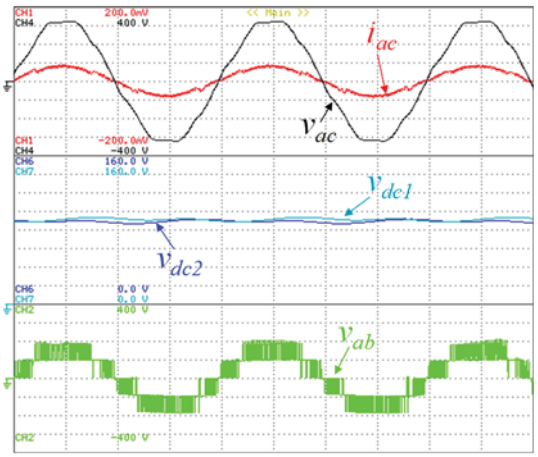

Fig. 7. Experimental results during a steady-state operation: Grid voltage (v_{ac}) and current (i_{ac}); Dc-link voltages of both capacitors (v_{dc1}, v_{dc2}); Voltage levels assumed by the converter ($+v_{dc}$, $+v_{dc}/2$, 0, $-v_{dc}/2$, $-v_{dc}$).

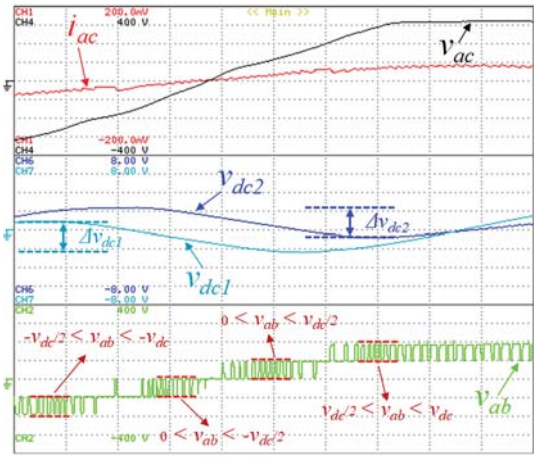

Fig. 8. Experimental results showing in detail the grid current (i_{ac}) crossing the grid voltage (v_{ac}), the dc-link voltage oscillation in both capacitors (v_{dc1}, v_{dc2}), and the five voltage levels ($+v_{dc}$, $+v_{dc}/2$, 0, $-v_{dc}/2$, $-v_{dc}$).

presented in Fig. 6(a) and Fig. 6(b), respectively. As experimentally demonstrated, the total harmonic distortion was reduced from 78.6% to 4.9%. Fig. 6 also shows the spectral analysis for each case, acquired with a FLUKE 435 Power Quality Analyzer. Fig. 7 shows the operation of the proposed topology during a steady state operation. The grid current is sinusoidal, and due to the boost-type characteristic of the converter, the dc-link voltage (sum of the voltage of both dc-link capacitors) is greater than the peak of the grid voltage (v_{ac}). In this case, since the converter was connected to a rms grid voltage of 115 V, it was selected a reference of 95 V for each dc-link capacitor. The grid voltage has a total harmonic distortion of 2.9%, which is affected by the nonlinear appliances in the electrical installation. A detail showing the grid current (i_{ac}) crossing the grid voltage (v_{ac}) is presented in Fig. 8. This experimental result was obtained in order to identify the operation with unitary power factor and to clearly identify the five voltage levels ($+v_{dc}$, $+v_{dc}/2$, 0, $-v_{dc}/2$, $-v_{dc}$), as well as to measure the dc-link voltage oscillation in both capacitors (v_{dc1}, v_{dc2}) (a peak-to-peak voltage of 4 V with an average value of 100 V). A detail of the grid current (i_{ac}) is presented in Fig. 9,

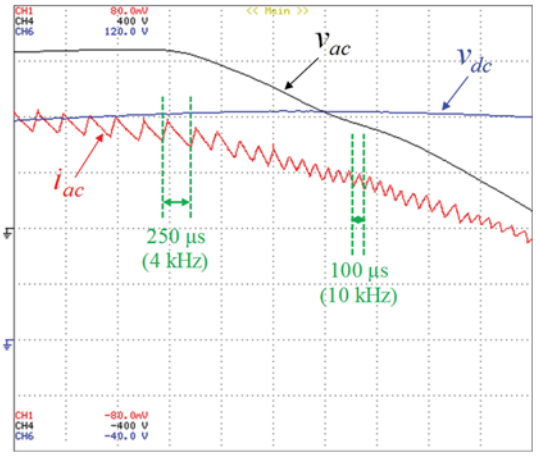

Fig. 9. Experimental results showing in detail the maximum and minimum switching frequency of the grid current (i_{ac}), the dc-link voltage (v_{dc}), and the grid voltage (v_{ac}).

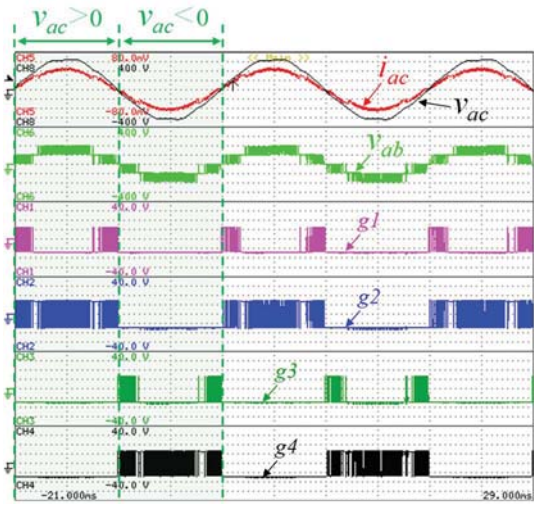

Fig. 10. Experimental results showing the grid current (i_{ac}), the grid voltage (v_{ac}) and the IGBTs ($g1$, $g2$, $g3$, $g4$) that are switched during the positive and negative half-cycles.

showing the variable switching frequency of the control strategy. In this experimental result, two main switching frequencies were identified according to the state of the proposed topology. The maximum measured switching frequency was 10 kHz, and the minimum was 4 kHz. The experimental result shown in Fig. 10 was attained in order to verify the IGBTs that are switched during the positive and negative half-cycles, as well as during the different states of the proposed topology. The IGBT *g2* is switched during the entire positive half-cycle, while the IGBT *g1* is switched only to state the voltage levels 0 and $+v_{dc}/2$. It should be distinguished that the IGBTs *g1* and *g2* are switched in a complementary way. In this half-cycle, the IGBTs *g3* and *g4* are OFF. On the other hand, the IGBT *g4* is switched during the entire negative half-cycle, while the IGBT *g3* is switched only to state the voltage levels 0 and $-v_{dc}/2$. Similarly to the previous case, it should be noted that the IGBTs *g3* and *g4* are switched in a complementary way and that the IGBTs *g1* and *g2* are OFF during this half-cycle. This result also shows that the grid current (i_{ac}) is sinusoidal.

V. Conclusions

A novel five-level semi-bridgeless power factor correction (PFC) topology is proposed. A comprehensive comparison with the traditional PFC topologies is presented, praising the main advantages of the proposed topology, mainly in terms of reduced number of power devices considering the establishment of five distinct voltage levels. The switching devices are controlled individually during each control period to define the state of the converter, and it is not required to apply any dead-time. The grid reference current is established according to the dc operating power, and it is used as a control variable to define the state of the converter during each control period. The acquired results during the experimental validation, both in transient and steady state, support the features of the proposed topology in terms of a sinusoidal grid current, unitary power factor operation, and controlled dc-link voltage.

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