Frequency Multipliers Based on Hybrid Technology with High Harmonic Suppression

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***Abstract* — A wideband frequency multipliers using SiGe bipolar transistors are proposed in this paper. The main circuit of these frequency multipliers consists of an attenuator followed by a bias network and a band pass filter which selects the desired harmonic at the output. The designed doubler can convert a 2-3 GHz input signal to a 4-6 GHz signal, with high suppressions of 59 dB, and 41 dB on the fundamental, and the third harmonic respectively. The tripler can convert a 2.3-2.7 GHz input signal to a 7-8 GHz signal, with suppressions of 68 dB, 52 dB, and 43 dB on the fundamental, the second, and fourth harmonics respectively.**

***Keywords* — frequency conversion, operation frequency, bipolar transistors, doubler, tripler, hybrid integrated circuits.**

I. Introduction

In many communications systems, frequency multipliers are used to translate a very stable local oscillator signal to a higher frequency for use in either upconversion or downconversion mixers, even though phase noise increases proportionally with multiplication factor, it might still be preferable multiply a high stability signal from a lower frequency to the operation frequency. Multipliers are also used in instrumentation applications such as frequency synthesizers. Whereas various FET-based frequency multiplier implementations exist, to date relatively few bipolar based frequency multipliers circuit topologies have been reported [1-3].

In this paper, a hybrid wideband frequency doubler, tripler and quadrupler using SiGe bipolar transistors are presented. The topology presented in this paper provides a compact size multiplier with a very high harmonic suppression due to the hairpin filer. SiGe bipolar transistors allow cost-effective frequency multiplier realizations for wideband wireless services. The key design parameters of the frequency multiplier are output power, harmonic suppression and fractional bandwidth (FBW).

These frequency multipliers will be used to increase the VCO (Voltage Controlled Oscillator) frequency in an S-C band, and an S-X band up/down converter. The converters will be part of a new generation C band and X band TTC transponder, this TTC transponder have a frequency plan based in only one oscillator and various multipliers to obtain the different frequencies.

II. Circuit Design

The circuit principle of most multipliers is based on a nonlinear element that distorts the input signal generating harmonics of the signal, and an output filter which selects the desired band [4]. In this paper, a low cost space qualified bipolar transistor (BFP740) is used as a nonlinear element. The transistor's maximum operation frequency is known to be 10 GHz. The transistor is biased through the bias network which determine the operating point, the bias network has a different design in each multiplier due to the operating point is not the same in each multiplier, and it consists of a $\lambda/4$ transmission line followed by a $\lambda/4$ radial stub. The transmission line along with the radial stub has the same effect than a capacitor connected to ground, this allows to isolate the DC power supply from the RF signal.

The input is a 10 dBm signal, in order to respect the maximum ratings of the transistor, the power at the base of the transistor must be lower than -5 dBm. That's the reason why there is no need to design an adaptation network for the input. A 15 dB T attenuator is used to reduce the input power from 10 to -5 dBm, this attenuator also provides system adaptation.

A hairpin band pass filter is used to select the desired harmonic at the output. The hairpin topology it's formed by quarter-wave parallel lines, each pair of parallel lines it's connected to the next pair using a short circuit [5]. This is a simple topology that allows high harmonic suppression. The filters dimensions are shown in the Fig. 1, the length of the $\lambda/4$ parallel lines depends of the frequency of each harmonic, 10.1 mm for the second harmonic, 6.6 mm for the third harmonic, and 4.9 mm for the fourth harmonic.

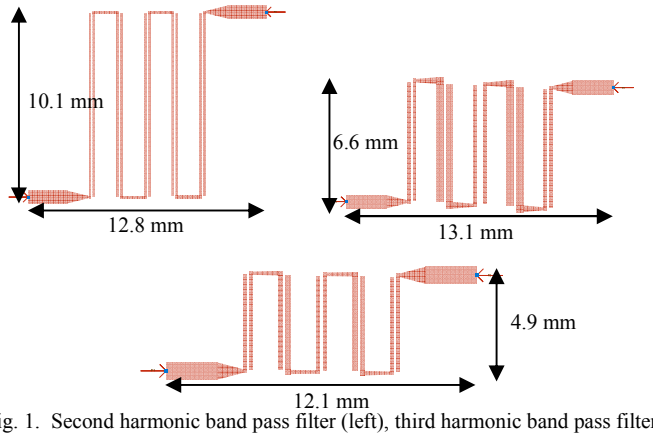

Fig. 1. Second harmonic band pass filter (left), third harmonic band pass filter (right), fourth harmonic band pass filter (center).

These circuits, the frequency doubler, tripler and quadrupler, consist of an attenuator, a bias network, and the

hairpin band pass filter explained above. All these parts are designed to achieve the optimum load impedance for each harmonic. The circuits are fabricated in a Rogers 4003C substrate with a thickness of 12 mils (0.305 mm), dielectric constant (ϵ_r) of 3.38 ± 0.05, and dissipation factor (δ) of 0.0021 at 2.5 GHz/23ºC.

The final designs of the frequency doubler, frequency tripler, and frequency quadrupler are shown in the Fig. 2.

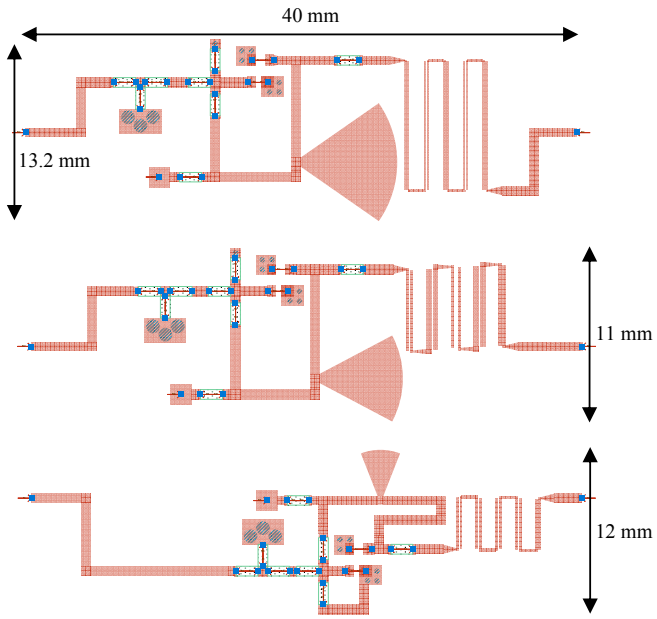

Fig. 2. Circuit design for the frequency doubler (above), tripler (center) and quadrupler (below).

III. Results

Fig. 3 and Fig. 4 shows a photograph of the 40x40mm PCB which contains the frequency doubler, tripler and quadrupler. The input signal is provided using a Rohde & Schwarz Signal Generator, which can provide signals from 5 KHz to 6 GHz. The output powers are measured using an Agilent E44464 spectrum analyser.

The frequency multipliers presented in this paper are designed to have a 5V DC bias.

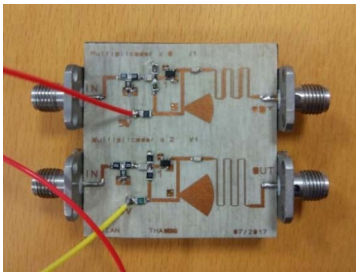

Fig. 3. Photograph of the frequency tripler (above) and doubler (below) assembly showing the SMA connectors for the input and output waveguide.

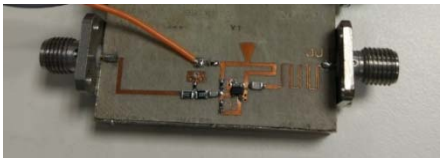

Fig. 4. Photograph of the frequency quadrupler assembly showing the SMA connectors for the input and output waveguide.

A. Frequency doubler

The input frequency of the frequency doubler is between 2-3 GHz. The measured and simulated output power vs the output frequency is showed in the Fig. 5. At 2.5 GHz input frequency, a peak output power of 7.05 dBm is achieved with a power consumption of 17.7 mW.

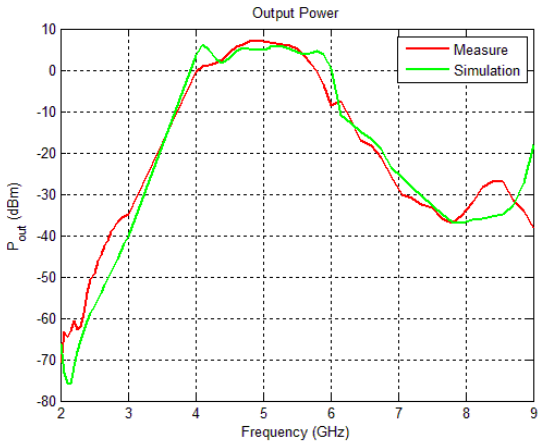

Fig. 5. A comparison between the measured and the simulated output power of the frequency doubler.

The output power at each harmonic vs the input frequency at 10 dBm input power is depicted in Fig. 6, which features a 3 dB bandwidth of 700 MHz and an FBW of 14%. The best fundamental and third harmonic suppression are 71.4 and 43.8 dB, respectively. The harmonic suppression for frequency doublers in MMIC technology are around 12 dB [6].

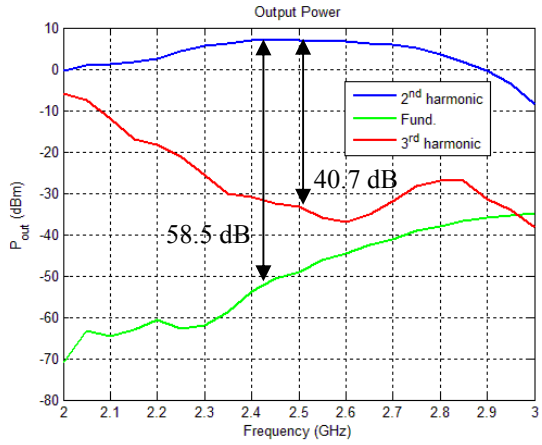

Fig. 6. Harmonic output power against input frequency of the frequency doubler

B. *Frequency Tripler*

In this case, the input frequency is between 2.3-2.7 GHz. The Fig. 7 shows the measured and simulated output power vs the output frequency. At 2.48 GHz input frequency, a peak output power of 3.85 dBm is achieved with only 10.4 mW of power consumption.

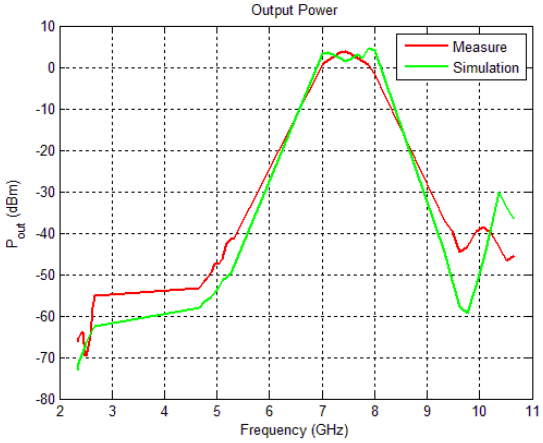

Fig. 7. A comparison between the measured and the simulated output power of the frequency tripler.

The output power at each harmonic vs the input frequency at 10 dBm input power is depicted in Fig. 8. In this case, the frequency tripler features a 3 dB bandwidth of 400 MHz and an FBW of 5.3%. The best fundamental, second, and fourth harmonic suppression are 73.4, 53.8 and 47.4 dB, respectively.

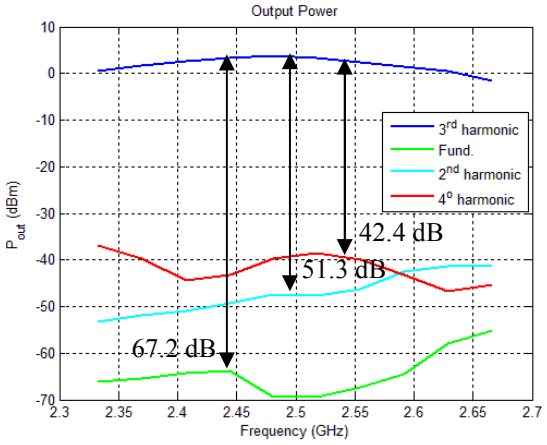

Fig. 8. A comparison between the measured and the simulated output power of the frequency tripler.

The frequency doubler and tripler show a wideband, high conversion gain, high harmonic suppression, low power consumption and compact size.

C. *Frequency Quadrupler*

A frequency by 4 was tried to; in spite the maximum operating frequency of the transistor was defined in 10 GHz. The input frequency goes from 2.6 to 3.2 GHz. The results depicted in the Fig. 9 shows a remarkable difference between simulation and measurements. The frequency target in the quadrupler is to have a bandwidth between 10.4-12.8 GHz with an input frequency of 2.6-3.2 GHz, the measurement result gives a narrower band as expected.

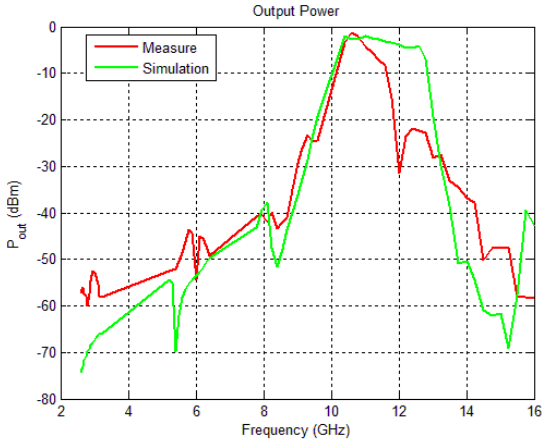

Fig. 9. A comparison between the measured and the simulated output power of the frequency quadrupler.

To solve this problem a frequency quadrupler formed by two frequency doublers is designed. The results depicted in the Fig. 10 still show a big difference in terms of output power between the simulations results and the measurement results, these results confirm that the bipolar transistor BFP740 used in this work is only useful up to 10 GHz.

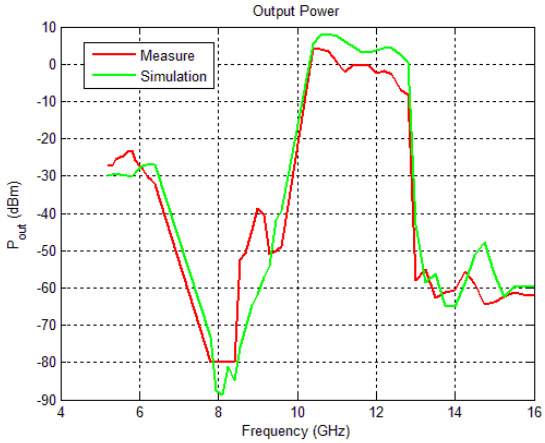

Fig. 10. A comparison between the measured and the simulated output power of the frequency quadrupler formed by two frequency doublers.

IV. Conclusion

In this paper, a wideband, cost-effective, SiGe bipolar frequency doubler and tripler with very high harmonic suppression are successfully presented. The maximum operation frequency of the BFP740 is confirmed to be 10 GHz with the design and measure of a frequency quadrupler. The hybrid technology offers design flexibility, and the SiGe bipolar transistor reduces the cost of the frequency multipliers.

According to the results, SiGe bipolar transistors have the potential capabilities in the microwave multipliers, with a better BFP740 transistor model, the measure results of the multipliers would be anticipated and the simulation response would be optimized to frequencies up to 10 GHz which is the limit of the operation frequency.

ACKNOWLEDGMENT

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