A compact current-mode instrumentation amplifier for general-purpose sensor interfaces.

Simone Del Cesta[a,c], Andrea Ria[a,c], Massimo Piotto[a,b], Roberto Simmarano[c], Paolo Bruschi[a,b]

[a] Dipartimento di Ingegneria dell'Informazione, University of Pisa,

via Caruso 16, I-56122 Pisa, Italy.

[b] CNR-IEIIT, via Caruso 16, I-56122 Pisa, Italy.

[c] Sensichips srl, Via Delle Valli 46, 04011, Latina – Italy.

e-mails:: simone.delcesta@ing.unipi.it, massimo.piotto@ieiit.cnr.it,

roberto.simmarano@sensichips.com, paolo.bruschi@unipi.it

Corresponding author: Paolo Bruschi: e-mail paolo.bruschi@unipi.it

Abstract - The proposed amplifier architecture follows a consolidated topology based on second-generation current conveyors (CCIIs), optimized for fully-differential operation. The architecture uses gain-boosting to improve the offset and noise characteristics of a recently proposed design. Wide input and output ranges and high accuracy are obtained by designing the CCIIs according to an original two-stage architecture with local voltage feedback. Embedding of chopper switch matrices into the amplifier enables vector analysis of the input signal, expanding the application field. The main strengths of the proposed amplifier are compactness and versatility. Measurements performed on a prototype designed with a 0.18 μm CMOS process are described.

Keywords: Instrumentation amplifier, wide input range, vector signal analysis, CMOS, sensor interfacing.

1. Introduction

The instrumentation amplifier (in-amp) is the optimal choice for interfacing sensors that generate, either directly or indirectly, a voltage. An in-amp designed for general-purpose sensor interfacing should be able to amplify and demodulate sinusoidal signals, enabling complex impedance

measurements or implementation of the lock-in approach [1]. At the same time, the in-amp should be configurable as a chopper amplifier to read dc signal with great accuracy [2]. In order to obtain compatibility with an as large as possible variety of sensors, a general-purpose in-amp should also have wide input common mode range (ICMR) and programmable gain. A unity gain option should be available to read sensors that produce relatively large output voltages, such as electrochemical gas sensors. Finally, compactness is mandatory to enable integration in low-cost systems on a chip (SoCs).

The classical three-op-amp [3] architecture generally does not meet the above criteria, since its first stage amplifies the differential mode while leaving the common mode unchanged, making the amplifier prone to saturation when the common mode is close to the rails. This architecture is also not optimized in terms of compactness and requires resistor trimming. Indirect current feedback amplifiers [4-6], involving direct application of the input differential signal to a differential pair, are less suitable to achieve the wide input ranges required in unity-gain settings. The current-balance in-amp uses source followers in the input stage [7] or even involves stacking of the input and output section [8], with severe limitation on the input common mode range and/or the output swing.

In this work, we propose a compact instrumentation amplifier based on second generation current conveyors (CCIIs) [9-10]. While the general architecture follows a well-known current-mode approach, the amplifier embodies also voltage-mode characteristics. A first example of the proposed architecture was presented in Ref. [11]. However, noise and offset performances of that preliminary version were not adequate for use in high accuracy sensor interfaces. In particular, flicker noise started to appear below 10 Hz, while statistical tests performed after Ref. [11] publication yielded input offset voltages up to 200 μV. Significant improvements of the offset

and flicker noise characteristics have been obtained in the amplifier proposed in this paper by introducing gain boosting in the output stage. The effectiveness of the approach is demonstrated by means of experiments performed on a prototype designed with a 0.18 μm CMOS process. Measurements described in this paper include also tests that were not presented in Ref.[11], such as statistical characterization of the offset voltage and quantitative estimation of the phase and magnitude errors achieved in demodulation experiments.

2. Circuit description

2.1. Principle of operation.

A simplified schematic view that represents the principle of operation of the proposed architecture is shown in Fig.1. Two identical CCIIs, indicated with dashed boxes in the figure, are connected to form a fully differential amplifier according to a scheme derived from Refs. [12,13]. Briefly, input voltages V_{Y+} and V_{Y-} are copied to nodes V_{X+} and V_{X-}, respectively. Thus, a current $(V_{IN+}\text{-}V_{IN-})/R_1$ flows across resistor R_1 and is replicated as a differential current across nodes V_{Z+} and V_{Z-}, so that R_1 and R_2 carry the same current. It can be easily shown that the differential-to-differential gain is given by:

$$A_{dd} = \frac{R_2}{R_1} \tag{1}$$

Let us consider the CCII on the left, since the same considerations applies to the right section. Note that M_{1L} forms a common-source inverting amplifier biased by a constant current provided by M_{3L} (V_B is a constant voltage). The cascade of the M_{1L}-M_{3L} amplifier and the single-stage amplifier indicated with OTA-L forms a two stage operational amplifier (op-amp) that, thanks to the voltage feedback connection, transfers voltage V_{Y+} to V_{X+}. Since M_{2L} is nominally identical to M_{1L}, current I_{D2L} tracks I_{D1L}.

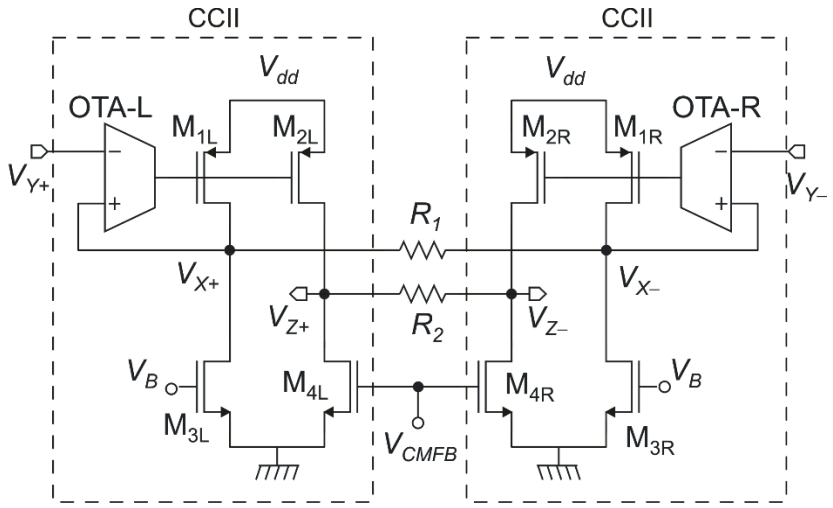

Fig.1. Simplified view of the proposed instrumentation amplifier.

For symmetry reasons, in nominal conditions, $I_{D3L}=I_{D4L}$, thus the currents exiting terminals V_{X+} and V_{Z+} are identical, as required by the CCII definition. The desired output common mode voltage is set by varying I_{D4L} and I_{D4R} through V_{CMFB}, controlled by a conventional common mode feedback (CMFB) loop. The input amplifiers OTA-L and OTA-R are designed to provide a rail-to-rail ICMR. In these conditions, the input common mode range of the whole amplifier is limited only by the maximum swing of voltage V_X, as shown in next section.

2.2. Proposed in-amp architecture with embedded chopper modulators.

Blocks S_{IN} and S_{OUT} in Fig.2 are chopper modulators, consisting in switch matrices that, depending on the logic value of the clock, transmit the signal along either the solid or dashed paths indicated inside the S_{IN}-S_{OUT} symbol, and labeled with the clock value (“0” or “1”) that enables them. For simplicity, arrows and labels inside the chopper modulator symbols will be omitted in the rest of the paper. Demodulation is performed by S_{OUT}, controlled by clock *ck*. If the input signal does not require modulation, then ck_{chop} =1, and S_{IN} becomes transparent. Otherwise, setting ck_{chop}=ck enables chopper modulation,. Block CA is a unity-gain current

amplifier, the purpose of which is lowering the resistance seen by modulator S_{OUT}, greatly increasing the frequency response. Capacitors C_{O1} and C_{O2} are added to operate pre-filtering of demodulation byproducts.

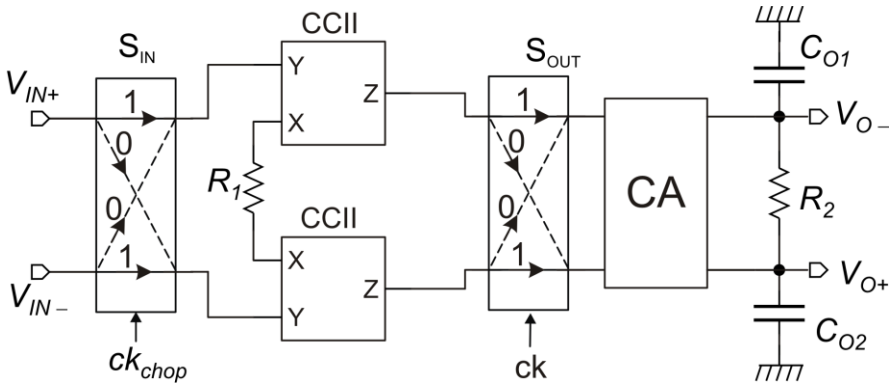

Fig. 2. Demodulation scheme. CA is a current amplifier. For demodulation functions, only clock *ck* is active. To implement chopper modulation, ck_{chop} is set equal to *ck*.

Application of the modulation/demodulation scheme of Fig. 2 to the amplifier of Fig. 1 leads to the circuit of Fig. 3, representing the proposed amplifier. The current amplifier CA consists of the common-gate stage M_{22L}-M_{22R}, which forms a cascode structure with M_{2L} and M_{2R}. In order to equalize M_{1L} and M_{2L} drain-source voltages and improve precision of the $I_Z=I_X$ relationship, common gates (M_{11L}, M_{11R}) are also introduced in the "X" section of the CCIIs. The same cascode structure is applied to the lower part of the circuit, composed of n-type devices. Modulator S_{OUT} is split into S_1 and S_2: the former actually implements signal (I_{2L}-I_{2R}) demodulation, whereas the latter is necessary to modulate the offset and flicker noise components of bias currents I_{D4L} and I_{D4R}.

To reduce offset and low frequency noise contributions from $M_{22L\text{-}R}$ and $M_{44L\text{-}R}$, which do not benefit from the modulation effect of S_1 and S_2, these devices have been included into individual feedback loops, based on amplifiers $A_{NL\text{-}R}$ and $A_{PL\text{-}R}$, respectively, forming a gain-boosting

configuration [14]. Offset and noise from $A_{NL\text{-}R}$ and $A_{PL\text{-}R}$ is rejected by the combined action of S_1 and S_3, for $A_{NL\text{-}R}$, and S_2, S_4 for $A_{PL\text{-}R}$.

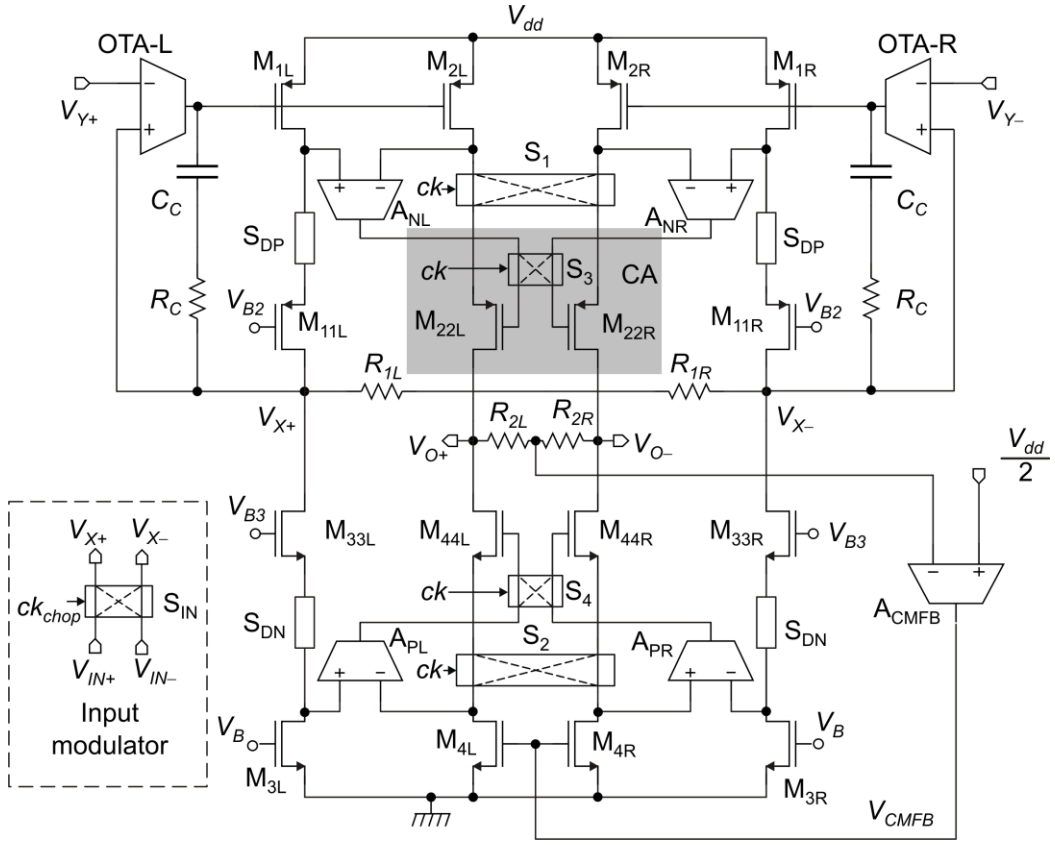

Fig.3. Proposed compact instrumentation amplifier. The current amplifier (CA in Fig.2) is indicated by the grey box; the role of S_{out} is played by S_1.

Resistors R_{1L}= R_{1H} and R_{2L}= R_{2H} are such that R_{1L}+R_{1H}=R_1 and R_{2L}+R_{2H}=R_2. Groups R_C,C_C implement standard Miller compensation of the mentioned two–stage feedback loop. Constant voltages V_{B2} and V_{B3} are generated by conventional bias circuits.

Dummy switches S_{DP} and S_{DN} (always on) are introduced to compensate for the static voltage drop introduced by modulators S_1 and S_2, respectively. The output common mode voltage is stabilized to $V_{dd}/2$ by the simple loop based on amplifier A_{CMFB}.

3. Analysis of non-idealities

3.1 Finite frequency bandwidth.

As far as bandwidth is concerned, we recall that it is necessary to maintain a flat frequency response over the required frequency range up to the demodulator input. The elements that dominate the frequency response are depicted in Fig.4 (a), showing the differential mode representation of the left half of the amplifier. The input signal, V_Y, is transferred to V_X by a low pass transfer function, with upper band limit equal to the 0-dB frequency (f_0) of the OTA-L / M_{1L} composite op-amp. The M_{1L}-M_{11L} series supplies the whole ac current exiting V_X node. This current includes the correct contribution, which flows into resistor R_{1L}, and an error component, which flows into parasitic capacitances (represented by C_{pX}) and into the C_C,R_C series. Assuming that i_{d2}=i_{d1}:

$$i_{d2} = \frac{v_y}{R_{1L}} \frac{1 + j\frac{f}{f_Z}}{1 + j\frac{f}{f_0}} \tag{2}$$

By means of simple calculations and neglecting the zero nulling resistor R_C, we can find the following approximations for f_0 and f_Z:

$$f_0 \cong \frac{g_{m-in}}{2\pi\left(C_C + \frac{C_{pA}}{g_{m-M2L}R_{1L}}\right)} \tag{3}$$

$$f_Z = \frac{1}{2\pi R_{1L}\left[C_{pX} + C_C\left(1 + \frac{1}{g_{m-2L}R_{1L}}\right)\right]} \tag{4}$$

where $g_{m\text{-}in}$ is the transconductance of OTA-L and OTA-R amplifiers.

For $R_{1L} > 1/g_{m\text{-}in}$, the zero f_Z may fall at frequencies lower than f_0, producing a peak in the frequency response that can significantly shrink the region of flat response. This peak was actually observed in the simulations.

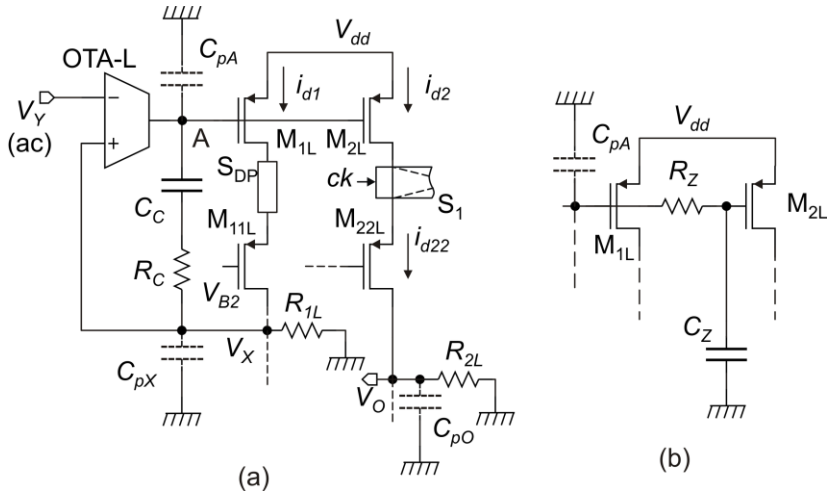

Fig. 4. (a) Simplified differential-mode model of the left half of the amplifier, with the elements that determine the frequency response. (b) Compensation scheme for unity gain setting.

An optimum strategy is trying to lower f_0 in order to make it match f_Z, forcing a pole-zero cancellation. To this aim, increasing the compensation capacitance C_C is not a viable option, since it affects both f_0 and f_Z. For moderate values of R_{1L}, an effective solution can be increasing the parasitic capacitance C_{PA}, by, for example, increasing M_{1L}, M_{2L} gate area. Notice that a gate area increase is also beneficial in terms of flicker noise density. For high R_{1L} values, the required capacitance C_{PA} could be unfeasible with integrated capacitors. In these cases, corresponding to $f_Z << f_0$, the problem is mitigated by introducing an additional pole at around f_Z in the path from M_{1L} gate to M_{2L} one, as shown in Fig. 4 (b), where the pole is implemented by the R_Z-C_Z filter.

3.2. Input and output voltage ranges.

Considering now the input and output ranges, the use of a common-source stage to drive node X (instead of source followers, as in popular CCII designs), allowed V_X to approach each rail with only a margin of two drain-source saturation voltages (V_{DSAT}). The same margin ($2V_{DSAT}$ to each rail) applies to the output swing, since the same cascode structure is used.

3.3 Noise analysis.

In order to estimate the output noise, we can start by considering that the voltage noise across R_1 can be written as:

$$v_{Xn} = v_{n-L} - v_{n-R} \tag{5}$$

where $v_{n\text{-}L}$ and $v_{n\text{-}R}$ are the input referred noise voltages of OTA-L and OTA-R amplifiers, respectively. The noise current flowing into R_1 is then replicated into R_2 with the addition of significant noise contributions from the equivalent noise sources of the resistances and from the drain noise currents of eight devices, namely: $M_{1L\text{-}R}$, $M_{2L\text{-}R}$, $M_{3L\text{-}R}$, and $M_{4L\text{-}R}$. From the above considerations, the in-amp output noise can be approximated by:

$$v_{n-out} = \left(v_{n-L} - v_{n-R}\right) A_{dd} + \frac{R_2}{2}\left(\Delta i_{n1} + \Delta i_{n3} - \Delta i_{n2} - \Delta i_{n4}\right) + v_{nR1} A_{dd} + v_{nR2} \tag{6}$$

where v_{nR1} and v_{nR2} are the equivalent noise voltages of resistors R_1 and R_2, respectively, A_{dd} is the overall amplifier gain and Δi_{nk} is defined by:,

$$\Delta i_{nk} = i_{n-kL} - i_{n-kR} \quad \text{with:} \quad k = 1,2,3,4 \tag{7}$$

with $i_{n\text{-}kL}$ and $i_{n\text{-}kR}$ being the equivalent drain current noise [15] of devices M_{kL} and M_{kR}, respectively. Considering that all noise sources in (6) are independent, the following output noise spectral power density (PSD) can be calculated:

$$S_{vn-out} = 2A_{dd}^2 S_{n-OTA} + 2\sum_{k=1}^{4} \frac{R_1^2}{4} S_{Ik} + 4k_B T R_2 \left(1 + A_{dd}\right) \tag{8}$$

where $S_{n\text{-}OTA}$ is the PSD of OTA-L, OTA-R input referred voltage noise, S_{Ik} is the PSD of M_{kL} ,M_{kR} equivalent noise current, k_B the Boltzmann constant and T the absolute temperature. Note that all flicker noise contributions to $S_{vn\text{-}out}$ are rejected by the effect of the modulators, so that only thermal contributions should be considered.

4. Design of the prototype

The architecture described so far was used to design a prototype using the 3.3 V CMOS subset of the RF/Mixed Mode 0.18 μm CMOS process of UMC. Input amplifiers OTA-L and OTA-R were implemented using a standard folded cascode topology [11] with rail-to-rail input common mode range. Resistor R_2 was fixed to 330 kΩ, while four different values could be selected for R_1: 8.25 kΩ, 16.5 kΩ, 27.5 kΩ and 330 kΩ, corresponding to a gain of 40, 20, 12 and 1, respectively. All resistors were implemented using high-resistivity polysilicon. Dimensions and bias currents of the devices that have the largest impact on the amplifier performances are shown in table 1.

Device(s)	W/L (μm/μm)	I_D (μA)	Device	W/L (μm/μm)	I_D (μA)
OTA_{L-R} input pair (p)	10/1	3.0	M_{1LR},M_{2L-R}	40/1	11 μA
OTA_{L-R} input pair (n)	8/4	3.0	M_{3L-R}, M_{4L-R}	68/6	11 μA

Table 1. Dimensions and bias current of selected devices.

Amplifiers A_{NL-R} were implemented using the elementary *n*-input differential amplifier shown in Fig. 6. For output range requirements, A_{NL-R} uses *n*-type input pairs, while A_{PL-R} use *p*-type ones. Such a simple amplifier introduce a problem in terms of dc operating point. To understand this, consider Fig.5, where also M_{2L} and M_{22L} are included to illustrate the connections of A_{NL}. In order to keep M_{1B} in saturation, the following condition should be respected:

$$V_{D1B} + V_{t1B} \geq V_{G1B} = V_{D1B} + \left|V_{GS22L}\right| \tag{9}$$

where V_{t1b} is the threshold voltage of M_{1B}. This results in:

$$V_{t1B} \geq \left|V_{GS22L}\right| \tag{10}$$

which is difficult to fulfill if the *n* and *p* devices have same threshold voltages (absolute value). The problem has been solved using devices with reduced threshold voltage for the common gate transistors (M_{22L-R}, M_{11L-R}). These devices are available in the quoted UMC CMOS technology. For the same reason, low threshold n-MOSFETs have been used for M_{44L-R} and M_{33L-R}.

The input modulator S_{IN} was implemented using complementary *p*-*n* pass-gates, while *p*-MOSFETs were used in S_1 and S_3 and *n*-MOSFETs in S_2 and S_4 switch matrices.

In order to obtain a flat response of the currents fed to the demodulator up to around 500 kHz, the solutions shown in Fig.4 (b) were adopted. In particular, a C_{PA} increase was sufficient for gains 12-40, while the R_Z-C_Z filter (C_Z=1pF,R_Z= 350 kΩ) was inserted for the unity gain option.

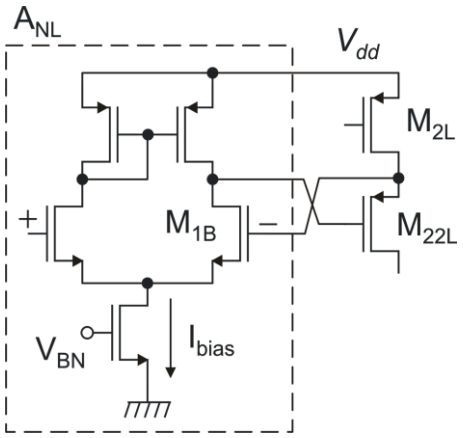

Fig.5. Schematic view of the A_{NL} amplifier with connection to the common gate stage.

A passive, fully-integrated multi-cell RC low pass filter with a -3 dB cut-off frequency of nearly 2.5 kHz was cascaded to the amplifier output in order to reject the high-frequency byproducts of the demodulation process. The amplifier has been integrated into a test chip including an internal RC oscillator (10 MHz) and programmable digital frequency dividers that produce clocks ck and ck_{chop}. The internal oscillator can be disabled and an external 10 MHz signal can be introduced through a dedicated pad. A micrograph of the proposed instrumentation amplifier, with the main block indicated, is shown in Fig. 6. The amplifier occupies an area of 248 × 265 μm^2. The output low-pass filter is not included in the micrograph.

5. Experimental results

The test chips were bonded into 44-pin JLCC-type ceramic cases. Purposely-built circuits

implemented on printed circuit boards were used to facilitate access to the chips and to provide bidirectional single-ended to differential conversion of the signals. An SMC100A Rohde & Schwarz signal generator was used to provide the input signal to the amplifier.

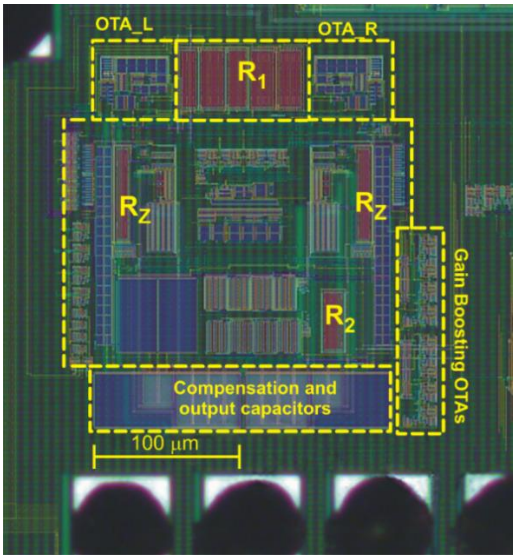

Fig.6. Optical micrograph of the amplifier with superimposition of the layout to show the circuit component buried under planarization dummies. The main blocks are indicated.

Dc transfer functions were acquired using an HP 4145B parameter analyzer. Noise measurements were performed by digitalizing the output signal by means of a 16 bit, computer-controlled oscilloscope (model PicoScope 4262, Pico Technology Ltd.) and performing digital processing. Temperature tests were performed using a purposely-built Peltier-cell cryostat.

The amplifier operates at supply voltages from 1.5 V to 3.6 V, with a current consumption of 100 µA. All measurements were performed with chopper modulation enabled ($ck=ck_{chop}$) using a chopper frequency of 20 kHz. The only exception are demodulation experiments described at the end of this section (table 2).

Figure 7 shows the differential-mode-to-differential-mode dc characteristics for the two extreme gain settings (1 and 40), measured for V_{dd}=1.5 V and 3.3 V.

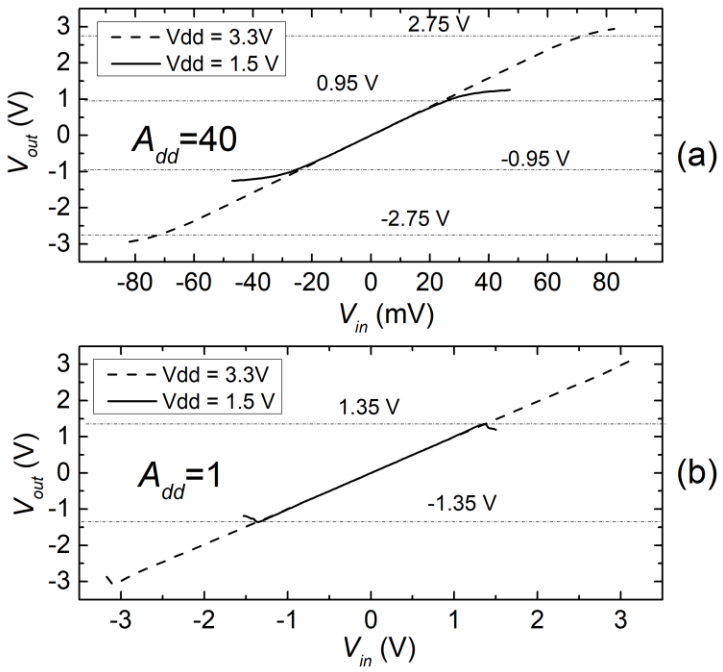

Fig.7. Differential output voltage (V_{out}) vs input differential voltage (V_{in}) for gain=40 (a), and gain=1 (b), measured for V_{dd}=1.5 V and V_{dd}=3.3 V.

For a gain of 40, we have a loss of nearly 550 mV with respect to ± V_{dd} . This means that each output port should respect a 275 mV margin with respect to both rails, which roughly corresponds to two V_{DSAT}, in line with the prediction. Wider ranges can be observed for A_{dd}=1. The input common mode range can be estimated from Fig. 8, showing the dependence of the differential output voltage on the input common mode voltage. The tests have been performed applying a constant differential voltage (V_{in}) to the input, chosen to set the output voltage to roughly 25 % of the full-scale value, and then sweeping the input common mode voltage. Clearly, V_{in} depends on the selected gain. For all V_{dd} settings and gains, except A_{dd}=1, the input common mode voltage shows a margin of only nearly 200 mV to both power rails, in agreement with the $2V_{DSAT}$ prediction. It can be easily shown that the seemingly worst performance found in the unity gain case is due to the presence of a non-negligible differential input voltage.

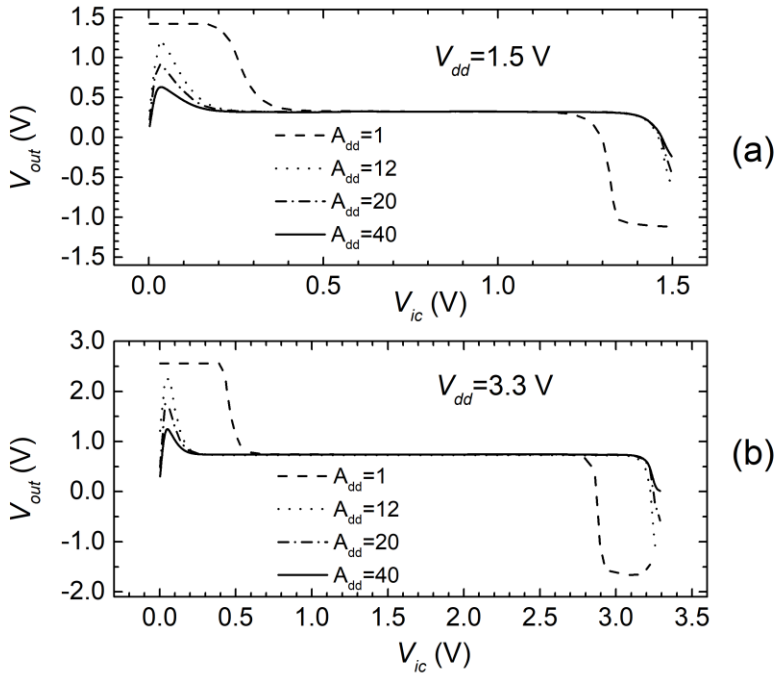

Fig.8. Dependence of the output voltage on the input common mode voltage (V_{ic}) at four different gain settings for V_{dd}=1.5 V (a) and V_{dd}=3.3 V (b), for a constant input differential signal.

The input offset voltage (V_{io}) histogram, involving nine samples (from the same wafer), is shown in Fig.9 for the same gain and V_{dd} settings as in Fig.7. Notice that the performances tend to get worse at smaller gains and supply voltages. Temperature measurements across the 10-80 °C interval showed that the offset drift for a gain of 40 is 300 nV/°C at V_{dd}=3.3 V and 450 nV/°C at V_{dd}=1.5 V. The offset drift for unity gain is 2 μV / °C at V_{dd}=3.3 V and 28 μV / °C at V_{dd}=1.5 V. The output noise density is shown in Fig.10 at V_{dd}=1.5 V and 3.3 V for gains of 1 and 40. The noise density decrease at around 2.5 kHz is due to the mentioned output passive filter. Flicker noise is negligible for all settings, except for a gain of 40 and V_{dd}=1.5 V, where, however, the flicker corner is still below 1 Hz. The noise density in the flat region is nearly independent of

gain and V_{dd} settings. In particular, considering Eq. (8), the fact that the gain does not affect the noise means that the contribute from $M_{kL\text{-}R}$ transistors (k=1-4) dominates.

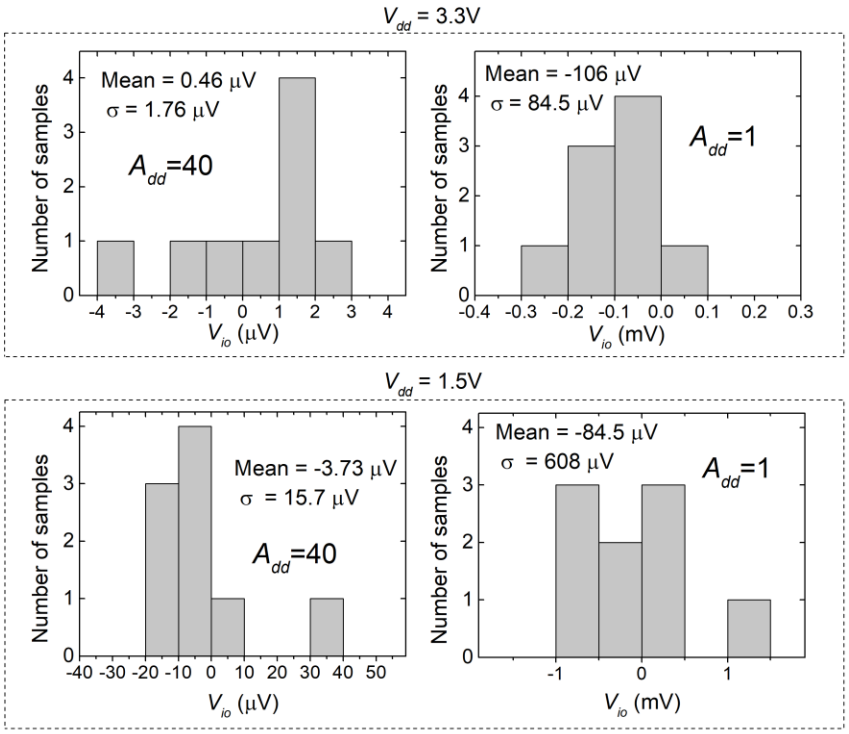

Fig. 9. Histograms of the offset voltage calculated over a set of 9 samples.

The results of in-phase and quadrature demodulation experiments (vector signal analysis) are summarized in table 2. The amplifier has been stimulated with a sinusoidal input voltage, with input modulator S_{IN} turned off. The system clock (10 MHz) was derived from the reference frequency port (RF out) of the signal generator allowing synchronization of the input and demodulation signals.

Due to limitations of the on-chip division logic and compatibility with the level of the RF-out reference signal, it has been possible to execute tests only at the frequencies shown in the table and V_{dd}=1.8 V. The difference between the expected and the actual amplifier output dc voltages, expressed as a magnitude and phase error, is reported in table 2 for two different gain settings.

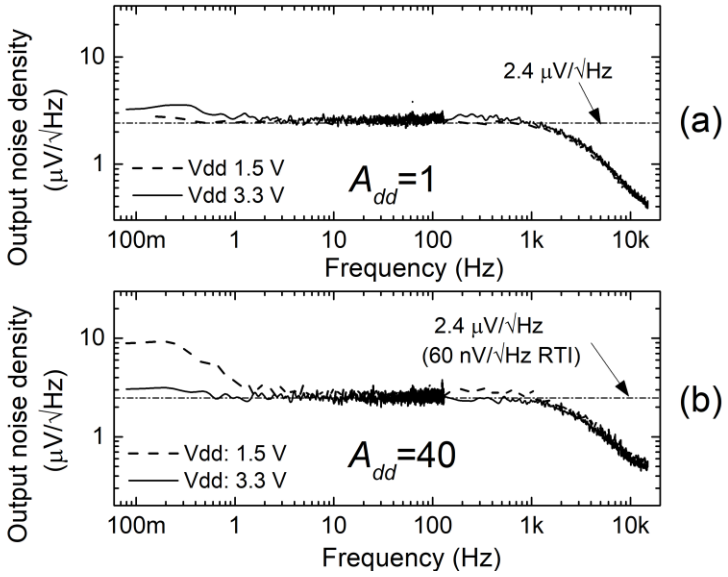

Fig. 10. Output noise spectra for a gain of 1 (a) and 40 (b) and V_{dd}=1.5 V and 3.3 V.

Gain	V_{in} (mV-pp)	Frequency (kHz)	Magnitude error (dB)	Phase error (deg)
1	600	78.125	-0.30919	-1.16952
1	600	625	0.95	-2.69088
1	600	1250	3.1	11.28373
40	12	78.125	-0.39	0.56
40	12	625	1.42795	9.8
40	12	1250	1.78623	24.8

Table 2. Magnitude and phase error measured with demodulation experiments.

While the behavior is nearly ideal only for the 78 kHz measurement, the errors are small enough to be easily recoverable through calibration at all examined frequencies.

The performances of the proposed amplifier are summarized in table 3, where they are compared with other compact designs proposed over the last four years. Refs. [16-18] deal with in-amps used as front-end of lock-in amplifiers, while Ref.[19] is a compact chopper amplifier. The input and output ranges have been extrapolated from inspection of the respective schematic views. Note that Ref. [16] has a very small input common mode range (ICMR), whereas the ICMR margins to V_{dd} reported in Refs. [17] and [18] include at least one threshold voltage (through the V_{GS} term). This margin is generally larger than the $4V_{DSAT}$ term obtained with the proposed

amplifier. The only exception is Ref.[18] with its rail-to-rail ranges. However, in Ref.[18] the input is not differential, so that a fair comparison is not possible. The GBW (gain-bandwidth product) vs. supply current ratio has been calculated for this work and Refs.[16-18] assuming that the bandwidth coincides with the highest frequency that can be demodulated with a maximum magnitude error of -3 dB. In this respect, the proposed amplifier performs better than all other designs reported in the table, with the exception of Ref.[16], whose figures are validate only by simulations.

	This work	[16]	[17]	[18]	[19]
Technology	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.13 μm
Vdd (V)	3.3-1.5	1.8	1.8	1.2	1.5
I-supply (μA)	100	267	200	970	194
Area (mm^2)	0.066	0.03	0.012	0.024	0.071
Gain	1,12,20,40	39–59	24.1-38.5	1-100	1000
Output Swing (V)	±(Vdd-550mV)	Vdd-0.26 V	NA	Rail-to-rail	NA
ICMR	Vdd-4V_{DSAT}	(V_{th}-V_{DSAT})	Vdd-V_{GS}-V_{DSAT}	Rail-to-rail	Vdd-V_{GS}-V_{DSAT}
CMRR (dB)	90 (1kHz)	78 (100 kHz)	78 (1 kHz)	NA	102
PSSR (dB)	100 (1 kHz)	NA	50	NA	101
THD (dB)	-60	NA	-52.1@300 mV_{pp}	NA	NA
Vio (μV)	4-40	NA	78	NA	3.5
e_n (nv/sqrt(Hz)	60	NA	5.6	63	13.5
Max input freq.	1.25 MHz	1.1 MHz	125 kHz	1.0MHz	32 kHz
NEF	29	NA	3.85	95	7.2
GBW/I supply	400 kHz/μA	3.67 MHz/μA	49 kHz/μA	103 kHz/μA	165 kHz//μA

Table 3. Symbols are as follows: ICMR: Input common mode range, e_n: input noise density; NEF: noise efficiency factor [20]; I supply: current consumption; Vio: input offset voltage (max); GBW: gain-bandwidth product. NA: Not available. For this work, THD (total harmonic distortion) has been measured at 1.0 Vpp for Vdd=1.5 V and 4.6 V for Vdd=3.3 V over the 1-500 Hz frequency range. All figures for the proposed amplifier refer to A_{dd}=40.

6. Conclusions

Experimental characterization of the amplifier confirmed the versatility of the proposed architecture. The higher offset voltage measured for the unity-gain setting is not an important

limiting factor, since this option is reserved for the case of large input voltages. The amplifier maintains usable voltage ranges and performances down to V_{dd}=1.5 V, exceeding the typical extension of the supply-voltage range required for sensor interfaces. Demodulation tests suggest that precision vector signal measurement is possible with the proposed amplifier up to frequencies of the order of one hundred kHz, with possibility to extend the measurement capability up to 1.25 MHz with a magnitude error less than 3 dB. The compact size of the amplifier makes it an interesting cell to be combined with a high-resolution delta-sigma analog to digital converter (ADC) to create a highly configurable readout channel for sensor interfacing.

References

[1] De Marcellis A, Ferri G, D'Amico A. One-Decade Frequency Range, In-Phase Auto-Aligned 1.8 V 2 mW Fully Analog CMOS Integrated Lock-In Amplifier for Small/Noisy Signal Detection. IEEE Sensors Journal. 2016;16(14):5690-701. DOI: 10.1109/JSEN.2016.2572732

[2] Enz CC, Temes GC. Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization. Proceedings of the IEEE. 1996;84(11):1584-614. DOI: 10.1109/5.542410.

[3] Spinelli EM, Mayosky MA. AC coupled three op-amp biopotential amplifier with active DC suppression. IEEE transactions on biomedical engineering. 2000;47(12):1616-9. DOI:10.1109/10.887943

[4] Van Den Dool BJ, Huijsing JK. Indirect current feedback instrumentation amplifier with a common-mode input range that includes the negative roll. IEEE Journal of Solid-State Circuits. 1993;28(7):743-9. DOI: 10.1109/4.222171.

[5] Wu R, Huijsing JH, Makinwa KA. A current-feedback instrumentation amplifier with a gain error reduction loop and 0.06% untrimmed gain error. IEEE Journal of Solid-State Circuits. 2011 Dec;46(12):2794-806. DOI: 10.1109/JSSC.2011.2162923

[6] Butti F, Piotto M, Bruschi P. A chopper instrumentation amplifier with input resistance boosting by means of synchronous dynamic element matching. IEEE Transactions on Circuits and Systems I: Regular Papers. 2017; 64(4):753-64. DOI:10.1109/TCSI.2016.2633384

[7] Yazicioglu RF, Kim S, Torfs T, Merken P, Van Hoof C. A 30μW Analog Signal Processor ASIC for biomedical signal monitoring. In Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International 2010 Feb 7 (pp. 124-125). DOI:10.1109/ISSCC.2010.5434026

[8] Yazicioglu RF, Merken P, Puers R, Van Hoof C. A 60 μW 60 nV/√Hz Readout Front-End for Portable Biopotential Acquisition Systems. IEEE Journal of Solid-State Circuits. 2007; 42(5):1100-10. DOI: 10.1109/JSSC.2007.894804.

[9] Senani R, Bhaskar DR, Singh AK. Current conveyors: variants, applications and hardware implementations. Springer; 2014 Oct 9. DOI: DOI 10.1007/978-3-319-08684-2

[10] Ferri G, Parente FR, Stornelli V. Current conveyor-based differential capacitance analog interface for displacement sensing application. AEU-International Journal of Electronics and Communications. 2017;81:83-91. DOI: 10.1016/j.aeue.2017.07.014.

[11] Bruschi P, Del Cesta F, Longhitano AN, Piotto M, Simmarano R. A very compact CMOS instrumentation amplifier with nearly rail-to-rail input common mode range. In European Solid State Circuits Conference (ESSCIRC), ESSCIRC 2014-40th 2014 Sep 22 (pp. 323-326). DOI: 10.1109/ESSCIRC.2014.6942087

[12] Wilson,B. Universal Conveyor Instrumentation Amplifier, Elec. Letters, 1989, 25(7),:470-71. DOI: 10.1049/el:19890323.

[13] Voulkidou A, Siskos A, Laopoulos T. A Low Noise Low Offset Current Mode Instrumentation Amplifier. In Mixed Design of Integrated Circuits and Systems (MIXDES) 2012 May 24, (pp.2013-7)

[14] Bult K, Geelen GJ. A fast-settling CMOS op amp for SC circuits with 90-dB DC gain. IEEE Journal of Solid-State Circuits. 1990; 25(6):1379-84. DOI: 10.1109/4.62165

[15] Gray PR, Hurst P, Meyer RG, Lewis S. Analysis and design of analog integrated circuits. Wiley; 2001, p-758.

[16] Hernández PM, Pascual MS, Calvo B. Micropower CMOS lock-in amplifier for portable applications. Electronics Letters. 2016 Apr 19;52(10):828-30. DOI: 10.1049/el.2015.4391

[17] Maya-Hernández PM, Sanz-Pascual MT, Calvo B. CMOS low-power lock-in amplifiers with signal rectification in current domain. IEEE Transactions on Instrumentation and Measurement. 2015 Jul;64(7):1858-67. DOI: 10.1109/TIM.2014.2366978.

[18] Valero MR, Medrano N, Celma S, Calvo B. A CMOS 1.2-V 1.7-mW lock-in amplifier for sensing applications up to 0.7-MHz. In IEEE SENSORS Conference, 2014 Nov 2 (pp. 78-81). DOI: 10.1109/ICSENS.2014.6984937

[19] Akita I, Ishida M. A chopper-stabilized instrumentation amplifier using area-efficient self-trimming technique. Analog Integrated Circuits and Signal Processing. 2014 ;81(3):571-82. DOI 10.1007/s10470-014-0371-4.:

[20] Steyaert MS, Sansen WM. A micropower low-noise monolithic instrumentation amplifier for medical purposes. IEEE Journal of Solid-State Circuits. 1987 Dec;22(6):1163-8. DOI: 10.1109/JSSC.1987.1052869.