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Improved control for multilevel inverters in grid applications

Martin Hofmann

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Universitat Politècnica de Catalunya

Departament d'Enginyeria Elèctrica

PhD thesis

Improved Control for Multilevel Inverters in Grid Applications

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Abstract

Control systems for three-phase grid connected voltage source inverters (VSI) play an important role in energy transformation systems. They are expected to be stable, robust and accurate during steady state as well as different grid faults and disturbances like voltage sags or unbalanced conditions. Caused by increasingly rising grid standards and efficiency requirements the use of multilevel inverter systems in grid connected low voltage applications is getting more and more attention. Nevertheless, the use of these inverter types leads to increased complexity of the control system and the hardware components.

This thesis presents an improved control scheme for multilevel inverters in grid applications. The system combines a robust and high-dynamic direct current control scheme called scalar hysteresis control (SHC) with a feed forward system being able to accurately detect the actual working point and selecting the best possible switching states. This leads to a significant improvement of the overall working behaviour especially under steady state conditions. The combination of SHC with the new feed forward system guarantees both a robust and dynamic working behaviour at any working point as well as optimal steady state operation.

The basic concept of the proposed feed forward system is based on a sensorless approach that is able to accurately detect the inverter output voltage including its harmonic components. The proposed system operates robustly and is independent from the load and any load changes such as impedances. The approach is based on multiple second order generalized integrators (SOGI) used to detect the harmonic components of the inverter output voltage. As a result, the sensorless system is able to operate even under grid disturbances. The generated voltage information can additionally be used for optimizing higher-level power control applications using symmetrical components.

To determine the best switching states of the inverter with minimal effort a coordinate transformation enables using simply integer values. This allows a selection of the best switching positions of multilevel inverter systems by simple mathematical relationships and operations. Since this approach is generic it can easily be extended to higher level inverter systems.

Simulations and experimental measurements using a three- and five-level inverter system are carried out to investigate and prove the proposed controller concept under steady state, harmonic distortions and unexpected grid disturbances. Compared to existing control systems it is shown that the proposed system demonstrates an improved working behaviour under these operating conditions.

Resum

En molts casos i, cada cop més, els sistemes de transformació energètica estan basats en convertidors en font de tensió connectats a la xarxa elèctrica trifàsica. Aquests convertidors necessiten de sistemes de control per controlar els fluxos energètics. Els sistemes de control han de ser estables, però també robustos i precisos durant el seu funcionament normal, però també en condicions on la xarxa pot presentar defectes, com curtcircuits, sots de tensió o desequilibris en la tensió. Degut a l'increment dels requeriments tècnics de connexió i d'eficiència energètica, els convertidors multinivell estan guanyant molt d'interès en aquest tipus d'aplicacions connectades a la xarxa tot i que el seu control i els seus components siguin més complexes.

Aquesta tesi presenta un mètode de control per convertidors multinivell connectats a la xarxa elèctrica. El mètode combina la robustesa davant de canvis en el sistema així com una alta capacitat dinàmica per controlar el corrent injectat a la xarxa. El mètode presentat està basat en l'anomenat Scalar Hysteresis Control (SHC) i incorpora un sistema feed forward que li permet seleccionar acuradament el punt de treball i seleccionar al millor estat de commutació en cada moment. La combinació del SHC amb el feed forward garanteix un comportament robust amb una alta dinàmica en totes les condicions de funcionament.

El concepte bàsic del mètode feed forward proposat no usa sensors i està basat en detectar la tensió de l'inversor que inclou les components harmòniques. El mètode està basat en l'ús d'integradors generalitzats de segon ordre (second order generatlized integrators, SOGI) per tal de detectar les components harmòniques de la tensió de sortida de l'inversor. El sistema pot operar sense sensor de tensió, fins i tot en situacions de defecte de la tensió. Fins i tot, la informació extreta del SOGI es pot usar per altres llaços de control d'ordre superior com el control de la potencia usant les components simètriques.

Per a determinar els millors estats de commutació de l'inversor amb el menor esforç s'usa en el mètode proposat en aquesta tesi un canvi de coordenades que usa valor enters. Això permet l'ús de relacions matemàtiques senzilles que es poden implementar fàcilment i que requereixen una menor potencia de càlcul. A més, el mètode és fàcilment generalitzable.

En la tesi es presenten simulacions i resultats experimentals en convertidors multinivell de tres i cinc nivells per tal d'investigar i demostrar les funcionalitats del sistema de control proposat. Tant les simulacions com els resultats experimentals es realitzen en totes les condicions possibles de la xarxa elèctrica, estat estacionari, sots i distorsions harmòniques.

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Acronyms

µC	Microcontroller.
A/D	Analog to Digital.
AC	Alternating Current.
ANPC	Active Neutral Point Clamped.
BP	Band-Pass.
BPSC	Balanced Positive Sequence Control.
D/A	Digital to Analog.
DC	Direct Current.
DCI	Diode Clamped Inverter.
DDSRF-PLL	Decoupled Double Synchronos Reference Frame Phase Locked Loop.
DIN	German Institute for Standardization.
DPC	Direct Power Control.
DSOGI	Double Second Order Generalized Integrator.
DSP	Digital Signal Processor.
DTC	Direct Torque Control.
Dy	Delta-Star.
EMI	Electromagnetic Interference.
EN	European Norm.
EPLL	Enhanced Phase Locked Loop.
FCI	Flying Capacitor Inverter.
FLL	Frequency Locked Loop.
FPGA	Field Programmable Gate Array.
GI	Generalized Integrator.

H-Bridge	Half-Bridge.
HV	High Voltage.
HVDC	High Voltage Direct Current.
IARC	Instantaneous Active and Reactive Control.
IEEE	Institute of Electrical and Electronics Engineers.
IGBT	Insulated Gate Bipolar Transistor.
LVDS	Low Voltage Differential Signaling.
MMC	Modular Multilevel Converter.
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor.
MPC	Model Predictive Control.
MSOGI	Multi Second Order Generalized Integrator.
NPC	Neutral Point Clamped.
PCC	Point of Common Coupling.
PI	Proportinal-Integral.
PLL	Phase Locked Loop.
PNSC	Positive and Negative Sequence Control.
PWM	Pulse-Width Modulation.
RAM	Random Access Memory.
RRF	Rotating Reference Frame.
SDHC	Switched Diamond Hysteresis Control.
SHC	Scalar Hysteresis Control.
Si	Silicon.
SiC	Silicon Carbide.
SOGI	Second Order Generalized Integrator.
SRF	Stationary Reference Frame.
SRF-PLL	Synchronos Reference Frame Phase Locked Loop.

STATCOM	Static Synchronous Compensator.
SV	Space Vector.
SVM	Space Vector Modulation.
SVPWM	Space Vector Pulse-Width Modulation.
THD	Total Harmonic Distortion.
T-NPC	T-Type Neutral Point Clamped.
TOSSI	Third Order Sinussoidal Integrator.
VCO	Voltage-Controlled Oscillator.
VF	Virtual-Flux.
VF-DPC	Virtual-Flux Direct Power Control.
VHDL	Very High Speed Integrated Circuit Hardware Description Language.
VOC	Voltage Orientated Control.
VSI	Voltage Source Inverter.
WBG	Wide-Bandgab.

List of Symbols

a_*, b_*, c_*	Normalised Components of the a_*b_* Coordinate System.
$\tilde{a}_*$, $\tilde{b}_*$, $\tilde{c}_*$	Components of the $\tilde{a}_*\tilde{b}_*$ System.
$\underline{a}$	Complex Phasor $\underline{a} = \mathrm{e}^{j\frac{2\pi}{3}}$.
α, β, γ	Clarke components.
α', β', α'', β''	Components of the $\alpha'\beta'$ and $\alpha''\beta''$ Coordinate System.
$\underline{B}$	Complex Tolerance Boundary.
B	Tolerance Boundary.
C	Capacitance [F].
ζ	Damping Ratio.
e	Inner voltage source [V].
f	Frequency [Hz].
ψ	Flux [Wb].
Γ	FLL coefficient.
g	Cost Function.
G	Transfer Function.
I,i	Current [A].
$\underline{I}$, $\underline{i}$	Complex Value of Current [A].
Im	Imaginary Part.
j	Imaginary Unit.
k	SOGI coefficient.

κ	Level Count Dependent Normalization Factor for $\tilde{a}_*\tilde{b}_* \rightarrow a_*b_*$.
λ	Power Factor.
L	Inductance [H].
L1, L2, L3	Phase L1, L2, L3.
$\boldsymbol{M}$	Matrix $\boldsymbol{M}$.
M	Modulation Index.
n	Level Count.
N	Neutral Point.
ω	Angular Frequency [rad/s].
P, p	Active Power [W].
π	Pi - $\pi \approx 3.14159$.
q	Phase Shift of $-90°$, $\mathrm{q} = \mathrm{e}^{-j\frac{\pi}{2}}$.
Q, q	Reactive Power [var].
Re	Real Part.
R	Resistance [Ω].
SV, $\vec{\mathrm{SV}}$	Space Vector.
s	Switching Signal of Phase.
θ	Phase Angle [rad].
t	Time.
$\boldsymbol{T}$	Transformation Matrix $\boldsymbol{T}$.
T	Sampling Time.
U, u	Voltage [V].
$\underline{U}$, $\underline{u}$	Complex Value of Voltage [V].
Z	Impedance.

List of Subscripts

a, b, c	Related to Phase a,b,c.
$\alpha\beta\tilde{a}_*\tilde{b}_*$	Transformation Matrix from $\alpha\beta \rightarrow \tilde{a}_*\tilde{b}_*$.
α, β, γ	Clarke Components.
a_*, b_*	Normalised Components of the a_*b_* Coordinate System.
$\tilde{a}_*$, $\tilde{b}_*$	Components of the $\tilde{a}_*\tilde{b}_*$ System.
α', β', α'', β''	Related to $\alpha'\beta'$ and $\alpha''\beta''$ Coordinate System.
avg	Related to Average Value.
base	Base Vector.
block	Block-Time.
BPSC	Related to Balanced Positive Sequence Control.
C	Related to Capacitance.
carr	Related to Carrier Signal.
c_2	Related to Cosine Oscillation with Double Fundamental Frequency.
DC	Related to DC Side.
dead	Dead-Time.
Diode	Related to IGBT.
d, q	Park Components.
ε	Error Signal.
e	Error Component.
F	Related to Filter.
f	Related to Faulted Value.
ff	Related to Feedforward Value.

FLL	Related to Frequency Locked Loop.
fc	Related to Flying Capacitor.
h	Harmonic Component.
hex	Related to Hexagon.
IARC	Related to Instantaneous Active and Reactive Power Control.
IGBT	Related to IGBT.
i	Related to Inner Tolerance Band.
inv	Inverter Output Voltage.
k	Output Voltage Vector Index.
L	Related to Inductance.
max	Maximum.
M	Midpoint.
min	Minimum.
m	Phase to Neutral $m = 1, 2, 3$.
MSOGI	Related to MSOGI.
N	Neutral.
nom	Related to Nominal Value.
opt	Optimum.
o	Related to Outer Tolerance Band.
PNSC	Related to Positive and Negative Sequence Control.
pseudo	Pseudo Reference Voltage.
q	Related to Second SOGI output.
R	Related to Resistance.
real	Related to Real Value.
red	Redundant Space Vector.
ref	Reference Component.
S	Related to Sampling Time.

set	Settling Time.
s_2	Related to Sine Oscillation with Double Fundamental Frequency.
SOGI – BP	Related to SOGI Band-Pass.
SV	Related to Space Vector.
sw	Related to Switch Offset Voltage.
s	Related to Switching Signal.
U, V, W	Inverter Output Phase.
$*$	Component in a_*b_* Format.
(1), (2), (0)	Positive-, Negative-, Zero- Sequence Components.

List of Superscripts

$\hat{}$	Peak Value.
pred	Predicted Value.
$'$	Related to SOGI, MSOGI and FLL Output Value.
$*$	Set Value.

Chapter 1

Introduction

1.1 Background

Within the last decades power electronic devices have become an integral part for the conversion of electrical energy in all power classes. This starts with low power devices like small switching power supplies for mobile devices, drive systems in electric bikes and cars up to large inverters utilized in distribution grids. During this time many topologies and control schemes were developed that can be used for one-phase systems up to any number of phases applied in electrical motor drive systems, in industrial and grid applications [1].

The increasing use of distributed power generation systems, leads to a changing workload and load flow within the grid. Instead of having a few large power plants with rotating generators, a variety of small volatile feeders using power electronics are used [2]. In Germany the generation of renewable energy, mainly by wind turbines and photovoltaics, has increased significantly in the last years. Figure 1.1 shows the development of the gross energy production by renewable sources [3]. As it can be seen the energy generation by renewable sources has more than quintupled since 2000 and in 2017 already 36 percent of the total electric power consumption were generated by renewable sources. This change of power generation puts high demands on the grid stability [4].

To fulfil all grid standards and to increase the efficiency as well as the power quality of the power conversion the development of power electronic devices and topologies and the optimization and advancement of state of the art control concepts is being pursued intensively. These developments include also new power electronic devices such as silicon carbide (SiC) or other wide-bandgap semiconductors (WBG). The advantages of these devices are, among others, a higher blocking voltages and reduced losses compared to

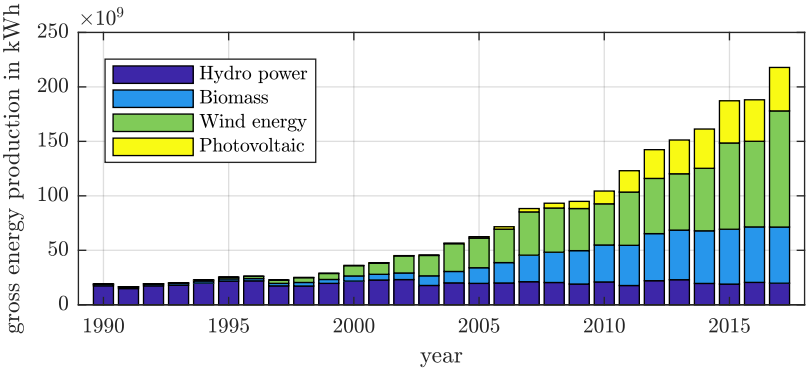


Figure 1.1: Development of gross energy production by renewable energy sources in Germany from 1990 to 2017

standard silicon devices (Si).

Furthermore, various circuit topologies including multilevel inverter systems have become state of the art within a very short time [5]. Intended initially for applications requiring high DC-link voltages like high voltage direct current transmission systems (HVDC) these topologies are increasingly gaining acceptance in the field of industrial and low-voltage applications [6]. However, using multiple power electronic devices such as insulated gate bipolar transistors (IGBTs) or metal-oxide-semiconductor field-effect transistors (MOSFETs) with multiple DC-link capacitor voltages which need to be monitored increase the complexity of the hardware and of the control system. Today and due to the wide availability of fast and low-cost microcontrollers (μC) and field programmable gate arrays (FPGAs) with their parallel calculation capability these complex control requirements can be handled.

Therefore, research on control techniques for grid connected multilevel inverter systems is a highly regarded topic in scientific publications. Many of the published control schemes are based on existing control methods for two-level inverters systems. For the use in multilevel inverter systems, these controllers are extended to higher levels. Thus they carry and copy their individual advantages and disadvantages unchanged to the higher level systems.

1.2 Motivation of Research

The requirements and the desired working behaviour for grid connected inverters depends mainly on the final application. In addition to these individual requirements, the stability and reliability of the inverter systems itself play an important role regardless of the application. Thereby grid connected inverters have to deal with a variety of unpredictable fault cases in their specific applications. The different grid faults defined in the grid standards and are divided in continuous phenomena and voltage events [7]. The most common grid faults and disturbances are:

- Continuous phenomena
  - Fast voltage changes
  - Harmonics and intermediate harmonics
  - Grid frequency changes
  - Grid voltage unbalance
  - Standard signal transmission
- Voltage events
  - Voltage interruption
  - Voltage sags and overshoots
  - Transient overvoltage

The response of the inverter system to the respective grid faults strongly depends on the control method used. Due to their load-independent and highly dynamic working behaviour, direct control methods are ideally suited to handle those fault cases. Nevertheless, because of higher demands on their control system and a worse performance under steady state conditions, compared to indirect control techniques, they are only rarely used as control scheme for inverter systems.

Another important aspect besides the optimal control method for grid connected inverter systems is an appropriate grid synchronization method. The synchronization system must ensure that all informations about the grid e.g. its phase voltages and frequency are correctly detected even during a fault. This is absolutely necessary in order to guarantee a stable operation of the inverter system whenever possible. Especially when considering a grid voltage sensorless inverter system the requirements for both the control and synchronization method are very high.

1.3 Objectives of Research

The main objective of this thesis is the development and the verification of an advancement for a direct current control scheme used in grid connected multilevel inverter systems. The advancement is intended to improve the steady state performance significantly while maintaining the excellent dynamic responsiveness. These two features are essential and key characteristics for grid connected inverters.

As mentioned above an exact detection of the grid voltage is an essential pre-condition for controlling grid connected inverters. Therefore, a major objective of the thesis is to detect this voltage accurately and sensorless. Once this goal is achieved this voltage information can be used for both the improvement of the current controller itself as well as for overall power control. Thus the voltage information should be detected by a specific grid synchronisation method and is used to improve the operating behaviour of the direct current controller under steady state conditions. For this purpose, the voltage informations are used to identify the actual working point of the multilevel inverter system and to select the best switching combinations.

For the selection of the correct switching combinations the high complexity of a multilevel inverter needs to be simplified in order to achieve short calculation times by avoiding high computational effort. These aims lead to the following objectives:

- Straightforward and generic method to quick and simple determine the correct switching combinations.
- Harmonic voltage component detection capability to ensure the selection of the correct switching combinations even in harmonic distorted grids when using multilevel inverter systems.
- Once the synchronization method mentioned above is already an objective of the thesis it should be used as well for higher-level set current calculation to achieve active and reactive power control methods.
- Since the complexity of higher level inverters increases significantly with the level count the new current controller should easily be expendable to multilevel inverter systems with higher level counts and different topologies.
- The thesis is intended to analyse and validate the working behaviour under steady state condition and under different dynamic grid fault conditions.

1.4 Contributions of Research

Based on the preceding objectives the main scientific contributions can be summarized to:

- The thesis introduces an approach to detect the average inverter output voltage without measurement informations. The presented combination of a voltage sensorless synchronization system and direct current control method is able to deal with different fault conditions that can occur within the gird. To further improve the system performance even under harmonic distortions the presented system is able to detect the fundamental component of the inverter output voltage and its grid specific harmonic components.
- On the basis of the exact voltage informations a feed forward system is set up that is able to accurately select the actual sector in the space vector diagram. Under steady state conditions, this system enables a direct current controller to control the current with three neighbouring space vectors without using additional outer tolerance bands. For this purpose, a new coordinate transformation simplifies the representation of the sectors and switching states of multilevel inverter systems. In addition, the general integer-value based description of the multilevel inverter system enables a simple extension to higher level counts and different topologies.
- To ensure the operational capability of the improved current controller concept during dynamic conditions the proposed system is combined with the standard outer tolerance band control concept known from literature. Depending on the actual working point the control system can dynamically choose one of the two sector selection methods to guarantee the best working behaviour under any condition.
- The proposed synchronization system can easily be extended for higher-level active and reactive power controllers. To compensate the filter components a simple mathematical approach using the symmetrical components is applied.
- Simulations and real laboratory measurements using a three- and five-level inverter system are carried out to investigate the behaviour of the new concept under real conditions and different working points. The measurements prove that the proposed system shows an excellent dynamic behaviour, high robustness and a significant improvement in steady state operation compared to the state of the art controllers.

1.5 Thesis Outline

Chapter 1 gives a short introduction to the subject and introduces the background of the thesis. In addition, the motivation, the objectives and the contributions of the thesis are summarised.

Chapter 2 offers a brief survey of the basic functionality of grid connected two-, three- and five-level inverter systems. Existing multilevel topologies with their advantages and disadvantages are described.

Chapter 3 presents an overview of state of the art control techniques for three-phase inverters. Thereby various indirect, direct and predictive controllers are described. Particular attention is given to the effort to extend these controller types to multilevel inverter systems.

Chapter 4 proposes a sensorless voltage detection scheme. The aim of this method is to detect the average output voltage of the inverter including specific harmonic voltage components. With the knowledge of these voltage informations a feed forward sector selection method is presented to improve the working behaviour of a state of the art direct current controller. For this purpose a new coordinate transformation is introduced to simplify the correct selection of sectors and space vectors.

Chapter 5 investigates the improved functionality of the proposed direct current controller method. Different operating characteristics under steady state conditions and during dynamic events are investigated. Simulations of a three- and five-level inverter system using the standard direct current controller and the improved direct current control are carried out and are compared.

Chapter 6 considers the integration of overlaid power control techniques in the proposed system. A short overview of power controllers used in grid application is provided. Compared to the preceding chapter the exact knowledge of the grid voltage needs to be determined. Therefore, the calculation of the grid voltage and the compensation of the inverter filter elements is shown using symmetrical components.

Chapter 7 presents experimental results with real hardware. For this pur-

pose, two test benches are set up in the laboratory. Various measurements on an off the shelf three-level and a self-built five level system with different grid distortions and faults are evaluated.

Chapter 8 summarizes the contributions of the thesis. Some additional aspects of the proposed control concept are described which were discovered during the research work. A list of scientific publications of the author is listed in this chapter.

Chapter 2

Grid Connected Voltage Source Inverter Systems

2.1 Introduction

The use of grid connected voltage source inverters (VSI) increased strongly during the last decades. Nowadays grid connected inverter systems play an important role for an efficient and flexible energy conversion in the grid. Used for various applications such as power supply and different industry applications the main task of these inverter systems is the conversion of electrical energy from direct current (DC) to alternating current (AC) and from AC to AC by the interconnection of two inverters [8]. Figure 2.2 shows a simplified structure of a grid connected inverter system including some typical applications. Hereby, the inverter system (inverter and the filter) serves as a flexible and controllable interface between an energy source or a load and the connected grid.

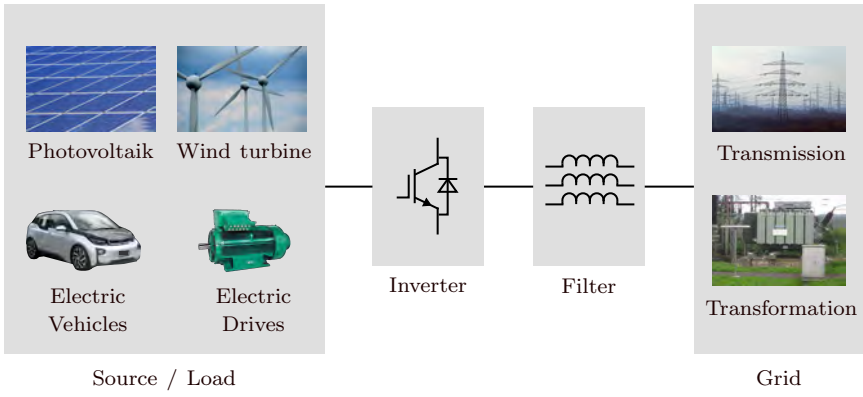


Figure 2.1: Example of grid connected inverter system

The main application areas of grid connected inverter systems are

- Distributed energy generation, primary renewable energy sources such as wind and solar power.
- Compensation of inductive and capacitive reactive power for grid stabilization (e.g. STATCOM).
- DC-link power supply for industry applications (e.g. electric drives).
- Parallel use in combination with non-linear loads (e.g. diode rectifier) as shunt active filter to compensate harmonic components in the output current.
- Grid integration of energy storage systems (e.g. batteries) to compensate local peaks in power generation and consumption.

In the following sections the basic functionality of grid connected inverters are described. Furthermore, the advantages and disadvantages of multilevel inverter systems compared to two-level inverter systems are shown. Therefore, the structure and operation principle of different multilevel topologies is presented.

2.2 System Description and Modeling

The circuit diagram of a simplified three-phase grid connected inverter system is shown in Figure 2.2. The illustrated equivalent three-phase circuit is divided into three main parts: the inverter, the filter and the grid.

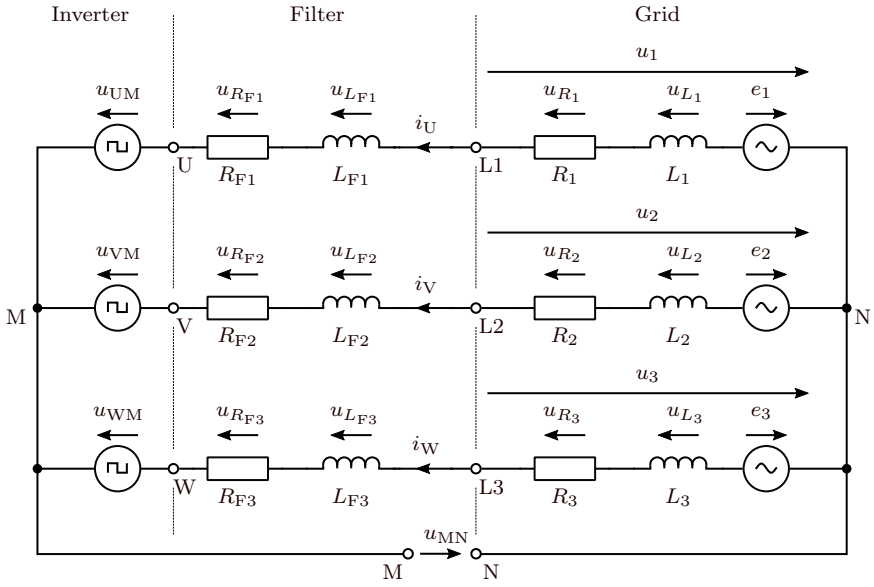


Figure 2.2: Equivalent circuit of a three-phase grid connected inverter system with L-filter

Three-Phase Grid

The first part corresponds to the three-phase grid side with the ideal sinusoidal grid voltage sources e_{123} generating a symmetrical three-phase system with 120° phase shift. The three voltages can thus be described by

$$e_1 = e_{1\mathrm{N}} = \hat{e} \cdot \sin(\omega t) \tag{2.1}$$

$$e_2 = e_{2\mathrm{N}} = \hat{e} \cdot \sin(\omega t - \frac{2\pi}{3}) \tag{2.2}$$

$$e_3 = e_{3\mathrm{N}} = \hat{e} \cdot \sin(\omega t - \frac{4\pi}{3}) \tag{2.3}$$

The inductances L_{123} and resistances R_{123} correspond to the grid impedance Z_{123} which represents the sum of all grid components such as electrical lines and transformers. Due to non-linear loads and other sources of harmonic currents connected to the grid, the voltage drop across the grid impedance leads to distorted grid voltages. The grid connection points L1, L2 and L3 represent the point of common coupling (PCC) and its voltages u_{123} can be calculated by [9]

$$u_1 = u_{1\mathrm{N}} = e_1 - u_{R_1} - u_{L_1} \tag{2.4}$$

$$u_2 = u_{2\mathrm{N}} = e_2 - u_{R_2} - u_{L_2} \tag{2.5}$$

$$u_3 = u_{3\mathrm{N}} = e_3 - u_{R_3} - u_{L_3} \tag{2.6}$$

Filter

The filter serves as coupling element and energy storage between the two voltage sources of the grid and the inverter system. In Figure 2.2 a first order L-filter represented by the inductive component L_F and resistance component R_F is used. Due to the inductance of the filter and the switching operation of the inverter, the current flow and thus the power flow between the grid and the system which is coupled to the DC-side of the inverter can be controlled. The slope of the current can be calculated using the voltage u_{L_F} applied to the inductance. This voltage corresponds to the difference between the grid and the inverter output voltage. The equation for the current slope is defined by

$$\frac{\mathrm{d}i}{\mathrm{d}t} = \frac{u_{L_\mathrm{F}}}{L_\mathrm{F}} \tag{2.7}$$

The size of the inductance must be chosen so, that all limits for the emitted current and voltage harmonics defined in the grid standards at the PCC are fulfilled [10, 11]. Thereby, the in this case used L-filter is the simplest form. In grid applications other filter topologies like the third order LCL-filter are often used as alternative. Compared to the first order L-filter this filter topology offers some advantages such as a smaller inductance to meet the same grid standards [12]. However, the disadvantages like possible system oscillations and instability may increase the design effort and needs to be considered as well [13].

Voltage Source Inverter

The voltage source inverter is the main element of the system and it is represented by the three voltage sources u_{UM}, u_{VM} and u_{WM}. Since the neutral point N is not connected to M in the three-wire grid connection of the inverter system, Kirchhoffs law can be applied leading to

$$0 = i_u + i_v + i_w \tag{2.8}$$

This leads to the fact that the current slope to be controlled is limited to

$$0 = \frac{\mathrm{d}i_{\mathrm{U}}}{\mathrm{d}t} + \frac{\mathrm{d}i_{\mathrm{V}}}{\mathrm{d}t} + \frac{\mathrm{d}i_{\mathrm{W}}}{\mathrm{d}t} \tag{2.9}$$

A simplified representation of a grid connected inverter system is shown in Figure 2.3. The inverter side is represented by the voltage source u_{UVW} which is connected to the neutral point N of the grid.

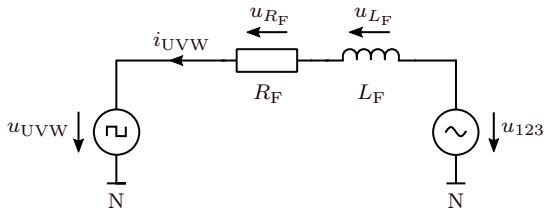


Figure 2.3: Simplified equivalent circuit of a grid connected inverter system with L-filter

Since the neutral point N is not connected in the three-wire application the inverter output voltages u_{UM}, u_{VM} and u_{WM} need to be summed up with the auxiliary voltage u_{MN} to calculate the voltages u_{U}, u_{V} and u_{W}.

$$u_{\mathrm{U}} = u_{\mathrm{UN}} \tag{2.10}$$

$$u_{\mathrm{V}} = u_{\mathrm{VN}} \tag{2.11}$$

$$u_{\mathrm{W}} = u_{\mathrm{WN}} \tag{2.12}$$

The grid side is represented by the voltage source u_{123} which is the voltage at the PCC. The inductive and resistive components of the grid impedance are neglected in this simplified representation because they are not exactly known and much smaller than the filter components. Furthermore, it is

assumed that the filter inductance L_F and R_F are constant in all three phases. Due to this simplification, the following equation can be used to describe the overall system

$$u_{123} = u_\mathrm{UVW} + R_\mathrm{F} \cdot i_\mathrm{UVW} + L_\mathrm{F} \cdot \frac{\mathrm{d}i_\mathrm{UVW}}{\mathrm{d}t} \tag{2.13}$$

Another common method to mathematically describe a grid connected inverter system uses the virtual-flux (VF). This method is based on the fact that the simplified circuit diagram of an electric drive is identical to that of a grid connected system [14]. Therefore, the inductive and resistive components represent the stator resistance and leakage inductance of the virtual motor. The phase voltages are considered to be generated by the air gap flux. This leads to the following expression

$$\psi_{123} = \int (u_\mathrm{UVW} + R_\mathrm{F} \cdot i_\mathrm{UVW})\ \mathrm{d}t + L_\mathrm{F} \cdot i_\mathrm{UVW} \tag{2.14}$$

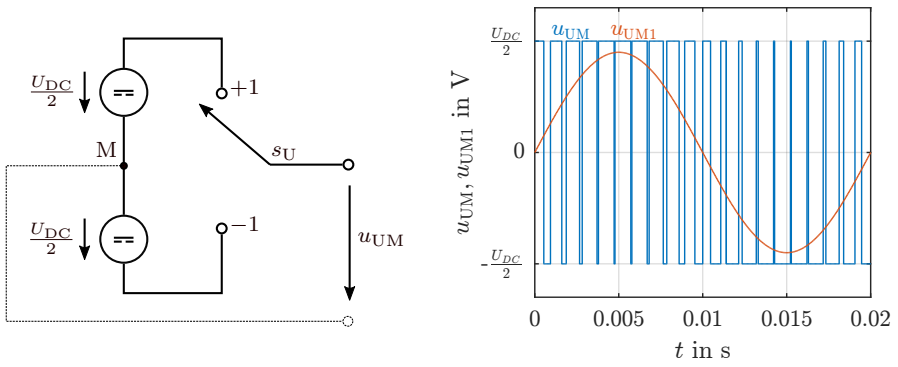
On the basis of this VF-modeling, it is possible to better describe and regulate voltage sensorless systems due to the low-pass characteristics of the integrator [15].

2.2.1 Two-Level Voltage Source Inverter

The basic working principle of a three-phase two-level inverter system which is state of the art in most low-voltage grid applications will be explained in the following section. As shown in Figure 2.4a for a single phase leg this inverter type can be simplified by an ideal switch and a series connection of two identical DC-sources both with $U_\mathrm{DC}/2$. This leads to the possibility to switch $\pm U_\mathrm{DC}/2$ to the output.

Figure 2.4b shows the generated output voltage of a single-phase two-level inverter system. In this example the output states are modulated in a way that the sinusoidal reference voltage u_UM1 is reconstructed using a classical pulse-width modulation (PWM) method. Due to the switching between the maximum available DC-voltages a high $\mathrm{d}i/\mathrm{d}t$ at the output is created.

$$u_\mathrm{UM} = \begin{cases} +U_\mathrm{DC}/2 \text{ for } s_\mathrm{U} = +1 \\ -U_\mathrm{DC}/2 \text{ for } s_\mathrm{U} = -1 \end{cases}$$



(a) Simplified circuit diagram

(b) Modulated output voltage u_{UM} and its reference voltage u_{UM1}

Figure 2.4: Simplified model and generated output voltage of a single-phase two-level inverter

Considering a three-phase two-level inverter system application with common DC-link, the number of possible output switching state combinations increases to eight. A circuit diagram of a three-phase inverter is shown in Figure 2.5. Each phase is represented by two IGBT's connected in series with their corresponding anti-parallel diode. The two voltage sources on the DC-side are replaced by capacitors which serve as energy storage between AC and DC-side.

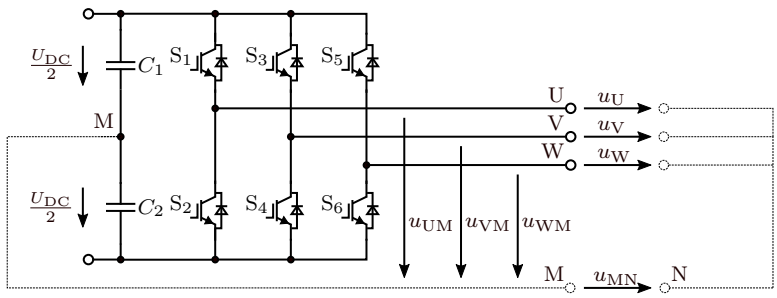


Figure 2.5: Circuit diagram of a three-phase two-level inverter system

Compared to the ideal switch in Figure 2.4a the switching position 1 is achieved by turning on the upper IGBT and the switching position −1 by turning on the lower IGBT. According to the output state s_{UVW} this type can generate three possible phase to phase voltages.

$$u_{\mathrm{UV}} \in \{+U_{\mathrm{DC}}, 0\ \mathrm{V}, -U_{\mathrm{DC}}\}$$

To calculate the generated output voltages u_{U}, u_{V} and u_{W} against the neutral point N, the relationship between the three phases in a three-wire system need to be considered. Using the following equation the auxiliary voltage u_{MN} can be calculated by

$$u_{\mathrm{MN}} = -\frac{1}{3} \cdot (u_{\mathrm{UM}} + u_{\mathrm{VM}} + u_{\mathrm{WM}}) \tag{2.15}$$

The phase to neutral voltages u_{UVW}, the inverter output voltages against the auxiliary midpoint M and the voltage u_{NM} can be calculated using

$$u_{\mathrm{U}} = u_{\mathrm{UM}} + u_{\mathrm{MN}} \tag{2.16}$$

$$u_{\mathrm{V}} = u_{\mathrm{VM}} + u_{\mathrm{MN}} \tag{2.17}$$

$$u_{\mathrm{W}} = u_{\mathrm{WM}} + u_{\mathrm{MN}} \tag{2.18}$$

The eight possible switching states, the resulting phase to neutral voltages u_{U}, u_{V} and u_{W} and the auxiliary voltage u_{MN} are listed in Table 2.1.

Table 2.1: Output voltage levels of a two-level inverter system in the three-phase UVW-system for all possible switching combinations

State	Switch positions	$u_{\mathrm{U}}/U_{\mathrm{DC}}$	$u_{\mathrm{V}}/U_{\mathrm{DC}}$	$u_{\mathrm{W}}/U_{\mathrm{DC}}$	$u_{\mathrm{MN}}/U_{\mathrm{DC}}$
0	−1 −1 −1	0	0	0	−1/2
1	1 −1 −1	2/3	−1/3	−1/3	−1/6
2	1 1 −1	1/3	1/3	−2/3	1/6
3	−1 1 −1	−1/3	2/3	−1/3	−1/6
4	−1 1 1	−2/3	1/3	1/3	1/6
5	−1 −1 1	−1/3	−1/3	2/3	−1/6
6	1 −1 1	1/3	−2/3	1/3	1/6
7	1 1 1	0	0	0	1/2

As it is apparent, the eight possible switching combinations can generate seven different voltage levels. The output state 0 with the switching position $[-1\ -1\ -1]$ and the output state 7 with the switching position [1 1 1] generate the same voltage in all three phases. Therefore, these two switching combinations are called redundant states. In the case of the two-level inverter system those states correspond to the zero voltage states.

2.2.2 Space Vector Representation

The space vector (SV) representation is an important part for the control of three-phase inverter systems. The basis for this approach is a coordinate transformation which was presented by Edith Clarke in 1950 [16]. The aim of this transformation is to convert a three-phase system, typically sinusoidal with three 120° phase shifted components to an orthogonal two-phase system. The so called $\alpha\beta$-system or stationary reference frame (SRF) is used to represent a symmetrical three-phase voltage u_{UVW} as a rotating vector $\underline{u}$. Due to the use of a three-phase three-wire system and the non-consideration of possible common-mode currents caused by capacitances to ground in the system the third Clarke component γ is neglected.

The geometrical relationship of the two systems is illustrated in Figure 2.6. As one can see the α-axis is orientated along the U-axis whereas the β-axis is phase shifted by 90°.

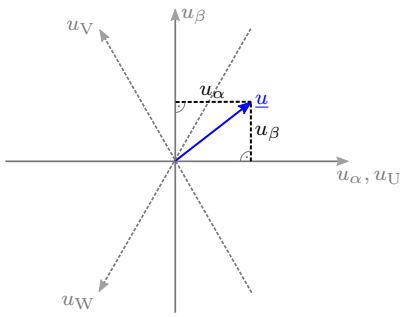


Figure 2.6: Geometrical representation of $\alpha\beta$-system

The mathematical relationship to calculate the $\alpha\beta$ components from the UVW components is given by

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \boldsymbol{T}_{\alpha\beta} \cdot \begin{bmatrix} u_\mathrm{U} \\ u_\mathrm{V} \\ u_\mathrm{W} \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} u_\mathrm{U} \\ u_\mathrm{V} \\ u_\mathrm{W} \end{bmatrix} \tag{2.19}$$

The factor 2/3 is used to unify the amplitudes of the $\alpha\beta$ and UVW coordinate systems. Due to the precondition that the sum of the three voltages is zero only two phases need to be measured. Therefore, the equation can be simplified to

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} 1 & 0 \\ \frac{1}{\sqrt{3}} & \frac{2}{\sqrt{3}} \end{bmatrix} \cdot \begin{bmatrix} u_\mathrm{U} \\ u_\mathrm{V} \end{bmatrix} \tag{2.20}$$

Considering the eight possible output voltages of the three-phase two-level inverter system, the voltages can be represented in the $\alpha\beta$ coordinate system. Those output states within the $\alpha\beta$-system are called space vectors. In Table 6.1 the eight output switching combinations with the corresponding $\alpha\beta$ voltages are listed.

Table 2.2: Output voltage levels of two-level inverter system in the two-phase $\alpha\beta$ system for all possible switch combinations

State	Space vector	Switch positions	u_α/U_DC	u_β/U_DC
0	SV_0	$-1\ -1\ -1$	0	0
1	SV_1	$1\ -1\ -1$	2/3	0
2	SV_2	$1\ \ 1\ -1$	1/3	$\sqrt{3}/3$
3	SV_3	$-1\ \ 1\ -1$	$-1/3$	$\sqrt{3}/3$
4	SV_4	$-1\ \ 1\ \ 1$	$-2/3$	0
5	SV_5	$-1\ -1\ \ 1$	$-1/3$	$-\sqrt{3}/3$
6	SV_6	$1\ -1\ \ 1$	1/3	$-\sqrt{3}/3$
7	SV_7	$1\ \ 1\ \ 1$	0	0

The geometrical representation of the space vectors in the $\alpha\beta$ coordinate system is shown in Figure 2.7. As one can see the space vectors span up a hexagon with six identical triangular sectors.

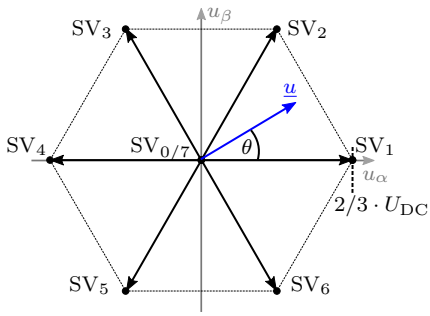


Figure 2.7: SV-diagram of a two-level inverter system with eight space vectors

The side length of each triangular sector is scaled to $2/3 \cdot U_{\mathrm{DC}}$. The corner points of the hexagon correspond to the six active space vectors (1 to 6) and the two redundant zero voltage space vectors (0 and 7) correspond to the centre point. In addition to eight switching states of the two-level inverter the voltage vector $\underline{u}$ and the corresponding phase angle θ is shown in Figure 2.7.

$$u_{\alpha\beta} = \underline{u} = \hat{u} \cdot e^{j\theta} \tag{2.21}$$

$$\theta = \tan^{-1}\left(\frac{u_\beta}{u_\alpha}\right) \tag{2.22}$$

The length of the vector can be used to describe the actual operating point of the inverter system with the so called modulation index M. According to Equation 2.23 this value is calculated from the ratio between the peak input voltage and half of the DC-link voltage.

$$M = \frac{2 \cdot \hat{u}}{U_{\mathrm{DC}}} \tag{2.23}$$

2.3 Multilevel Inverters

The basic idea of multilevel inverters is to provide a more sinusoidal output voltage using multiple individual but equal DC-voltages (levels). Therefore, multilevel inverters are defined by the number of possible output voltages ≥ 3 in single-phase operation. With an increasing number of individual voltages the inverter output voltage reproduces a more sinusoidal waveform leading to less harmonic distortions. Basically, the individual voltages are generated by splitting the DC-link voltage into several equally distributed parts. The basic idea to use standard power electronic devices for higher voltages than the blocking voltage of the devices was firstly presented 1975 [17]. Further developments of multilevel inverter topologies and hardware concepts based on the same working principle are presented in [18, 5]. Nowadays multilevel inverters are already used in low-voltage applications for grid connected inverter systems. The main advantages of using multilevel inverters are

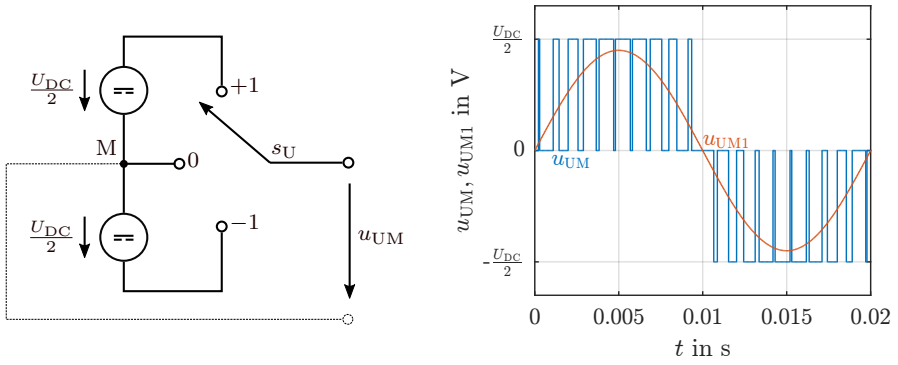
- A more sinusoidal output voltage of the inverter due to the increased number of output voltage steps
- Possible reduction of passive filter components due to the lower $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}u/\mathrm{d}t$ values
- Reduced harmonic distortions within the inverter output voltages and currents
- Realization of higher DC-link voltages due to the interconnection of standard active and passive power electronic components without using expensive HV-components or directly series connected devices.
- Improved electromagnetic interference (EMI)
- Reduced system oscillations on the load side due to the lower du/dt that could damage the connected system
- Fail-safe operation in some special topologies of multilevel inverters

The main disadvantage of multilevel inverters is a higher demand on passive and active power electronic devices such as IGBTs and diodes with negative effects on the reliability of the grid connected inverter system. The increased number of possible switching states requires a more complex control and the need of additional control aspects like DC-link balancing.

In the following subsections the general operation of a three- and five-level inverter system by means of a simplified representation are explained in more detail.

Three-Level Inverter

A simplified single-phase circuit diagram of the three-level inverter system and the generated output voltage are shown in Figure 2.8. The DC-link is similar to the two-level inverter divided into two parts represented by two DC-sources with $U_{\mathrm{DC}}/2$ each. Additionally to the voltage potentials $\pm U_{\mathrm{DC}}/2$ the midpoint voltage 0 V can be switched to the output.



(a) Simplified circuit diagram

(b) Modulated output voltage u_{UM} and its reference voltage u_{UM1}

Figure 2.8: Simplified model and output voltage of a single phase three-level inverter

Figure 2.8b shows the additional voltage level. According to the sign of the sinusoidal reference voltage u_{UM1} only the switching states $+U_{\mathrm{DC}}/2$ and 0 V or, $-U_{\mathrm{DC}}/2$ and 0 V are used to modulate the voltage.

$$u_{\mathrm{UM}} = \begin{cases} +U_{\mathrm{DC}}/2 & \text{for } s_{\mathrm{U}} = +1 \\ 0\ V & \text{for } s_{\mathrm{U}} = 0 \\ -U_{\mathrm{DC}}/2 & \text{for } s_{\mathrm{U}} = -1 \end{cases}$$

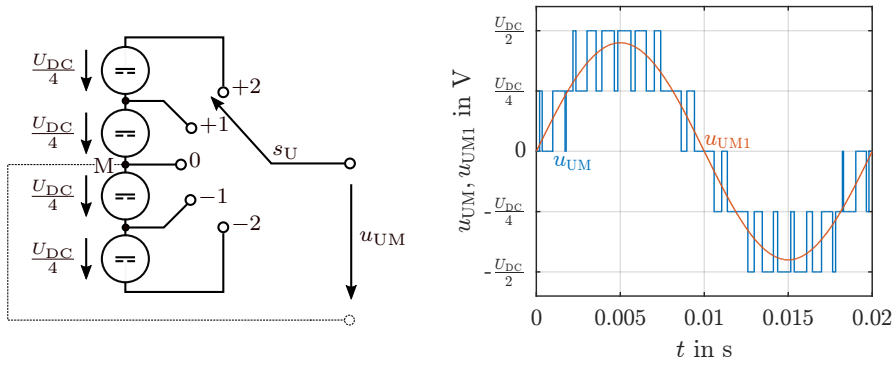
In a three-phase application the three-level inverter system can generate a total number of 27 output states where nine of them are redundant switching states. These states are often used to balance the the DC-link capacitor voltages of the inverter system. To balance the capacitor voltages the fact that the redundant states provide the same output voltage with inverse effect on the DC-link capacitor currents is used. Out of the three voltage levels of

one phase leg the three-phase three-level inverter system can generate a total number of five phase to phase voltages and nine phase to neutral voltages.

$$u_{\mathrm{UV}} \in \{+U_{\mathrm{DC}}, +U_{\mathrm{DC}}/2, 0\ V, -U_{\mathrm{DC}}/2, -U_{\mathrm{DC}}\}$$

Five-Level Inverter System

Considering a five-level inverter system the DC-link is divided into four parts as it is shown in the simplified model in Figure 2.9a. Therefore, each DC-source has a voltage of $U_{\mathrm{DC}}/4$.



(a) Simplified circuit diagram

(b) Modulated output voltage u_{UM} and its reference voltage u_{UM1}

Figure 2.9: Simplified circuit diagram and generated output voltage of a single phase five-level inverter

The generated output voltage of the five-level inverter system with its five voltage steps is shown in Figure 2.9b. The designations for the five possible output voltage states are defined to be from -2 to $+2$ generating the inverter output voltages

$$u_{\mathrm{UM}} = \begin{cases} +U_{\mathrm{DC}}/2 \text{ for } s_{\mathrm{U}} = +2 \\ +U_{\mathrm{DC}}/4 \text{ for } s_{\mathrm{U}} = +1 \\ 0\ V \quad\ \text{for } s_{\mathrm{U}} = 0 \\ -U_{\mathrm{DC}}/4 \text{ for } s_{\mathrm{U}} = -1 \\ -U_{\mathrm{DC}}/2 \text{ for } s_{\mathrm{U}} = -2 \end{cases}$$

When using a five-level inverter in a three-phase system the total number of possible output state combinations increases to 125. The related number of phase to phase voltage levels is rising up to nine and the possible number of phase to neutral voltages to 17 different voltages.

$$u_{\mathrm{UV}} \in \{+U_{\mathrm{DC}}, +3U_{\mathrm{DC}}/4, +U_{\mathrm{DC}}/2, +U_{\mathrm{DC}}/4,\ 0\ V, \\ -U_{\mathrm{DC}}/4, -U_{\mathrm{DC}}/2, -3U_{\mathrm{DC}}/4, -U_{\mathrm{DC}}\}$$

For multilevel inverters with n-levels the step voltage can be calculated by applying the following equation

$$u_{\mathrm{UM}} = \frac{U_{\mathrm{DC}}}{n-1} \tag{2.24}$$

Considering the three-phase application of a n-level inverter system the total number of possible output states increases to n^3, the associated number of phase to phase voltages to $2 \cdot n - 1$ and the total number of phase to neutral voltages to $4 \cdot n - 3$. For the example of the 13-level inverter system 8192 possible output state combinations with 49 possible phase to neutral voltages need to be considered.

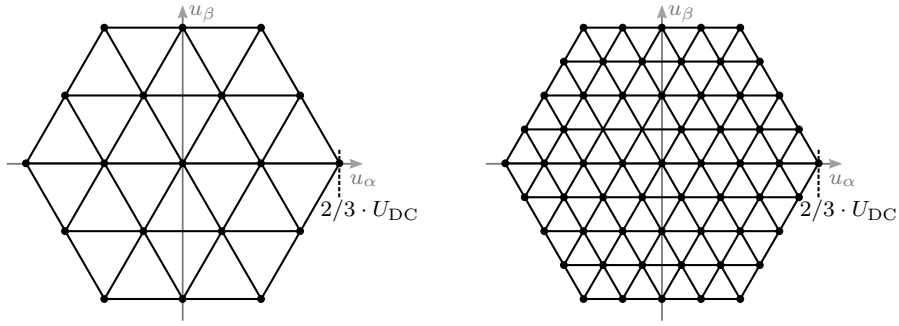
Space Vector Representation of Three- and Five-Level Inverters

The level count n shows a major impact on the SV-representation of the inverter system. While the outer voltage dimensions of the hexagonal SV-diagram in the $\alpha\beta$ system remain the same, the number of possible space vectors and triangular sector increases as a function of the level count.

The effect of a three-phase three-level inverter system with its 27 switching state combinations on the SV-diagram is shown in Figure 2.10a. The table with all switching possibilities and the corresponding voltages in the $\alpha\beta$ system are shown in Appendix A. As one can see the SV-diagram includes only 19 different voltage positions in the $\alpha\beta$ system. This is due the fact that eight space vector positions have redundant space vectors. The zero voltage vector can be generated by three different switching combinations ([−1 −1 −1], [0 0 0] and [1 1 1]). In addition to the zero voltage vectors, each of the six active space vector positions on the inner hexagon can be generated with two switching states, each of them with a reverse impact on the DC-link capacitor voltage. Some of the space vectors on the outer hexagon also have an impact on the DC-link capacitor voltages without being able to provide redundant switching possibilities. Compared to the two-level

inverter the resulting size of the triangular sectors decreases whereas the number of sectors increases to 24.

A similar characteristic can be seen in the three-phase five-level inverter system SV-diagram which is shown in Figure 2.10b. The 125 output switching combinations can only generate 61 different voltages in the $\alpha\beta$ system. The zero voltage vector can be generated with five different combinations. The number of possible redundant states decreases by one from midpoint to the outer hexagon where no redundant space vectors are available.



(a) Three-level SV-diagram (b) Five-level SV-diagram

Figure 2.10: SV-diagrams of selected multilevel inverters

The basic structure of the SV-diagram of a n-level inverter system with its voltage positions and number of redundant states remains the same regardless of the used hardware topology. However, the number of available hardware switching states reproducing the n voltage levels can vary with different topologies. In general, the total number of triangular sectors in the SV-diagram increases quadratically with the level count n leading to the following expression

$$\text{Number of triangular sectors} = 6 \cdot (n-1)^2 \tag{2.25}$$

The number of different space vector voltage positions increases accordingly with $n^3 - (n-1)^3$. The number of redundant space vectors rises to $(n-1)^3$.

2.4 Multilevel Topologies

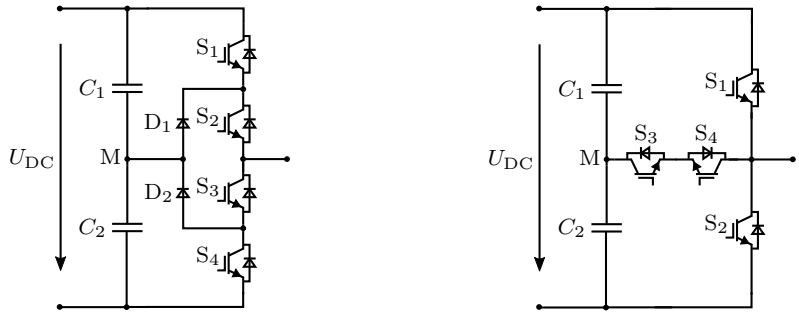
Since the first valuable concepts of multilevel hardware topologies were proposed in the 1980s the interest on these inverter types rapidly grows. The concepts leads to many different topologies that were introduced through the last decades [18, 19]. Besides the ability to use standard power electronic devices in medium and high voltage applications the use of multilevel inverter systems in low-voltage applications such as photovoltaic systems is driven by increased demands on the power quality and system costs. In the following sections a selection of multilevel inverter structures is described. Thereby, the different topologies can be divided according to their basic setup. The first group are special developments for multilevel inverters using active and passive power electronic devices as clamping elements for the connection to a subdivided common DC-link. The second group uses flying capacitor cells in each phase to produce intermediate voltage steps. The third group which is mainly used for higher level counts is the cell based multilevel inverter structure. This type uses a simple series connection of state of the art two-level inverter structures to guarantee the multilevel behavior.

2.4.1 Diode Clamped Multilevel Inverter

The neutral point clamped (NPC) multilevel inverter topology was first introduced in [20]. This state of the art concept belongs to the so called diode clamped inverters (DCI). As illustrated in Figure 2.11a, each phase of a three-level NPC inverter consists of four transistors and six diodes. The two clamping diodes connect the centre of the DC-link capacitors M to the connection point between the outer and inner transistors. Compared to a two-level inverter this structure provides the additional switching state 0 by selecting the two inner transistors. To switch $\pm U_{\mathrm{DC}}/2$ the two upper (for state 1) or two lower transistors (for state -1) have to be turned on.

A modification of the three-level NPC is the T-Type neutral point clamped inverter (T-NPC) which was introduced in [21]. In this configuration, IGBTs connected in opposed direction are used to control the midpoint current. To apply the full voltage to the output only one IGBT for state 1 and -1 has to be switched on. Compared to the NPC topology this results in different operating characteristics and efficiency at varying modulation ranges and switching frequencies for both configurations [22].

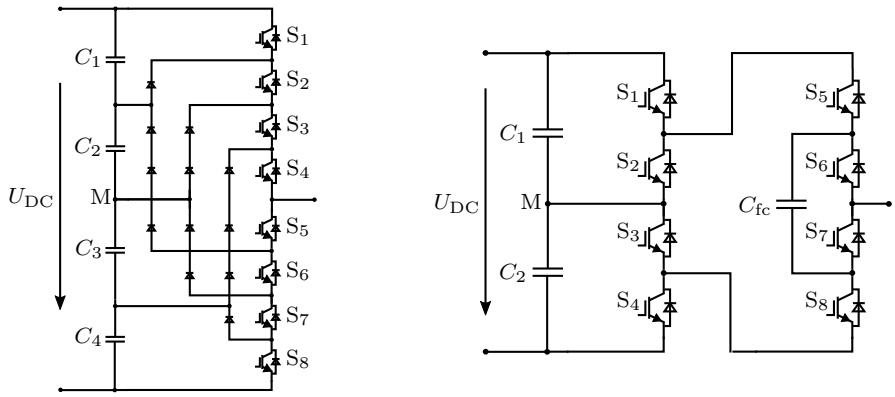
The extension of the NPC topology to higher level counts was presented in [23]. The necessary number of components for n-level DCI inverters in-



(a) Three-level NPC (DCI) (b) Three-level T-Type NPC

Figure 2.11: Single-phase schematics of possible three-level NPC configurations using passive or active components

creases to $3{\cdot}2{\cdot}(n{-}1)$ transistors, $n{-}1$ DC-link capacitors and $3{\cdot}(n{-}1){\cdot}(n{-}2)$ clamping diodes. A phase leg of a five-level DCI is shown in Figure 2.12a. By connecting the ports of the four DC-link capacitors the additional output voltages $\pm U_{DC}/4$ are available. Unfortunately, the five-level DCI can not be used without certain precautions because of the limited DC-link balancing ability for a higher modulation index [24].



(a) Five-level DCI (b) Five-level ANPC

Figure 2.12: Single-phase schematics of possible five-level configuration for the DCI (NPC) topology

Another promising hardware topology to extend a three-level NPC to higher levels is the combination with a flying-capacitor converter to create a hybrid configuration called active neutral point clamped inverter (ANPC) [25]. One phase leg of an ANPC is shown in Figure 2.12b. While the two common DC-link capacitors remain charged with $U_{\mathrm{DC}}/2$ the flying capacitor which needs to be added in each phase has to be controlled to $U_{\mathrm{DC}}/4$. To increase the level count of the ANPC structure additional flying capacitor cells have to be added.

2.4.2 Flying Capacitor Multilevel Inverter

The capacitor clamped or flying capacitor inverter (FCI) topology was first presented in [26]. Figure 2.13 shows the circuit diagram of a single phase three-level FCI. Like the NPC topology each phase of the FCI consists of four transistors. Instead of diodes connecting the midpoint M between the upper and lower transistors, the FCI uses a separate capacitor cell in each phase.

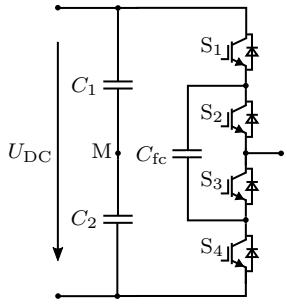


Figure 2.13: One-phase schematic of three-level FCI

This flying capacitor C_{fc} is charged to $U_{\mathrm{DC}}/2$ and has no connection to the common DC-link and to the other phases. To select the output states 1 and -1 with the voltages $+U_{\mathrm{DC}}/2$ and $-U_{\mathrm{DC}}/2$ the two upper or two lower IGBTs need to be switched on. The third state that corresponds to the output voltage of 0 V can be realized by switching on IGBT S_1 and S_3 or S_2 and S_4. Using these redundant states the current direction through the capacitor can be adjusted to control the cell voltage.

As described in [26] the functional principle of the FCI inverter can easily be adapted to higher level systems. To implement a five-level FCI three cells for each phase are required. Each cell is, therefore, charged to a different voltage level. For a five-level the inner cell has to be charged to $U_{\mathrm{DC}}/4$, the middle cell to $U_{\mathrm{DC}}/2$ and the outer cell to $3U_{\mathrm{DC}}/4$. The limited balancing capability of the NPC does not exist when using the FCI. Because of the separated cells and additional switching possibilities in each phase the FCI has a higher degree of freedom and more flexibility compared to the NPC inverter [18]. In return, the high number of capacitors leads to a greater monitoring effort.

2.4.3 Cascaded H-Brigde Inverter

A common and frequently mentioned cell based structure is the H-bridge multilevel inverter topology which was presented in [27]. The behaviour of a multilevel inverter is reproduced by the interconnection of several and independent H-bridge modules in series. Figure 2.14 shows this topology for a three-phase five-level application.

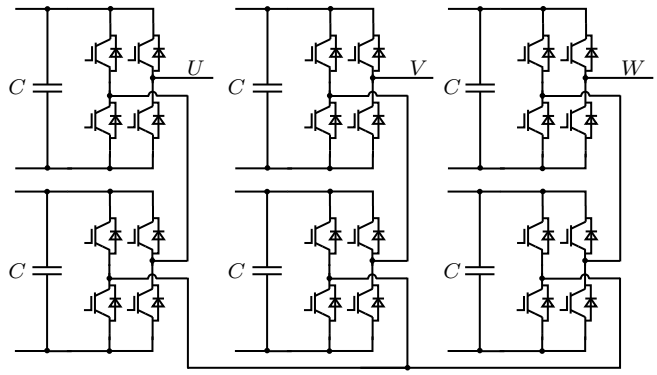


Figure 2.14: Three-phase schematic of five-level H-bridge inverter system

The output voltage levels are generated by connecting or bypassing the DC-link capacitors in series. This fact leads to an easy expanse capability to any level count by adding more H-bridge cells. The required number of H-bridges per phase for n-level inverter system is $(n-1)/2$. The main disadvantage of this topology is that each H-brigde needs a separate and isolated DC-source. To overcome this disadvantage a multi-winding transformer with

several secondary windings and a rectifier for each H-bridge module is often used [28].

2.4.4 Modular Multilevel Converter

A cell based topology which is state of the art in most high voltage applications is the modular multilevel converter (MMC) [29, 30]. As shown in Figure 2.15 each phase of a five-level inverter consists of 8 submodules. The total number of submodules for a n-level inverter system is defined by $2 \cdot (n-1)$. In the simplest case each submodule is built from a half-bridge cell with two transistors and one capacitor. The transistors are used to connect the capacitor in series to the output or to bypass it. The sum of all capacitor voltages is twice the voltage of the connected common DC-link. In normal operation mode half of the submodule capacitors are connected in series and the other half is bypassed. The two inductors at the phase connection point are necessary to minimize the circulating currents during the switching events.

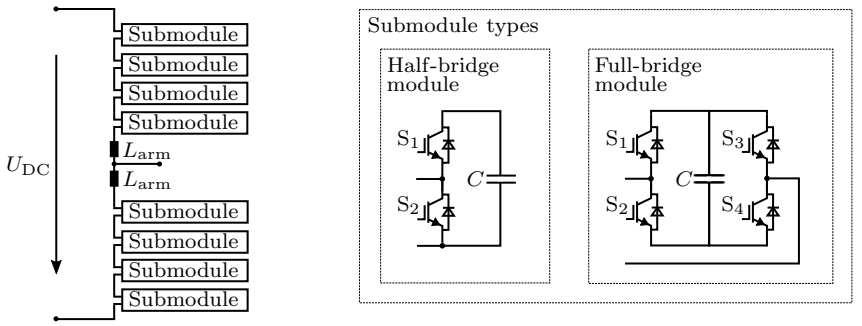


Figure 2.15: One-phase five-level MMC and possible submodules

Instead of using a half-bridge cell several other topologies (even NPC or FCI) can be used as submodule as well [31]. A frequently used cell topology is the full-bridge cell which makes the MMC fault tolerant against short circuits on the DC-side. Further advantages of the MMC topology are the possibility to built up redundant cells or bypass damaged cells to increase the availability of the system. A drawback of this topology is that each capacitor voltage needs to be monitored and balanced during operation. This leads to increased demands in the control scheme.

2.5 Summary

This chapter shows the basic operation of two-level and multilevel grid connected inverter systems and an abstract of several topologies. To allow a comparison between the different multilevel topologies the component effort of the previously mentioned topologies is shown in Table 2.3. For the MMC topology half-bridge submodules are considered. In addition to the components each hardware topology has special requirements that need to be considered by the the used control algorithm.

Table 2.3: Comparison of multilevel inverter topologies

	DCI (NPC)	FCI	H-Brigde	MMC (HB)
Switches	$2 \cdot (n-1)$	$2 \cdot (n-1)$	$2 \cdot (n-1)$	$4 \cdot (n-1)$
DC-link capacitors	$n-1$	$n-1$	$\frac{3}{2} \cdot (n-1)$	$2 \cdot (n-1)$
Clamping diodes	$(n-1) \cdot (n-2)$	0	0	0
Clamping capacitors	0	$(n-2) \cdot \left(\frac{n-1}{2}\right)$	0	0
DC-link sources	1	1	$\frac{3}{2} \cdot (n-1)$	1

Chapter 3

Control and Modulation Techniques for Multilevel Inverters

The control of grid connected inverter systems is subject of research and discussion since many decades [32, 33, 34]. The developments are driven forward due to different requirements and specific use cases in grid connected applications. However, the main objective for grid connected inverters is to accurately control the active power p and the reactive power q with a unity power factor λ. Most of the control methods used today were originally developed for electrical machines and were later adopted for grid application. In comparison to electric drives, a controller used in grid applications needs to include additional aspects like unknown grid conditions and unpredictable disturbances caused by other loads and feeders in the system. Furthermore, the controller needs to be robust against dynamic grid faults like, typical voltage sags, short time interruptions or phase jumps as well as other system variations [7].

Based on their structure and basic characteristics, the controllers can be subdivided into three main groups. These groups are indirect, direct and predictive control techniques. A simplified representation of the three different types is shown in Figure 3.1. All three control techniques use the current error signal i_e as an input signal. The output signal is the actual output switching signal that has to be applied by the inverter. Necessary transformations are neglected in this figure.

The most important component of indirect control systems is the inner current controller loop which generates the reference voltage. The modulator use this voltage as input to select the switching states to reproduce this voltage. Due to their easy application and the availability of suitable microcontrollers indirect control techniques have established themselves as state of the art in most grid applications today. The rarely used group of direct controllers are applied in cases where very high dynamic performance

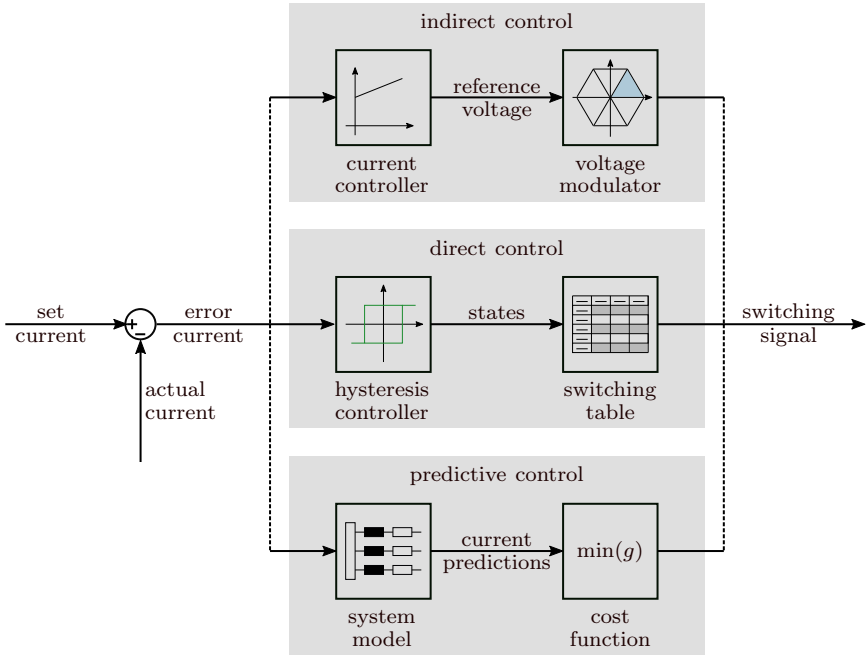


Figure 3.1: Simplified structure of indirect, direct and predictive control systems

is required (e.g. weak grids). In most cases this controller type consists of a hysteresis controller and a switching table which selects the output switching state according to the actual state of the hysteresis band. The third group are predictive controllers. Due to the increasing computational power of microcontrollers and the use of FPGAs with their parallel computing ability predictive controllers are a good alternative for several applications.

In addition to the development of two-level inverter control methods the control of multilevel inverters for low-voltage applications is part of intensive research. When using multilevel inverters the complexity increases because of additional switching states and additional control tasks like DC-link balancing. These aspects need to be considered when investigating control systems for multilevel inverters. When comparing the control methods the main focus is on the applicability to multilevel inverters (in this case three- and five-level) and the increased complexity when selecting the switching states. The following overview concentrates on the main control task for multilevel inverters only. The DC-link balancing is initially neglected.

3.1 Indirect Control Techniques

The group of indirect current controllers also known as voltage orientated control (VOC) is mostly used for power electronic devices [32]. To realize a desired output current the output voltage of the inverter is applied by a modulator which selects the corresponding switching state or sequence of states. The concept to generate this voltage will be explained in Chapter 3.1.2 by way of example.

The main advantages of using indirect control techniques are [35]:

- Fixed switching frequency of the inverter
- Good steady-state performance
- The voltage modulator generates a well defined harmonic spectrum
- Simple and state of the art implementation with microcontrollers
- Good DC-link voltage utilization

The main disadvantages are the inferior dynamic reaction compared to direct controllers and the load depending design of the required linear controllers caused by delays of the controller, dead times of the used inverter circuitry and system non-linearities [36]. Since the following subsections considers the functionality of the selection of the correct inverter switching states, the structure and operation of different modulators is mainly considered as part of an indirect control system.

3.1.1 Carrier Based Modulation

The most simple realization of a modulator for an indirect controlled inverter system is the carrier based PWM [37]. The switching signals are generated by comparison of the set voltage with a high frequency carrier signal. Possible waveforms for the carrier signal are triangular, sawtooth or a trapezoidal signal. The carrier is related to the DC-link voltage and has a peak to peak value of U_{DC} in the case of a two-level inverter. The frequency of the carrier signal specifies the inverter switching frequency. Furthermore, it generates a well defined output pulse pattern. A simplified diagram of this controller type is shown in Figure 3.2.

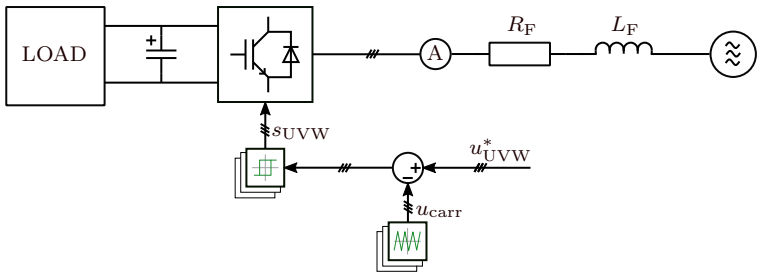


Figure 3.2: Carrier based PWM modulator scheme

As it is shown, each phase of the inverter needs a separate modulator. The difference between the set voltage u^*_{UVW} and the carrier is used to trigger a comparator. In case of a two-level system the sign of the result directly selects the upper or lower switch. If the difference between the two signals is positive the upper switch in the belonging phase is turned on and vice versa. For phase U the voltage u_{UM} is as follows:

$$u_{\mathrm{UM}} = \begin{cases} +U_{\mathrm{DC}}/2 \text{ for } u^*_{\mathrm{U}} > u_{carr} \\ -U_{\mathrm{DC}}/2 \text{ for } u^*_{\mathrm{U}} < u_{carr} \end{cases}$$

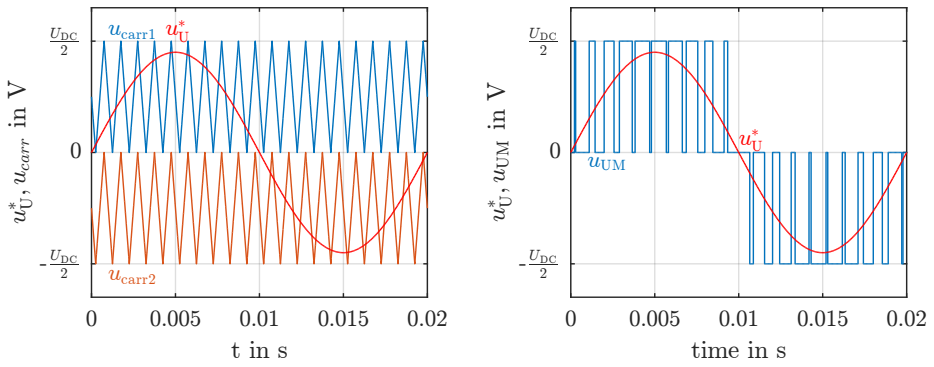
Implementation Effort for Multilevel Systems

When using carrier based PWM with multilevel systems it must be extended. For standard implementation of carrier based PWM for multilevel inverters additional carrier signals are introduced as described in [38, 39]. Figure 3.3a shows a multi carrier signal as it is used for a three-level inverter.

As it can be seen two carrier signals are level shifted to each other with equal phase. The upper carrier u_{carr1} and the lower carrier u_{carr2} are set to a peak to peak voltage of $U_{\mathrm{DC}}/2$. The two carrier signals cover the full output voltage range of the three-level system. Using both carrier signals the three possible output states of a three level inverter can be applied. The conditions for the selection of the output states are

$$u_{\mathrm{UM}} = \begin{cases} +U_{\mathrm{DC}}/2 \text{ for } u^*_{\mathrm{U}} > u_{carr1} \\ 0\ V \text{ for } u^*_{\mathrm{U}} \leq u_{carr1} \text{ and } u^*_{\mathrm{U}} \geq u_{carr2} \\ -U_{\mathrm{DC}}/2 \text{ for } u^*_{\mathrm{U}} < u_{carr2} \end{cases}$$

Figure 3.3b shows the generated three-level output voltage of the two carrier



(a) Three-level carrier signal (b) Generated output voltage

Figure 3.3: Single-phase carrier based PWM and output voltage for a three-level inverter

signals and the set voltage u_U^*. When considering multilevel converters with higher level counts $n-1$ carrier signals are necessary to cover all available switching positions. In addition, it should be mentioned that the output spectrum can be varied by changing the disposition between the carrier signals as pointed out in [40].

3.1.2 Space Vector Pulse-Width Modulation

The space vector pulse-width modulation (SVPWM) was developed as an alternative to carrier based solutions in the 1980s [41]. Instead of using a modulator for each phase the SVPWM calculates the sequence for all three phases in one step. In today's applications the SVPWM is the most common modulation method for three-phase inverter systems. Similar to the carrier based modulation the SVPWM based methods show a fixed switching frequency. A simplified circuit diagram of the SVPWM controller scheme is shown in Figure 3.4.

Based on the SVPWM, the structure of an indirect control system to generate the set voltage $u_{\alpha\beta}^*$ will be briefly described. The three-phase current i_{UVW} is transformed into the dq system using the Park transformation by applying Equation 3.7 [42]. The dq frame is also known as rotating reference frame (RRF) and uses the angle θ which corresponds to the phase of the

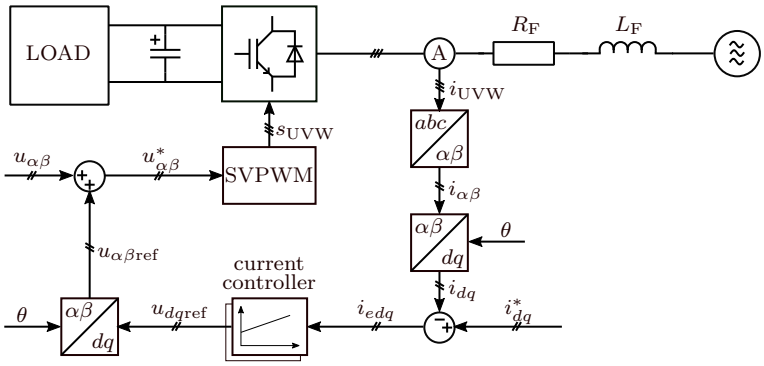


Figure 3.4: Controller scheme of SVPWM with current control circuit

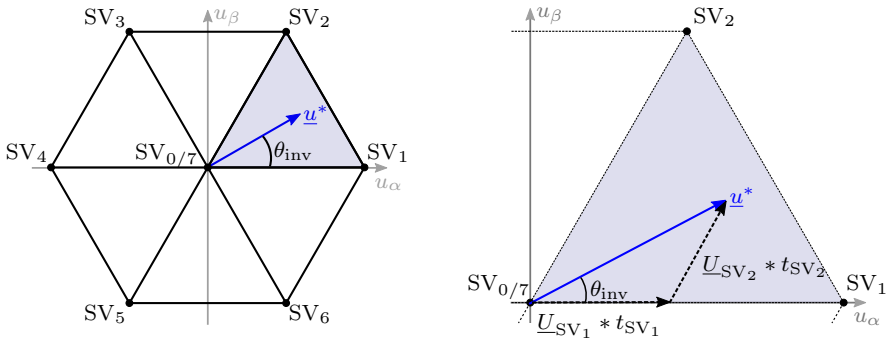
grid voltage.

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \boldsymbol{T}_{dq} \cdot \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \cdot \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{3.1}$$

Having the DC-components i_d and i_q in the dq-system standard linear controllers (e.g. PI) can be used. For grid connected applications, the current component i_d corresponds to the active power and i_q to the reactive power. The set current i_d is normally generated by an additional linear controller to control the DC-link voltage. To guarantee a unity power factor the component i_q is normally set to zero. The linear controller defines the stability and dynamic properties of the whole control system, therefore, the main task when implementing a SVPWM is the correct setting of this controller. The generated voltage in dq-coordinates is transformed into $u_{\alpha\beta\text{ref}}$ by using the reverse Clarke transformation. This voltage is added to the actual grid voltage $u_{\alpha\beta}$ which results in the set voltage $u^*_{\alpha\beta}$ used for the modulator.

The inner current control loop presented in Figure 3.4 can also be used with the previous described carrier based PWM. The only difference is that the set voltage $u^*_{\alpha\beta}$ has to be transformed to a three-phase voltage instead of an $\alpha\beta$ voltage.

The modulator determines one of the six triangular sectors that is used to reproduce the reference voltage as shown in Figure 3.5a. In the case of a two-level system knowing the phase angle θ_{inv} of the set voltage $u^*_{\alpha\beta}$ is sufficient for selecting the correct sector with its three associated space vectors.



(a) SV-diagram of a two-level inverter (b) Space vector combination

Figure 3.5: SVPWM selection of used sector and required space vector combination for reproduction of the set voltage

The highlighted sector defines the three surrounding space vectors which will be used to reproduce the set voltage (Figure 3.5b). The on time duration for each space vector is calculated in a way that the mean voltage value over T_S is equal to the set value by using Equation 3.2.

$$\underline{u}^* = \frac{1}{T_S} \cdot (\underline{U}_{\mathrm{SV}_1} \cdot t_{\mathrm{SV}_1} + \underline{U}_{\mathrm{SV}_2} \cdot t_{\mathrm{SV}_2} + \underline{U}_{\mathrm{SV}_0} \cdot t_{\mathrm{SV}_0}) \tag{3.2}$$

$$T_S = t_{\mathrm{SV}_1} + t_{\mathrm{SV}_2} + t_{\mathrm{SV}_0} \tag{3.3}$$

This calculation procedure is repeated continuously with a fixed sample time T_S by the modulator.

Implementation Effort for Multilevel Systems

Due to the increased complexity and sector number when using multilevel inverters, several methods are presented that are used to simplify the application of SVPWM [43]. One possible approach is to divide the hexagonal multilevel space vector diagram in a set of smaller hexagons that are equal to the SV-diagram of a two-level inverter system [44]. This allows to apply and adopt control methods of two-level inverter systems. As illustrated in Figure 3.6 a three-level space vector diagram can be divided into six two-level SV-diagrams. The set voltage vector is moved to be at the centre point of

the corresponding two-level space vector diagram. Therefore, the set voltage $u^*_{\alpha\beta}$ is the sum of the centre voltage of the chosen hexagonal area $u_{\alpha\beta\mathrm{hex}}$ and the set voltage $u^*_{\alpha\beta\mathrm{hex}}$ from this point.

$$u^*_{\alpha\beta} = u_{\alpha\beta\mathrm{hex}} + u^*_{\alpha\beta\mathrm{hex}} \tag{3.4}$$

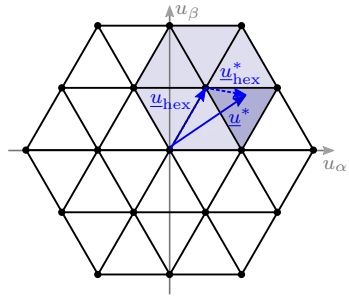


Figure 3.6: Simplified multilevel SVPWM scheme for a three-level inverter

3.2 Direct Control Techniques

Direct controllers try to directly adjust the output current, active and reactive power or flux and torque without an intermediate step [45]. In most cases the principle working behaviour of direct controllers is based on hysteresis limits. A violation leads immediately to a change of the inverter output switching states. This working principle leads to a very fast reaction on current or power steps and other high dynamic system changes like grid faults. Nevertheless, due to their higher requirements on the current measurement and processing power, direct controllers are not widely used. The main advantages of direct control techniques are:

- High dynamic response
- Overcurrent protection
- Load independence
- No need for linear controllers
- No need for modulator

The main disadvantages of these controllers are the variable and, according to the controller type, unsymmetrical switching frequency between the phases and the dependency on the modulation index of the inverter [46]. To prevent damage of the inverter hardware caused by overfrequency, the tolerance band needs to be adapted [47]. The corresponding spread output spectrum complicates the design of grid filters that are necessary to comply with the grid standards in industry applications.

3.2.1 Three-Phase Hysteresis Current Control

The three-phase hysteresis current controller is the most simple form of a direct current controller [45]. A simplified illustration of the controller structure is shown in Figure 3.7. For a two-level inverter system, each phase consists of the current measurement, current error calculation and one independent two-stage comparator (relay). The output switching states are generated independently in each phase by using the calculated three-phase current error $i_{e\mathrm{UVM}}$.

$$i_{e\mathrm{UVM}} = i^{*}_{\mathrm{UVM}} - i_{\mathrm{UVM}} \tag{3.5}$$

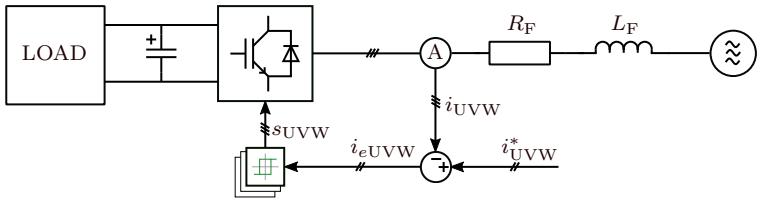


Figure 3.7: Three-phase hysteresis direct current controller scheme

Each relay compares the current error i_{eUVM} with a positive and negative limit $\pm B_{UVM}$, hereinafter named tolerance band. After a violation occurs, the output state changes immediately to reduce the current error in the related phase. As illustrated in Figure 3.8 reaching the positive limit $+B$ indicates that the current error is too high and reaching $-B$ too low. According to the tolerance band violation the upper or lower state is selected. This simple working behaviour results in a very high dynamic reaction speed.

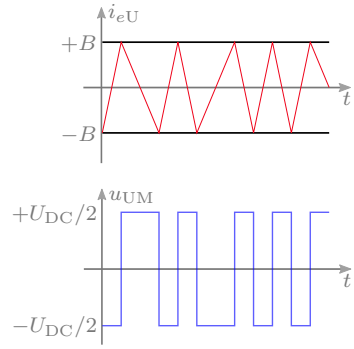


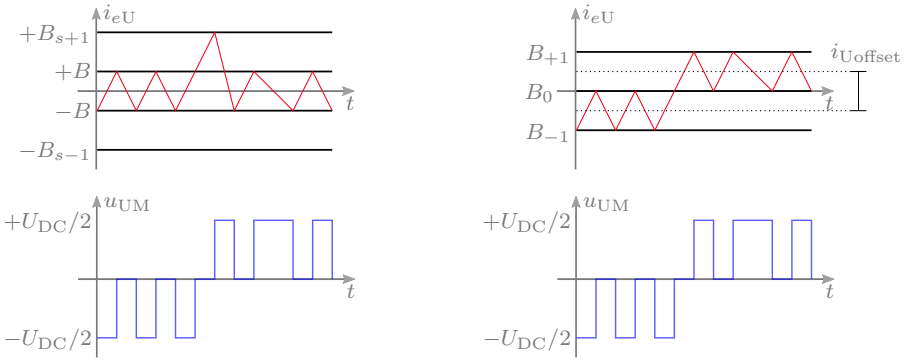
Figure 3.8: Error current and generated output voltage for a two-level inverter in phase U

Due to the individual consideration of each phase and the fact that the dependency of the three phases is neglected, the error currents can exceed the tolerance limits for a short time even though the correct switching state is selected. In this case the current error reduces if also the two other phases switch the correct combination to increase the output voltage against the neutral point in the affected phase. This fact results in a higher switching frequency compared to other direct controllers. The switching frequency also varies in all phases according to changes in the grid. To compensate such an

unintentional working behaviour a switching frequency control which adjusts the border levels has to be applied [48]. Another option to avoid the variable switching frequency over the modulation area is using an equidistant sampling of the hysteresis controller. Hereby the current error is triggered with a fixed sample rate. The sign of the current error decides which switching state is selected next [49].

Implementation Effort for Multilevel Systems

When using the hysteresis controller with multilevel systems, additional tolerance bands are needed [50, 51]. The structure for the tolerance bands can be implemented in two different ways. One with fixed reference to the switching state and the other with a floating reference. In Figure 3.9 both types are shown for a three-level implementation with the three corresponding states +1, 0 and −1. Figure 3.9a shows the floating type with its four bands. The two inner bands are used to control the current with the two states −1 and 0. If the current reaches the upper tolerance band $+B_{s+1}$ both states are incremented by one. The references for inner bands $-B$ and $+B$ are now state 0 and +1. Because of the higher inverter output voltage the current error decreases until it is inside the inner limits. The references changes again when the lower band $-B_{s-1}$ is touched.



(a) Floating tolerance band (b) Fixed reference tolerance band

Figure 3.9: Error current and generated output voltage by different tolerance band types for a three-level inverter in phase U

The fixed reference type as shown in Figure 3.9b needs only three hysteresis bands for controlling a three-level inverter. Compared to the floating

type all three bands are connected to a fixed switching state. The lower to -1, the mid to 0 and the upper to $+1$. The error current remains between the two bands as long the two corresponding switching states can keep the current error inside the limits. This results in a permanent offset of the output current. To avoid this DC-offset in the output current a compensation for the set current is required.

Independent from the chosen type the use of additional tolerance bands leads to an increased current error which decreases the output current quality. The number of tolerance bands rises with higher level count. For the fixed reference type n tolerance bands and for the floating type $2+2\cdot(n-2)$ tolerance bands are required. This rapidly growing number in the case of the floating type is necessary because of the fact that several states need to be skipped immediately in some special operating points.

3.2.2 $\alpha\beta$ Hysteresis Current Control

In contrast to the three-phase hysteresis controller which disregards the phase relationship between the three output voltages and currents, the $\alpha\beta$ hysteresis controller does respect it and uses the $\alpha\beta$ components to control the three-phase currents [47]. Therefore, the relationship $i_\mathrm{U} + i_\mathrm{V} + i_\mathrm{W} = 0$ in a three-wire system is taken into account. Also, the $\alpha\beta$ hysteresis current controller provides the basis for many further developments [52, 53]. A simplified structure of the $\alpha\beta$ control system is shown in Figure 3.10.

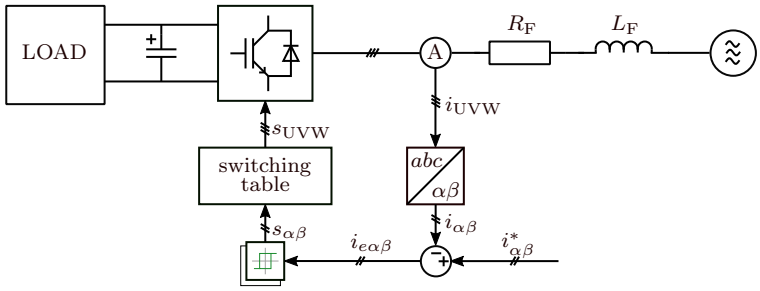


Figure 3.10: $\alpha\beta$ hysteresis direct current controller scheme

The measured three-phase current i_UVW is transformed to the stationary reference frame using the Clarke transformation. Using the set current $i^*_{\alpha\beta}$ the error current can be calculated as follows.

$$i_{e\alpha\beta} = i^*_{\alpha\beta} - i_{\alpha\beta} \tag{3.6}$$

In Figure 3.11 it is shown that the definition of the tolerance band structure is different compared to the three phase hysteresis controller. Since the error current is considered in the $\alpha\beta$ system tolerance limits for each component are introduced resulting in a rectangular tolerance area. This results in four possible error states according to the location of the violation of this area.

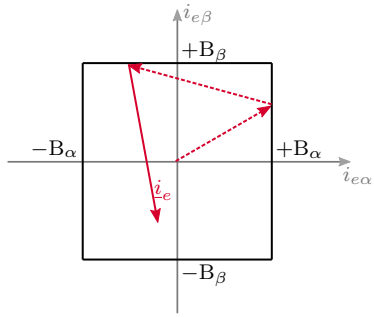


Figure 3.11: Rectangular tolerance area for a $\alpha\beta$ hysteresis direct current control

From Figure 3.11 it is obvious that four different switching states are sufficient for controlling the current error within the tolerance area. However, the two-level inverter has eight different switching states. To cover all switching states of a two-level inverter a one stage comparator is, therefore, no longer sufficient for selecting the best possible switching state. Therefore, the α comparator is designed to consider four stages (++, +, -, - -) and the β comparator is designed to consider three stages (+, 0, -). This stages-count corresponds to the number of different α and β voltage levels in the SV-diagram. To select the space vector being able to reduce the current error a switching table is applied. The corresponding switching table when using a two-level system is shown in Table 3.1.

As it can be seen, that regardless which four $\alpha\beta$ states in the table (2x2 field) are selected, one state occurs always twice. This fact results in a under determined system with three space vectors for four current error states leading to possibly short time tolerance band violations. Another disadvantage is that the $\alpha\beta$ hysteresis current control generates unsymmetrical

Table 3.1: $\alpha\beta$ hysteresis control switching table

		α-state			
		+ +	+	-	- -
β-state	+	SV_5	SV_5	SV_6	SV_6
	0	SV_4	$SV_{0/7}$	$SV_{0/7}$	SV_1
	-	SV_3	SV_3	SV_2	SV_2

switching frequencies between the phases. This occurs because of the direct relation between the α component and phase U. As a result of this relation the switching frequency in phase U is significantly higher compared to the phases V and W.

Implementation Effort for Multilevel Systems

The principle structure of the $\alpha\beta$ hysteresis controller for multilevel systems is similar to the three-phase hysteresis controller but needs to be adapted. According to the additionally available voltage levels in the α and β direction extra tolerance bands need to be applied to the control system. When using a three-level system nine α stages and five β stages are necessary. Considering a five-level application the number of stages increases for α to 17 and for β to nine. The number of switching tables with the corresponding switching states also increases to 45 for three- and 153 for five-level inverter systems. Redundant space vectors can be used for DC-link balancing by adding a further input argument to the switching table. This additionally increases the necessary number of switching states.

3.2.3 Switched Diamond Hysteresis Current Control

The so called Switched Diamond Hysteresis Current Control (SDHC) is based on the $\alpha\beta$ hysteresis controller and was presented in 2010 as direct current control method for electric drives and for grid applications [54, 55]. The SDHC method solves some disadvantages of the standard $\alpha\beta$-concept including the unequal switching frequency in the three phases and the temporary violation of tolerance bands due to the undetermined switching tables.

The basic structure of the SDHC algorithm is shown in Figure 3.12.

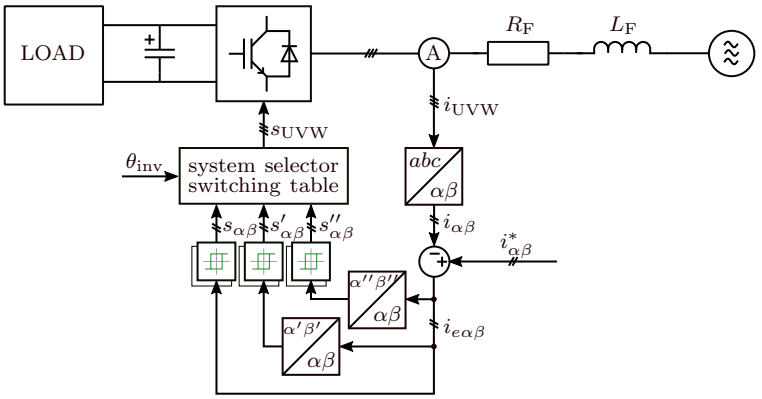
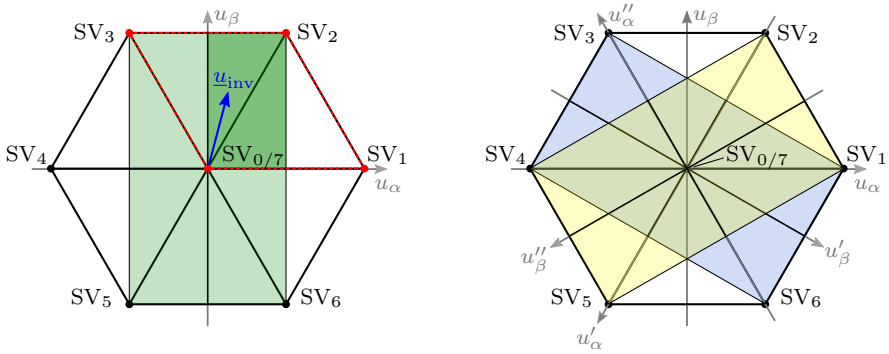


Figure 3.12: Switched Diamond Hysteresis controller scheme

To overcome the disadvantages of the standard $\alpha\beta$ controller, two additional coordinate systems are introduced as described in [36]. The new systems are based on the Clarke transformation but with the α-axis being oriented along phase W and phase V instead along phase U. The coordinate system which is orientated to phase W is named $\alpha'\beta'$ and the for phase V $\alpha''\beta''$. The components for the two additional coordinate systems can be calculated by

$$\begin{bmatrix} u_{\alpha'} \\ u_{\beta'} \\ u_{\alpha''} \\ u_{\beta''} \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} -\frac{1}{2} & -\frac{1}{2} & 1 \\ \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ -\frac{1}{2} & 1 & -\frac{1}{2} \\ -\frac{\sqrt{3}}{2} & 0 & \frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} u_U \\ u_V \\ u_W \end{bmatrix} \tag{3.7}$$

The current is controlled by an α and β tolerance band. However, the sectors are predefined as rectangular areas. The four sectors in the standard $\alpha\beta$-system and the average inverter output voltage $\underline{u}_{inv}$ which is located in the upper right sector are shown Figure 3.13a. The used space vectors for this sector are shown in Table 3.2 and defined by the corners of the eponymous diamond around the sector. This table leads to one explicit space vector for each possible current error direction. The only problem with this method is that the rectangular areas do not cover the whole area of the SV-diagram as it can be seen in Figure 3.13a. In the white triangular areas the specified space vectors cannot control the current correctly.



(a) Sectors in standard $\alpha\beta$ coordinate system

(b) Sectors in rotated $\alpha'\beta'$- and $\alpha''\beta''$ coordinate system

Figure 3.13: Structure and orientation of preselecting sectors for the SDHC method in all three used coordinate systems

To overcome this problem the two additional coordinate systems are used. The respective four sectors of the $\alpha'\beta'$ and $\alpha''\beta''$ system are shown in Figure 3.13b. It can be seen that the whole area of the SV-diagram is covered when using all three coordinate systems. As selection criterion for the correct coordinate system in case of a two-level inverter the phase angle θ_{inv} of the average inverter output voltage $\underline{u}_{\text{inv}}$ is used. The applied angular ranges for the standard $\alpha\beta$-system are 60°-120° and 240°-300°, for the $\alpha'\beta'$-system 120°-180° and 300°-360° and for the $\alpha''\beta''$-system 0°-60° and 180°-240°. Thus the angular areas correspond to the sections in the SV-diagram where the related rectangular sectors cover the entire area. Due to the overlapping

Table 3.2: SDHC switching table for highlighted rectangular sector in Figure 3.13

		α-state	
		+	-
β-state	+	$SV_{0/7}$	SV_1
	-	SV_3	SV_2

structure of the sectors in the different coordinate systems the pre-selection process with the phase angle is sufficient for two-level inverters. Therefore, no additional tolerance bands are needed in normal operation under standard grid conditions. They are only required for high dynamic reactions. The rotation of the coordinate systems leads to a symmetrical switching frequency.

The previously introduced three coordinate systems have an impact on the tolerance area. Since the used rectangular sectors rotate, the current error and thus the tolerance band boundaries need to be evaluated and transformed into the corresponding system. The resulting tolerance band structures are shown in Figure 3.14.

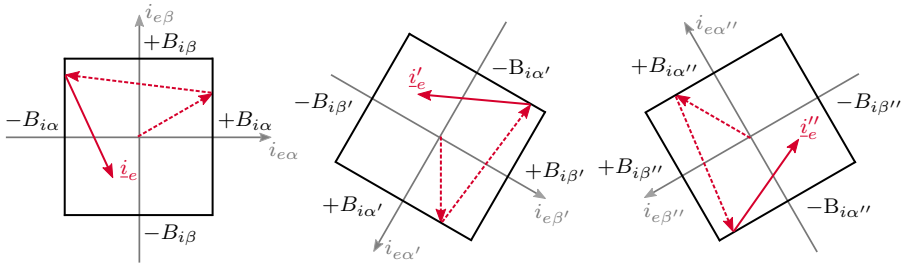


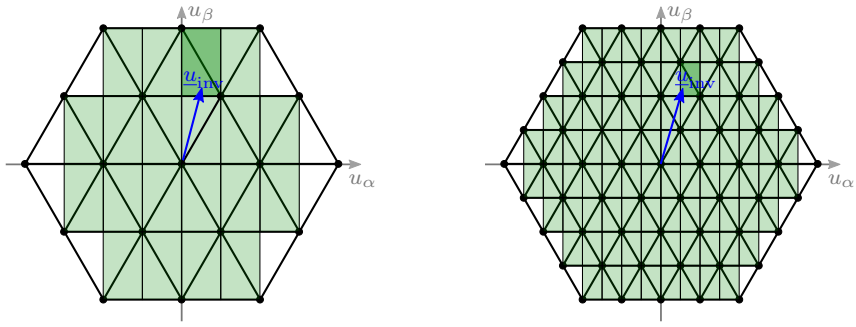
Figure 3.14: Structure and orientation of current error and tolerance bands for the SDHC method in all three used coordinate systems

The rotation of the current tolerance area for the different coordinate systems results in a star-shaped band when considered over one grid period. This leads effectively to constant variation of the tolerance size when the current error is observed in the standard $\alpha\beta$-system or measured in the three-phase system.

Implementation Effort for Multilevel Systems

The SDHC method for a three-level NPC inverter system was presented in [56]. As illustrated in Figure 3.15a for one coordinate system ($\alpha\beta$) the number of rectangular sectors increases from 4 to 20 per coordinate system, i.e. in total 60 switching tables with four states each. The angular ranges needed to select the correct coordinate system are identical to the two-level

system as previously defined. As one can see the phase angle θ_{inv} of the average inverter output voltage $\underline{u}_{\text{inv}}$ is no longer sufficient to precisely detect the correct sector. Therefore, both the angle and the amplitude of $\underline{u}_{\text{inv}}$ are necessary to identify the correct sector and to trigger the sector changes within a coordinate system.



(a) Three-level SDHC (b) Five-level SDHC

Figure 3.15: Structure and orientation of preselecting sectors for the SDHC method in standard $\alpha\beta$ coordinate system for a three- and five-level inverter

When investigating the SDHC method for level counts $n > 3$ the number of switching tables increases significantly. A SV-diagram of a five-level inverter system is shown in Figure 3.15b. The number of sectors and switching tables that need to be set up for a SDHC controlled n-level inverter can be calculated using the following expression.

$$\text{Number of switching tables} = 12 \cdot ((n-1)^2 + \frac{(n-1)}{2}) \tag{3.8}$$

It can be seen from Figure 3.15b and Equation 3.8 that the exact selection of the correct rectangular sector becomes more complicated with an increased level count. Therefore, a strategy that detects all sector transitions very accurately is mandatory.

3.2.4 Direct Power Control

The so called Direct Power Control (DPC) is based on the $\alpha\beta$-system and was first introduced in [57]. It is described as a variation of the Direct Torque Control (DTC) which is used to control torque and flux in electrical machines for electric drives [58]. Compared to the previously presented controller types, this method doesn't use the inverter error currents $i_{e\mathrm{UVW}}$ or $i_{e\alpha\beta}$ to trigger a switching event when touching the tolerance bands. Instead new output states are selected when the error of the active power p_e and reactive power q_e of the system exceed the tolerance limits set by the controller. This leads to the advantage that no superimposed active and reactive power controller, as typically used in most grid applications, is necessary any more. A simplified circuit diagram of the DPC is illustrated in Figure 3.16.

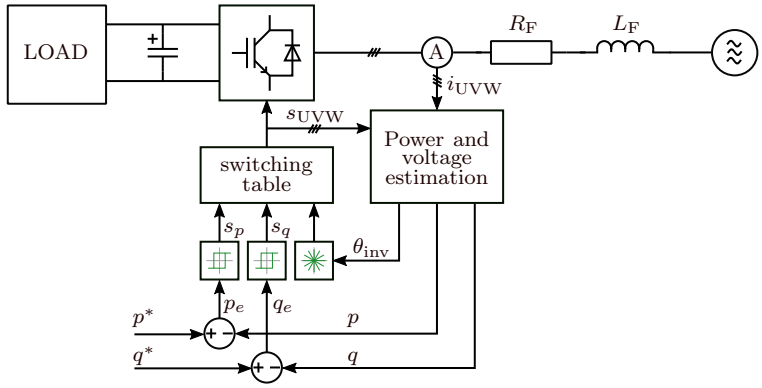


Figure 3.16: Direct Power Control scheme

Calculating the instantaneous active and reactive power requires the currents and voltages of the grid. Using the current and voltage within the stationary reference frame the active and reactive power can be calculated by

$$p = \frac{3}{2} \cdot (u_\alpha \cdot i_\alpha + u_\beta \cdot i_\beta) \tag{3.9}$$

$$q = \frac{3}{2} \cdot (u_\alpha \cdot i_\beta - u_\beta \cdot i_\alpha) \tag{3.10}$$

In standard operation the reference value for the active power p^* is controlled by the DC-link voltage controller and the reference value for the reactive

power q^* is set to zero for a unity power factor. To avoid using additional tolerance bands the DPC takes the phase angle θ_{inv} to pre-select the correct sector. Considering a two-level inverter system the SV-diagram is divided into twelve 30° sectors. For each sector a switching table is implemented containing four different switching states to manipulate the active and reactive power in any direction. To overcome the disadvantage of variable switching frequency the working principle of the DPC can be combined with indirect controllers generating a voltage set-point for an SVPWM-DPC [59]. The Virtual-Flux Direct Power Control (VF-DPC), an advancement of the DPC using the virtual-flux approach, requires lower sampling times and is easier to implement [14]. This algorithm can be modified to generate sinusoidal and balanced output currents even under unsymmetrical grid conditions. The equations to calculate the active and reactive power using the virtual-flux are defined to be

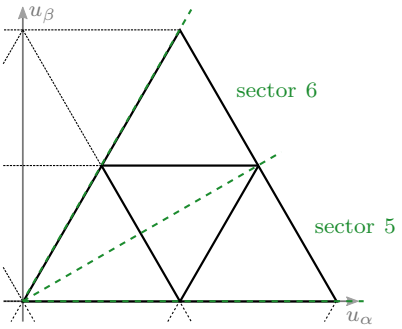
$$p = \frac{3}{2} \cdot \omega \cdot (\psi_\alpha \cdot i_\beta - \psi_\beta \cdot i_\alpha) \tag{3.11}$$

$$q = \frac{3}{2} \cdot \omega \cdot (\psi_\alpha \cdot i_\alpha + \psi_\beta \cdot i_\beta) \tag{3.12}$$

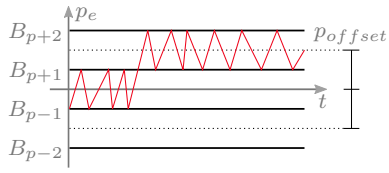
Implementation Effort for Multilevel Systems

The VF-DPC for a three-level NPC and a five-level ANPC inverter was investigated in [60, 61]. Within two-level systems the DPC uses only one single positive and one negative tolerance band for active and reactive power. When adapting the DPC to three-level systems additional tolerance bands for the active and reactive power are introduced. Those additional tolerance bands represent the change between the inner and outer hexagon of the three-level SV-diagram. An illustration of the SV-diagram with the angular sectors and the tolerance band for the active power is shown in Figure 3.17. For the reactive power a three-stage comparator is sufficient. In order to prevent a set-point deviation an offset correction of active and reactive power to compensate the additional tolerance band areas is used. In contrast to the previously presented direct control methods the phase angle θ_{inv} is, furthermore, sufficient for selecting the correct sector.

Figure 3.18 shows the SV-diagram of a VF-DPC controlled five-level system. As it can be seen in Figure 3.18a the angular division changes from 12 sectors to 24 sectors. While the sector subdivision for a two- and three-level inverter system is the same, the size of a sector for a five-level inverter



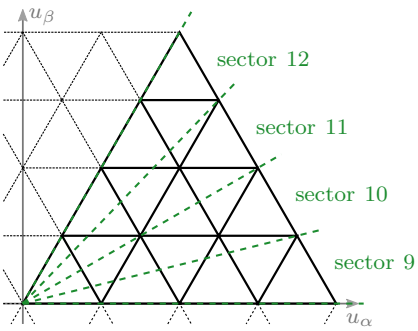
(a) Detail of sector subdivision



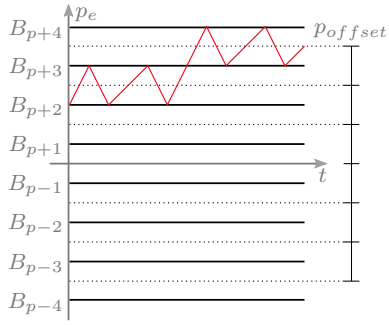
(b) Tolerance band structur of active power

Figure 3.17: Structure of preselecting sectors and active power tolerance bands of VF-DPC for a three-level NPC

system is 15° which creates 24 sectors. To cover all switching states used within the sector an eight-stage comparator for the active power is introduced (Figure 3.18b). The tolerance band structure for the reactive power is a three-stage comparator, the same as for the three-level system. This fact allows that only the neighbouring space vectors are used for control [61].



(a) Detail of sector subdivision



(b) Tolerance band structure of active power

Figure 3.18: Structure of preselecting sectors and active power tolerance bands of VF-DPC for a five-level ANPC

As long as the modulation index remains constant the power error stays between the same two active power tolerance bands. For level counts greater than five the number of angular sector and tolerance bands as well as switching tables increases.

3.2.5 Scalar Hysteresis Control

The so called Scalar Hysteresis Controller (SHC) was presented in [62, 63] and is the base for the presented work. The structure of the SHC is shown in Figure 3.19. Compared to other direct controllers, the SHC controls the current in the $\alpha\beta$-system to remain inside a circular tolerance area around the current set point. It does not need predetermined switching tables for space vector selection. After a tolerance band violation the correct space vector being able to reduce the current error is calculated and not taken from any switching table.

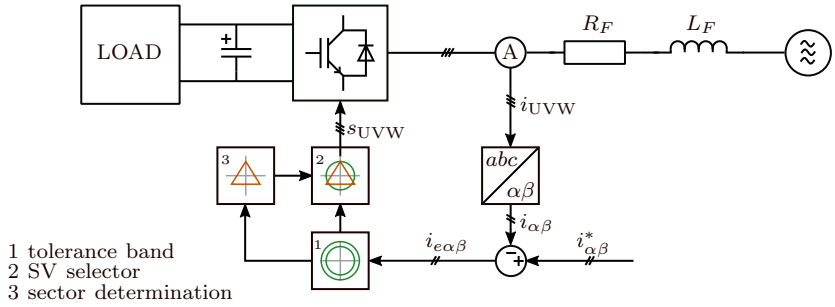


Figure 3.19: Scalar Hysteresis controller scheme

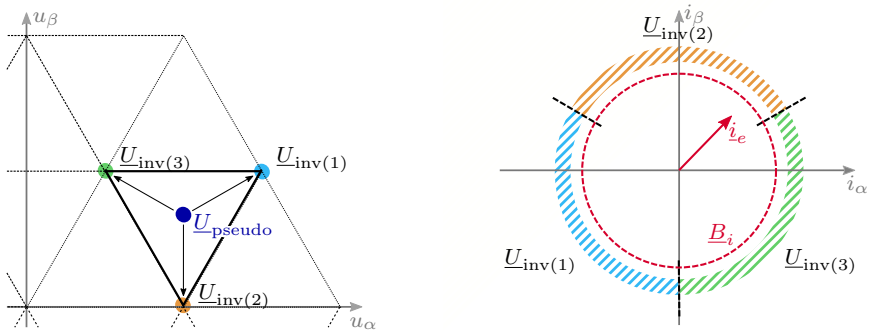
The triangular sector geometry used by the SHC is the smallest possible sector size in a SV-diagram. This sector geometry is independent from the used topology and level count. To control the current to stay within the circular area, only those three space vectors are used that directly surround the average inverter output voltage. Another difference compared to other direct controllers is, that the SHC does not use separate tolerance bands for α and β current error. For this purpose, the two current errors $i_{e\alpha}$ and $i_{e\beta}$ are considered in a combined way and the circular tolerance band is introduced.

$$i_e^2 = i_\alpha^2 + i_\beta^2 \tag{3.13}$$

Through the rotational symmetry of the triangular sector geometry and the circular tolerance band the switching frequency of all phases is equal under standard grid conditions. The mode of operation of the SHC, especially the sector and space vector selection procedure, is briefly explained below.

Inner Tolerance Band

The inner tolerance band that is used to select the current error reducing space vector is described using the three-level SV-diagram shown in Figure 3.20a. In the case shown, an arbitrary triangular sector is chosen and no additional informations about the voltage position are available. Therefore, the midpoint of the active triangle is selected as an auxiliary ("pseudo") voltage. For simplification and midpoint definition a new coordinate transformation is applied in the SV-diagram [64]. The basic functionality of this coordinate transformation will be described in more detail in Chapter 4.4.1.



(a) Sector subdivision

(b) Inner tolerance band

Figure 3.20: SHC selection mechanism and structure of inner tolerance band with highlighted space vector sections

The centre point of the selected triangle $\underline{U}_{\mathrm{pseudo}}$ serves as a basis for the calculation of the best error-reducing space vector. The three voltage vectors $\underline{U}_{\mathrm{L_F}(k)}$ to the corner points of the surrounding triangle can be calculated by

$$\underline{U}_{\mathrm{L_F}(k)} = \underline{U}_{\mathrm{inv}(k)} - \underline{U}_{\mathrm{pseudo}}, \qquad k = 1, 2, 3 \tag{3.14}$$

The calculated voltages $\underline{U}_{L_F(k)}$ correspond to the voltage at the filter inductance of the inverter system. The different directions of the three voltages

also represent the impact of the three space vectors on the inverter output current. The aim is now, to choose that space vector which minimizes the current error best. Therefore, the one space vector $\underline{U}_{\mathrm{inv}(k)}$ out of three is selected for which the angle between $\underline{U}_{\mathrm{L_F}(k)}$ and the error current $\underline{i}_e$ is best opposing. A computational efficient possibility to determine k is calculating the complex scalar product.

$$\langle \underline{U}_{L_F(k)}, \underline{i}_{\mathrm{e}} \rangle = \underline{U}_{L_F(k)} \cdot \bar{\underline{i}}_{\mathrm{e}} \tag{3.15}$$

where $\bar{\underline{i}}_{\mathrm{e}}$ is the complex conjugate of the current error $\underline{i}_{\mathrm{e}}$. This equation can be simplified according to Equation 3.16 when only the real part of the complex scalar product is calculated [63].

$$k_{\mathrm{opt}} = \underset{k\in\{1,2,3\}}{\arg\min} \left(\mathrm{Re}\{\underline{U}_{\mathrm{L_F}(k)} \cdot \bar{\underline{i}}_{\mathrm{e}}\} \right). \tag{3.16}$$

Due to this online calculation procedure, the SHC method has similarities to a predictive controller, however, with the difference, that no system model or other system parameters are used. In order to avoid complex geometrical calculation effort to detect a violation of the circular tolerance band, the absolute squared value of the current error $|\underline{i}_e|^2$ is used as trigger event.

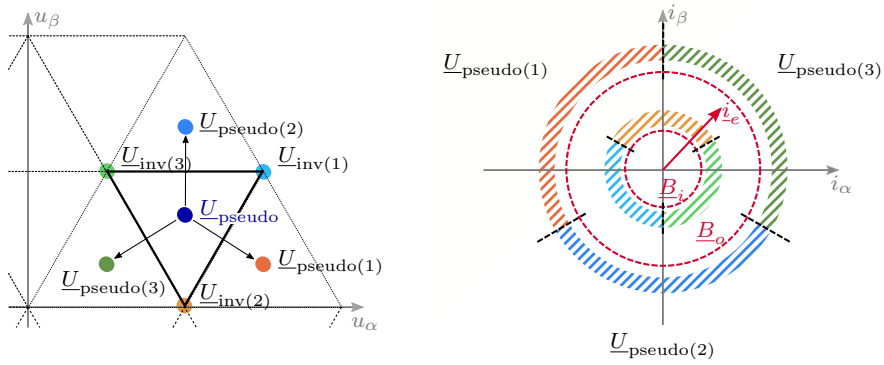
The geometrical representation of the proposed concept and the SV-areas are shown in Figure 3.20b. The fixed positions of the mid- and corner points of the triangle yield to three circular segments with 120° each. This division represents the selection area for the three surrounding space vectors. From Figure 3.20 it is apparent that the corresponding space vector is always on the opposite side of the current error tolerance band area.

Outer Tolerance Band

In the previous part the working behaviour of the SHC within a sector was presented. As the standard SHC configuration uses no information about the voltage position in the SV-diagram, a seeking algorithm is introduced to determine the correct triangular sector necessary to control the current. Therefore, a second tolerance band $\underline{B}_o$ is introduced to trigger the triangle selection process (Equation 3.17). For this purpose the midpoints $\underline{U}_{\mathrm{pseudo}(k)}$ of the three adjoining triangles are considered within the calculation. This leads to a similar expression as Equation 3.16.

$$k_{\text{opt}} = \underset{k\in\{1,2,3\}}{\arg\min} \left(\text{Re}\{\underline{U}_{\text{pseudo}(k)} \cdot \bar{\underline{i}}_{\text{e}}\} \right). \tag{3.17}$$

Compared to Figure 3.20a the centre points of the surrounding triangular sectors $\underline{U}_{\text{pseudo}(1)}$, $\underline{U}_{\text{pseudo}(1)}$ and $\underline{U}_{\text{pseudo}(3)}$ are additionally highlighted in Figure 3.21a. The tolerance band structure of the inner and outer band is shown in Figure 3.21b.



(a) Sector subdivision (b) Tolerance bands structure

Figure 3.21: SHC selection mechanism of outer tolerance band

If the selected triangular sector is incorrect, the SHC is not able any more to control the output current to stay inside the inner tolerance band $\underline{B}_i$ by applying only the three adjacent space vectors of the triangular sector. Consequently when switching the wrong space vectors the current error exceeds the inner tolerance band. As soon as the outer tolerance band $\underline{B}_o$ is violated, a sector change according to Equation 3.17 and Figure 3.21b is performed. After the sector has changed three new space vectors from that new sector are used to control the current. As shown in Figure 3.21b the outer tolerance band is divided in three 120° segments for geometry reason.

To avoid additional outer tolerance bands when using multilevel inverters or for higher dynamic reactions the outer tolerance band functionality of the SHC is designed in a way that it can trigger multiple events. This approach enables the SHC for an arbitrary level count of the inverter system. Like any other hysteresis controller exceeding the inner tolerance band area is mandatory for switching sectors. Thus, when using outer tolerance bands the current error is temporarily too high, leading to an increased output current distortion.

3.3 Predictive Control

Predictive controllers try to forecasts the course of the current and to choose the best possible switching state for a certain purpose. For this, the controller needs exact information of all load and system parameters to set up a system model. Originated from the selection process predictive controllers are divided into several substructures [65].

The hysteresis band based predictive control tries to control the current within a tolerance band [58, 66]. Instead of using predefined switching tables for state selection the predictive controller calculates the possible current course for all available output states and compares it with the future set current location. Normally the state with the smallest deviation and thus the longest on period without touching the tolerance band is selected. This procedure results in a minimum switching frequency of the inverter. Figure 3.22 illustrates the tolerance band area and the possible directions of all available space vectors of a two-level inverter.

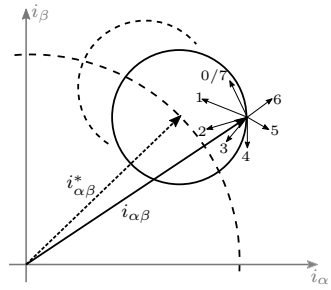


Figure 3.22: Hysteresis based predictive controller scheme

Model predictive controllers (MPC) calculating not only one next output state of the inverter, but predict multiple time steps into the future [65]. By using fixed time steps the method realizes a fixed switching frequency. The limiting factor of this type is the accuracy of the model parameters and the computational effort of the system that grows exponentially with the number of future switching steps. A simplified structure of a model predictive controller is shown in Figure 3.23. The task of the predictive model of the system is to calculate the current course for the next time steps.

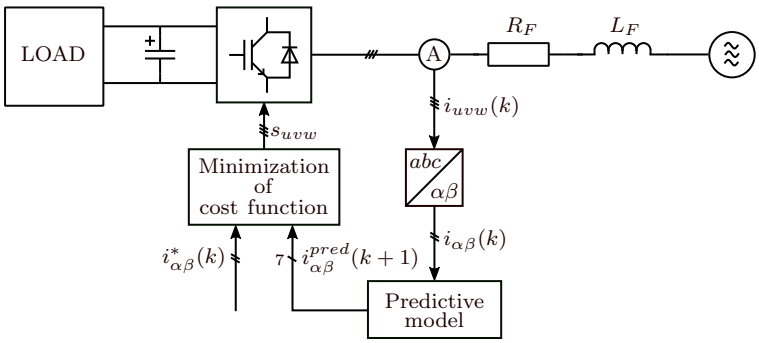


Figure 3.23: Model based predictive controller scheme

The major part of the MPC is the cost function which defines the aim of the control. An example of a cost function for controlling the grid current is

$$g = \left|i^*_\alpha - i^{pred}_\alpha\right| + \left|i^*_\beta - i^{pred}_\beta\right| \tag{3.18}$$

where i^*_α, i^*_β are the reference values and i^{pred}_α, i^{pred}_β are the predicted values [67]. The best result for the controller would be zero current error after the used time step. Therefore, the state which minimizes g is selected and switched to the output. Based on this equation the controller can select a sequence of switching states for several time steps in future without reaching a tolerance band. The cost function is not limited to control currents. To control active and reactive power in grid applications the cost function can be extended as predictive power controller resulting in [68]:

$$g = \left|Q^* - Q^{pred}\right| + \left|P^* - P^{pred}\right| \tag{3.19}$$

where Q^*, P^* are the reference and Q^{pred}, P^{pred} are the predicted power values. Both cost functions can thereby be optionally extended to fulfil additional control properties like switching losses. When several control factors need to be considered weighting factors are introduced.

To sum up, predictive controllers have the following advantages:

- Simple handling
- No linear controllers or modulators are needed
- Non-linearities can be modelled and taken into account

The main disadvantage is that an exact knowledge of all system parameters for setting up the model is required. Differences between model and reality could impair the stationary and dynamic behaviour of the controller. Furthermore, the increased computational effort depends strongly on the number of future steps that need to be considered.

Implementation Effort for Multilevel Systems

Predictive controllers for multilevel systems are part of intensive research [69, 70]. The main challenge is the dramatic rise of possible switching states to n^3 compared to the 2^3 for the two-level inverter. Thereby the required computational power increases even faster. Especially for online calculation of the current course several steps in the future would lead to an exponential growth of switching possibilities. To reduce the calculation effort different simplification strategies for multilevel application are considered. One possibility is a heuristic pre-selection of relevant space vectors like using only the closest ones to the actual sector [71]. Another method is an extrapolation of additional future current steps instead of an exact calculation of each state to save computational resources. Additional to the high count of switching possibilities further control task must be implemented in the cost function which complicates the setup. One of the main parts that must be added to the cost function is thereby the DC-link balancing which is necessary in most multilevel applications.

3.4 Summary

The previous chapter showed an overview of indirect, direct and predictive control methods and the corresponding advantages and disadvantages. The necessary extensions of direct controllers for multilevel inverter application were explained. Almost all methods show that the adaptation for higher levels results in a significant increase of complexity. To detect the best possible switching state in multilevel inverter systems the following approaches are used in direct controlled systems.

- Introduction of additional hysteresis bands for selection of the best matching state. However this results in rising current deviation with higher level count.
- Simplification of the SV-diagram by its subdivision in angular areas using the detected phase angle for pre-selection. Combination with multi-stage hysteresis bands to subdivide the sector according the level count.
- Combination of hysteresis bands with exact sector pre-selection using the voltage information. Count of switching tables for the defined sectors increases rapidly with higher level count.

Chapter 4

Feed Forward Sector Control

4.1 Problem Statement

As the previous chapter has shown, the effort for selecting the correct sector in the SV-diagram increases significantly when using multilevel inverters. For this reason, a concept for detecting the correct sector has to be developed. The basis for the controller concept for grid connected multilevel inverter systems presented in the following sections is the SHC algorithm which was introduced in Chapter 3.2.5. The simplified structure of this control method is shown in Figure 4.1.

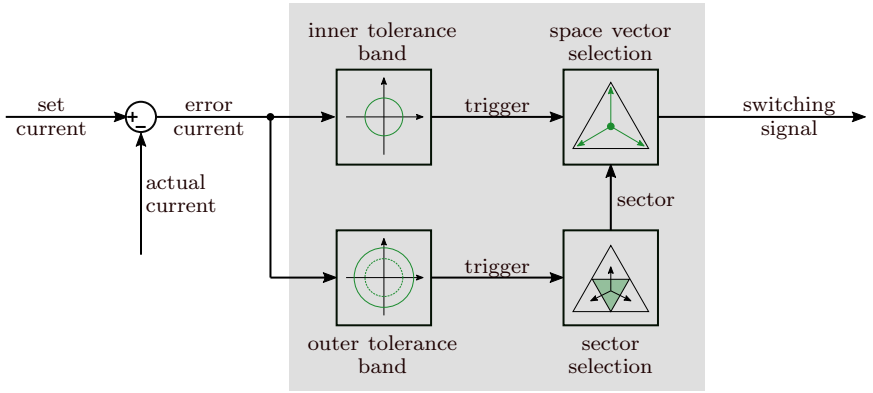


Figure 4.1: Simplified structure of scalar hysteresis controller (SHC)

In the standard configuration, this direct current controller has an inner $\underline{B}_i$ and an outer tolerance band $\underline{B}_o$ and the advantage that it does not require switching tables for the individual sectors in the SV-diagram. However, the additional outer tolerance band is mandatory to change the triangular sec-

tors, whereby the error current increases at each change for a short time. Considering a two-level inverter system, six sector changes are necessary, when using multilevel inverters the number of required sector changes increases significantly. This working behaviour leads to increased harmonic distortion in the output current.

The aim of the proposed concept is to avoid the need of an outer tolerance band in steady state conditions by using a new intelligent feed forward sector control system. Considering a two-level inverter SV-diagram a feed forward control using the phase angle θ_{inv} of the average inverter output voltage is able to perform this task in a simple way. Nevertheless, the demands for a correct sector selection process increase with the number of levels. For $n \geq 3$ the quadratically increasing number of triangular sectors leads to insufficient sector selection when only the phase angle θ_{inv} is used. Thus, for the precise feed forward control the exact knowledge of the phase angle and amplitude of the average inverter output voltage including the harmonic components is necessary [72]. If only the fundamental voltage is used the harmonic components would negatively effect the feed forward control in standard grid applications. In case of indirect control methods, the feed forward voltage would be the input signal for the modulator. Since the SHC controls the current directly it does not provide information about its selected average output voltage. This voltage must be generated in a proper way. To achieve this the proposed feed forward sector control has to meet the following requirements:

- In phase detection of the average inverter output voltage $\underline{u}_{\text{inv}}$ for feed forward sector control.
- Detection of harmonic voltage components to improve the controller performance under harmonic distortions within the grid (optional).
- A simple derivation of the triangular sectors surrounding the detected inverter output voltage.
- Additional use of the detected inverter output voltage for a higher-level control, e.g. generation of set current via a power control

4.2 Voltage Synchronization Methods

Most of the synchronization concepts presented in literature have the aim to detect the fundamental grid voltage, phase angle and grid frequency as accurately as possible and to filter all other possible interferences [73]. A good synchronization system should provide the following features [74]:

- distortion rejection capability and noise immunity
- frequency adaptivity
- phase angle adaptivity
- voltage unbalance robustness
- highly dynamic and accurate
- structural simplicity
- low computational effort

Even if the average inverter output voltage is not equal to the fundamental grid voltage, the requirements are almost identical. For example, informations about harmonic voltage distortions and unbalanced voltages are needed by the proposed feed forward sector control.

Nowadays phase locked loop (PLL) structures are state of the art for grid connected inverters [75]. Basic components of a PLL are the phase detector, a low-pass filter for noise suppression and a voltage-controlled oscillator (VCO) to generate the phase signal. For three-phase inverter systems the synchronous reference frame phase locked loop (SRF-PLL) is most common [76]. The basic structure of this type is shown in Figure 4.2.

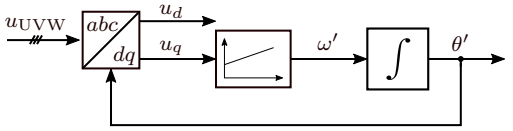


Figure 4.2: Circuit diagram of SRF-PLL

To implement the SRF-PLL the three-phase voltage u_{UVW} is transformed into the dq-system using the Park transformation. The PI-controller regulates the q-component of the grid voltage to zero. Therefore, the output of the controller is related to the detected angular frequency ω' of the input voltage. To generate the estimated phase signal of the grid an integrator

is used. If the phase θ' is locked, the calculated q-component of the dq-transformation is zero and the d-component is equal to the actual amplitude of the grid voltage. The limitations when using the SRF-PLL synchronization method under unbalanced grid conditions leads to the development of several improved PLL schemes like the decoupled double synchronous reference frame PLL (DDSRF-PLL) or the enhanced PLL (EPLL) [77, 78]. Further possibilities to detect grid informations are the zero-crossing detection method or open loop structures like low-pass filtering [79]. When using a low-pass filter, an exact reproduction of the average output voltage of the inverter would be possible. The disadvantage of these filter-based methods is the time delay between the input and the output signal, which needs to be compensated.

4.2.1 Second Order Generalized Integrator

A promising synchronization method that meets the requirements is an adaptive filter structure based on a second order generalized integrator (SOGI) which was presented in [80]. The structure of the SOGI band-pass (SOGI-BP) circuit is shown in Figure 4.3.

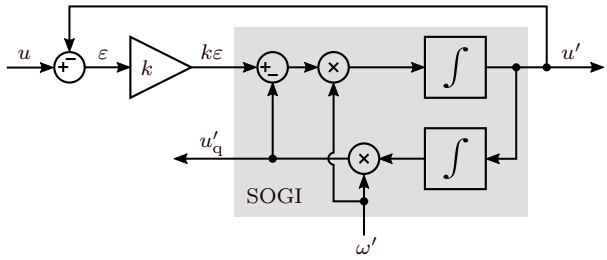


Figure 4.3: SOGI band-pass circuit

The circuit of the SOGI band-pass consists of two integrators, three multipliers and two adders. The inner gray marked area represents the SOGI circuit and has the following transfer function:

$$G_{\mathrm{SOGI}}(s) = \frac{u'}{k\varepsilon}(s) = \frac{\omega' s}{s^2 + \omega'^2} \tag{4.1}$$

The working principle of the SOGI circuit can be interpreted as an application of the so-called internal model principle [81, 82]. The literature states

that the input signal to a subsystem which has poles with non-negative real part cannot contain signal parts corresponding to those poles. This is valid in stationary operation provided that the overall system is stable. In case of the SOGI band-pass circuit in Figure 4.3 the gray SOGI circuit represents a subsystem with the poles $\pm j\omega'$. Consequently, the signal $k\varepsilon$ will no longer contain any oscillations with the angular frequency ω' after initial transients have faded. This implies, however, that the output signal u' compensates all signal components with the angular frequency ω' in the input signal u. As a result the overall structure of the SOGI band-pass in Figure 4.3 observes sinusoidal oscillations at ω' in u with correct amplitude and without phase shift. The resulting transfer function for the first output u' of the adaptive SOGI based band-pass is

$$G_{\mathrm{SOGI-BP}}(s) = \frac{u'}{u}(s) = \frac{k\omega' s}{s^2 + k\omega' s + \omega'^2} \tag{4.2}$$

With the factor k the damping performance can be configured. For $k = 1$ the SOGI band-pass acts like a second order band-pass where a sinusoidal input signal with the angular frequency ω' has a gain of 0 dB and all other frequencies are damped with -20 dB per decade. A value of $k < 1$ would increase the damping of the surrounding frequencies and a value of $k > 1$ would decrease the effect. The transfer function for the second SOGI output u'_{q} is

$$G_{\mathrm{SOGI-BPq}}(s) = \frac{u'_{\mathrm{q}}}{u}(s) = \frac{k\omega'^2}{s^2 + k\omega' s + \omega'^2} \tag{4.3}$$

For the specific case that the SOGI input signal u is a sinusoidal signal with the angular frequency ω' the signal after the second integrator and multiplier u'_{q} is a $-90°$ phase shifted version of the output signal u' of the first integrator. Through this characteristic the signal u'_{q} can be used to generate the virtual-flux [83].

The amplitude and frequency response of both transfer functions for $k = 1$ and $\omega' = 314$ rad/s ($f = 50$ Hz) are shown in Figure 4.4. As expected the amplitude response of the first output u' corresponds to an band-pass with a damping of -20 dB per decade. The output after the second integrator and multiplier u'_{q} shows a low-pass filter capability with an increased damping against high-frequency components of the input signal. The damping corresponds to the first output multiplied by two, i.e. to a damping of -40 dB per decade.

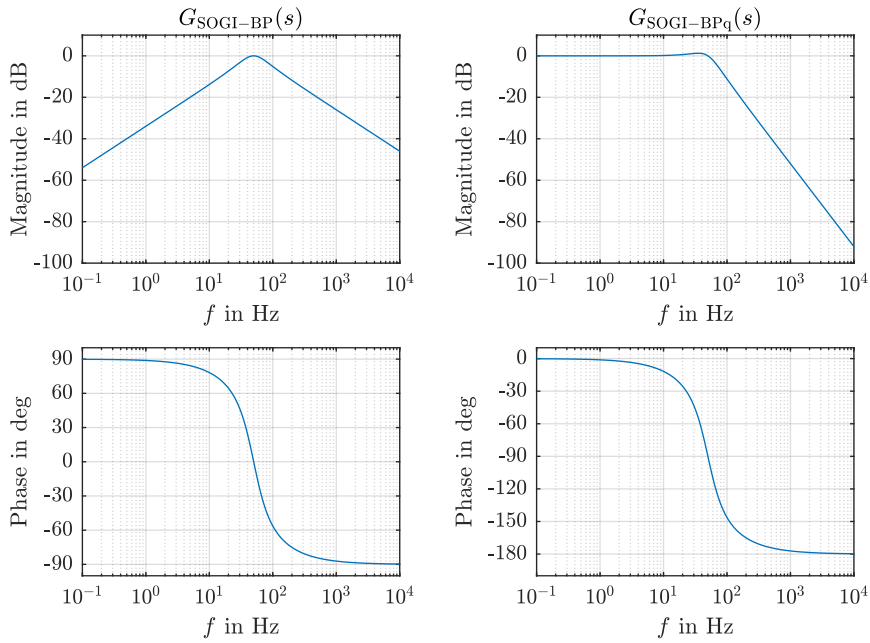


Figure 4.4: Bode diagram of SOGI band-pass (left) and after second integrator stage (right) with damping factor $k = 1$

To use the SOGI band pass for synchronization of a three-phase inverter system the input voltage u_{abc} is transformed to the $\alpha\beta$-system. This reduces the number of required SOGI-circuits to two. In literature this system is denoted by double second order generalized integrator (DSOGI) [80].

4.2.2 Frequency Readjustment

The previous shown SOGI circuit can only be used in grid application with a fixed frequency e.g. 50 Hz. For the case that the grid frequency varies a permanent deviation in the output signal can occur. To extend the SOGI to a frequency adaptive system several possibilities are presented in literature. One possibility could be using a standard SRF-PLL and its detected frequency ω' as input to the SOGI circuit [80]. In this case the SRF-PLL uses the calculated positive sequence as input to detect the actual centre frequency of the grid.

Another possibility is the usage of a Frequency-Locked-Loop (FLL) [84, 85]. This concept includes the property of the SOGI error signal ε and the SOGI output signal u'_{q}. When the input signal frequency is lower than the centre frequency of the SOGI the average value of the product is positive and vice versa. This signal can be used to readjust the centre frequency ω' by using an integrator with an initial value of 314 rad/s.

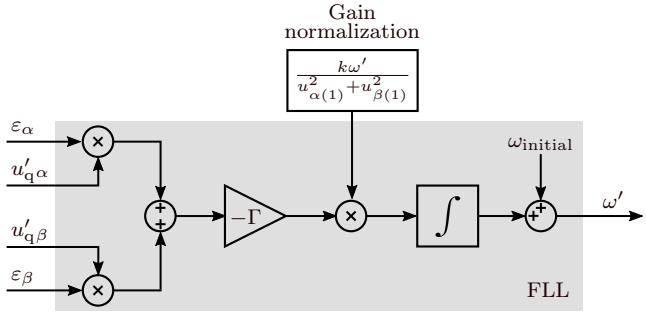


Figure 4.5: Circuit diagram of FLL for a three-phase application with gain normalization

To improve the reaction time of the system the additional factor Γ is introduced. The gain normalization ensures a linear response and a constant settling time of the FLL. The calculation of the necessary components of the positive sequence voltage is explained in more detail in Chapter 6.1. The whole structure of the FLL is shown in Figure 4.5. The two error signals of the α and β components are combined to use only a single FLL circuit in a three-phase application.

4.2.3 Additional Harmonic Component Acquisition

Due to the band-pass behaviour of the SOGI circuit harmonic components close to the centre frequency ω' are damped insufficiently. This leads to the problem that low order harmonics can still distort the output signal. To further improve the filter characteristics and harmonic rejection capability several approaches were published in literature.

- Connecting a comb-filter in front of the SOGI circuit which damps all even-numbered multiples of the fundamental frequency [86].
- Improving the filter characteristic of all harmonic components by a

series connection of two or more SOGI circuits to increase the band-pass behaviour [87].

- A synchronization method with improved harmonic filter characteristics also based on generalized integrators (GI) is the third order sinusoidal signal integrator (TOSSI) [88].
- A possibility to filter specific harmonic components is the parallel connection of several SOGI circuits to build a multi second order generalized integrator system (MSOGI) [89, 85].

The hereafter selected method for the inverter output voltage detection is the MSOGI. Despite the fact that the MSOGI has the greatest computational effort of the methods listed above, it allows the use of the determined harmonic components for the feed forward control of the inverter system. A simplified circuit of the MSOGI is shown in Figure 4.6.

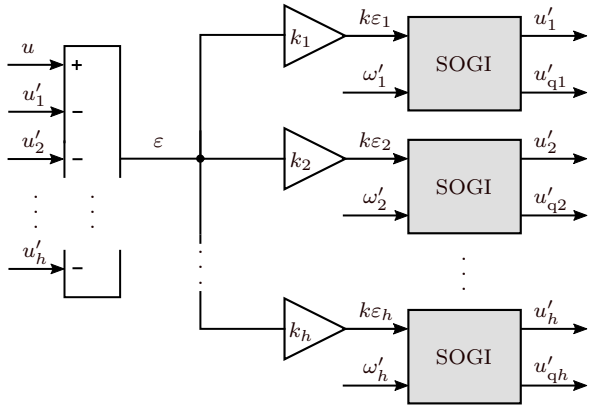


Figure 4.6: MSOGI band-pass circuit

Each individual SOGI circuit is set to a specific frequency ω'_h. The in-phase output signals u'_h are summed up and then subtracted from the input signal u forming the combined error signal ε for all SOGI circuits. The used factor for the SOGI which detects the fundamental component was set to $k_1 = \sqrt{2}$ which is the typical selected factor in literature [80, 83]. With this value the damping ratio of the circuit is $\zeta = 1/\sqrt{2}$ leading to a good compromise between settling time, overshot limitation, rejection of high frequency harmonics and dynamic response [8].

The factors k_h of the remaining SOGI circuits to detect the specific harmonic components h are calculated by

$$k_h = \frac{k_1}{h} \tag{4.4}$$

This relationship of the factors k_h leads to equal damping characteristics of all SOGI circuits against high frequency components of the input signal u. The detection of the fundamental frequency is realized by a FLL as explained before. The centre frequencies of the additional SOGI circuits can be easily calculated by

$$\omega'_h = \omega'_1 \cdot h \tag{4.5}$$

In this thesis for practical reasons only the harmonic components h of the 3rd, 5th, 7th, 11th and 13th are used for the MSOGI. These specific components are selected due to their higher permissible value ($U_h \geq 3$ %) in the grid standards [90]. Depending on the available computing power, further harmonics could be detected in the same way. The transfer function of the MSOGI circuit for a specified component can be calculated according to the following expression [89].

$$\begin{aligned} G_{\mathrm{MSOGI}h}(s) = &\frac{u'_h}{u}(s) = G_{\mathrm{SOGI-BP}h}(s) \\ &\cdot \prod_{\substack{i=1 \\ i \neq h}}^{n} \left(\frac{1 - G_{\mathrm{SOGI-BP}i}(s)}{1 - G_{\mathrm{SOGI-BP}h}(s) \cdot G_{\mathrm{SOGI-BP}i}(s)} \right) \end{aligned} \tag{4.6}$$

where h is the specified harmonic, i all considered harmonic components with $i \neq h$. In this specific case $h \in \{1, 3, 5, 7, 11, 13\}$.

The amplitude response of this transfer function is shown in Figure 4.7. In the upper part of the Figure the magnitude response of the fundamental (50 Hz) and all specified harmonic components when considering individual single SOGI circuits are shown. In the bottom figures the magnitude responses when using the MSOGI structure are shown. The transfer functions for the fundamental and 5th harmonic MSOGI component are shown in Appendix B.

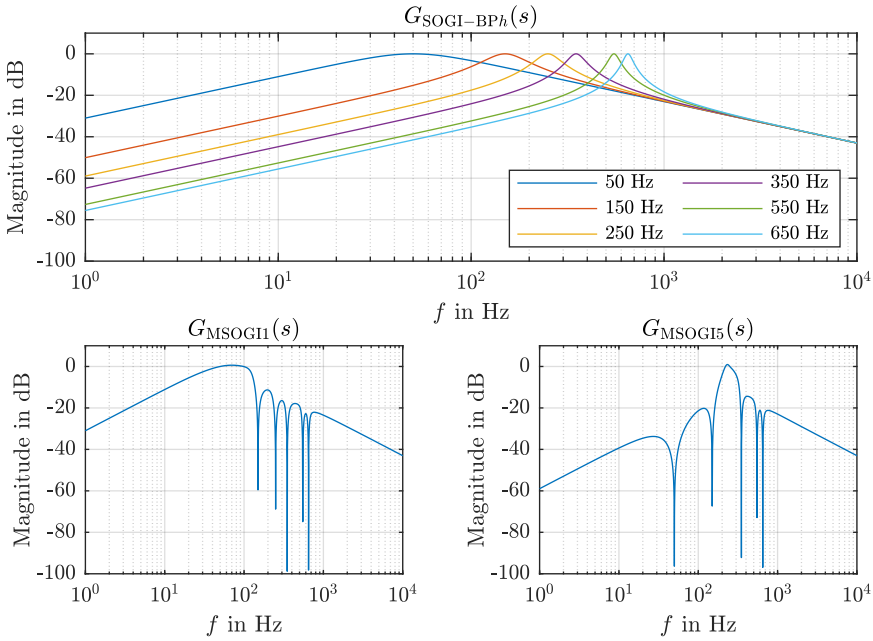


Figure 4.7: Top: magnitude responses of SOGI circuits for all selected harmonics. Bottom: magnitude responses of MSOGI circuits for the fundamental component (left) and the 5th harmonic (right)

It can be clearly seen that all harmonic components that are implemented in the MSOGI system show strong damping whereby the filter effect of the selected component is significantly improved compared to the standard SOGI.

The data obtained can not only be used to better filter the fundamental voltage, but also for the feed forward sector control of the inverter. For this purpose, the output values u'_h of the individual SOGI systems of all harmonic components are summed up, to generate an approximate reproduction of the average inverter output voltage.

$$\underline{u}_{\mathrm{ff}} = \sum_{h} \underline{u}'_h \qquad , h \in \{1, 3, 5, 7, 9, 11, 13\} \tag{4.7}$$

This calculation can also be used for the second SOGI outputs $u'_{\mathrm{q}h}$ to generate $\underline{u}_{\mathrm{qff}}$.

$$\underline{u}_{\mathrm{qff}} = \sum_{h} \underline{u}'_{\mathrm{q}h} \tag{4.8}$$

This phase shifted version of $\underline{u}_{\mathrm{ff}}$ is required in Chapter 6 to calculate the symmetrical components.

4.3 Sensorless Voltage Calculation

In the previous sections a concept to detect the average inverter output voltage for the proposed feed forward sector control was presented. Thereby the estimation of the input voltage signal u for the presented MSOGI system can be measured or calculated at different points which are shown in Figure 4.8:

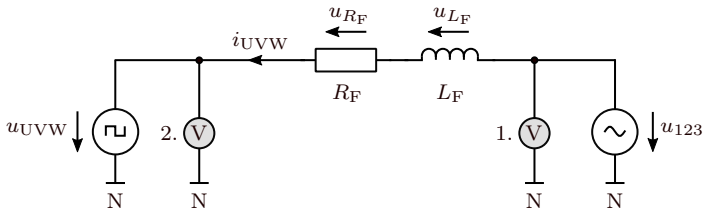


Figure 4.8: Simplified equivalent circuit of a grid connected inverter system with voltage measurement points

- Voltage measurement of u_{123} at the grid side of the filter (measurement point 1.). This has the advantage that the measured voltage can be used directly for the higher-level power control without compensation of voltage drops at the filter. But for determining the inverter output voltage u_{UVW} the voltage drop across the inductive and resistive component of the filter need to be compensated.
- Voltage measurement of u_{UVW} at the inverter output (measurement point 2.). After the necessary filtering of the rectangular inverter output voltage u_{UVW}, the filtered average inverter output voltage $\underline{u}_{\mathrm{inv}}$ can be used for sector control. For the set current or power control the filter needs to be compensated.
- Sensorless voltage calculation of u_{UVW}. This approach calculates the inverter output voltage u_{UVW} from the actual switching states and the

overall DC-link voltage. Similar to the measurement at the inverter output, this voltage needs to be filtered in an appropriate way.

Experiments using each of the three concepts showed that the feed forward sector selection for a direct current control method is a time critical system. Thus, a short time delay in the measurement circuit could lead to insufficient operation. This results in high demands on the measuring system that is used. To avoid those problems and for simplicity reasons the sensorless approach was selected and realized. The advantage here is, that the direct current controller will still work without or incorrect feed forward control, which increases the robustness of the proposed system.

It should be noted that in comparison to the ideal consideration of an inverter some real hardware characteristics should be taken into account. These include the inverter dead-time and the voltage drops across the inverter components. When using indirect controllers the dead-time and voltage drops at the components are compensated in the modulator to guarantee accurate control [32]. So far, the SHC algorithm used within this thesis completely ignores those effects.

However, to guarantee an accurate detection of the inverter output voltage these inverter properties should be included in the feed forward voltage calculation. The adoptions required to consider those aspects when considering a three- or five-level inverter system are explained below.

Output Voltage at Intermediate States

Chapter 2 shows the basic working principle of an inverter using ideal switches. In real hardware systems the switching behaviour of IGBTs is limited due to various reasons. For example, this means that when changing the output state of the inverter a certain time must pass between turning off one switch and turning on another. This time is called dead-time [32]. A dead-time chosen too short could lead to a short-term short-circuit of the DC-link in case of a two-level inverter, leading to a possible damage of the inverter. When considering multilevel inverters, this can also cause a destruction if the blocking voltage of the individual components is exceeded. The simplified modelling of the output voltage during the dead-time includes the selection of the voltage which is applied after the first IGBT is switched off and before the next one is switched on. The influence of these states on the output voltage of the inverter increases with the switching frequency and the dead-time. Table 4.1 shows all possible switching states of a three-level

Table 4.1: Output voltage states of a single-phase three-level inverter system including current depending intermediate states

State	Switch signals	u_{UM} ($i_{\mathrm{U}} > 0$)	u_{UM} ($i_{\mathrm{U}} < 0$)
1	1100	$U_{\mathrm{DC}}/2$	$U_{\mathrm{DC}}/2$
0.5	0100	0	$U_{\mathrm{DC}}/2$
0	0110	0	0
-0.5	0010	$-U_{\mathrm{DC}}/2$	0
-1	0011	$-U_{\mathrm{DC}}/2$	$-U_{\mathrm{DC}}/2$

inverter system. The two intermediate states are defined with state 0.5 and -0.5. In both cases only one of the four switches is turned on resulting in an inverter output voltage depending on the phase current and its sign.

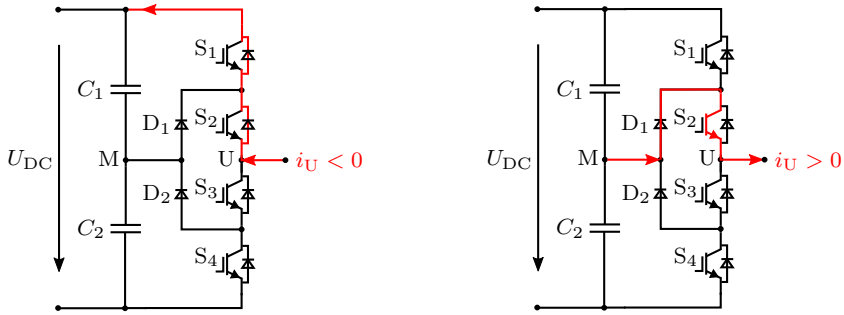
Table 4.2: Output voltage states of a single-phase five-level inverter system including current depending intermediate states

State	Switch signals	u_{UM} ($i_{\mathrm{U}} > 0$)	u_{UM} ($i_{\mathrm{U}} < 0$)
2	11110000	$U_{DC}/2$	$U_{DC}/2$
1.5	01110000	0	$U_{DC}/2$
1	01111000	$U_{DC}/4$	$U_{DC}/4$
0.5	00111000	0	$U_{DC}/4$
0	00111100	0	0
-0.5	00011100	$-U_{DC}/4$	0
-1	00011110	$-U_{DC}/4$	$-U_{DC}/4$
-1.5	00001110	$-U_{DC}/2$	0
-2	00011110	$-U_{DC}/2$	$-U_{DC}/2$

The nine possible output switching states of a five-level DCI system are listed in Table 4.2. Since the direct current controller does not take the intermediate states into account these states are subsequently generated via a generic state machine. Furthermore, in order to avoid additional filter effort for the measured current i_{UVW}, the set current i^*_{UVW} is used instead for selection.

Voltage Drops across IGBT's and Diodes

Due to the increased number of active and passive components when using multilevel inverters, an additional step to calculate the inverter output voltage is considered. So far, the inverter output voltage is calculated using the output state s_{UVW} and the total DC-Link voltage U_{DC}. Because of the voltage drop across the components and depending on the direction and magnitude of the inverter output current, the output voltage has to be adapted. Additional component characteristics that show also an impact on the output voltage are the temperature and the used driver circuitry of the IGBTs [91]. Figure 4.9 shows the resulting current paths and voltage drops for switching state 0.5 at the components of a three-level NPC depending on the current directions. In this intermediate switching state only the IGBT S_2 is turned on.



(a) Output current $i_{\mathrm{U}} < 0$ (b) Output current $i_{\mathrm{U}} > 0$

Figure 4.9: Current path of intermediate output state 0.5 [0 1 0 0], only S_2 = ON for a three-level DCI with different current directions

Figure 4.9a shows for $i_{\mathrm{U}} < 0$ that the current flows through the two body diodes of the IGBTs S_1 and S_2. The resulting voltage drops across the

diodes will lead to an increased output voltage u_{UM} for this specific switching state. In Figure 4.9b for $i_{\mathrm{U}} > 0$ the output voltage is reduced through the voltage drops across the clamping diode D_1 and IGBT S_2. Considering the condition, that the voltage drop of the IGBTs (u_{IGBT}) and the voltage drop of the diodes (u_{Diode}) are almost equal and that the number of passed components is always the same, the expression to calculate the real output voltage of an n-level DCI is given by

$$u_{\mathrm{UMreal}} = \begin{cases} u_{\mathrm{UM}} - (n-1) \cdot u_{\mathrm{IGBT}} \text{ for } i_{\mathrm{U}} > 0 \\ u_{\mathrm{UM}} + (n-1) \cdot u_{\mathrm{IGBT}} \text{ for } i_{\mathrm{U}} < 0 \end{cases} \tag{4.9}$$

4.3.1 Simulation Results of Synchronization System

To verify the functionality of the described concept, a simulation for a three-level inverter system was performed. A simplified circuit diagram of concept consisting of the MSOGI, FLL and the described inverter output voltage calculation is shown in Figure 4.10.

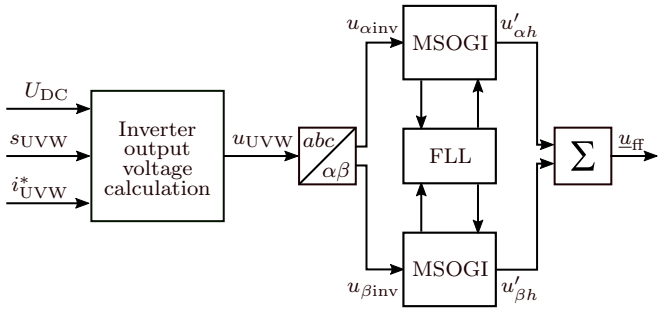


Figure 4.10: Simplified circuit of sensorless inverter output voltage detection concept

The output signals s_{UVM} of the standard SHC algorithm with outer tolerance bands for sector selection were used as input for the inverter output voltage calculation. The grid voltage in this specific case was simulated with 10 % 5th harmonic component and 5 % 7th harmonic component compared to the fundamental component with an amplitude of 325 V. The set point for the inverter output current was set to 0 A. This leads to the fact, that the average inverter output voltage is equal to the grid voltage. The initial value $\omega_{\mathrm{initial}}$ of the FLL was set to 314 rad/s and the factor Γ was set to -50.

The calculated rectangular output voltages of the inverter and the outputs of the MSOGI system are shown in Figure 4.11. For the sake of better illustration all output signals of the MSOGI system were transformed into the UVW-system.

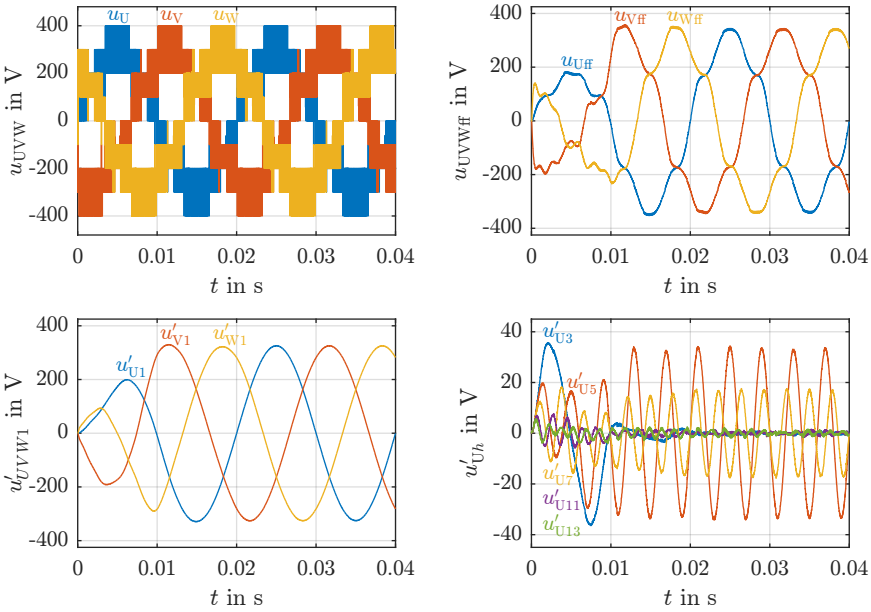


Figure 4.11: Simulation result for test of synchronization system. Left side: input voltage of MSOGI-system and detected fundamental voltage. Right side: sum of all MSOGI outputs and harmonic components of phase U

As one can see the detected fundamental output voltage u'_{UVW1} is detected without harmonic distortions. The amplitude of the fundamental voltage is 325,2 V and thus shows only a very small deviation to the real voltage. The settling time t_s of the generated output voltage is approximately one grid period and matches to the expected value which can be calculated according to [8, 92] by

$$t_{\mathrm{set}h} = \frac{9.2}{k_h \cdot \omega_h} \tag{4.10}$$

This equation and the choice of the MSOGI damping factors k_h results in

a constant settling time for all harmonic components. The harmonic components of 33,1 V (+1,8 %) for the 5th and 16,8 V (+3,4 %) for the 7th harmonic amplitude are also very accurate and close to the set point. The accuracy of the detected harmonic components increases with a higher number of levels due to the smaller voltage steps in the input signals. The noise on the other harmonic components shows a maximum of 1 V. Summarized it can be concluded that the proposed concept is well suited for the intended purpose. Due to the fact that no compensation of any grid filter is required, one of the main advantages is that the feed forward system can work independently from the load.

4.4 Space Vector Selection

4.4.1 $\tilde{a}_*\tilde{b}_*$-Transformation

Since the average inverter output voltage $\underline{u}_{\mathrm{ff}}$ is accurately determined by the MSOGI concept such method must be applied, that is able to calculate the correct location in the SV-diagram and to obtain the correct triangular sector surrounding that voltage. The corresponding space vectors are best suitable to control the output current. The generated average inverter output voltage $\underline{u}_{\mathrm{ff}}$ is transformed into the so called $\tilde{a}_*\tilde{b}_*$-system which was introduced in combination with the SHC algorithm in [64]. The idea of this transformation is to easily select the matching triangular sector and the surrounding space vectors for the direct current control scheme without using switching tables by simple integer calculation. Therefore, the new coordinate system is orientated on the diamond shaped unit cell. With this 120° coordinate system it is possible to represent all space vector positions of a multilevel inverter system with integer coordinates. The transformation of a three-phase voltage or current into the $\tilde{a}_*\tilde{b}_*$-system is defined by

$$\begin{bmatrix} u_{\tilde{a}_*} \\ u_{\tilde{b}_*} \end{bmatrix} = \boldsymbol{T}_{\tilde{a}_*\tilde{b}_*} \cdot \begin{bmatrix} u_{\mathrm{U}} \\ u_{\mathrm{V}} \\ u_{\mathrm{W}} \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} 1 & 0 & -1 \\ 0 & 1 & -1 \end{bmatrix} \cdot \begin{bmatrix} u_{\mathrm{U}} \\ u_{\mathrm{V}} \\ u_{\mathrm{W}} \end{bmatrix} \tag{4.11}$$

The geometrical representation of the new system is illustrated in Figure 4.12. As one can see the orientation of the $\tilde{a}_*$-axis is equal to the axis of α and phase U of the three-phase representation while the alignment of the 120° shifted axis for $\tilde{b}_*$ is identical to phase W.

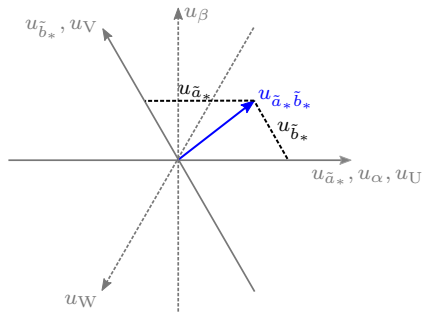


Figure 4.12: Geometrical representation of $u_{\tilde{a}_*\tilde{b}_*}$ system

To easily combine this system with the MSOGI output voltages the transformation from the $\alpha\beta$-system to the $\tilde{a}_*\tilde{b}_*$-system is required and given by

$$\begin{bmatrix} u_{\tilde{a}_*} \\ u_{\tilde{b}_*} \end{bmatrix} = \boldsymbol{T}_{\alpha\beta\tilde{a}_*\tilde{b}_*} \cdot \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \boldsymbol{T}_{\tilde{a}_*\tilde{b}_*} \cdot \boldsymbol{T}_{\alpha\beta}^{-1} \cdot \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \end{bmatrix} \cdot \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} \tag{4.12}$$

4.4.2 Sector Selection

To allow a simplified selection of the sector within the SV-diagram the $\tilde{a}_*\tilde{b}_*$ voltage needs to be normalized. Therefore, the factor κ which depends on the level count of the inverter is introduced to calculate the normalized a_*b_* components

$$\begin{bmatrix} u_{a_*} \\ u_{b_*} \end{bmatrix} = \kappa \cdot \boldsymbol{T}_{\alpha\beta\tilde{a}_*\tilde{b}_*} \cdot \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} \tag{4.13}$$

The factor κ depends on the level count n and the overall DC-link voltage U_{DC} and can be calculated by

$$\kappa = \frac{3 \cdot (n-1)}{2 \cdot U_{\mathrm{DC}}} \tag{4.14}$$

This transformation can now be used to convert all space vector positions from the $\alpha\beta$-system into the a_*b_*-system represented with integer coordinates only.

To increase clarity the normalized transformation is designated by

$$\boldsymbol{T}_{\alpha\beta *} = \kappa \cdot \boldsymbol{T}_{\alpha\beta \tilde{a}_* \tilde{b}_*} \tag{4.15}$$

and the resulting vector in the a_*b_*-system by

$$\vec{u}_* = \begin{bmatrix} u_{a_*} \\ u_{b_*} \end{bmatrix} \tag{4.16}$$

With these notations, the triangular sector selection process can be carried out with the following steps.

1. The generated feed forward voltage $\underline{u}_{\mathrm{ff}}$ is transformed into the normalized a_*b_*-system resulting in the feed forward voltage vector $\vec{u}_{\mathrm{ff}*}$.

$$\vec{u}_{\mathrm{ff}*} = \boldsymbol{T}_{\alpha\beta *} \cdot \underline{u}_{\mathrm{ff}} \tag{4.17}$$

2. Calculation of the floor function to detect the base vector of the diamond shaped unit cell within the SV-diagram. The base vector of a diamond-shaped unit cell is always located in the bottom-left corner of each diamond.

$$\vec{U}_{\mathrm{ff}*\mathrm{base}} = \lfloor \vec{u}_{\mathrm{ff}*} \rfloor = \begin{bmatrix} \lfloor u_{a_*\mathrm{ff}} \rfloor \\ \lfloor u_{b_*\mathrm{ff}} \rfloor \end{bmatrix} \tag{4.18}$$

   An illustration of a three-level inverter SV-diagram in normalized a_*b_* coordinates with one example of $\vec{u}_{\mathrm{ff}*}$ and its unit cell (green) is shown in Figure 4.13. In addition, all possible base vectors for the shown feed forward voltage during one grid period are highlighted.

3. The calculation of the surrounding four space vectors $\vec{\mathrm{SV}}_*$ of the selected diamond in a_*b_* coordinates. The applied feed forward voltage $\vec{u}_{\mathrm{ff}*}$ is shown in Figure 4.13. The base vector coordinates for this example are [1 0] defining the green diamond shaped unit cell as shown in the Figure 4.13. The first space surrounding vector is equal to the base vector.

$$\vec{\mathrm{SV}}_{*1} = \vec{U}_{\mathrm{ff}*\mathrm{base}} = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \tag{4.19}$$

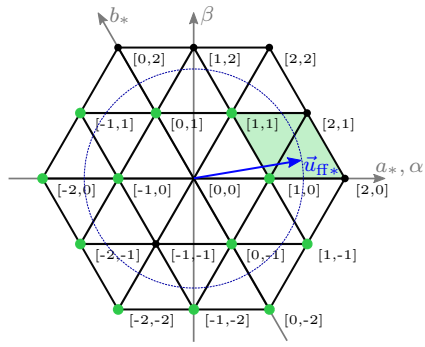


Figure 4.13: Representation of feed forward voltage $\vec{u}_{\mathrm{ff}*}$, selected sector base vectors $\vec{U}_{\mathrm{ff}*\mathrm{base}}$ and three-level SV-diagram in normalized $\alpha_*\beta_*$ coordinates

The three remaining surrounding space vector positions of the diamond are calculated by

$$\vec{\mathrm{SV}}_{*2} = \vec{U}_{\mathrm{ff}*\mathrm{base}} + \begin{bmatrix}1\\0\end{bmatrix} = \begin{bmatrix}1\\0\end{bmatrix} + \begin{bmatrix}1\\0\end{bmatrix} = \begin{bmatrix}2\\0\end{bmatrix} \tag{4.20}$$

$$\vec{\mathrm{SV}}_{*3} = \vec{U}_{\mathrm{ff}*\mathrm{base}} + \begin{bmatrix}1\\1\end{bmatrix} = \begin{bmatrix}1\\0\end{bmatrix} + \begin{bmatrix}1\\1\end{bmatrix} = \begin{bmatrix}2\\1\end{bmatrix} \tag{4.21}$$

$$\vec{\mathrm{SV}}_{*4} = \vec{U}_{\mathrm{ff}*\mathrm{base}} + \begin{bmatrix}0\\1\end{bmatrix} = \begin{bmatrix}1\\0\end{bmatrix} + \begin{bmatrix}0\\1\end{bmatrix} = \begin{bmatrix}1\\1\end{bmatrix} \tag{4.22}$$

As the number of possible space vector coordinates is limited, the maximum steps in a_* and b_* directions depends on the level count of the inverter system. The limits can be described by

$$\left\{a_*, b_* \in \mathbb{Z} \middle| -l \leq a_*, b_* \; and \; a_* - b_* \leq l\right\} \tag{4.23}$$

where l is the level dependent boundary:

$$l = n - 1 \tag{4.24}$$

4. Calculation of the used triangular sector. As shown in Figure 4.13 the base vector only detects the diamond sector in which the actual

feed forward voltage is located. However, the SHC algorithm requires only one of the two triangular sectors defined by the diamond unit cell to control the inverter output current. Therefore, to choose the correct triangular sector, the auxiliary parameter $\vec{u}_{\mathrm{ff}*\mathrm{base}}$ which defines the vector between the actual feed forward voltage and the associated base vector is calculated by

$$\vec{u}_{\mathrm{ff}*\mathrm{base}} = \vec{u}_{\mathrm{ff}*} - \vec{U}_{\mathrm{ff}*\mathrm{base}} \tag{4.25}$$

and multiplied with the vector $\begin{bmatrix} 1 \\ -1 \end{bmatrix}$ which is perpendicular to the border-line between both triangles.

$$\text{sector} = \begin{cases} \text{right for } \vec{u}_{\mathrm{ff}*\mathrm{base}} \cdot \begin{bmatrix} 1 \\ -1 \end{bmatrix} > 0 \\ \text{left} \quad \text{for } \vec{u}_{\mathrm{ff}*\mathrm{base}} \cdot \begin{bmatrix} 1 \\ -1 \end{bmatrix} < 0 \end{cases} \tag{4.26}$$

4.4.3 Generation of Switching States

One further advantage of the introduced coordinate system is that the inverter output switching positions s_{UVW} can be directly determined by the integer coordinates of the space vectors. To determine those inverter switching positions the corresponding coordinates of the selected space vectors $\mathrm{S}\vec{\mathrm{V}}_*$ in the a_*b_*-system are extended by a third component which is set to zero.

$$s_{\mathrm{UVW}*} = \begin{bmatrix} a_* \\ b_* \\ 0 \end{bmatrix} \tag{4.27}$$

In order to obtain the real switching state the components must be modified by applying the following expression.

$$s_{\mathrm{UVW}} = s_{\mathrm{UVW}*} - \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \cdot \left(max(s_{\mathrm{UVW}*}) - \frac{n-1}{2} \right) \tag{4.28}$$

Considering for example the space vector $\mathrm{S}\vec{\mathrm{V}}_{*1}$ the following switching signal would be calculated.

$$\vec{\mathrm{SV}}_{*1} = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \Rightarrow s_{\mathrm{UVW}*} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \Rightarrow s_{\mathrm{UVW}} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \tag{4.29}$$

The redundant switching states can also be calculated using the relationship. The available number of possible switching positions is limited depending on the level count n as defined before. For a three-level inverter, the switching positions are ± 1 and 0, and for a five-level inverter ± 2, ± 1 and 0. In general, the following condition can be used for odd-numbered level counts.

$$\left\{ s \in \mathbb{Z} \middle| -\frac{n-1}{2} \leq s \leq \frac{n-1}{2} \right\} \tag{4.30}$$

To calculate all possible redundant states the vector [1 1 1] is added or subtracted as long as one of the three components reaches the described maximum condition. For $\vec{\mathrm{SV}}_{*1}$ in the above example, one redundant switching position exists. The redundant switching position s_{UVWred} is therefore calculated by

$$s_{\mathrm{UVWred}} = s_{\mathrm{UVW}} - \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} - \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} = \begin{bmatrix} 0 \\ -1 \\ -1 \end{bmatrix} \tag{4.31}$$

4.5 Summary

This chapter introduced the basic principles of an improved controller concept based on the SHC algorithm for a grid connected multilevel inverter system. With the presented feed forward sector control concept the actual triangular sector can be detected and thus the use of the outer tolerance band which increases the output current distortion under steady state conditions is avoided. Caused by input values that depend on measured system variables, the proposed system is not a strict feed forward control. Nevertheless, the term feed forward sector control will be used to describe the system in the following chapters.

The main components of the feed forward sector selection system are the MSOGI-FLL system for the sensorless generation of the average inverter output voltage combined with a novel coordinate transformation for easy determination of the voltage sector in the multilevel SV-diagram. The basic structure of the proposed feed forward system described in this chapter is shown in Figure 4.14.

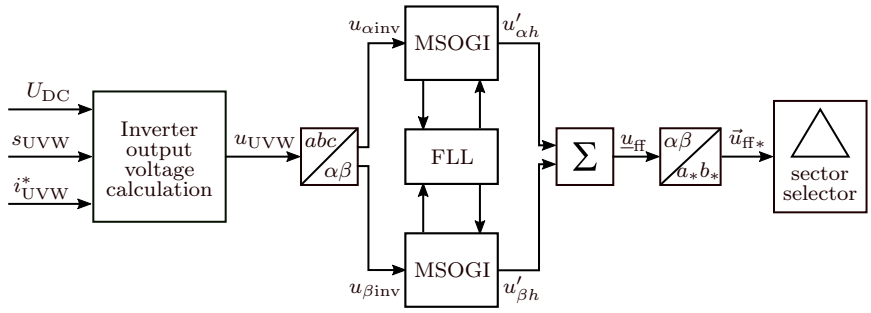


Figure 4.14: Simplified circuit of the presented sensorless feed forward sector selection system

Chapter 5

Improved Direct Current Control

In the following chapter the principle working behavior of the proposed feed forward concept combined with the SHC algorithm is investigated. This new combination is expected to provide both, a good steady-state as well as a robust and fast dynamic performance. The simplified structure of the improved SHC with the feed forward sector control is shown in Figure 5.1. The new feed forward sector control block consists of all components shown in Figure 4.14.

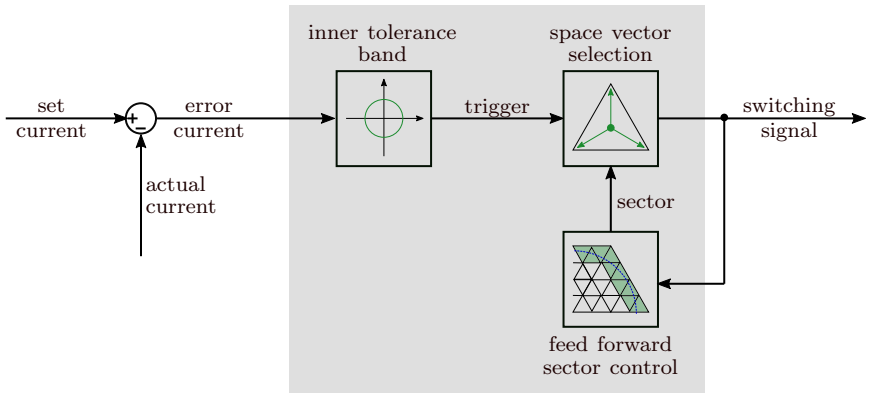


Figure 5.1: Simplified structure of SHC with feed forward sector control

Within the simulations a three-level NPC and a five-level DCI system are used to verify the functionality. Additionally combining the feed forward control with the standard outer tolerance band guarantees a high dynamic reaction during possible grid faults. This enables the overall control system to guarantee a problem-free operation under dynamic situations which can occur in the grid.

5.1 Simulation Parameters

Table 5.1: Simulation parameters of three- and five-level DCI models

Parameter	Symbol	Value
Grid voltage	u_{123}	400 V (50 Hz)
Filter inductance	L_{F}	1.0 mH
Set current	$\hat{I}^*_{123}$	20 A
Inner hysteresis band	$\underline{B_i}$	$\sqrt{2}$ A
Outer hysteresis band	$\underline{B_o}$	$\sqrt{9}$ A
MSOGI coefficient	k_1	$\sqrt{2}$
FLL coefficient	Γ	-50
Dead-time	t_{dead}	3 μs
Block-time	t_{block}	3 μs

All following simulations of the improved SHC control scheme are conducted with the parameters listed in Table 5.1. For comparability, the three- and five-level inverter models are simulated with the same parameters. The phase angle for the set current $\hat{I}^*_{123}$ is in phase with the positive sequence of the grid voltage. For realistic simulation, the inverter dead-time, to prevent DC-link short circuits, and a controller block-time, to avoid possible unwanted switching operations, triggered by system oscillations after the switching operation are taken into account. After completion of the dead-time the block-time locks the current controller for a short time. If changes to individual parameters were necessary for certain special cases, these are noted in the relevant section. All indicated switching frequencies are the values per IGBT averaged over one second. The necessary DC-link voltage balancing for the three-level NPC is based on the working principle as presented in [62, 63]. Due to limited balancing capability of the five-level DCI, this type is simulated with four DC-sources connected to the DC-link capacitors. Since the proposed concept works independently of the DC-link balancing, it has no influence on the feed forward control.

All simulations in the next chapters were carried out using MATLAB/ SIMULINK. To ensure a good compatibility with the measurements within the experimental verification, the simulation models for the current controller and synchronization method were build up compatible to the HDL coder toolbox. This means that almost all delay times necessary for calculations in the final FPGA hardware implementation are also implemented in the simulation model. This procedure has the further advantage that the simulation model can directly be used to generate the VHDL code from SIMULINK. In the final hardware implementation on the FPGA platform this code is directly used to generate the program code with XILINX Vivado. For realistic simulation of the non-ideal properties in the experimental inverter hardware the Simscape Power Systems toolbox was used.

5.2 Feed forward Control Within the Sector

All space vector based direct current or power controllers presented in chapter 3.2 show one common characteristic. If the correct sector in the SV-diagram for controlling the current inside a tolerance band or tolerance area is selected, no further benefit of the voltage information within the sector is obtained. Only the current or power error is used to set the output switching states using predefined switching tables for space vector selection.

In addition to the feed forward control of the sector described in Chapter 4, the SHC enables the use of the feed forward voltage $\underline{u}_{\mathrm{ff}}$ within the sector instead of the pseudo voltage $\underline{U}_{\mathrm{pseudo}}$. This can be realized by replacing the triangle midpoint voltage $\underline{U}_{\mathrm{pseudo}}$ within Equation 3.14 by the generated feed forward voltage.

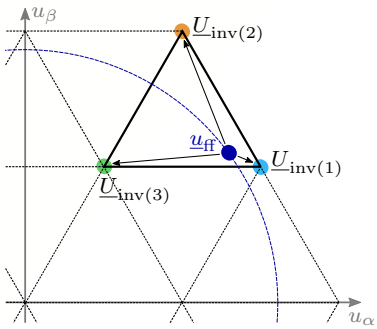
$$\underline{u}_{\mathrm{L_F ff}(k)} = \underline{U}_{inv(k)} - \underline{u}_{\mathrm{ff}}, \qquad k = 1, 2, 3 \tag{5.1}$$

The one space vector that reduces the current error best can be calculated by

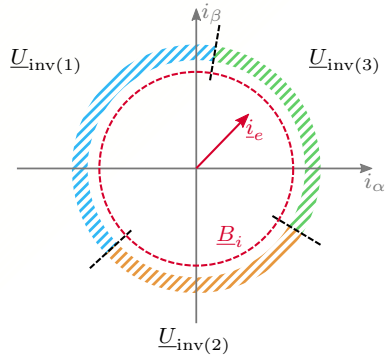
$$k_{\mathrm{optff}} = \underset{k \in \{1,2,3\}}{\arg\min} \left(\mathrm{Re}\{\underline{u}_{\mathrm{L_F ff}(k)} \cdot \bar{\underline{i}}_{\mathrm{e}}\} \right). \tag{5.2}$$

This relationship shows a dependency of the three angular ranges around the circular tolerance band on the actual voltage position within a sector. They identify the best space vector. Figure 5.2 shows an example of the effects on the angular ranges of the tolerance band when passing through a triangular sector. For better illustration, the figure is divided into the following three voltage operating points.

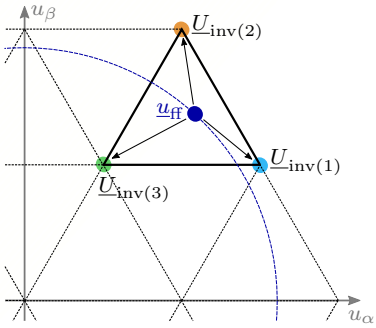
- Operating point one (Figure 5.2a). At this point the feed forward voltage $\underline{u}_{\mathrm{ff}}$ is located near the space vector position $\underline{U}_{\mathrm{inv}(1)}$. According to Equation 5.2 the resulting optimal angular range of the tolerance band increases to 142° for $\underline{U}_{\mathrm{inv}(1)}$ while the other two angular areas for $\underline{U}_{\mathrm{inv}(2)}$ and $\underline{U}_{\mathrm{inv}(3)}$ decrease. Compared to the fixed centre position of $\underline{U}_{\mathrm{pseudo}}$ from the standard SHC where each angular range is 120°, $\underline{u}_{\mathrm{ff}}$ leads to varying ranges.
- Operating point two (Figure 5.2c). The feed forward voltage is close to the centre of the triangle. This results almost in the same angular ranges around the tolerance band like the standard SHC controller with its pseudo reference voltage.



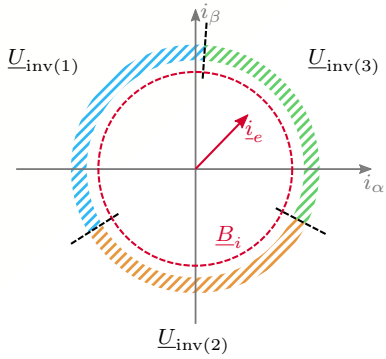
(a) Operating point one



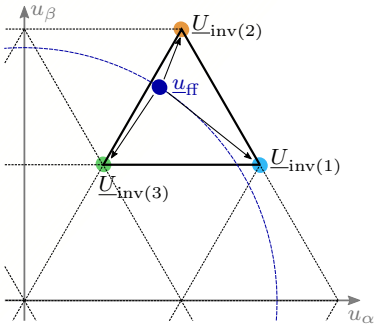
(b) Tolerance band at point one



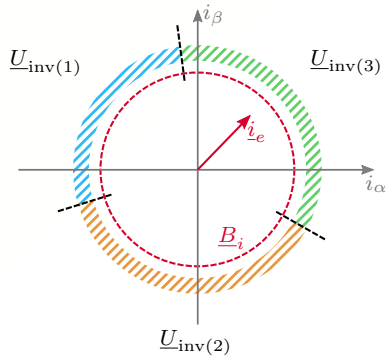
(c) Operating point two



(d) Tolerance band at point two



(e) Operating point three



(f) Tolerance band at point three

Figure 5.2: Impact of the feed forward voltage control on the angular sections of the tolerance circle within one sector

- Operating point three (Figure 5.2e). The detected voltage is located at the left border of the triangle and thus almost exactly between two switching positions. The effect of the space vectors $\underline{U}_{\mathrm{inv}(2)}$ and $\underline{U}_{\mathrm{inv}(3)}$ within this operation point in the α and β direction is, therefore, almost inverted. These two space vectors cover a large angular area of the current tolerance band.

The angular ranges of the described voltage operating points are additionally listed in Table 5.2.

Table 5.2: Angular ranges of the possible space vectors for the presented voltage points in Figure 5.2

Voltage point	$\underline{U}_{\mathrm{inv1}}$	$\underline{U}_{\mathrm{inv2}}$	$\underline{U}_{\mathrm{inv3}}$
1	142°	112°	106°
2	125°	123°	112°
3	98°	127°	135°

In contrast to that, the standard SHC algorithm known from literature would have three fixed 120° segments around the current error tolerance band due to the fixed voltage position of $\underline{U}_{\mathrm{pseudo}}$ in the centre of the triangular sector. It can be concluded from Table 5.2 that the working behaviour of the standard SHC could lead to a wrong selection of the best space vector for current control.

5.3 Comparison of Switching Characteristics

In the following section the switching characteristic of the sector selection process and the influence on the resulting inverter output current i_{UVW} are investigated in more detail. Therefore, a comparison of the new and previously proposed feed forward sector selection scheme and the state of the art sector selection using the outer tolerance band of the standard SHC controller is performed.

5.3.1 Switching Characteristic of Three-Level NPC

Figure 5.3 shows the three-level SV-diagram and the respective voltages for the space vector selection when using the outer tolerance band or the feed forward control for selection of the correct sector. The standard grid voltage for this working point corresponds to a modulation index of 1.08. As it can be seen when using only the outer tolerance band the voltage location jumps between the centre points of the triangles. Since the grid voltage is located in the outer hexagon, 18 sector changes per grid period are necessary for accurate control. The generated feed forward control voltage is a continuous signal with a slight noise due to the summation of the individual components

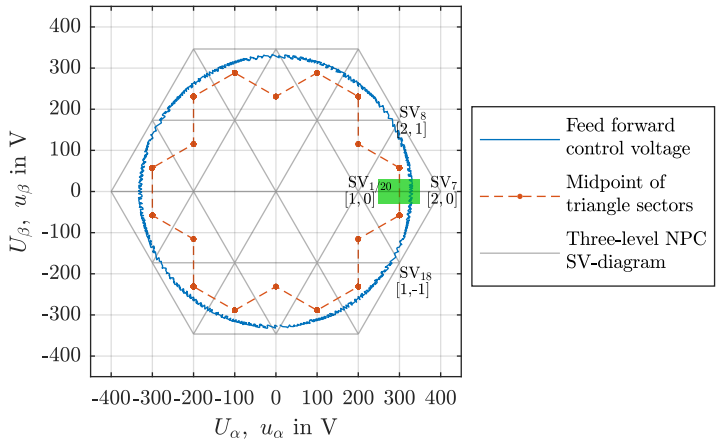


Figure 5.3: Three-level SV-diagram with feed forward voltage and midpoint voltage of triangle sectors selected by the outer tolerance band

of the MSOGI system. It can clearly be seen that the feed forward voltage control provides a better voltage-position tracking.

In addition to the overall picture of the two voltages, the transition between two triangular sectors is highlighted in green colour. The effect of both methods on the sector transition and the current error is considered in more detail for the highlighted region in the following section. The lower one of the two sectors uses the space vectors SV_1, SV_7 and SV_{18} and the upper sector uses SV_1, SV_7 and SV_8 for controlling the current.

The effects on the current error for using the standard outer tolerance band control and the feed forward method are shown in Figure 5.4. In addition to the three-phase output current, the respective error currents are shown as α and β components and as squared absolute value. This value is used to trigger the selection of a new space vector or the selection of a new sector as described in Chapter 3.2.5.

Considering the inverter output current when using the outer tolerance band small and short spikes in the three-phase current are apparent. These errors can be better analysed in the figure of the squared absolute value of the error current. Based on the three-level SV-diagram (Figure 5.3) and the desired operating point the voltage has to pass 18 sectors. However, investigating the squared absolute value of the current error only 12 violations of the outer tolerance band are visible. This is caused by the small dwell times in some sectors where the outer tolerance band is triggered twice within a short time period.

From the $\alpha\beta$ representation of the current error it is noticeable, that the outer tolerance band is always reached at the same six areas. To explain this effect it is necessary to consider the setting up of the inner tolerance band again. According to the fixed position of $\underline{U}_{\text{pseudo}}$ in the centre of the triangular sector, the tolerance band can be divided into three identical segments. Considering the two different triangular sector orientations, i.e. one triangle with the top showing upwards, the other downwards a total of six borderlines between the angular ranges exist. Figure 5.5 shows an example of the three angular tolerance band segments for the upper and lower sector highlighted in Figure 5.3. As one can see, the six borders between the segments correspond exactly to the area where the current error is exceeding the inner tolerance band. This behaviour is caused by the fact that every time when the boundary between two triangular sectors is reached, the SHC continually selects only those two space vectors that are not strong enough to reduce the current error until the outer tolerance band

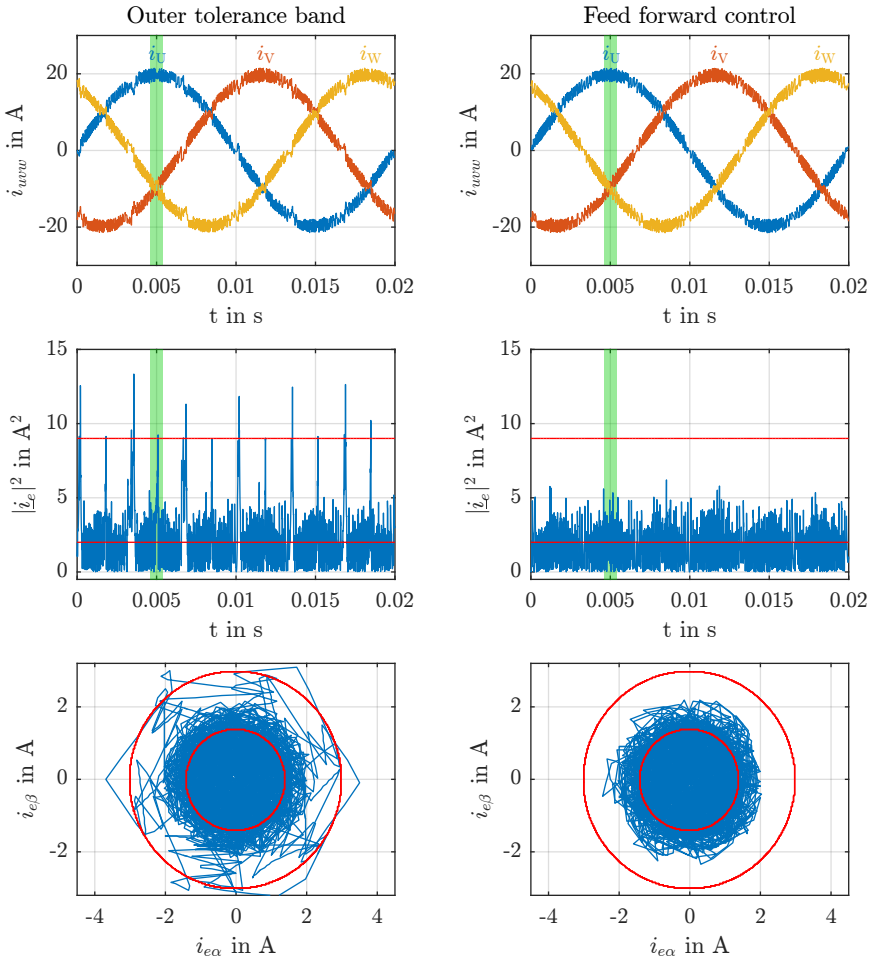
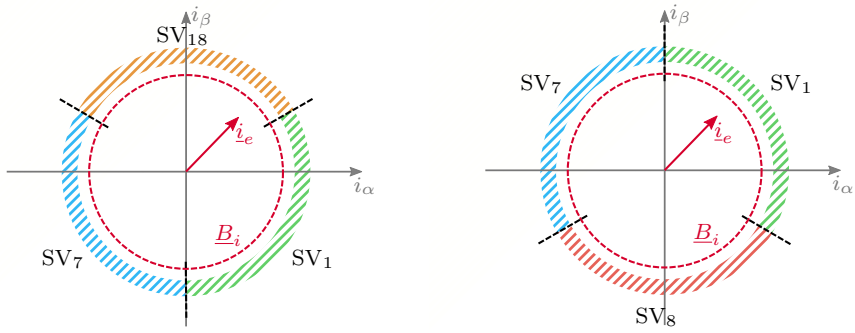


Figure 5.4: Comparison of simulated three-level NPC output current and current error at standard working point for SHC using outer tolerance bands and feed forward control

is reached. Therefore, the current error is toggling between the inner and outer tolerance band by switching between two angular segment.

Comparing the output current and current error of the proposed feed forward sector control system it is obvious that the current error does not reach the outer tolerance band. This shows that the proposed system can



(a) Lower sector (b) Upper sector

Figure 5.5: Tolerance band areas and used space vectors of standard SHC of the two viewed sectors

be used to better and more precisely control all sector changes. The small overshoot above the inner tolerance band occurs due to the calculation times of the controller and the intermediate switching states during the dead-time. The average switching frequencies in all three phases were 4200 Hz while using the outer tolerance band control and 4100 Hz for the feed forward sector control. Figure 5.4 shows that the proposed system is able to reduce both the switching frequency by the improved selection of the best space vector as well as the error current.

To explain the sector change of both methods in more detail the highlighted time segment around 5 ms from Figure 5.4 is used. Figure 5.6 shows the point in time were the specific sector change occurred.

In both error current figures, the point in time of the sector change is highlighted. Using the outer tolerance band control the sector change is detected at $t = 5.1$ ms whereas with the feed forward control at $t = 4.9$ ms. As a result, the feed forward control detects the sector change approximately 200 μs earlier than the outer tolerance band control. Between $t = 4.9$ ms and $t = 5.1$ ms, i.e. the time of the real sector change, it can also be seen that the outer tolerance band control is not strong enough any more to keep the current error below the inner tolerance band. Without being able to reduce the error current, the SHC changes the output state several times. This is caused by the SHC algorithm which is continually recalculating the best space vector out of three as soon as the error current is rising and above the inner tolerance band.

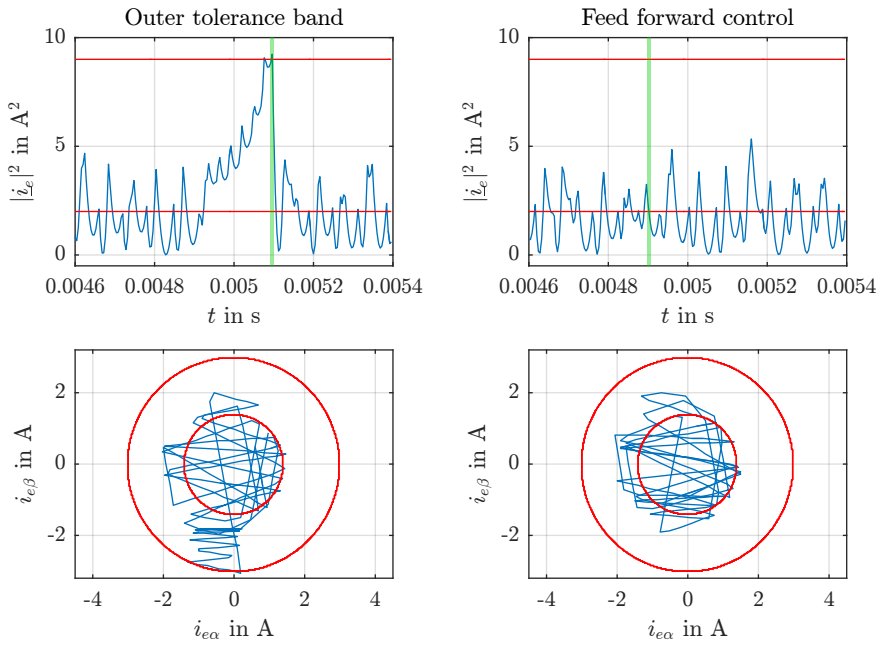


Figure 5.6: Detail enlargement of current error at standard working point for SHC using outer tolerance bands and feed forward control

The selected space vectors related to this time segment in the normalized a_*b_* coordinates are shown in Figure 5.7. As one can see the controller is switching between the two identical space vectors in the time segment between the inner and outer tolerance band. The normalized a_*b_* coordinates [1 0] and [2 0] thereby correspond to the space vectors SV_1 and SV_7. When considering the current error in the $\alpha\beta$ representation of Figure 5.6 and the tolerance band structure of the active sector at this time in Figure 5.5a the switching behaviour at this point can be explained. As soon as the real voltage has changed the sector and the controller itself remains in the old sector and, therefore, still uses the old space vectors the effects of these space vectors on the current error are incorrect. In this particular case, the current error increases in the negative β direction. This error can not be reduced by any of the three space vectors of the lower sector because the voltage has moved already into the next sector. In contrast, the α component can still be controlled with the available space vectors. This is also the reason

for the current error to follow the shown path. Since the squared absolute current error can be reduced by reducing the α component, the controller always switches between the two space vectors SV_1 and SV_7. As soon as the outer tolerance band is reached, the tolerance band structure changes to that in Figure 5.5b. This leads to the selection of space vector SV_8 which corresponds to the coordinates [2 1]. This space vector is able to reduce the error current and its α and β component.

The described switching behaviour is also mandatory in some scenarios within a sector. If the selected space vector has only a small effect the current error is sometimes not reduced fast enough below the inner tolerance band. In the described case the current error might reach another segment and thus the SHC would choose an alternative space vector out of this sector. Without this switching behaviour unnecessary trigger events of the outer tolerance band would occur.

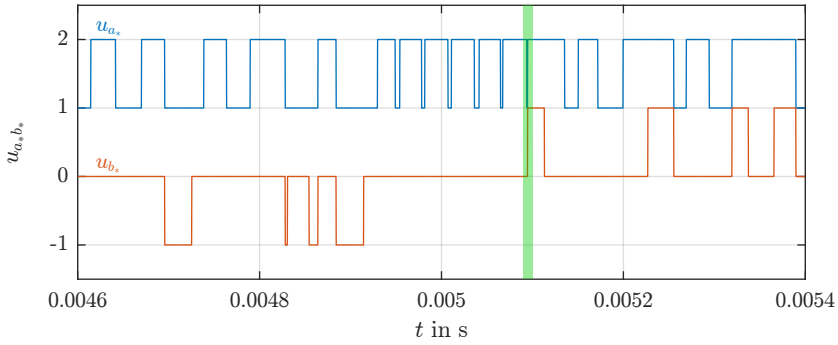


Figure 5.7: Detail enlargement of choosen SV-coordinates by using the outer tolerance band

5.3.2 Switching Behaviour of Five-level DCI

The switching behaviour of a five-level DCI inverter system is analysed similar to the analysis of the three-level system switching behaviour in the previous section. Figure 5.8 shows the SV-diagram of a five-level inverter system with its 96 triangular sectors. For the specific working point, the outer tolerance band has to be triggered 42 times per grid period. The average inverter output voltage detected by the proposed feed forward system

is able to exactly trigger all sector changes as before.

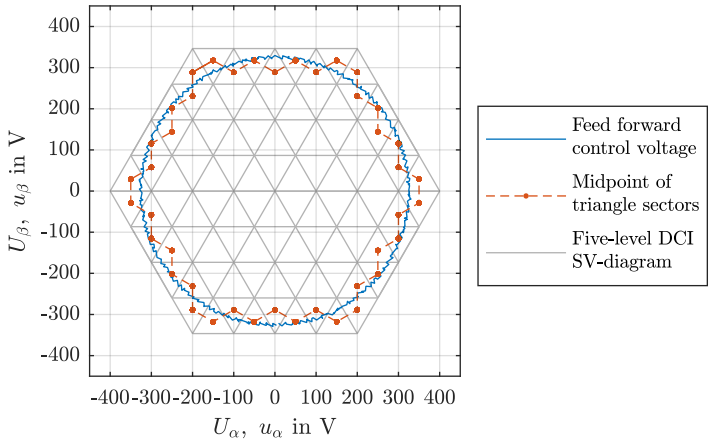


Figure 5.8: Five-level SV-diagram with feed forward voltage and midpoint voltage of triangle sectors selected by the outer tolerance band

The working behaviour of both control concepts of the inverter output current is shown in Figure 5.9. When considering the output current using only the outer tolerance bands, the outer tolerance band is reached multiple times. This behaviour is also shown in the squared absolute value of the error current. The trajectory of the error current shows that an increased level count leads to an increased current error since the dwell time within the triangular sectors become very small. Above a certain level count, the current error would permanently touch the outer tolerance band.

The representation of the error current in α and β components shows similar characteristics compared to the three-level system. The outer tolerance band is violated at the six equal points as before caused by the switching behaviour between the inner and outer tolerance band.

In contrast the output current and current error of the feed forward controlled inverter system is kept below the outer tolerance band. The smaller overshoot of the inner tolerance band is caused by the decreased $\mathrm{d}i/\mathrm{d}t$ compared to the three-level simulations. This benefit would allow to decrease the outer tolerance band. The switching frequencies of both control methods were 2030 Hz while using only the outer tolerance band and 1170 Hz for using the feed forward control. The difference of 42 % is caused by the

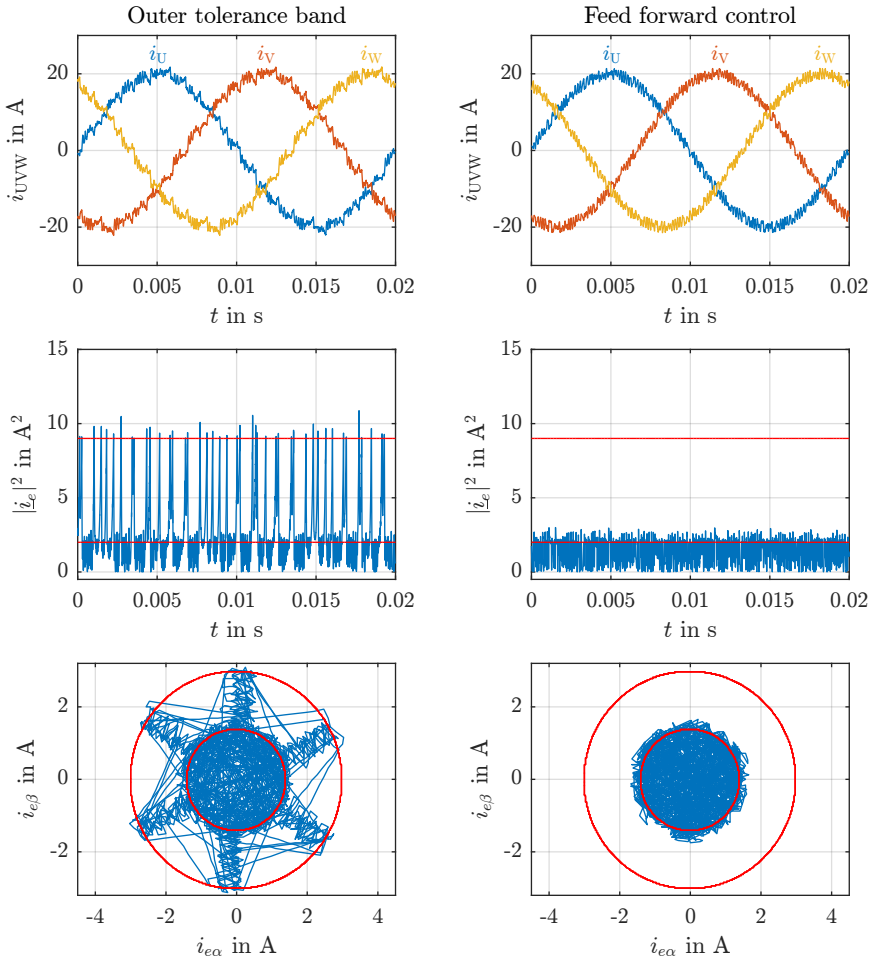


Figure 5.9: Comparison of simulated five-level DCI output current and current error at standard working point for SHC using outer tolerance band and feed forward control

higher number of switching operations between the inner and outer tolerance bands. This indicates that this difference would further increase if the level count and thus the number of required sector changes per grid period increases.

5.4 Sector Control under Dynamic Conditions

As shown in previous sections, the proposed feed forward sector selection control has advantages compared to the standard SHC. These advantages increase thereby with the level count of the used inverter system. However, the two test cases were carried out under steady state conditions. In grid connected applications dynamic fault cases like voltage sags can occur. To guarantee a proper functionality the proposed sector selection control should, therefore, be combined with the standard outer tolerance band sector control of the SHC algorithm. If a dynamic situation occurs accurate control of the current can not be guaranteed any more due to the wrongly selected sector during the settling time of the MSOGI system. Therefore, the outer tolerance band control must be active and needs priority over the feed forward control as long as the generated feed forward voltage is located in the wrong sector. As soon as this voltage is correct again the SHC uses the feed forward voltage for sector selection. In order to realize this behaviour, the following properties are implemented in the controller.

- Both selection procedures are always active and outer tolerance band control is dominant.
- If the outer tolerance band is triggered, the following steps are initiated.
  1. Calculation of the centre point voltage $\underline{U}_{\text{pseudo}}$ of the actual triangle.

$$\underline{U}_{\text{pseudo}} = \begin{cases} \vec{u}_{\text{ff}*\text{base}} + \begin{bmatrix} \frac{2}{3} \\ \frac{1}{3} \end{bmatrix} & \text{for right triangle} \\ \vec{u}_{\text{ff}*\text{base}} + \begin{bmatrix} \frac{1}{3} \\ \frac{2}{3} \end{bmatrix} & \text{for left triangle} \end{cases} \tag{5.3}$$

  2. Calculation of the centre points $\underline{U}_{\text{pseudo}(k)}$ of the surrounding triangles. Considering that the active triangle is the left the voltages can be calculated by

$$\underline{U}_{\text{pseudo}(1)} = \underline{U}_{\text{pseudo}} + \begin{bmatrix} \frac{1}{3} \\ -\frac{1}{3} \end{bmatrix} \tag{5.4}$$

$$\underline{U}_{\text{pseudo}(2)} = \underline{U}_{\text{pseudo}} + \begin{bmatrix} \frac{1}{3} \\ \frac{2}{3} \end{bmatrix} \tag{5.5}$$

$$\underline{U}_{\text{pseudo(3)}} = \underline{U}_{\text{pseudo}} + \begin{bmatrix} -\frac{2}{3} \\ -\frac{1}{3} \end{bmatrix} \tag{5.6}$$

If the active triangle is the right, the centre point voltages can be calculated by

$$\underline{U}_{\text{pseudo(1)}} = \underline{U}_{\text{pseudo}} + \begin{bmatrix} \frac{2}{3} \\ \frac{1}{3} \end{bmatrix} \tag{5.7}$$

$$\underline{U}_{\text{pseudo(2)}} = \underline{U}_{\text{pseudo}} + \begin{bmatrix} -\frac{1}{3} \\ \frac{1}{3} \end{bmatrix} \tag{5.8}$$

$$\underline{U}_{\text{pseudo(3)}} = \underline{U}_{\text{pseudo}} + \begin{bmatrix} -\frac{1}{3} \\ -\frac{2}{3} \end{bmatrix} \tag{5.9}$$

3. Calculation of the complex dot product for current control according to Equation 3.17 in Chapter 3.2.5.

- The use of the outer tolerance band is continued until the generated feed forward voltage selects the same triangle for control as the outer limit. Once this happens, the feed forward control becomes active until the outer tolerance band is triggered the next time.

A simplified circuit diagram of the improved SHC direct current controller combined with the outer tolerance band control is shown in Figure 5.10.

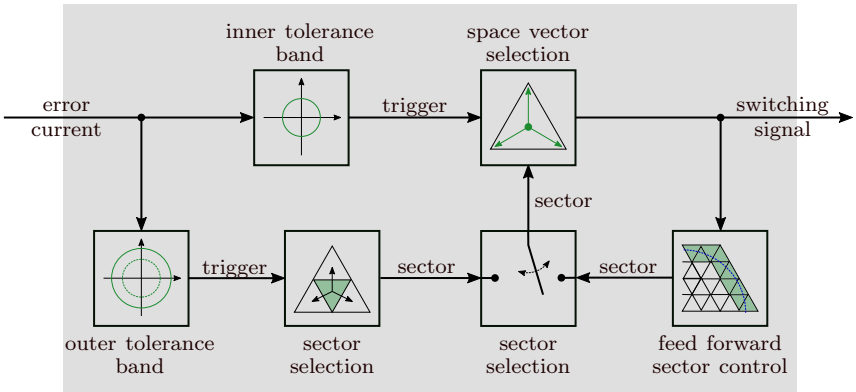


Figure 5.10: Simplified circuit of the proposed improved direct current control system

With this concept, it is possible to combine the advantages of both systems and thus to ensure maximum dynamics and a minimized current error and switching frequency. In order to demonstrate the working behaviour of this system, various simulations with possible dynamic situations will be carried out below.

5.4.1 Grid Voltage Sag

One type of grid fault with high demands on the dynamic reaction of the inverter system are voltage sags. These sags are divided into different types (A to G) according to the number of phases involved or additional phase shifts [7]. The properties of the individual types are explained in more detail in the Appendix C.

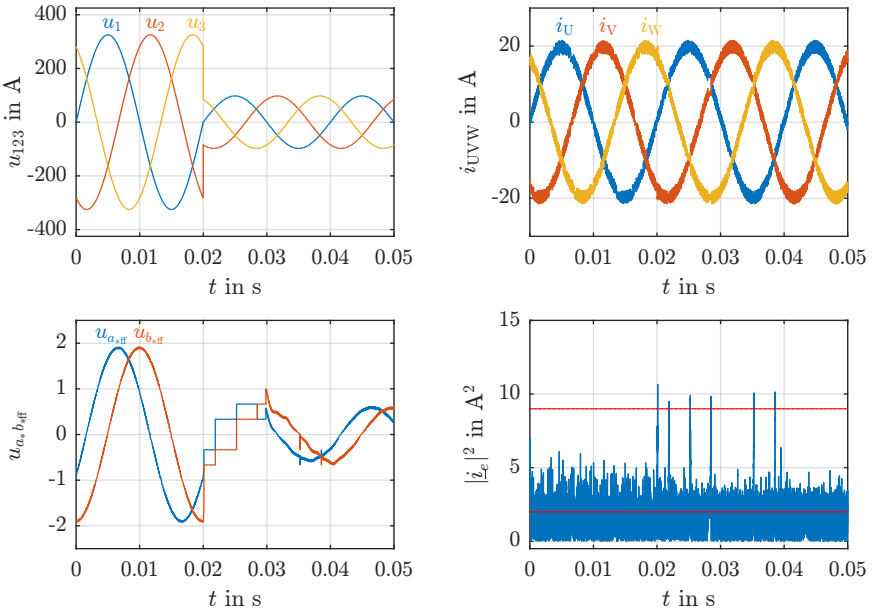


Figure 5.11: Simulation results of three-level NPC reaction on three-phase voltage sag (Type A) to 30 %. Left side: grid voltage and feed forward signal. Right side: grid current and error current.

A three-phase voltage sag (type A) from 100 % to 30 % of the standard grid voltage is used to verify the concept and investigate the working behaviour. The modulation index during the voltage sag, therefore, decreases from 1.08 to 0.33. This corresponds to a change from the sectors of the outer hexagon to the sectors of the inner hexagon of the used three-level inverter system. As a result, the number of sector changes required for operation decreases from 18 to 6 after the sag has occurred. Figure 5.11 shows the reaction of the system during the specified fault case. In the example shown the voltage sag was initiated at time $t = 0.02$ s.

In the three-phase current no deviation can be seen whereas the squared absolute value of the current error shows several violations of the outer tolerance band. The effects of this outer tolerance band violations can be seen in the generated sector control voltage (bottom left). The continuous feed forward voltage filtered by the MSOGI system is immediately replaced by the step-shaped midpoint voltage of the appropriate sector at the time the fault occurs. The outer tolerance band control is active for about 10 ms. After this time, the feed forward voltage is reactivated since both signals detect the same triangular sector. However, as the MSOGI generated voltage is not yet determined exactly, the feed forward voltage is repeatedly switched to the midpoint voltage. This behaviour is indicated by the short peaks in

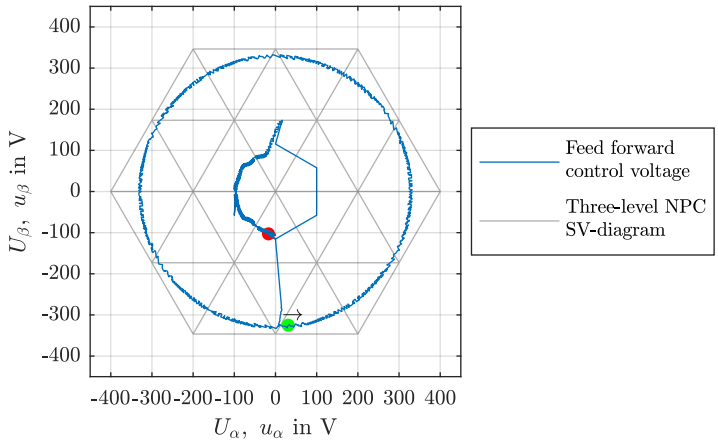


Figure 5.12: Three-level SV-diagram with feed forward voltage for a three-phase voltage sag (Type A) to 30 %

the normalized signal at $t = 0.035$ s and $t = 0.039$ s. After approximately one grid period, the new voltage position is detected accurately enough by the MSOGI and no further violations of the outer tolerance band are necessary to control the current.

Figure 5.12 shows the corresponding trajectory of the generated feed forward voltage in the three-level SV-diagram. The time segment in the diagram corresponds to that from $t = 0$ s (green point) to $t = 0.04$ s (red point) in Figure 5.11. At the time the voltage sag occurs, the feed forward voltage immediately changes the triangular sector. After half a grid period using the outer tolerance band control and thus the centre points of selected triangular sectors in the inner hexagon, the feed forward voltage of the MSOGI reaches the inner sectors and is activated.

5.4.2 Grid Frequency Jump

This test case corresponds to a jump in the grid frequency. Although a frequency jump in the grid is abnormal, the grid standards allow short-term fluctuations [90]. Normally it is distinguished between an integrated or an island grid. For the integrated grid a maximum deviation of $+4\ \%/-6\ \%$ is permitted. This corresponds to a frequency range from 47 Hz to 52 Hz. For an island grid the limits of $\pm 15\ \%$ are acceptable which corresponds to 42,5 Hz to 57,5 Hz. In the following simulation a frequency jump of 10 Hz from 45 Hz to 55 Hz is considered. As before the dynamic change from the feed forward sector selection to the outer tolerance band control for sector selection is shown. Additionally the interaction of the MSOGI and the connected FLL is investigated.

The results of this case are shown in Figure 5.13. The jump in the grid frequency takes place at $t = 0.01$ s. As it can be seen from the error current, no violation of the outer tolerance band occurs at this time. After the phase angles of the actual feed forward voltage with 45 Hz and the real voltage of 55 Hz drift apart the outer limit is reached at approximately $t = 0.012$ s. After a short time the feed forward voltage control is reactivated as both methods are propose the same sector. The two sector control methods are activated several times. The duration in which the triangle midpoint voltage is used reaches its maximum at about $t = 0.02$ s. After this point, the active time decreases due to the adjustment of the feed forward signal. The permanent error caused by the lag of the phase position in the MSOGI leads to a readjustment of the fundamental frequency in the FLL. After approximately 20 ms the detected frequency reaches the new value of 55 Hz

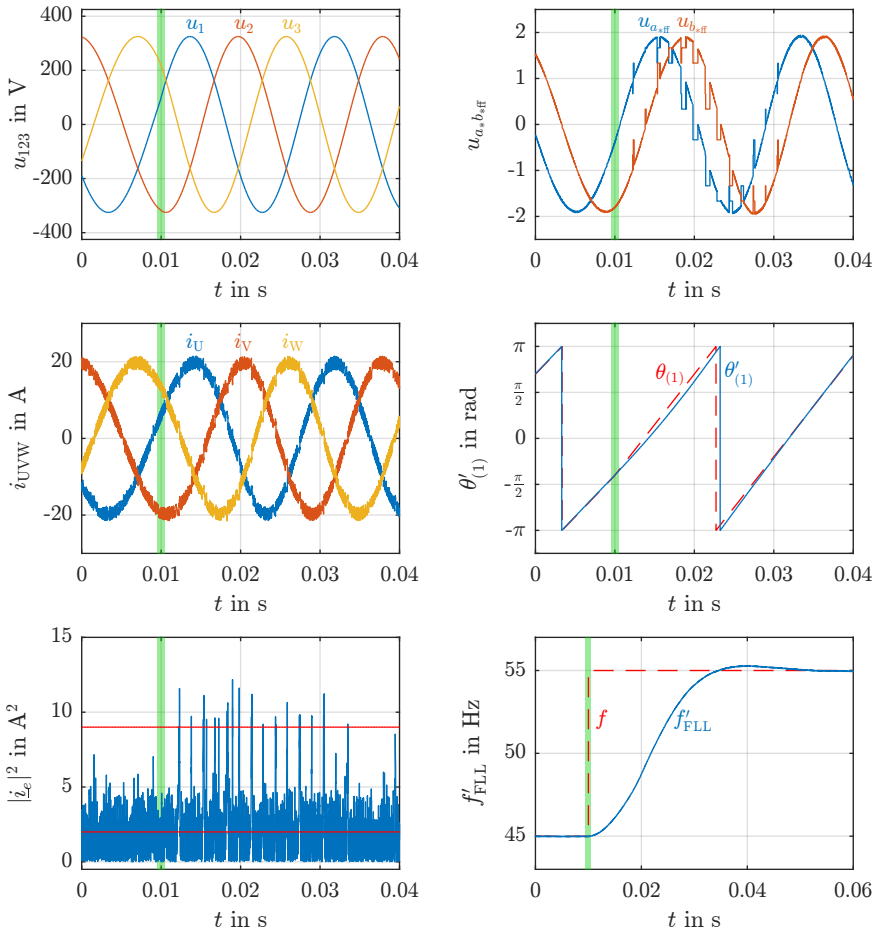


Figure 5.13: Simulation results of three-level NPC reaction on frequency jump from 45 Hz to 55 Hz at $t = 0.01$ s. Left side: grid voltage, output current, error current. Right side: feed forward signal, detected phase angle, detected frequency.

and the inverter system control changes to normal operating mode with correct feed forward control.

5.4.3 Set Current Jump

This test case is used to analyse the reaction of the control system to a jump of the set current. In this test, the set current amplitude was set from 20 A to −20 A at the time $t = 0.01$ s. Figure 5.14 shows the inverter output current, the error current and the sector control voltage in normalized coordinates.

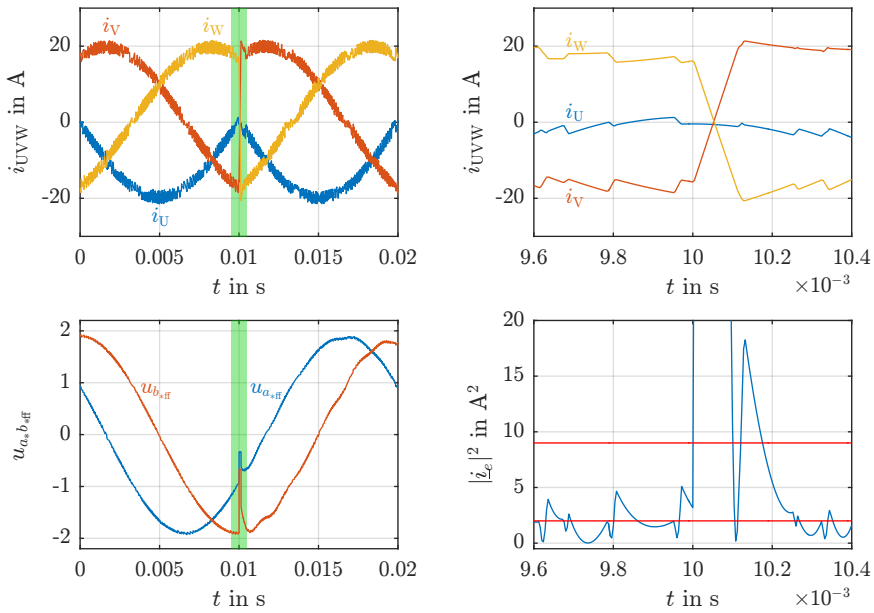


Figure 5.14: Simulation results of three-level NPC reaction on set current jump from 20 A to −20 A. Left side: grid current and feed forward signal. Right side: detail enlargement of grid current and error current.

Immediately after the set point change the error current increases significantly, causing a single sector change. After this no further sector change is triggered as the error is decreasing after the first sector change. After the error current is below the inner tolerance band, the SHC algorithm triggers a new space vector within this sector. However, since the real voltage is in another sector, the SHC can not operate properly, causing the error current to trigger the outer tolerance band at $t = 0.0101$ s. After this the

selected sector is equal to the sector selected by the MSOGI voltage. From this point on, the exact feed forward voltage is used for the sector selection. The path of the sector control voltage is shown in three-level SV-diagram in Figure 5.15.

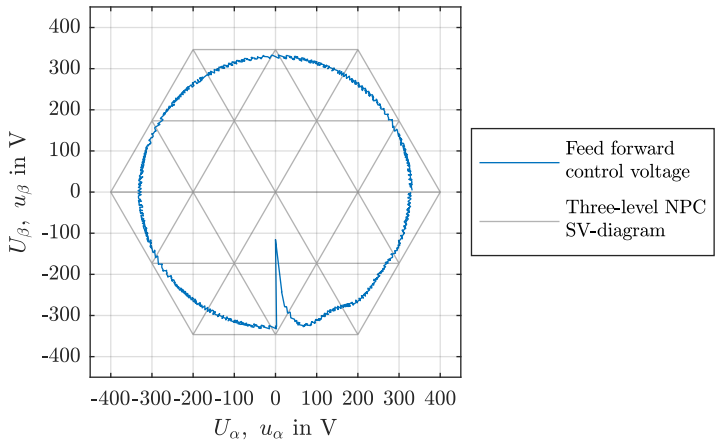


Figure 5.15: Three-level SV-diagram with feed forward voltage for an set current jump from 20 A to −20 A

As one can see, the sector control voltage performs only one sector change at the time the jump occurs. It should be mentioned that the reaction to the set point jump strongly depends on the actual voltage position and the direction of the current jump. This means that the return path after the change to the correct sector may take several intermediate sector-steps depending on the location of the current error. Other controller concepts with multiple tolerance bands could directly jump the other side of the SV-diagram. However, this would lead to a greater overshoot after reaching the end value until the right sector is reached again. The short-term deformation of the feed forward control voltage generated by the MSOGI system after the jump results from the fact that the system under test already monitors and models the switched output voltage with the the harmonic components.

5.4.4 Unbalanced Grid Voltages

This test case investigates the switching behaviour of a five-level inverter system under unbalanced grid conditions. As test condition a single phase voltage sag (type B) from 100 % to 0 % in phase U is simulated. This test condition demonstrates the behaviour of the controller with a continuously changing modulation index. Figure 5.16 shows the five-level SV-diagram and the respective voltages for the space vector selection when using the outer tolerance band or the feed forward control sector selection. The sectors required for accurate control are distributed between the inner and outer hexagons. When using only the outer tolerance band 34 sector changes per grid period are necessary.

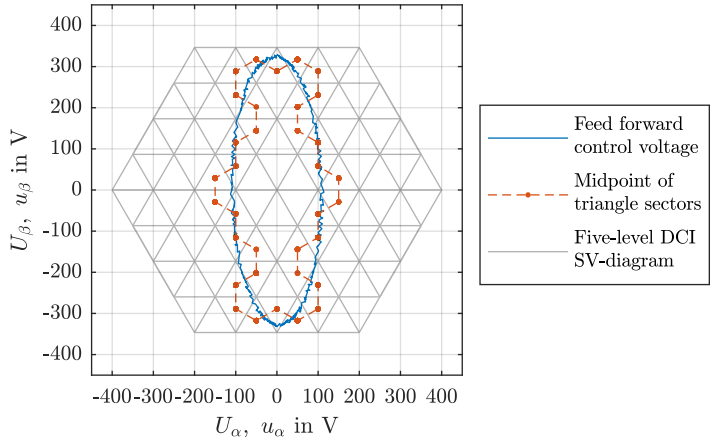


Figure 5.16: Five-level SV-diagram for unbalanced grid condition with feed forward voltage control and midpoint voltage of triangle sectors selected by the outer tolerance band

When using the feed forward sector control method all sectors are accurately detected again. Alternative direct controllers with multiple tolerance bands have to use these additional bands for controlling the current in this unbalanced situation. The inverter output current, error current and sector control voltage for this test case is shown in Figure 5.17. Due to the unbalanced grid voltage condition the switching frequencies of the SHC in the three phases of the inverter are different. Phase U has the highest switching frequency of 1150 Hz. The switching frequencies of the other two phases are

890 Hz for phase V and 940 Hz for Phase W.

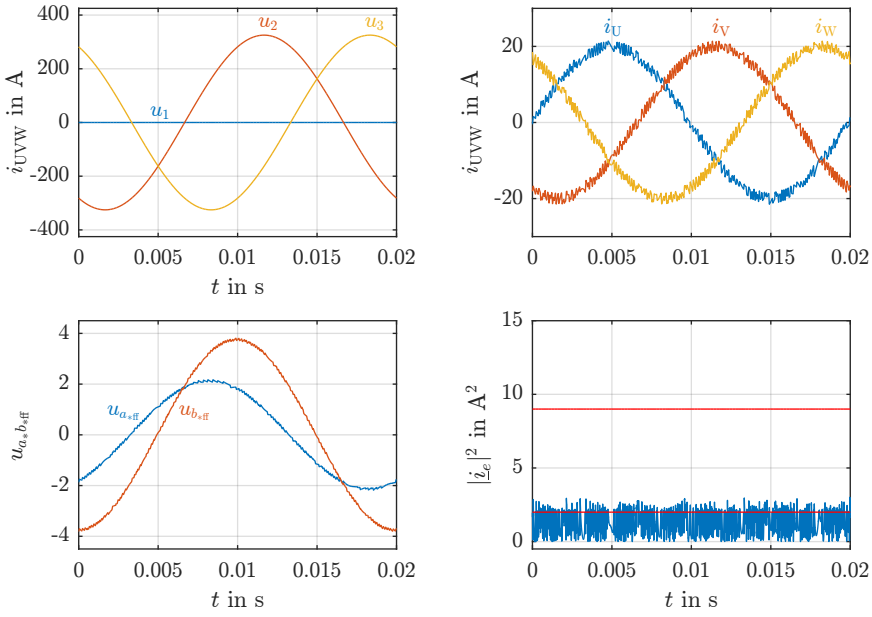


Figure 5.17: Simulation results of five-level DCI reaction on single-phase voltage sag (Type B) to 0 % in phase U. Left side: grid voltage and feed forward signal. Right side: grid current and error current.

5.5 Operational Limitations

During the simulations and tests of the proposed concept, some operating points of the inverter systems showed an unexpected behaviour. In these special cases the outer tolerance band is used for current control although the feed forward voltage is accurately detected. Further investigations of this problem revealed that the output states during the dead-time are causing this special behaviour.

Especially when using a three-level NPC inverter system with a modulation index of 0.52 this special behaviour occurs significantly. At this working point, the average output voltage of the inverter is always located within the inner hexagon but very close to the boundary to the outer. Therefore, the feed forward voltage would always select one of the inner sectors. The resulting current and current error with the standard configuration of this test case are shown in Figure 5.18.

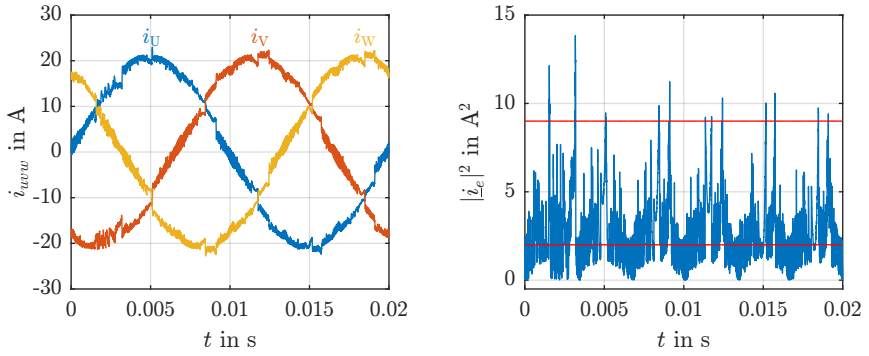


Figure 5.18: Simulation results of three-level NPC at a limited working point. Left: three-phase output current. Right: error current

As one can see the outer tolerance band is often triggered within this working point. Those violations of the outer border cause the current controller to select a sector and thus space vectors of the outer hexagon. This happens even though the average output voltage detected by the feed forward system is correct. Based on this operating point, the origin of this switching behaviour will be explained in more detail with two slightly modified simulation models.

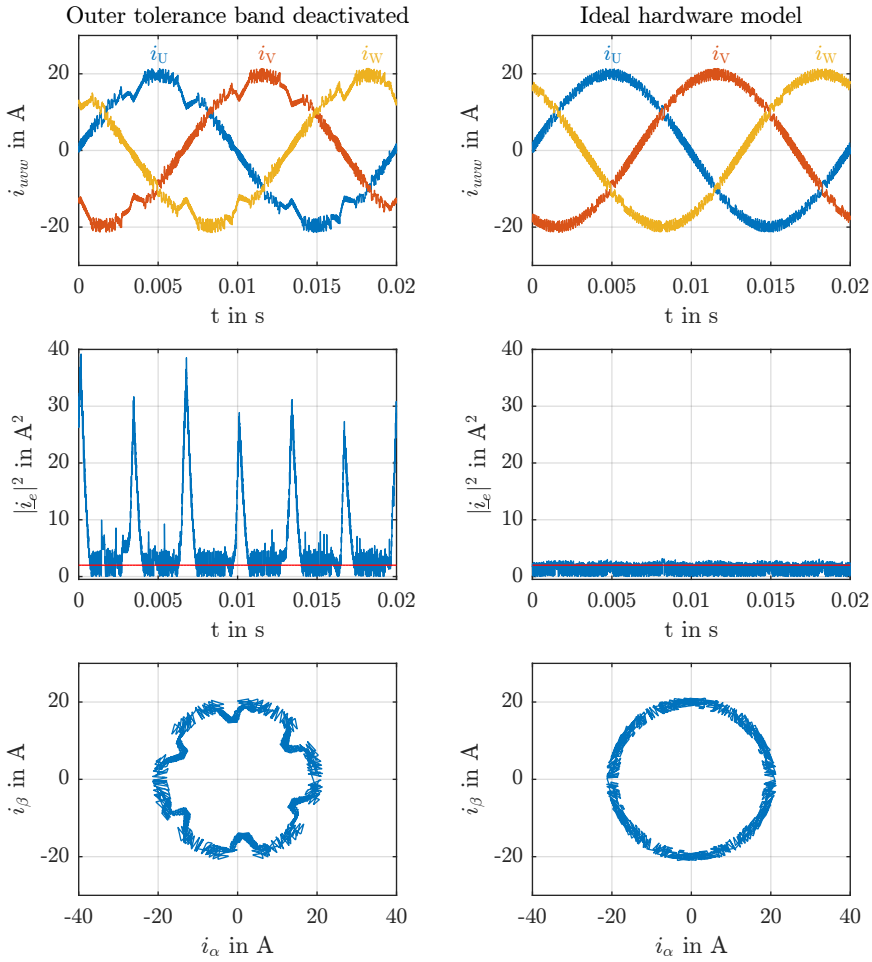


Figure 5.19: Simulation results of modified models with deactivated outer tolerance band (left) and ideal hardware (right)

Within the first variant the outer tolerance band is deactivated leading to the selection of the space vectors of only the inner hexagonal areas for current control. The second variant implements an ideal inverter hardware. This means that no dead-time and thus no intermediate switching states are used. The block-time for the ideal hardware simulation was increased to 6 μs to compensate the dead-time and to get comparable results. The selection

of the triangular sectors for both variants is done with the proposed MSOGI system. The resulting three-phase current, combined square error current value and the output current in the $\alpha\beta$-system are shown in Figure 5.19.

As apparent when the dead-time is set to 0 μs the SHC is able to control the current accurately with only the space vectors of the inner sectors. In contrast to that, when the dead-time is active and the outer tolerance band is deactivated, a significant increase in the current error occurs. This drop in the output current can be recognized at certain points in time. Considering the inner hexagon of the three-level SV-diagram this points correspond to the point where the voltage has reached the centre between two space vectors at the edge of the triangular sector. This special operating point leads to the fact that the two corresponding space vectors show an inverted effect on the α and β components of the output current. This could result in a continuous and rapid switching between those two space vectors depending on the working point. Due to the output voltages during the dead-time, the average output voltage decreases, whereby the current exceeds the inner tolerance band. In this special case, the selected space vectors are not able to compensate this effect. To increase the average output voltage, the SHC needs to select a space vector of an outer sector to correct the real output voltage of the inverter. As the average inverter output voltage would still remain within the inner hexagonal area, the proposed feed forward system

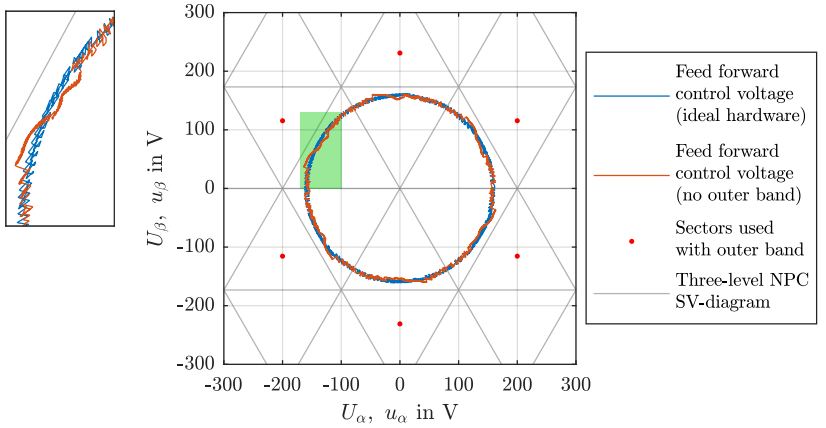


Figure 5.20: Simulation results of detected feed forward voltage and enlarged segment

is not able to indicate the necessary sector changes to an outer sector. The feed forward voltages for the two test cases are shown in Figure 5.20. In addition, the six triangle centre points selected by the outer tolerance band control are highlighted.

The slight drop in the detected feed forward voltage for the variant with deactivated outer tolerance band can also be seen, but since it is always only a single short drop this can not be completely displayed with the used MSOGI configuration.

The occurrence of the described effect depends on several properties of the inverter system, including

- the amplitude of grid voltage and used grid filter. Both properties influence the output voltage and generated $\mathrm{d}i/\mathrm{d}t$ of the available three space vectors of the inverter.
- the level count and DC-link voltage defining the size of the triangular sectors and thus the average time within a triangular sector. The count also decreases the $\mathrm{d}i/\mathrm{d}t$ and the resulting switching frequency.
- the implemented dead-time in the inverter system which has direct impact on the switching duration of intermediate switching states.
- the amplitude and power factor of the set current. This defines the current rise at each point in the SV-diagram.

The described switching behaviour could lead to the selection of the wrong sector as the resulting output voltage is shifted by the selected switching operations during the dead-time. In this situations the generated voltage by the MSOGI system is still correct but not used for sector control. However, in combination with the outer tolerance band a stable control of the output current under these cases is possible.

5.6 Summary

This chapter investigates the proposed feed forward sector control system with several special operating points. The improved switching behaviour is compared with the standard SHC method which uses only the outer tolerance band for sector changes. The simulations show a significant improvement in the working behaviour when using multilevel inverters. Especially, the current error can be significantly reduced when higher level counts are used. Furthermore, the reaction of the system to grid fault cases are investigated. For this purpose, the feed forward control system was combined with the outer tolerance band control in a way that all dynamic errors can be applied. By using the proposed selection process for the sector, the advantages of both systems in steady and dynamic operation can be optimally combined.

Chapter 6

Grid Synchronization and Power Control

Almost all grid connected inverters have the purpose to feed active power into the grid or extract active power from the grid. To achieve this goal the output currents of the inverter $\underline{i}$ have to be in phase with the grid voltage $\underline{u}$ to extract active power or phase shifted by 180° to feed active power. In the previous chapters the average inverter output voltage $\underline{u}_{\mathrm{ff}}$ was determined to select both the correct triangular sector as well as the current error reducing space vector. However, in grid applications the knowledge of the exact voltage $\underline{u}$ at the point of common coupling (PCC) is important. Figure 6.1 shows the simplified circuit of a grid connected inverter system with an L-filter. The voltage source $\underline{u}_{\mathrm{ff}}$ represents the average output voltage of the inverter .

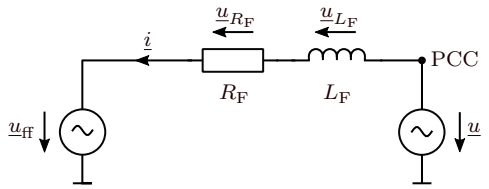


Figure 6.1: Simplified equivalent circuit of a grid connected inverter system in $\alpha\beta$ representation

The equation of the grid voltage is, therefore, defined by

$$\underline{u} = \underline{u}_{\mathrm{ff}} + \underline{u}_{R_\mathrm{F}} + \underline{u}_{L_\mathrm{F}} = \underline{u}_{\mathrm{ff}} + R_\mathrm{F} \cdot \underline{i} + j \cdot \omega \cdot L_\mathrm{F} \cdot \underline{i} \tag{6.1}$$

Knowing the grid voltage $\underline{u}$ would allow an exact calculation of the inverter set current to control the active power p and reactive power q at the

PCC. However $\underline{u}$ is not known, but by compensating the voltage drop across the L-filter components it can be determined. Thus, unintentional phase shifts between the output current and the grid voltage can be avoided. This voltage drop has a resistive component $\underline{u}_{R_\mathrm{F}}$ and an inductive component $\underline{u}_{L_\mathrm{F}}$ which depends on the amplitude and direction of the phase currents. The relationship between the inverter output voltage $\underline{u}_\mathrm{ff}$ and grid voltage $\underline{u}$ is shown in Equation 6.1 and shown in the vector diagram in Figure 6.2 for example of the current $\underline{i}$ being in phase with $\underline{u}$.

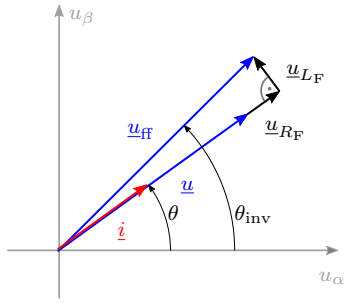


Figure 6.2: Relationship of generated feed forward voltage and grid voltage for pure active current

In the following section three different calculation methods to determine the set current for power control are presented. Depending on the application of the inverter system, different requirements especially during a grid fault need to be considered. In addition to the set current calculation with the different power control strategies, a simple compensation method for the filter components using the symmetrical components is presented.

Power Control in $\alpha\beta$-System

The simplest way to determine the set currents for controlling the instantaneous active and reactive power (IARC) is to calculate the power in the $\alpha\beta$-system [93]. Starting from the Equations 3.9 and 3.10, the matrix to calculate the active and reactive power in a three-phase three-wire system is given by

$$\begin{bmatrix} p \\ q \end{bmatrix} = \frac{3}{2} \cdot \underbrace{\begin{bmatrix} u_\alpha & u_\beta \\ u_\beta & -u_\alpha \end{bmatrix}}_{\boldsymbol{M}_{\mathrm{IARC}}} \cdot \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{6.2}$$

Inverting and rearranging the Equation 6.2, the set currents for the direct current controller can be calculated by

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = \frac{2}{3} \cdot \boldsymbol{M}_{\mathrm{IARC}}^{-1} \cdot \begin{bmatrix} p^* \\ q^* \end{bmatrix} = \frac{2}{3} \cdot \frac{1}{u_\alpha^2 + u_\beta^2} \cdot \begin{bmatrix} u_\alpha & u_\beta \\ u_\beta & -u_\alpha \end{bmatrix} \cdot \begin{bmatrix} p^* \\ q^* \end{bmatrix} \tag{6.3}$$

The simulation results using the IARC strategy combined with the improved SHC structure and a three-level NPC inverter system are shown in Figure 6.3. At time $t = 0.01$ s, the set value for the active power p^* is increased from 0 to 10 kW. Under normal grid conditions this corresponds to a current amplitude of approximately 20 A, same as in the previous chapters. From $t = 0.03$ s to $t = 0.05$ s the set value of the reactive power q^* is set to 5 kvar. As it can be seen, all changes of the set points lead to an immediate reaction of the direct current controller. In these cases the outer tolerance band is exceeded only once. Since the average inverter output voltage changes slightly as a result of the changed output current (Equation 6.1), the outer tolerance band may be triggered due to the subsequent grid period.

To show the working behaviour during an unbalanced grid fault, a type B voltage sag from 100 % to 30 % in phase U was simulated from $t = 0.08$ s to $t = 0.12$ s. The short deviation in the active and reactive power at the beginning and at the end of the sag is caused by the settling time of the MSOGI system. After reaching the correct voltage the active and reactive power are controlled correctly again. However, the unbalanced grid voltage and the power calculation in the $\alpha\beta$-system lead to phase currents that show harmonic distortions and a significantly increased amplitude. The current controller itself is always able to follow each set current form as long as the

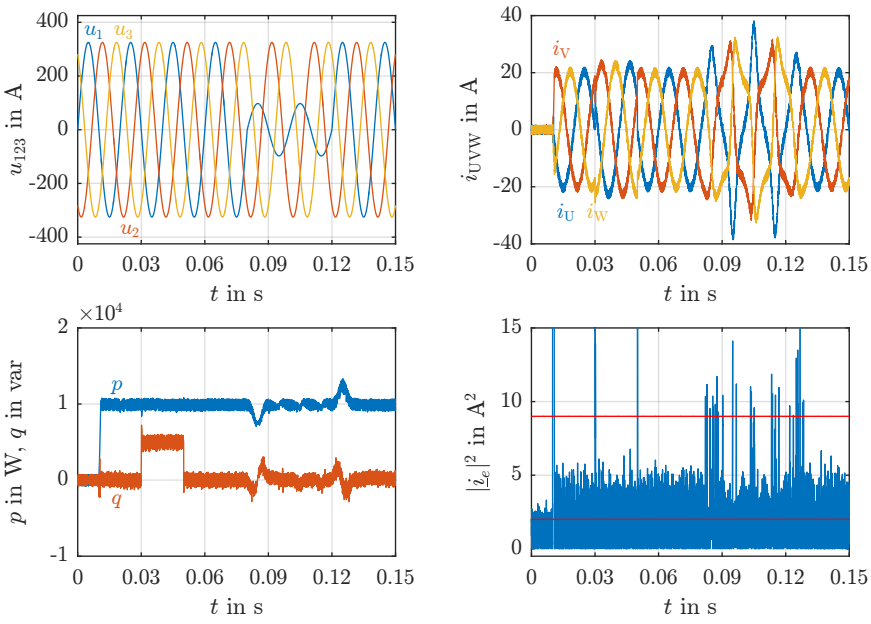


Figure 6.3: Simulation results of realized power control with IARC. Left side: grid voltage and active and reactive power. Right side: grid current and error current.

sum of the set currents in the three-phase system is zero. This working behaviour maintains the power but could lead to a violation of the harmonic limits defined by the grid standards. In order to ensure undistorted sinusoidal currents even under unbalanced grid conditions, the power calculation is often carried out using the symmetrical components.

6.1 Symmetrical Components

The concept of the symmetrical components was first introduced by Fortescue in 1918 [94]. The main property of the proposed system is the possibility to transform an unbalanced m-phase system into $m-1$ balanced m-phase systems and one additional zero-system with m phases having identical magnitudes and phase angles [95]. With the help of this representation, system fault conditions can be easier visualized, analysed and calculated.

Considering the standard grid with its three-phase system, two balanced systems which are known as positive and negative sequence and the zero system can be set up using this theory [96]. The components of the positive, negative and zero sequence can thereby calculated by

$$\begin{bmatrix} u_{1(1)} \\ u_{2(1)} \\ u_{3(1)} \end{bmatrix} = \boldsymbol{T}_{(1)} \cdot \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} = \frac{1}{3} \cdot \begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix} \cdot \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} \tag{6.4}$$

$$\begin{bmatrix} u_{1(2)} \\ u_{2(2)} \\ u_{3(2)} \end{bmatrix} = \boldsymbol{T}_{(2)} \cdot \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} = \frac{1}{3} \cdot \begin{bmatrix} 1 & a^2 & a \\ a & 1 & a^2 \\ a^2 & a & 1 \end{bmatrix} \cdot \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} \tag{6.5}$$

$$\begin{bmatrix} u_{1(0)} \\ u_{2(0)} \\ u_{3(0)} \end{bmatrix} = \boldsymbol{T}_{(0)} \cdot \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} = \frac{1}{3} \cdot \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} \tag{6.6}$$

where $a = e^{j2\pi/3}$ is the rotation operator. The sum of those components leads to the three-phase grid voltage.

$$u_{123} = u_{123(0)} + u_{123(1)} + u_{123(2)} \tag{6.7}$$

To avoid additional calculation effort within the proposed controller system the transformations are converted into the $\alpha\beta$-system. The positive and negative sequence are given by

$$\begin{bmatrix} u_{\alpha(1)} \\ u_{\beta(1)} \end{bmatrix} = \boldsymbol{T}_{\alpha\beta(1)} \cdot \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \boldsymbol{T}_{\alpha\beta} \cdot \boldsymbol{T}_{(1)} \cdot \boldsymbol{T}_{\alpha\beta}^{-1} \cdot \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \frac{1}{2} \cdot \begin{bmatrix} 1 & -\mathrm{q} \\ \mathrm{q} & 1 \end{bmatrix} \cdot \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} \tag{6.8}$$

$$\begin{bmatrix} u_{\alpha(2)} \\ u_{\beta(2)} \end{bmatrix} = \boldsymbol{T}_{\alpha\beta(2)} \cdot \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \boldsymbol{T}_{\alpha\beta} \cdot \boldsymbol{T}_{(2)} \cdot \boldsymbol{T}_{\alpha\beta}^{-1} \cdot \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \frac{1}{2} \cdot \begin{bmatrix} 1 & \mathrm{q} \\ -\mathrm{q} & 1 \end{bmatrix} \cdot \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} \tag{6.9}$$

where $\mathrm{q} = e^{-j\pi/2}$. As only the three-phase three-wire system is considered the zero sequence can be neglected for the following power control strategies. Considering the basic structure of the SOGI band-pass with its two integrators (Figure 4.3) the phase shifted values are already calculated after the second integrator and multiplier stage when the input signal u is a sinusoidal signal with the angular frequency ω' [97]. Thus the voltage $\underline{u}_{\mathrm{ff}}$ and $\underline{u}_{\mathrm{qff}}$ can be used for the transformation. This leads to a simple extension of the proposed concept to calculate the average inverter output voltage in the positive and negative sequence.

6.1.1 Filter Compensation

As shown in Figure 6.2 it is necessary to compensate the resistive and the phase-shifted inductive voltage component of the filter in order to calculate the grid voltage at the grid connection point. Based on the symmetrical components, a compensation method with low mathematical effort and with no need to filter or to differentiate the measured inverter output current is presented in the following.

Filter Compensation in Positive Sequence

To calculate the positive sequence of the inverter output voltage the feed forward voltage $\underline{u}_{1\mathrm{ff}}$ and its phase shifted component $\underline{u}_{\mathrm{q}1\mathrm{ff}}$ are used. To avoid harmonic distortions only the detected fundamental component of the voltage is used. The resulting equation is given by

$$\begin{bmatrix} u_{\alpha(1)\mathrm{ff}} \\ u_{\beta(1)\mathrm{ff}} \end{bmatrix} = \frac{1}{2} \cdot \begin{bmatrix} 1 & -\mathrm{q} \\ \mathrm{q} & 1 \end{bmatrix} \cdot \begin{bmatrix} u_{\alpha 1\mathrm{ff}} \\ u_{\beta 1\mathrm{ff}} \end{bmatrix} \tag{6.10}$$

The equation to calculate the positive sequence of the grid voltage $u_{\alpha\beta(1)}$ using an inductive filter is, therefore, given by

$$\begin{bmatrix} u_{\alpha(1)} \\ u_{\beta(1)} \end{bmatrix} = \begin{bmatrix} u_{\alpha(1)\mathrm{ff}} \\ u_{\beta(1)\mathrm{ff}} \end{bmatrix} + R_{\mathrm{F}} \cdot \begin{bmatrix} i_{\alpha(1)} \\ i_{\beta(1)} \end{bmatrix} + L_{\mathrm{F}} \cdot \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{\alpha(1)} \\ i_{\beta(1)} \end{bmatrix} \tag{6.11}$$

The main difficulty with this equation is the derivative of the output current $i_{\alpha\beta}$. To avoid this step the following simplifications are done:

- The load current $i_{\alpha\beta}$ of a direct current controlled inverter can be assumed to be the set current $i^*_{\alpha\beta}$.

- All phase currents of the positive sequence are symmetrical and have identical and constant amplitudes and phases.

Due to these simplifications, the following relationship can be made to avoid the derivation of the current:

$$\begin{aligned} \frac{\mathrm{d}}{\mathrm{d}t}(i^*_{\alpha(1)} + j \cdot i^*_{\beta(1)}) &= \frac{\mathrm{d}}{\mathrm{d}t}\left(I^*_{(1)} e^{j\omega t}\right) = j \cdot \omega \cdot I^*_{(1)} e^{j\omega t} \\ \frac{\mathrm{d}i^*_{\alpha(1)}}{\mathrm{d}t} + j \cdot \frac{\mathrm{d}i^*_{\beta(1)}}{\mathrm{d}t} &= -\omega \cdot i^*_{\beta(1)} + j \cdot \omega \cdot i^*_{\alpha(1)} \end{aligned} \tag{6.12}$$

From the relationship of real and imaginary part from Equation 6.12 the following expression to replace the derivation of the current can be made:

$$\frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i^*_{\alpha(1)} \\ i^*_{\beta(1)} \end{bmatrix} = \omega \cdot \begin{bmatrix} -i^*_{\beta(1)} \\ i^*_{\alpha(1)} \end{bmatrix} \tag{6.13}$$

which leads to the following equation to calculate the grid voltage.

$$\begin{bmatrix} u_{\alpha(1)} \\ u_{\beta(1)} \end{bmatrix} = \begin{bmatrix} u_{\alpha(1)\mathrm{ff}} \\ u_{\beta(1)\mathrm{ff}} \end{bmatrix} + R_\mathrm{F} \cdot \begin{bmatrix} i^*_{\alpha(1)} \\ i^*_{\beta(1)} \end{bmatrix} + \omega' \cdot L_\mathrm{F} \cdot \begin{bmatrix} -i^*_{\beta(1)} \\ i^*_{\alpha(1)} \end{bmatrix} \tag{6.14}$$

For the required angular frequency ω the angular frequency ω' detected by the FLL is used.

Filter Compensation in Negative Sequence

The filter compensation in the negative sequence can be realized in a similar way. The first step is the transformation of the fundamental component of the feed forward voltage to the negative sequence using Equation 6.9.

$$\begin{bmatrix} u_{\alpha(2)\mathrm{ff}} \\ u_{\beta(2)\mathrm{ff}} \end{bmatrix} = \frac{1}{2} \cdot \begin{bmatrix} 1 & -\mathrm{q} \\ \mathrm{q} & 1 \end{bmatrix} \cdot \begin{bmatrix} u_{\alpha 1\mathrm{ff}} \\ u_{\beta 1\mathrm{ff}} \end{bmatrix} \tag{6.15}$$

With the negative sequence of the feed forward voltage the equation for the negative sequence of the grid can be set up.

$$\begin{bmatrix} u_{\alpha(2)} \\ u_{\beta(2)} \end{bmatrix} = \begin{bmatrix} u_{\alpha(2)\mathrm{ff}} \\ u_{\beta(2)\mathrm{ff}} \end{bmatrix} + R_\mathrm{F} \cdot \begin{bmatrix} i_{\alpha(2)} \\ i_{\beta(2)} \end{bmatrix} + L_\mathrm{F} \cdot \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{\alpha(2)} \\ i_{\beta(2)} \end{bmatrix} \tag{6.16}$$

As introduced before the following relationship for the set currents can be done. At this step the reversed phase order of the negative sequence needs to be considered.

$$\begin{aligned}\frac{\mathrm{d}}{\mathrm{d}t}(i^*_{\alpha(2)} + j \cdot i^*_{\beta(2)}) =& \frac{\mathrm{d}}{\mathrm{d}t}\left(I^*_{(2)} e^{-j\omega t}\right) = -j \cdot \omega \cdot I^*_{(2)} e^{j\omega t} \\ \frac{\mathrm{d}i^*_{\alpha(2)}}{\mathrm{d}t} + j \cdot \frac{\mathrm{d}i^*_{\beta(2)}}{\mathrm{d}t} =& \omega \cdot i^*_{\beta(2)} - j \cdot \omega \cdot i^*_{\alpha(2)}\end{aligned} \tag{6.17}$$

Based on this relationship the derivative of the current in the negative sequence can be replaced with

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i^*_{\alpha(2)} \\ i^*_{\beta(2)} \end{bmatrix} = \omega \cdot \begin{bmatrix} i^*_{\beta(2)} \\ -i^*_{\alpha(2)} \end{bmatrix} \tag{6.18}$$

Combining this in Equation 6.16 results in

$$\begin{bmatrix} u_{\alpha(2)} \\ u_{\beta(2)} \end{bmatrix} = \begin{bmatrix} u_{\alpha(2)\mathrm{ff}} \\ u_{\beta(2)\mathrm{ff}} \end{bmatrix} + R_\mathrm{F} \cdot \begin{bmatrix} i^*_{\alpha(2)} \\ i^*_{\beta(2)} \end{bmatrix} + \omega' \cdot L_\mathrm{F} \cdot \begin{bmatrix} i^*_{\beta(2)} \\ -i^*_{\alpha(2)} \end{bmatrix} \tag{6.19}$$

6.1.2 Power Control with Symmetrical Components

Power Control with Positive Sequence

One possibility to realize a power control using the symmetrical components is called balanced positive-sequence control (BPSC) [8]. Basis for this control strategy are the same equations as for the IARC concept. But instead of the grid voltage in the $\alpha\beta$-system the positive sequence of the grid voltage is used. Accordingly the equations for the active and reactive power in the positive sequence can be set up by

$$p_{(1)} = u_{\alpha(1)} \cdot i_{\alpha(1)} + u_{\beta(1)} \cdot i_{\beta(1)} \tag{6.20}$$

$$q_{(1)} = u_{\beta(1)} \cdot i_{\alpha(1)} - u_{\alpha(1)} \cdot i_{\beta(1)} \tag{6.21}$$

This leads to the following calculation matrix for the active and reactive power.

$$\begin{bmatrix} p_{(1)} \\ q_{(1)} \end{bmatrix} = \frac{3}{2} \cdot \underbrace{\begin{bmatrix} u_{\alpha(1)} & u_{\beta(1)} \\ u_{\beta(1)} & -u_{\alpha(1)} \end{bmatrix}}_{\boldsymbol{M}_{\mathrm{BPSC}}} \cdot \begin{bmatrix} i_{\alpha(1)} \\ i_{\beta(1)} \end{bmatrix} \tag{6.22}$$

Rearranging the equation leads to the following equation to calculate the set values.

$$\begin{aligned} \begin{bmatrix} i^*_{\alpha} \\ i^*_{\beta} \end{bmatrix} = \begin{bmatrix} i^*_{\alpha(1)} \\ i^*_{\beta(1)} \end{bmatrix} &= \frac{2}{3} \cdot \boldsymbol{M}^{-1}_{\mathrm{BPSC}} \cdot \begin{bmatrix} p^*_{(1)} \\ q^*_{(1)} \end{bmatrix} \\ &= \frac{2}{3} \cdot \frac{1}{u^2_{\alpha(1)} + u^2_{\beta(1)}} \cdot \begin{bmatrix} u_{\alpha(1)} & u_{\beta(1)} \\ u_{\beta(1)} & -u_{\alpha(1)} \end{bmatrix} \cdot \begin{bmatrix} p^*_{(1)} \\ q^*_{(1)} \end{bmatrix} \end{aligned} \tag{6.23}$$

A simplified schematic of the BPSC method combined with the sensorless inverter output voltage detection system is shown in Figure 6.4. In this figure the MSOGI-FLL is represented as one block. Besides the MSOGI and FLL this block contains the Clarke transformation of the calculated inverter output voltage u_{UVW} and the calculation of the feed forward voltage $\underline{u}_{\mathrm{ff}}$ and its phase shifted version $\underline{u}_{\mathrm{qff}}$.

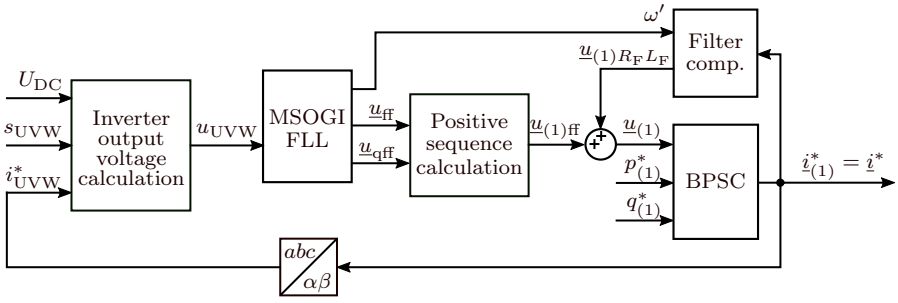


Figure 6.4: Simplified schematic of BPSC method combined with the inverter output voltage detection system

The algebraic loop created by the simplified filter compensation is resolved by the implementation in the FPGA. Because calculations of voltage at the inductive and resistive part of the filter $\underline{u}_{(1)R_{\mathrm{F}}L_{\mathrm{F}}}$ require several clock cycles, a delayed value of the voltage drop at the filter is generated and added to $\underline{u}_{(1)\mathrm{ff}}$. Due to the high clock speed of the FPGA of 40 MHz compared to the rate of change of the grid voltage the resulting error in $\underline{u}_{(1)}$ can be neglected.

The simulation results using the BPSC power control strategy are shown in Figure 6.5. The grid properties and the set values for the active and reactive power are the same as before.

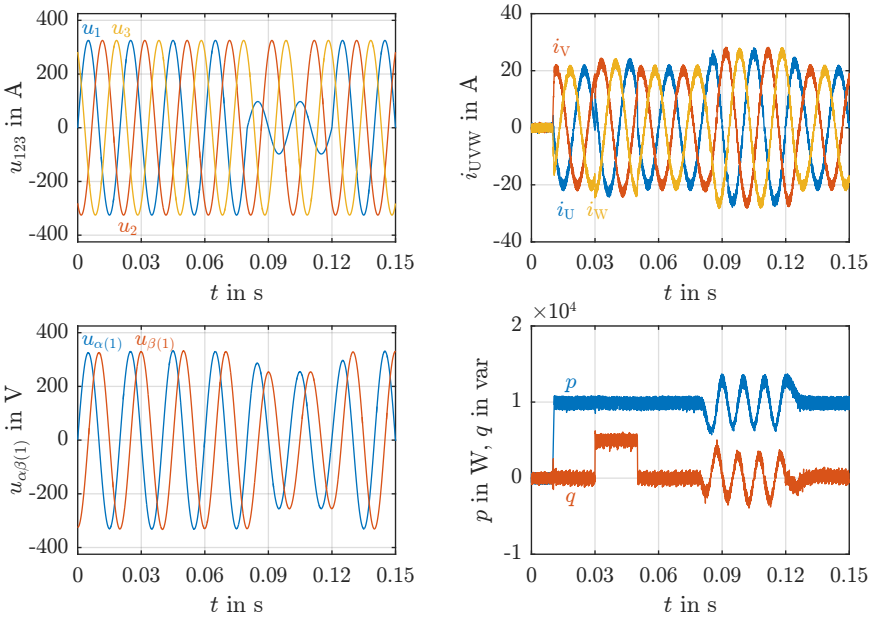


Figure 6.5: Simulation results of realized BPSC power control. Left side: grid voltage and detected positive sequence. Right side: grid current and active and reactive power.

Under normal grid conditions the working behaviour of the BPSC method is the same as the IARC. However, when a grid unbalance occurs, the difference is clearly visible. Since the positive sequence voltage is used for the calculation, the set current is always sinusoidal and symmetrical. Due to the reduced positive sequence voltage amplitude during the type B fault, the set current increases but remains smaller as with the IARC concept. The balanced phase currents during the unbalanced fault cause the active and reactive power to oscillate with double fundamental frequency. The average value of the active and reactive power is always the set value.

Power Control with Positive and Negative Sequence

To avoid the power oscillations of the BPSC method, the calculation of the set currents for the SHC are extended by the negative sequence as shown in [98]. According to this, the behaviour of the active and reactive power including the oscillations during the unbalanced fault can be described by

$$p = P_{\text{avg}} + P_{\text{c2}} \cos(2\omega t) + P_{\text{s2}} \sin(2\omega t) \tag{6.24}$$

$$q = Q_{\text{avg}} + Q_{\text{c2}} \cos(2\omega t) + Q_{\text{s2}} \sin(2\omega t) \tag{6.25}$$

where P_{avg} and Q_{avg} are the average values of the active and reactive power. The active power components P_{c2} and P_{s2} and reactive power components Q_{c2} and Q_{s2} represent the amplitude of the oscillations with double fundamental frequency. Using the positive and negative sequence voltages and currents the following calculation matrix can be established [98].

$$\begin{bmatrix} P_{\text{avg}} \\ P_{\text{c2}} \\ P_{\text{s2}} \\ Q_{\text{avg}} \\ Q_{\text{c2}} \\ Q_{\text{s2}} \end{bmatrix} = \frac{3}{2} \cdot \begin{bmatrix} u_{\alpha(1)} & u_{\beta(1)} & u_{\alpha(2)} & u_{\beta(2)} \\ u_{\alpha(2)} & u_{\beta(2)} & u_{\alpha(1)} & u_{\beta(1)} \\ u_{\beta(2)} & -u_{\alpha(2)} & -u_{\beta(1)} & u_{\alpha(1)} \\ u_{\beta(1)} & -u_{\alpha(1)} & u_{\beta(2)} & -u_{\alpha(2)} \\ u_{\beta(2)} & -u_{\alpha(2)} & u_{\beta(1)} & -u_{\alpha(1)} \\ -u_{\alpha(2)} & -u_{\beta(2)} & u_{\alpha(1)} & u_{\beta(1)} \end{bmatrix} \cdot \begin{bmatrix} i_{\alpha(1)} \\ i_{\beta(1)} \\ i_{\alpha(2)} \\ i_{\beta(2)} \end{bmatrix} \tag{6.26}$$

To calculate the set currents, this matrix must be inverted. It should be noted that this is not possible since the matrix has the dimensions 6x4. For this reason, two power components must be removed from the equation to create a 4x4 matrix. As the aim of the control strategy is to avoid active power oscillations, the reactive power components Q_{c2} and Q_{s2} are removed. This leads to Equation 6.27 which is used by the positive and negative sequence control (PNSC) method [8].

$$\begin{bmatrix} P^*_{\text{avg}} \\ P^*_{\text{c2}} \\ P^*_{\text{s2}} \\ Q^*_{\text{avg}} \end{bmatrix} = \frac{3}{2} \cdot \underbrace{\begin{bmatrix} u_{\alpha(1)} & u_{\beta(1)} & u_{\alpha(2)} & u_{\beta(2)} \\ u_{\alpha(2)} & u_{\beta(2)} & u_{\alpha(1)} & u_{\beta(1)} \\ u_{\beta(2)} & -u_{\alpha(2)} & -u_{\beta(1)} & u_{\alpha(1)} \\ u_{\beta(1)} & -u_{\alpha(1)} & u_{\beta(2)} & -u_{\alpha(2)} \end{bmatrix}}_{\boldsymbol{M}_{\text{PNSC}}} \cdot \begin{bmatrix} i^*_{\alpha(1)} \\ i^*_{\beta(1)} \\ i^*_{\alpha(2)} \\ i^*_{\beta(2)} \end{bmatrix} \tag{6.27}$$

With the 4x4 matrix, the set current can be calculated by

$$\begin{bmatrix} i^*_{\alpha(1)} \\ i^*_{\beta(1)} \\ i^*_{\alpha(2)} \\ i^*_{\beta(2)} \end{bmatrix} = \frac{2}{3} \cdot \boldsymbol{M}^{-1}_{\mathrm{PNSC}} \cdot \begin{bmatrix} P^*_{\mathrm{avg}} \\ P^*_{\mathrm{c2}} \\ P^*_{\mathrm{s2}} \\ Q^*_{\mathrm{avg}} \end{bmatrix} \tag{6.28}$$

Now, the set current for the SHC in the $\alpha\beta$-system can be calculated as the sum of the positive and negative sequence components.

$$i^*_{\alpha} = i^*_{\alpha(1)} + i^*_{\alpha(2)} \tag{6.29}$$

$$i^*_{\beta} = i^*_{\beta(1)} + i^*_{\beta(2)} \tag{6.30}$$

A simplified schematic of the PNSC method combined with the sensorless inverter output voltage detection system is shown in Figure 6.6.

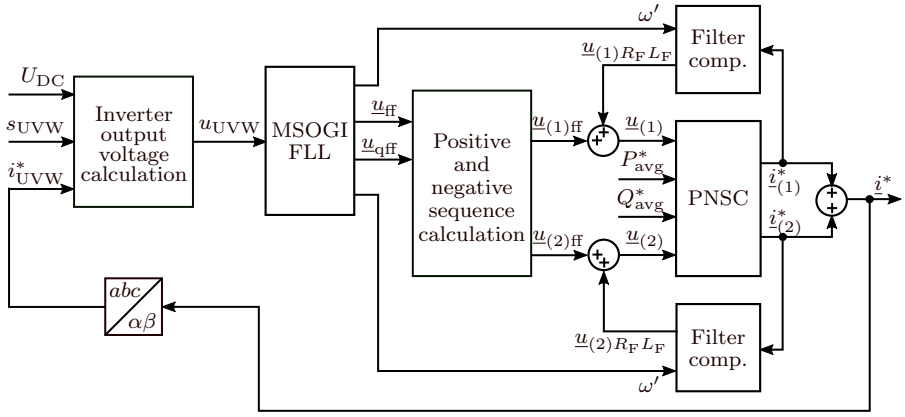


Figure 6.6: Simplified schematic of BPSC method combined with the inverter output voltage detection system

The simulation results for the PNSC method combined with the proposed current controller concept are shown in Figure 6.7. The set values for the active and reactive power and the grid condition are the same as before. The set values for the oscillating active power components P_{c2} and P_{s2} are set to zero.

As one can see the behaviour under standard conditions is identical to the two previously presented power control strategies. As expected the be-

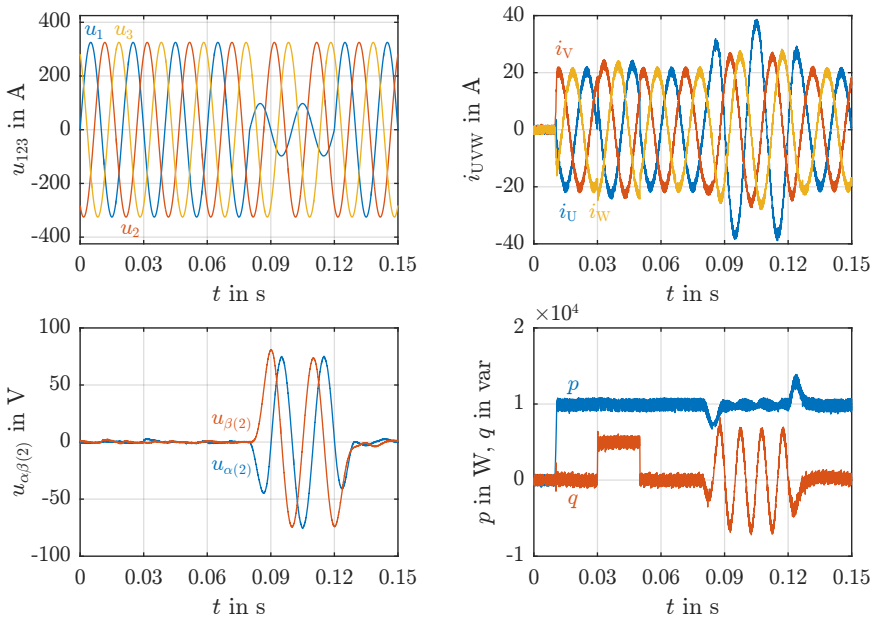


Figure 6.7: Simulation results of realized PNSC power control. Left side: grid voltage and detected negative sequence. Right side: grid current and active and reactive power.

haviour under unbalanced grid conditions is different and the active power is controlled without oscillations. In contrast, the reactive power has significantly higher oscillations. This behaviour guarantees a stable DC-link voltage under unbalanced grid conditions. In order to stabilize the active power, the phase current in the phase which is affected by the voltage sag increases compared to the others. Since the sum of the three-phase currents must be zero a phase shift of the output currents occurs. The negative sequence voltage only occurs during unbalanced grid conditions.

Alternatively, the same calculation principle can also be implemented for a constant reactive power during the unbalanced condition. In this case, the oscillating active power components P_{c2} and P_{s2} need to be removed from Equation 6.26.

6.2 Summary

This chapter shows three different methods for controlling the active and reactive power at the PCC of the inverter. Depending on the intended purpose of the inverter system, the direct current controller concept proposed in this thesis can be easily extended by one of the three power control methods. In combination with the sector feed forward control presented in Chapter 4 and the improved direct current controller based on the SHC presented in Chapter 5 a control system can be build up showing excellent behaviour in dynamic and steady state operation. In addition to the power control a simple method to calculate the grid voltage using the symmetrical components and without additional effort for filtering and differentiating the output current was presented.

The simulations show that all three power control methods show identical behaviour under standard grid conditions. Differences occur during unbalanced grid conditions. The differences in the output current and power under these faults are summarized in the following table.

Table 6.1: Working behaviour of different active and reactive power calculations under unbalanced grid conditions

	IARC	BPSC	PNSC
Balanced phase currents	no	yes	no
Harmonic distorted currents	yes	no	no
Active power oscillations	no	yes	no
Reactive power oscillations	no	yes	yes

Chapter 7

Experimental Verification

In the following chapter the working behaviour of the proposed system is investigated on a hardware test bench. Several measurements are carried out to prove and validate the concept of the improved control system.

7.1 Test Bench and System Parameters

The structure of the test bench in the laboratory is shown in Figure 7.1. To emulate the grid a bidirectional three-phase AC-source (grid simulator) is used. This device is able to add harmonic components to the voltage, to emulate faults like voltage sags and to vary the frequency. Like in the simulations in Chapter 5 a first order L-filter is used. A three-phase three-level NPC system and a three-phase five-level DCI system are used as hardware topologies for testing. On the DC-side up to four bidirectional DC-Sources could be connected to the DC-link capacitors of the inverter system. The control system described in Chapter 4 and Chapter 5 was implemented on a high-speed FPGA system which has several fast analog to digital (A/D) inputs for current and voltage measurement. To set the initial values and

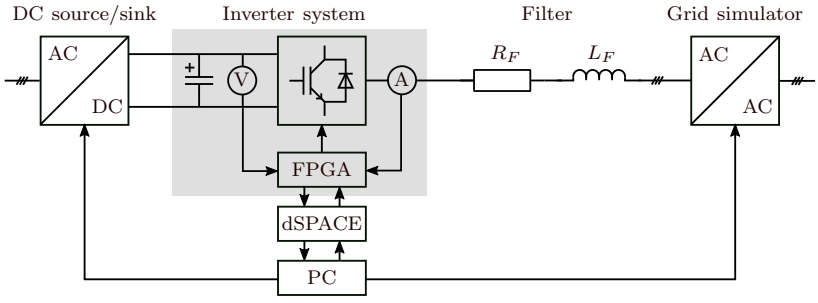


Figure 7.1: Simplified structure of the test bench

control the overall system a dSPACE system was connected to the FPGA. The detailed technical information about the hardware components are listed in the Appendix D. The system parameters used for the measurement with the three- and five-level inverter hardware are shown in Table 7.1. Due to existing signal delay times and increased measurement noise, the radius of each tolerance band was increased compared to the simulations.

Table 7.1: Parameters for three-level and five-level inverter test benches

Parameter	Symbol	Value
Grid voltage	u_{123}	400 V (50 Hz)
Filter inductance	L_F	1.0 mH
Filter resistance	R_F	0.1 Ω
Set current	$\hat{I}^*_{123}$	20 A
Inner hysteresis band	B_i	$\sqrt{2}$ A
Outer hysteresis band	B_o	$\sqrt{16}$ A (3L) / $\sqrt{9}$ A (5L)
MSOGI coefficient	k_1	$\sqrt{2}$
FLL coefficient	Γ	-50
IGBT voltage drop	u_IGBT	3 V (3L) / 4 V (5L)
Dead-time	t_dead	3 μs
Block-time	t_block	3 μs

The presented measurement results in the figures of the following sections consist partly of measured and calculated values. The three-phase inverter output currents i_UVW and grid voltages u_{123} were measured. The combined square error current $|\underline{i}_e|^2$ was calculated subsequently using MATLAB. Additionally shown signals such as the feed forward sector control voltage, detected phase and frequency were logged via a digital to analog (D/A) interface of the used FPGA system. The harmonic components and the total harmonic distortion THD_i of the inverter output current were calculated according to DIN EN 61000-4-7 [99]. The equation for the THD_i is defined by

$$THD_i = \frac{\sqrt{\sum_{h=2}^{40} I_h^2}}{I_1} \tag{7.1}$$

7.2 Measurement Results using a Three-Level NPC

The experimental results shown in this section have been performed using a three-level NPC system. A comparison between the working behaviour of the outer tolerance band and the feed forward sector control method under standard grid conditions and with harmonic distortions is made. Investigations of dynamic fault cases are shown later on the basis of a five-level inverter system.

7.2.1 Standard Operating Point

The first test case investigates the working behaviour under standard grid conditions. The modulation index for this specific operating point is 1.08. This leads to the use of the triangular sectors of the outer hexagonal area in the three-level SV-diagram. The measurement results of the outer tolerance band control and the feed forward sector control method are shown in Figure 7.2. In addition to the inverter output current and the current error the harmonic spectrum of the output current up to the 50th order is shown. Considering the outer tolerance band control method 18 sector changes have to be triggered by the outer tolerance band to control the sectors and thus the current accurately. As one can see in the $\alpha\beta$ representation of the current error the outer tolerance band is triggered equally as it was triggered in the simulations. Considering the results of the proposed feed forward sector control all sector changes are accurately detected whereby the outer tolerance band is not triggered any more during this working point. The difference of the output current and of the current error leads to a noticeable difference in the spectrum of the current. The resulting switching frequency and the calculated THD_i are shown in Table 7.2. While the average switching frequency is reduced only slightly, the THD_i is halved when using the feed forward sector control.

Table 7.2: Measurement results for standard operation of a three-level NPC

	Outer tolerance band	Feed forward control	Difference
f_s	3.43 kHz	3.22 kHz	−6 %
THD_i	4.27 %	1.75 %	−59 %

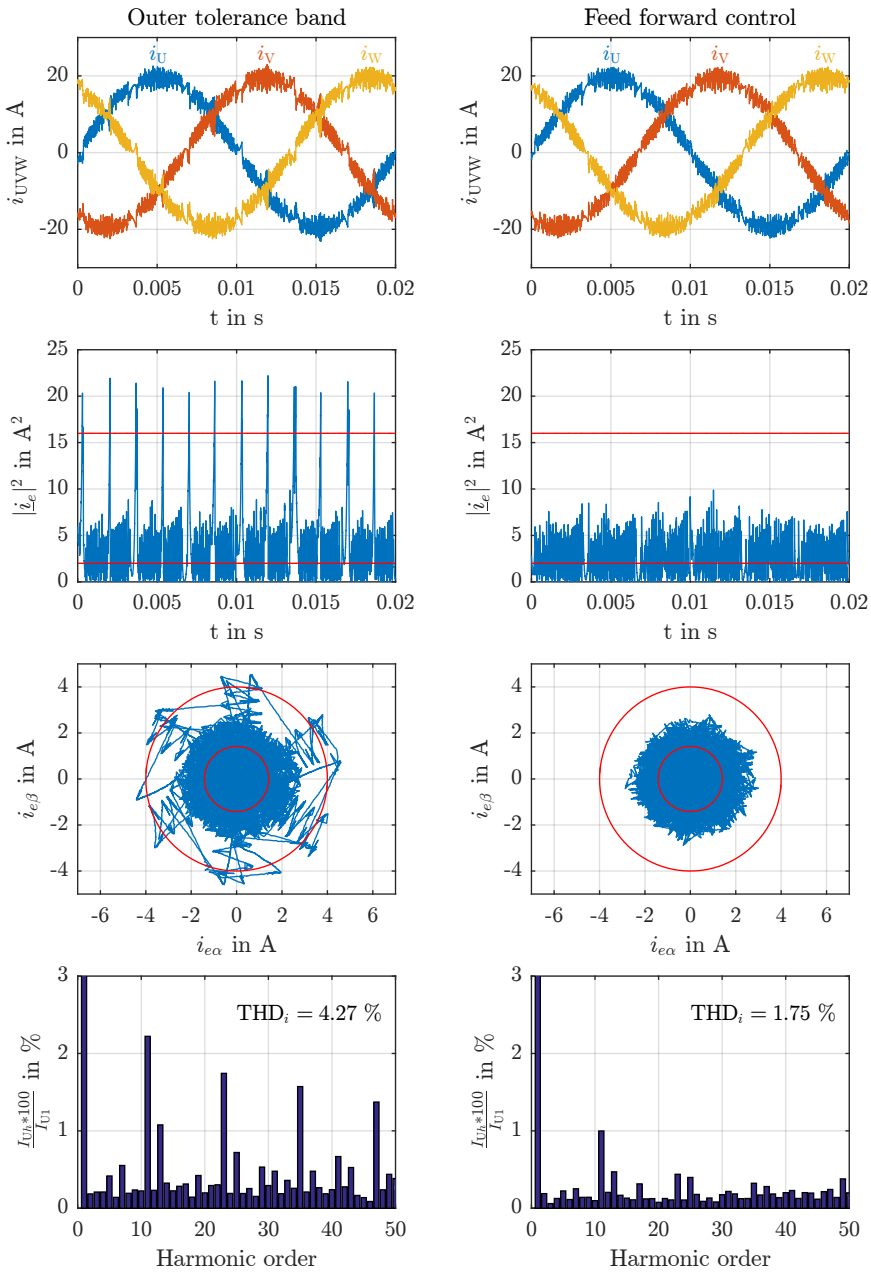


Figure 7.2: Comparison of measured grid current, current error and resulting THD$_i$ under standard grid conditions for different control schemes using a three-level NPC inverter

7.2.2 Harmonic distortion

The following measurement shows the working behaviour of the proposed system connected to a grid with harmonic voltage components. In the grid standards different test cases are defined to investigate the immunity against harmonic distortions [100]. Thereby, the test levels of the harmonic components are divided into three environment classes. Class 1 has the lowest test levels and is used for sensitive equipment like laboratory instrumentation. Class 2 defines the standard levels for all components connected to the grid. Class 3 has the highest compatibility levels and is used for equipment in industrial environments with rapidly varying loads [101].

For the following test a 7th harmonic component with 10 % was added to the fundamental as it is defined for class 3 equipment. The resulting deformation of the grid voltage is shown in Figure 7.3. The distorted grid voltage remains in the outer hexagon of the the three-level SV-diagram. The locations and the time points of the sector changes are different compared to the non-distorted test cases. In order to ensure a sufficient voltage capability of the inverter at each point, the DC-voltage for this test case was increased to 650 V.

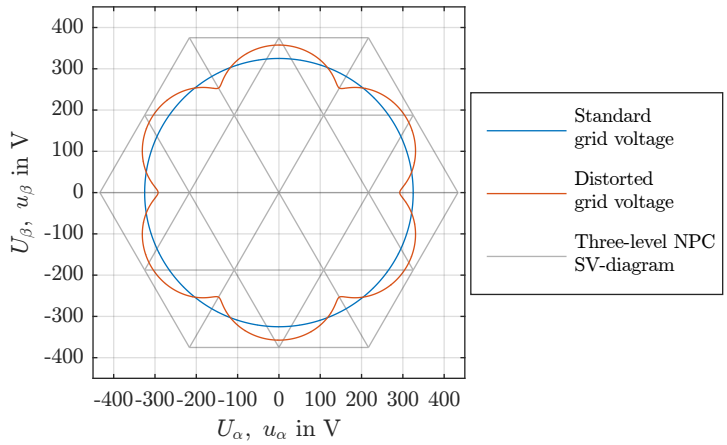


Figure 7.3: Three-level SV-diagram with standard and harmonic distorted grid voltage

To investigate this working point and the influence of the harmonic distorted grid voltage on the implemented controller system three different

measurements were performed. The first measurement was carried out using only the outer tolerance band control method, the second uses the proposed feed forward control but only with its fundamental component and the third uses the feed forward control method with all detected harmonic components. The set current was identical in all three test cases. The resulting three-phase output currents and the related spectrums for the three test cases are shown in Figure 7.4.

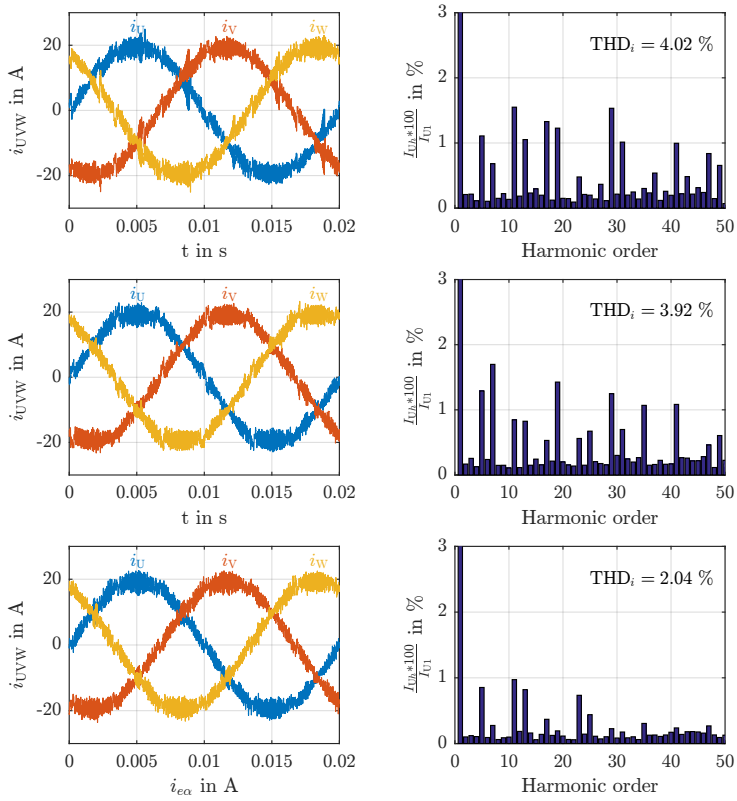


Figure 7.4: Comparison of measured output current and calculated current spectrum under harmonic distorted grid voltage using the outer tolerance band (top), the fundamental component as feed forward voltage (mid) and all harmonic components as feed forward voltage (bottom).

It is apparent that all three methods can be used with high harmonic

distortions. However, the average switching frequencies of the inverter and the resulting THD_i differ significantly. The values for the average switching frequencies and THD_i are listed in Table 7.3.

Table 7.3: Measurement results for a three-level NPC under distorted grid conditions

	Outer tolerance band	Feed forward control (only fundamental)	Feed forward control (with all harmonics)
f_s	4.70 kHz	4.48 kHz	4.36 kHz
THD_i	4.02 %	3.92 %	2.04 %

When using only the fundamental component as feed forward signal the outer tolerance band is touched several times whereby the switching frequency is reduced by 5 % and the THD_i by 2.5 % compared to the use of the outer tolerance band. In contrast, when using all harmonic components for the feed forward control the switching frequency is reduced by 7 % and the THD_i by 49 %.

7.2.3 Comparison of Operation Modes for Three-Level NPC

The following measurement shows the variation of the average switching frequency over the modulation index. Therefore, the grid voltage without harmonics was increased by 25 V steps from 25 V to 350 V in amplitude which corresponds to 8 % to 108 % of the nominal grid voltage. Figure 7.5 shows the covered area for this test in a three-level SV-diagram. The set current amplitude for all measurements was 10 A.

The resulting average switching frequencies of the two operation modes are shown in Figure 7.6. Considering the basic structure of the three-level SV-diagram with its inner and outer hexagonal area two maxima in the switching frequency are visible for both control methods. These points are reached when the inverter output voltage is located in the centre of the triangular sectors. Due to the voltage relationship of the surrounding space vectors and the average inverter output voltage the switching frequency is higher at these operating points. As one can see the feed forward sector control method has the smallest switching frequency over the entire modulation

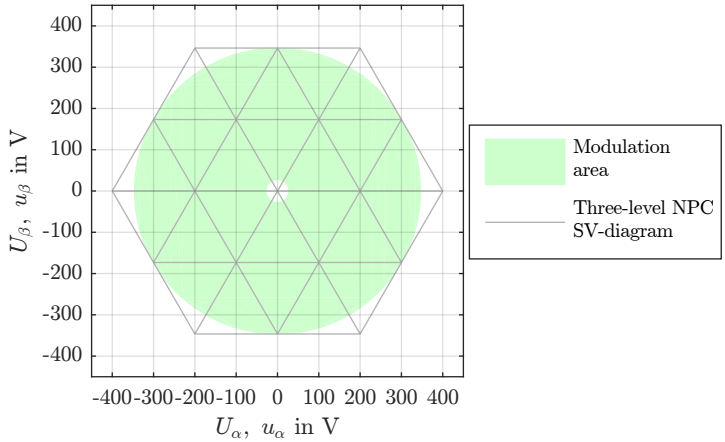


Figure 7.5: Three-level SV-diagram with tested modulation area

index. The difference between the methods has its maxima when the average inverter output voltage is in the centre of a triangular sector. At the corner of the hexagonal areas, the switching frequencies approach each other. The variation of the switching frequencies is 1.97 kHz to 5.36 kHz for the outer tolerance band and 1.66 kHz to 4.41 kHz for the feed forward sector control.

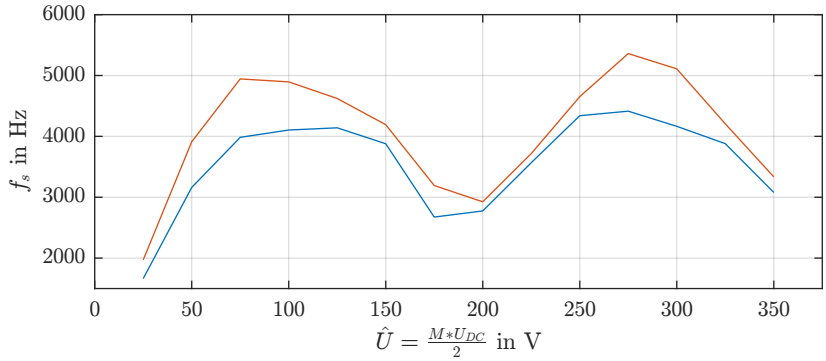


Figure 7.6: Measured average switching frequency versus modulation index for a three-level NPC when using the outer tolerance band control (red) and the feed forward sector control method (blue)

7.3 Measurements using a Five-Level DCI

In the following section measurements using a five-level DCI system are presented. The increased number of triangular sectors leads to increased requirements for the accuracy of the implemented feed forward control system. In addition to standard operation, different measurements were performed to investigate the working behaviour of the proposed system during dynamic changes in the grid.

7.3.1 Standard Operating Point

The first measurement using the five-level DCI system investigates the working behaviour of the proposed system under steady state conditions. As shown in Table 7.1 the outer tolerance band is reduced for the following tests using the five-level inverter. The measurement results using the outer tolerance band control and the feed forward sector control method under standard grid conditions are shown in Figure 7.7. In addition to the measured output current, the squared absolute value and the $\alpha\beta$-representation of the current error, the calculated harmonic spectrum is shown. As one can see, the characteristics of the inverter output current and the current error are equal to that of the simulations. When using the outer tolerance band control the outer tolerance band is reached regularly as expected. The voltage sensorless feed forward system shows a good working behaviour for the five-level inverter system. In this case, all 42 sector changes in the SV-diagram are detected accurately. The resulting switching frequency and the calculated THD_i for both control methods are showed in Table 7.4. The increased number of sector changes for this working point results in a worse THD_i for the outer tolerance band control method. The switching behaviour between the inner and outer tolerance bands also leads to a significantly increased switching frequency.

Table 7.4: Measurement results for standard operation of a five-level DCI

	Outer tolerance band	Feed forward control	Difference
f_s	1.87 kHz	1.21 kHz	−35 %
THD_i	4.43 %	1.33 %	−70 %

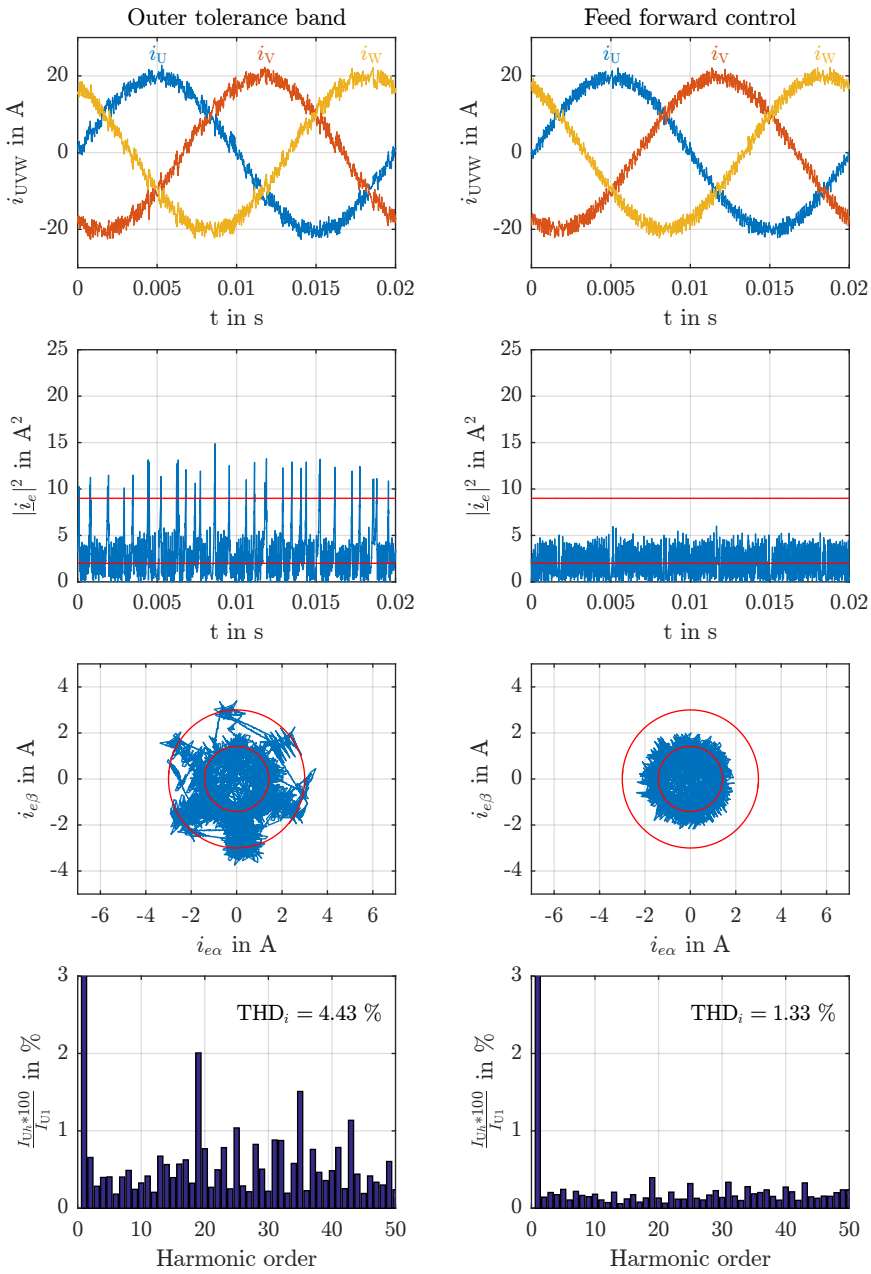


Figure 7.7: Comparison of measured grid current, current error and resulting THD$_i$ under standard grid conditions for different control schemes using a five-level DCI inverter

7.3.2 Voltage Sag

This test is used to investigate the dynamic reaction of the proposed system with a five-level inverter system. During the used type A sag all three phase voltages decrease from 100 % to 20 % of the amplitude of the nominal grid voltage. Considering the five-level SV-diagram this sag corresponds to a change from the outer hexagonal area to the innermost. The modulation index during the sag, therefore, decreases from 1.08 to 0.22. The results for this test case are shown in Figure 7.8.

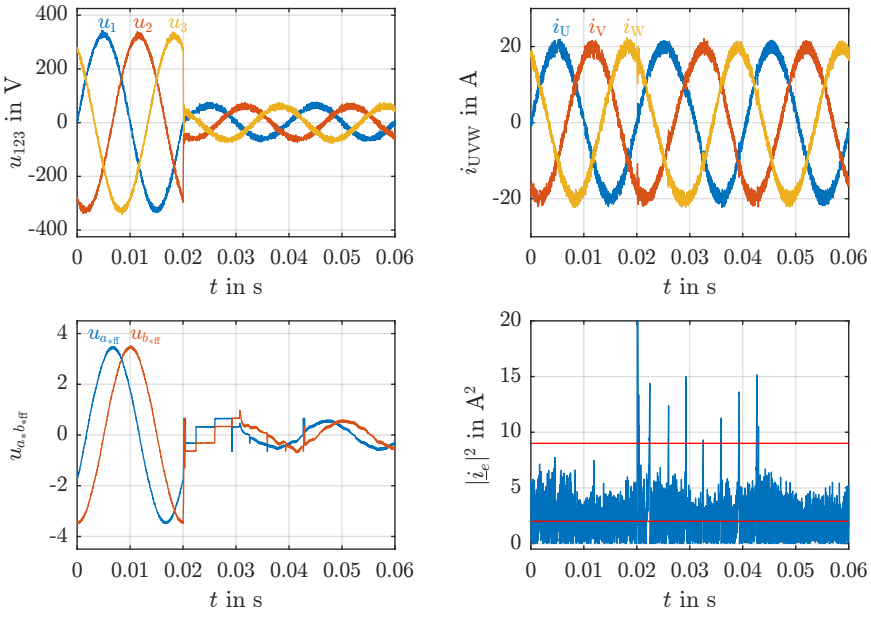


Figure 7.8: Measurement results of five-level DCI reaction on voltage sag (type A) to 20 %. Left side: grid voltage, feed forward signal. Right side: output current, error current

As one can see the squared absolute value of the current error reaches the outer tolerance band immediately at $t = 0.02$ s when the voltage sag is performed. Compared to the simulated voltage sag with a three-level inverter in Chapter 5.4.1 the deviation in the three-phase output current is more clearly noticeable. This error is caused by the time the SHC needs to

change the necessary sectors step by step and thus the space vectors. In this specific case the control system needs 236 μs to reduce the current error back into the inner tolerance band. The use of the outer tolerance band control is continued for about half a grid period. After this time, the feed forward control is reactivated for the first time again. After several changes between both sector control systems the feed forward control is correct enough and continues to works like expected. The trajectory of feed forward control voltage during the fault is shown in Figure 7.9.

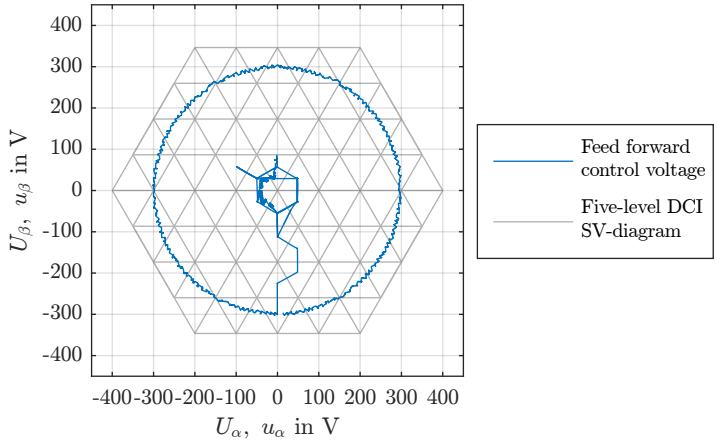


Figure 7.9: Five-level SV-diagram with feed forward voltage for a three-phase voltage sag (type A) from 100 % to 20 %

The time range in this figure corresponds to $t = 0$ s to $t = 0.04$ s. When the voltage sag occurs, the feed forward voltage changes from the outer to the inner hexagonal area over five intermediate sectors triggered by the outer tolerance band.

7.3.3 Harmonic Distortion

The next test is used to investigate the ability of the implemented MSOGI system to detect different harmonic components in the inverter output voltage. Therefore, the harmonic test cases defined in the grid standards for the 5th, 7th, 11th and 13th in class 3 environments are summed up [100]. The individual values for the harmonic components are shown in Table 7.5.

Table 7.5: Harmonic components of distorted grid voltage

h	U_h/U_1
5	12 %
7	10 %
11	7 %
13	7 %

The resulting distorted grid voltage is generated by the grid simulator and shown in $\alpha\beta$-representation in Figure 7.10. As shown, when using a five-level inverter system 76 sector changes per grid period are necessary to accurately control the current. The resulting working behaviour under this distorted grid voltage is shown in Figure 7.11. The amplitude of the set current was set to 20 A.

As one can see the squared absolute value of the current error never reaches the outer tolerance band. That means that all harmonic components were exactly detected by the newly proposed controller system. It also shows

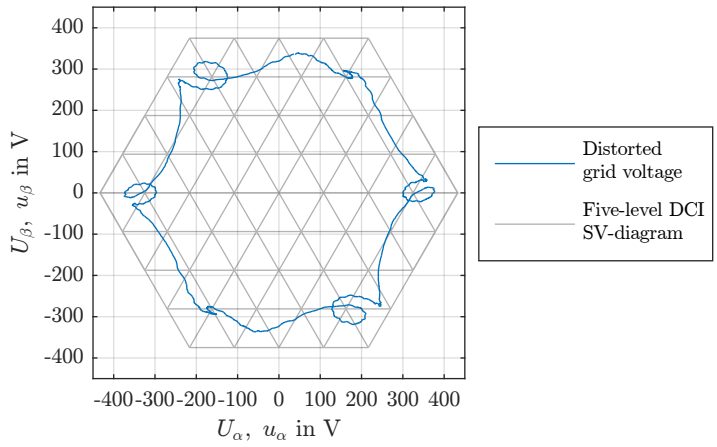


Figure 7.10: Five-level SV-diagram with distorted grid voltage

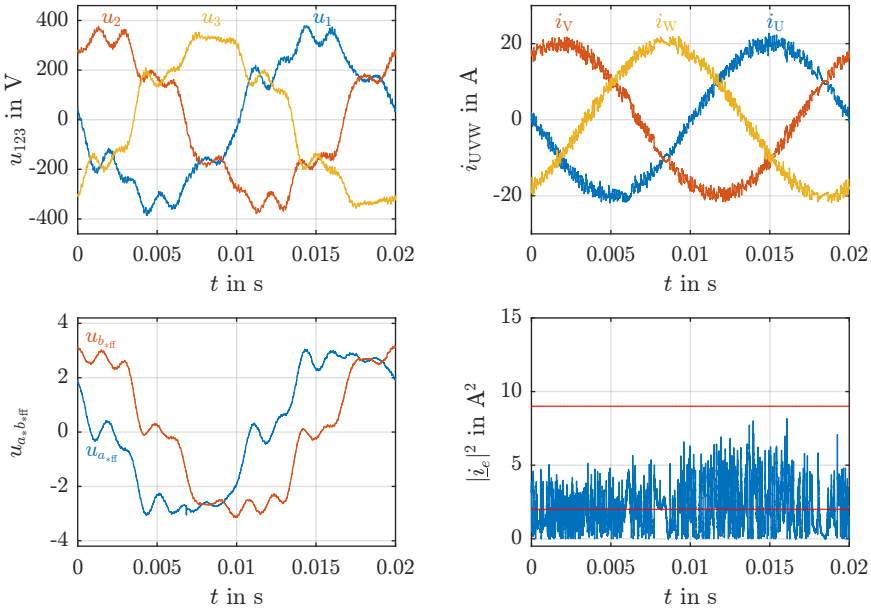


Figure 7.11: Measurement results of five-level DCI system under harmonic grid distortions. Left side: grid voltage, feed forward signal. Right side: output current, error current

the capability of the feed forward control system to detect the fundamental voltage component even in strongly distorted grids.

7.3.4 Frequency Jump

The next test investigates the working behaviour of the five-level inverter system during a variation of the grid frequency from 45 Hz to 55 Hz. The results of this test case are shown in Figure 7.12. The jump in the grid frequency takes place at t = 0.02 s. As it can be seen from the error current, no immediately violation of the outer tolerance band occurs at the time of the frequency jump.

The outer tolerance band is firstly triggered after the phase angles of the actual feed forward voltage with 45 Hz and the real voltage of 55 Hz drift

apart. As it is apparent the feed forward voltage is reactivated after a short time period. The two sector control methods are alternately activated several times. The duration where the triangle midpoint voltage is used reaches its maximum at t = 0.03 s. After this point, its active time decreases

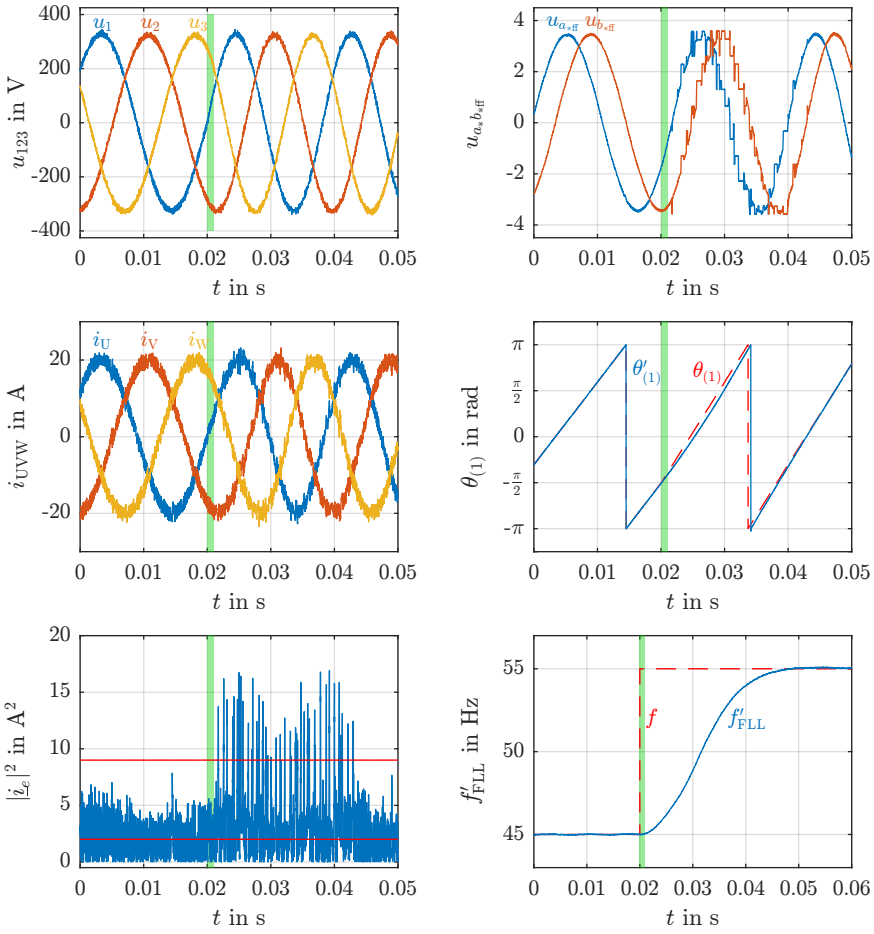


Figure 7.12: Measurement results of three-level NPC reaction on a frequency jump from 45 Hz to 55 Hz. Left side: grid voltage, output current, error current. Right side: feed forward signal, detected phase, detected frequency.

due to the increasing adjustment of the feed forward signal. The permanent error caused by the lag of the phase position in the MSOGI leads to a readjustment of the fundamental frequency in the FLL. After approximately 25 ms the detected frequency reaches the new value of 55 Hz. From this time on, no outer tolerance band is triggered any more.

7.3.5 System Start Up

When using an inverter system without sensors for the grid voltage measurement the working behaviour during the start up needs special attention. At this time the system has no informations about the connected grid. It is, therefore, important to get the correct voltage and frequency information from the grid voltage as fast as possible. A common solution in other voltage sensorless grid connected systems is using only short switching pulses

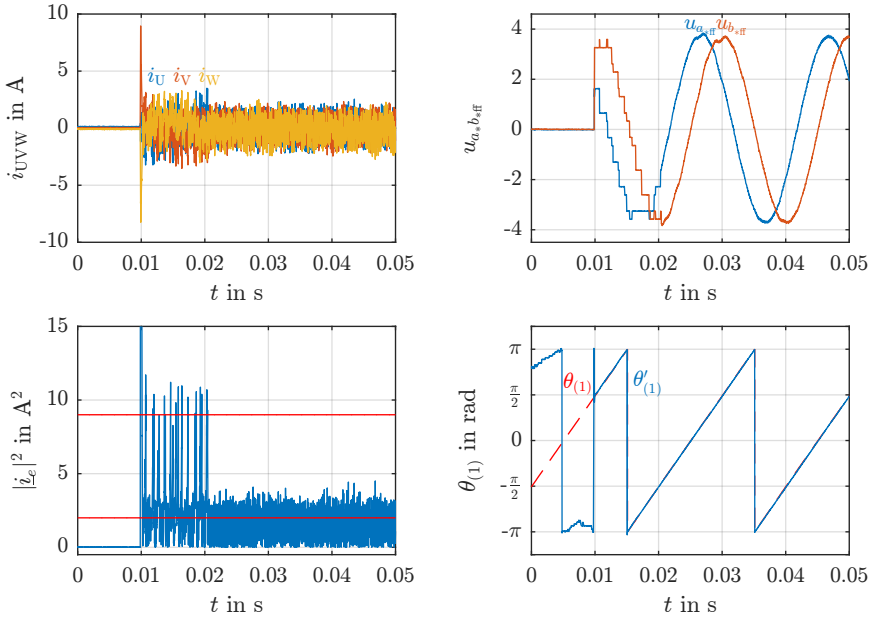


Figure 7.13: Measurement results of five-level DCI during startup. Left side: output current, error current. Right side: feed forward signal, detected phase.

to prevent overcurrent [83, 102]. By evaluating the current trajectory during the short pulses, conclusions about the actual grid voltage and phase can be made. However, since the proposed system is based on a direct current controller no special patterns during start up are necessary to prevent overcurrent.

The working behaviour of the proposed system during the start up is shown in Figure 7.13. The initial value of the current was set to 0 A. The integrators in the MSOGI system are starting with 0 V. As one can see at $t = 0.01$ s the three phase current increases to 8 A for a short time. This is caused by the outer tolerance band control which is used to find the correct triangular sector. The detected grid phase is almost immediately correct after system start. The correct voltage amplitude is detected after approximately 10 ms. From this point in time the outer tolerance band control is no longer needed.

In the presented case the FLL is deactivated for the first 20 ms after start up. During this time period the centre frequency ω' of the MSOGI system is set to the fixed value of 314 rad/s. This approach is used to speed up the start up process. If the FLL is enabled from beginning the centre frequency would decrease as long as the detected amplitude is too small. This would result in a delay of further 10 ms until the feed forward voltage is correct.

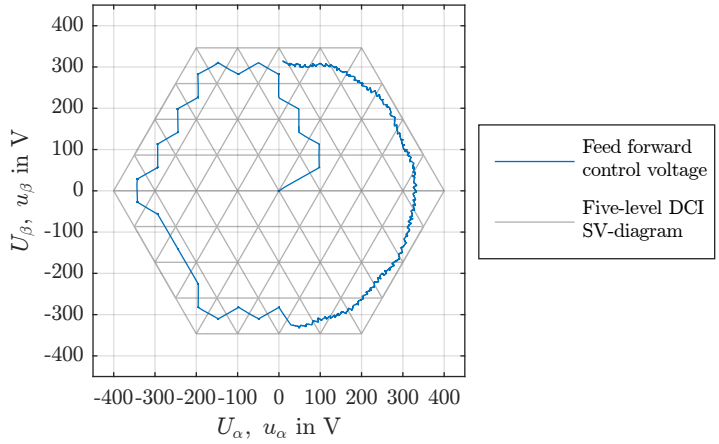


Figure 7.14: Five-level SV-diagram with feed forward voltage during startup

The trajectory of the feed forward control voltage is additionally shown

within a five-level SV-diagram in Figure 7.14. The time range corresponds to $t = 0.01$ s to $t = 0.03$ s. Due to the high number of triangulars it is apparent that the outer tolerance band control has to switch the sectors seven times until the correct sector is reached. The duration to find the correct sector was 330 μs.

7.3.6 Comparison of SHC Operation Modes for 5-level DCI

Similar to the three-level inverter system the influence of the modulation index on the switching frequency is investigated for the five-level inverter system. The grid voltage was increased by 25 V steps from 25 V to 350 V. The set current was set to 10 A for all 14 measurement points. The covered test area within a five-level SV-diagram is shown in Figure 7.16.

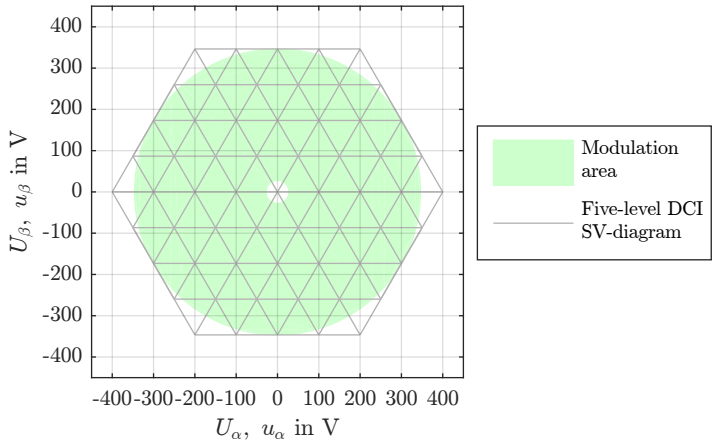


Figure 7.15: Five-level SV-diagram with marked area of tested modulation indexes

The resulting average switching frequencies when using the outer tolerance band control and the feed forward sector control are shown in Figure 7.16. Considering the basic structure of the five-level SV-diagram with its four hexagonal areas four maxima in the switching frequency are recognizable. Compared to the three-level measurements the fluctuation range of the switching frequency for the outer tolerance band control has increased significantly (1.15 kHz to 2.49 kHz). When using the feed forward sector

control the minimum value is 0.83 kHz and the maximum value is 1.21 kHz. This shows that the switching frequency of the inverter system can be reduced at all operating points when using the feed forward sector control method. It is also visible, that the difference in the switching frequency between the the two control methods increases when the modulation index is increased. This is due to the number of triangular sectors which have to be used during a period.

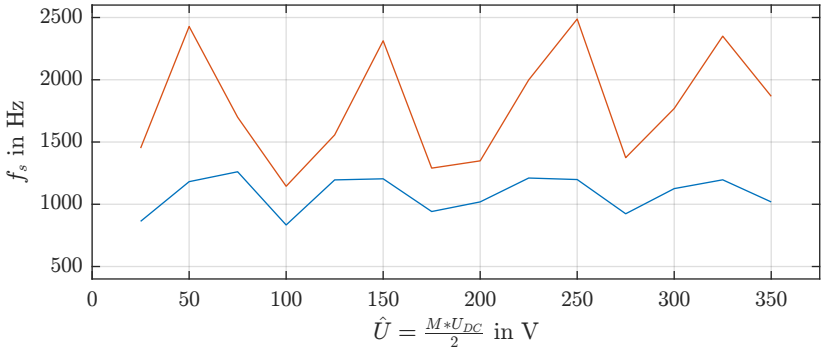


Figure 7.16: Measured average switching frequency versus modulation index for a five-level DCI when using the outer tolerance band control (red) and the feed forward sector control method (blue)

7.4 Summary

This chapter shows the working behaviour of the improved control system for multilevel inverters consisting of the direct current controller SHC and a novel feed forward sector control based on real hardware measurements. All measurements show advancements of the new system and a good conformity with the simulations in Chapter 5. On the basis of the measurements it can be concluded that with higher level counts and thus a higher number of required sector changes, the advantage of feed forward control system increases.

Chapter 8

Conclusion and Future Works

8.1 Conclusion

This thesis proposes an improved direct current controller concept based on the SHC method for multilevel inverter systems in grid applications. The advancement compared to the state of the art concept is based on the use of the average inverter output voltage to determine the exact location within the SV-diagram of multilevel inverter systems and thus to improve the space vector selection process for the direct current controller. For detection of the average inverter output voltage a sensorless voltage synchronization system based on the second order generalized integrator (SOGI) structure was introduced. By using multiple interconnected SOGI circuits the system is able to detect not only the fundamental but also specific harmonic voltage components.

To realize a simple adaptation of the improved current control concept to any inverter level count a novel integer number based coordinate transformation to simplify the representation of the inverter switching states is used. By using this integer representation a general approach to select the correct sectors for multilevel inverter systems is presented. In addition, different possibilities to realize a higher-level power control are shown.

The working behaviour of the improved SHC using the new feed forward sector control from this thesis is investigated and proved with different simulations and measurements on real hardware test benches. As inverter topologies for the simulation and measurements a three-level NPC and a five-level DCI system are used. The results of the simulation and real measurements presented in this thesis show an excellent working behaviour under steady state conditions and a high dynamic reaction speed under different fault cases.

The exact knowledge of the average inverter output voltage leads to a signifi-

cantly improved working behaviour of the control system under steady state conditions. By minimising the use of the outer tolerance band from the state of the art SHC controller the switching frequency, the current error and thus the total harmonic distortion (THD_i) of the inverter output current are reduced with the proposed new controller. When using a three-level inverter system under steady-state conditions in the investigated operating points the improved SHC algorithm reduces the average switching frequency by 6 % and the THD_i by 59 % compared to the standard SHC concept presented in literature [62, 63]. These advantages of the working behaviour increase with higher level count of the inverter system significantly. For a five-level inverter system measured at typical operating points results show a 35 % reduction of the average switching frequency with simultaneous reduction of the THD_i by 70 %. Due to the detection of the harmonic components in the average inverter output voltage the improved current controller system is able to maintain this advantages even in highly harmonic distorted grids.

Summarising the main properties of the proposed control system and comparing the achievements with the objectives of the thesis laid out in Chapter 1 one can conclude that the goals are accomplished with the presented work:

- Improved working behaviour under steady state conditions with reduced current error and THD_i and at the same time reduction of the average switching frequency.
- Stable and accurate working behaviour under dynamic changes in the system.
- The voltage sensorless approach reduces system complexity and costs.
- The detection of harmonic voltage components improves the functionality under harmonic distorted grid conditions.
- The feed forward sector control is independent from the connected filter and impedance of the grid.
- Since the feed forward sector control is already implemented for current control, it can easily be used as well for power control purposes.
- Simple adaptability to higher level inverter systems due to a general approach for describing and selecting correct sectors and space vectors for current control.

8.2 Future Work

The proposed feed forward selection method for direct current controlled multilevel inverters offers several topics for further research. The following examples describe possible subjects for investigations.

Behaviour on Unsymmetrical DC-Link Voltages

Depending on the multilevel inverter topology, certain operation modes or system failures can lead to unbalanced DC-link capacitor voltages or loss of individual DC-cells of the inverter system [103]. Considering the state of the art functionality of the SHC method this fault condition results in a distortion of the space vector positions and its triangular sectors in the SV-diagram. Especially when redundant switching states are used the behaviour of the inverter needs to be considered in more detail. An example of the effects of unsymmetrical DC-link capacitor voltages is shown in Figure 8.1. Here, a five-level SV-diagram is illustrated with voltage deviation of 10 % and 20 %.

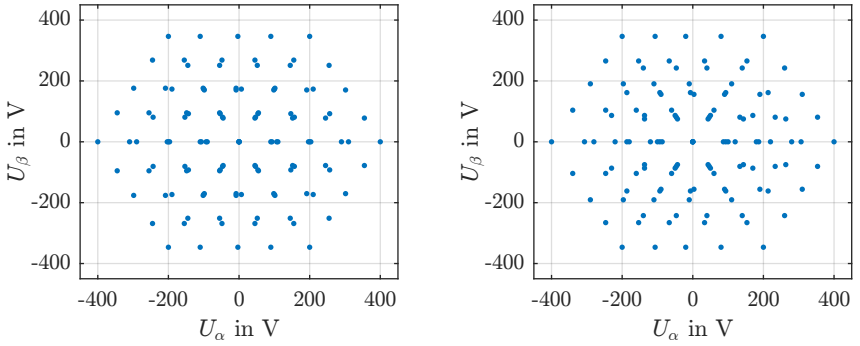


Figure 8.1: Space vector positions for a five-level inverter system with a DC-link capacitor voltage deviation of 10 % (left) and 20 % (right)

As one can see the areas of the triangular sectors are shifted. Therefore, the correct selection of the actual sector and the corresponding space vectors become more complex and, if not performed exactly, could result in a wrong working behaviour of the inverter.

Combination with LCL-Filter

All simulations and measurements in this thesis were carried out using a first order L-filter. However, depending on the grid impedance, packaging space and cost targets third order LCL-filter have become state of the art in industrial applications and typical grid connected inverter systems [12]. A simplified circuit diagram of a grid connected inverter system with an LCL-filter is shown in Figure 8.2. The resistive components of the filter are neglected in this representation.

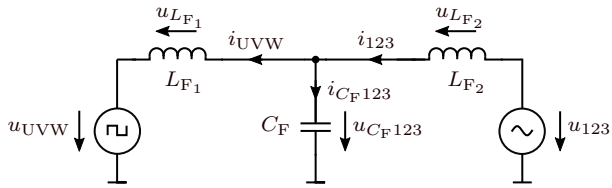


Figure 8.2: Simplified equivalent circuit of a grid connected inverter system with LCL-filter

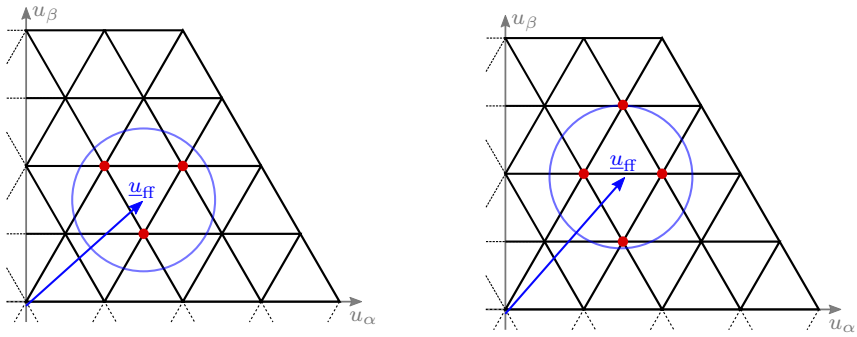
When using the LCL-filter instead of an L-filter, the grid current i_{123} deviates from the measured output current i_{UVW} of the inverter. Including the capacitor current $i_{C_{\mathrm{F}}123}$ the grid current can be calculated by

$$i_{123} = i_{\mathrm{UVM}} + i_{C_{\mathrm{F}}123} \tag{8.1}$$

The new current controller with its feed forward sector control system needs no change at all when using the LCL-filter since it works independent from the load. However, the grid synchronization system requires some adaptations. To correctly determine the set current for power control, all further system variables such as the filter capacitor currents $i_{C_{\mathrm{F}}123}$ and voltages $u_{C_{\mathrm{F}}123}$ need to be considered when calculating the voltage drop across the filter. Additional attention must also be paid to the proposed control system combined with an LCL-filter with respect to the non-constant switching frequency of the direct current controller in order to avoid the excitation of unwanted oscillations in the filter.

Extended Area for Space Vector Selection

As shown in Chapter 5.5 the selection of only the three surrounding space vectors from the used triangular sector results in some special situations in the triggering of the outer tolerance band although the exact location of the inverter output voltage is known. This behaviour can occur if the modulation index is in the transition region between the hexagonal areas of the multilevel SV-diagram. In those situations it would be advantageous to use additional space vectors from other neighbouring sectors. An extended selection process could easily be realized by defining a circle with a defined radius as shown in Figure 8.3. The centre point of the circle would be the detected feed forward voltage $\underline{u}_{\mathrm{ff}}$.



(a) Position in the middle of the sector (b) Position at the border of the sector

Figure 8.3: Selected space vectors by extended selection method within a five-level SV-diagram

The radius of the circle should be chosen such that as long as the average inverter output voltage is clearly within the sector as shown in Figure 8.3a only the three space vectors of the triangular sectors are selected. However, when the voltage position is close to the sector boundary as shown in Figure 8.3b one or more space vectors from other neighbouring sectors are included to better ensure the correct control of the current direction. Using this modification the switching frequency of the inverter should not rise because this selection process would not change the maximum voltage difference between the space vectors.

Fixed frequency operation

One of the disadvantages of direct controllers is the variable switching frequency over the modulation index. Especially for the design and use of LCL grid filters this behaviour might cause problems since certain switching times and frequencies may cause oscillations in the LCL-filter. Possible solutions to eliminate this switching behaviour of direct controllers is to work with a fixed switching frequency by using an equidistant sampling or a readjustment of the tolerance band.

The online calculation of the best possible space vector known from SHC could easily be performed equidistantly. However, it has to be ensured that the same space vector must not be selected twice in order to prevent low switching frequencies critical for the filter. Investigations of such a controller modification needs to be done with special attention on the current error.

8.3 Publications and Patent Applications of the Author

8.3.1 Results Related to Current Control Techniques for Multilevel Systems

1. M. Schaefer, W. Goetze, M. Hofmann, D. Montesinos-Miracle, A. Ackva, "Three Phase Transformation for Simplified Space Vector Control of Multilevel Inverters", *16th IEEE Workshop on Control and Modeling for Power Electronics, COMPEL 2015*

   Abstract - Multilevel inverters provide numerous advantages compared to standard type inverters, most importantly a line voltage with low harmonic distortion through multiple output voltage levels. The control of such a system with space vector modulation techniques leads to more complex algorithms for determining the correct switching behaviour. This paper presents a new three phase transformation with the ability to simplify space vector based control schemes for multilevel inverters. Based on that transformation transistor switching states, redundant switching states and gate signals can easily be determined.

2. M. Schaefer, M. Hofmann, S. Raab, A. Ackva, "Multilevel direct current control for grid connected inverters", *17th European Conference on Power Electronics and Applications, EPE 2015*

   Abstract - One of the most important requirements for grid-connected inverters is an accurate control of the line currents. Applying the switched diamond hysteresis control (SDHC) to multilevel inverters combines the advantages of both techniques and is an enabling step towards a better inverter performance than using state of the art controllers.

3. M. Hofmann, M. Schaefer, A. Ackva, "Optimization of direct current controlled multilevel inverters under distorted conditions" *18th European Conference on Power Electronics and Applications, EPE 2016*

   Abstract - Nowadays current controlled inverters need to be dynamic and robust even under grid disturbances and different grid faults. Besides a robust control method the requirements for the synchronization of the system become more and more important especially when multilevel inverter topologies are used.

4. M. Schaefer, Wolf Goetze, M. Hofmann, F. Bayer, D. Montesinos-Miracle, A. Ackva, "Direct Current Control for Grid-Connected Diode-Clamped Inverters" *IEEE Transactions on Industrial Electronics, Volume: 64, Issue: 4, April 2017*

   Abstract - The accurate control of the line current, robust and dynamic behaviour even under distorted grids and other system faults are the most important requirements for grid-connected inverters. Applying direct current control to multilevel inverters combines the advantages of both and is an enabling step towards improved inverter performance. Direct current controllers suffer from high complexity at increased level count, which is resolved by using geometrical principles and simple analytical calculations for switching vector selection within the space vector diagram. The simplified, novel parametric controller concept is scalable to inverters with arbitrary level count, which does not require any switching tables and the new fully symmetric setup guarantees equal switching frequencies among the three phases. The hypotheses are further confirmed on a real hardware test setup on the example of a three-level NPC inverter hardware and a Xilinx development platform. Experimental results prove the expected behaviour of the direct current control under various conditions, which shows a general approach to balance the dc-link capacitors of diode-clamped inverters within the theoretical limits and demonstrates the benefits of using field programmable gate arrays as a controller platform.

5. M. Schaefer, M. Hofmann, S. Raab, A. Ackva, "FPGA Based Control of an Three Level Neutral Point Clamped Inverter" *Power conversion and Intelligent Motion Conference, PCIM Europe 2017*

   Abstract - The accurate control of the line current, the robustness and the dynamic behaviour are major factors when benchmarking grid connected inverters. Due to weak grids even fast reactions on distortions and other system faults are required properties. Direct current control in combination with multilevel inverters could combine the advantages and give opportunities for future systems designs. As the complexity, the speed and the calculation effort increases within those systems very fast data processing is indispensable. To meet the mentioned demands Field Programmable Gate Arrays (FGPAs) are an alternative to state of the art Microcontroller Units (MCUs).

6. M. Hofmann, M. Schaefer, A. Ackva, "Sensor-less Grid Voltage Synchronization of Direct Current Controlled Multilevel Converters" *19th European Conference on Power Electronics and Applications, EPE 17*

   Abstract - The accurate control of the line current, robust and dynamic behaviour even under distorted grids and the behaviour on other faults are important requirements for grid connected inverter systems. This paper presents a sensorless grid voltage determination system in combination with an direct current control method optimized for multilevel inverters.

7. M. Schaefer, M. Hofmann, S. Raab, A. Kraemer, A. Ackva, "Hochdynamisches und robustes Stromregelverfahren fuer Umrichter unterschiedlicher Topologien" *Elektrische Antriebstechnologie fuer Hybrid- und Elektrofahrzeuge HdT*

8.3.2 Results Related to Applications for Current Control Techniques

1. A. Ackva, J. Endres, M. Hofmann, "Novel line-side inverter with active filter option: Two paralleled inverters with high speed direct current control algorithms" *4th International Symposium on Power Electronics for distributed Generation Systems (PEDG), 2013, Rogers, AR, USA*

   Abstract - This paper presents a novel direct current control algorithm for Voltage Source Inverters (VSI) which combines the advantages of common space vector pulse-width modulation (SVPWM) techniques with the outstanding dynamic performance of direct current control methods. An implementation on a grid-connected line-side inverter is introduced followed by corresponding measurement results. In this connection an active filter option for improved power quality is discussed.

2. M. Hofmann, S. Raab, M. Schaefer, P. Ponomarov, A. Ackva, "Measurements on vehicle to grid application in industrial power grid for peak load reduction", *6th International Symposium on Power Electronics for distributed Generation Systems (PEDG), 2016, Aachen, Germany*

   Abstract - The combination of "electric mobility" and "renewable energy production" heavily demands for energy storage systems. Investigations of technical possibilities to use the stored energy of electric vehicles (EV) and so called plug-in hybrid electric vehicles (PHEVs)

for smoothing the grid load and reduce power peaks are inalienable. Within the limits given by the cars battery management system consumption driven charge and discharge signals could be used for effective integration in V2G systems. This paper will give a detailed overview of a system for bidirectional charging in an industrial grid. First real measurements and test results are given to proof the concept and show the opportunities.

3. S. Raab, M. Hofmann, M. Schaefer, A. Ackva, "V2G-faehige bidirektionale Schnellladestation fuer Elektrofahrzeuge", *EMA-Nuernberg 2014 Elektromobilitaetsausstellung und Fachtagung*

   Abstract - Die ungeregelte, wetterabhaengige Einspeisung von Photovoltaikanlagen in das Energienetz sorgt fuer einen immensen Ausbaubedarf der Elektrizitaetsversorgungsnetze. Dieser Ausbau kann durch den gezielten Einsatz von Speichersyste-men stark reduziert werden. Die Untersuchung der technischen Moeglichkeiten, um Elektrofahrzeuge und auch Plug-In Hybridfahrzeuge, die ueber einen enorme Speicherkapazitaet verfuegen, als Speichersysteme einzusetzen, wird somit unabdingbar. Innerhalb der vom fahrzeuginternen Batteriemanagementsystem vorgegebenen Grenzen kann der Fahrzeug akkumulator ueber verbrauchsgesteuerte Lade- und Entladesignale effektiv in zukuenftige V2G- Systeme integriert werden. Um die technischen Moeglichkeiten einer solchen Technologie auszuloten, wurde in der Hochschule fuer Angewandte Wissenschaften Wuerzburg - Schweinfurt der Prototyp einer V2G- faehigen, bidirektionalen Schnellladestation fuer Elektrofahrzeuge entwickelt.

4. M. Hofmann, M. Schaefer, A. Ackva, "Bi-directional charging system for electric vehicles", *3rd International Energy Transfer for Electric Vehicles Conference, Nuremberg, Germany*

   Abstract - The combination of "electric mobility" and "renewable energy production" heavily demands for energy storage systems. Investigations of technical possibilities to use electric vehicles (ev) and so called plug-in hybrid electric vehicles (phevs), containing a relevant amount of storage capacity, as storage systems are inalienable. Within the limits given by the car's battery management system consumption-driven charge and discharge signals could be used for effective integration in future V2G systems. This paper will give a detailed overview about a concept for bi-directional charging and first test results.

5. S. Raab, P. Ponomarov, M. Hofmann, M. Schaefer, A. Ackva, "Performance evaluations of load balancing in industrial power grids using vehicle to grid technology", *19th European Conference on Power Electronics and Applications, EPE 17*

   Abstract - The presented paper evaluates measurement results and reports about further development from the vehicle to grid system presented. It uses a number of mass-production electric vehicles in sink and source mode to balance the load of an industrial plant by cutting off its peak loads. The actual load is detected and the balancing power is calculated by a predictive algorithm which keeps the total load below the setpoint. Analysis show that the goal of peak load shaving is reached using the presented control strategy. Although mean availability of balancing performance is lower than assumed. Improvements were made, reducing DC link ripple current by passively low pass filtering. After evaluating proportion of stations' active to passive times, a standby mode was implemented improving efficiency of overall system.

6. S. Raab, P. Ponomarov, M. Hofmann, M. Schaefer, A. Kraemer, A. Ackva, "Vehicle to Grid Anwendung zur Spitzenlastreduktion in Industrienetzen" *Elektrische Antriebstechnologie fuer Hybrid- und Elektrofahrzeuge HdT*

7. M. Schaefer, M. Hofmann, F. Bayer, B. Mueller, A. Ackva, "Direct Current Control Method for Three-Phase Motor Drives" *13th International Conference on Ecological Vehicles and Renewable Energies, EVER2018*

   Abstract - The requirements of three-phase motor drives in terms of reliability, efficiency, robustness, dynamic as well as cost efficiency are continuously increasing within the last years. To meet this demand the hardware components and motor drives are used in non-linear and special operating points leading to increased requirements for the control method. This paper presents a new direct current control method that is able to work at these operating points. It is robust, able to deal with non-linear loads and that overcomes some disadvantages of existing direct current control methods. The generic approach would even allow to use inverter systems with more than two levels.

8.3.3 Patent Applications

1. Patent Application: M. Hofmann, J. Koch, L. Neumann, M. Schaefer, H. Wiessmann, "REGELUNG EINES DREI-LEVEL WECHSELRICHTERS", *Application Number: 16190787.8-1809*

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Appendix A

Three-level SV-Diagram

The SV-diagram of a three-level NPC system is shown in Figure A.1. The side length of the triangular sectors is scaled to $1/3 \cdot U_{\mathrm{DC}}$.

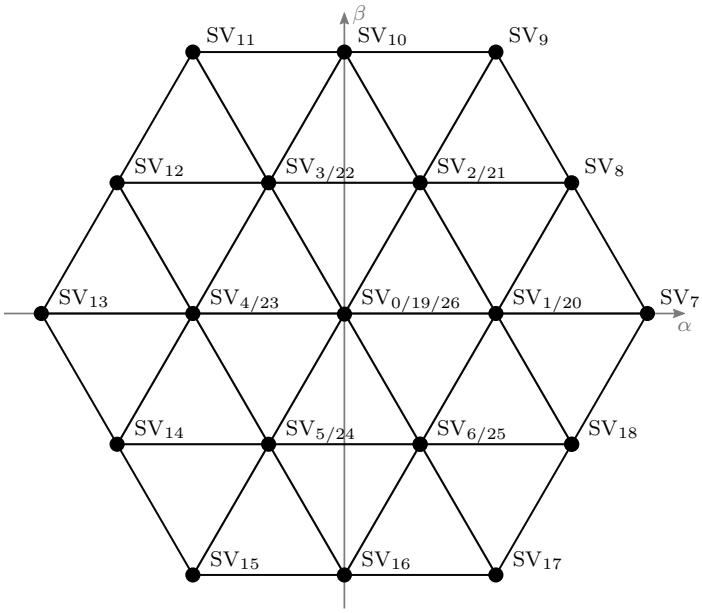


Figure A.1: SV-diagram of three-level NPC system

All 27 switching positions and output voltages in the $\alpha\beta$-system are shown in Table A.1. The eight redundant switching positions are SV_{19} to SV_{26}.

Table A.1: Output voltage levels of three-level NPC system in the two-phase $\alpha\beta$-system for all possible switch combinations

State	Space Vector	Switch positions	u_α/U_{DC}	u_β/U_{DC}
0	SV_0	− 1 − 1 − 1	0	0
1	SV_1	0 − 1 − 1	1/3	0
2	SV_2	0 0 − 1	1/6	$\sqrt{3}/6$
3	SV_3	− 1 0 − 1	−1/6	$\sqrt{3}/6$
4	SV_4	− 1 0 0	−1/3	0
5	SV_5	− 1 − 1 0	−1/6	$-\sqrt{3}/6$
6	SV_6	0 − 1 0	1/6	$-\sqrt{3}/6$
7	SV_7	1 − 1 − 1	2/3	0
8	SV_8	1 0 − 1	1/2	$\sqrt{3}/6$
9	SV_9	1 1 − 1	1/3	$\sqrt{3}/3$
10	SV_{10}	0 1 − 1	0	$\sqrt{3}/3$
11	SV_{11}	− 1 1 − 1	−1/3	$\sqrt{3}/3$
12	SV_{12}	− 1 1 0	−1/2	$\sqrt{3}/6$
13	SV_{13}	− 1 1 1	0	−2/3
14	SV_{14}	− 1 0 1	−1/2	$-\sqrt{3}/6$
15	SV_{15}	− 1 − 1 1	−1/3	$-\sqrt{3}/3$
16	SV_{16}	0 − 1 1	0	$-\sqrt{3}/3$
17	SV_{17}	1 − 1 1	1/3	$-\sqrt{3}/3$
18	SV_{18}	1 − 1 0	1/2	$-\sqrt{3}/6$
19	SV_{19}	0 0 0	0	0
20	SV_{20}	1 0 0	1/3	0
21	SV_{21}	1 1 0	1/6	$\sqrt{3}/6$
22	SV_{22}	0 1 0	−1/6	$\sqrt{3}/6$
23	SV_{23}	0 1 1	−1/3	0
24	SV_{24}	0 0 1	−1/6	$-\sqrt{3}/6$
25	SV_{25}	1 0 1	1/6	$-\sqrt{3}/6$
26	SV_{26}	1 1 1	0	0

Appendix B

Transfer Function of Used MSOGI System

The following two functions show the transfer function of the fundamental and fifth component of the MSOGI system used to detect the harmonic components of the average inverter output voltage in the simulations and measurements.

$$G_{\mathrm{MSOGI1}}(s) =$$

$$\frac{443s^{31} + 1.962e06s^{30} + 3.674e10s^{29} + 1.427e14s^{28} + 1.281e18s^{27}}{s^{32} + 7087s^{31} + 9.678e07s^{30} + 5.357e11s^{29} + 3.82e15s^{28} + 1.689e19s^{27}}$$

$$\frac{+4.343e21s^{26} + 2.459e25s^{25} + 7.216e28s^{24} + 2.861e32s^{23} + 7.192e35s^{22}}{+8.124e22s^{26} + 2.9e26s^{25} + 1.032e30s^{24} + 2.984e33s^{23} + 8.177e36s^{22}}$$

$$\frac{+2.104e39s^{21} + 4.47e42s^{20} + 9.939e45s^{19} + 1.756e49s^{18} + 3.013e52s^{17}}{+1.913e40s^{21} + 4.118e43s^{20} + 7.753e46s^{19} + 1.319e50s^{18} + 1.982e53s^{17}}$$

$$\frac{+4.346e55s^{16} + 5.777e58s^{15} + 6.643e61s^{14} + 6.794e64s^{13} + 6.043e67s^{12}}{+2.655e56s^{16} + 3.144e59s^{15} + 3.285e62s^{14} + 3.011e65s^{13} + 2.409e68s^{12}}$$

$$\frac{+4.663e70s^{11} + 3.085e73s^{10} + 1.726e76s^{9} + 8.01e78s^{8} + 3.029e81s^{7}}{+1.671e71s^{1}1 + 9.975e73s^{10} + 5.08e76s^{9} + 2.185e79s^{8} + 7.849e81s^{7}}$$

$$\frac{+9.167e83s^{6} + 2.173e86s^{5} + 3.911e88s^{4} + 5.081e90s^{3} + 4.304e92s^{2}}{+2.327e84s^{6} + 5.602e86s^{5} + 1.072e89s^{4} + 1.576e91s^{3} + 1.685e93s^{2}}$$

$$\frac{+1.849e94s}{+1.178e95s + 4.12e96}$$

$$G_{\mathrm{MSOGI5}}(s) =$$

$$\frac{\begin{array}{c}443s^{31} + 1.962e06s^{30} + 3.989e10s^{29} + 1.548e14s^{28} + 1.542e18s^{27}\end{array}}{\begin{array}{l}s^{32} + 7087s^{31} + 1.063e08s^{30} + 5.987e11s^{29} + 4.743e15s^{28} + 2.178e19s^{27}\\ +5.23e21s^{26} + 3.373e25s^{25} + 9.952e28s^{24} + 4.637e32s^{23} + 1.184e36s^{22}\\ +1.185e23s^{26} + 4.508e26s^{25} + 1.858e30s^{24} + 5.912e33s^{23} + 1.938e37s^{22}\\ +4.219e39s^{21} + 9.266e42s^{20} + 2.611e46s^{19} + 4.897e49s^{18} + 1.113e53s^{17}\\ +5.192e40s^{21} + 1.39e44s^{20} + 3.15e47s^{19} + 6.992e50s^{18} + 1.342e54s^{17}\\ +1.768e56s^{16} + 3.271e59s^{15} + 4.35e62s^{14} + 6.564e65s^{13} + 7.191e68s^{12}\\ +2.488e57s^{16} + 4.039e60s^{15} + 6.261e63s^{14} + 8.541e66s^{13} + 1.101e70s^{12}\\ +8.782e71s^{11} + 7.741e74s^{10} + 7.503e77s^{9} + 5.128e80s^{8} + 3.795e83s^{7}\\ +1.248e73s^{1}1 + 1.321e76s^{10} + 1.22e79s^{9} + 1.034e82s^{8} + 7.524e84s^{7}\\ +1.891e86s^{6} + 9.846e88s^{5} + 3.203e91s^{4} + 9.592e93s^{3} + 1.745e96s^{2}\\ +4.884e87s^{6} + 2.636e90s^{5} + 1.201e93s^{4} + 4.25e95s^{3} + 1.107e98s^{2}\\ +2.889e98s\\ +1.828e100s + 1.609e102\end{array}}$$

Appendix C

Voltage Sag Classification

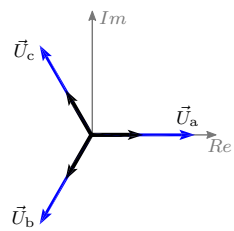
During a voltage sag the voltages and the phases of the three-phase grid can change. These voltage sags can be caused by the following grid conditions:

- Three-phase fault
- Three-phase to ground fault
- Single-phase to ground fault
- Phase to phase fault
- Two phase to ground fault

According to the cause of the fault and grid connection of the load six different voltage sag types can occur in the grid. This sags are classified from type A to G [7]. In following, the properties of these six types are generally described. All specified phase voltages are related to the nominal phase voltage U_{nom} or the faulted phase voltage U_{f}. In the shown vector diagrams of the fault types the nominal phase vectors are illustrated in blue and the phase voltages of the specified fault case are illustrated in black.

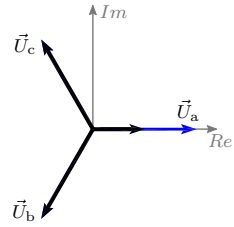
- **Type A**

$$\vec{U}_{\mathrm{a}} = U_{\mathrm{f}}$$
$$\vec{U}_{\mathrm{b}} = -\tfrac{1}{2} \cdot U_{\mathrm{f}} - j \cdot \tfrac{\sqrt{3}}{2} \cdot U_{\mathrm{f}}$$
$$\vec{U}_{\mathrm{c}} = -\tfrac{1}{2} \cdot U_{\mathrm{f}} + j \cdot \tfrac{\sqrt{3}}{2} \cdot U_{\mathrm{f}}$$



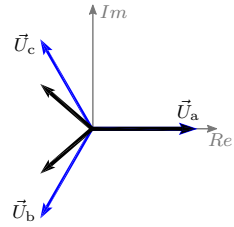
- **Type B**

$$\vec{U}_\mathrm{a} = U_\mathrm{f}$$
$$\vec{U}_\mathrm{b} = -\tfrac{1}{2} \cdot U_\mathrm{nom} - j \cdot \tfrac{\sqrt{3}}{2} \cdot U_\mathrm{nom}$$
$$\vec{U}_\mathrm{c} = -\tfrac{1}{2} \cdot U_\mathrm{nom} + j \cdot \tfrac{\sqrt{3}}{2} \cdot U_\mathrm{nom}$$



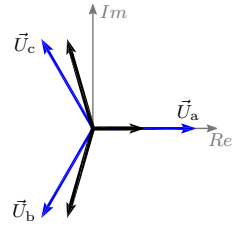
- **Type C**

$$\vec{U}_\mathrm{a} = U_\mathrm{nom}$$
$$\vec{U}_\mathrm{b} = -\tfrac{1}{2} \cdot U_\mathrm{nom} - j \cdot \tfrac{\sqrt{3}}{2} \cdot U_\mathrm{f}$$
$$\vec{U}_\mathrm{c} = -\tfrac{1}{2} \cdot U_\mathrm{nom} + j \cdot \tfrac{\sqrt{3}}{2} \cdot U_\mathrm{f}$$



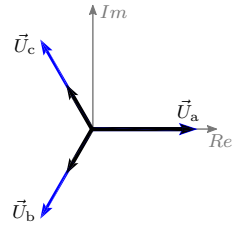
- **Type D**

$$\vec{U}_\mathrm{a} = U_\mathrm{f}$$
$$\vec{U}_\mathrm{b} = -\tfrac{1}{2} \cdot U_\mathrm{f} - j \cdot \tfrac{\sqrt{3}}{2} \cdot U_\mathrm{nom}$$
$$\vec{U}_\mathrm{c} = -\tfrac{1}{2} \cdot U_\mathrm{f} + j \cdot \tfrac{\sqrt{3}}{2} \cdot U_\mathrm{nom}$$



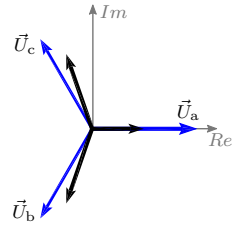
- **Type E**

$$\vec{U}_\mathrm{a} = U_\mathrm{nom}$$
$$\vec{U}_\mathrm{b} = -\tfrac{1}{2} \cdot U_\mathrm{f} - j \cdot \tfrac{\sqrt{3}}{2} \cdot U_\mathrm{f}$$
$$\vec{U}_\mathrm{c} = -\tfrac{1}{2} \cdot U_\mathrm{f} + j \cdot \tfrac{\sqrt{3}}{2} \cdot U_\mathrm{f}$$



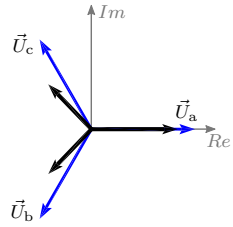
- **Type F**

$$\vec{U}_\mathrm{a} = U_\mathrm{f}$$
$$\vec{U}_\mathrm{b} = -\tfrac{1}{2} \cdot U_\mathrm{nom} - j \cdot \left(\tfrac{\sqrt{3}}{6} \cdot U_\mathrm{f} + \tfrac{\sqrt{3}}{3} \cdot U_\mathrm{nom} \right)$$
$$\vec{U}_\mathrm{b} = -\tfrac{1}{2} \cdot U_\mathrm{nom} + j \cdot \left(\tfrac{\sqrt{3}}{6} \cdot U_\mathrm{f} + \tfrac{\sqrt{3}}{3} \cdot U_\mathrm{nom} \right)$$



- **Type G**

$$\vec{U}_{\mathrm{a}} = \frac{2}{3} \cdot U_{\mathrm{nom}} + \frac{1}{3} \cdot U_{\mathrm{f}}$$
$$\vec{U}_{\mathrm{b}} = -\frac{1}{3} \cdot U_{\mathrm{nom}} - \frac{1}{6} \cdot U_{\mathrm{f}} - j \cdot \frac{\sqrt{3}}{2} \cdot U_{\mathrm{f}}$$
$$\vec{U}_{\mathrm{b}} = -\frac{1}{3} \cdot U_{\mathrm{nom}} - \frac{1}{6} \cdot U_{\mathrm{f}} + j \cdot \frac{\sqrt{3}}{2} \cdot U_{\mathrm{f}}$$



Depending on the location of the fault, the number and design of existing transformers in the transmission line to the load, the fault type may change [104]. An example of a transmission line with two transformer in delta-star (Dy) connection and three connection points is shown in Figure C.1.

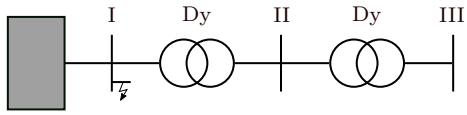


Figure C.1: Example of transmission line

According to the location of fault and the connected load the voltage sag types change after the transformer as shown in Table C.1.

Table C.1: Change of voltage sag types caused by transformers in the transmission line

	Connection point		
Fault case	I	II	III
Three-phase fault	A	A	A
Two-phase to ground fault	E	F	G
Two-phase fault	C	D	C
Single-phase to ground fault	B	C	D

Appendix D

Inverter Hardware and Testbench

The following section of the Appendix gives a short overview of the used hardware for the experimental verification in Chapter 7.

Gridsimulator

The three-phase grid simulator in the laboratory is used to emulate the grid side of the inverter system. The adjustable output voltage parameters can be used to simulate various grid faults such as voltage sags. The main system parameters of the grid simulator are:

Table D.1: Parameters of the grid simulator

Description	Value
Name/Type	Regatron TopCon TC.ACS
Output phase voltage	0 - 280 V
Output phase current	0 - 72 A
Power range	0 - 50 kVA
Power factor	0 - 1
Output frequency	0 - 1000 Hz

DC-Source/Sink

As supply for the DC-link capacitors of the multilevel inverter system, up to four bidirectional DC-sources can be used. Depending on the application, these can be connected in series or in parallel. The main system parameters of the DC-sources are:

Table D.2: Parameters of DC-sources

Description	Value
Name/Type	Regatron TopCon TC.GSS
Output phase voltage	0 - 500 V
Output phase current	0 - ±50 A
Power range	0 - ±20 kW

Figure D.1: Grid simulator and DC-sources

Three-Level NPC

Figure D.2: Three-level NPC module

Table D.3: Three-level inverter specification

Description	Value
Name/Type	3L SKiiP28MLI07E3V1 [105]
Supplier	Semikron
DC-link voltage	750 V
Rated current	100 A
IGBT blocking voltage	650 V
DC-link capacitance	2 mF
Interlock time	2.6 μs
Maximum switching frequency	20 kHz

Five-Level DCI

Figure D.3: Phase module of five-level inverter

Table D.4: Five-level inverter specification

Description	Value
Name/Type	5L FHWS-5LDCI
IGBT	IXYS IXYN100N120B3H1
Blocking voltage	1200 V
Rated current	75 A
Clamping Diodes	IXYS DSEP2x91-06A
DC-link voltage	900 V
DC-link capacitance	1 mF
Interlock time	2 μs
Maximum switching frequency	20 kHz

FPGA Control System

All control algorithms, like the improved SHC and the MSOGI synchronization, used in the thesis were implemented in a FPGA development system. The system is designed to speed up complex calculation and control algorithms for different inverter applications. The basic specifications of the FPGA controller board are listed in Table D.5.

Table D.5: Parameters of the FPGA controller board

Description	Value
Name/Type	FHWS-XC7A200
FPGA	Xilinx Artix-7
	XC7A200T-2FFG1156C
	215.360 Logic cells
	740 DSP48E1 Slices
	13.140 Kb Block RAM
Features	1 GB DDR3-SDRAM (800 Mb/s)
	2 Gigabit Ethernet ports
	1 SATA port (6Gb/s)
	Flash (32 MB)
	EEPROM (1 MB)
	SD card slot
	250 IOs (120 LVDS pairs)
	4 LVDS pairs with 6Gb/s
	8 User LED and DIP switches
	...

The controller board is designed as plug-in card for a standard 19 inch rack system. A picture of the FPGA controller board is shown in Figure D.4.

Via a system backplane up to 10 extension cards, each connected to 25 IOs of the FPGA controller board, can be used for various applications like data acquisition, communication or interfacing with an inverter.

Figure D.4: FPGA controller board

To monitor and control all components of the test bench by the FPGA, several expansion boards were required which use the inputs and outputs of the FPGA for various tasks. The following cards have been used for this purpose:

- 4 channel A/D converter card for AC current measurement (14 bit @ 40 MS/s) connected to LEM LA-200P current transducers.
- 10 channel A/D converter card with sigma-delta modulators for voltage measurement (16 bit @ 312 kS/s).
- 4 channel D/A converter card for signal output (12 bit @ 192 kS/s).
- Inverter interface cards for three-level NPC and five-level DCI systems.
- 8 channel digital IO card (4 in / 4 out) for control of contactors.