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Optimization of FinFET-Based Gain Cells for Low Power Sub-V_T Embedded DRAMs

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Sub-threshold circuits (sub-V_T) are a promising alternative in the implementation of low power electronics. The implementation of gain-cell embedded DRAMs (eDRAMs) based on FinFET devices requires a careful design to achieve the maximum cell performance (i.e., retention time, access time, and energy consumption) suitable for the sub-V_T operating level. In this work, we show that asymmetrically resizing the memory cell (i.e., the channel length of the write access transistor and the width of the rest of the devices) results in a 3.5× increase in retention time when compared to the nominal case while reducing area, as well. In terms of reliability (e.g., variability and soft errors), the resizing also improves the cell robustness (50% and 1.9×, respectively) when the cells are operated at sub-V_T level.

Keywords: FinFET, eDRAM, Sub-V_T, Single Event Upsets, Variability, Reliability.

1. INTRODUCTION

The booming of the Internet of Things (IoT) and healthcare applications domains[1–3] has increased the interest for ultra-low power circuits. In this sense, circuits that operate below the threshold voltage (sub-V_T circuits) have emerged as a plausible choice. In sub-V_T circuits, supply voltage (V_{DD}) is reduced below the device threshold voltage (V_T) to reduce the power consumption. Wireless sensor networks, medical applications and mobile signal processing[2,3] with medium-speed applications (kHz–MHz regime) are the most appropriate applications for such sub-V_T circuits. To enhance (enlarge the drive current) of sub-V_T circuits, sizing appropriately the cell devices is one of the most effective solutions.[4] In such systems, energy efficiency is of primary concern. The lowest energy consumption is usually achieved at the sub-threshold level, where the minimum energy point (MEP) is observed.[4,5] At sub-V_T level, the main driving current is the sub-threshold current (I_{SUB}), which is highly sensitive to changes in temperature and bias conditions. Performance is greatly affected by device variability, due to the devices' exponential sensitivity to source voltage,[4] and single event upsets (SEUs), due to its lower electric fields.[6]

Nowadays, beyond 32 nm technology nodes, vertical multi-gate devices (FinFETs) have replaced bulk planar devices in very large-scale integrated (VLSI) circuits in the quest of higher density, lower power and higher performance. These devices offer several advantages that give them a high potential to push back the integration limits: lower impact on short-channel effects, steeper sub-threshold slope, lower leakage current and relevant variability reduction.[7] FinFETs also introduce several reliability concerns, such as the self-heating effect. On top of that, scaling down device dimensions leads to lower node capacitances and, thus, increased sensitivity to ion impacts (i.e., SEUs[8]). SEUs are now one of the main reliability threats for sub-V_T circuits and specially for memories.[6] SEUs occur when an ionizing particle strikes a sensitive node (e.g., storing node), transferring energy that generates enough charge disturbances to flip a circuit node's data. To determine the robustness against SEUs, we compute the minimum charge required to upset a circuit node (i.e., the critical charge-Q_{crit}).[8] Initially, FinFETs provide a higher SEU robustness due to their 3D topology.[9] However, this advantage reduces as dimensions scale down. Plus, the use of lower V_{DD} generates small electric fields and drive currents within the cell devices, which increases vulnerability to SEUs. All of these reliability issues damage memory cell behavior. It is especially severe in SRAM as shown in Refs. [10–12]. In this context, gain-cell eDRAMs are more attractive than other memory cell proposals due to: (1) their higher density and better reliability;[13,14] (2) compatibility with mainstream CMOS processes; and (3) non-destructive read operations (in contrast to conventional 1T1C DRAM[15]). In order to

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hold the data, periodic refreshes are required[12] as the leakage current significantly reduces the DRAM's retention time (RT).[14] To introduce the gain-cells in the sub-V_T operating range is of great interest in areas such as biomedical applications where the power consumption of the CPU and memory accounts for 55% of the system's power.[1] Memory systems are usually based on SRAM cells; few studies have evaluated the use of gain-cell eDRAM-based systems at sub-V_T range.[3] Current state of the art in sub-V_T gain-cell eDRAM design mostly focuses on bulk CMOS devices. Although the continuous device dimension reduction has been questioned[16] and it is not trivial, FinFETs may be able to continue device scaling in smaller technologies; as shown in our previous work.[17]

The rest of this paper is organized as follows: Section 2 explains the device models used to simulate the FinFET gain-cell eDRAM and the simulation environment. Section 3 compares the performance and energy efficiency of different gain-cell eDRAM configurations. Section 4 reports the reliability study (variability and SEU) carried out on all the memory cells and different device types. Finally, Section 5 presents the conclusions of this work.

2. SIMULATION FRAMEWORK

This section presents the memory cells, the figures of merit, and the configuration parameters of the analysis.

2.1. Gain-Cell eDRAM Re-Design

Different eDRAM cells are usually considered to replace conventional DRAM capacitance-based cells (1T1C). 2T cells are the most likely to be implemented due to their higher integration level. Yet, 3T1D offer better reliability robustness.[13] In fact, 2T cells show good operability in the sub-V_T range for biomedical applications.[3] In this context, we have focused to analyze the feasibility of FinFET-based 2T and 3T1D eDRAM cells to operate at sub-V_T level. Figure 1 illustrates the schematics of the two gain-cell eDRAMs (2T and 3T1D). The baseline device to implement the gain-cell eDRAMs has always been 10 nm FinFET. These devices are based on the High-Performance Predictive Technology Models Multi-Gate (HP PTM-MG) environment.[18] Note that this paper complements a previous study[13] for nominal V_{DD} range (0.4–1 V). This version focuses on the analysis of sub-V_T-level performance; V_{DD} range is set between 0.16 and 0.3 V. When considering the complete system data path (e.g., sense amplifier, multiplexer, and flip-flop), memory cells become the critical component when variability occurs.[19] This is caused by their design with minimum device dimensions, which make them more susceptible to variations. Hence, we concentrate on the cell analysis. The following cell parameters are measured:

(a) *Retention Time* (RT), defined as the time required for the storage node voltage (V_S) in the cell to decay to V_{Smin}, (the minimum cell voltage that can be read at a given frequency[10]). This is used as the reference parameter to analyze the cells' suitability.

(b) *Dynamic Power consumption* (PW) obtained by the average value in one read/write cycle.

(c) *Write Access Time* (WAT), defined as the time elapsed between $V(WL_{write}) = (0.5 * V_{DD})$ and $V_S = (0.9 * V_{DD})$.

(d) *Read Access Time* (RAT), defined as the time elapsed between $V(WL_{read}) = (0.5 * V_{DD})$ and $V(BL_{read}) = (0.9 * V_{DD})$.

Previous papers [13], [20] report a significant performance improvement in gain-cell eDRAMs when *p*- and *n*FinFET devices are properly mixed in a cell. In fact, the use of pFinFET devices for write access transistors provides a longer retention time and better robustness against variability, due to their lower leakage currents.[13] Note that sub-V_T circuits underperform their above-threshold counterparts as the drive current (I_{SUB}) is significantly lower. To solve this problem, devices are often resized to improve their electrical behavior.[4] The increment in drive strength is usually achieved by increasing the device width (W), but it can also be achieved by increasing the channel length (L) in the sub-V_T regime.[4] Consequently, this paper explores the potential of upsizing the cell dimensions (i.e., L and W) to enhance cell performance. To this end, the following gain-cell eDRAM topologies are analyzed: (1) 2W cell, double width (W) of the cell devices; (2) 2L, double channel length (L) of all cell devices; (3) 2WL, double L and W of all cell devices; and, (4) mWL, double L of the write access transistor and double W of the rest of the cell devices. To double the device width in FinFET devices, we

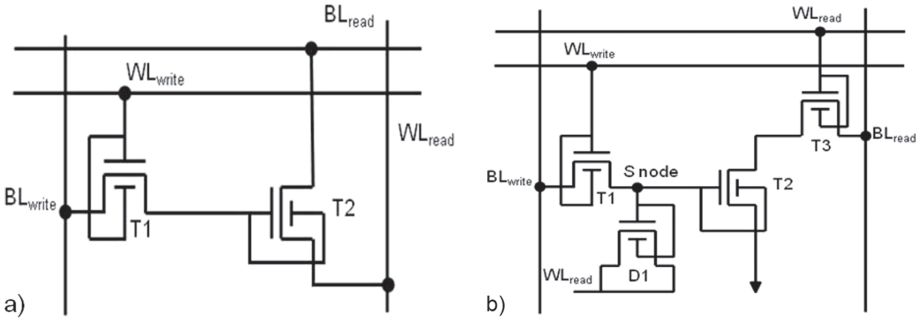

Fig. 1. Schematic structures for the gain-cell eDRAM: (a) 2T and (b) 3T1D. WL is wordline and BL is bitline.

double the number of fins in the transistor. Increasing the FinFET width means using a larger number of fins, which, in turn, leads to larger area overhead than when only the length is increased. In other words, increasing the write access device's channel length instead of its width causes a smaller increase in cell area. This smaller area overhead contrasts with the usual strategy, where the width of all devices is doubled ($2W$) for sub-V_T memory cells in order to improve overall performance.

2.2. Reliability Concerns for Studying eDRAM Cell Suitability at Sub-V_T Level

The continuous reduction of technology nodes towards a nanometer regime (<32 nm) has increased the impact of reliability effects on memory-cell behavior. Moreover, in the case of circuits operating at sub-V_T level, some reliability issues have taken on even more importance in terms of performance, such as process variations, changes in temperature, and soft errors.[21] This subsection describes the different reliability scenarios considered in the analysis of the gain-cell eDRAM's behavior.

The device fluctuation on the eDRAM cell parameters is determined by analyzing 10,000 sample Monte Carlo simulations. Experimental variability data is still not available so the variability impact is modeled by assuming a change in the threshold voltage (V_T) of the devices in the memory cell. In this regard, the process variation level is set as a 10% V_T shift. The relevance of the variability is evaluated using a statistical distribution with mean (μ) and standard deviation (σ), obtaining the ratio factor $3\sigma/\mu$, expressed as a percentage. The influence of the ambient temperature on the eDRAM performance is analyzed at −30, 25, 75 and 100 °C. Finally, all simulations take into account he self-heating effect of FinFETs through the consequent modification of the 10 nm FinFET model parameter.

To emulate SEU sensitivity of the memory cell at sub-V_T level, the impact of an ion strike is simulated with a pulse wave current obtained on 10 nm FinFET technology from 3D-TCAD simulations. Figure 2(a) depicts the

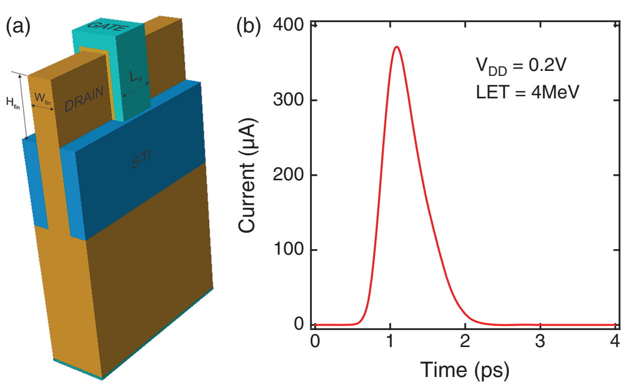

Fig. 2. (a) 3D-TCAD device representation. (b) Drain current pulse simulating the radiation impact on a 10 nm FinFET device.

Table I. 3D-TCAD 10 nm FiNFET dimensions.

Parameter	Description	Value (nm)
H_{Fin}	Fin height	21
W_{Fin}	Fin width	9
$L_{Channel}$	Channel length	14

FinFET 3D-TCAD device designed for this study, and Table I shows its main dimensions. Unlike the nominal voltage operational range, the current induced by the radiation impact has two main components (drift and diffusion), but when circuits operate at sub-V_T level, the single event effect (SEE) is mainly caused by diffusion.[6] In this sense, the SEU study is adapted to this concrete environment. Figure 2(b) shows the drain current pulse produced by the radiation impact of a Linear Energy Transfer (LET) of 4 MeV/mg/cm^2. All SEU studies are conducted at room temperature, since temperature has a negligible effect on Q_{crit}.[8] Only strikes occurring in the middle of the drain region with normal incidence are considered, as these account for most of the soft error upsets, even in scaled devices. The ion characteristic radius is about 10 nm, and maximum range is 160 nm. In the context of DRAMs, the most sensitive region is the drain region of the write access transistor as it is directly connected to the storage node voltage (V_S),[13] while the others are connected to the cell's word-line (WL) and bit-line (BL) (Fig. 1), which entails a high load capacitance at those nodes and, therefore, greater robustness to SEUs.

3. eDRAM CELL PERFORMANCE AT SUB-V_T RANGE

In this section, we compare the behavior of the two types of gain-cell eDRAMs (2T and 3T1D) at sub-V_T level, focusing mainly on RT. Both types of eDRAM mix p/nFinFET devices in the same cell. We also added an nFinFET-only 3T1D cell for comparison. Figure 3(a) shows the RT as a function of the V_{DD} at sub-V_T level (0.16–0.3 V) for all the cells. Note that the 3T1D-eDRAM cell is implemented by two different configurations, mixed and nFinFET-only. Although the mixed-based 3T1D and 2T had a similar evolution in terms of RT with V_{DD}, the gated-diode gain cell (3T1D) yielded higher RT values (65%), as shown in Figure 3(b). These findings are consistent with previous studies[13] at above-threshold voltage, where the 3T1D DRAM cell had the best performance. When the nMOS-only 3T1D eDRAM cells are compared to the mixed ones, the latter significantly achieve higher RT values (20×). Consequently, the mixed 3T1D cell is used in the rest of the paper as the baseline memory cell. It is worth mentioning that the RT values obtained can still be larger when considering layout strategies such as metal stacking.[3] Metal stacking increases the storage node capacitance, and consequently increase the overall retention time value of the gain-cells.

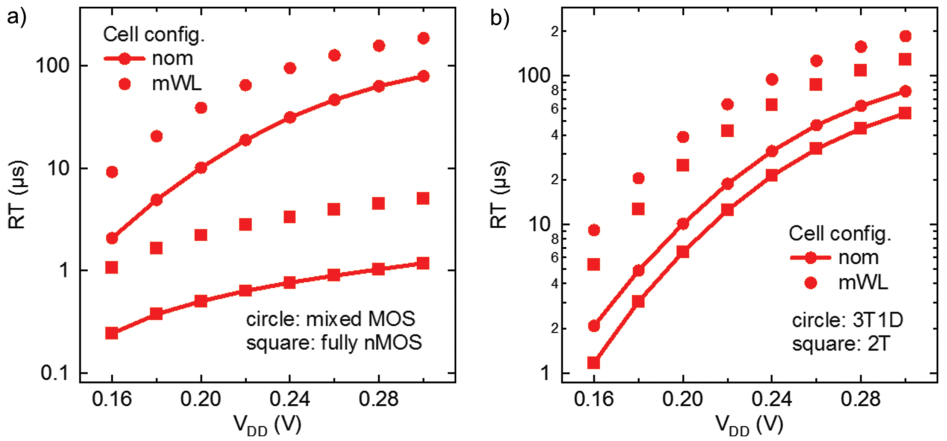

Fig. 3. RT of the different eDRAM cell configurations when V_{DD} is swept from 0.16 to 0.3 V under different cell scenarios: (a) Memory cell is fully implemented by nFET devices or when p and nFETs are mixed; and (b) 2T (squares) and 3T1D (circles). Mixed 3T1D cell yields higher RT values (65%) at sub-V_T level than the other two proposals.

3.1. Relevance of eDRAM Resizing Ant Sub-V_T Level

Next, we analyze the impact on RT of resizing the memory cell devices. Figure 4(a) shows that RT is higher when the cell is upsized for all of the cell proposals considered ($2W$, $2L$, $2WL$, and mWL). When only the W or L is increased, we observe a different RT trend. While the $2L$ cell has a better RT ($2\times$) at the ultra-low V_{DD} level (0.16–0.24 V), beyond that point, the RT values are similar to those of the nominal cell. In contrast, the opposite behavior is observed for the $2W$ cell: although the RT is initially almost the same as the nominal proposal, it improves ($2\times$) as V_{DD} increased. It is worth noting that the RT cross-point is observed around 0.25 V, close to the threshold voltage of the 10 nm PTM pFinFET devices used in this study for

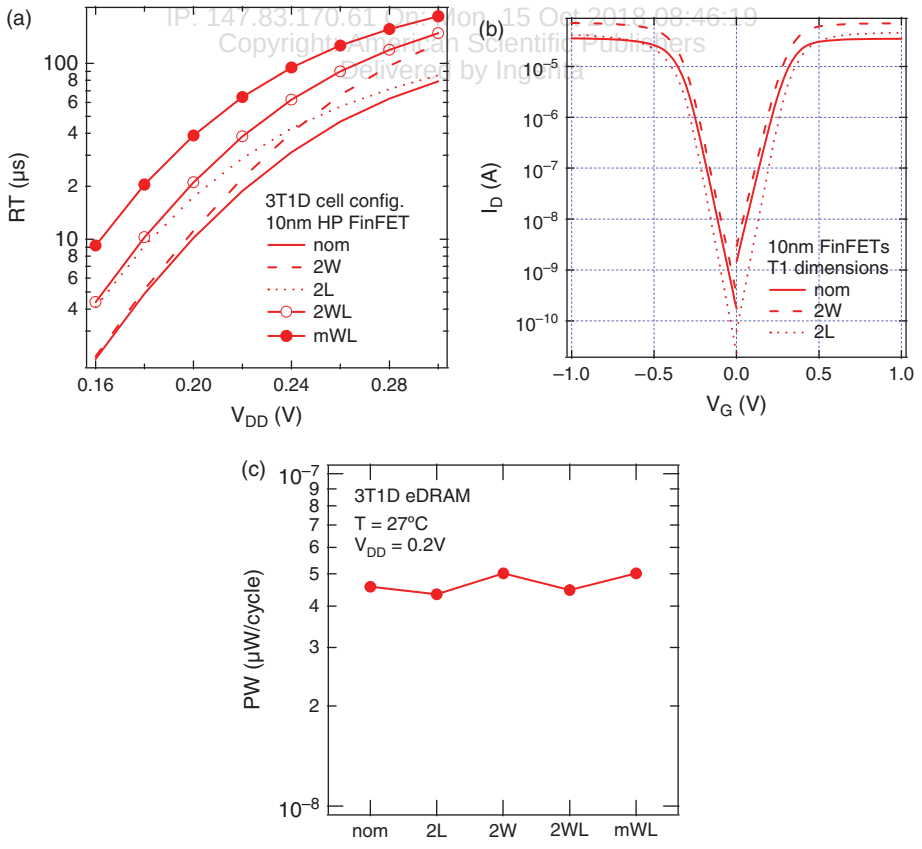

Fig. 4. (a) RT as a function of V_{DD} (0.16–0.3 V) when different device dimensions are considered; (b) $I_D - V_G$ curves for 10 nm PTM p/nFinFETs for different device dimensions. (c) Power consumption of the different 3T1D-eDRAM cells resizing strategies (nominal, $2L$, $2W$, $2WL$ and mWL).

the write access transistor (Fig. 4(b)). For the 2*WL* cell, the RT shows a more uniform increase (2×) as compared to the nominal cell for the entire V_{DD} range. Finally, the *mWL* proposal shows the largest increase in RT (3.5×). This improved performance of the asymmetrically upsized 3T1D-eDRAM cell can be explained by the larger subthreshold slope values and lower leakage current (I_{off}) values (Fig. 4(b)) as *L* increased in the write access pFinFET. These results corroborate the largest RT values obtained when the gain-cell devices are up-scaled[22] in other memory cells and using different technologies. In terms of memory cell power consumption, Figure 4(c) points out no relevant difference between the 3T1D-DRAM cells with different device dimensions strategies (nominal, 2*L*, 2*W*, 2*WL* and *mWL*) when V_{DD} is 0.2 V and it operates at room temperature. So, for next studies we will mainly focus on RT evolution as it is the most relevant parameter for the suitability of the eDRAM cells at sub-V_T level.

The working frequency of a memory circuit is usually determined by the longest access time, either WAT or RAT, obtained in the memory cell simulations. Then, in terms of access time, as expected, the different device dimensions resulted in different WAT and RAT values. In this context, Figure 5(a) shows the working frequency for different 3T1D-eDRAM cell proposals (nominal, 2*W*, and *mWL*). The 2*W* configuration achieves the highest frequency due to the larger drive current resulting from the cell devices' doubled *W*. In contrast, the *mWL* proposal has the lowest frequency value, although it is still within the usual operational range (>100 MHz) of sub-V_T memory circuits. Please note that these values are obtained regarding the performance of a single gain-cell memory. Note that a full memory data-path is not considered in this work.

It is important to pay attention to the ambient temperature influence on the different 3T1D-eDRAM cell device size configurations, as it is usually considered a limiting factor of circuit behavior. Figure 5(b) shows how temperature variations significantly affected RT values. Ultra-low V_{DD} (sub-V_T) circuits are highly affected by the temperature increase, as the RT reduces more significantly, due to the larger relevance of the leakage current as temperatures rise, since the I_{SUB} (driving current) is highly affected by temperature. This study compared the nominal-dimension cell with the *mWL* proposal. In general, all the cells have longer RTs when operating at −30 °C (significantly so at ultra-low V_{DD}). Likewise, all the DRAM cells shows a significant reduction in RT as the temperature rises up to 100 °C. In particular, the *mWL* proposal shows less RT degradation (49×) as a result of ambient temperature than the nominal case (64×). Similar trends are observed for the 2T-eDRAM cells, but they are not plotted here to avoid redundant information.

3.2. Energy Efficiency of the Different Cell Proposals

A system's energy efficiency can be monitored at the circuit's minimum energy point, defined as the voltage at which the total energy consumed per operation is minimized. The MEP is equal to the minimum value of the total energy consumed by a circuit,[4] which is the sum of the dynamic and static energies. Dynamic energy is related to circuit-switching activity and is usually determined as $1.2 * C * V_{DD}^2$, where *C* is the switched capacitance. Static energy usually corresponds to the circuit's leakage contribution, although it is also closely related to the circuit's delay ($V_{DD} * I_{leak} * t_d$).[4]

Figure 6 shows the different energy curves per operation depending on the V_{DD} for the baseline memory cell (3T1D) for each of the different gain-cell eDRAM proposals (i.e., nominal, 2*W*, 2*L*, and *mWL*). In terms of voltage at the MEP, while there are slight differences between the various cell configurations, the minimum value for all of them is around 0.2–0.22 V. Consequently, 0.2 V is used as the study's reference operating voltage for sub-V_T level gain-cell eDRAM operation to ensure maximum energy efficiency. In terms of energy consumption, the value for the *mWL* proposal is ~30% smaller than that for the 2*W* proposal.

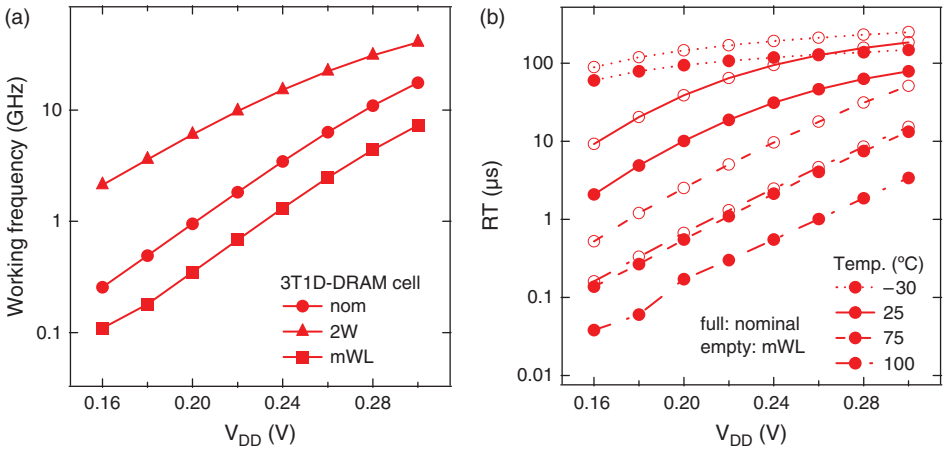

Fig. 5. (a) Working frequency considered for the different 3T1D-eDRAM cell proposals at sub-V_T level; (b) influence of ambient temperature on the different cell configurations.

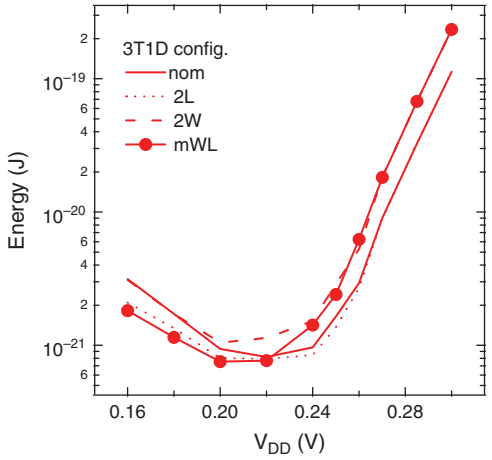

Fig. 6. Energy efficiency of the different 3T1D-eDRAM proposals (nominal, 2*W*, 2*L*, and *mWL*). Similar MEP voltages are observed for the different proposals, but energy consumption is ~30% lower for the *mWL* proposal than for the 2*W* one.

4. RELIABILITY OF THE eDRAM CELLS AT SUB-V_T LEVEL

Environmental conditions significantly affect memory cells performance and reliability, when they are designed to operate at sub-V_T level. For this, we have analyzed two different reliability issues—variability and SEU—to determine the suitability of the gain-cell eDRAM to operate at sub-V_T level.

4.1. Influence of Variability on the eDRAM Cells at Sub-V_T Level

Process variations have emerged as a relevant reliability factor as devices have been scaled into the nanometer regime. Sub-V_T circuits designed at these nodes are more prone to suffer variability, making it the main reliability concern.[4] This section examines the impact of process variations on eDRAM cells (2T and 3T1D) performance, in particular on RT. Specifically, it looks at the impact of a moderate level of variability (10%) on 10 nm FinFET-based gain-cell eDRAM. Although memory cell speed also suffers from variability impact, we focus on RT because we have regarded as the main eDRAM cells parameter. Figure 7 shows the RT change for all the 3T1D-eDRAM cells subject to device process variation ($3\sigma/\mu$) at sub-V_T level ($V_{DD} = 0.2$ V). As expected, the larger the device dimensions, the smaller the cell variability. However, RT decreases for all the resized eDRAM cells. The 2*WL* and *n*WEl show the smallest RT variation (~50%). Moreover, the *mWL* reduces the impact to 30% compared to the 2*W* with just a slightly smaller cell area. This can be attributed to the use of a longer channel length, which improves the sub-threshold slope.[5] It is worth to mention that 2T cells designed by using *mWL* cell configuration subjected to process variations, show larger RT variation (25%) compared to their 3T1D counterparts. This can be caused by the higher number of devices in the 3T1D and

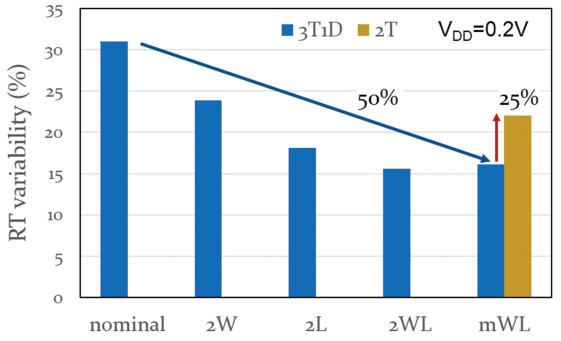

Fig. 7. RT deviation for the different eDRAM cell proposals subject to a 10% variability level, when operated at sub-V_T level ($V_{DD} = 0.2$ V).

the sharpened distribution obtained when gain-cell devices are up-sized.[22] For a more realistic analysis, we compute the manufacturing yield of a 32 kB cache memory block based on 3T1D cells, in a 10% variability scenario and operating at sub-V_T level ($V_{DD} = 0.2$ V). For this purpose, the circuit is evaluated with a reconfigurable array of 512 cells per column, for 512 columns, followed by 24 redundant columns.[23] In this context, 3T1D-eDRAM cells with RTs lower than 714 ns are considered defective, as such an RT value only ensures that the performance loss in a system based on 3T1Ds will be within ~2% of an ideal 6T design.[12] Figure 8 shows the results for the 32 kB 3T1D-eDRAM memory blocks based on the different cell upsizing proposals; all of them achieved a 99% yield under 10% device variability at room temperature (25 °C). When the ambient temperate changes, the retention time of the 32kB block falls significantly; and while at 75 °C (squares) only the *mWL* proposal meets the time criterion, at 100 °C (triangles) none of them do. This RT limit

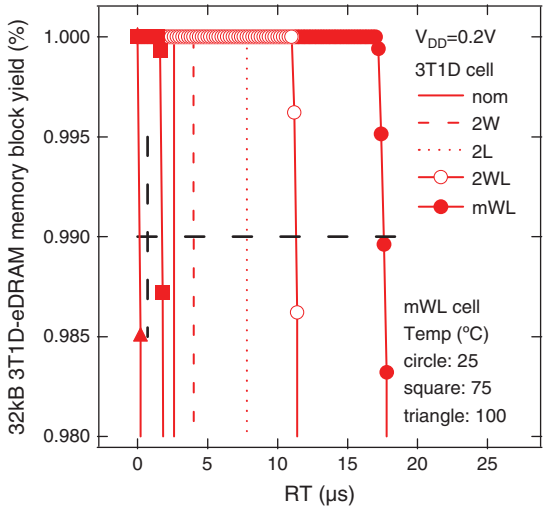

Fig. 8. Yield behavior for a 32 kB memory block based on 10 nm FinFET-based 3T1D cells subject to a 10% variability level for each of the different cell proposals (nominal, 2*W*, 2*L*, 2*WL*, and *mWL*) at sub-V_T level ($V_{DD} = 0.2$ V). Additionally, studies at high temperatures for the *mWL* 3T1D-eDRAM proposals are shown. Although the 32kB memory block met the timing criterion, 714 ns, at 75 °C (squares), at higher temperatures (100 °C, triangles) it did not.

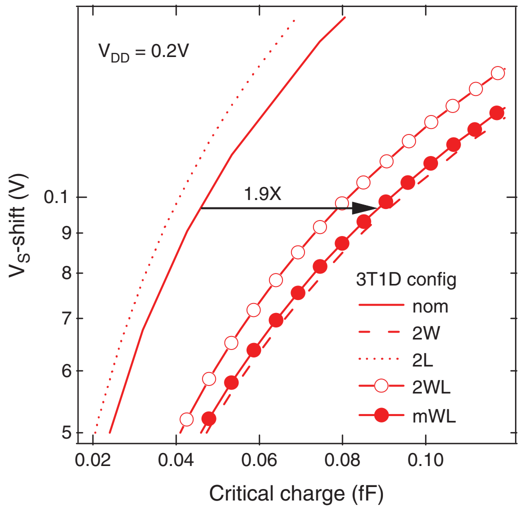

Fig. 9. Study of SEU impact on 3T1D-eDRAM cells. When using different device dimensions, larger injected charges are required to obtain a V_S-shift of $V_{DD}/2$ for the *mWL* configuration.

(714 ns) may seem a very aggressive regarding the refresh period, but there are different proposals for "refresh-free" cells, dual-ported memories, and other refresh optimization techniques.[12, 18]

4.2. Impact of SEUs on the eDRAM Cells

In the context of SEU analysis, only those ion impacts occurring in the drain region are considered (see Section 2.2). In particular, the devices connected to the storage node are the weakest, as they are the most sensitive node of the circuit. Thus, the only device significantly affected by an ion strike is the write access device, as the other devices are either connected to high capacitance lines, i.e., the bit-line (BL) and word-line (WL), or they exhibit a low influence on the cell performance following an ion impact.[13] Hence, we compare the relevance of the different configurations of upsized device dimensions used to implement the gain-cell eDRAMs at sub-V_T level ($V_{DD} = 0.2$ V). In this context, Figure 9 shows the influence of the device dimensions (nominal, $2W$, $2L$, $2WL$, and mWL) when considering a V_S-shift of $V_{DD}/2$ (i.e., loss of the stored data) as opposed to the critical charge required upsetting the node. In this regard, the *mWL* and $2W$ proposals are the most robust, as they have a larger Q_{crit} ($\sim 1.9\times$). This is related to the influence of the upsized transistors in the SER, specifically for the W increase.[8] Although the same trend ($1.8\times$) is observed for the 2T-DRAM (not included in the figure), the critical charge required to upset the node is smaller (50%), as previously reported in Ref. [13], indicating the higher robustness of the 3T1D memory cells to SEU.

5. CONCLUSIONS

Gain-cell eDRAMs for sub-V_T operation have been presented as a suitable option for ultra-low power memory systems. The best gain-cell device configuration mixes *p*- and *n*FinFET devices. This configuration can achieve $20\times$ higher RT at the sub-V_T operational level when compared to other alternatives. Per-device resizing also improves the RT of the cell for the FinFET-based cells at sub-V_T level. The best resizing comes with doubling the channel length of the write access transistor and the width of the rest of the devices (*mWL* proposal). *mWL* yielded the highest RT ($3.5\times$), due to its better subthreshold slope and the lower leakage. This proposal (*mWL*) entailed lower area overhead than the conventional strategy ($2W$). In terms of power consumption no significant impact is observed for the different cell configurations. Considering the working frequency, the *mWL* matches the usual values of the sub-V_T circuits ($\sim$100 MHz). The *mWL*-based 3T1D proposal shows a larger tolerance to operating at higher temperatures. The MEP is $\sim$0.2V V_{DD} for all the 3T1D cell proposals, but the *mWL* configuration consumes 30% less energy. In terms of process variations on sub-V_T 3T1D-eDRAM cells, the *mWL* proposal shows greater robustness (50%). In a 32 kB memory block configuration, the minimum RT criterion (714 ns) is met even at high ambient temperatures (75 °C). Finally, in relation to SEUs, the *mWL* proposal shows to be $1.9\times$ more robust, due to the larger critical charge required to upset the information node.

Summarizing, the asymmetrically sized gain-cell eDRAM implemented with 10 nm FinFET devices offers a clear improvement in terms of cell performance and reliability at sub-V_T level and for low power consumption memory cells.

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