Master Thesis

MSc Energy for Smart Electrical Networks and Systems (SENSE)

Capacitive Energy Balancing of Multilevel Submodules for Cascaded Converter in STATCOM Applications

MEMORY

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ABSTRACT

Cascaded converters also known as modular converters are used for STATCOM applications due to their small footprint, capability to achieve high voltage levels, modularity and reduced losses. A commonly used modular converter consists of a series connection of full-bridge also known as H-bridge cells or submodules. There is a wide area of research that focuses in various topologies of these submodules. In this project a new multilevel submodule has been proposed. This project investigates operational principles and capacitive energy balancing of this multilevel submodule that can be used in any type of modular multilevel converter. The investigation consists of analysis of the submodule circuit and its switching states, design and simulation of the modulation strategy as well as the capacitive energy balancing algorithm in the case when multiple submodules are connected in series forming a cascaded converter. Various methods of capacitive energy balancing that employ different ways of sorting capacitor voltages and deciding which capacitors/submodules should be inserted in the current path are investigated in this thesis. These energy balancing methods have been simulated and evaluated in terms of their impact on the capacitor voltage ripple and switching frequency of the new multilevel submodule. This evaluation results in the selection of the most promising energy balancing method, which is embedded in a simulation model of a three-phase STATCOM constructed with the proposed multilevel cells. Finally, the simulation model is used for evaluating the performance of the proposed multilevel cell and capacitive energy balancing method under steady-state and fault conditions, which would typically occur in a utility application.

Summary

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1. Introduction

1.1. Background and motivation

Most of the world's electric power supply is widely interconnected. This involves interconnections within utilities' own territories, inter-utility connections, inter-regional and international connections. This is done to reduce the cost of electric power supply and to improve its reliability. Transmission interconnection take the advantage of load diversity, availability of resources, and fuel price, to supply electricity to the loads at minimum cost with a required reliability [1].

Interconnected transmission systems are complex to operate, and the system can become less secure for riding through the major outages. Hence, they require careful planning, design and operation. The increasing electric power demand and the consequent growth of the electrical power system has put a lot of emphasis on system operation and control. These topics are becoming of more and more interest due to the recent trend towards restructuring and deregulating of the power supplies [2]. It is under this scenario that the use Flexible AC Transmission Systems (FACTS) technology opens up new opportunities for controlling power and enhancing the usable capacity of present, as well as new and upgraded transmission lines and prevent outages.

There have been many recent advances in the power electronics industry which have created a dramatic growth in the use of power electronic devices. FACTS devices are based on the integration of power electronics in the existing AC grid and distribution system to improve the stability and performance of the network. They can improve the efficiency of the electricity networks and the quality of consumer voltage waveforms [3]. Typically, FACTS devices are divided into two main categories: series-connected and shunt-connected configurations.

It has long been recognized that the steady-state active power transmission capability can be increased and the voltage profile along the line can be controlled by appropriate reactive shunt compensation [1]. Shunt-connected reactive power compensators are available based on both thyristor-based (named Static VAR Compensator, SVC) and Voltage Source Converter (VSC) technologies. The thyristor-based technology is today the preferred option for high-power installations (typically above several hundreds of MVAR). On the other hand, the VSC technology is the most suitable choice when higher speed of response and smaller footprint is needed. VSC technology also allows lower harmonic content in the injected/absorbed current as compared with the SVC. These items, together with a higher operational flexibility and good dynamic characteristics under various operating conditions (for example, large variations in

the short-circuit strength of the grid at the point of common coupling), indicate that the VSC technology is superior to the thyristor-based SVC for static shunt compensation [2].

Static Compensator (STATCOM) is a reactive power compensation device that is shunt connected to the AC transmission and distribution systems to increase the power quality by performing several compensations such as dynamic voltage control, power oscillations damping, and active and reactive power control in the transmission and distribution systems. The basic topology is based on VSC technology with power switches, a closed-loop control system which controls the ON-OFF state of switches, and output filters [4]. Furthermore, STATCOM can also be utilized in renewable-based power plants, mainly for grid-codes fulfillment and to allow fast reactive power compensation [2]. An interesting feature of STATCOM is that the DC side of the VSC can be incorporated as an energy storage, thus allowing temporary active power exchange (for example, to limit power fluctuations).

The main objective of a VSC is to produce an AC output waveform from a DC voltage source. These converters are constructed using power electronic switches, like IGBTs. In a VSC, each basic switching element is composed of a fully controllable, unidirectional semiconductor switch with a diode connected in antiparallel to it. There are various VSC topologies available today. The most fundamental of all these are the single-phase full bridge (H-bridge) and half bridge VSC as shown in Figure 1.

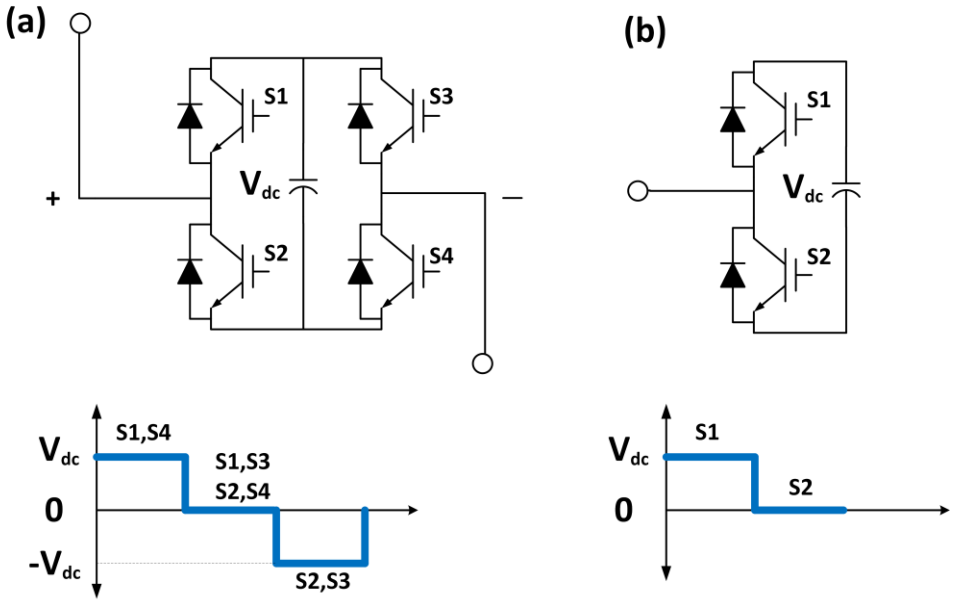


Figure 1: a) Full-bridge VSC b) Half-bridge VSC

The single-phase half bridge converter consists of one leg with two switching devices. This topology can be used to produce two-level output voltage waveform. The full bridge or H-bridge VSC consists of two legs, with two switching devices on each leg. With the same DC input voltage, the output of the full bridge is twice that of the half bridge. The full bridge VSC can be used to produce both two-level or three-level output voltage waveforms.

Depending upon the application, STATCOM can be used in different power levels. Based on different power levels, there are three-main areas for the STATCOM application as shown in Figure 2.

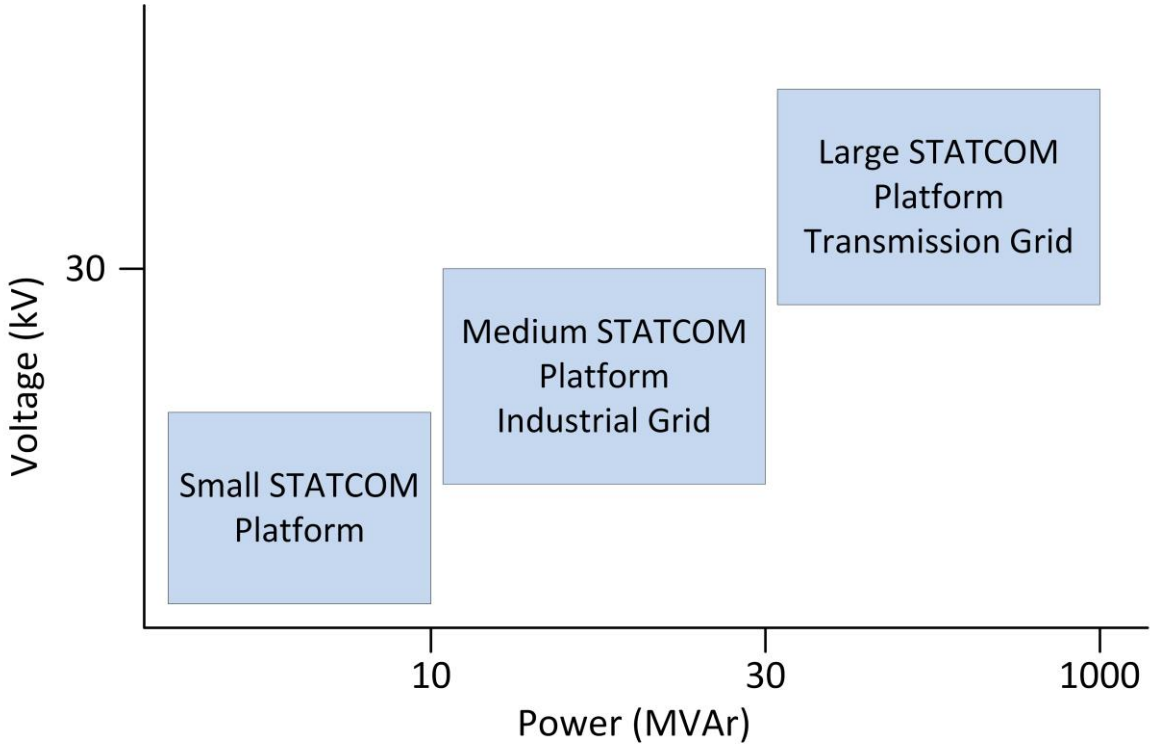


Figure 2: Power level of STATCOMs [4]

To implement the STATCOMs at medium and high-power levels, high power converters are needed, that in most of the cases exceeds the power handling capacity of a simple two-level converter without any device series/parallel connection [4]. For this reason, series connection of the static switches is needed in the VSC design for FACTS applications. Furthermore, there is a need to keep down the power losses, which severely limits the switching frequency that can be used in such installations, leading to relatively large filters being employed. For these reasons, in the last decades, multilevel converters have gained more and more attention for medium and high-power applications and to meet the imposed line side current and voltage harmonic distortion standards, without extending its device ratings [4].

The most popular examples of multilevel converters are the flying capacitor converter, neutral-point clamped converter, cascaded cell multilevel converter, and modular multilevel converter (MMC) [11][13][14]. A commonly used cascaded cell multilevel converter consists of a series connection of full-bridge also known as H-bridge cells or submodules. Here each cell consists of four semiconductor switches, for example Insulated-Gate Bipolar Transistor (IGBT) or Integrated Gate-Commutated Thyristor (IGCT), and one DC capacitor unit. The losses in semiconductor switches are dependent on both the switching of, as well as conduction by, the switches. In many FACTS converters, the conduction losses have a greater impact on the total loss than the switching losses.

To reduce the conduction losses, semiconductor switches having higher voltages can be used in full-bridge converters to reduce the number of submodules. However, reducing the number of submodules reduces the number of levels in the output voltage. Thus, a trade-off will be made between harmonic performance of the converter and the switching frequency of the switches. In FACTS application comprising of full-bridge converters, it is difficult to reduce the number of submodules beyond a certain point without negatively affecting the harmonic performance, and therefore the harmonic requirements of the power system cannot be met.

[18] describes an alternative to full-bridge submodules, wherein the number of submodules is reduced for a converter having the equal number of levels in the output voltage. In [15], a commutation cell is introduced that allows modularity and flexibility in terms of series or parallel connection of multiple cells. Adding multiple cells in series results in an increase in the number of levels in the output voltage, whereas a parallel connection of multiple cells enables single-fault safe operation. A modified topology for flying capacitor multicell converters (FCMC) has been proposed in [16]. The main advantage of the modified FCMC, as compared to the conventional one is that the number and voltage rating of the required DC voltage sources is halved. [17] presents a DC-AC interconnected modular multilevel converter (IMMC) for high performance AC motor drives, that produces sinusoidal output voltage with v/f control, no acoustic noise, low electro-magnetic interference (EMI), absence of dv/dt related issues due to long motor leads, and compact size/weight/volume.

There is still a need to reduce the losses even further, without lowering the quality in terms of harmonic performance of the cascaded converters. For this purpose, a new multilevel submodule has been proposed in this thesis. The aim of this submodule is to reduce the number of submodules in the cascaded converter, still providing a comparatively large number of voltage levels in the output.

1.2. Objectives of the project

A new multilevel cell has been proposed in this thesis with each cell capable of producing nine levels in the output voltage. This project aims at:

- Studying the proposed multilevel cell or submodule in detail
- Developing a modulation technique to obtain gate pulses for all the switches in the cascaded converter with proposed submodules
- Formulating an algorithm for balancing the energy in all the capacitors inside the cascaded converter with proposed submodules
- Comparing the proposed submodule against conventional full-bridge or H-bridge submodule
- Implementing delta-STATCOM using the cascaded converter with proposed submodules
- Evaluating the performance of STATCOM under steady-state and fault conditions which would typically occur in a utility application

2. Multilevel converter topologies and modulation technique

2.1. Introduction

The concept of multilevel converters was first introduced in 1975 [5]. Multilevel VSC uses an array of power semiconductor switches and several low voltage DC sources (realized by capacitors, batteries, and renewable energy voltage sources) to achieve high voltage at the output of the converter. The rated voltage of the power semiconductor switches in such multilevel VSC is only a fraction of the total DC voltage. The output voltage waveform of a multilevel converter is synthesized by selecting different voltage levels obtained from the DC voltage sources. By increasing the number of DC voltage sources (which increases the number of voltage levels at the output), the AC voltage produced at the output of VSC approaches a sinusoid. Hence, the increased number of levels provides the opportunity to eliminate more harmonic contents. Because of this, the filters become smaller and less expensive.

The number of levels of a multilevel converter are defined as the number of constant voltage values that can be generated between the output terminal and a reference node within the converter. Each phase leg of the converter must generate a minimum of three voltage levels to be included in the family of multilevel converters.

A multilevel converter has several advantages and disadvantages over a conventional two-level converter. Some of the advantages can be briefly summarized as follows [6][7][8][9].

- Multilevel converters generate the output voltages with lower distortion and reduced dv/dt stresses.
- For the same harmonic spectrum of the converter output voltage, the switching frequency of the power semiconductors can be much lower than in a two-level converter. This leads to lower switching losses and thereby higher efficiency.
- Since the rated voltage of the power semiconductor switches in such multilevel VSC is only a fraction of the total DC voltage, the stress across the power semiconductors reduces and consequently power semiconductors with lower ratings are required.

- Most of the time, a multilevel converter can be used at a reduced power level if a component inside the converter fails. Also, a desired voltage can be produced by more than one way in a multilevel converter as they have switching redundancies. This improves the system reliability.

On the other hand, some of the disadvantages of multilevel converters are as follows [6][7][8][9].

- A multilevel converter comprises of a greater number of power semiconductors which increases the probability of system failure.
- The increased number of switches in multilevel converter leads to complexity in the control and modulation of such a converter as compared to the conventional two-level converter.
- A multilevel converter requires several DC voltage sources, which are usually provided by capacitors. Balancing the voltages of these capacitors according to an operating point is a challenging task and requires more complex algorithms.

During the last two decades, several multilevel converter topologies have been proposed. These topologies can be broadly classified into two groups namely [4]; (i) Monolithic converters and (ii) Modular converters. The following sub-sections first briefly describe a few monolithic VSC topologies and then two modular topologies and their modulation techniques are discussed in detail.

2.2. Monolithic multilevel converters

Several monolithic multilevel converters have been proposed based on different structures of their DC voltage sources that generate staircase output voltage levels. The two most actively developed of these topologies are the diode-clamped multilevel converter and flying capacitor (also known as floating capacitor) multilevel converter. Let us now briefly look at these topologies, their operating principles, few advantages & drawbacks.

2.2.1. Diode-clamped multilevel converter (DCMC)

The first practical (and still widely studied) multilevel topology is the neutral-point-clamped (NPC) topology that was first introduced by Nabae et al., in 1981 [10]. This is an example of a

three-level diode-clamped converter. Figure 3 shows a three-phase three-level NPC.

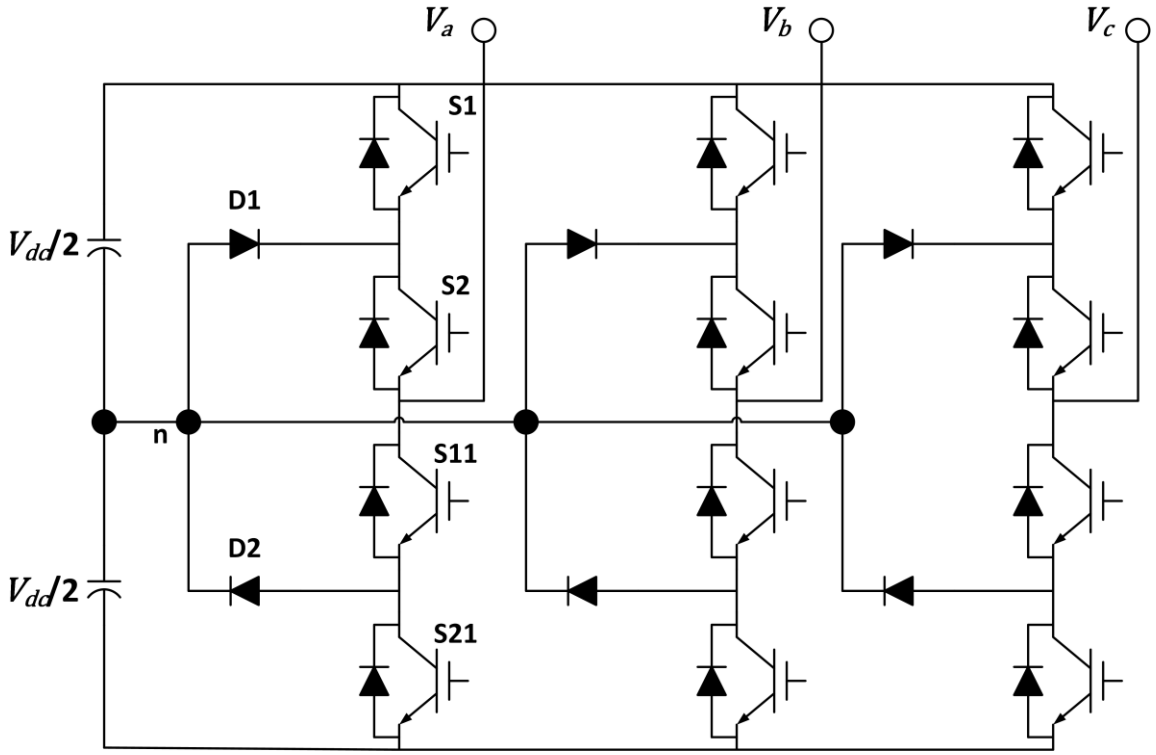


Figure 3: Three-phase three-level NPC

The NPC consists of two pairs of series switches (S1,S2 & S11,S21 in Figure 3), and two clamping diodes (D1 & D2 in Figure 3), in each phase. The DC-link consists of two capacitors connected in series. If the point 'n' is taken as the ground reference, the three-possible output phase voltage levels are $-V_{dc}/2$, 0, $+V_{dc}/2$. Table 1 lists the possible switching combinations for producing three-level output phase voltage for the topology shown in Figure 3.

Table 1: Switching scheme for NPC

S1	S2	S11	S21	V_n
1	1	0	0	$+V_{dc}/2$
0	1	1	0	0
0	0	1	1	$-V_{dc}/2$

In Table 1 ON state of each power semiconductor is represented by 1 and OFF state is represented by 0. Similar switching combinations are also valid for other two phases to produce corresponding three-level output phase voltages. The clamping diodes distinguish this circuit from a conventional two-level converter. These diodes clamp the voltage across switching device to half the level of the DC-link voltage.

Although it is theoretically possible to increase the number of levels, the use of NPC is limited to five-level due to increased complexity of the system, complexity of the control and large number of components required [7]. Asymmetrical distribution of losses among the semiconductors, which limits the switching frequency and the output power, is another limiting factor for the number of levels in NPC.

2.2.2. Flying capacitor multilevel converter (FCMC)

FCMC was first introduced by Meynard et al. and Foch in 1992 [11]. Figure 4 shows a three-phase three-level FCMC. The structure of FCMC is similar to that of NPC topology except that

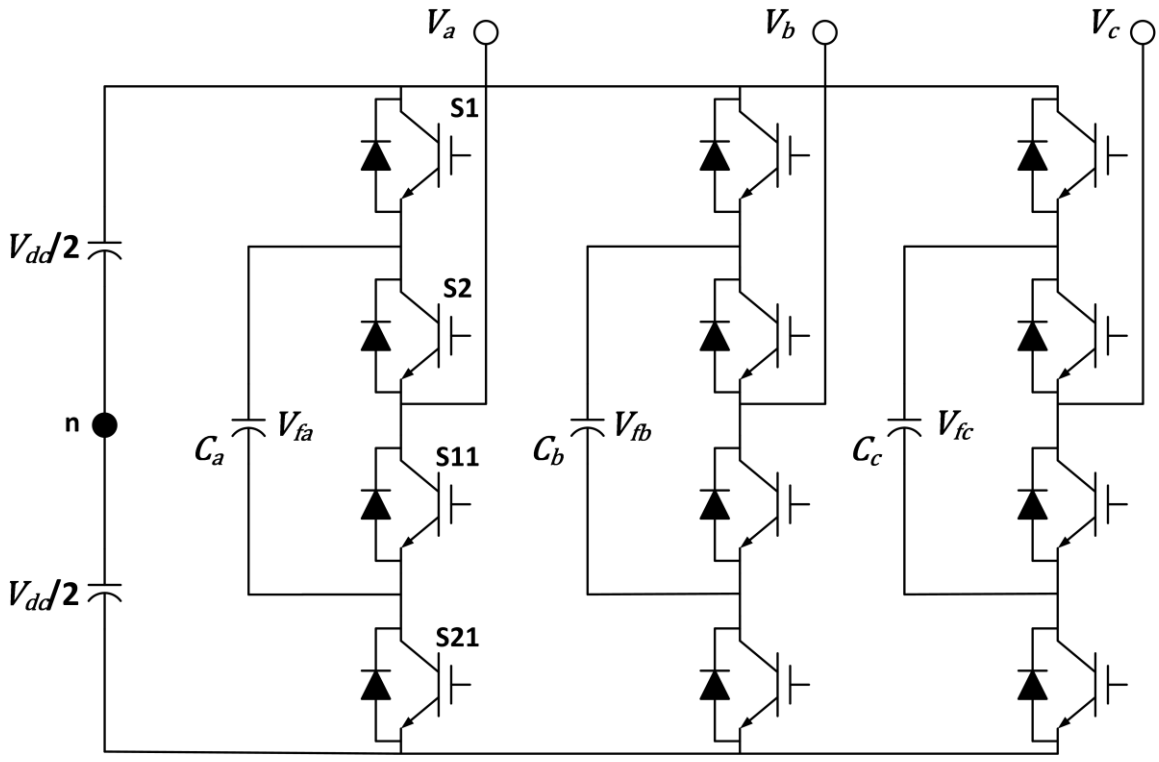


Figure 4: Three-phase three-level FCMC

instead of using clamping diodes, the converter uses capacitors. In FCMC, the clamping capacitors which are 'floating' with respect to DC source, are used to achieve multilevel

waveform and voltage clamping. These floating capacitors are commonly known as 'flying capacitors'. Table 1 lists the possible switching combinations for producing three-level output phase voltage for the topology shown in Figure 4.

Table 2: Switching scheme for three-level FCMC

S1	S2	S11	S21	V_n
1	1	0	0	$+V_{dc}/2$
1	0	1	0	0
0	1	0	1	0
0	0	1	1	$-V_{dc}/2$

In the FCMC topology shown in Figure 4, voltage across all the flying capacitors shown is regulated at $+V_{dc}/2$. By doing so, the voltage stress across the semiconductor devices is also limited to $+V_{dc}/2$. The flying capacitor voltage balancing is achieved by using voltage level redundancy i.e. using different switching combination available to generate same voltage level at the output of the converter [4].

High number of voltage levels requires a relatively higher number of capacitors in this topology. This can reduce the reliability of this converter. The size of the capacitors can also become large when using low switching frequencies (typically, for switching frequencies below 800-1000 Hz) [2].

2.3. Modular multilevel converters

Modularity in general refers to a technique to develop large systems by combining smaller and identical subsystems. For power converter topologies, modularity refers to a cascaded or series connection of converter cells, also known as submodules, forming a submodule string or chain-link. The number of levels in the output voltage can be increased very easily by simply adding more submodules. This seems to be an interesting solution to reach high voltage and high-quality waveforms.

Modular multilevel converters can be built by either connecting the basic building blocks, i.e.

half-bridge or H-bridge submodules, or by connecting submodules with monolithic multilevel topologies. First, let's discuss about the structure and modulation technique for a modular multilevel converter built using H-bridge submodules. Secondly, a new multi-level submodule will be introduced, and its operating principle will be discussed in detail.

2.3.1. Chain-link multilevel converters based on H-bridge submodules

A cascaded H-bridge converter is built using series connection of several H-bridges. As illustrated in Figure 1, a H-bridge can produce voltage waveforms with three discrete levels: $-V_{dc}$, 0, and $+V_{dc}$, where V_{dc} is voltage of its DC source. A H-bridge submodule producing $+V_{dc}$ or $-V_{dc}$ voltage level at its output is said to be inserted, otherwise bypassed. A series combination of several H-bridges should be able to produce more than three-level output voltage waveform. This forms the basis of the cascaded H-bridge converter. Figure 5 shows three-phase structure of a cascaded H-bridge converter with N_{cell} H-bridge submodules per phase.

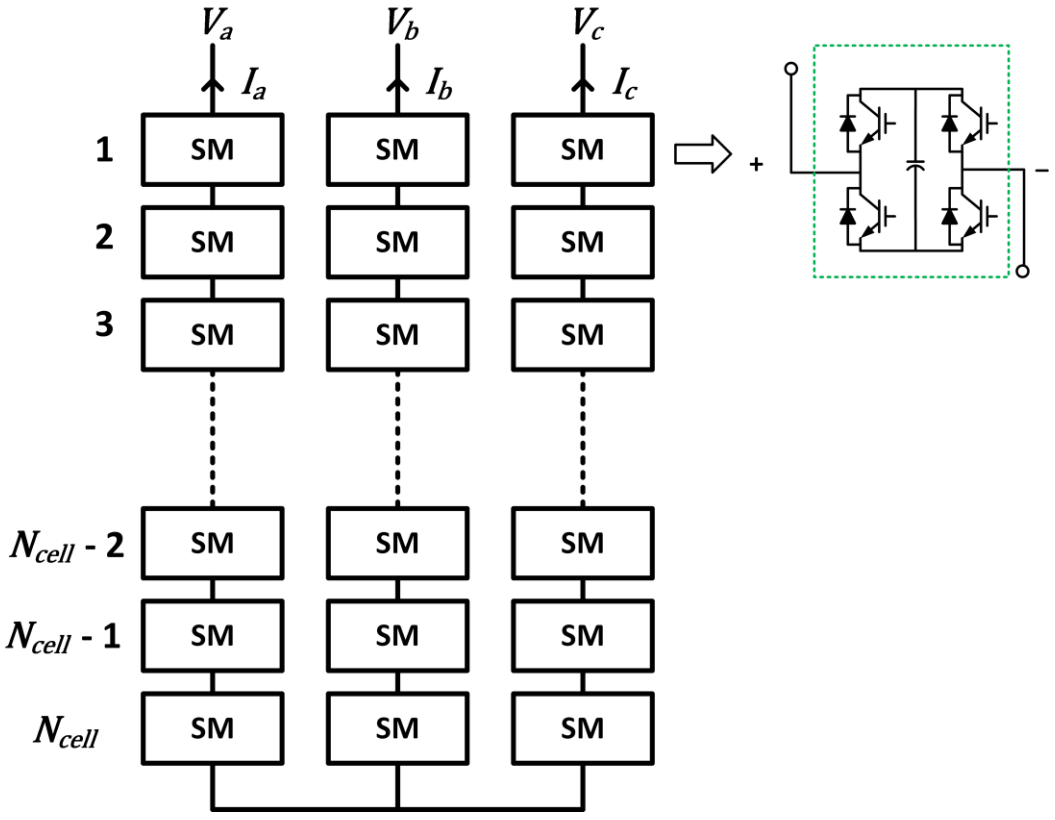


Figure 5: Three-phase structure of a cascaded H-bridge converter

It is evident from Figure 5 that H-bridge submodules are connected in series in a manner that

the synthesized voltage waveform of the cascaded converter is the sum of AC output of each submodule. The number of levels m in output voltage waveform of each phase of the cascaded H-bridge converter is given by $m = 2N_{cell} + 1$, where N_{cell} is the number of submodules in each phase.

2.3.1.1. Modulation technique for cascaded H-bridge converter

A power converter cannot provide a continuously varying output. Instead, the output voltage of the power converter can only assume a number of discrete levels. The purpose of any modulation technique is, therefore, to choose the instances for switching between the levels to ensure that the short-time average of the AC output voltage of the converter coincides with the reference signal over a switching cycle. For a sinusoidal reference this is equivalent to ensuring that the magnitude and phase of the fundamental component of the switched waveform should coincide with the reference. In addition to the desired low-frequency reference voltage, the switching process also produces higher-order harmonics which are undesirable and have several negative consequences on the equipment connected to the converter. In most of the cases, increasing the switching frequency reduces the harmonic content in the output voltage of the converter, at the cost of increased switching losses.

As discussed in the section 2.1, a multilevel converter topology allows for improved harmonic performance at a given switching frequency. In cascaded converter, where hundreds of submodules are used, resulting in a corresponding number of voltage-levels, this improvement is even more pronounced. Henceforth, the harmonic requirements are not decisive in determining the required switching frequency. There is still a need for suitable technique for selecting the number of submodules inserted at each instant. An additional purpose of the control scheme for a cascaded converter is to achieve voltage balancing between the submodule capacitors over time. This is achieved by appropriately selecting the submodules to be inserted or bypassed. Both the modulation and submodule balancing are concerned with the issue of when to switch the individual submodules and are therefore intimately linked to each other. Let us now discuss Nearest-level modulation scheme suitable for cascaded converters and a submodule energy balancing algorithm.

Nearest-Level Modulation (NLM) is a modulation technique that can be implemented with ease for multilevel converters. This technique is based on approximation of sinusoidal voltage reference to the nearest available level. This approximation is formulated mathematically by using $round(x)$ function, which approximates the continuous argument to the closest integer

as described in Equation 2.1.

$$round(x) = \begin{cases} floor(x) & x < floor(x) + 0.5 \\ ceil(x) & x \geq floor(x) + 0.5 \end{cases} \quad (2.1)$$

where, $floor(x)$ is the largest integer lower than x and $ceil(x)$ is the lowest integer higher than x. Thus, the reference waveform becomes a staircase. A challenge here is that the lower levels will be used for longer time as compared to the higher ones, potentially leading to unbalance in the submodule capacitor voltages. Hence NLM requires a submodule energy balancing algorithm for assigning the submodules to be inserted and bypassed. Figure 6 shows the concept of NLM.

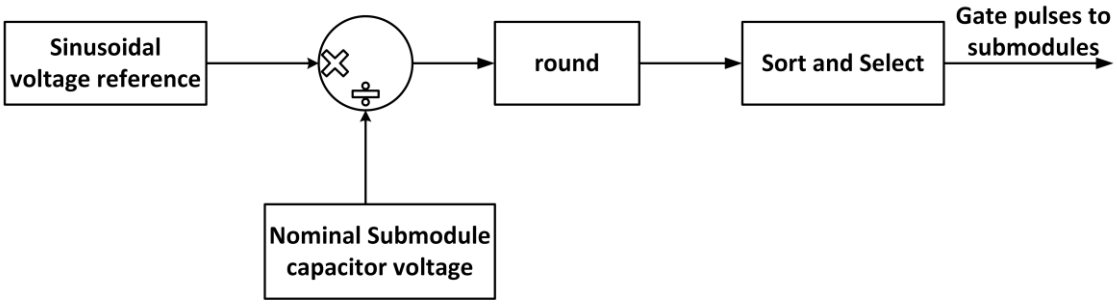


Figure 6: Nearest-level modulation concept

2.3.1.2. Submodule energy balancing algorithm for cascaded H-bridge converter

A submodule energy balancing algorithm is required along with NLM to balance the submodule capacitor energies, and thus limit the voltage differences among the submodule capacitors. The algorithm takes as input the staircase reference waveform that represents the number of submodules to be inserted at any instant, also known as insertion index N. Whenever this input signal changes by $+1$ or -1, the balancing algorithm selects the submodules to be inserted or bypassed in such a way that it brings the individual submodule capacitor voltages closer to their nominal voltages. In inserted submodules, the capacitors will be charged or discharged depending on the polarity of insertion and direction of the concerned arm current. In bypassed submodules, the capacitor voltages will remain unchanged.

The flow chart of the voltage balancing algorithm is shown in Figure 7. To select the submodules, the algorithm requires the direction of arm current I_x, and value of insertion index N as input. Based on the direction of arm current and insertion index, the algorithm selects the maximum or minimum voltage submodules selection logic as shown in Figure 8 and Figure 9 respectively. Instantaneous value of each submodule capacitor voltage is given as input to the

submodules selection logic. Inside this logic, each capacitor voltage is compared with other capacitor voltages and the output of each comparator is added together to obtain so-called priority order m_{h_k} or m_{l_k} of the corresponding submodule k. The priority order of each

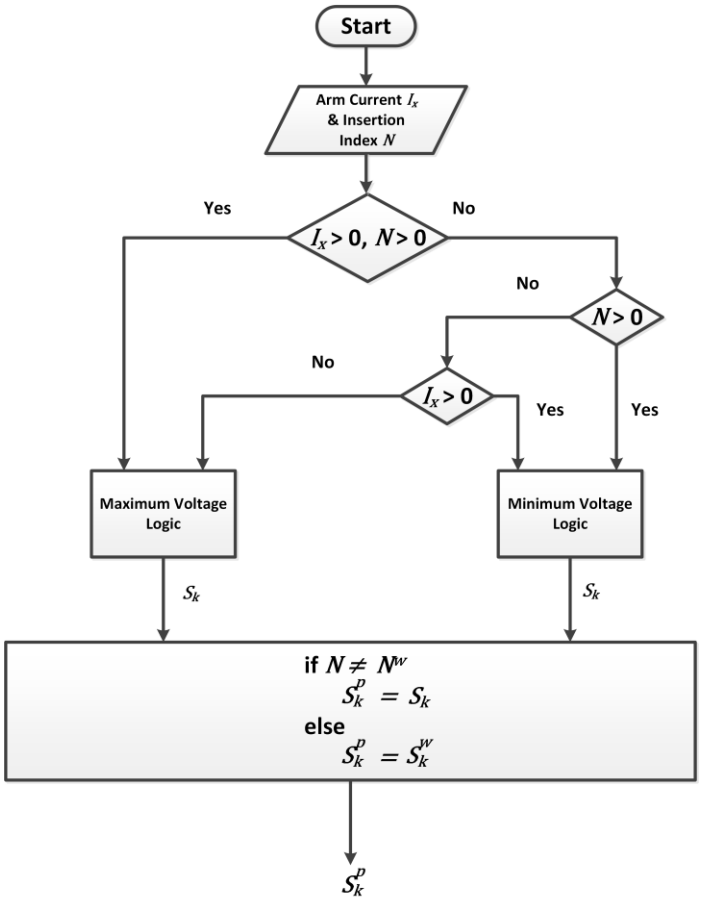


Figure 7: Flow chart of voltage balancing algorithm for cascaded H-bridge converter

submodule is then passed to the cell selector which then selects the submodules of higher priority for insertion. The number of submodules selected is equal to the insertion index. Finally, the switching state S_k is generated for each selected submodule. To minimize the device switching frequency, the present value of insertion index N is compared with the previous value of insertion index N^w. If the present and previous values of insertion index are equal, then the algorithm will keep the previous switching state S_k^w of each submodule. By using this approach, the device switching losses can be reduced.

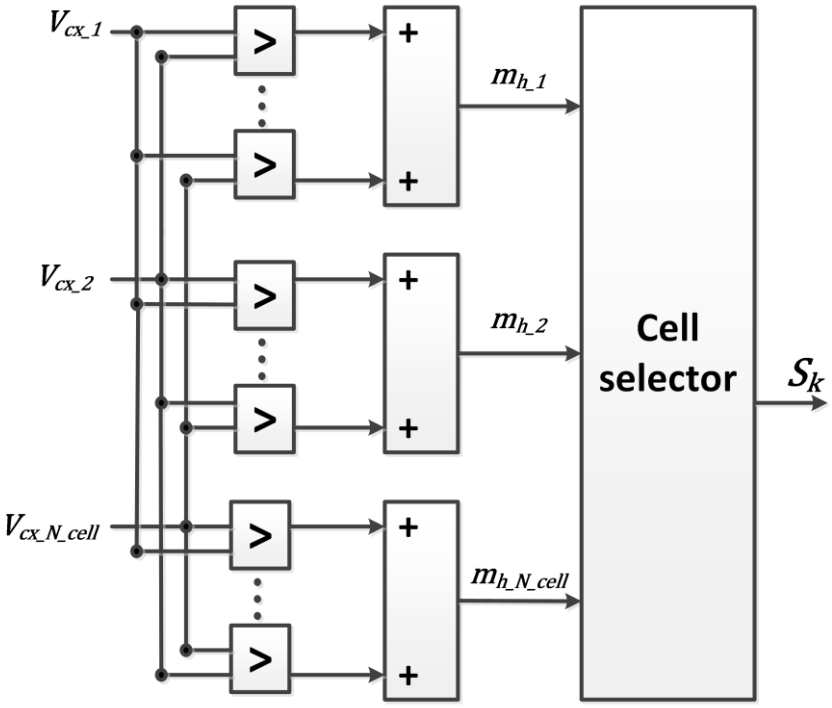


Figure 8: Maximum voltage submodules selection logic

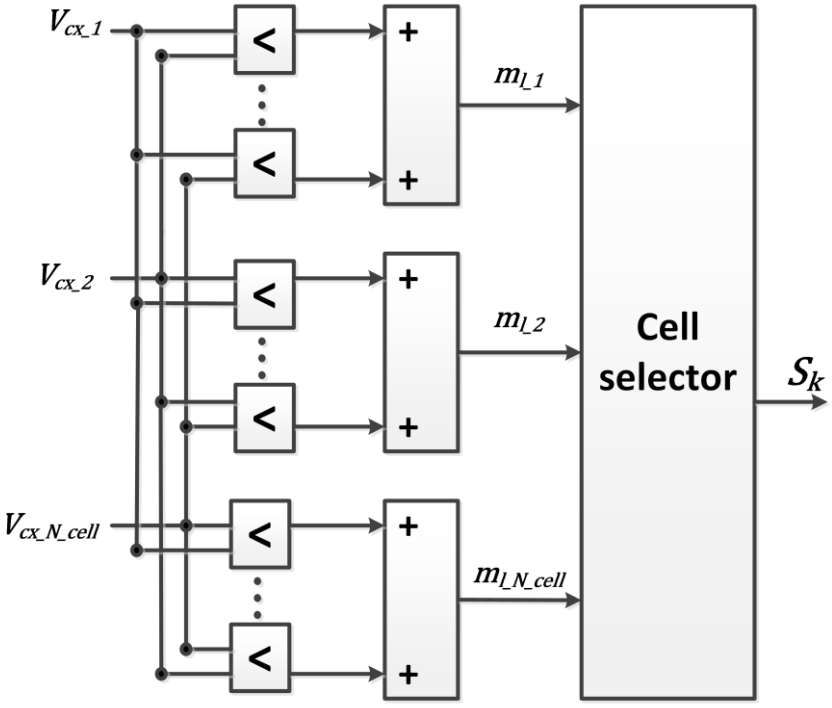


Figure 9: Minimum voltage submodules selection logic

2.3.2. A new multilevel converter topology

Figure 10 shows a new multilevel converter topology. This converter topology was invented by Alireza Nami and Christopher Townsend in 2016 [12]. From Figure 10 we can see that the submodules, marked by dotted green line, form a building block for the converter. The series connection of such submodules allows a scalable and modular layout for the converter. Each submodule in this topology comprises of three capacitors, and two switching devices as seen in Figure 10.

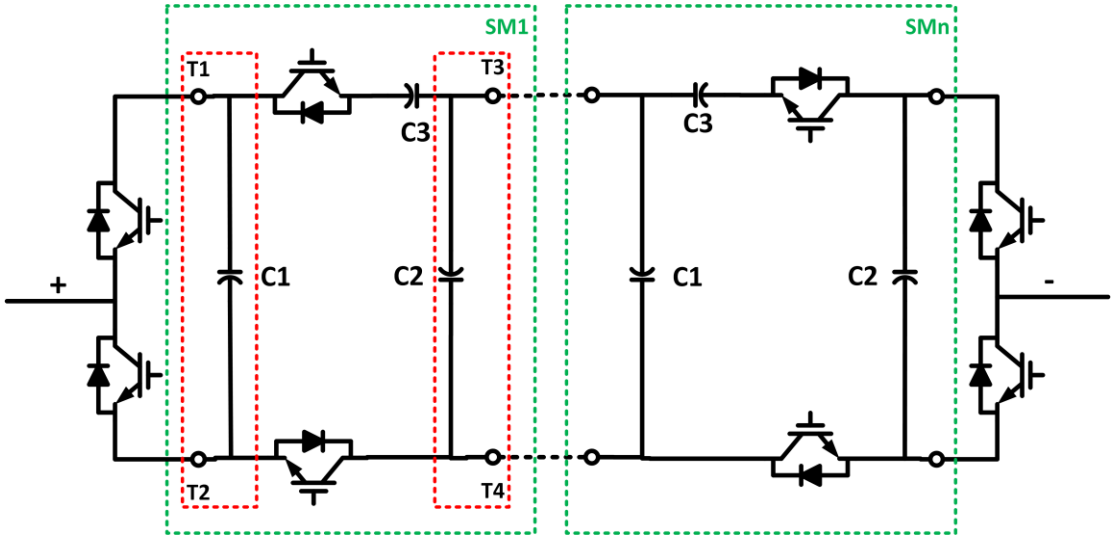


Figure 10: Proposed multilevel converter topology

A series connection of two such submodules leads to a nine-level converter as shown in Figure 11. It comprises of eight switching devices (S1, S2, S3, S4, S5, S6, S7, & S8), and six capacitors (C1, C2, C3, C4, C5, & C6). The parallel combination of two capacitors C2 and C5 in Figure 11 can be replaced by a single capacitor. Henceforth, it is assumed that all the capacitors in the converter are of equal capacitance and are initially charged to the nominal voltage of $1\ p.u.$. Switching devices S1, S2, S3, and S4 have a reverse blocking voltage of $1\ p.u.$, whereas switching devices S5, S6, S7, and S8 have a reverse blocking voltage of $3\ p.u.$. This converter can produce an output voltage waveform comprising of nine distinct voltage levels $(0, \pm 1\ p.u., \pm 2\ p.u., \pm 3\ p.u., \pm 4\ p.u.)$. Hence, this converter topology is equivalent to a cascaded H-bridge converter comprising of four H-bridge submodules.

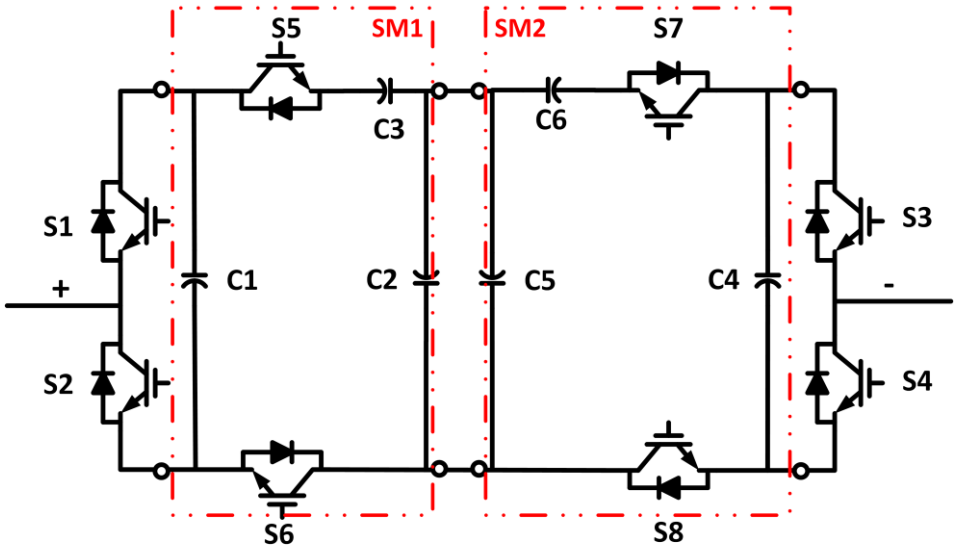
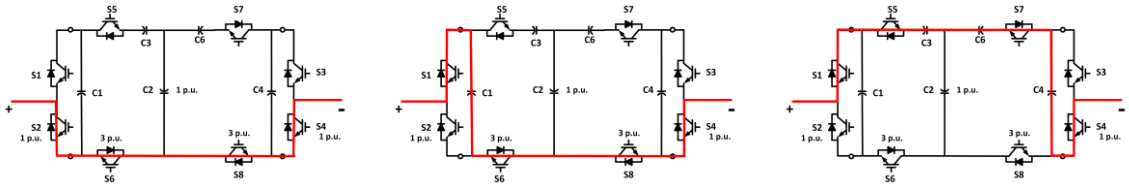


Figure 11: Nine-level converter

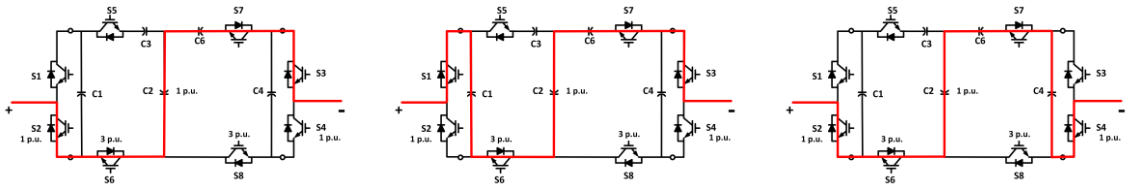
Figure 12 shows different switching states for the nine-level converter and their corresponding output voltage levels. It can be seen from Figure 12 that redundant switching states exit for $\pm 1\ p.u.$ and $\pm 3\ p.u.$ output voltages. These redundancies can be used for balancing the energy of all the capacitors in the converter.

2.3.2.1. Modulation technique for the nine-level converter

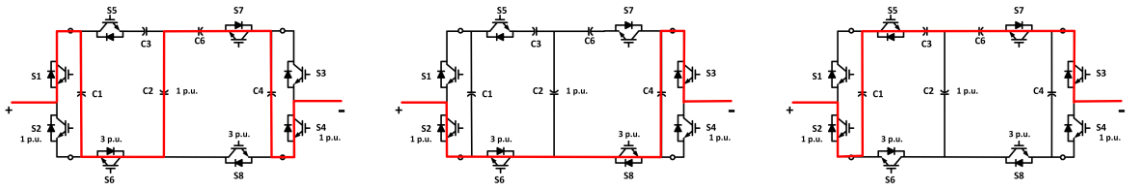
A modified NLM technique is described below for obtaining the gate pulses for the switching devices in the nine-level converter. This technique is based on mathematically calculating the pulse-width of each discrete level in the reference voltage waveform $v(t)$, to obtain a staircase waveform as shown in Figure 13.



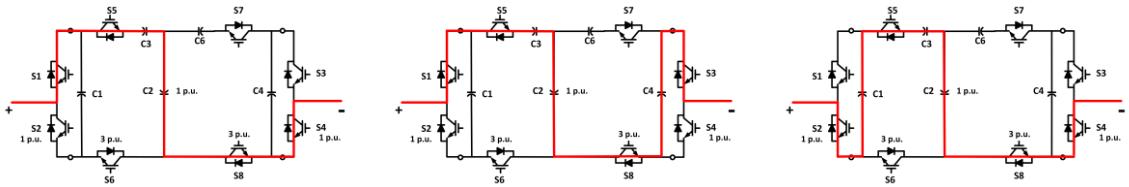
$V_{out} = 0\ p.u.$ $V_{out} = +1\ p.u.$ $V_{out} = +1\ p.u.$



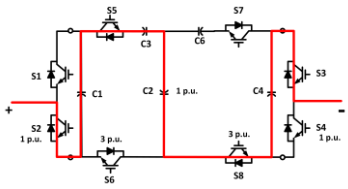
$V_{out} = +2\ p.u.$ $V_{out} = +3\ p.u.$ $V_{out} = +3\ p.u.$



$V_{out} = +4\ p.u.$ $V_{out} = -1\ p.u.$ $V_{out} = -1\ p.u.$



$V_{out} = -2\ p.u.$ $V_{out} = -3\ p.u.$ $V_{out} = -3\ p.u.$



$V_{out} = -4\ p.u.$

Figure 12: Nine-level converter switching states and corresponding output voltage levels

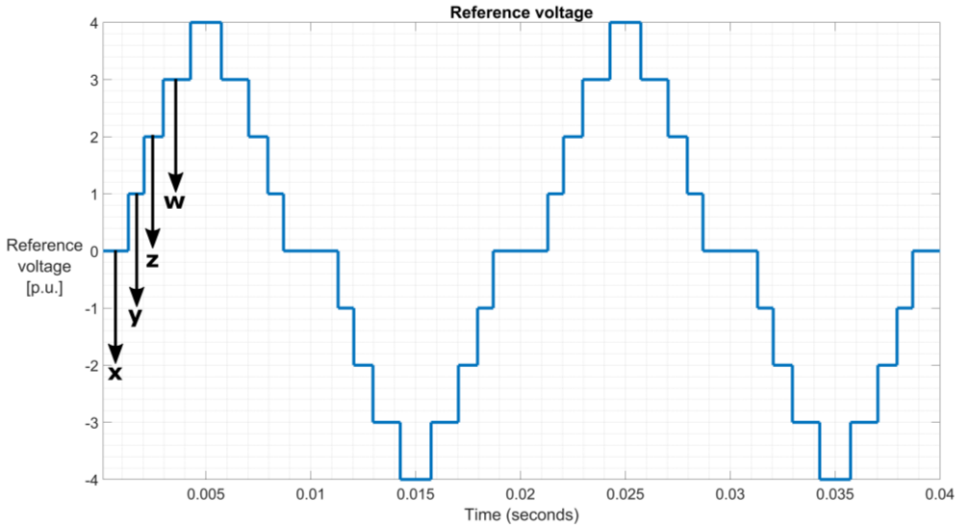


Figure 13: Modified NLM reference voltage waveform

Pulse-widths of each discrete level $(x, y, z, \& w)$ shown in Figure 13 is calculated by solving system of equations concerning:

- Amplitude of the fundamental component of reference voltage
- Deviation in voltage levels of submodule capacitors

The reference voltage waveform $v(t)$ shown in Figure 13 is a periodic waveform of zero mean and a period $T_1 = \frac{2\pi}{w_1}$, where w_1 is the angular frequency (nominal value of $100\pi\ rad/s$). This waveform can be expanded into Fourier series as,

$$v(t) = \sum_{h=1}^{\infty} a_h \cos hw_1 t + b_h \sin hw_1 t \qquad (2.2)$$

where

$$a_h = \frac{w_1}{\pi} \int_{-\frac{T_1}{2}}^{\frac{T_1}{2}} v(t) \cos hw_1 t\, dt \qquad b_h = \frac{w_1}{\pi} \int_{-\frac{T_1}{2}}^{\frac{T_1}{2}} v(t) \sin hw_1 t\, dt \qquad (2.3)$$

In Equation 2.2, $h = 1$ gives the fundamental component. The amplitude of the fundamental component $\hat{V}_1$ is given by,

$$\hat{V}_1^2 = a_1^2 + b_1^2 \qquad (2.4)$$

Using Equation 2.3 and Equation 2.4 we get,

$$\hat{V}_1 = \frac{4}{\pi}[\cos w_1(x) + \cos w_1(x+y) + \cos w_1(x+y+z) + \cos w_1(x+y+z+w)] \qquad (2.5)$$

Now let us assume that an ideal sinusoidal current $i(t)$, phase shifted by $-\pi/2$ from fundamental component of reference voltage (for STATCOM application) as shown in Figure 14 , is flowing through the nine-level converter shown in Figure 15.

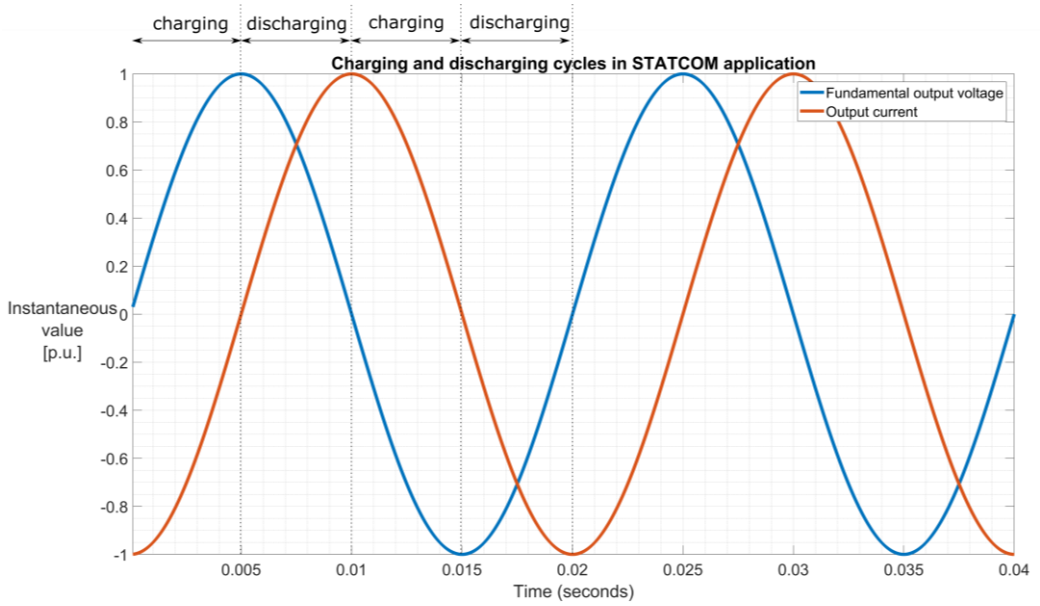


Figure 14: Charging and discharging cycles for STATCOM application

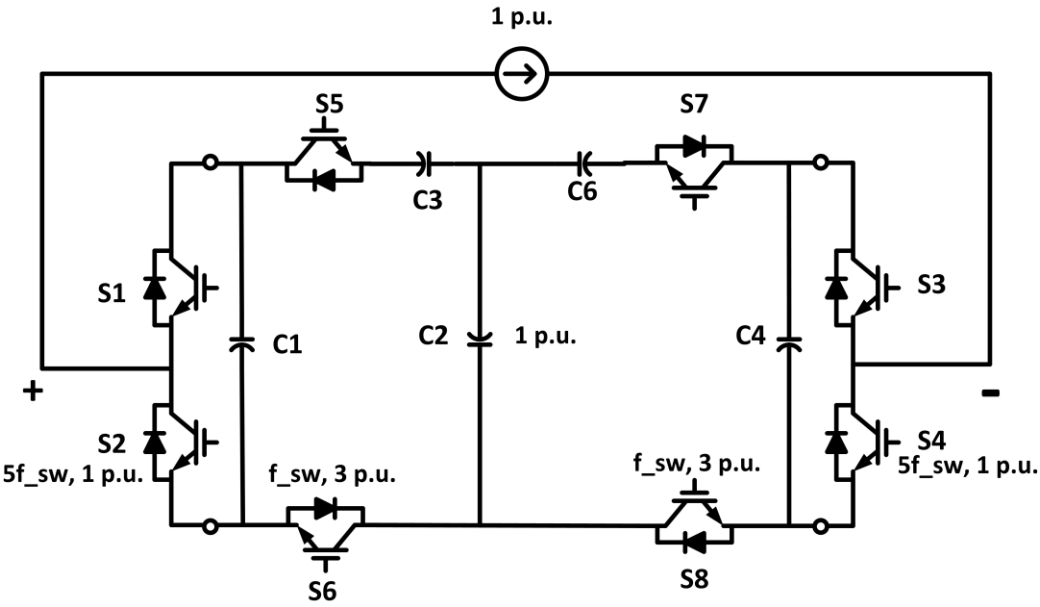


Figure 15: Nine-level converter simulation circuit

Without using the redundant switching state, if the switching state with capacitor 'C1' inserted is used to produce $+1\ p.u.$ level in the output voltage during charging cycle, the deviation dV_{C1} in the voltage level of capacitor 'C1' during this interval is given by,

$$dV_{C1} = \frac{1}{C}\int_{x}^{x+y} i(t)dt \qquad (2.6)$$

where, C is the capacitance of each capacitor in Figure 15.

The deviations dV_{C2} in the voltage level of capacitor 'C2' and dV_{C6} in the voltage level of capacitor 'C6' during $+2\ p.u.$ level in the output voltage are equal, as they are inserted in series during this interval and are given by,

$$dV_{C2} = dV_{C6} = \frac{1}{C}\int_{x+y}^{x+y+z} i(t)dt \qquad (2.7)$$

If the deviations dV_{C1}, dV_{C2}, & dV_{C6} are ensured to be equal at the end of $+2\ p.u.$ level in the output voltage during charging cycle, the energies in three capacitors 'C1', 'C2', & 'C6' will get balanced at the end of this interval. These energies will remain balanced until the end of $+3\ p.u.$ level in the output voltage during discharging cycle, if the switching state with capacitors 'C1', 'C2', & 'C6' inserted is used to produce $+3\ p.u.$ level in the output voltage. The deviation dV in the voltage level of capacitors 'C1', 'C2', & 'C6' during $+3\ p.u.$ level in the output voltage is given by,

$$dV = \frac{1}{C}\int_{x+y+z}^{x+y+z+w} i(t)dt \qquad (2.8)$$

Setting the desired amplitude of the fundamental component of reference voltage and the deviations in the voltage level of capacitors, Equations 2.5, 2.6, 2.7, & 2.8 can be solved analytically to obtain the pulse-widths of each discrete level $(x, y, z, \& w)$ shown in Figure 13.

By using this kind of feed-forward approach, and not utilizing the redundant switching states available for $\pm 1\ p.u.$ and $\pm 3\ p.u.$ output voltages, maximum voltage ripple in each capacitor within the nine-level converter can be controlled, and energy in all the capacitors can be balanced in one fundamental cycle.

2.3.2.2. Simulation results

The circuit shown in Figure 15 was used to perform the simulations in Simulink. The capacitors used in the circuit were dimensioned to obtain a total arm energy of $20\ kJ/MVA$. Figure 16 shows the ripple in the capacitor voltages and the output voltage waveforms for modulation index of 1.0. It can be seen clearly from Figure 16 that the maximum voltage ripple in each

capacitor within the converter can be controlled to 12% and capacitive energy balancing can be ensured within one fundamental cycle, using the modified NLM technique discussed in the section 2.3.2.1.

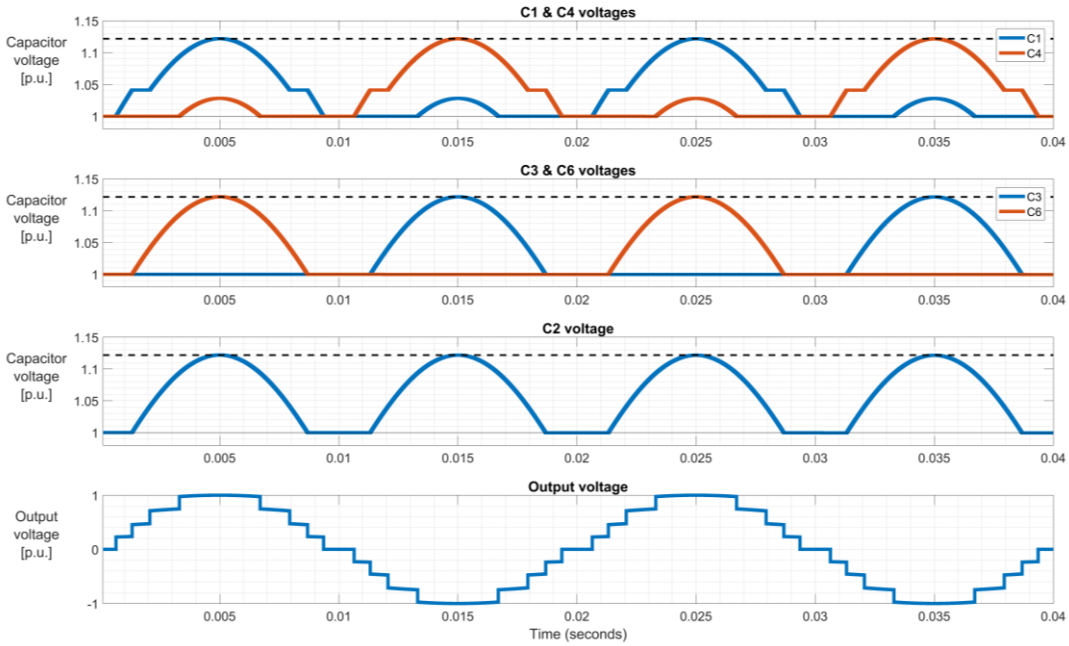


Figure 16: Capacitor voltage ripple and output voltage waveforms for modulation index 1.0

Figure 17 and Figure 18 shows the ripple in the capacitor voltages and the output voltage waveforms for modulation index of 0.8 and 0.5 respectively. It can be seen from Figure 16, Figure 17, and Figure 18 that the modified NLM technique works well over a range of modulation index.

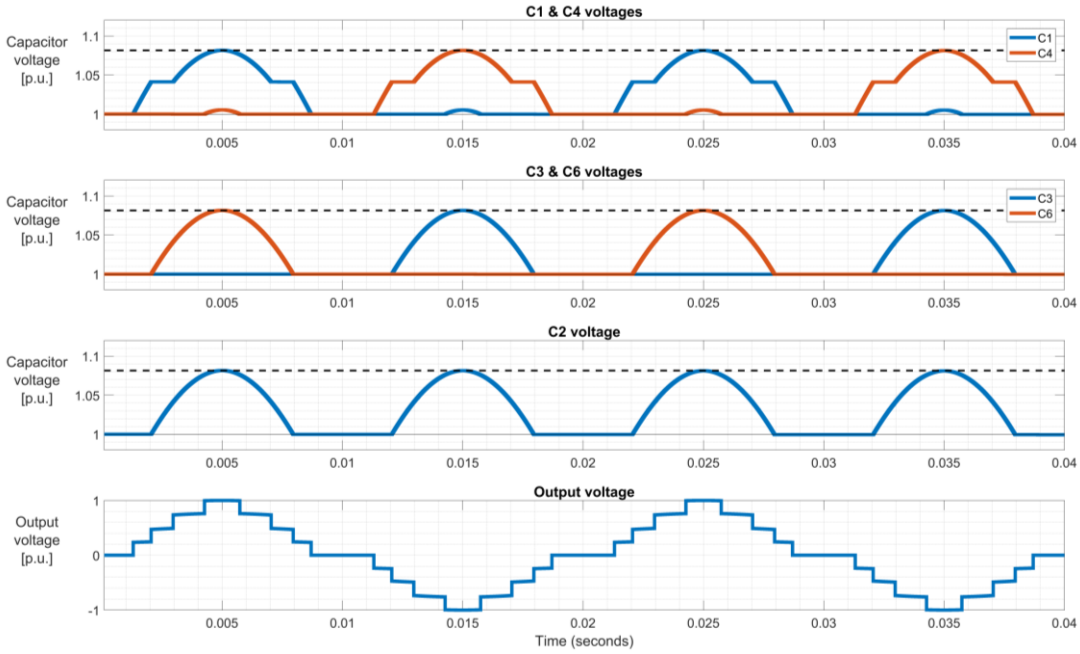


Figure 17: Capacitor voltage ripple and output voltage waveforms for modulation index 0.8

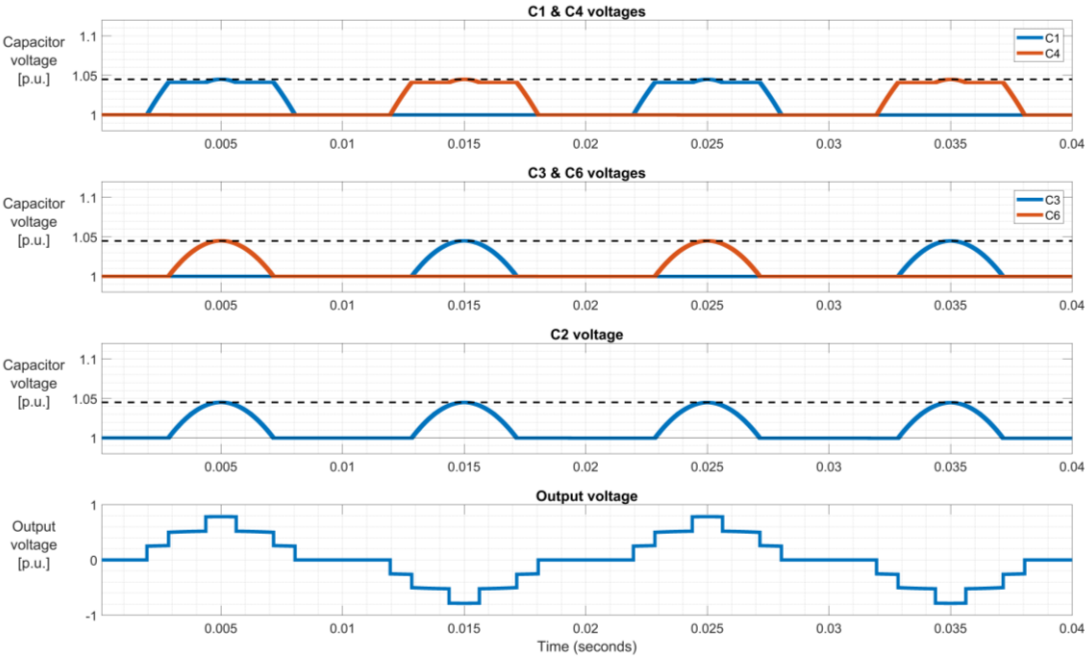


Figure 18: Capacitor voltage ripple and output voltage waveforms for modulation index 0.5

3. Chain-link multilevel converters based on submodules with monolithic multilevel topology

As discussed in section 2.3, modular multilevel converters can be built by either connecting the basic building blocks, i.e. half-bridge or H-bridge submodules, or by connecting submodules with monolithic multilevel topologies. In this chapter we will discuss about a chain-link built using the nine-level converter topology shown in Figure 11 as cells or submodules. Let us now discuss the modulation technique and capacitive energy balancing scheme for the cascaded converter shown in Figure 19, built using proposed submodule.

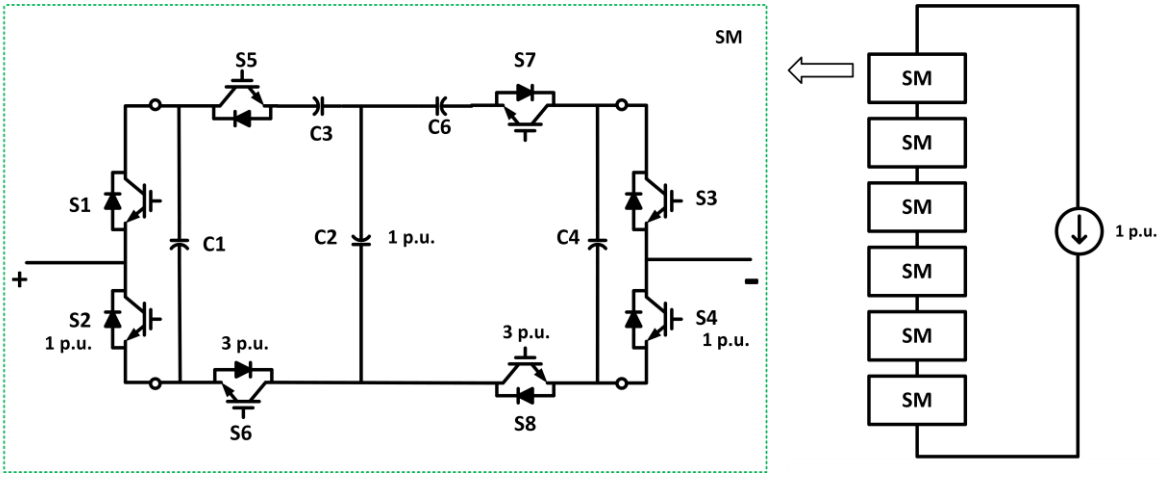


Figure 19: Cascaded converter with proposed submodule

3.1. Modulation and Balancing Scheme

The cascaded converter shown in Figure 19 consists of six submodules, with each submodule producing voltage waveforms with nine discrete levels as discussed in section 2.3.2. Hence a series connection of such submodules shown in Figure 19 can produce voltage waveform with forty-nine discrete levels.

NLM technique discussed in section 2.3.1.1 is used to modulate the converter shown in Figure 19 due to its simplicity in implementation. As stated in section 2.3.1.1, NLM requires a submodule energy balancing algorithm. The submodule energy balancing algorithm for cascaded converter with multilevel cells needs to ensure that both the capacitive energy within

the cells (intra-cell) and that between the cells (inter-cell) is balanced. Let us now discuss the proposed energy balancing algorithm in detail.

The proposed submodule energy balancing algorithm is used to limit the voltage differences among all capacitors in the arm of the converter. The algorithm takes as input the staircase reference waveform that represents the number of capacitors to be inserted at any instant, also known as insertion index N and number of submodules N_{cell}. Whenever the insertion index N changes by $+1$ or -1, the balancing algorithm selects the capacitors to be inserted or bypassed in such a way that it brings the individual capacitor voltages closer to their nominal voltages. The inserted capacitors are charged or discharged depending on the polarity of insertion and direction of the arm current. In the bypassed capacitors, their voltages will remain unchanged. The flow chart of the proposed submodule energy balancing algorithm for cascaded converter with multilevel cells is shown in Figure 20.

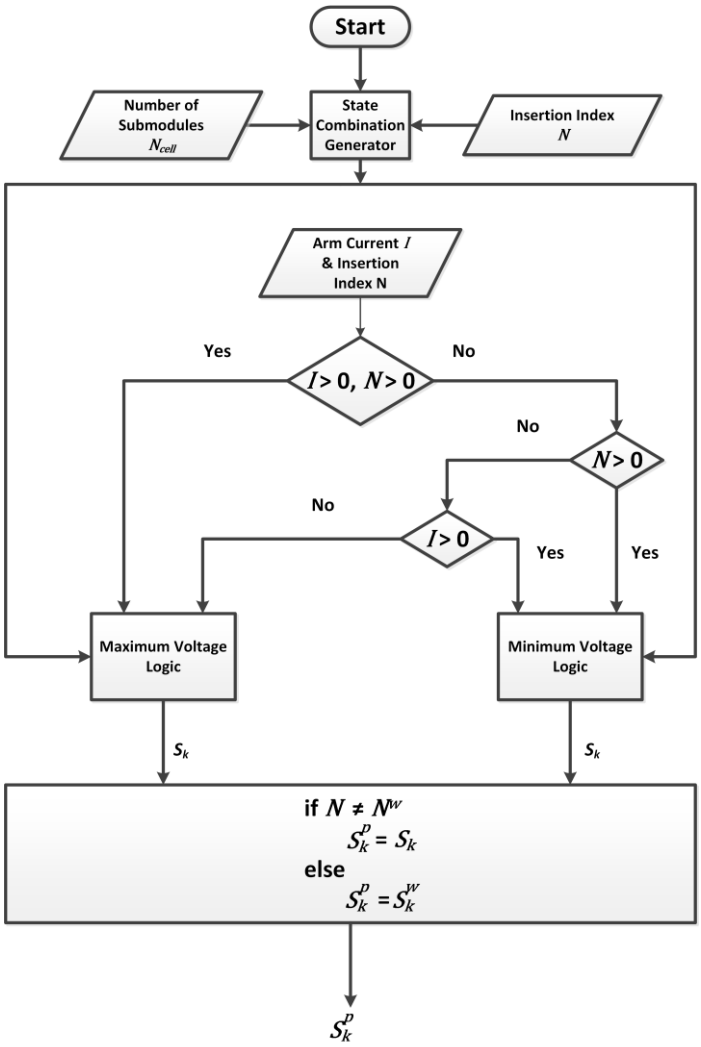


Figure 20: Proposed capacitor voltage balancing algorithm for cascaded converter

with multilevel cells

As stated earlier, each submodule can produce voltage waveform with nine discrete levels and we call these voltage levels as states. These states can be combined in several ways with the states of other submodules in order to synthesize a certain level in the output voltage waveform of the converter. The first step of the algorithm is to generate a list of all possible state combinations for the insertion index N. For this purpose, the state combination generator inputs the number of submodules in the converter arm N_{cell}, and the absolute value of insertion index and generates all the possible state combinations. For example, for $N_{cell} = 2$ and $N = \pm 4$, the state combination generator will generate $\{(0,4); (4,0); (1,3); (3,1); (2,2)\}$. Based on the direction of arm current and the sign (positive or negative) of insertion index, the algorithm then selects the capacitors to be inserted of bypassed, and hence the corresponding state of the submodule, by executing the maximum/minimum voltage logic shown in Figure 21.

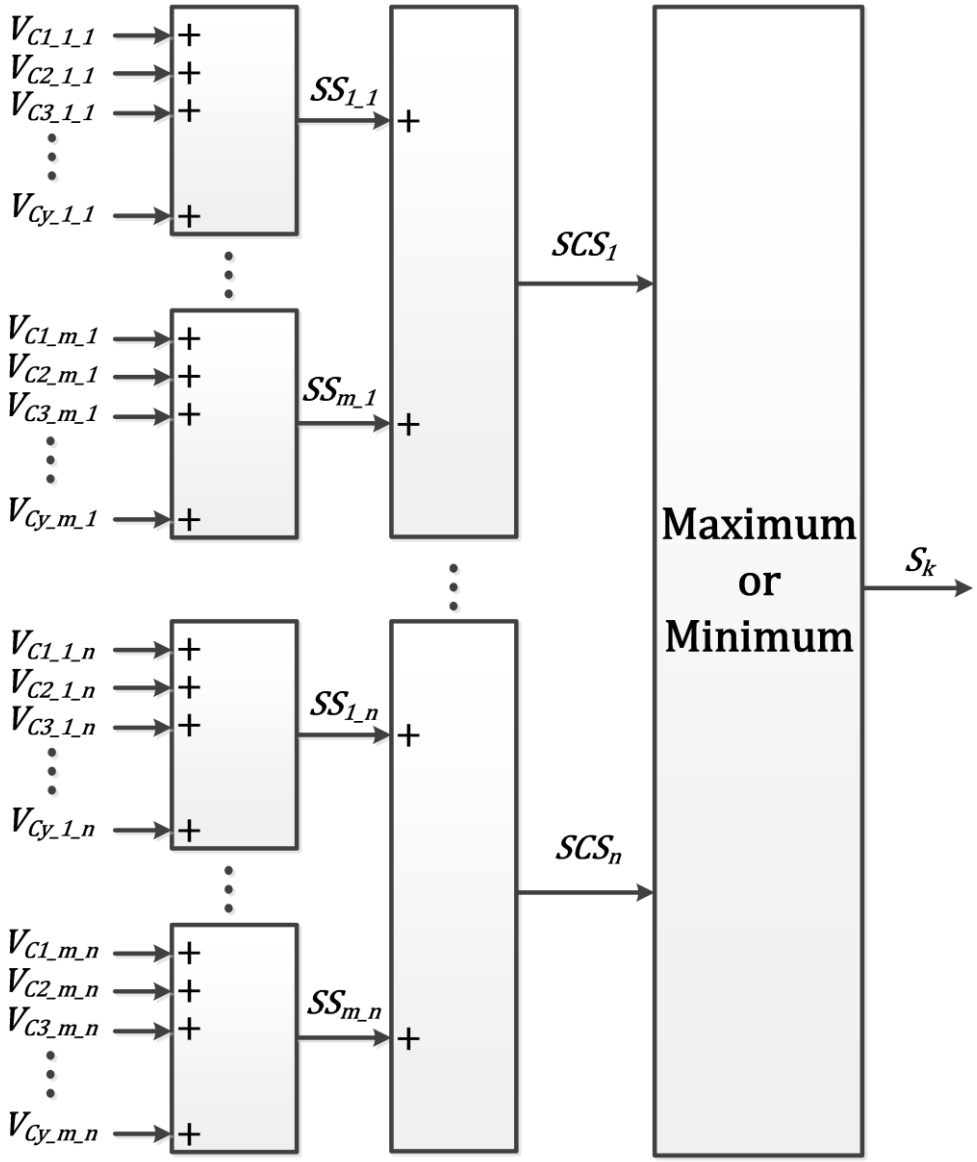


Figure 21: Maximum/Minimum voltage capacitors selection logic

The maximum voltage logic is selected when the arm current is such that it discharges the capacitors. Otherwise, the minimum voltage logic is selected. For each combination C_n generated by the state combination generator, the voltage of all the capacitors $V_{Cy\_m\_n}$ in the m^{th} submodule, involved in producing the respective state of the submodule as defined in the combination C_n, are added together to obtain the so-called "submodule sum" SS_{m_n} of the m^{th} submodule for the n^{th} combination C_n. This is done for each submodule in the converter arm. The "submodule sum" of all the submodules is then added together and resultant is the so-called "state combination sum" SCS_n for the n^{th} combination C_n. Depending on the selected maximum or minimum voltage logic, the combination that gives either the maximum or the minimum "state combination sum" is selected respectively. In this way the highly charged

capacitors or the less charged capacitors can be selected for discharging or charging respectively.

To minimize the device switching frequency, the present value of insertion index N is compared with the previous value of insertion index N^w. If the present and previous values of insertion index are equal, then the algorithm will keep the previous state S_k^w of each submodule. By using this approach, the device switching losses can be reduced. Finally, corresponding switching signals are generated for all the submodules.

3.2. Simulation Results

The circuit shown in Figure 19 was used to perform the simulations in Simulink. The capacitors used in the circuit were dimensioned to obtain a total arm energy of $20\ kJ/MVA$. Figure 22 shows the ripple in the capacitor voltages of first, second and third submodule. Figure 23 shows the ripple in the capacitor voltages of fourth, fifth and sixth submodule. It can be seen clearly from Figure 22 and Figure 23 that both the intra-cell and inter-cell capacitive energy balancing is ensured by using the proposed capacitor voltage balancing algorithm for cascaded converters with multilevel cells.

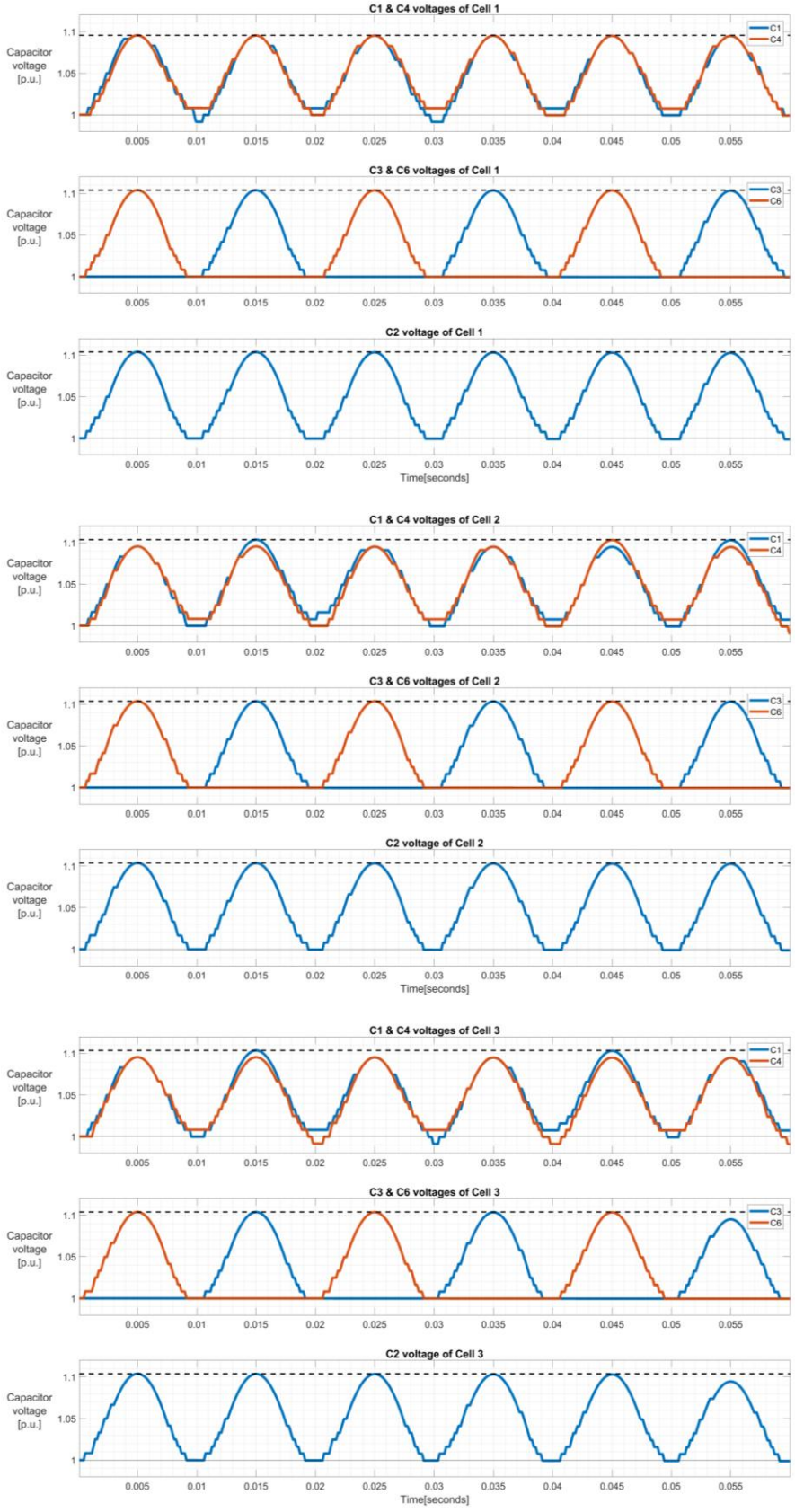


Figure 22: Capacitor voltage ripple of first, second and third submodule

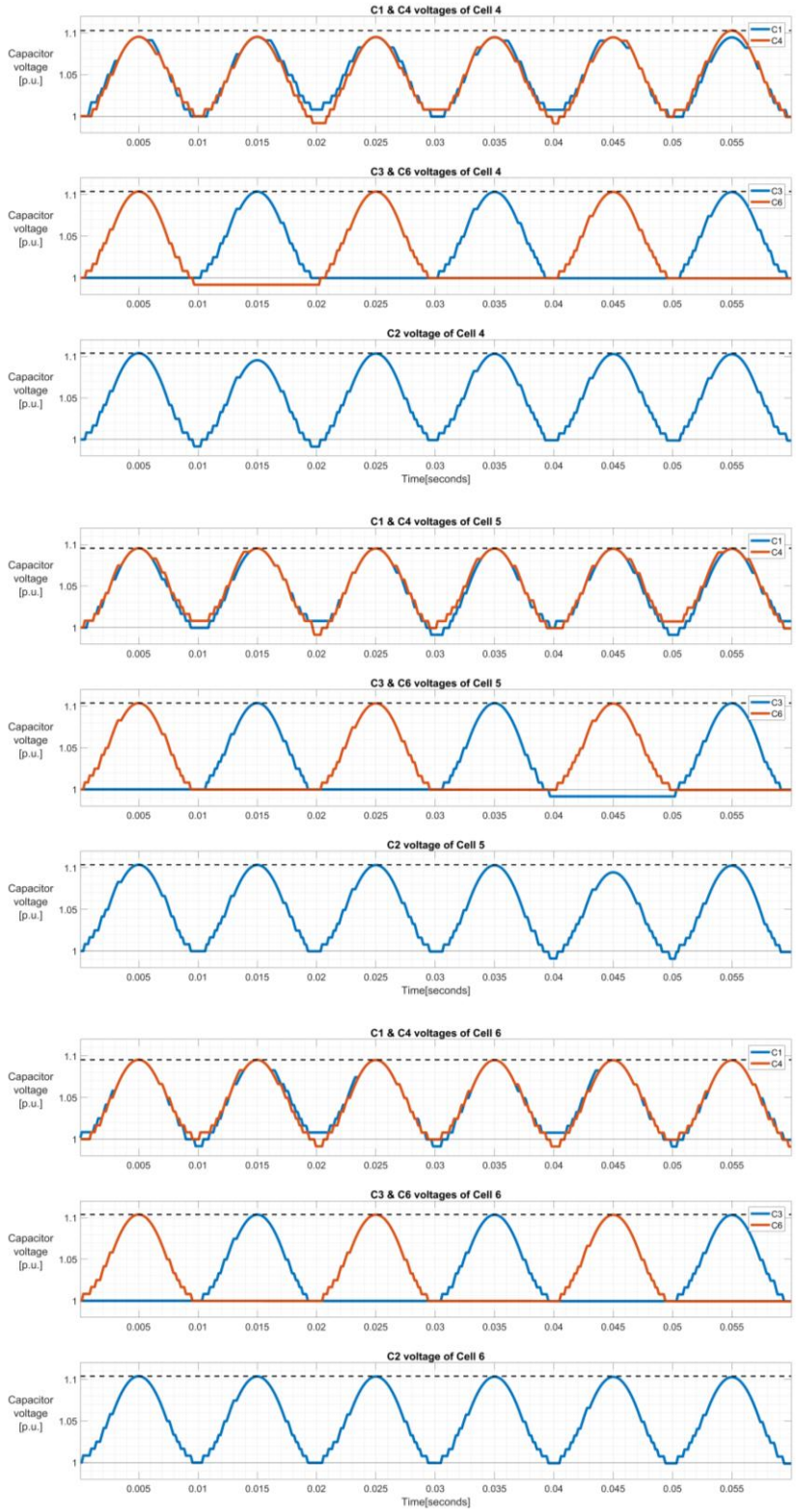


Figure 23: Capacitor voltage ripple of fourth, fifth and sixth submodule

3.3. Comparison with cascaded H-bridge converter

As discussed in section 3.1, cascaded converter shown in Figure 19 can produce output voltage waveform with forty-nine discrete levels. To perform a comparative study of this converter against a cascaded H-bridge converter discussed in section 2.3.1, twenty-four H-bridge submodules should be connected in series per arm of the converter as shown in Figure 24, to obtain the same number of levels in the output voltage of the two converters.

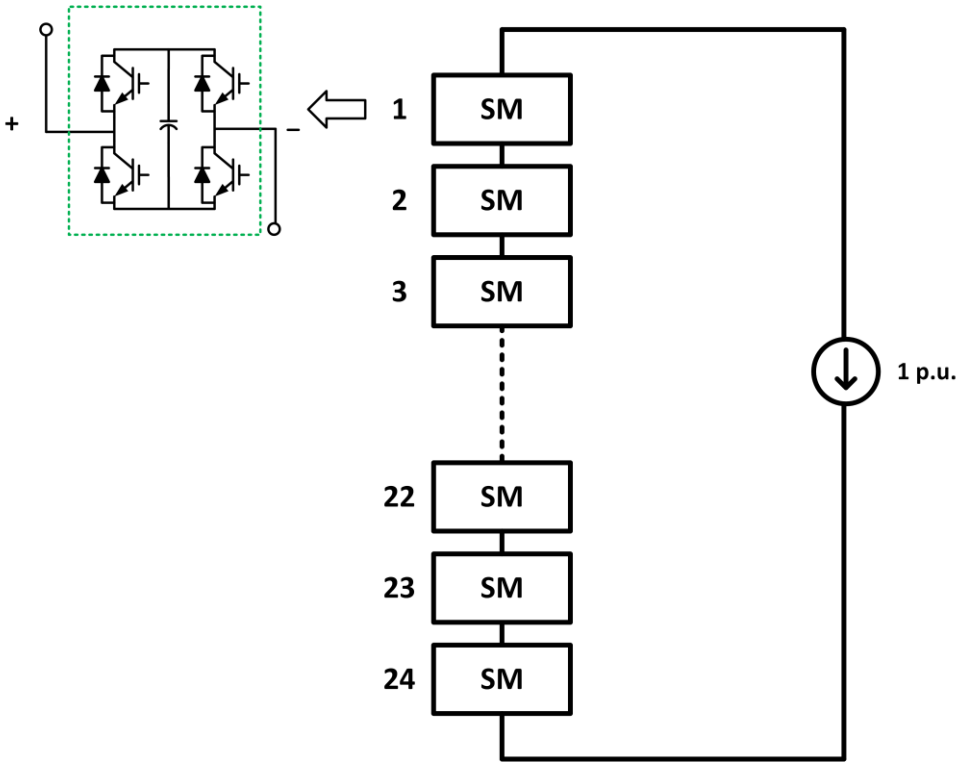


Figure 24: Cascaded converter with H-bridge submodules

The comparison between the two converters is performed by taking the following conditions into account:

- Same number of levels in the output voltage waveforms of both the converters
- Equal arm energy in both the converters
- Equivalent total rating of the switching devices in both the converters
- Same modulation technique used for both the converters
- Comparable switching actions in both the converters
- Equal amplitudes of the fundamental component of the output voltage in both the converters

Figure 25 shows the Fourier analysis of the output voltage waveform of the cascaded converter with multilevel submodules. Figure 26 shows the Fourier analysis of the output voltage of the cascaded H-bridge converter.

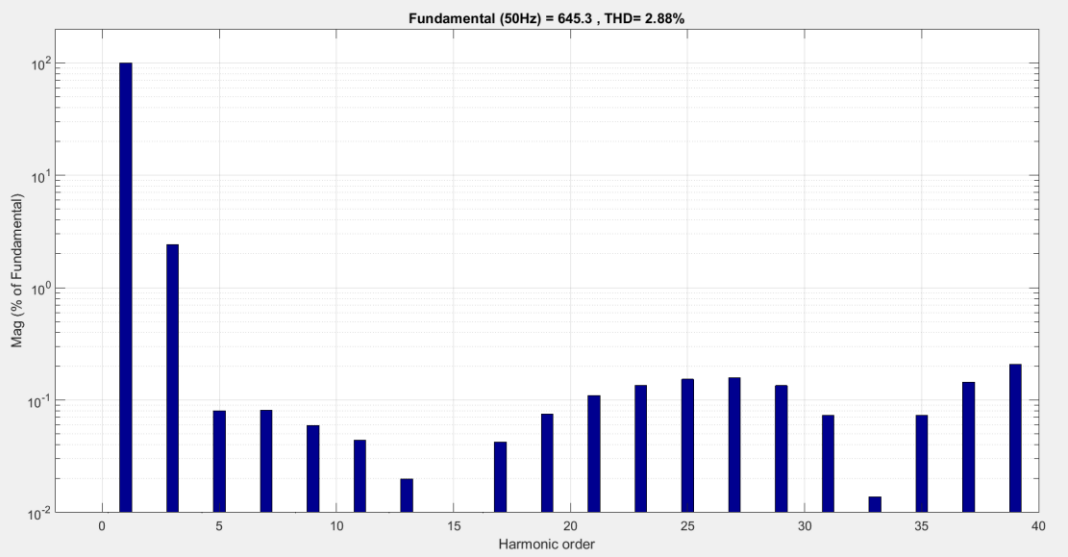


Figure 25: Fourier analysis of the output voltage waveform of the cascaded converter with multilevel submodules

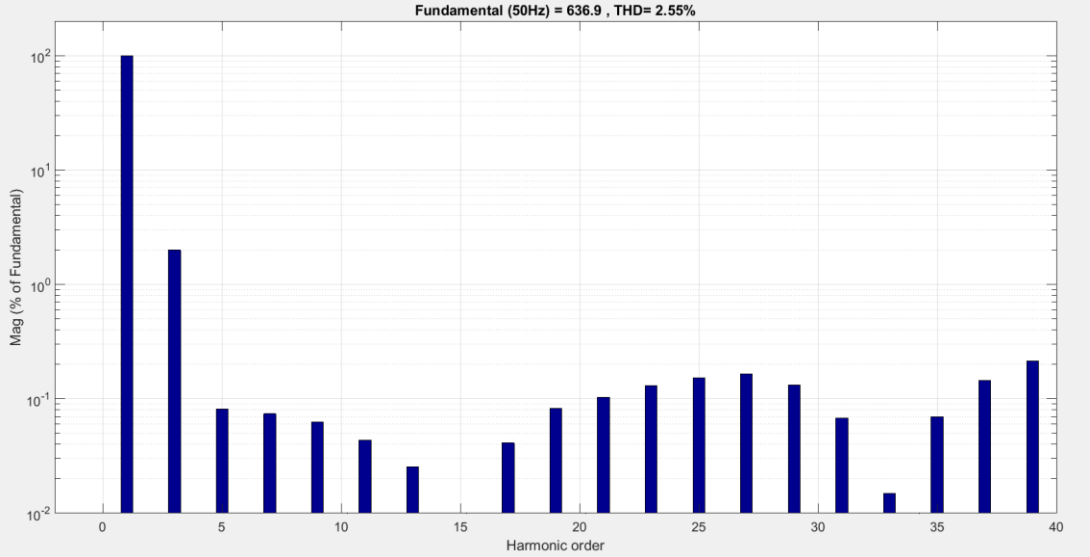


Figure 26: Fourier analysis of the output voltage waveform of the cascaded H-bridge converter

It can be seen from Figure 25 and Figure 26 that both the converters behave in a similar manner in terms of harmonic content in the output voltage. When the number of switching pulses over a fundamental cycle for each switch in the respective converters are added together, a count of $1133\,pulses/cycle$ is obtained for cascaded converter with multilevel submodules, and $1130\,pulses/cycle$ is obtained for cascaded H-bridge converter. This provides an indication of equal switching losses in both the converters.

3.4. Conclusion

Modulation technique and capacitive energy balancing algorithm for a cascaded converter with multilevel submodules was proposed in this chapter. The balancing mechanism was verified through the simulation results during steady-state operation of the single-phase converter. A comparative study of the cascaded converter with multilevel submodules was performed against the cascaded H-bridge converter. It was found out that both the converters behave in a similar manner in terms of harmonic content in the output voltage and have comparable switching losses.

4. Chain-link multilevel converter in STATCOM application

Chain-link multilevel converters offer an outstanding advantage over other multilevel topologies due to their modularity in design, and high power and voltage capability using low rated components. Hence, they are of great choice to implement the STATCOMs for transmission and distribution applications. In this chapter, we will discuss the operation of a delta STATCOM during steady state, and during symmetrical & unsymmetrical faults in the three-phase system. The STATCOM is connected to a $33\ kV$, $50\ Hz$, sine-base grid model, through a purely inductive filter. This filter is used to filter the harmonics in the injected current. For the delta configuration STATCOM, the filter is typically connected inside the delta as shown in Figure 27. In this way the filter can handle the voltage difference between the converter phases and limit the circulating current inside the delta. The nominal value of grid current is $2.12\ kA$.

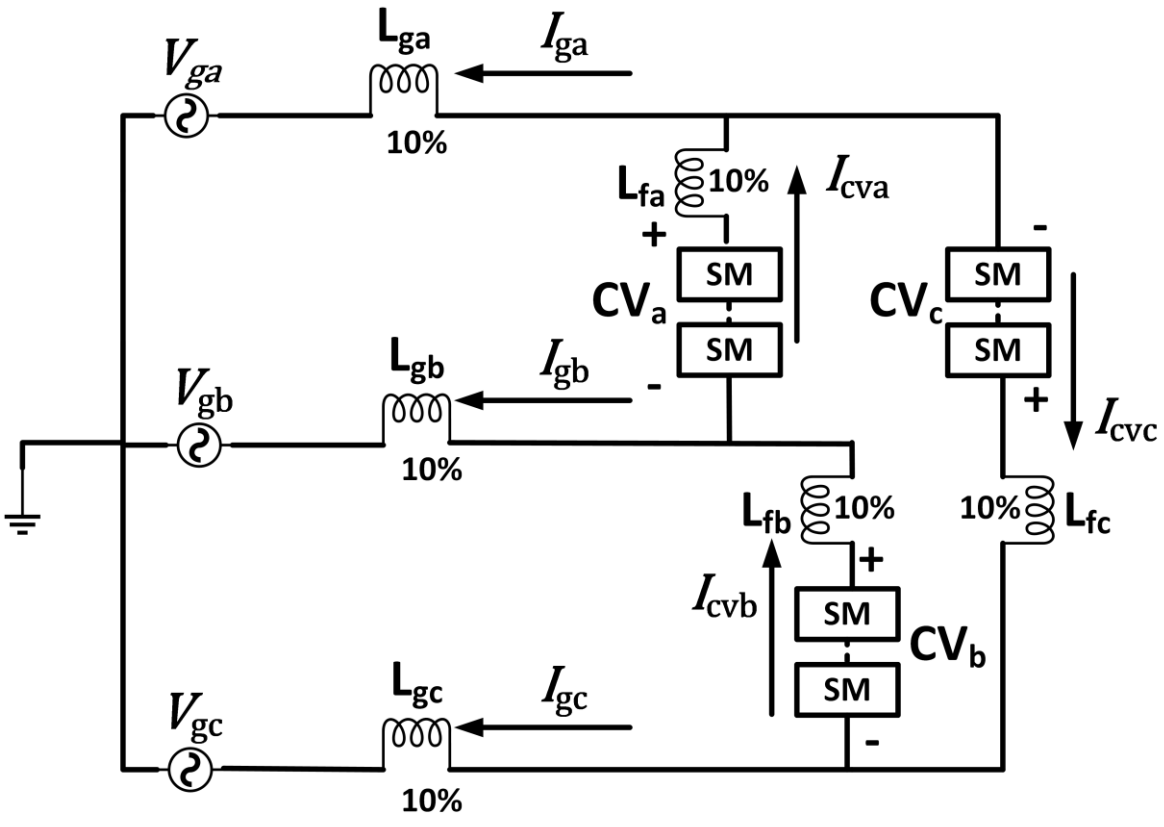


Figure 27: Delta STATCOM

The STATCOM is built using cascaded converter discussed in chapter 3. It consists of six multilevel submodules per phase/arm of the converter. The capacitors in the converter are dimensioned in order to obtain arm energy of $20\ kJ/MVA$. It is assumed that all the capacitors in the converter are initially charged to a voltage of $2.25\ kV$.

In this chapter, the overall control of the STATCOM is based on PI controllers implemented in the rotating dq-reference frame. Transformations of three-phase variables into synchronous reference frame are based on the amplitude-invariant Park transformation. It is assumed that a robust synchronization method exists to transform the AC quantities to DC. The modulation and balancing scheme discussed in section 3.1 is used for the modulation of the converter.

4.1. Control algorithm

The control method used for the STATCOM consist of an inner current control loop, which is used to control the converter output current, and outer control loops, used to determine the reference currents. Figure 28 show shows the block diagram of the implemented control system. It is assumed that the grid-voltage angle 'theta' (θ) is known accurately through the synchronization loop (not considered here for simplicity) like Phase-Locked-Loop (PLL). This angle is required for coordinate transformations. The cluster controller determines the reference value for the quadrature component of the current $i_{g,q}^*$, based on the selected initial voltage of the capacitors in the converter V_C^*. For delta configuration the line-to-line reference quantities are required. Hence, the output of the controller is transferred to three-phase using a transformation angle of $\theta + \frac{\pi}{6}$ and an amplification factor of $\sqrt{3}$.

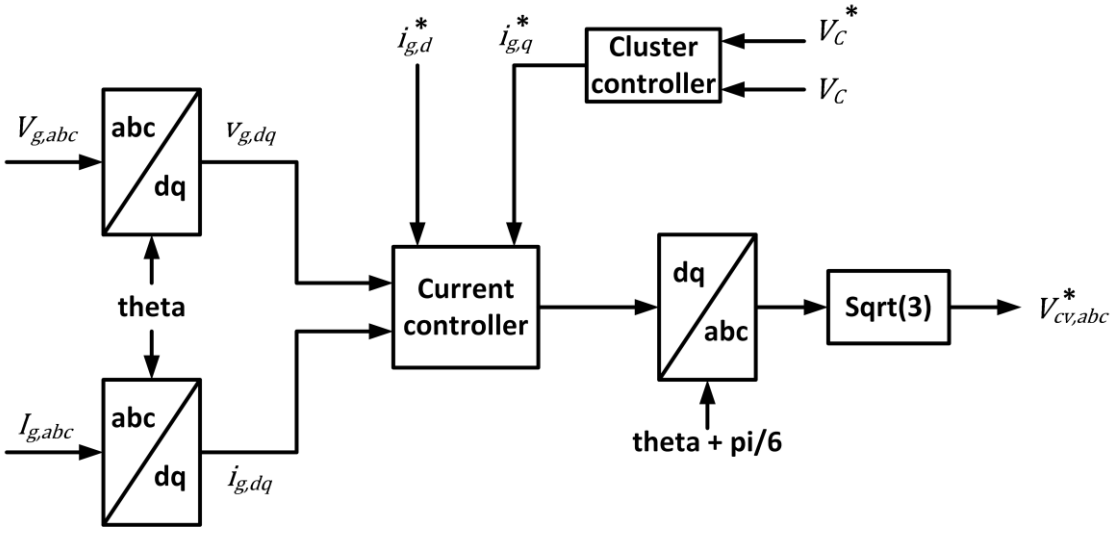


Figure 28: Overall control block diagram of STATCOM

4.1.1. Current controller

In order to design the current controller, firstly the dynamics of the system shown in Figure 27 are required. To do this let us first consider the single-phase equivalent of the system as shown in Figure 29.

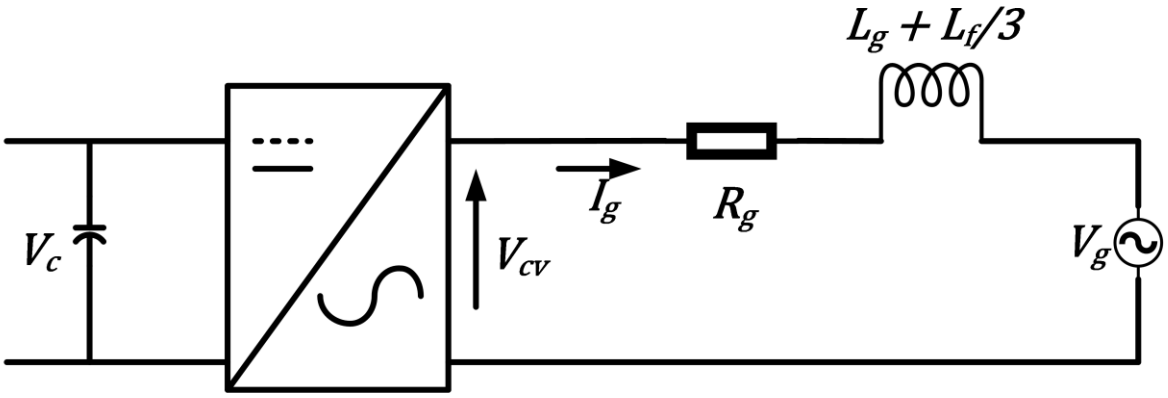


Figure 29: VSC and single-phase AC circuit representation

In the dq-reference frame the dynamics of the RL network shown in Figure 29 are given by

$$v_{cv} = L\frac{di_g}{dt} + (R + jw_gL)i_g + v_g \qquad (4.1)$$

where, v_{cv} is the VSC output voltage, i_g is the phase current, v_g is the grid phase voltage, w_g is the nominal angular frequency of the grid, $R = R_g$ is the phase resistance (equal to zero for the system under consideration), $L = L_g + \frac{L_f}{3}$ is the phase inductance.

The term jw_gL introduces a cross-coupling between the d and q components of the current. This can be seen from Equations 4.2 and 4.3, obtained by splitting real and imaginary terms in Equation 4.1.

$$L\frac{di_{g,d}}{dt} = v_{cv,d} - Ri_{g,d} + w_gLi_{g,q} - v_{g,d} \qquad (4.2)$$

$$L\frac{di_{g,q}}{dt} = v_{cv,q} - Ri_{g,q} - w_gLi_{g,d} - v_{g,q} \qquad (4.3)$$

The terms related to the grid voltage $v_{g,d}$, $v_{g,q}$ are added as a load-disturbance as shown in the block diagram of current controller in Figure 30.

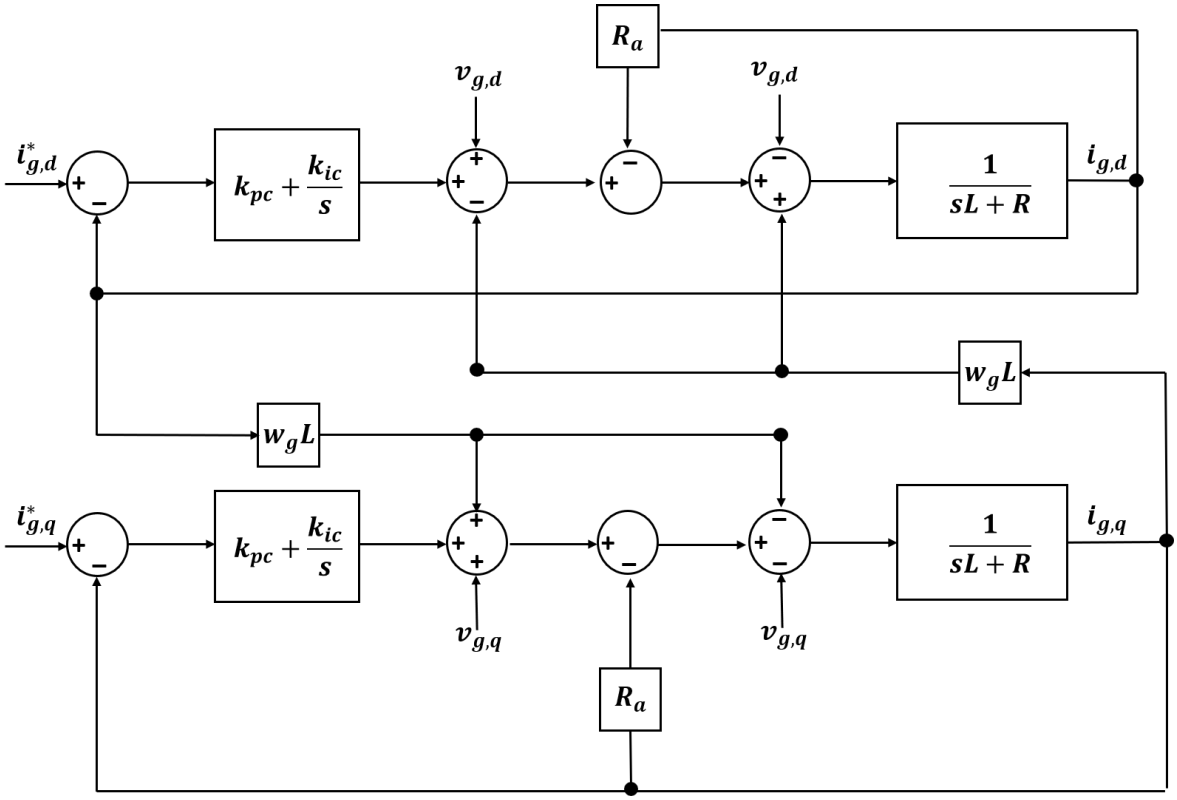


Figure 30: Current controller block diagram

The output of the current controller is voltage reference that is used to modulate the VSC. The current controller is designed in such a way that cross-coupling terms in Equations 4.2 and 4.3 are cancelled. This is performed by selecting the output of the current controller to be

$$v_{cv} = v'_{cv} + (jw_g L - R_a) i_g \qquad (4.4)$$

where, R_a is an active damping term that enhances the load-disturbance rejection.

By selecting the output of the current controller, and hence the voltage reference of the VSC as given in Equation 4.4, Equation 4.1 is modified as

$$v'_{cv} = L\frac{di_g}{dt} + (R + R_a) i_g + v_g \qquad (4.5)$$

Applying Laplace transform to Equation 4.5, the transfer function of the of the plant is given by

$$G'(s) = \frac{I_g(s)}{V'_{cv}(s)} = \frac{1}{sL+R+R_a} \qquad (4.6)$$

The closed current-control loop is shaped to have the same response as a first-order low-pass filter of bandwidth α_c. Hence, its transfer is given by

$$G_c(s) = \frac{\alpha_c}{s+\alpha_c} \tag{4.7}$$

Now if the a PI controller with transfer function F_c is assumed, then F_c is given by

$$F_c = \alpha_c L + \frac{\alpha_c(R+R_a)}{s} \tag{4.8}$$

Equation 4.8 represents a PI controller with active damping R_a, proportional gain k_{pc}, and integral gain k_{ic} defined as

$$R_a = \alpha_c L - R,\ k_{pc} = \alpha_c L,\ k_{ic} = \alpha_c(R + R_a) \tag{4.9}$$

The PI controller parameters can be calculated by using Equation 4.9 and setting the controller bandwidth α_c.

4.1.2. Cluster controller

The cluster controller determines the reference value for the quadrature component of the current $i_{g,q}^*$ as shown in Figure 31. This loop is used to compensate for the losses in the converter. It forces the average of all the capacitor voltages in the converter V_C, to follow its reference value V_C^* which is the initial voltage of the capacitors in the converter ($2.5\ kV$ in this case). The average capacitor voltage V_C is calculated by summing the instantaneous value of voltages of all the capacitors in the converter, divided by the total number of capacitors in the converter.

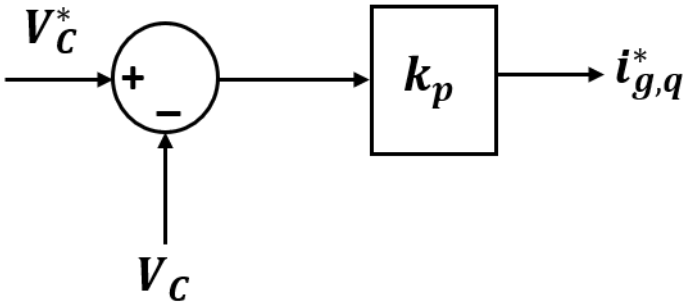


Figure 31: Cluster controller block diagram

4.1.3. Circulating-current controller

Figure 32 shows the block diagram of the circulating-current controller. This loop forces the circulating current I_z to follow its reference value I_z^* (zero in steady-state), producing the voltage command V_z^* which is then added to the output of the current controller $V_{cv,abc}^*$, to obtain the final value of reference voltages used to modulate the converter.

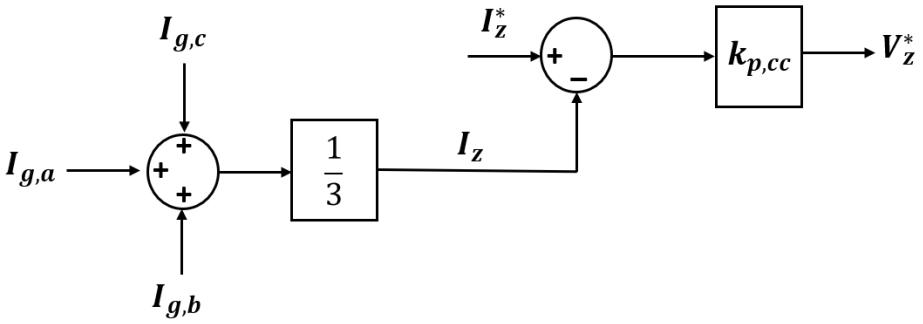


Figure 32: Circulating-current controller block diagram

4.2. Simulation results

The circuit shown in Figure 27 was used to perform simulations in Simulink. Table 3 summarizes the system and the control parameters used in the simulations.

4.2.1. Steady-state operation

Figure 33 shows the grid current in the rotating dq-reference frame as well as in the stationary-reference frame during steady-state operation. It can be seen clearly from Figure 33 that the reactive current follows the set reference value. Figure 34 shows the plot of arm voltages and currents. It can be seen clearly from Figure 34 that there is no circulating-current within the converter during its steady-state operation.

Table 3: System and Control Parameters

Parameters	**Values**
Cell capacitor initial voltage V_C^*	$2.25\ kV, 1\ p.u.$
Nominal value of line to line grid voltage V_g	$33\ kV$
Nominal value of grid current I_g	$\frac{3}{\sqrt{2}}\ kA, 1\ p.u.$
System frequency f_0	$50\ Hz$
Grid inductor L_g	$3\ mH$
Filter inductor L_f	$3\ mH$
Number of cells per arm N_{cell}	6
Closed loop current controller bandwidth α_c	$2000\ rad/s$
Cluster controller gain k_p	0.0027
Circulating-current controller gain $k_{p,cc}$	30

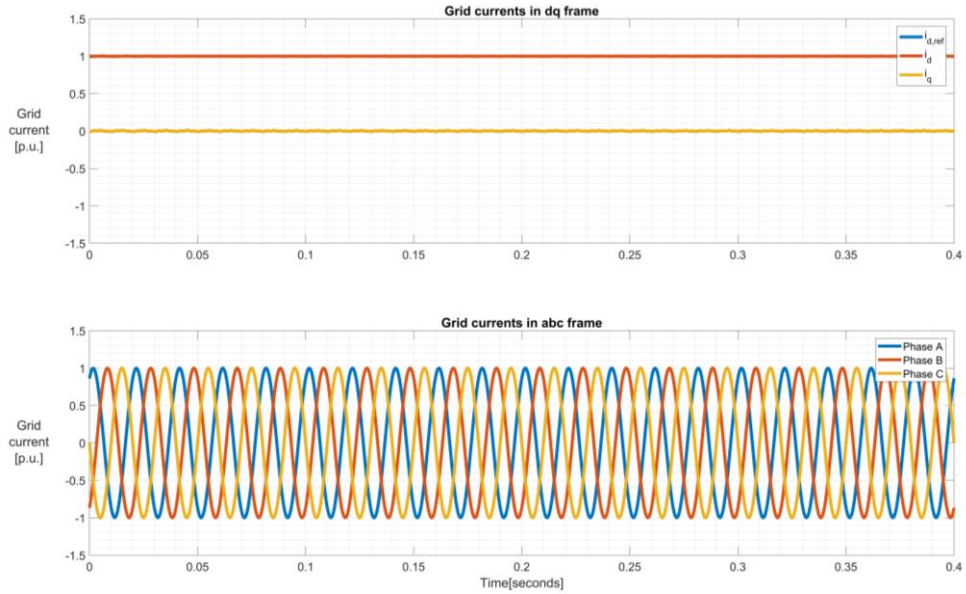


Figure 33: Grid current during steady-state operation

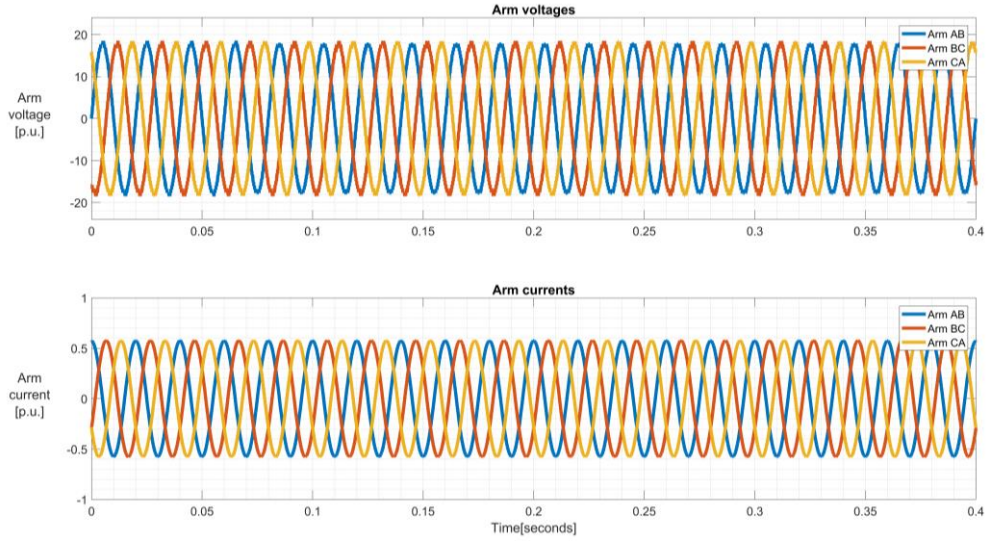


Figure 34: Arm currents and voltages during steady-state operation

Figure 35 shows the ripple in the capacitor voltages of first, second and third submodule of Phase A (Arm AB). Figure 36 shows the ripple in the capacitor voltages of fourth, fifth and sixth submodule of Phase A (Arm AB). Figure 37 shows the ripple in the capacitor voltages of first, second and third submodule of Phase B (Arm BC) and Phase C (Arm CA). Figure 38 shows the ripple in the capacitor voltages of fourth, fifth and sixth submodule of Phase B (Arm BC) and Phase C (Arm CA).

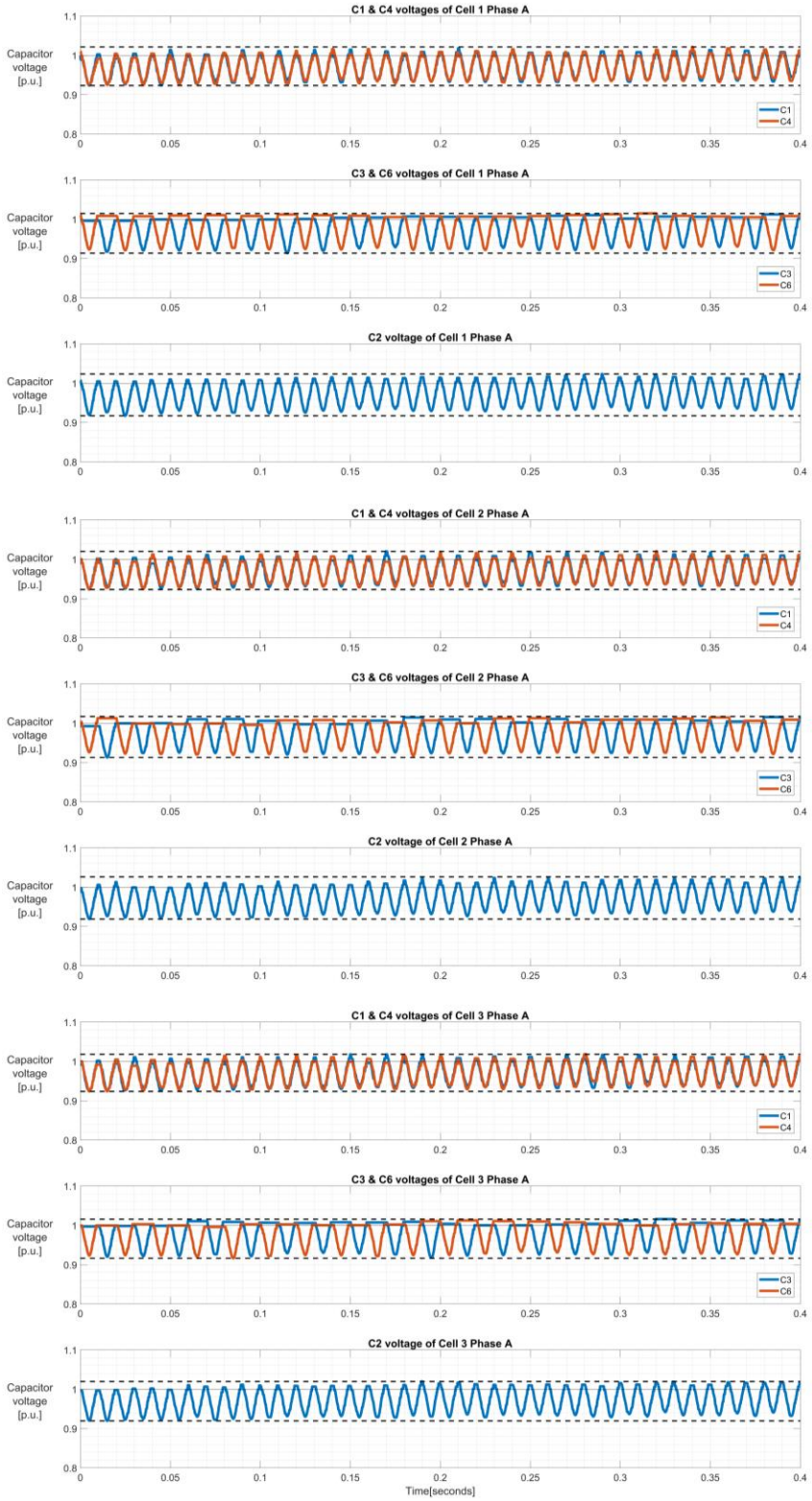


Figure 35: Capacitor voltage ripple of first, second and third submodule of Phase A

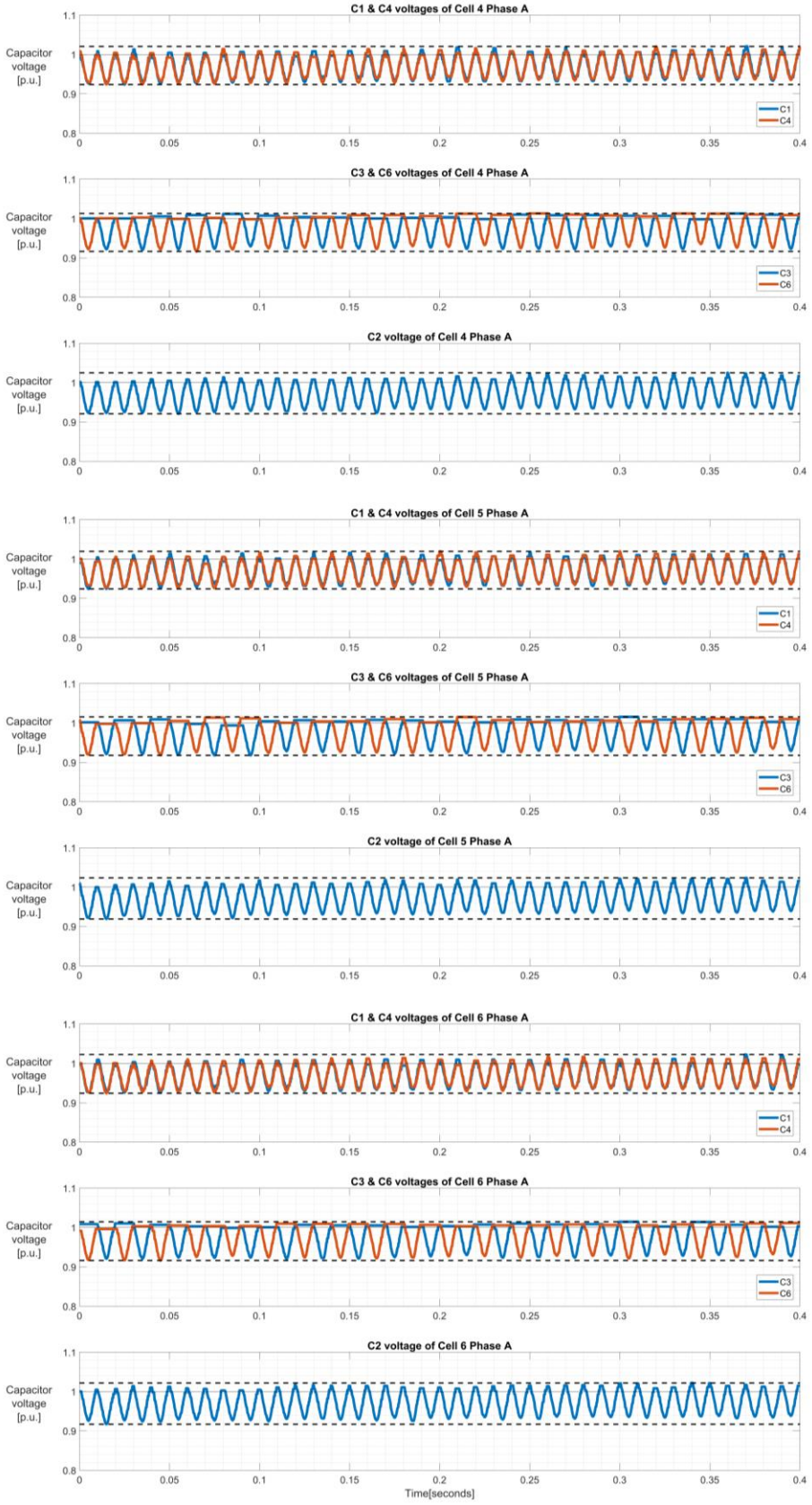


Figure 36: Capacitor voltage ripple of fourth, fifth and sixth submodule of Phase A

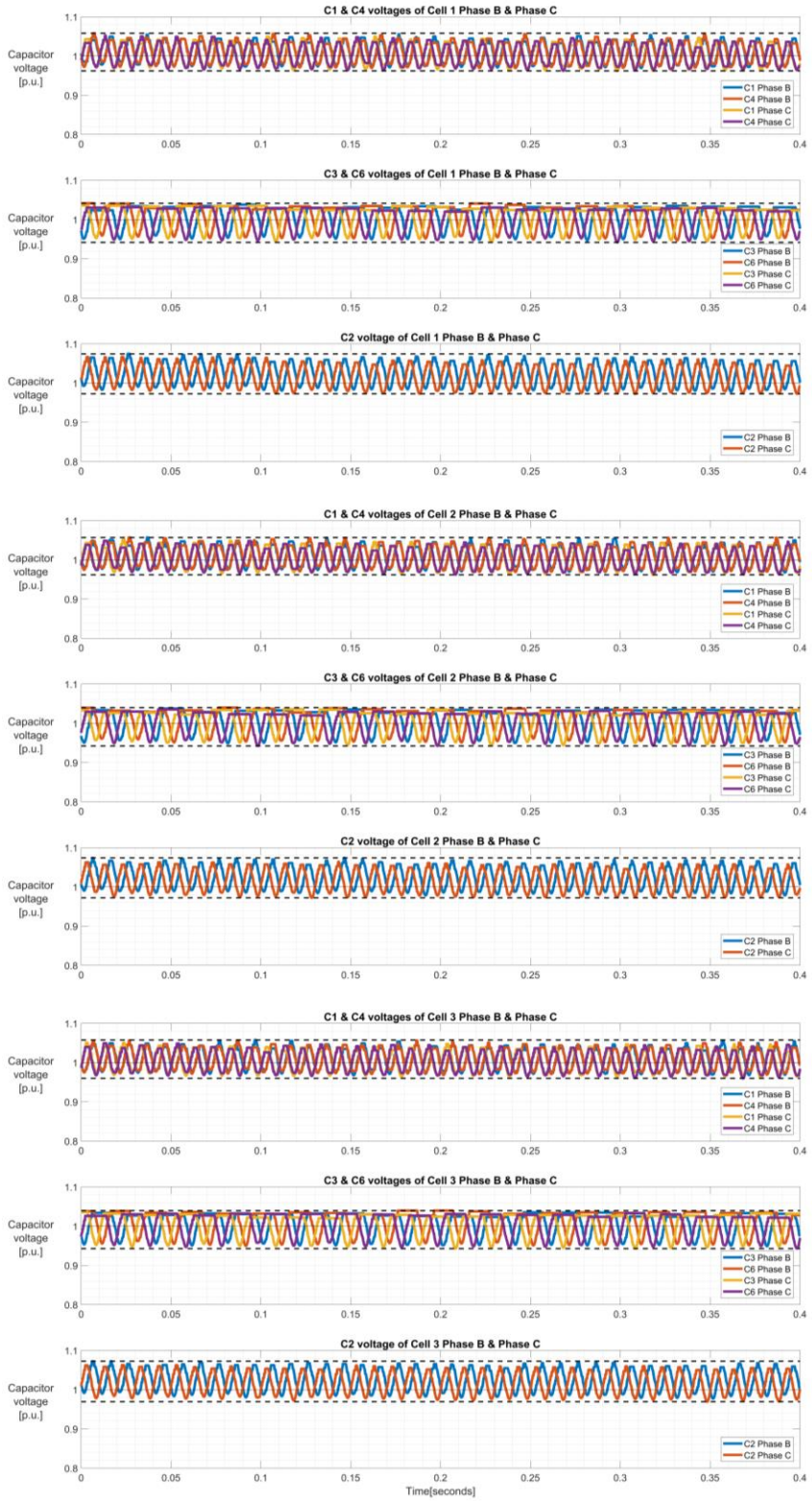


Figure 37: Capacitor voltage ripple of first, second and third submodule of Phase B&C

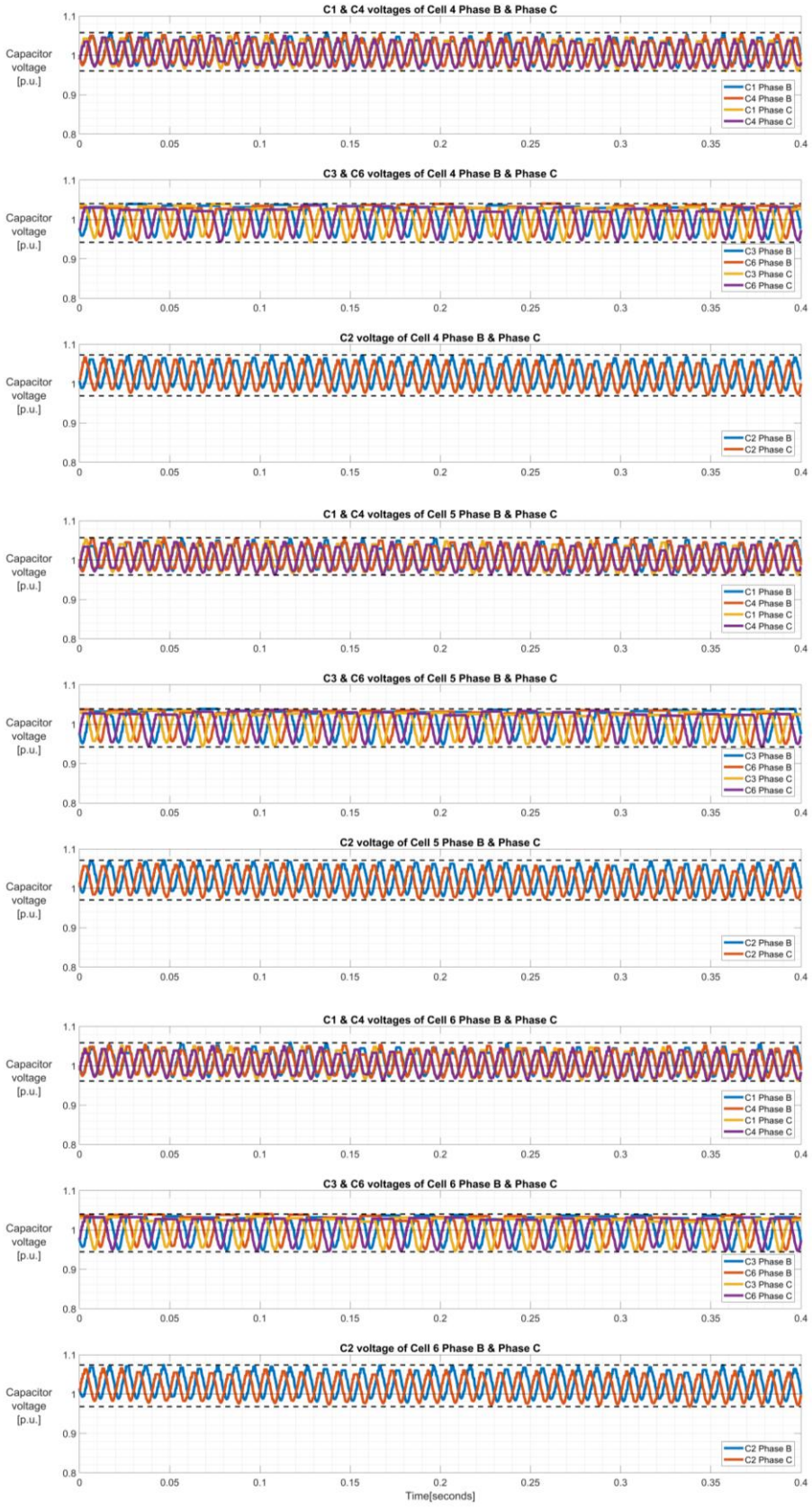


Figure 38: Capacitor voltage ripple of fourth, fifth and sixth submodule of Phase B&C

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It can be seen clearly from Figure 35, Figure 36, Figure 37, and Figure 38 that during steady state operation of STATCOM, both the intra-cell and inter-cell capacitive energy balancing is ensured in all the three phases by using the proposed capacitor voltage balancing algorithm proposed in section 3.1. The ripple in the voltage of each capacitor is below 10%.

4.2.2. Load-changing operation

Figure 39 shows the grid current in the rotating dq-reference frame as well as in the stationary-reference frame during load-changing operation. It can be seen clearly from Figure 39 that there is a change in nature of the connected load from inductive at $0.2\ s$ to capacitive at $0.22\ s$. Figure 40 shows the plot of arm voltages and currents.

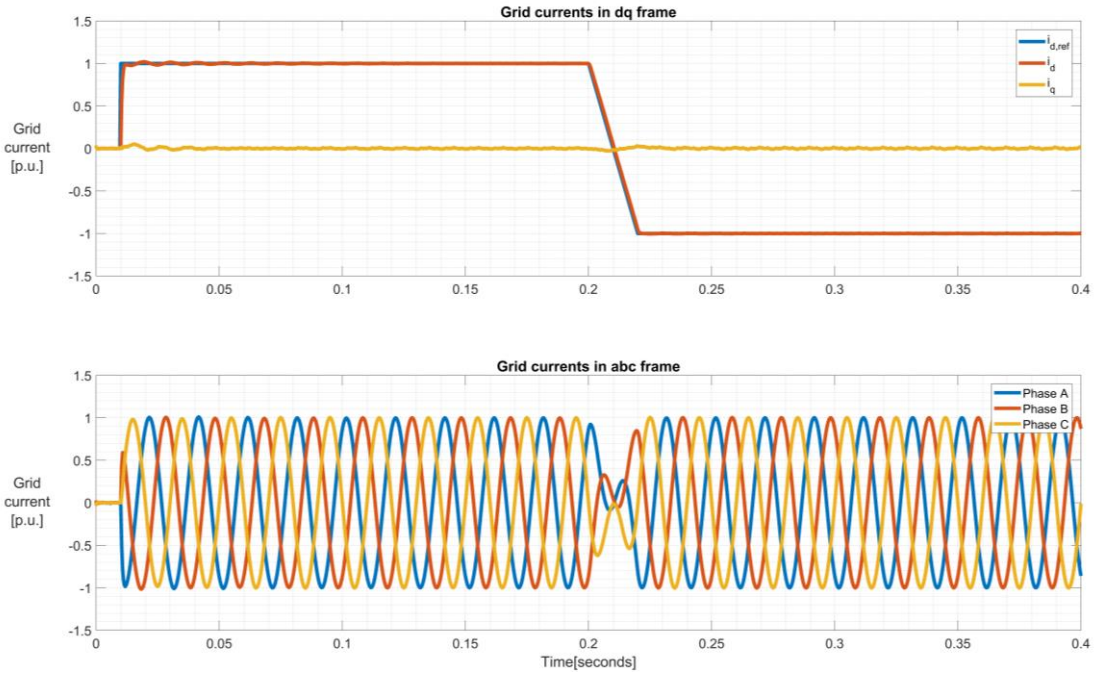

Figure 39: Grid current during load-changing operation

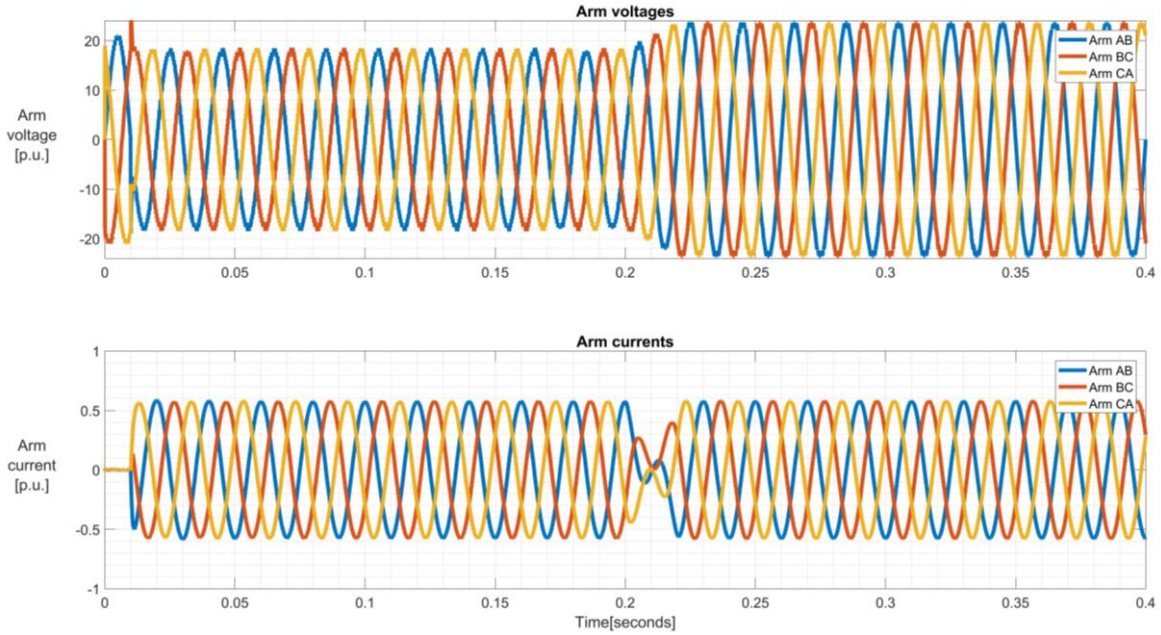

Figure 40: Arm currents and voltages during load-changing operation

Figure 41 shows the ripple in the capacitor voltages of first, third, and sixth submodule of Phase A (Arm AB). Figure 42 shows the ripple in the capacitor voltages of first, third and sixth submodule of Phase B (Arm BC) and Phase C (Arm CA).

It can be seen clearly from Figure 41 & Figure 42 that throughout the operation of STATCOM, both the intra-cell and inter-cell capacitive energy balancing is ensured in all the three phases. The maximum ripple in the voltage of any of the capacitors in the converter is below 16% throughout the operation of the STATCOM.

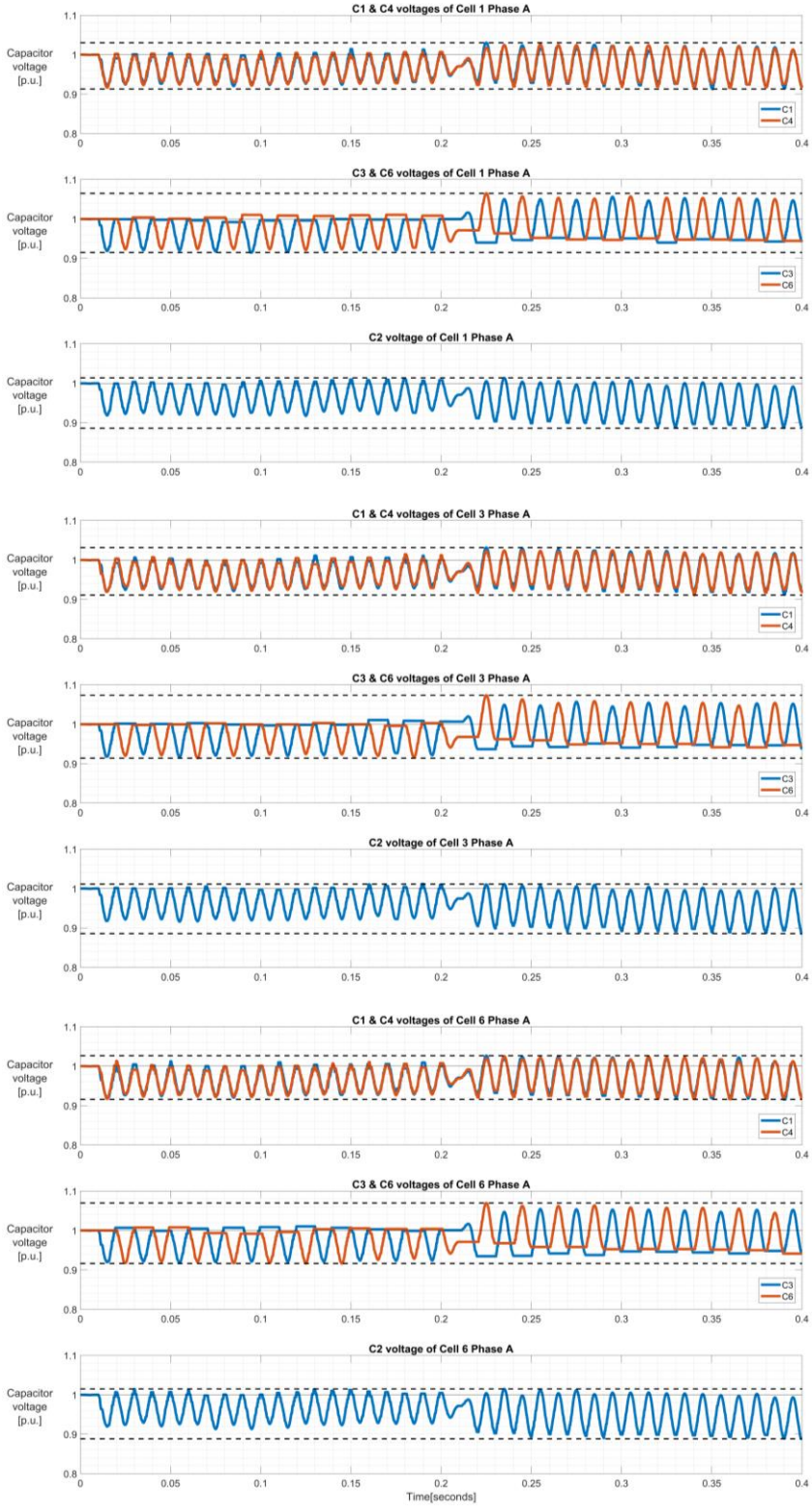

Figure 41: Capacitor voltage ripples in Phase A during load-change

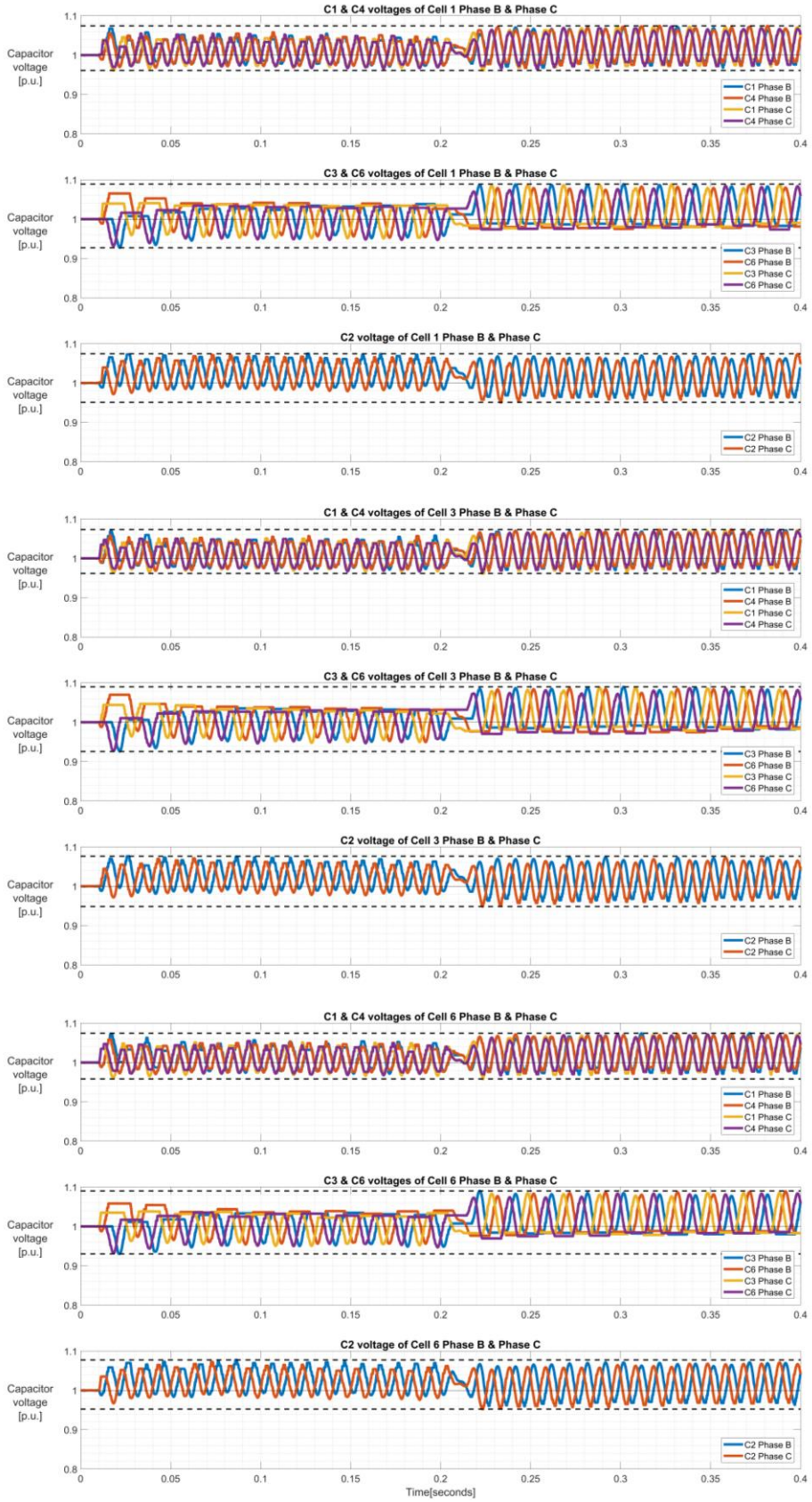

Figure 42: Capacitor voltage ripples in Phase B & C during load-change

4.2.3. Operation during faults

The operation of the system during both symmetrical (three-line-to-ground) and unsymmetrical faults (two-line-to-ground) is studied in this section. For simulating unsymmetrical fault, the amplitude of the grid voltage of Phase A and Phase B is reduced to 5% of the nominal value at $0.12\ s$ until $0.22\ s$. For simulating symmetrical fault, the amplitude of the grid voltage of all three phases is reduced to 5% of the nominal value at $0.32\ s$ until $0.42\ s$. Figure 43 shows the grid current in the rotating dq-reference frame as well as in the stationary-reference frame during the operation of the STATCOM in faulty grid condition. Figure 44 shows the plot of arm voltages and currents.

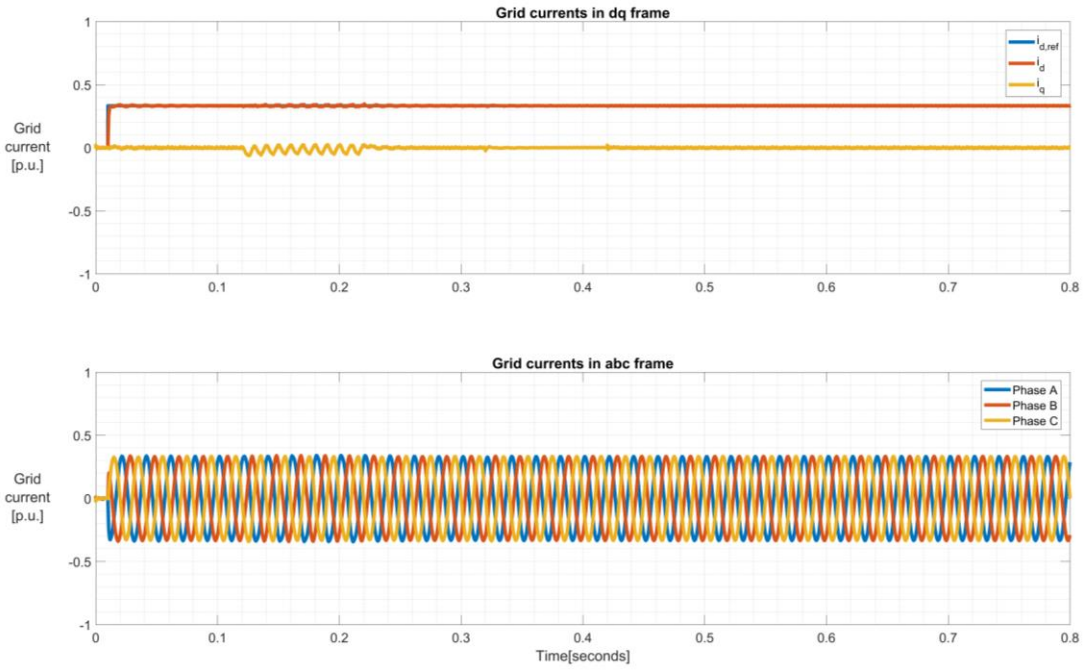

Figure 43: Grid current during faults

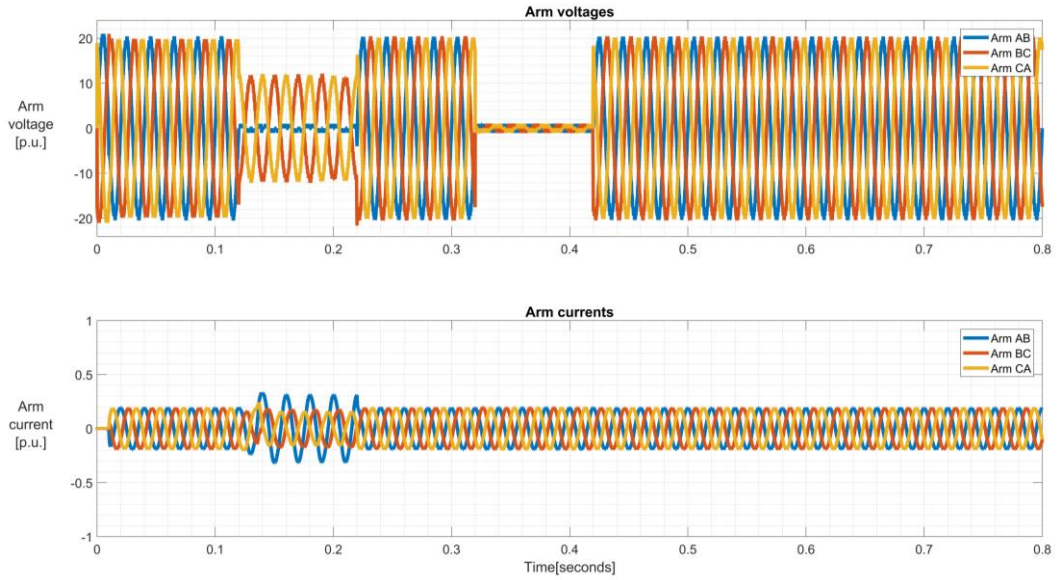

Figure 44: Arm currents and voltages during faults

It can be seen from Figure 44 that during unsymmetrical fault, a controlled zero-sequence current circulates inside the delta STATCOM. This circulating-current allows a power exchange between the phases without affecting the grid and is used to achieve capacitor balancing.

Figure 45 shows the ripple in the capacitor voltages of first, third, and sixth submodule of Phase A (Arm AB) during the operation of the STATCOM in faulty grid condition. Figure 46 shows the ripple in the capacitor voltages of first submodule of Phase B (Arm BC) and Phase C (Arm CA). It can be seen from Figure 45 and Figure 46 that capacitor balancing is ensured in all the three phases using the proposed modulation and control algorithm.

4.3 Conclusion

The operation of a delta STATCOM during steady state, and during symmetrical & unsymmetrical faults in the three-phase system was studied in this chapter. It can be concluded that the modulation and capacitive energy balancing algorithm for the cascaded converter with multilevel cells proposed in section 3.1, works well during steady-state as well as faulty grid conditions.

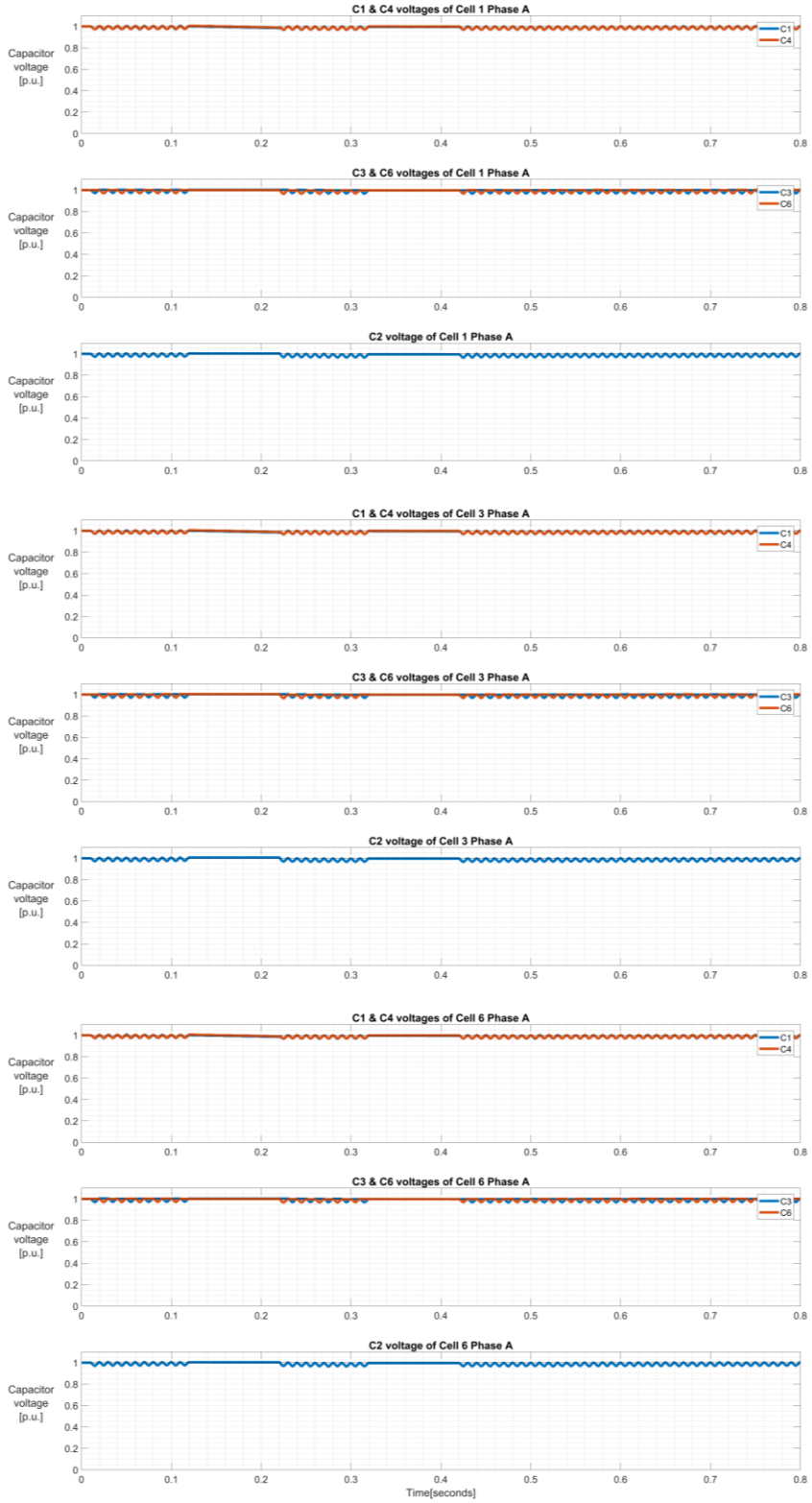

Figure 45: Capacitor voltage ripples in Phase A during faults

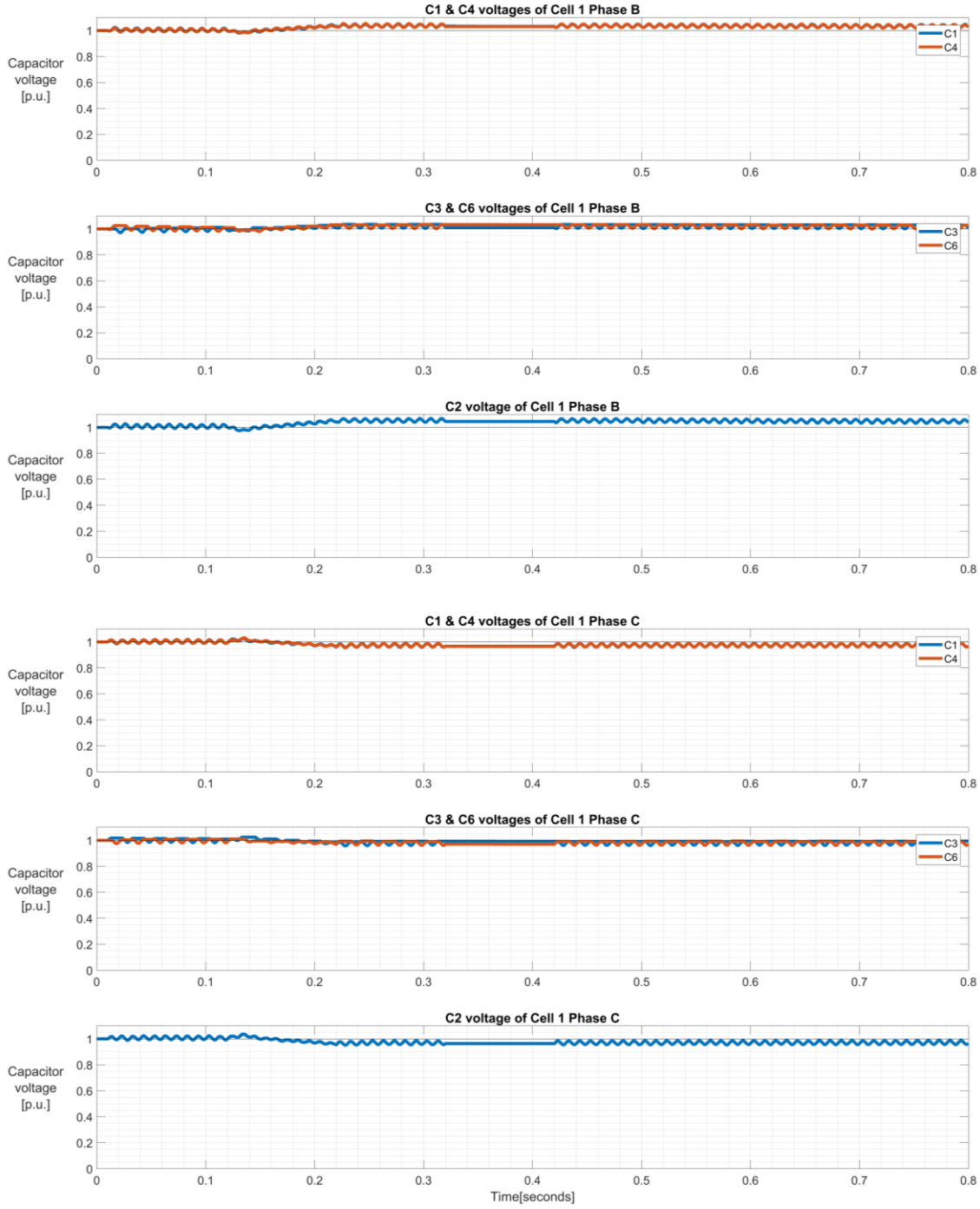

Figure 46: Capacitor voltage ripples in Phase B & C during faults

5. Conclusions

This thesis deals with modulation and capacitive energy balancing of multilevel submodules for cascaded converter in STATCOM application. Chapter 2 gives an overview of various multilevel converter topologies. Further it discusses a modulation and capacitive energy balancing technique for cascaded converter with H-bridge submodules. A new multilevel converter topology was introduced in section 2.3.2. This type of converter allows a scalable and modular layout with submodules connected in a two-input two-output manner. In chapter 3, modulation and energy balancing algorithm for cascaded converter with multilevel submodules was proposed and verified using simulations. The proposed energy balancing algorithm can be used in cascaded converter with any kind of submodule. Also, a comparative study of cascaded converter with multilevel submodules was performed against a cascaded converter with full-bridge submodules. It was found out that both the converters behave in a similar manner in terms of harmonic content in the output voltage and have comparable switching losses. In chapter 4, the proposed energy balancing algorithm was embedded in a simulation model of a three-phase STATCOM constructed with the proposed multilevel cells. This model was used for evaluating the performance of the proposed multilevel cell and capacitive energy balancing method under steady-state and fault conditions, which would typically occur in a utility application. The simulation results verified that the modulation and capacitive energy balancing algorithm for the cascaded converter with multilevel cells proposed in section 3.1, works well during steady-state as well as faulty grid conditions.

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