IMPROVED SEQUENCE NETWORK FOR A GRID-TIED CURRENT CONTROLLED INVERTER

by

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The development of equipment for harvesting renewable energy has lead to an increase in the number of inverters connected to electric grid architectures. The power electronic inverter is a key element to interface most renewables with the grid. Often manufacturers will not provide the detailed schematics of the inverter control scheme that has been implemented. But, current control mode is one of the most common control strategies for inverter design.

The control design of such inverters is realized by assuming nominal operating conditions for the grid voltage. However, it is common to model a current-controlled inverter as a three-phase current source even under non-nominal conditions. Therefore, the classical fault analysis tools, such as symmetrical components, needs to consider unbalanced condition impacts on control to make an accurate estimation of the fault current expected from the power electronic unit. The contribution of this work is to study the behavior of a grid-tied current controlled inverter when the grid is experiencing a single line-to-ground fault and to analytically develop a sequence network model that takes into account the control strategy implemented and the nature

of the fault. A PLECS simulation of a current controlled inverter is realized to prove that the new sequence network model, that takes into account the impact of the fault on the inverter's control system behavior, is more representative of inverter behavior compared to a sequence network developed using classical assumptions.

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discussions. Finally, I would like to especially thank Hashim Al Hassan that largely contributes to the construction of this project and provided me with very good advices on the direction of the project.

1.0 INTRODUCTION

1.1 BACKGROUND

Historically, the electrical grid was built following a radial configuration where clients are supplied by large power sources. However, with the increasing penetration of renewables, more inverter-based generation were connected to the grid. The flow of power that was primarily unidirectional (from power source to clients) became bidirectional as it becomes possible to provide power to the grid at the distribution level. Those distributed generations decrease the efficiency of classical fault detection scheme as they can reduce and even shadow fault currents [1]. Therefore, detection algorithm based on phase shift measurement between line current and voltage was developed to improve the fault detection capability in an inverter-based generation distribution circuit [2]. However, this scheme was developed considering balanced faults. For unbalanced faults, symmetrical components are used for fault current predictions. Nevertheless, this fault assessment technic were developed for networks, where rotating machines were the dominant contributor to fault currents [1]. In fact, traditional generators behave differently compared to inverter-based generations under unbalanced conditions making the modeling if inverters into sequence networks challenging. In that context, this project aims at providing an accurate answer in the sequence network modeling of inverter.

1.2 CURRENT MODE CONTROL VERSUS VOLTAGE MODE CONTROL

Most of the control schemes of an inverter aim at regulating the amount of active and reactive power injected into the grid. Two main strategies exist to control these parameters [3]. The first one is known as the *voltage-mode control.* In this mode the amount of active power delivered to the grid is controlled by acting on the phase angle of the converter output voltage while the amount of reactive power injected is controlled by acting on the converter output voltage amplitude with respect to grid voltage. The main advantage of the voltage-mode control is the simplicity of operation as only two independent control loops are required on the condition that the voltage amplitude and phase are closed to those of the grid voltage. However, this strategy suffers from a lack protection against overcurrent happening when the power references are changing too fast or when a fault occurs.

The second strategy to regulate the real and reactive power is the *current-mode control.* In this mode the real and reactive power regulations relies on controlling the phase angle and amplitude of the line current with respect to the grid voltage. Even if the regulation of dq parameters implies dynamics that need to be decoupled the advantages of this mode over the voltage mode are numerous. In fact, they include robustness against variations in parameters of the voltage sourced converter and a higher precision added to an inner protection from overcurrents.

Consequently, the current mode control has been chosen in this project as it represents most of the existing voltage sourced converter control scheme for the regulation of the real and reactive power. Moreover, the voltage source converter control of this project doesn’t include a control loop of real and reactive power as it would bring more unexpected behaviors from the converter that are relevant to analyze but aren’t in the scope of this project.

1.3 PROJECT CONSTRAINTS

The work presented in this report aims at realizing the sequence network of a grid-tied current controlled inverter system without any interfacing three-phase transformer and experiencing a single line-to-ground fault on phase A presented in figure 1. The goal is to predict accurately the fault current going through the fault resistance R_F and to explain any unexpected behavior in the inverter's output current that would appear under unbalanced conditions.

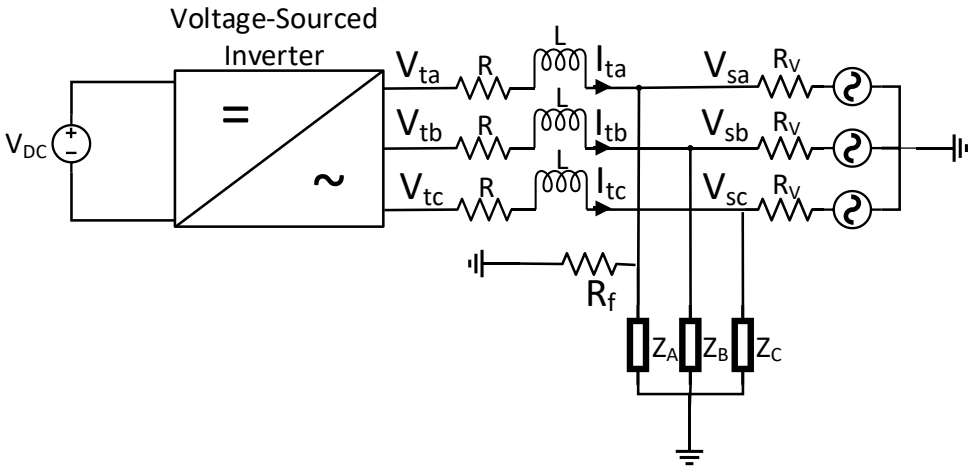


Figure 1: Schematic of a grid-tied current controlled inverter

1.4 CONTENT ROAD MAP

As the system to model has been defined, the analysis of the problem is decomposed in three chapters. The chapter 2 aims at providing a pre-analysis of the problem, modeling basic elements of the distribution circuit using the symmetrical components. This chapter provides the technical background concerning symmetrical components and study the classical assumptions concerning the sequence network model of inverters in literature. The chapter 3 provides a detailed analysis of the Grid-tied current-controlled inverter design. This chapter includes the validation of a simulation model of Grid-tied current controlled inverter that is used in the next chapter. The chapter 4 constitutes the core of this project presenting a new sequence model of the Grid-Tied controlled inverter. This accuracy of the new model is compared to the sequence network using classical assumptions presented in chapter 2. A PLECS simulation is realized to validate the proper sequence network model for the Grid-Tied current controlled inverter.

2.0 PRELIMINARY FAULT ANALYSIS

This chapter aims at providing the fundamentals of the existing tools to model fault events in the grid [4]. The use of symmetrical component theory is the basis to build sequence networks that are used to predict the fault current expected for a particular type of fault. The section 2 of this chapter will apply these principles to the voltage source and the series impedance of the system to start building the sequence network. However, as the sequence network of the inverter is the core of the problem in this project, the last section of this chapter presents the primary statements found in literature to model the sequence network of an inverter. The results of these classical assumptions will be compared in chapter 4 to a new sequence network model based on the study of the inverter's control in chapter 3.

2.1 SYMMETRICAL COMPONENTS

Thanks to the Fortescue transformation any set of three phasors can be expressed as a linear combination of sets of three-phasors as represented in figure 2.

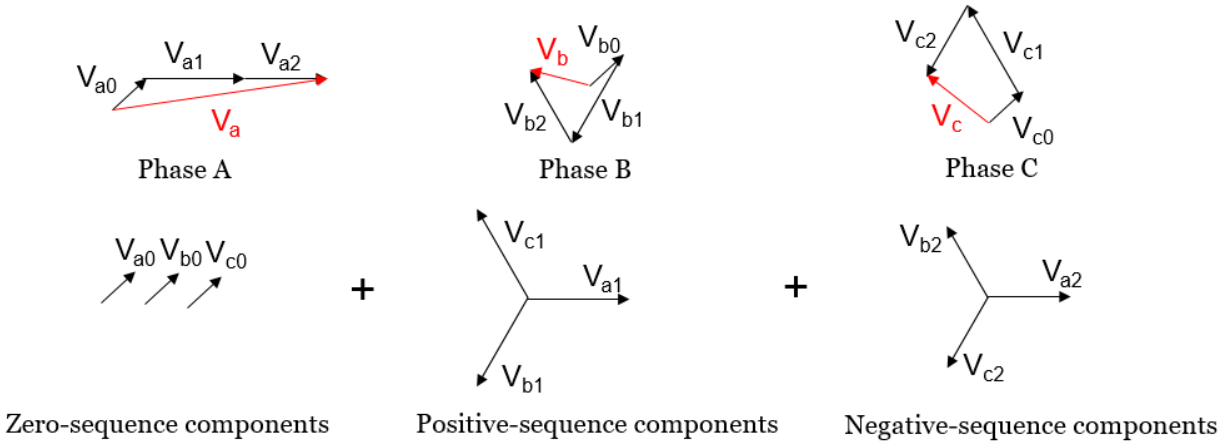


Figure 2: Decomposition of three phasors into sequence components

The first set is the Zero sequence components, composed of three phasors with the same magnitude and with no phase difference between them and represented by the subscript 0 (V_{a0}, V_{b0}, V_{c0}). The second set is the Positive sequence components, composed of three phasors with the same magnitude with 120° phase difference between them, in a positive sequence and represented by the subscript 1(V_{a1}, V_{b1}, V_{c1}). The last set is the Negative sequence components, composed of three phasors with the same magnitude, with 120° phase difference between them, in a negative sequence and represented by the subscript 2 (V_{a2}, V_{b2}, V_{c2}). As in a set of phasors (zero, positive or negative) the magnitudes of the phasors are identical and the phase difference between each phasor is known, each set of phasors (zero, positive, negative) can be expressed by a single complex number (V_0, V_1, V_2 respectively).

Relations between a set of phasors and its associate complex number are given in (2-1), (2-2) and (2-3), where $a = e^{j\frac{2\pi}{3}}$ and $a^2 = e^{j\frac{4\pi}{3}} = e^{-j\frac{2\pi}{3}}$.

$$V_0 = V_{a0} = V_{b0} = V_{c0} \tag{2-1}$$

$$\begin{cases} V_{a1} = V_1 \\ V_{b1} = a^2 V_1 \\ V_{c1} = a V_1 \end{cases} \tag{2-2}$$

$$\begin{cases} V_{a2} = V_2 \\ V_{b2} = a V_2 \\ V_{c2} = a^2 V_2 \end{cases} \tag{2-3}$$

With the previous simplifications, the Fortescue transformation in (2-4) can be expressed as well as its inverse in (2-5) to obtain the sequence components of a set of three phasors.

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} V_0 \\ V_1 \\ V_2 \end{bmatrix} \tag{2-4}$$

$$\begin{bmatrix} V_0 \\ V_1 \\ V_2 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{2-5}$$

2.2 PRELIMINARY SEQUENCE NETWORK OF THE SYSTEM

2.2.1 Sequence network of the three-phase voltage source and its output impedance

The goal of this part is to build the sequence networks of a three-phase voltage sources and its output impedance represented in figure 3.

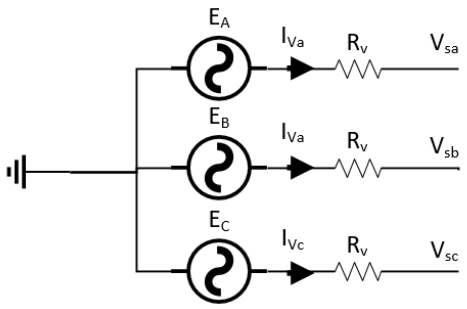


Figure 3: Schematic of the three-phase voltage source and its output impedance

Using the notations of figure 3, each phase follows the relation given in (2-6):

$$\begin{cases} V_{sa} = E_a - R_v I_{va} \\ V_{sb} = E_b - R_v I_{vb} \\ V_{sc} = E_c - R_v I_{vc} \end{cases} \tag{2-6}$$

From the relations in (2-6) it is possible to apply the inverse Fortescue transformation to have a relation linking zero sequence phasors in (2-7), positive sequence phasors in (2-8), and negative sequence phasors in (2-9).

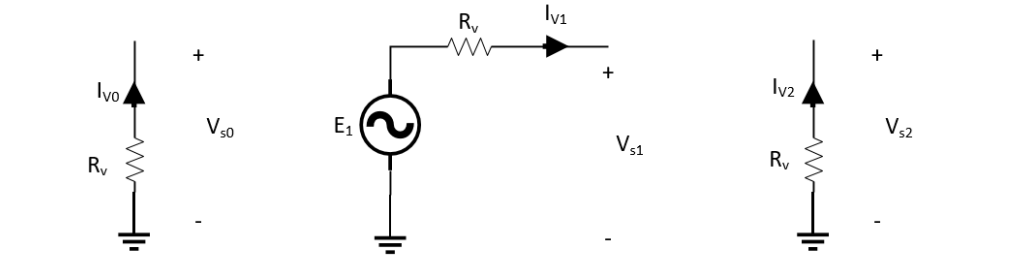
$$V_{s0} = \frac{V_{sa} + V_{sb} + V_{sc}}{3} = \frac{E_a + E_b + E_c}{3} - R_v \frac{(I_{va} + I_{vb} + I_{vc})}{3} \tag{2-7}$$

$$V_{s0} = E_0 - R_v I_{v0} = -R_v I_{v0}$$

$$V_{s1} = \frac{(V_{sa} + a^2 V_{sb} + aV_{sc})}{3} = \frac{E_a + a^2 E_b + aE_c}{3} - R_v \frac{(I_{va} + a^2 I_{vb} + aI_{vc})}{3}$$
$$V_{s1} = E_1 - R_v I_{v1} \tag{2-8}$$

$$V_{s2} = \frac{V_{sa} + aV_{sb} + a^2 V_{sc}}{3} = \frac{E_a + aE_b + a^2 E_c}{3} - R_v \frac{(I_a + aI_b + a^2 I_c)}{3}$$
$$V_{s2} = E_2 - R_v I_2 = -R_v I_2 \tag{2-9}$$

As the three-phase voltage provides a balanced set of voltages in a positive sequence only $E_1 \neq 0$. Thanks to the equations in (2-7), (2-8) and (2-9), it is possible to draw the equivalent zero sequence network (a)), positive sequence network (b)) and negative sequence network (c)) in figure 4.

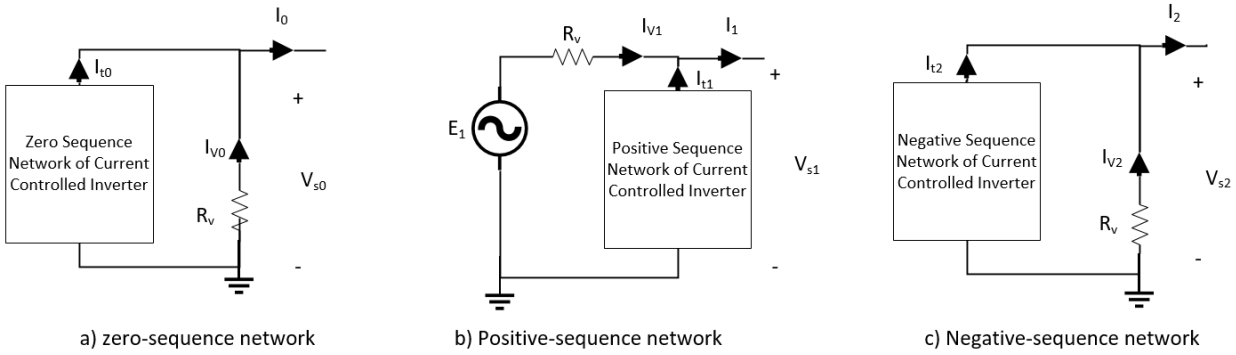


a) zero-sequence network b) Positive-sequence network c) Negative-sequence network

Figure 4: Sequence networks of the three-phase voltage source and its output impedance

2.2.2 Single line-to-ground fault on phase A modeling

As the sequence network of the current controlled inverter, in parallel with the three-phase voltage source and its output impedance, is subject to study, the sequence networks in figure 5 are modeled to consider the inverter as a black box that will be modeled later on.



a) zero-sequence network b) Positive-sequence network c) Negative-sequence network

Figure 5: Sequence network of the system with unknown contribution of the inverter

The fault condition modeled is a short-circuit between phase A and the ground with a fault impedance R_F. Considering that the pre-fault current (I_A, I_B, I_C before the fault occurs) is negligible then it is possible to state some fault conditions in (2-10)

$$\begin{cases} I_B = I_c = 0\ A \\ V_{sa} = R_F I_A \end{cases} \tag{2-10}$$

From the first relation of (2-10) and the transformations in (2-4) and (2-5) it is possible to express relations linking sequence components of load currents and grid voltage.

$$\begin{cases} I_0 = I_1 = I_2 = \dfrac{I_A}{3} \\ (V_{s0} + V_{s1} + V_{s2}) = 3R_F I_1 \end{cases} \tag{2-11}$$

From the relations in (2-11), it is possible to connect the zero, positive and negative sequence networks to get the sequence network model in figure 6.

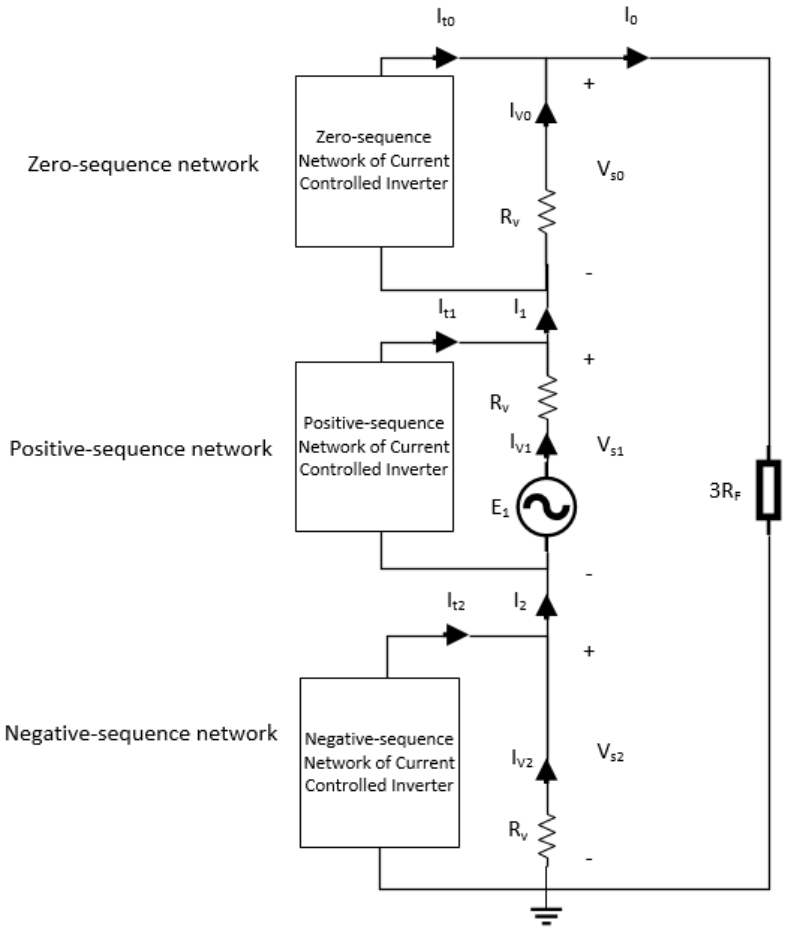


Figure 6: Sequence network modeling the single line-to-ground on phase A with unknown contribution of the inverter

To compute the fault current, the circuit figure has to be solved to express $I_0 = I_1 = I_2$, as the fault current expected is given by computing $I_A = 3I_1$.

2.2.3 Literature review on Inverter's fault contribution

This part will summarize two reference documents to establish the classical assumptions made to model the fault contribution of Inverters. The first document [5] is a technical report from the IEEE Power & Energy society analyzing the Fault Current Contributions from Wind Plants. The report realizes the assessment of each type of wind turbine generator (type I, type II, type III, type IV and type V) for the design of protecting equipment. The type IV wind turbine generators presented in figure 7 is composed of an electrical machine interconnected with a full-scale back-to-back frequency converter.

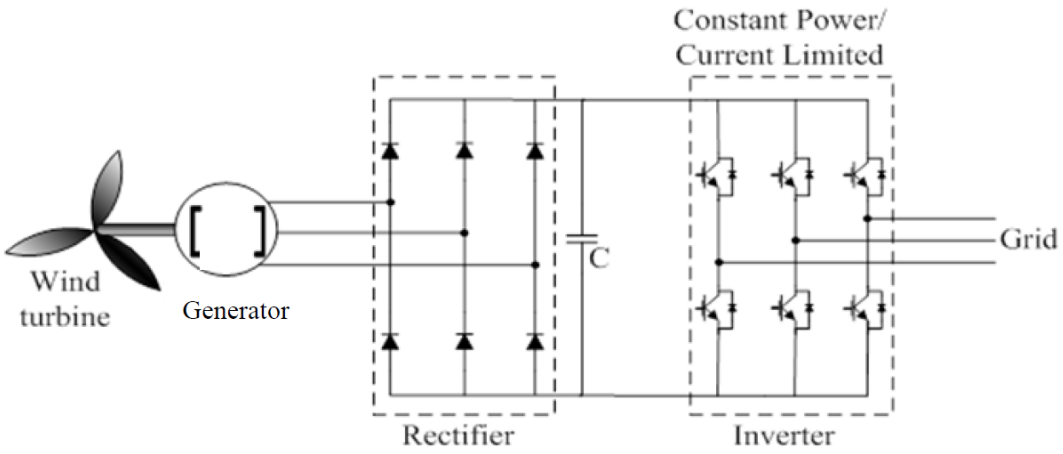


Figure 7: WTG type IV topology [5]

The report mentions that the fault response of this type of wind plant is highly dependent on the control strategy implemented. However, the inverter of this type of wind plant is assumed to only inject a symmetrical current under balanced and unbalanced faults. In other words, the wind turbine is not injecting any Negative or Zero-sequence current during a fault.

The second paper [6] presents a fault current and overvoltage calculations of a typical distribution circuit with solar photovoltaic (PV) in figure 8 creating a sequence network model shown in figure 9.

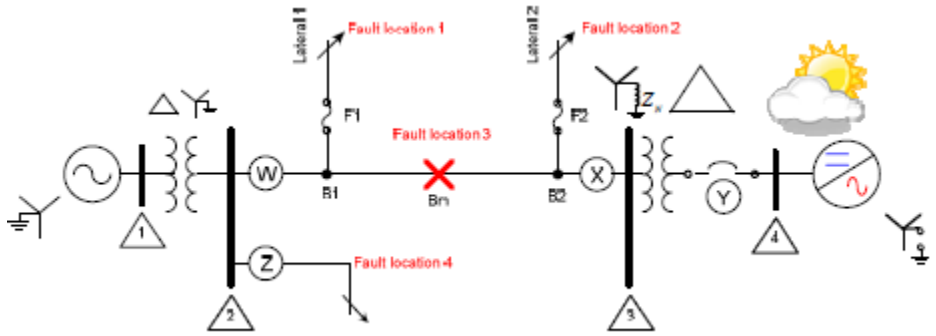


Figure 8: Distribution circuit under study [6]

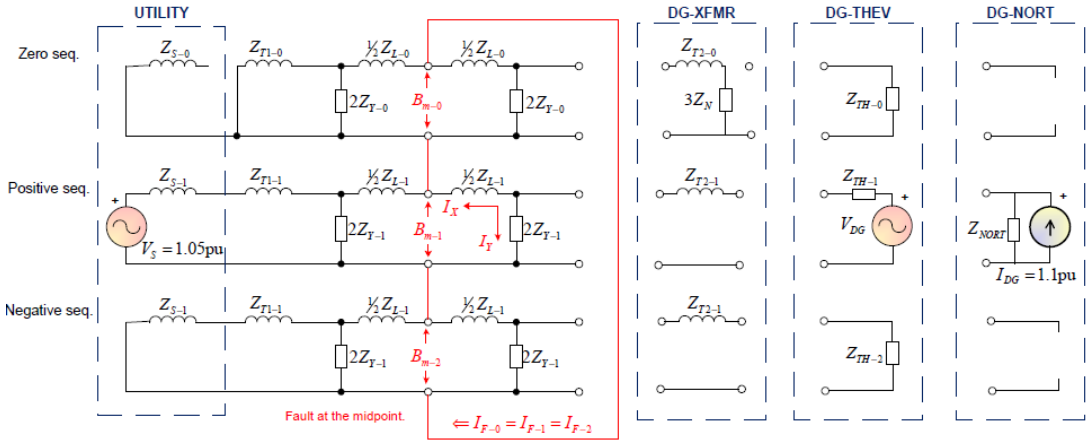


Figure 9: Sequence network of the distribution circuit [6]

In figure 9 the inverter is modeled as a current source that provides only a positive sequence of current. It is important to notice that the inverter is interfaced with a Wye-Delta three-phase transformer that acts, in zero sequence, as an open circuit across the zero sequence network of the inverter. Therefore, even if the inverter provides a zero sequence of current, this current would not flow throughout the rest of the zero sequence network of the distribution circuit.

As a conclusion, a current controlled inverter is assumed to provide only a positive sequence of current under balanced and unbalanced conditions. In [6], this assumption is accurate because the inverter is interconnected with a Delta-Wye three-phase transformer that acts as an open circuit in the Zero-sequence domain and will prevent any Zero-sequence current from flowing to the distribution circuit. Hence, the scope of this work is to prove that the case study in [6] is a particular case and that an inverter without interfacing Delta-Wye three-phase inverter can’t be modeled as providing only a Positive-sequence of current under unbalanced conditions.

3.0 GRID-TIED CURRENT CONTROLLED INVERTER ANALYSIS

The purpose of this chapter is to highlight key elements in the design of the inverter described as a Two Level, Three Phase Voltage-Sourced Converter. The first section describes the steps to obtain the averaged model of the converter, The second section introduces the Park Transformation used to simplify the design of its current control loop presented in section 3 [3]. The voltage sourced inverter is said "grid-tied" as the inverter picks up the frequency the electrical network to produce AC voltages that have the same frequency. Therefore, the design of the Phase-Locked Loop (PLL), aiming at extracting the electrical grid frequency, is described in section 3. Finally, the section 4 describes the validation of the model with a PLECS simulation.

3.1 GRID-TIED CURRENT CONTROLLED INVERTER ANALYSIS

3.1.1 Three Phase Voltage Sourced Converter Switched Model

The Three-Phase Voltage Sourced Inverter in figure 10 is composed of three half-bridge converter that will each convert the input DC voltage into an AC voltage on each phase. The converter is called "Voltage Sourced" because the input of the converter is composed of DC voltage sources. Furthermore, this Three-Phase Voltage Sourced Inverter is called "Two-level" as voltages V_{ta}, V_{tb}, V_{tc} can be only $-V_{DC}/2$ or $V_{DC}/2$. The first step to get the averaged model of

the converter is to mathematically describe the functioning of one phase, that is to say, one half-bridge converter.

The single phase DC/AC half bridge converter in figure 11 produces an AC voltage alternating the switch of two “switch cells”. A switch cell is composed of a unidirectional switch, such as an IGBT, and a diode connected in antiparallel to make a fully controllable *reverse*

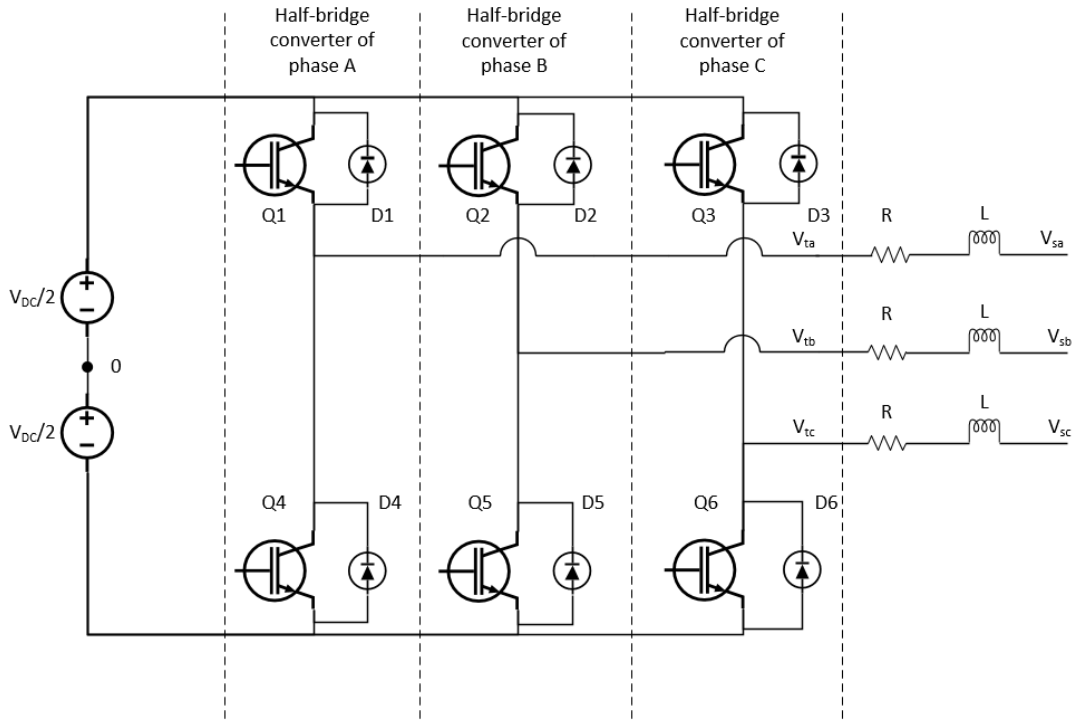


Figure 10: Three-Phase Voltage Sourced Converter

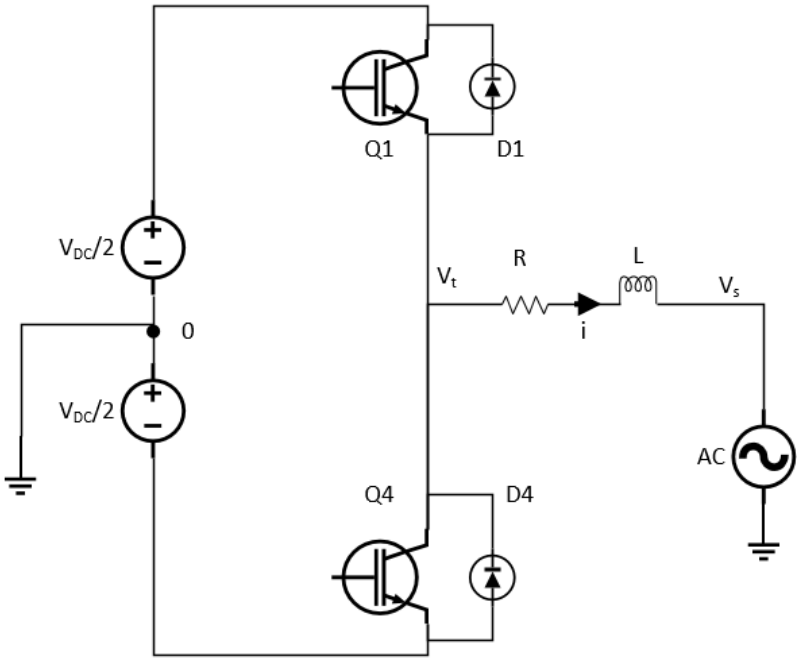


Figure 11: DC/AC Single-Phase Half Bridge Converter

conducting switch. The main feature of such a switch is that it can be considered as a unipolar switch that is able to conduct in the opposite direction when reverse biased by a small voltage. The converter is controlled through the gates of the IGBT in each switch cell thanks to "switching functions". A switching function can be defined by the following statement:

$$s_{1,4}(t) = \begin{cases} 1, & turn\ on\ command\ for\ the\ switch \\ 0, & turn\ off\ command\ for\ the\ switch \end{cases} \quad (3\text{-}1)$$

Let $s_1(t)$ and $s_4(t)$ be the switching function of the switch cell 1 and switch cell 4 respectively. Then it is possible to describe the waveform of the output voltage considering two cases related to the direction of the output current.

This analysis requires to state several assumptions to obtained the switched model of the Half-Bridge converter:

- The diodes and IGBT are considered as perfect switch
- Transition from a conduction state to a blocking state takes place instantaneously

Q_1 and Q_4 can't be commanded to conduct in the same time as it would short-circuit the DC input voltage.

Referring to figure 2, in the case of a positive current *i*:

- If $s_1(t)=0$ then Q_1 is blocked. The current *i* can't flow through D_1 because i_{D1} can't be negative. As i_{Q4} can't be negative, Q_4 is blocked even if $s_4(t)=1$ and the current can only flow through D_4.

$$V_t = V_n = -V_{DC}/2 \tag{3-2}$$

- If $s_1(t)=1$ then $s_4(t)=0$ then Q_1 conducts and Q_4 is blocked. The current *i* still can't flow through D_1 because i_{D1} can't be negative. The diode D_4 is reverse biased and is blocked.

$$V_t = V_n = -V_{DC}/2 \tag{3-3}$$

In the case of a negative current *i*:

- If $s_4(t)=0$ then Q_4 is blocked. The current *i* can't flow through D_4 because i_{D4} can't be negative. As i_{Q1} can't be negative, Q_1 is blocked even if $s_1(t)=1$ and the current *i* can only flow through D_1.

$$V_t = V_p = V_{DC}/2 \tag{3-4}$$

- If $s_4(t)=1$ then $s_1(t)=0$ then Q_1 conducts and Q_4 is blocked. The current *i* still can't flow through D_4 because i_{D4} can't be negative. The diode D_1 is reverse biased and is blocked.

$$V_t = V_p = V_{DC}/2 \tag{3-5}$$

Therefore, independently from the current *i* sign:

- If $s_1(t)=1$ and $s_4(t)=0$ then $V_t = V_p = V_{DC}/2$
- If $s_4(t)=1$ and $s_1(t)=0$ then $V_t = V_n = -V_{DC}/2$

The switched model of the half-bridge converter is therefore given by:

$$V_t(t) = \left({}^{V_{DC}}/_{2}\right) s_1(t) - \left({}^{V_{DC}}/_{2}\right) s_4(t) \tag{3-6}$$

To establish a simpler switched model of the half-bridge converter it is assumed that the switching functions satisfy the following condition.

$$s_1(t) + s_4(t) = 1 \tag{3-7}$$

Finally, the switched model of the half-bridge converter can be expressed by (3-8).

$$V_t(t) = {}^{V_{DC}}/_{2}\,(2s_1(t) - 1) \tag{3-8}$$

To get a more accurate expression of the switched model, it is necessary to take into account the process used to issue the turn on/off commands for switches. The pulse-width modulation (PWM) is a classical method to build switching functions. This method consists in comparing a modulating signal acting as the command with a triangular waveform of period T_s to create a square waveform. As shown by the figure, if the modulating signal, also called modulation index is higher in amplitude than the carrier then the switching function value is set to 1 otherwise the value is set to 0. The result is a square waveform with a duty cycle that vary from a switching interval $\widehat{T_s}$ to another.

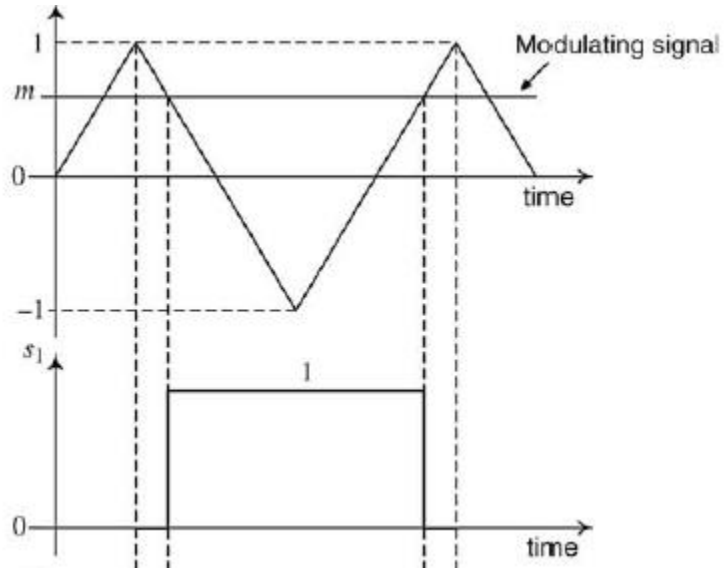


Figure 12: Comparison of a triangle waveform with a modulating signal to realize a PWM on a switching function [3]

If the modulating signal m is constant over the switching interval $\widehat{T_s}$, the resulting duty cycle d for this interval follows the relation below.

$$d = \frac{m}{2} + 0.5 \tag{3-9}$$

Let's study the particular case where the modulating signal is a sinusoidal function of the time:

$$m(t) = M\cos(\omega t) \tag{3-10}$$

To continue the analysis, it has to be assumed that $\frac{2\pi}{T_S} \gg \omega$. Therefore, at the scale of a switching interval T_s, $m(t)$ is a constant value. The value of duty cycle during a switching interval $\widehat{T_s}$ is labeled $D|_{\widehat{T_s}}$. Yet, it is important to note that $D|_{\widehat{T_s}}$ will change from a cycle to another.

The switching function $s_1(t)$ can be expressed by:

$$s_1(t) = D|_{\widehat{T_s}} + \frac{2}{\pi}\sum_{n=1}^{+\infty}\frac{\sin(n\pi D|_{\widehat{T_s}})}{n}\cos(n\omega_s t - n\varphi_s) \tag{3-11}$$

Plugging the expression above into (3-8), it is possible to give a new expression including harmonics for the switched model of the Half-Bridge converter in (3-12)

$$V_t(t) = {}^{V_{DC}}/_{2}\left(2D|_{\widehat{T_s}} - 1\right) + \frac{2V_{DC}}{\pi}\sum_{n=1}^{+\infty}\frac{\sin(n\pi D|_{\widehat{T_s}})}{n}\cos(n\omega_s t - n\varphi_s) \tag{3-12}$$

3.1.2 Three-Phase Voltage Sourced Converter Average Model

The dynamic equation of the output current of the converter is represented by (3-13)

$$L\frac{di(t)}{dt} + Ri(t) = V_t(t) - V_s(t) \tag{3-13}$$

$V_s(t) = V_s\cos(\omega t)$ corresponds to the voltage of the grid in figure 10. This voltage is considered as constant during a switching interval T_s as $\frac{2\pi}{T_S} \gg \omega$.

By superposition it is possible to consider the dynamic of the output current as the summation of the response of the DC component of $V_t(t)$ labeled $\overline{\imath(t)}$ and the response of the AC component of $V_t(t)$ labeled $\widetilde{\imath(t)}$

$$\begin{gathered}
\frac{d\overline{\imath(t)}}{dt} + R\overline{\imath(t)} = {}^{V_{DC}}/_{2}\left(2D|_{\widehat{T_s}} - 1\right) - V_s(nT_s) \\
L\frac{d\widetilde{\imath(t)}}{dt} + R\widetilde{\imath(t)} = \frac{2V_{DC}}{\pi}\sum_{n=1}^{+\infty}\frac{\sin(n\pi D|_{\widehat{T_s}})}{n}\cos(n\omega_s t - n\varphi_s) \\
i(t) = \overline{\imath(t)} + \widetilde{\imath(t)}
\end{gathered} \tag{3-14}$$

The dynamic equation of the output current represents a low-pass filter with a cut-off frequency $\omega_c = \frac{R}{L}$. Therefore if $\frac{2\pi}{T_s} \gg \omega_c$, the impact of $\widetilde{\imath(t)}$ on $i(t)$ is negligible and the dynamic equation for the current can be expressed in (3-15).

$$L\frac{d\overline{\imath(t)}}{dt} + R\overline{\imath(t)} = {}^{V_{DC}}/_{2}\left(2D|_{\widehat{T_s}} - 1\right) - V_s(t) \tag{3-15}$$

It is important to notice that the response of the DC component (3-15) can be extracted from the dynamic equation of current in (3-13) by applying the average operator to the two sides of the equation. As the average of a variable can vary from one switch cycle to another, the average operator is given by the equation below.

$$\overline{x(t)} = \frac{1}{T_s}\int_{t}^{t-T_s} x(t)dt \tag{3-16}$$

This operator can only be applied if the frequency of the carrier signal $\frac{1}{T_s}$ is higher than the frequency of the modulating signal (10 times higher). Moreover, as T_s can be considered to be very small, the averaged model of the output current of the single phase half-bridge converter is given by the equation (3-4) by expressing the varying duty cycle as a function of the modulation index.

$$L\frac{d\overline{\imath(t)}}{dt} + R\overline{\imath(t)} = \frac{MV_{DC}}{2}\cos(\omega t) - V_s(t) \tag{3-17}$$

The modulation index $m(t)$ represents therefore the ratio between the input voltage ($\frac{V_{DC}}{2}$) and the output voltage of the converter. As the duty cycle of the switching function can't be superior to 1 over a switching interval the amplitude of $m(t)$ can't go above 1 otherwise the converter will start to saturate.

Going back to the three-phase voltage sourced converter, it is possible to consider the system with three dynamic equations (3-18), one per phase, with three inputs represented by the modulation indexes in (3-19) applied to each phase of the converter. Each phase voltage of the grid can be seen as a disturbance while the current of each phase represent the output of the system.

$$\begin{cases} L\dfrac{d\overline{\imath_a(t)}}{dt} + R\overline{\imath_a(t)} = \dfrac{V_{DC}}{2}m_a(t) - V_s\cos(\omega t) \\ L\dfrac{d\overline{\imath_b(t)}}{dt} + R\overline{\imath_b(t)} = \dfrac{V_{DC}}{2}m_b(t) - V_s\cos(\omega t - \dfrac{2\pi}{3}) \\ L\dfrac{d\overline{\imath_c(t)}}{dt} + R\overline{\imath_c(t)} = \dfrac{V_{DC}}{2}m_c(t) - V_s\cos(\omega t + \dfrac{2\pi}{3}) \end{cases} \tag{3-18}$$

$$\begin{cases} m_a(t) = M_a\cos(\omega t) \\ m_b(t) = M_b\cos(\omega t - \dfrac{2\pi}{3}) \\ m_c(t) = M_c\cos(\omega t + \dfrac{2\pi}{3}) \end{cases} \tag{3-19}$$

To control the system and get balanced three-phase currents, time varying references have to be used for each phase. Consequently, this control will involve complex compensators to track with zero steady state error and no phase delay the time-varying reference. Another solution is to implement a control strategy in the dq-frame using the Park transformation on the equations (3-18) and (3-19). As the references to track for this control strategy will be DC values only PI compensators would be required. The next section realizes a deep analysis of the Park transformation and use to design the current control of the three-phase voltage sourced converter.

3.2 PARK TRANSFORMATION FUNDAMENTALS

To understand and build a better intuition of the Park transformation, let's consider the concept of space phasor (3-20) of a balanced set of time varying functions (3-21).

$$\begin{cases} f_a(t) = \hat{f}cos(\omega t + \theta_0) \\ f_b(t) = \hat{f}cos(\omega t - \frac{2\pi}{3} + \theta_0) \\ f_c(t) = \hat{f}cos(\omega t + \frac{2\pi}{3} + \theta_0) \end{cases} \tag{3-20}$$

$$\overrightarrow{f(t)} = \frac{2}{3}\left[e^{j0}f_a(t) + e^{j\frac{2\pi}{3}}f_b(t) + e^{j\frac{2\pi}{3}}f_b(t)\right] = \left(\hat{f}e^{j\theta_0}\right)e^{j\omega t} = \underline{f}e^{j\omega t} \tag{3-21}$$

In (3-20), $\hat{f}$ refers to a time varying amplitude and θ_0 to the initial phase angle. If $\hat{f}$ is constant, $\overrightarrow{f(t)}$ can be represented by a vector in the complex plane turning counterclockwise at the speed ω in figure 13.

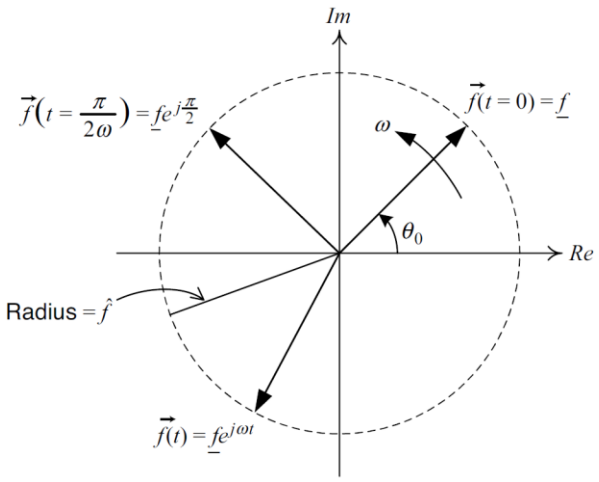


Figure 13: Space phasor in the complex plane [3]

The equations in (3-22) might be used to extract the time domain functions from the space phasor.

$$\begin{aligned} f_a(t) &= Re\{\overrightarrow{f(t)}e^{-j0}\} \\ f_b(t) &= Re\left\{\overrightarrow{f(t)}e^{-j\frac{2\pi}{3}}\right\} \\ f_c(t) &= Re\left\{\overrightarrow{f(t)}e^{-j\frac{2\pi}{3}}\right\} \end{aligned} \tag{3-22}$$

With the concept of space phasor comes the space phasor phase-shifter/scaler in (3-23) that aims at changing the amplitude and phase of the three-phase signal.

$$\overrightarrow{f'}(t) = \overrightarrow{f(t)}A(t)e^{j\emptyset(t)} \tag{3-23}$$

The Park transformation (3-24) is a particular case of a space phasor phase-shifter/scaler that only phase shifts the space phasor of an angle $-\varepsilon(t) = \varepsilon_0 + \int \omega(\tau)d\tau$.

$$f_d + jf_q = \left(\overrightarrow{f(t)}\right)e^{-j\varepsilon(t)} = \left(\underline{f}e^{j\omega t}\right)e^{-j\varepsilon(t)} = \hat{f}e^{j(\theta_0-\varepsilon_0)} \tag{3-24}$$

If $\hat{f}$ is constant, then the result of the transformation is a constant complex number. To realize properly the Park transformation, $\frac{d\varepsilon(t)}{dt}$ must be equal to ω but ε_0 is not necessarily equal to θ_0 . The transformation can also be understood as the projection of the space phasor in a "synchronously rotating reference frame" in figure 14. The Clark transformation is the expression of the real (α) and imaginary (β) component of the space phasor and can also be seen as a projection in a static reference frame.

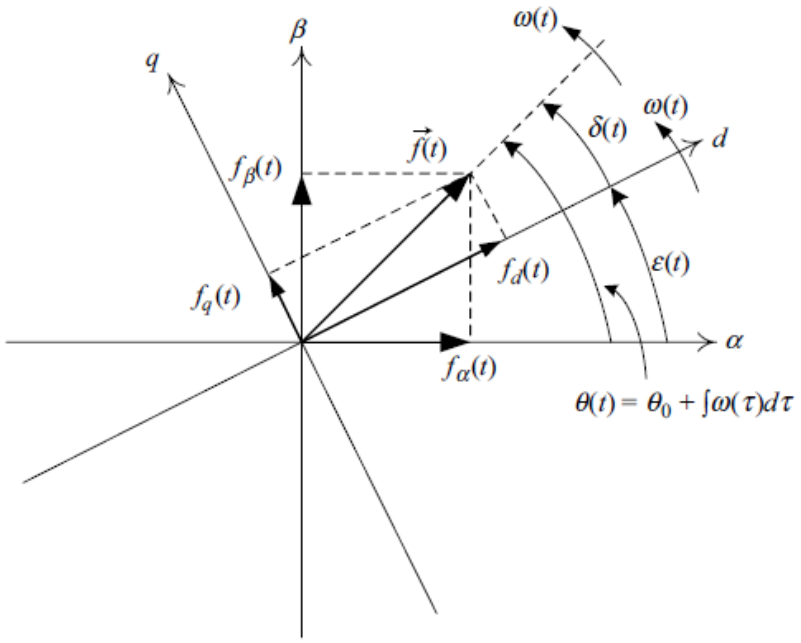


Figure 14: dq- and αβ- coordinate of a space-phasor [3]

As the transformation is currently using three AC inputs to get two DC outputs, the common mode or zero component in (3-25) is generally added to the result of this phase shift to make the whole Park transformation.

$$f_0 = \frac{1}{3}(f_a(t) + f_b(t) + f_c(t)) \tag{3-25}$$

In control design considerations, nominal conditions assume balanced signals making the Zero-sequence component equal to zero. Therefore, this component is often not taken into account and only the space phasor expressed in the synchronously rotating frame in (3-24) is considered.

In practical applications the transformation in (3-26) and (3-27) are used to directly express the dqo components from three-phase signal and the time varying signals from dqo components respectively.

$$\begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos(\varepsilon(t)) & \cos(\varepsilon(t)-\frac{2\pi}{3}) & \cos(\varepsilon(t)+\frac{2\pi}{3}) \\ \sin(\varepsilon(t)) & \sin(\varepsilon(t)-\frac{2\pi}{3}) & \sin(\varepsilon(t)+\frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} \tag{3-26}$$

$$\begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} = \begin{bmatrix} \cos(\varepsilon(t)) & \sin(\varepsilon(t)) & 1 \\ \cos(\varepsilon(t)-\frac{2\pi}{3}) & \sin(\varepsilon(t)-\frac{2\pi}{3}) & 1 \\ \cos(\varepsilon(t)+\frac{2\pi}{3}) & \sin(\varepsilon(t)+\frac{2\pi}{3}) & 1 \end{bmatrix}\begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} \tag{3-27}$$

3.3 CURRENT CONTROL IN THE DQ-FRAME OF THE GRID IMPOSED FREQUENCY THREE-PHASE VOLTAGE SOURCED CONVERTER

3.3.1 Dynamic Model of the Voltage Sourced Converter in the dq-frame

As equations (3-18) and (3-19) are representing a decoupled symmetrical three-phase system, it is possible to express a dynamic equation relating the space phasors of each variable in (3-28) using the operation introduced in (3-21) on the set of equations in (3-18)

$$L\frac{d\overrightarrow{\imath(t)}}{dt} + R\overrightarrow{\imath(t)} = \frac{V_{DC}}{2}\overrightarrow{m(t)} - V_s e^{j\omega t+\theta_0} \tag{3-28}$$

It is assumed that the space phasor of each variable has a constant amplitude. Moreover if the dq components of the modulation index and the current are obtained using a rotating frame that is not rotating at the speed ω but realizing a phase shift of angle -ε(t) of the space phasor,

$$\begin{aligned}\overrightarrow{\imath(t)} &= (i_d + ji_q)e^{j\varepsilon(t)} \\ \overrightarrow{m(t)} &= (m_d + jm_q)e^{j\varepsilon(t)}\end{aligned} \tag{3-29}$$

The equation (3-28) can be transformed into the equations (3-30) using the new expressions for the current and the modulation index above and separating the real components from the imaginary components, with $V_{sd} = V_s\cos(\omega t + \theta_0 - \varepsilon(t))$ and $V_{sq} = V_s\sin(\omega t + \theta_0 - \varepsilon(t))$

$$\begin{cases} L\dfrac{di_d}{dt} - L\dfrac{d\varepsilon(t)}{dt}I_q + Ri_d = \dfrac{V_{DC}}{2}m_d - V_{sd}(t) \\ L\dfrac{di_q}{dt} + L\dfrac{d\varepsilon(t)}{dt}I_d + Ri_q = \dfrac{V_{DC}}{2}m_q - V_{sq}(t) \end{cases} \tag{3-30}$$

In the case that $\varepsilon(t) = \omega t + \theta_0$, the equation (3-30) can be simplified to get the equation in (3-31)

$$\begin{cases} L\dfrac{di_d}{dt} - L\omega I_q + Ri_d = \dfrac{V_{DC}}{2}m_d - V_s \\ L\dfrac{di_q}{dt} + L\omega I_d + Ri_q = \dfrac{V_{DC}}{2}m_q \end{cases} \tag{3-31}$$

As the input modulation indexes in dq-frame are DC references then i_d and i_q are DC variables in steady-state. The equations in (3-32) represent the dq components of output current in steady-state and considering that the dq component of each variable is computed using a synchronously rotating frame.

$$\begin{cases} L\omega I_q + Ri_d = \dfrac{V_{DC}}{2} m_d - V_s \\ L\omega I_d + Ri_q = \dfrac{V_{DC}}{2} m_q \end{cases} \tag{3-32}$$

The PLL extracts the frequency of the grid voltage to fulfill the requirement of a synchronously rotating frame. The next part describes the design of such a function.

3.3.2 Design and Control of the PLL

The main function of a PLL is to extract the frequency of the grid voltage so that the inverter is able to produce a three-phase output voltage having the same frequency. This frequency is used to realize the Park transformation of input and output variables for the control in the dq-frame of the inverter.

To realize such a function, the q component of the grid voltage V_{sq} will be used to adjust the angle $\varepsilon(t)$ to be equal to $\omega t + \theta_0$. It is important to notice that to make such an adjustment, $\varepsilon(t)$ has to be set to regulate V_{sq} to 0. However, the expression of V_{sq} is a sinusoidal function and can't be used directly as a feedback signal to regulate $\varepsilon(t)$. If $\varepsilon(t)$ respects the initial conditions in (3-33) then it is possible to state that $V_{sq} \approx V_s(\omega t + \theta_0 - \varepsilon(t))$.

$$\frac{d\varepsilon}{dt}(0) = \omega_\epsilon(0) = \omega$$
$$\omega_{\epsilon min} \leq \omega_\epsilon \leq \omega_{\epsilon max} \tag{3-33}$$

The process of PLL presented in figure 15 is able to track $\omega t + \theta_0$ and can be transformed into a classical feedback control block diagram in figure 16.

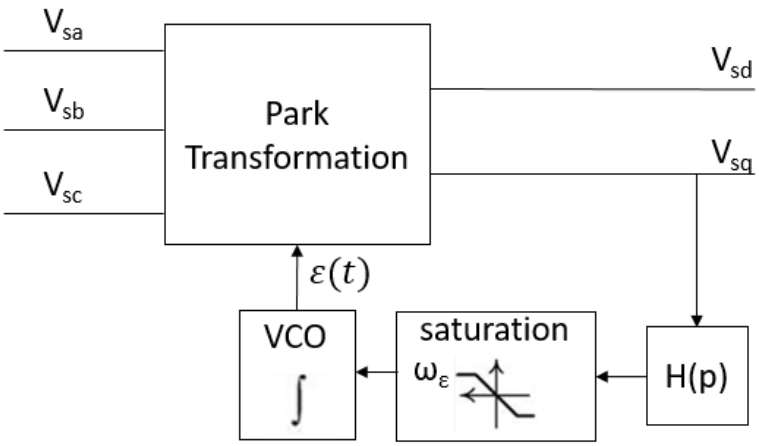


Figure 15: Schematic of the Phase Locked Loop (PLL) process

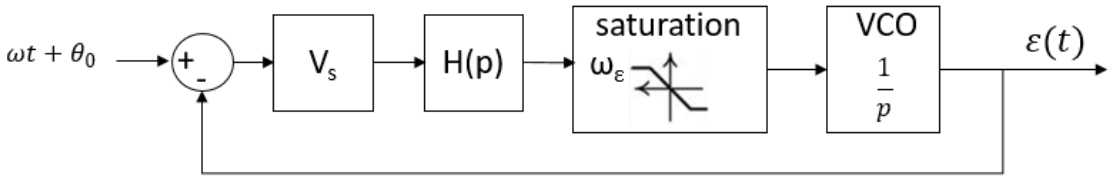


Figure 16: Equivalent Feedback control loop diagram

The VCO in figure 15 and 16 can be represented as a resettable integrator of ω_ϵ every time the result of the integration reaches 2π.

If the voltage grid is under nominal conditions, then the loop gain needs to integrate two integrators as the reference $\omega t + \theta_0$ is a ramp function. Therefore, the compensator H(p) needs to contain at least one integrator for $\varepsilon(t)$ to track $(\omega t + \theta_0)$ without steady-state error. However, the expression of V_{sq} is different if the voltage grid is unbalanced changing the design features of the compensator H(p).

3.3.3 Compensator design for PLL under non-nominal conditions

As seen in the first chapter, the event of a single line-to-ground fault brings a zero and a negative sequence component in the grid voltage that is therefore expressed in (3-34)

$$\begin{cases} V_{sa}(t) = V_{s1}cos(\omega t + \theta_0) + V_{s2}cos(\omega t + \theta_0) + V_{s0}cos(\omega t + \theta_0) \\ V_{sb}(t) = V_{s1}cos\left(\omega t + \theta_0 - \frac{2\pi}{3}\right) + V_{s2}cos\left(\omega t + \theta_0 - \frac{4\pi}{3}\right) + V_{s0}cos(\omega t + \theta_0) \\ V_{sc}(t) = V_{s1}cos\left(\omega t + \theta_0 - \frac{4\pi}{3}\right) + V_{s2}cos\left(\omega t + \theta_0 - \frac{2\pi}{3}\right) + V_{s0}cos(\omega t + \theta_0) \end{cases} \quad (3\text{-}34)$$

The space phasor of the set of voltages in (3-34) is expressed in (3-35) and shows that the zero component no longer appears in the expression of the space phasor.

$$\overrightarrow{V_s(t)} = (V_{s1} + V_{s2}e^{-j2\omega t})e^{j(\omega t + \theta_0)} \quad (3\text{-}35)$$

The space phasor of the Negative-sequence component can be represented by a vector turning clockwise at the speed ω. Therefore, a projection of this component on a frame that is rotating counterclockwise at the speed ω represents a vector turning at the speed -2ω clockwise.

Therefore, the impact of the negative sequence component is a complex time-varying expression representing a phase shift of $-2\omega t$ in (3-35). The expression in (3-36) gives the Park Transformation of (3-35) in the synchronously rotating frame.

$$\begin{cases} V_{sd} = V_{s1} + V_{s2}\cos(2\omega t) \\ V_{sq} = -V_{s2}\sin(2\omega t) \end{cases} \tag{3-36}$$

The expression of V_{sq} tells that a sinusoidal component is present when the angle $\varepsilon(t)$ has reached the reference $\omega t + \theta_0$. Therefore, if the compensator doesn't remove this component from V_{sq}, ω_ϵ and $\varepsilon(t)$ will contain it and lead to distortions of signals transformed from dq- to abc- frame and from abc- to dq- frame. One solution is to design the compensator to have strong low-pass filter characteristics but it will reduce the closed-loop bandwidth of the PLL. Another solution is to include one pair of complex conjugate zeros at $s = \mp j2\omega_0$ so that the sinusoidal component of V_{sq} expected in steady-state will not be present in ω_ϵ and $\varepsilon(t)$ without reducing the closed-loop bandwidth of the PLL.

3.3.4 Current control loop in the dq-frame

First of all, it is important to notice that the set of equation in (3-31) are coupled and can't be used directly. However, it is possible to decouple these equations by adding the dq components of the grid signal and the dq components of current to the input dq components of the modulation index. If the expression of the modulation index in (3-37) is plugged into (3-31), it is possible to get two decoupled dynamic equations for the output current represented in (3-38).

$$\begin{cases} m_d = \dfrac{2}{V_{DC}}(u_d - L\omega i_q + V_{sd}) \\ m_q = \dfrac{2}{V_{DC}}(u_q + L\omega i_d + V_{sq}) \end{cases} \tag{3-37}$$

$$\begin{cases} L\dfrac{di_d}{dt} + Ri_d = u_d \\ L\dfrac{di_q}{dt} + Ri_q = u_q \end{cases} \tag{3-38}$$

The equations in (3-38) are two first order equations leading to the expression of transfer functions of the system for the d- and q- axis using Laplace transformation in (3-39).

$$\frac{I_d(s)}{U_d(s)} = \frac{I_q(s)}{U_q(s)} = \frac{1}{R + Ls} \tag{3-39}$$

Therefore, the d-axis and q-axis can be controlled independently with two feedback loops in figure 17 thanks to the new inputs u_d and u_q respectively, outputs of the compensator in the d-axis control loop and of the compensator in the q-axis respectively.

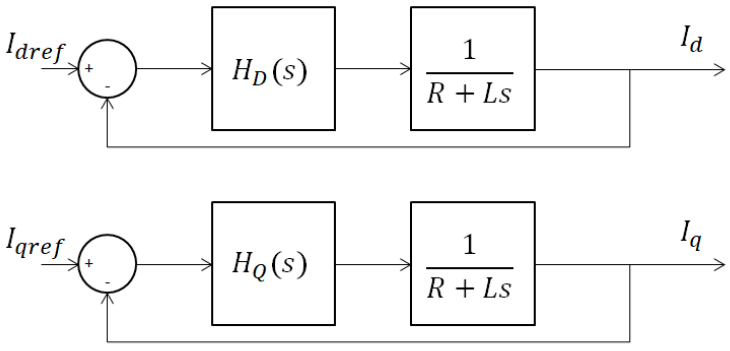


Figure 17: d-axis and q-axis control block diagram

The compensators for the d- and q- axis are identical so that $H_D(s) = H_Q(s) = H_{DQ}(s)$. The equivalent transfer function linking the reference current i_{dref} and i_{qref} to the output current i_d and i_q respectively are expressed in (3-40)

$$\frac{i_d}{i_{dref}} = \frac{i_q}{i_{qref}} = \frac{\frac{H_{DQ}(s)}{R + Ls}}{1 + \frac{H_{DQ}(s)}{R + Ls}} \tag{3-40}$$

The compensator H_{DQ} is chosen to be a PI compensator as one integrator is required to track a DC reference with zero steady-state error. First of all, the proportional gain k_p and integral gains k_i will be designed to compensate the pole of the system at $s = -\frac{R}{L}$ as this pole represents a small frequency or a big time constant.

$$H_{DQ}(s) = \frac{k_p s + k_i}{s} \tag{3-41}$$

The two degrees of liberty offered by the two parameters of the compensator allows setting a new time constant τ_i for the control loop dynamic. On one hand this time constant needs to be small enough to ensure a fast tracking of the reference. On the other hand, this time constant needs to be big enough for the system to filter the switching harmonics. Typically, the closed-loop bandwidth should be at least ten times smaller than the switching frequency. To respect the two previous constraints, k_p and k_i are computed thanks to the relations in (3-42).

$$\begin{cases} k_p = \frac{L}{\tau_i} \\ k_i = \frac{R}{\tau_i} \end{cases} \tag{3-42}$$

The closed-loop transfer function in (3-41) simplified with the new expression of the PI compensator is a first order behavior of time constant τ_i expressed in (3-43).

$$\frac{i_d}{i_{dref}} = \frac{i_q}{i_{qref}} = \frac{1}{1+\tau_i} \tag{3-43}$$

As the dq components of the current are the control input of the system, the converter is therefore seen as a current source that will provide, in steady-state, a balanced three-phase current obtained by realizing the inverse Park transformation of the dq references of current. However, in (3-23) the control of the inverter uses the voltage grid as a feedforward signal to decouple the dynamics of the d-axis and q-axis of the output current. Under unbalanced conditions the grid voltage might contain a zero component that will not be part of the feedforward signal as only the d and q component of the grid voltage are kept for control.

3.4 GRID-TIED CURRENT CONTROLLED INVERTER VALIDATION

This section is dedicated to validate through simulation results, the model of grid-tied current control inverter under nominal conditions presented in the previous section. The schematic figure 18 presents the simulation diagram used in PLECS.

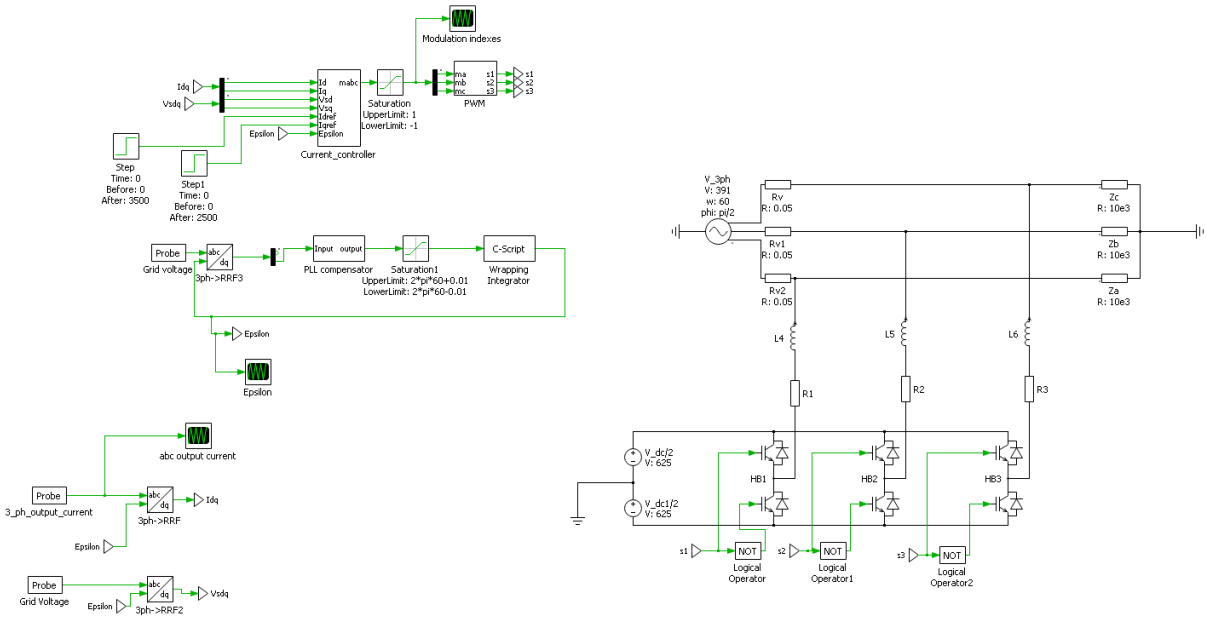


Figure 18: Current controlled inverter simulation diagram in PLECS

The schematic is composed of several subsystems for the sake of clarity. Each subsystem will be described in detail as well as the plot that are displayed on the picture. The simulation parameters chosen for the system are summarized on table 1.

If the output current of the inverter has reached references set by the control, then the amplitude of each line current is given by the relation below.

$$I_{Apk} = I_{Bpk} = I_{Cpk} = \sqrt{{I_{dref}}^2 + {I_{qref}}^2} = 4301.16A \tag{3-44}$$

The figure 19 demonstrates that the line currents amplitudes are in agreement with the prediction of amplitude using the dq components of the current reference.

Table 1. Simulation parameters for the model validation in PLECS

Parameter	Value
AC Voltage source magnitude	480 V_{RMS} line-to-line
AC voltage source frequency	60 Hz
Voltage source output impedance	0.05Ω
DC voltage source(V_{DC}/2)	625V
Line Resistance (R)	1.63 mΩ
Line Inductance (L)	100μH
Load Impedance per phase	10kΩ
Switching Frequency ($1/T_s$)	3420 Hz
d-axis reference current	3500
q-axis reference current	2500
Closed-loop time constant for d-axis and q-axis current (τ_i)	2 ms
PLL frequency upper limit ($\omega_{\varepsilon max}$)	377.001rad/s
PLL frequency lower limit ($\omega_{\varepsilon min}$)	376.981 rad/s

The modulation index of each phase presented in figure 20 show no sign of saturation as their amplitude never exceeds 1. Finally, the figure 21 demonstrates that the closed-loop of the PLL managed to track the grid frequency as the slope of the ramp curve during one cycle is equal to 376.9766 rad/s. The C-Script block in figure 18 simulates the behavior of a VCO and is provided by the PLECS library.

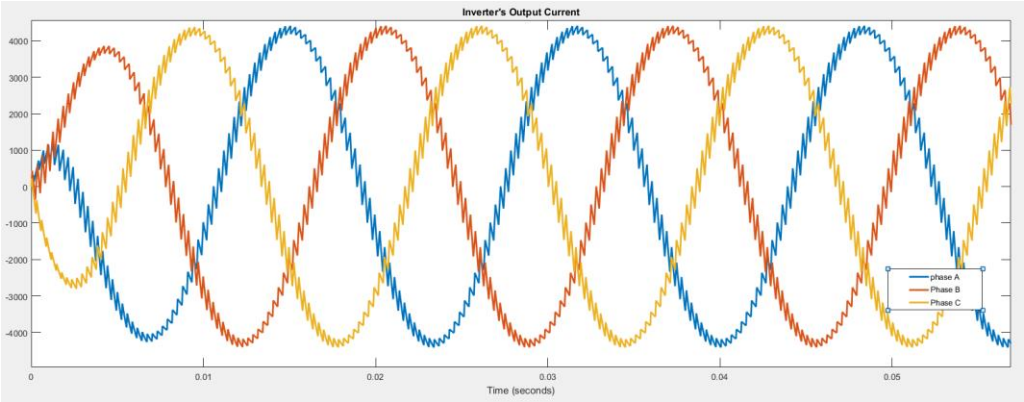


Figure 19: Line currents in time domain

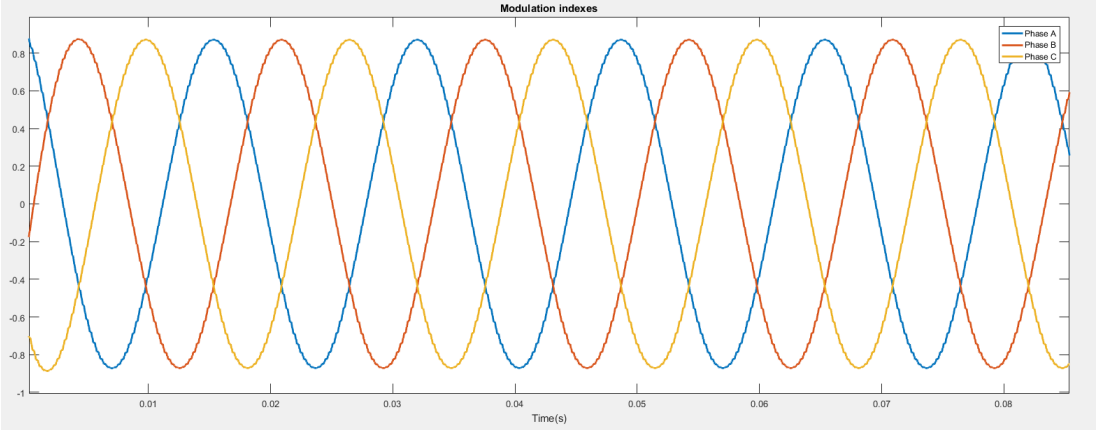


Figure 20: Modulation indexes of phase A, B and C in time domain

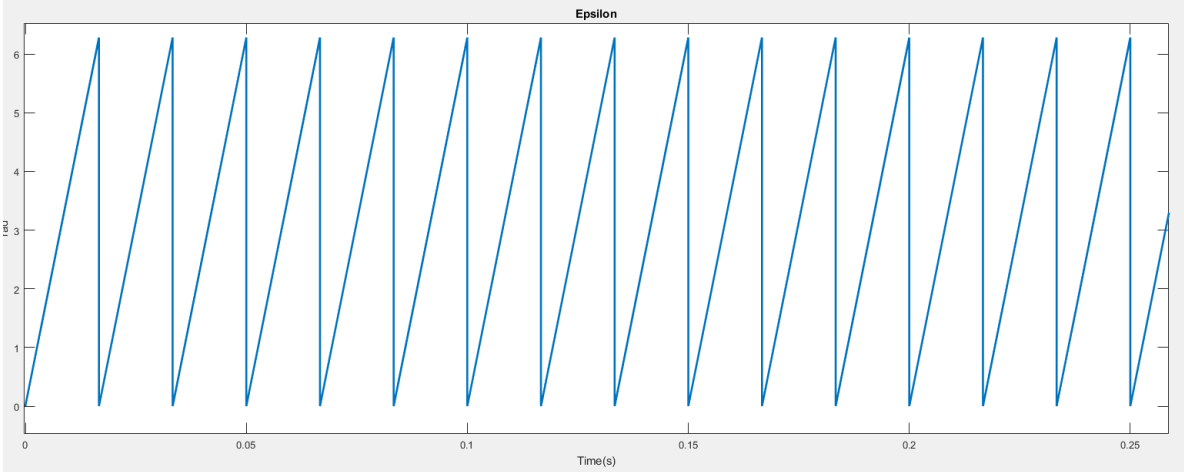


Figure 21: Dynamic of the angle Epsilon used for Park transformation

The detail of the PWM subsystem is shown in figure 22 and show the comparison of each modulating signal with a triangular waveform.

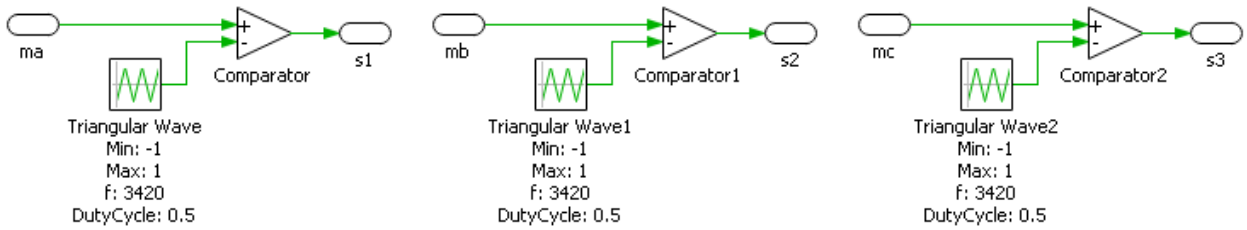


Figure 22: PWM producing the switching function for each phase

The schematic figure 23 illustrates the current controller of the inverter with the different signals operations to decouple the dynamics of the d- and q- axis and also the PI compensator respecting the following design constraints.

$$k_p = \frac{L}{\tau_i} = 0.05$$
$$k_i = \frac{R}{\tau_i} = 0.815 \qquad (3\text{-}45)$$

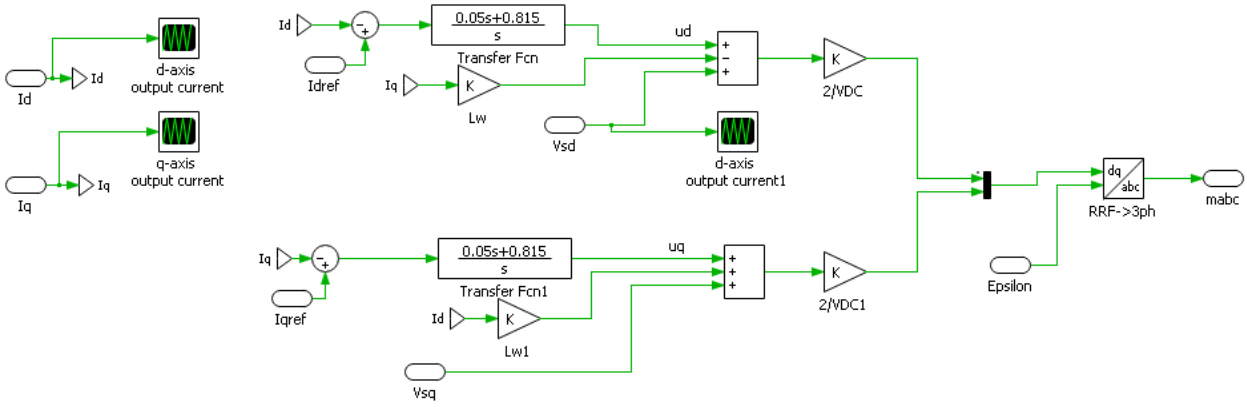


Figure 23: Current controller of the simulation model on PLECS

As the closed-loop transfer function for each axis of the current has a first order behavior of time constant τ_i = 2ms, then I_d and I_q will reach 63% of their steady-state value (2205 A for I_d and 1575 A for I_q) at time t=2ms. Plots in figure 24 and 25 prove that I_d and I_q have a first order behavior of time constant τ_i = 2ms set by the closed-loop transfer function as I_d and I_q reach 63% of their steady-state value (2205 A for I_d and 1575 A for I_q) at time t=2ms and reach 95% of their steady-state value after $5\tau_i$=10ms.

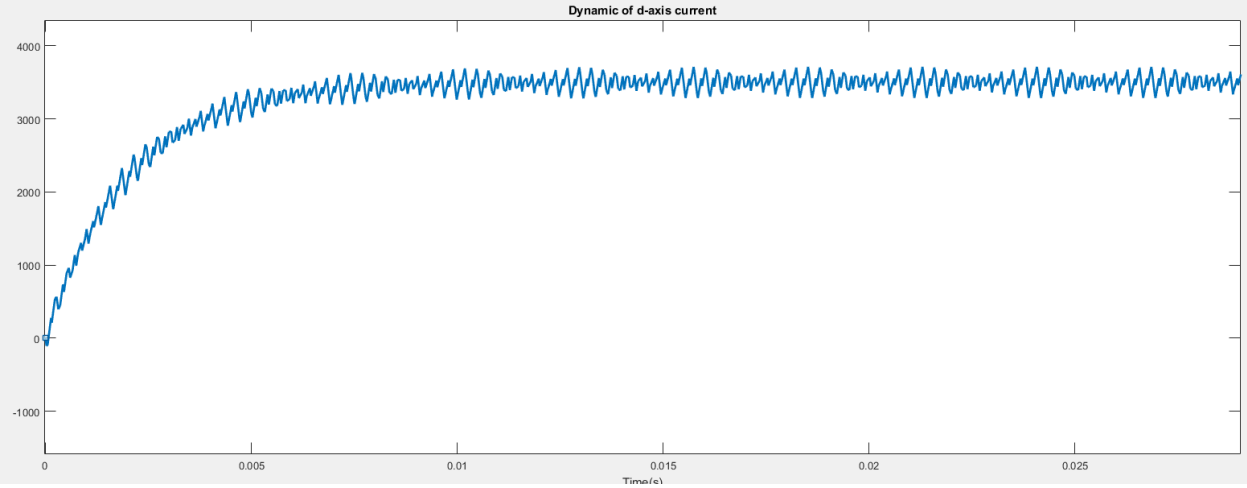


Figure 24: d-axis output current dynamic in time domain

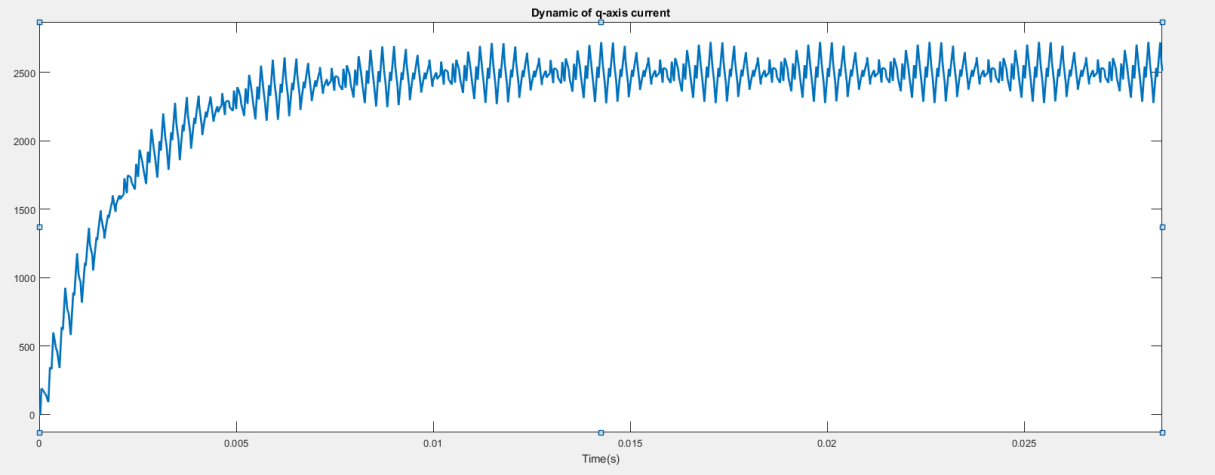


Figure 25: q-axis output current dynamic in time domain

4.0 IMPROVED SYMMETRICAL COMPONENT MODEL FOR A GRID-TIED, CURRENT CONTROLLED INVERTER

Even if grid interconnected current controlled inverters are designed based upon nominal grid voltage conditions it is possible to find in literature that specific voltage and current control architectures are based upon symmetrical components for handling unbalanced grid conditions [7]–[11]. However, most of the existing current controlled inverters use only the synchronously rotating frame for regulation. This control is based upon the assumption that the grid voltage is balanced and, as seen in chapter 3, requires only two closed feedback loops.

In chapter 2, a literature review established that the prediction of the fault response of a three-phase inverter with the control mentioned, a common practice is to model the inverter as an ideal current source in its positive sequence representation only [5], [6]. However, unbalanced loads on the grid are able to disturb the output voltage symmetry and the model prediction of an islanded inverter unless this inverter is interfaced to the grid through a wye-delta transformer [12]. The fault analysis in [6] is actually a special case where it is correct to model the inverter as a current source in the positive sequence only because the inverter is interfaced with a wye-delta transformer. As in [12], this transformer isolates the inverter from experiencing any zero sequence voltage provided by the grid experiencing a single line-to- ground fault (SLGF). Thus, without an interfacing transformer, the output current symmetry of the inverter in [6] would be disturbed due to the presence of a zero sequence voltage component. The inverter cannot be

modeled as an ideal source providing only a positive sequence current because this assumption will result in poor estimations of the expected fault current. This chapter will be organized as follows: Section 1 provides the necessary background knowledge on how to build sequence networks assuming the inverter acts as an ideal three-phase current source providing balanced currents. In Section 2, the control limitations of the inverter under a SLGF scenario are analyzed and used to create a proposed sequence network. Section 3 compares sequence networks of Section 1 and 2 with a computer simulation model conducted in PLECS.

4.1 INVERTER SEQUENCE NETWORK MODEL USING CLASSICAL ASSUMPTIONS FROM LITERATURE

The sequence network construction of figure 1 requires both the sequence components of the non-ideal three-phase voltage source and the inverter. One accepted community assumption is that the current controlled inverter generates balanced current during a fault. Therefore, the inverter will only provide a positive sequence current component defined by the phasor, $Ie^{j\phi}$. As the inverter is current controlled with references established in the synchronous reference frame, I_d and I_q, the positive sequence current phasor is determined by (4-1) and (4-2).

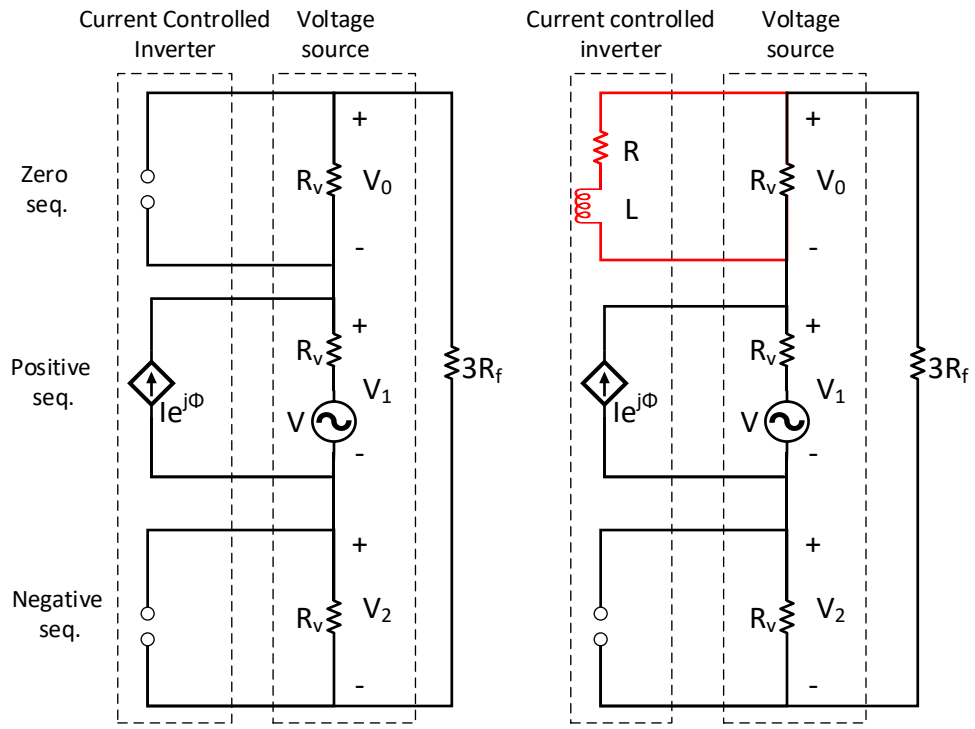


Figure 26: Sequence networks that model the fault response of a grid-tied, current controlled inverter in response to a SLGF with the classical assumptions on the inverter's behavior (left) and proposed (right).

$$I = \sqrt{{I_d}^2 + {I_q}^2} \tag{4-1}$$

$$\Phi = \begin{cases} \arctan\left(\frac{I_q}{I_d}\right) \; if \; I_d > 0 \\ \arctan\left(\frac{I_q}{I_d}\right) + \pi \; if \; I_d < 0, and \; I_q > 0 \\ \arctan\left(\frac{I_q}{I_d}\right) - \pi \; if \; I_d < 0, and \; I_q < 0 \end{cases} \tag{4-2}$$

Assuming that the pre-fault current magnitude is negligible compared to the fault current magnitude, a SLGF sequence network can be formulated and shown in the left of figure 26 thanks to the analysis realized in chapter 2.

4.2 SEQUENCE NETWORK MODEL ACCOUNTING FOR INVERTER CURRENT CONTROL

For our analysis here, it is assumed that the inverter does not output balanced currents during a fault. Fundamentally, the current controlled inverter uses the grid voltage as a feedforward signal to apply the proper voltage difference across the *RL* filter. In the context of this work, the inverter is controlled in the synchronous rotating reference frame. It is recalled that the dynamics associated with the inverter output current are governed by the relationships in (4-3).

$$\begin{cases} L\dfrac{di_d}{dt} - L\omega I_q + Ri_d = \dfrac{V_{DC}}{2}m_d - V_s \\ L\dfrac{di_q}{dt} + L\omega I_d + Ri_q = \dfrac{V_{DC}}{2}m_q \end{cases} \tag{4-3}$$

It is assumed that the grid voltage contains a positive, a negative and a zero sequence component due to the SLGF. A general expression for this set of voltages is given by (4-4). The *dq* components of the grid voltage signal can be shown to be (4-5). Note that V_{s1}, V_{s2}, and V_{s0} represent the positive, negative, and zero sequence voltage amplitudes, respectively.

$$\begin{cases} V_{sa}(t) = V_{s1}cos(\omega t + \theta_0) + V_{s2}cos(\omega t + \theta_0) + V_{s0}cos(\omega t + \theta_0) \\ V_{sb}(t) = V_{s1}cos\left(\omega t + \theta_0 - \dfrac{2\pi}{3}\right) + V_{s2}cos\left(\omega t + \theta_0 - \dfrac{4\pi}{3}\right) + V_{s0}cos(\omega t + \theta_0) \\ V_{sc}(t) = V_{s1}cos\left(\omega t + \theta_0 - \dfrac{4\pi}{3}\right) + V_{s2}cos\left(\omega t + \theta_0 - \dfrac{2\pi}{3}\right) + V_{s0}cos(\omega t + \theta_0) \end{cases} \tag{4-4}$$

$$V_{sd} = V_{s1} + V_{s2}\cos(2\omega t)$$
$$V_{sq} = -V_{s2}\sin(2\omega t) \tag{4-5}$$

As the grid voltage is expressed in the synchronous rotating frame, (4-5), a zero sequence component is not observed by the inverter control. In steady-state, I_d and I_q will be equal to their reference set points established by the PI controllers and will be DC values. Consequently, the derivatives in (4-3) are equal to zero in steady-state. By substituting (4-5) into (4-3), the steady-state, inverter terminal voltages for the *d*-axis and *q*-axis can be expressed by (4-6). An interesting finding to note is that if an inverse Park transformation was applied to the AC terms in (4-6) ($V_{s2}\cos(2\omega t)$ in V_{td} and $-V_{s2}\sin(2\omega t)$ in V_{tq}), the negative sequence component of the grid voltage will be obtained.

$$V_{td} = -L\omega I_q + RI_d + V_{s1} + V_{s2}\cos(2\omega t)$$
$$V_{tq} = L\omega I_d + RI_q - V_{s2}\sin(2\omega t) \tag{4-6}$$

Performing an inverse Park transformation on (4-6) and then applying the Fortescue transformation, one will obtain (4-7), which represents the symmetrical component terminal voltages for the inverter. Graphically, the sequence components of the average model of a voltage sourced inverter with its *RL* filter operating at its fundamental frequency can be modeled by the sequence networks shown in figure 27. In figure 27, $V_1 = V_{s1}$, $V_2 = V_{s2}$, and $V_0 = V_{s0}$.

$$V_{t2} = V_{s2}$$
$$V_{t1} = -L\omega I_q + RI_d + V_{s1} + j(L\omega I_d + RI_q) \tag{4-7}$$
$$V_{t0} = 0$$

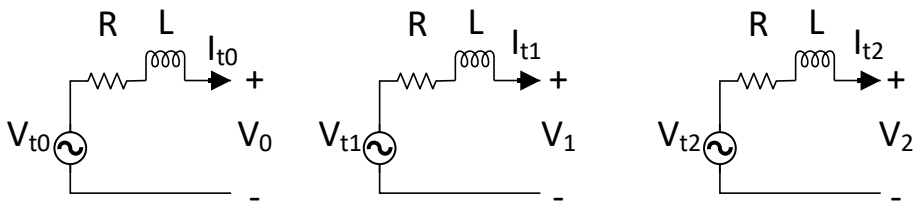


Figure 27: General Sequence Network of a Grid tied current controlled inverter

Based upon (4-7), the zero sequence voltage associated with the zero sequence network of figure 27 is short circuited. In (4-7), the conditions also show that $V_{t2} = V_{s2}$. Therefore, no current will flow in the negative sequence network and V_{t2} can be treated as an open circuit. Equation (4-3) is typically used to regulate I_d and I_q. These current values will influence V_{t1} in (4-7), which will drive the positive sequence output current flow, I_{t1}, through the *RL* filter. With these constraints the final sequence network for a SLGF scenario that accounts for inverter current control is found in the right of figure 26.

The critical difference between the new and classical model is the *RL* filter placed in parallel with R_v in the zero sequence network. This adjustment accounts for the inverter supplying zero sequence current through the *RL* filter resulting in imbalances in the output current of the inverter. Finally, the proposed model will predict a higher fault current compared to the classical model. The parallel impedance, seen in red in figure 26, will reduce the equivalent impedance, therefore increasing the system fault current.

4.3 SIMULATION RESULTS

To validate the new sequence network model accounting for inverter current control, a PLECS simulation of a current controlled grid tied inverter was developed. The system in figure 1 was simulated with the following parameters: L = 100μH, R = 1.63mΩ, V_{DC} = 1250V, and R_v = 0.05Ω. The source line-to-line peak voltage and frequency are 480V and 377rad/s, respectively. Each PI compensator for the *d*-axis and *q*-axis were designed to have a proportional gain value of 0.05 and integral gain value of 0.815. The inverter is controlled to reach current references of $I_{d,ref}$ = 3kA and $I_{q,ref}$ = 0 A, [3]. A single line-to-ground fault is located on Phase *A* and modeled by a fault impedance, R_f, of 0.0163mΩ connected to the ground. A wye-connected resistive load of 10kΩ per phase is used. The system power base is set to 1.7 MVA and the voltage base is set to 277 V.

Table 2 provides the computed numerical per unit values for the sequence voltages across the load and the fault current. Comparisons are made between the analytical calculation of the classical sequence network modeling approach (figure 26) using (4-8), the proposed model taking into account the inverter's current control using (4-9), and the simulation of the system at steady-state. Table 2 shows that the proposed inverter model for computing the expected fault current has stronger agreement with the simulation result compared to the classical approach. The proposed model is able to predict a difference in magnitude between the negative (V_2) and zero (V_0) sequence load voltage.

Table 2. Comparison of Classical Sequence Model, Proposed Model, and Simulation Results

Parameter	Classical System Modeling	Proposed Model	Simulation Result
V_0	0.51	0.38	0.38
V_1	1.03	0.92	0.92
V_2	0.51	0.64	0.64
$3I_1$	4.17	5.18	5.19
I_{t0}	0	1.36	1.35

$$I_f = 3I_1 = \frac{R_v I e^{j\emptyset} + V}{R_v + R_f}$$

$$V_0 = V_2 = R_v I_1 \tag{4-8}$$

$$V_1 = 3I_1 R_f - 2R_v I_1$$

$$I_f = 3I_1 = 3\left(\frac{R_v I e^{j\emptyset} + V}{2R_v + R_v//(R + j\omega L) + 3R_f}\right)$$

$$V_2 = R_v I_1 \tag{4-9}$$

$$V_0 = R_v//(R + j\omega L) I_1$$

$$V_1 = 3I_1 R_f - R_v I_1 - R_v//(R + j\omega L) I_1$$

Figure 28 shows that the inverter's output current is no longer balanced. A sequence analysis of this current reveals that a positive and a zero sequence component is found within the signal. Therefore, the zero sequence current is responsible for the inverter's output current asymmetry.

The zero sequence component of the inverter's output current can be predicted by computing the current entering through the *RL* filter in the proposed zero sequence network model of Fig. 2. The result of this calculation is listed as I_{t0} in Table I and matches well with the simulation result shown in figure 29.

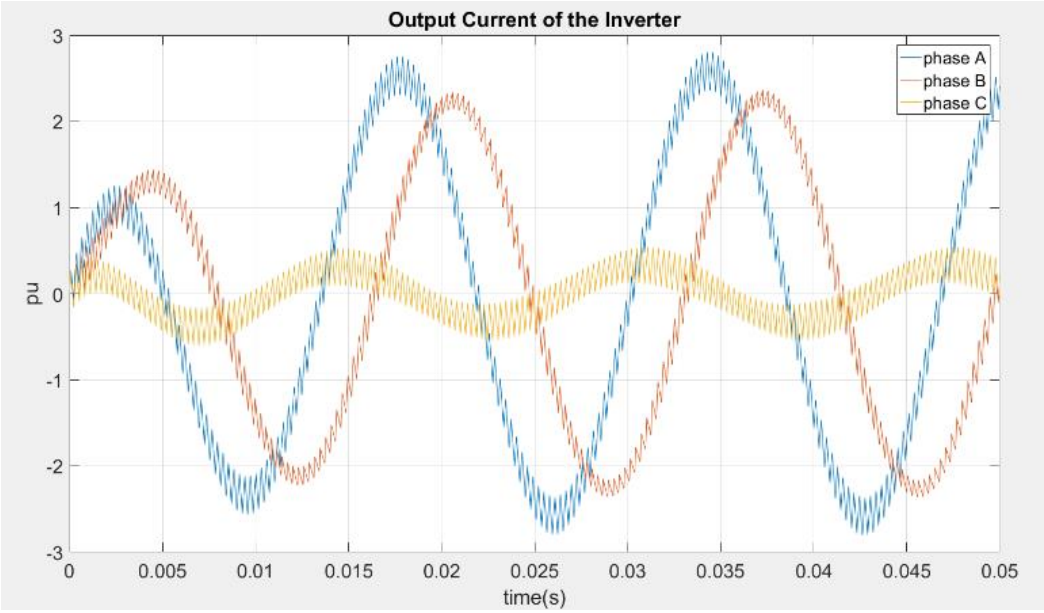


Figure 28:Simulation of inverter current under a SLGF.

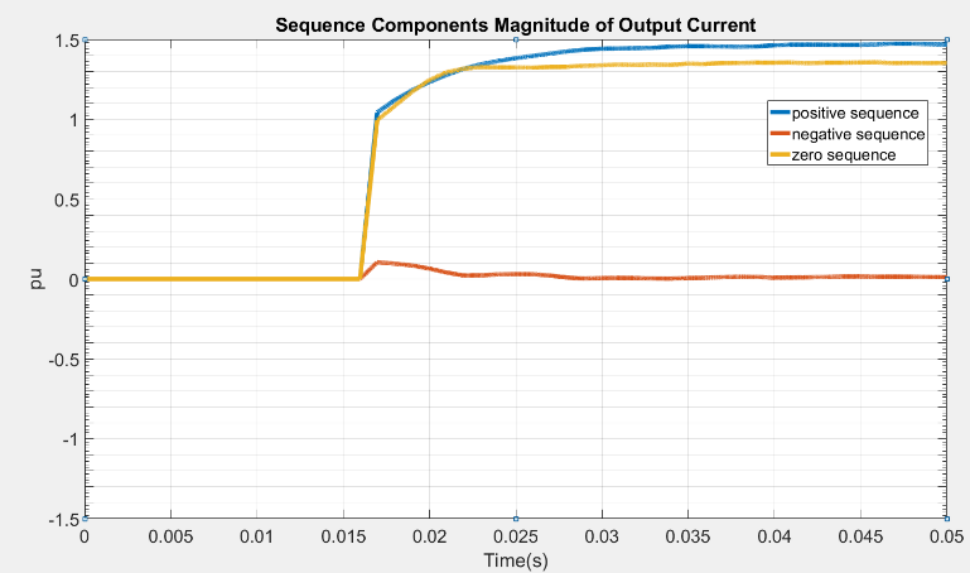


Figure 29:Sequence analysis of inverter current under a SLGF.

5.0 CONCLUSION

5.1 CONTRIBUTION

Working group committee reports for modeling power electronic system impacts on the grid often state the limitation of not knowing the control architecture for a vendor's product. However, this work is still able to provide some insight into the controller's impact on fault current contribution by an inverter by utilizing a commonly used current control architecture for low power and high power, power electronic systems.

A SLGF symmetrical component model of a grid-tied current control inverter without an interconnecting transformer has been discussed and has shown to predict fault current magnitudes accurately. The comparison of the PLECS simulation inverter model with the mathematical analytics from the classical fault network approach and proposed model demonstrates that the inverter can be assumed to provide balanced three-phase currents only under normal grid voltage conditions. Under unbalanced grid supply to the inverter, a *dq* current controlled inverter cannot be assumed to only produce positive sequence current but, has been shown, that the zero sequence component impacts the inverter's output current symmetry.

5.2 FUTURE WORK

The model presented has shown the impact of a single line-to-ground fault on the behavior of a Grid-Tied Current Controlled Inverter only considering the layer of current control but not the layer of active and reactive power control. In fact, the fault event is subject to have an impact on the reference of current that depends on the expression of the grid voltage in dq-frame. A similar analysis, as the one realized in this work, might extend the accuracy of the sequence network model provided in this report.

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