ON GRID CONVERTER RELIABILITY: PRESERVING THE LIFE OF POWER ELECTRONICS THROUGH ACTIVE THERMAL BOUNDARY CONTROL

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University of Pittsburgh, 2018

This dissertation proposes a method of preserving the lifetime of power electronic conversion systems through apt control design. Leading up to the inception of the contribution herein, this work involved exploring the impacts of advanced grid converter capabilities and control methods upon semiconductor device reliability. As distributed generation and loads are increasingly interfaced with the electric grid through power electronics, adverse challenges arise including voltage and frequency instability due to a reduction in system inertia. Said challenges incentivize various advanced grid converter features such as dynamic reactive compensation for grid voltage support, but such features can threaten to quicken the pace of device degradation, decreasing converter lifetime.

The reliability of power electronic conversion systems is correlated to the thermal stress experienced by the semiconductor device materials. The longevity of the device diminishes with high amplitudes of junction temperature fluctuations experienced by the device. This work introduces a control method designed to preserve converter life by minimizing thermal cycling amplitudes, particularly preventing the cooling of device materials when grid interactions would have situationally allowed cooling.

The solution is based upon natural switching surface (NSS) control, previously applied in the literature to the dual active bridge for efficiency gains. Utilizing NSS control for the purpose of actively controlling thermal cycling behavior lays the foundational contribution of the work. In contrast to conventional pulse-width modulation strategies, this approach bears unique merit for the management of thermal behavior because of the unique ability to control the switching trajectories according to desired switching and conduction losses. With appropriate design measures this methodology is also applicable to various converter topologies.

This dissertation initially provides groundwork for the reliability of power electronics. Extensive case studies of electro-thermal performance assessments are presented for both reactive compensation and virtual synchronous machine control, evaluating the impacts of such advanced grid converter features upon device reliability. Theoretical foundation as well as an application case study are provided for natural switching surface control. The contributed work includes the development of active thermal boundary control for the dual active bridge operating under interval loading.

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P. T. Lewis

1.0 INTRODUCTION

By 2030, as much as 80% of all U.S. electric power is predicted to be processed through power electronics between generation and consumption [1]. As of 2005, this statistic was approximately 30% of processed power in contrast to 80% [1]. Along with increased amounts of power electronics interfaced loads, a significant driver of this trend is the increasing adoption of renewable energy resources, particularly solar and wind power, for both environmental and economical motivations. Figure 1 provides a bar graph of the economic progress and goals associated with the DOE SunShot program arranged into residential, commercial, and utility subdivisions. Achieving three cents per kilowatt-hour would make utility scale solar power to be one of the least expensive sources of electricity generation, less expensive than most fossil-fueled generation [2]. This affordability will be one significant catalyst of the growing trend of power-electronics interfacing with the electric grid, moving beyond the 80% statistic in years and decades to come.

With this proliferation of power electronics, reliability becomes an increasingly important concern. How long would one expect the power electronics to last? Lifetime expectancy for power electronic systems vary per the application. For a few examples of such applications, Table 1 provides typical lifetime expectancies associated with each. The next question: what is the most critical factor that decreases the reliability of power electronic systems? On a component level, the power electronic device is the source of most frequent failures with electrolytic capacitors as a second. What are the more influential factors that decrease the lifetime of the device? Table 2 provides a form of an answer with a focus points matrix, presenting the factors that most critically impact the reliability of power electronic devices [3]. Additionally, a survey was performed among industry experts as to what was the critical reliability stressor for power electronic systems,

resulting with thermal cycling and magnitudes on the junction of a device as being the most critical as depicted in Figure 2 [4].

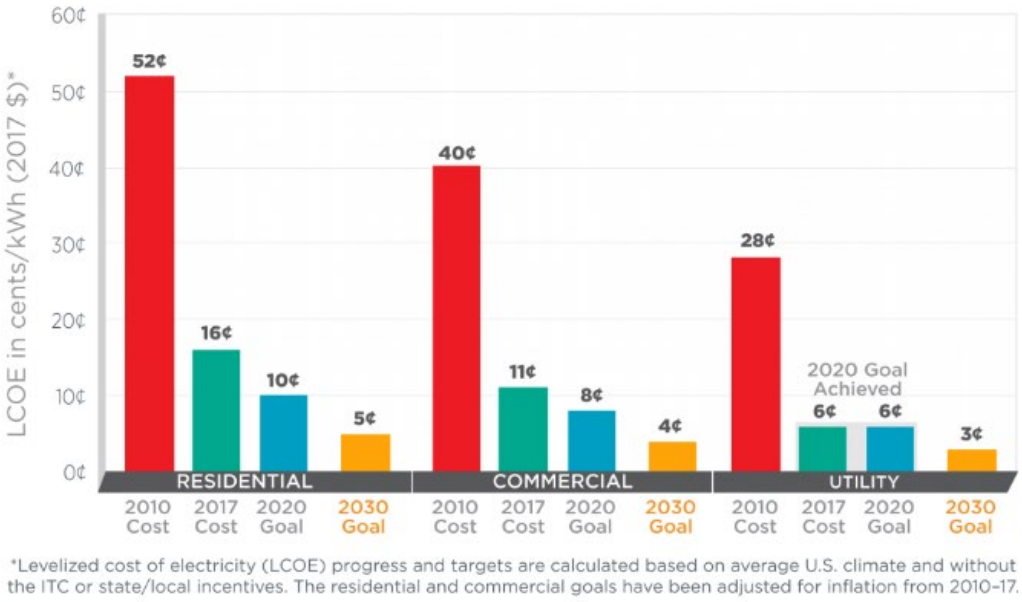


Figure 1: Economic Progress and Goals for the DOE SunShot Program [2]

Table 1: Typical Lifetime Targets for Various Power Electronics Applications [3]

Applications	**Typical design target of lifetime**
Aircraft	24 years (100,000 hours flight operation)
Automotive	15 years (10,000 operating hours, 300,000 km)
Industry motor drives	5–20 years (60,000 hours in at full load)
Railway	20–30 years (73,000–110,000 hours)
Wind turbines	20 years (120,000 hours)
Photovoltaic plants	30 years (90,000–130,000 hours)

Table 2: Focus Points Matrix for Reliability of Power Electronic Components

Load			**Focus points**									
Climate + Design ⇒ Stressor			**Active power components**			**Passive power components**		**Control circuitry, IC, PCB, connectors…**				
Ambient	**Product design**	**Stressors**	**Die**	**LASJ**	**Wire-bond**	**Cap.**	**Ind.**	**Solder joint**	**MLCC**	**IC**	**PCB**	**Connectors**
Relative humidity – $RH(t)$	– Thermal system	Temperature swing ΔT	**X**	**X**	**X**			**X**				
	– Operation point	Average temperature T	X	X	X	**X**		X	X	x	x	x
Temperature – $T(t)$	– ON/OFF	dT/dt	x	x	x	x						
	– Power $P(t)$	Water								**X**	**X**	x
		Relative humidity	x	x	x	X	x	x	x	**X**	**X**	x
Pollution	Tightness	Pollution						x			x	
Mains	Circuit	Voltage	x	x	x	**X**	X		x	x	x	x
Cosmic	Circuit	Voltage	x									
Mounting	Mechanical	Chock/vibration	x			x	x	x	x			x

LASJ – large area solder joint, MLCC – multi-layer ceramic capacitor, IC – integrated circuit, PCB – printed circuit board, Cap. – capacitor, Ind. – inductor, level of importance (from high to low): **X**–**X**–X–x.

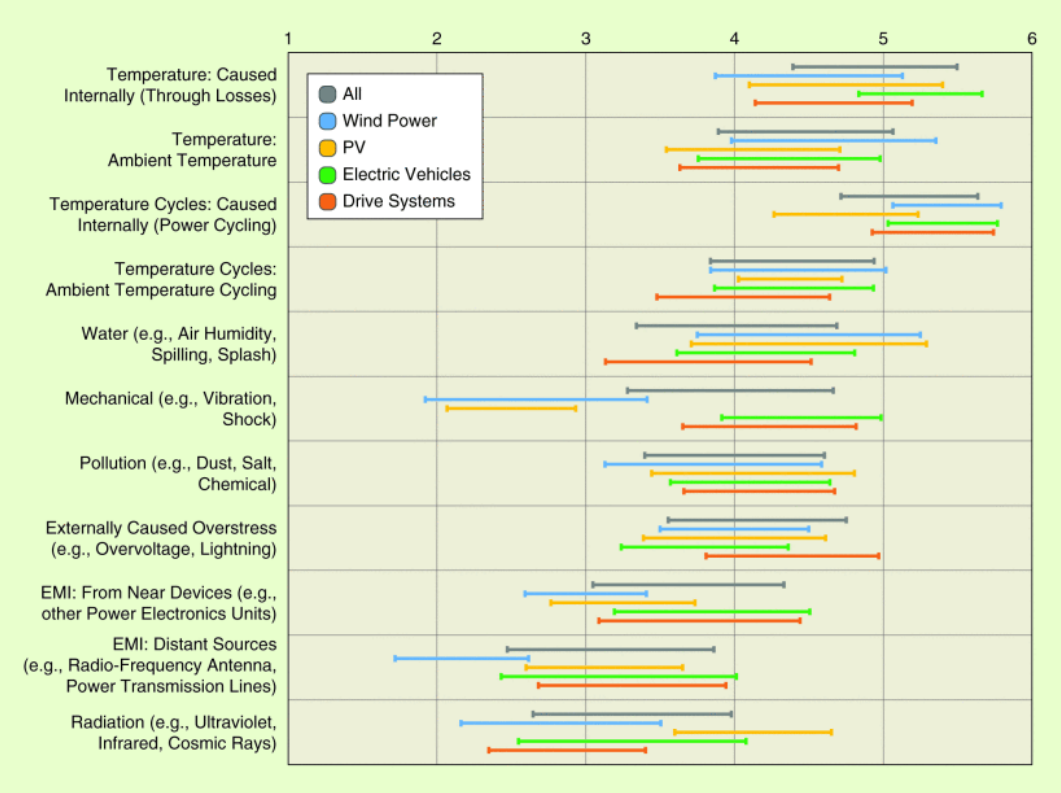


Figure 2: Critical reliability stressors for power electronic systems by application, an industry perception

With the evolution of the electric grid, the increase of converter-interfaced distributed generation (DG) results in grid voltage and frequency instability due to a reduction of inertia or system strength conventionally safeguarded by radially connected synchronous machines (SM) generation. This can be especially apparent for islanded microgrids. Resulting voltage instability can be addressed by reactive compensation as a grid support feature for smart inverters but not without added device degradation reducing system reliability [5]–[7]. Resulting frequency instability and the lack of desired SM inertial dynamics can be resolved by an increasingly popular solution, virtual synchronous machine (VSM) control also known as the synchronverter [8]–[10]. As distributed generation increases and as power electronics conversion technologies functionally advance in response to the challenges associated with increased penetration of power electronics power processing on the grid, advanced grid converter features threaten to quicken the pace of device degradation. Understanding and mitigating any negative impacts of such advanced grid converter solutions upon device lifetime is the purpose of this work.

The reliability of power electronic conversion systems is primarily correlated to the thermal stress experienced by the semiconductor device materials [11], [12]. Lifetime, the longevity of the power electronic semiconductor device, diminishes with high averages and more emphatically high amplitudes of device junction temperature thermal cycling dynamics experienced by the device [13]. For proper assessment of power electronic device reliability, electro-thermal semiconductor device models are created. Since wide bandgap materials are of particular interest in the power electronics community, reliability assessments include the comparison of conventional Si IGBT transistor and SiC power MOSFET models, based upon datasheets from the manufacturer for specific devices. All work is performed utilizing ANSYS Simplorer. Notably a reduction of thermal cycle amplitude preserves device reliability, and counter-intuitively this

reduction can be achieved by preventing junction temperatures from dropping to cooler temperatures.

The contribution proposed in this work is principally inspired by a control methodology previously applied to the dual active bridge, among others, based upon natural switching surfaces (NSS) applied for efficiency gain. Forms of NSS control are also known as boundary or trajectory control in the literature. Additionally, this work is inspired by the various active thermal control (ATC) methods that have been introduced in the literature. Utilizing NSS methodology for the purpose of actively controlling thermal cycling behavior lays the foundation of the proposed research. This approach bears unique merit for management of thermal behavior through designed electrical boundaries placed upon natural switching surfaces, influencing the thermal dynamics for lifetime preservation even while implementing advanced grid converter performance capability. The resulting method is autonomous, natural switching control with boundaries designed to accommodate improved device reliability.

First, this work provides a power electronic device reliability assessment utilizing electro-thermal semiconductor device models for the enlightenment of the benefits of an interdisciplinary design perspective. Secondly and of primary contribution, this work proposes a means of device lifetime preservation leveraging natural switching surface control methodology as a means of active thermal control.

1.1 OBJECTIVE

The objective of this work is to propose a method of converter control that actively mitigates decreased device lifetime that is related to adverse thermal performance. The methodology preferably would be applicable to various converter topologies.

More specifically, this work is dual-purposed in objective, 1) to enlighten electric power engineers with a more interdisciplinary perspective of power electronic converter system design accounting for electro-thermal behavior with regards to device reliability and 2) to provide a control methodology that minimizes the negative impacts of thermal behavior even while maintaining advanced converter performance benefits desired. Inherent to such an objective is a trade-off to be taken into account between reliability and performance.

1.2 ORGANIZATION

This proposal is organized in order that any content can be placed into three primary categories: literature review, preliminary work, and proposed solution. Section 2 addresses a background literature review, concerning grid converter electrical performance features and the relationship between thermal performance and device reliability. Also addressed is the electro-thermal semiconductor device modeling necessary in order to observe impacts upon thermal performance. Sections 3 covers the preliminary work pertaining to the control features of distributed generation inverters including reactive compensation and virtual synchronous machine supporting grid voltage and frequency stability, respectively. Section 4 provides the theoretical background of natural switching surface control applied to the dual active bridge as well as a specific case study

design for efficient performance. Section 5 introduces the utilization of boundary or natural switching surface control to contribute a form of active thermal control for interval-based loads. The same control approach is proposed for future work to be developed for the distributed generation inverter accommodating the reliability cost of reactive compensation as a grid support feature. Section 6 concludes the work with a summary, suggested future research directions, and possible applications.

2.0 BACKGROUND ON DEVICE RELIABILITY AND MODELING

This background section provides the space for setting the scene, for primarily power electronic device reliability, but also for the electro-thermal semiconductor device modeling necessary for the validation of the proposed contribution. Device reliability requires an extensive background due to the proposed contribution being related to an improvement in such area. An appropriate understanding of device reliability is needed for a grasp of what is being proposed, as well as for a grasp of what is not being proposed. Integrally, background is given on the topic of active thermal control and how it can enable the preservation of power electronics reliability. The background and modeling details of electro-thermal device models are also provided, including model validation according to manufacturer datasheets for specific IGBT and MOSFET devices. The two advanced DG inverter functionalities explored in this work are dynamic reactive compensation and virtual synchronous machine control, supporting grid voltage and frequency instability, respectively. Background for each function is provided in their respective sections, 4 and 5. Lastly, the origin story of natural switching surface control in application to the dual active bridge is given coverage here, being the inspiration for the primary contribution of this work. Within the literature, this control methodology has existed outside the realm of active thermal control, until now.

2.1 ON POWER ELECTRONICS RELIABILITY

Reliability for this work will be defined as “maintaining the characteristics relevant to operation over a defined period of time [14],” typically measured in terms of probability of survival or failure rate. The essence of reliability engineering in this sense is to preserve life or prevent failure.

Reliability of a semiconductor device can correspondingly be defined as maintaining switched conduction for the expected lifetime of the device, and power electronics reliability engineering as preservation of the life of the component. Of power electronics more generally, the reliability of conversion systems are predominantly threatened by power semiconductor devices (e.g. Si and SiC IGBTs and MOSFETs, and GaN devices), but also by capacitors, connections, and fans [3]. This work addresses the reliability of power devices as they are a severe threat to converter system reliability on their own. All other said reliability vulnerabilities are outside the scope of this work.

Electronic reliability engineering has existed as a discipline in its own right since the early 1950s, with its origins in military electronics during World War II when the electronic tube was the most unreliable component in electronic systems [15]. This backdrop is the start of U. S. military handbooks on electronic reliability engineering. Such were the origins of the popularly utilized MIL-HDBK-217F titled "Reliability Prediction of Electronic Equipment" [16]. That said, the topic of electronic reliability engineering has come short of an exact science over the last seven decades. The cover page of this widely used handbook states its purpose to be guidance only and not to be cited as a requirement. The approach is that of documenting observed device failure data. This guide and many like it have been incredibly helpful, but they especially have limitations as power electronics technology advances and grid interconnection applications become more widespread. Additionally, advanced approaches seek to design for reliability proactively as much as possible. A paradigmatic shift exists nowadays towards a physics-of-failure approach for power electronics reliability engineering [3], [13]. This approach is being pioneered by prominent names in the power electronics engineering community, the likes of Dr. Huai Wang, Dr. Marco Liserre, Dr. Frede Blaabjerg, and Dr. Ke Ma among others. The physics-of-failure perspective takes a multi-disciplinary design for reliability (DFR) approach.

The broad and multi-disciplinary scope of power electronics research is effectively portrayed with the diagram in Figure 3 [13]. According to William E. Newell in 1974, the scope of power electronics research is subdivided into three primary disciplines of electrical engineering, the categories of power, electronics, and control as in Figure 3 (a) [17]. According to [13], the future trends of power electronics reliability can similarly be subdivided into primary disciplines of control and monitoring, design and verification, and analytical physics as seen in Figure 3 (b).

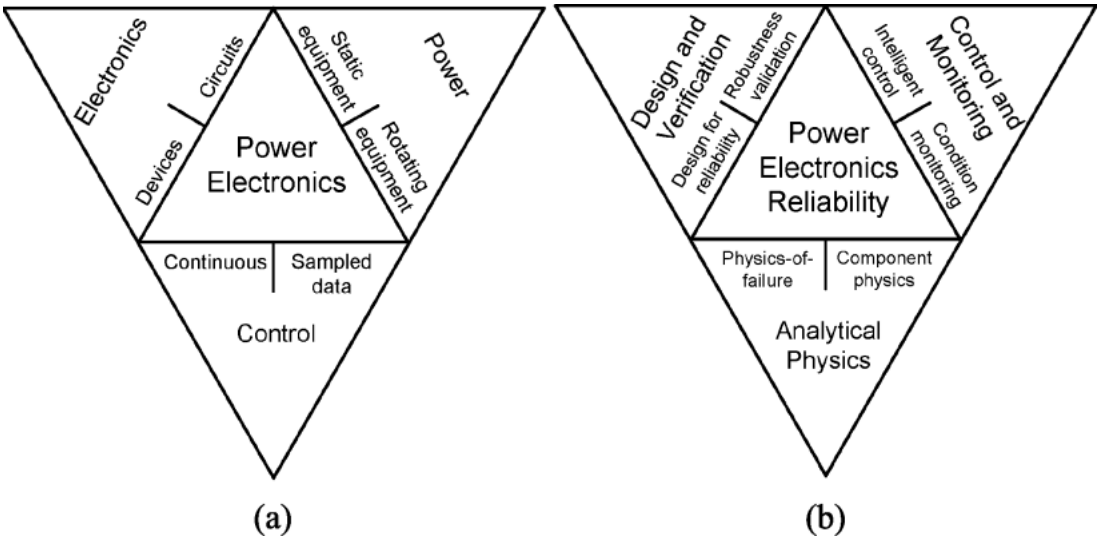


Figure 3: Defining the scope of (a) power electronics research according to William E. Newell in 1974 [17] and (b) power electronics reliability research trends today [13]

Where does this proposed research fall within the future disciplinary trends of power electronics reliability research? Within this multi-faceted topic, the contribution is primarily an intelligent control design, ensuring reliable field operation of grid converters from the start through means of control methodology. Secondarily, the contribution is an example of designing for reliability, building reliable operational dynamics into the design. Lastly, the proposed work is

founded upon a physics-of-failure approach since previous research literature addressing how and why devices fail is the enlightenment of the controller contribution.

The relationship between device junction temperatures and device reliability is linked to the mechanical component physics. When the heterogeneous materials that make up a device module heat up and cool down at varying speeds, the life of the device diminishes. The reliability of a device is primarily correlated to this type of thermal stress experienced by the device module [11], [12]. The longevity of the functional life diminishes with high averages and more notably high amplitudes of device junction temperature fluctuations experienced by the device [13]. One rise and fall of temperature fluctuation on the junction of a power semiconductor device is known as one thermal cycle. Device failure ultimately results from stressed physical contacts between materials of differing thermal expansion coefficients, finally degrading into a crack at the maximum amount of thermal stress cycles that the contact could withstand.

For an insulated gate bipolar junction transistor (IGBT) module, the material contacts relevant to reliability vulnerability include cracking of baseplate solder joints or chip solder joints and the lifting of wire bonds. A structural diagram of an IGBT is provided in Figure 4 with vulnerable points of contact highlighted in red. A helpful metaphor to conceptually grasp the physical cause of device failure is the repeated bending of a piece of metal wire. The wire will eventually snap from the cyclical bending. Cyclical temperature fluctuations on junctions of the power electronic device similarly result in device failure. Material junctions shifting on the order of 5 to 50 μm is enough to cause such a failure [14]. For an example, a magnified picture of an actual failed IGBT caused by bond wire lifting and cracking is depicted in Figure 5. Note that power MOSFETs, whether they are based off of conventional Si or wide bandgap GaN materials, do not have bond wires due to having body diodes instead of anti-parallel diodes like IGBTs.

Nonetheless, reliability is an issue specifically with regards to cracking of baseplate solder joints or chip solder joints.

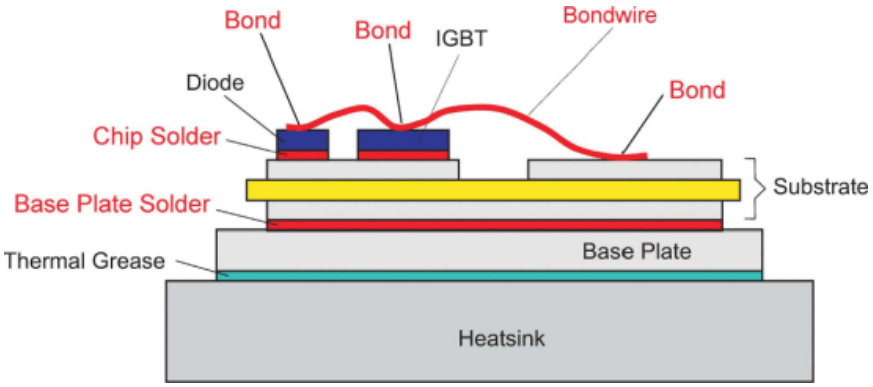


Figure 4: Cross section of an IGBT module with highlighted physical points of contact relevant to device lifetime [14]

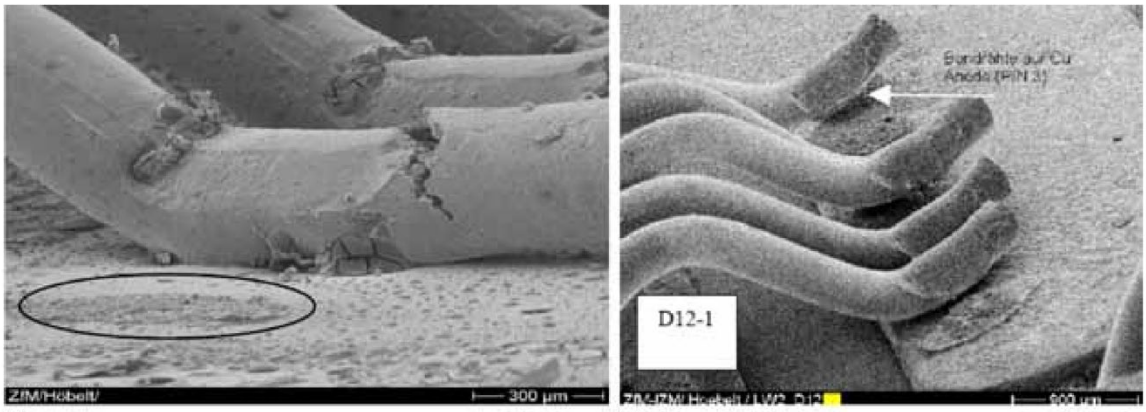


Figure 5: IGBT bond wire damage: (a) cracking and lift-off (b) bond wire lift-off [14]

An established mathematical approximation of power electronic device reliability, based upon thermal cycling, is the Coffin-Manson-based lifetime estimation model [11], [13], [18], [19].

Derived in [20], the remaining number of thermal cycles until device failure (N) can be calculated according to (1).

$$N = C\left(\Delta T_j - \Delta T_{j,0}\right)^{-n} \quad (1)$$

Where N is the number of cycles to failure and ΔT_j is the range of temperature in the thermal cycle while C and n are constants determined empirically through simulation or experiment. The $\Delta T_{j,0}$ is a thermal stress forgiveness region within which elasticity of material allows for a small amount of thermal cycling without causing added stress. When $\Delta T_{j,0}$ is negligible in contrast to ΔT_j, it can be dropped, resulting with the Coffin-Manson model of lifetime estimation, equation (2).

$$N = C\left(\Delta T_j\right)^{-n} \quad (2)$$

One more model that builds upon the work of Coffin and Manson is the Arrhenius life stress model, also known as the Arrhenius relationship. This relationship is likely the most commonly used life-stress relationships for accelerated life testing. My work is not geared towards accelerated life testing but simply to minimize the critical accelerators. Nonetheless, speaking of reliability would be incomplete without speaking of this relationship. It is derived from the Arrhenius equation, a reaction rate. In application to reliability of power electronics, the Arrhenius relationship is used to modify the Coffin-Manson model, resulting in the Coffin-Manson-Arrhenius model (3) [21].

$$N = D(\Delta T_j)^{-m}\left(e^{\frac{E_a}{k_B T_{j,m}}}\right) \quad (3)$$

Where k_B is the Boltzmann constant, E_a is the activation energy, and $T_{j,m}$ is the mean device temperature, while D and m are constants determined empirically. One can see that the average junction temperature is now incorporated into the Coffin-Manson, with added accuracy. Nevertheless, the Coffin-Manson is a foundational relationship because the thermal cycles are the dominant factor in the relationship between junction temperature and acceleration of degradation. That is as long as the magnitudes of the device are within rated thresholds provided within a datasheet.

An example of these estimated cycles to failure calculations for an IGBT is depicted in Figure 6 with respect to both thermal cycling amplitude and mean temperature. The relationship between thermal cycling amplitude (ΔT_j) and mean junction temperature ($T_{j,m}$) is defined in equation (4).

$$\Delta T_j = T_{j,m} - T_j \quad (4)$$

Where T_j represents the measured junction temperature in real time or the estimated junction temperature for given reliability engineering solutions. Beyond using the Coffin-Manson model

or even the Coffin-Manson-Arrhenius model, Miner's Rule is also a cumulative damage rule used for estimating device lifetime, provided in (5).

$$C = \sum_i \frac{n_i}{N_i} \tag{5}$$

Where C is the cumulative damage, n_i is the number of cycles within stress range, and N_i the number of cycles to failure in ith stress range [21]. Miner's Rule might be utilized for future validation of proposed research as is fitting.

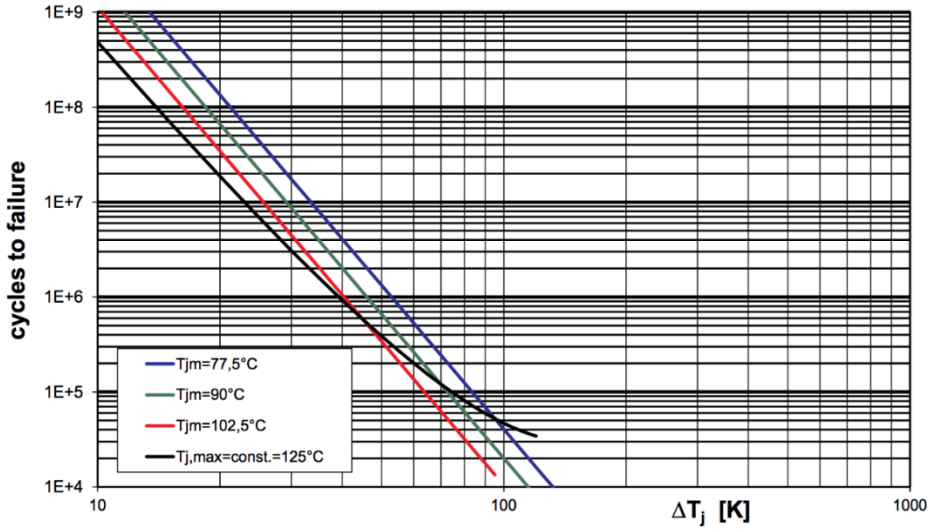


Figure 6: Power cycling lifetime in relation to cycling amplitude and mean temperature for an IGBT module [14]

Note that some power electronics reliability research performs statistical analysis as in mission profiling or rainflow-counting analysis seeking to better predict the lifetime of the converter system by accelerated stress methods. This proposed work is not concerned with attempts to develop better estimations of device lifetime through statistical analysis. This work is interested in the lifetime prediction relationships described only for the purpose of recognizing the desired objective of reducing thermal cycling for lifetime preservation. Instead of predictions of lifetime, this work is involved with active reduction of junction temperature magnitudes and cycle amplitudes, as a form of what is coined as active thermal control (ATC) in the literature [22].

Numerous works have proposed various forms of ATC to improve converter reliability, utilizing various thermally-oriented control strategies, gate driver modification, and modulation methods as forms of ATC [21], [23]–[25]. Discontinuous pulse-width modulation, a well-known strategy for controlling device loading, reduces the amount of experienced losses and consequently temperatures due to intervals of discrete voltage output reducing switching actions [24], [26]. Active gate driver control provides the possibility of influencing both conduction and switching losses without hindering device functionality [27]. Additionally, a reduction of junction temperature variation can be achieved through proper switching frequency (f_{sw}) variation per operating condition [21], [22]. The work in [22], takes this latter ATC approach and uniquely varies switching frequency to prevent excessive device cooling during power reductions, and the control design exploiting the switching frequency is informed by power loss estimations. Common among these ATC methods, is that either average or cycling amplitude junction temperature are reduced, and the savings are achieved due to reduced device loss. The device power loss (P_{loss}), consisting of both switching (P_{sw}) and conduction loss (P_{cond}), is generally defined as in (6).

$$P_{loss} = P_{sw} + P_{cond} = \frac{I_{on}V_{off}}{a} f\Delta t_{sw} + I_{on}^2 R_{DS,on} \quad (6)$$

The work presented here is a form of ATC that reduces thermal cycling amplitudes particularly.

Where junction temperature averages and thermal cycling amplitudes can be minimized, device reliability is improved. Notably thermal cycle amplitude minimization, even if causing the devices to experience added loss and stay at higher temperatures, consequently extends device lifetime. This is consistent with the Coffin-Manson model and related estimations seen in equations (1) through (3). This form of active thermal control is a proven method of extending the lifetime of power electronic devices by limiting how far the devices cool down, effectively reducing the thermal cycling on the junction of a semiconductor device, ΔT_j.

With all of this background, the narrowed scope of this work is related to the development of an active thermal control methodology, a form of intelligent control as seen in Figure 3 (b) within the larger scope of power electronics reliability. In order to validate the benefit of such a methodology, a means of assessing thermal cycling behavior is necessary. Electro-thermal semiconductor device modeling enters the scene, a physics-of-failure approach incorporating device physics into grid converter simulations for proper assessment of reliability engineering.

2.2 ON ELECTRO-THERMAL SEMICONDUCTOR DEVICE MODELING

The thermal dynamics of the semiconductor devices are incorporated into CAD simulation by use of a thermal impedance network that is separate from yet coupled to the electrical device circuitry.

The impedance network is made up of parallel combinations of resistive and capacitive impedances, connected in series as shown in Figure 7 for a power MOSFET and for an IGBT with its associated anti-parallel diode. The physical layers of the device that are modeled include the following: device junction to device packaging case ($Z_{th,jc}$), device case to the ambient temperature ($Z_{th,ca}$), for which typical values for a heat sink thermal impedance are utilized in this work. The overall junction to ambient thermal impedance can be calculated as in (7) in units of degrees Celsius per Watt.

$$Z_{th,ja} = \frac{T_j - T_a}{P_{loss}} \ (°C/W) \tag{7}$$

Where T_a is the ambient temperature, T_j is junction temperature, P_{loss} is the total loss, and $Z_{th,ja}$ is the total thermal impedance from junction to ambient. The thermal impedance from heat sink to ambient with intermediary layers of thermal impedance is calculated as shown in (8).

$$Z_{th,ja} = Z_{th,jc} + Z_{th,cs} + Z_{th,sa} \tag{8}$$

Moving forward, the thermal impedance from casing to the heat sink, $Z_{th,cs}$, is lumped into a case to ambient thermal impedance, $Z_{th,ca}$. The junction temperature rises above ambient temperature by the amount of power loss dissipated across the described thermal impedances as in (9).

$$T_j = T_{ambient} + P_{diss}(Z_{th,jc} + Z_{th,ca}) \quad (9)$$

Of the two popularly utilized thermal impedance networks, the Cauer and Foster models, the Foster network is implemented. The Foster network, also known as the partial fraction circuit, combines parallel combinations of thermal impedances that extrapolate manufacturer generated curves of transient thermal impedance. The Cauer network, also known as the continued fraction circuit, combines thermal impedances that specifically reflect the physical layers of the materials. Because material characteristics of the individual layers were not known for all device cases and because transient thermal impedance curves were available in datasheets, the Foster model was utilized.

The four Foster thermal impedances ($C_{\text{th,i-4}}$ and $R_{\text{th,i-4}}$) for each device are mathematical approximations to map each correlating transient thermal impedance curve. The curves represent the thermal impedance between the *p-n* junction and device packaging case over the specified switching pulse time. Network models were created based upon datasheet characteristics, and the resulting thermal impedance values are listed for the SiC power MOSFET in Figure 6 and for the Si IGBT and its associated anti-parallel diode in Figure 7 and Figure 10, respectively. The IGBT and anti-parallel diode have different thermal characteristics and are hence modeled separately while the body diode of the MOSFET has inherently the same thermal characteristic as in Figure 8. For the purpose of validation, Figure 6, Figure 7, and Figure 8 also provide comparisons of the transient thermal impedance curves between the generated device model and its datasheet.

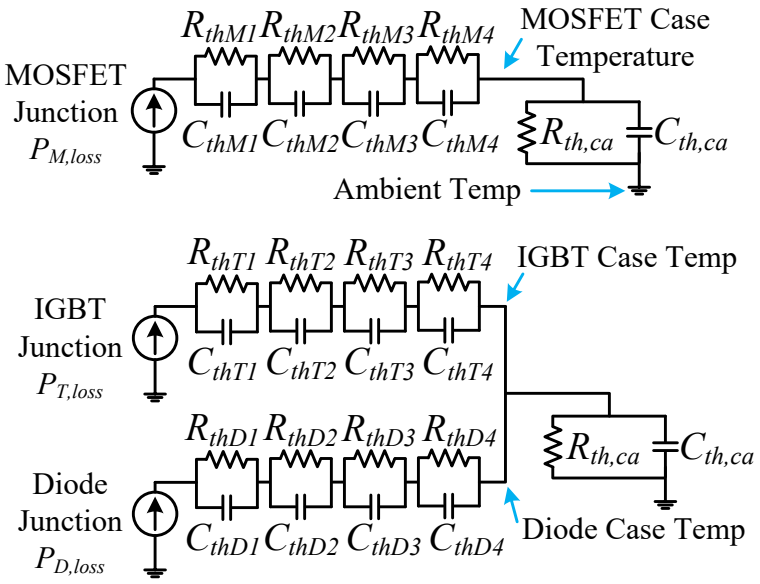
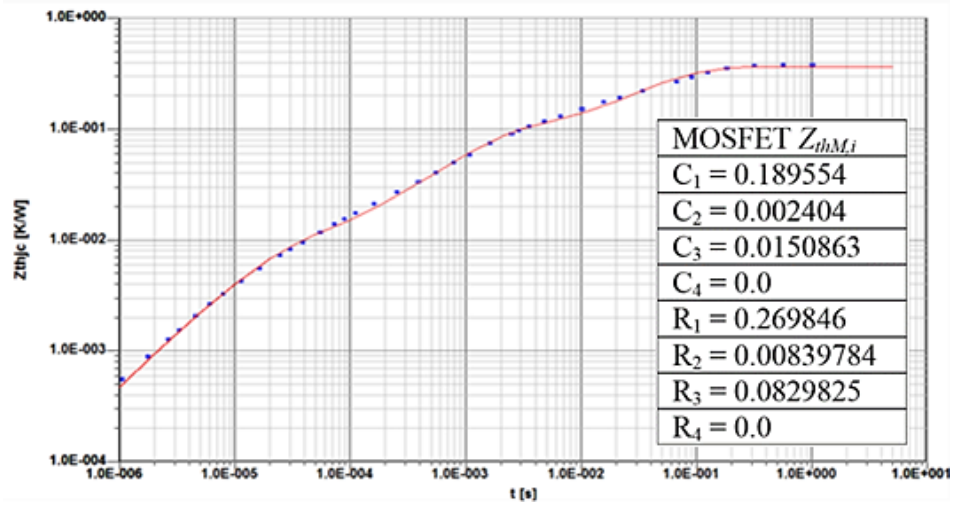


Figure 7: Transient Thermal Impedance Foster Networks



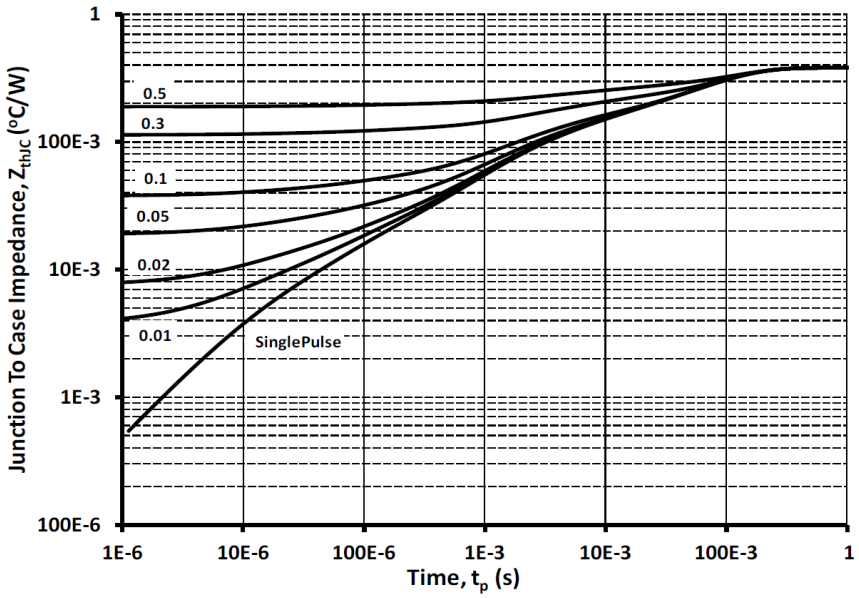
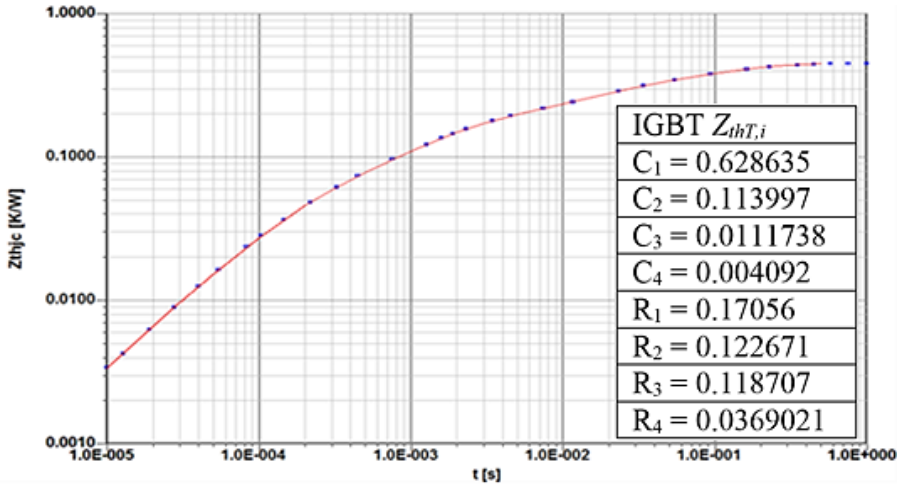


Figure 8: Transient Thermal Impedance Model for the SiC MOSFET. Model (above) and Manufacturer (below)



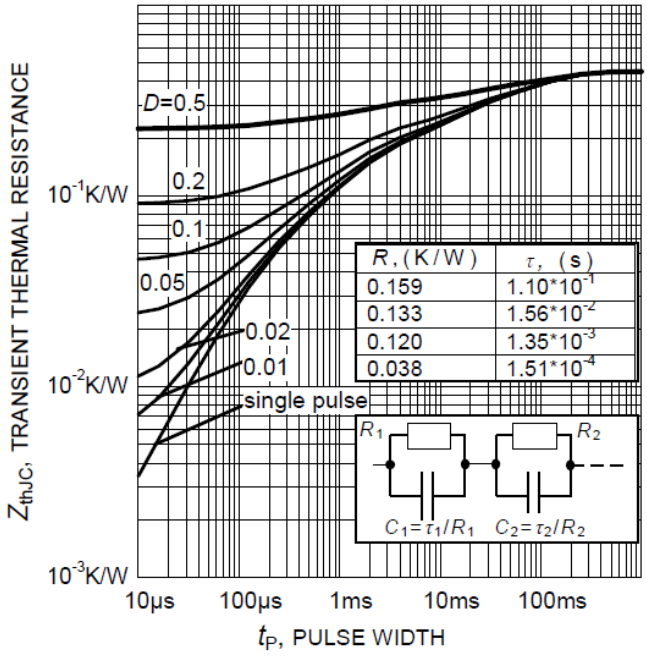


Figure 9: Transient Thermal Impedance Model for Si IGBT. Simulation Model (above) and Manufacturer Measurement (below)

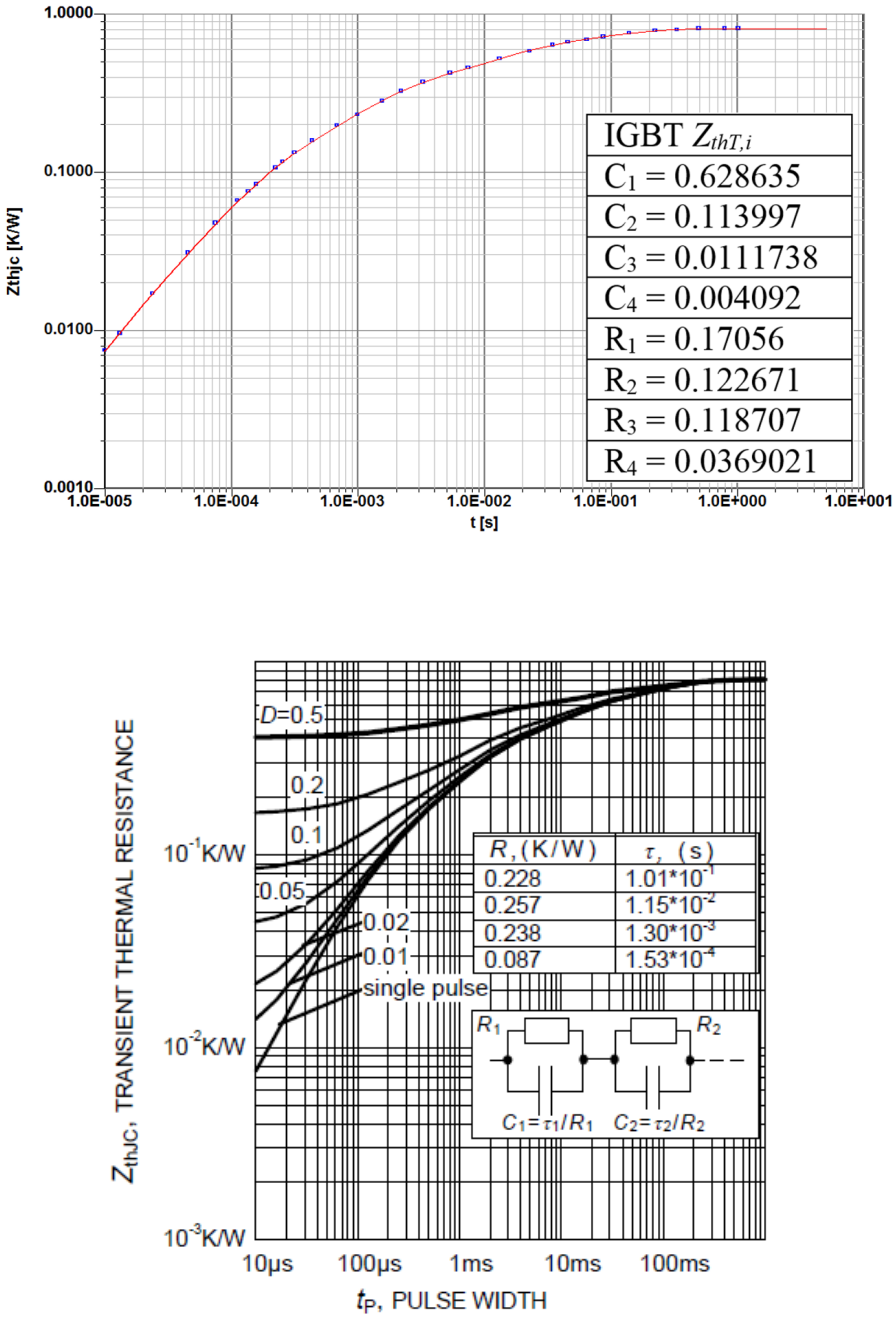


Figure 10: Transient Thermal Impedance Model for Si Anti-parallel Diode. Simulation Model (above) and Manufacturer Measurement (below)

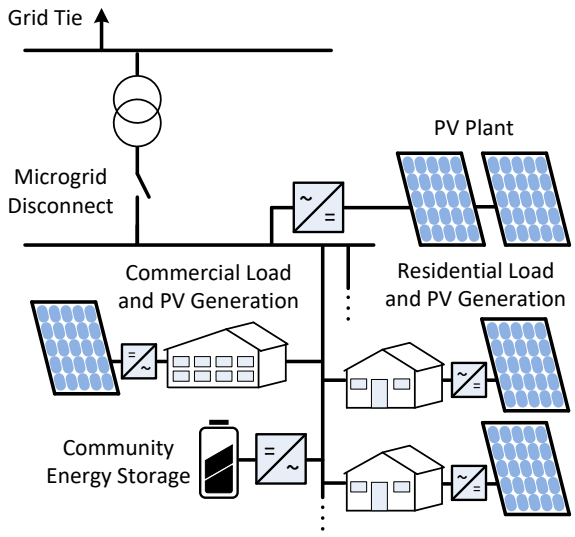
3.0 INVESTIGATING IMPACTS OF ADVANCED INVERTER FEATURES

Included here are two in-depth studies (3.1 and 3.2) of the impacts that two advanced inverter features have upon power electronics systems reliability. These two features are reactive compensation and virtual synchronous machine control, grid support features for voltage and frequency stability, respectively.

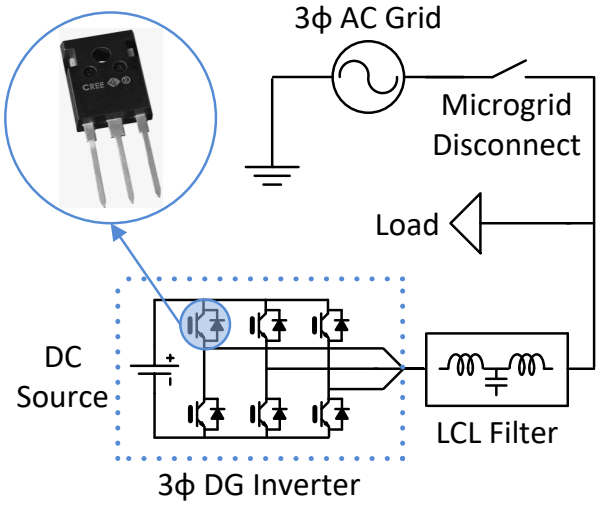
3.1 IMPACT OF REACTIVE COMPENSATION GRID SUPPORT

As advanced functionality is being demanded from distributed generation (DG) systems, smart inverters are being developed to provide reactive compensation to provide system support during grid disturbances. This compensation, however, leads to increased semiconductor device stress in the inverter. This work investigates the electro-thermal impacts of inverter grid support upon the longevity of SiC power MOSFET and Si IGBT products. This work is meant to inform the evolving standard development for smart inverter design.

With increasing distributed generation (DG) on the grid, an expected paradigm shift is the requirement of DG inverters to provide grid support features, notably within microgrid systems, as depicted in Figure 11(a). A voltage sag that is experienced as result of system events, such as a grid fault or microgrid islanding, can be remedied through reactive power compensation. However, by performing reactive compensation with a smart inverter, additional device losses and stresses are created in the semiconductor switches [5], [13], [28], [29]. With this additional capability of voltage source converters (VSCs), there is a foreseen tradeoff: the grid voltage support added by the smart inverter and the reliability of the inverter (devices handling added stress).



(a)



(b)

Figure 11: Example Microgrid System (a) and Modeled System (b)

There is also a need to determine standards for advanced features required of smart inverters. The Electric Power Research Institute (EPRI) began such efforts in 2009 and documented the work "Common Functions for Smart Inverters Version 3," published in February

2014 [30] and updated in December 2016 [31], attempting to provide a common language for the subject of advanced inverter functions. Dynamic reactive current support is one of the discussed functions. Grid codes and evolving standards associated with advanced inverter features include IEEE 1547, CA Rule 21, UL 1741, and IEC 62109. Exploring the reliability of DG converters will help inform evolving requirements while maintaining balance between grid resiliency and converter reliability.

Mechanical reliability of a power electronics system is directly correlated with the thermal stress experienced within the semiconductor devices. This is dictated by increasing mean junction temperature and by junction temperature fluctuations experienced by each power electronic device. When p-n junction temperature magnitudes and fluctuations are minimized, reliability is improved. Numerous works have proposed various methods to improve converter reliability by such minimization utilizing various control strategies and modulation methods [23], [24], [32]. In [6], the optimization of reactive power flow is explored to achieve higher reliability of power converters interfacing doubly fed induction generators.

In this work a SiC power MOSFET and a Si IGBT, the CREE C2M0040120D [33] and the Infineon IKW40T120 [34], are characterized for a microgrid-based inverter system and modeled in ANSYS Simplorer. These models are used for comparison during a grid disconnect, in which the inverter control system must compensate for the voltage dip by injecting reactive current. The resulting temperature excursions experienced by the semiconductors in each inverter are examined, with analysis over a range of real and reactive power levels supplied by the inverter. These results demonstrate the mechanical impact of reactive power compensation on the longevity of power electronic devices in developing smart inverter systems.

This work is organized into the following parts. Section II presents the implementation of smart inverter control capable of the reactive compensation support feature. Section III describes further modeling efforts associated with a switched converter model including device losses. Electro-thermal device characterizations are presented and validated in Section IV. Lastly, Section V gives the results of various case scenarios, followed by observations and conclusions in Section VI.

3.1.1 Smart DG Inverter Control Implementation

This section provides the model and controller implementation of the reactive compensation technique. The examined inverter is a commonly used VSC, two-level, three-phase, DG inverter with controllable reactive power injection. It is connected to the microgrid, as shown in Figure 11(b), via a LCL filter interface at the point of common coupling. The equivalent grid, modeled as an infinite bus, is disconnected from an islanded microgrid by a transfer switch. The system parameters, given in Table 3, are based upon typical values for a residential scale three-phase inverter. The VSC inverter control system performs standard inner current control regulation and outputs *d*-axis and *q*-axis voltage references for pulse width modulation control as seen in (1) and (2) [35]. Figure 12 presents this control structure and how it interfaces with the full system.

$$v_{d-ref} = v_d - \omega L_1 i_q + (K_P + K_I/s)\left(i_d - i_{d-ref}\right) \tag{1}$$

$$v_{q-ref} = v_q + \omega L_1 i_d + (K_P + K_I/s)\left(i_q - i_{q-ref}\right) \tag{2}$$

When injecting reactive current, the reference $i_{\text{q-ref}}$ is altered according to the necessary amount of compensation for voltage recovery. As depicted in Figure 3, the maximum amount of possible reactive power compensation for a given event is limited by the rated capacity of the inverter. By adopting a constant active power strategy, the system achieves ramp rate control as defined in (3) and (4) [28], [36], [37].

$$i_{d-ref} = I_N / v_g \tag{3}$$

$$i_{q-ref} = k(1 - v_g) I_N \tag{4}$$

Here, k is the ramp rate of injection, I_{N} is the rated current of the inverter, $i_{\text{q-ref}}$ is the injected reactive current reference, and v_{g} is the grid voltage measured at the point of connection.

The rate of current injection, k, is solved for from (13) and depicted within Figure 14. The German E.ON Grid Codes requires a minimum compensation of $k = 2$ [36]. The IEEE Standard 1547 is yet to determine such a code of implementation. The grid voltage measurement, calculated as a control input in (5), is the per unitized magnitude of the three phase grid voltages (v_{a}, v_{b}, and v_{c}) after conversion into the *d-q* reference frame.

$$v_g = \sqrt{v_d^2 + v_q^2} \tag{5}$$

Note that all calculations within the control system in Figure 12 are performed in per unit base, and the inverse park transform (with corresponding park transform) utilized in this control for both voltages and currents is provided here for clarity in (6).

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ -\sin(\omega t) & -\sin\left(\omega t - \frac{2\pi}{3}\right) & -\sin\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{6}$$

Table 3: DG Inverter System Parameters for Reactive Compensation Implementation

System Parameter	Value
AC Output Voltage (RMS)	120 V_{LN}
DC Input Voltage ($V_{DC}/2$)	275 V
Inverter Rated Power	9 kVA
Three Phase Load	9 kW
Grid Frequency f_G	60 Hz
Current Rating (RMS)	25 A
Filter Inverter-Side L_1	11.3 mH
Filter Grid-Side L_2	229.2 µH
Filter C_f	26.52 µF
Filter Damping R_f	0.97 Ω
Switching Frequency f_S	5 kHz

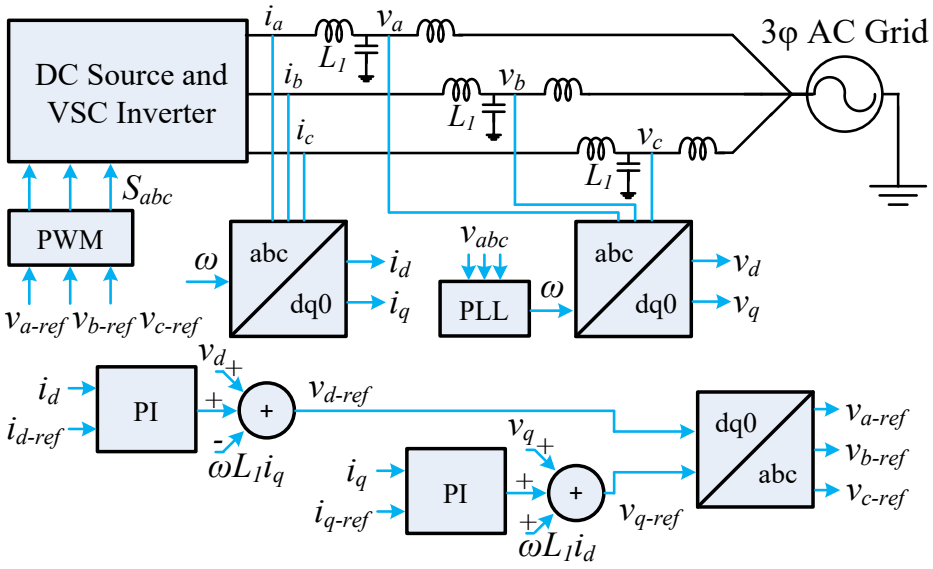


Figure 12: VSC Control System Implemented for Reactive Current Injection Control

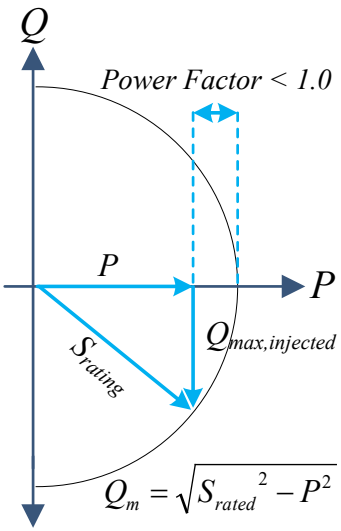


Figure 13: Maximum Compensation according to Rated Inverter Capacity

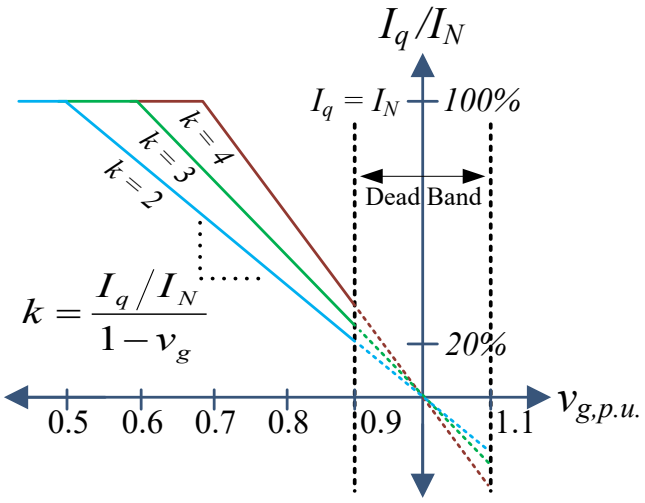


Figure 14: Control of Reactive Compensation for Voltage Instability Events with the injection Ramp Rate Defined

Provided here is further detail of implementing a system model that appropriately accounts for a detailed switched converter model including device losses. Particularly, this type of model needs to circumvent shoot-through phenomena and requires a LCL filter design due to harmonics generated. Also explained is the difference in inverter control between grid-connected and islanded modes of system operation.

When non-ideal device models are incorporated into the system model, where turn-on and turn-off switching times are not equal to zero, shoot-through phenomenon will exist. Shoot-through is an operational short created between the DC terminals through a phase arm when one device of the arm is attempting to turn on while the other device of the same arm attempts to turn

off. During this simultaneous action, there is an overlapping time period where both devices are conducting at the same time effectively creating the short.

Shoot-through existing in simulation can be effectively eliminated through modification of the PWM output control signals, by lagging the turn-on signals and leading the turn-off signals of either the upper or lower device(s) per arm of the converter. The lag can be a phase-shift of up to 10% of the switching frequency period without distorting PWM, as calculated in (7).

$$t_{lag} \leq 0.1\left(\frac{1}{f_s}\right) \tag{7}$$

The lead of the turn-off signal must then be twice the initial phase shift lag as in (8).

$$t_{lead} = 2t_{lag} \tag{8}$$

These lag and lead times are applied to the lower device signals of each phase in the studied system model. Satisfactory periods of time result between the upper and lower device signals of phase *N*. As a solution, these periods allow for satisfactory turn off of the upper device before the lower device begins to turn on and vice versa.

In order to properly filter the outputs of the detailed switched converter model, an LCL filter was implemented, a third order low pass filter. Such a filter effectively removes any harmonic

noise caused by device switching as well as any problematic interactions between system and filter resonance frequencies. Following the filter design in [38] as one of many methods of optimizing a third order filter, parameters were determined.

The filter design starts with defining both the switching frequency and the allowable amount of ripple in the line current (typically 10%). The inverter side inductance calculation follows these definitions according to (9).

$$L_1 = \frac{V_{DC}}{n f_S \Delta I_{Lmax}} \tag{9}$$

Here, n is the number of voltage levels of the converter output, f_S is the switching frequency selected, and ΔI_{Lmax} is the maximum allowable ripple current on the line. The filter capacitance parameter is defined as equal to or less than 5% of the base capacitance (Y-connected) as in (10).

$$C_f = 0.05(C_{base}) = 0.05\left(\frac{1}{\omega_G Z_{base}}\right) \tag{10}$$

Here, ω_G is the grid angular frequency, and Z_{base} is the base impedance of the system $\left(Z_{base} = V_{LL(RMS)}^2 / P_{rated}\right)$. With a desired attenuation of 20% ($k_a = 0.2$) which is a typical design selection, the grid side filter inductance is determined using (11).

$$L_2 = \left(\sqrt{\frac{1}{k_a^2} + 1}\right) \Big/ C_f \omega_S^2 \tag{11}$$

The last of the parameters, the damping resistance, placed in series with the filter capacitance, is determined by use of (11).

$$R_f = \frac{1}{3\omega_{res}C_f} \tag{11}$$

The resonant frequency of the LCL filter, ω_{res}, is calculated according to (12) with the given range for appropriate design.

$$\omega_{res} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}}, \qquad 10f_G < f_{res} < 0.5f_S \tag{12}$$

Calculated results for various switching frequencies are given in Table 4. These values correspond to a single-phase LCL filter utilized for each phase of the three-phase *Y*-connected system. With an increased inverter switching frequency, the impedance values are reduced. The 5 kHz switching frequency was selected for the presented model in order to safely avoid resonant interaction between switching frequency and resonant frequency.

Table 4: Filter Parameters for Various Inverter Switching Frequencies

Switching Freq. f_s	L_1	C_f	L_2	R_f
3 kHz	18.9 mH	26.52 μF	636.6 μF	1.606 Ω
5 kHz	11.3 mH	26.52 μF	229.2 μF	0.970 Ω
10 kHz	5.7 mH	26.52 μF	57.3 μH	0.487 Ω
15 kHz	3.8 mH	26.52 μF	25.47 μF	0.326 Ω

As one last note of modeling explanation, the difference in control between grid-connected and islanded modes of operation is primarily related to the phase-locked loop (PLL). In grid-connected mode, measurements from the grid at the point of common coupling are input to the inverter control for a reference frequency, but when running in islanded mode there is no grid frequency measurement for PLL synchronization. Upon detection of an islanding event, the control switches mode of operation to input ideal 60 Hz signals as inputs to the PLL control instead of grid measurements.

3.1.2 Case Results

A microgrid disconnection is simulated at 0.5 sec, after which the DG is solely powering the local load. A low voltage ride through event results when the inverter is not providing its full capacity ($P_{ref} < 1$ p.u.). Comparisons are drawn between the compensated and uncompensated systems. In order to observe temperature dynamics for both cases, P_{ref} is preprogrammed for each simulation case through the range of 0.2 to 1.0 p.u. power delivery, incremented by 0.2 p.u. Figure 15 plots the junction temperatures of the phase *A* upper branch SiC MOSFET for the specified range of P_{ref}, with and without reactive compensation. The temperature range is observed to be between 25 ^{0}C and 34 ^{0}C. In a reactive compensated system, the T_j fluctuations are constant regardless of P_{ref}. To utilize all of the inverter's apparent power, shown in Figure 13, the current experienced by a device is constrained by the total system current, (13), which is fixed while i_d and i_q vary.

$$i_{total} = \sqrt{i_d^2 + i_q^2} \tag{13}$$

The result is that for a compensated system, the device degradation will be faster because for a given P_{ref} the magnitudes and fluctuations of T_j are always larger. For the purpose of comparison, the junction temperatures for the Si IGBT without reactive compensation are shown in Figure 16.

Figure 17 provides post-processed data comparisons of the MOSFET and IGBT maximum junction temperatures. As observed over the entire range of P_{ref}, the SiC MOSFET always exhibits lower temperatures. Comparing ΔT_j for $P_{ref} = 1$, the Si IGBT has a ΔT_j twice that of the SiC MOSFET. The primary drawback of SiC based products is a cost justification. However, if SiC-based systems indirectly help reduce the size of mechanical components required for cooling, there will be an economic tradeoff to justify its use compared to Si as observed in this work.

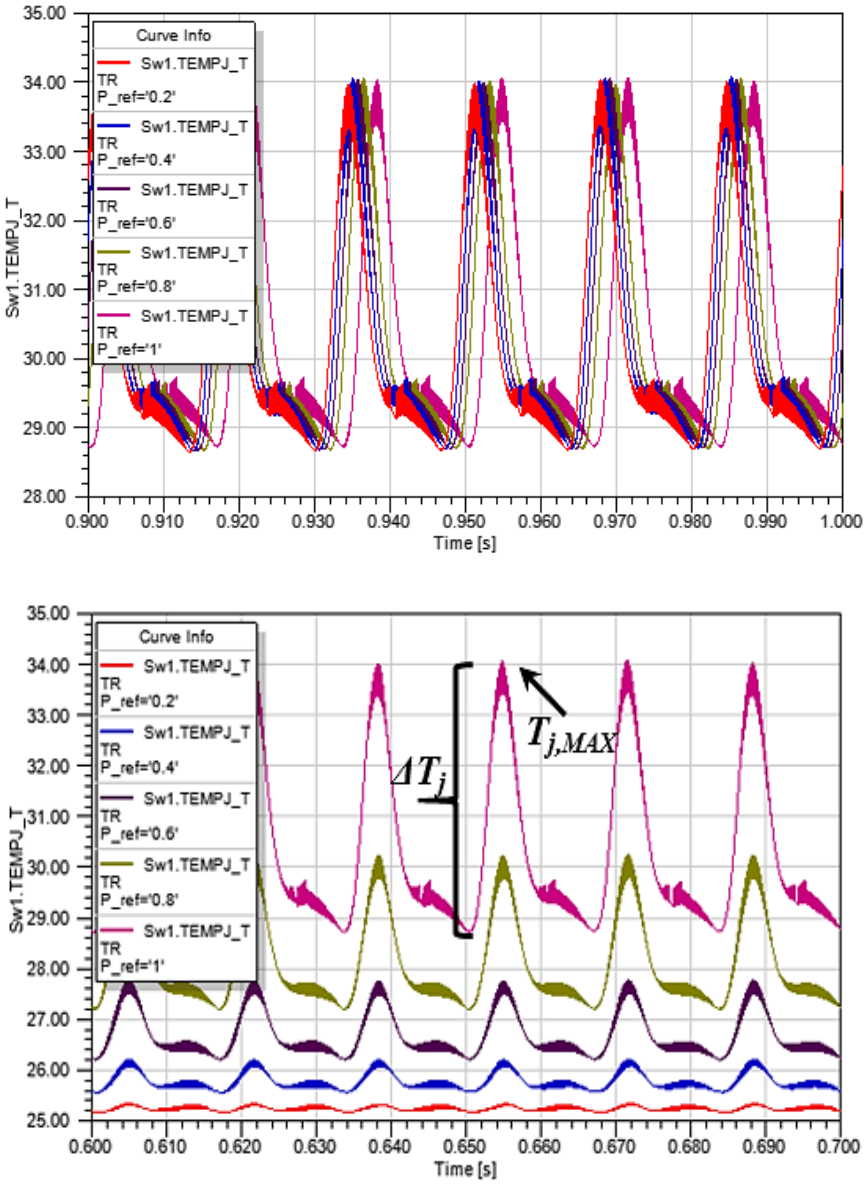


Figure 15: Junction Temperature on Phase *A* Upper SiC MOSFET with (above) and without (below) Reactive Compensation

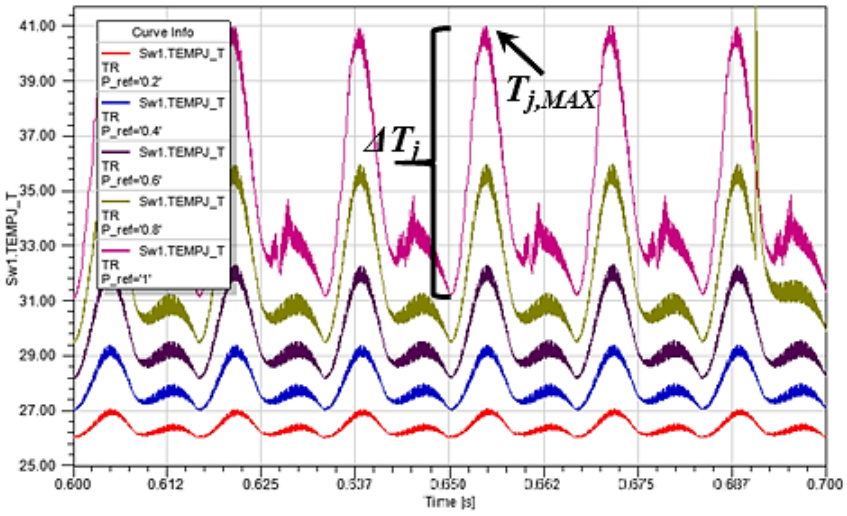


Figure 16: Junction Temperature on Phase *A* Upper IGBT during steady state (P_{ref} = 0.2 - 1.0 p.u.)

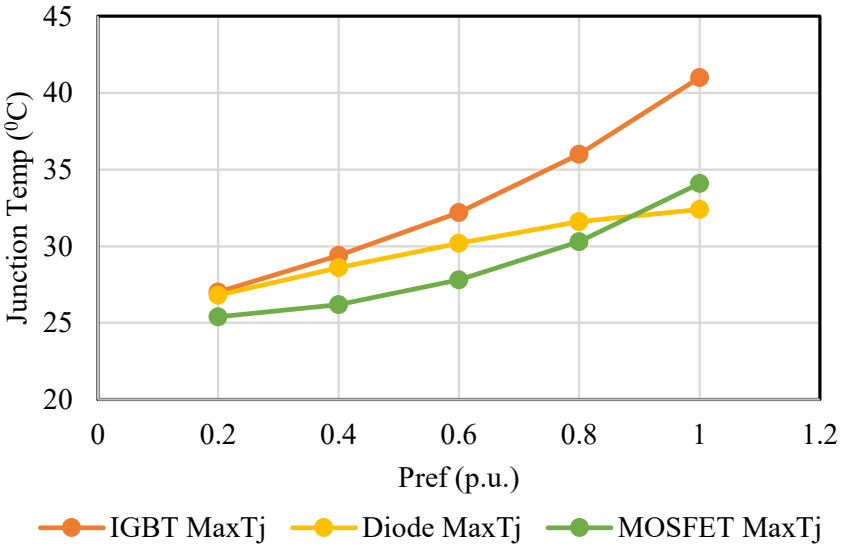


Figure 17: Comparing Maximum Junction Temperature for SiC MOSFET and Si IGBT and Diode with respect to Reference Power

3.1.3 Conclusions

This work has shown that with the adoption of smart inverters providing reactive compensation, higher thermal rise and device degradation rate are expected. This is exacerbated in Si IGBT-based inverter systems, compared to those using SiC MOSFETS. These observations should inform the evolving standards related to smart inverter design. Future work involves investigating the electro-thermal impacts of varying *k*, the ramp rate of current power injection.

3.2 IMPACT OF VIRTUAL SYNCHRONOUS MACHINE GRID SUPPORT

The increase of converter-interfaced distributed generation (DG), particularly renewable energy resources, results in a reduction of inertia or system strength conventionally safeguarded by synchronous machines (SM), especially apparent for self-contained microgrids. Resulting voltage instability can be addressed by reactive compensation as a grid support feature for smart inverters but not without added device degradation reducing system reliability [5]–[7]. Resulting frequency instability and the lack of desired SM inertial dynamics can be resolved by an increasingly popular solution, the synchronverter [8]–[10]. Designing the control of a DG inverter to mimic SM dynamics through virtual synchronous machine (VSM) control, is an approach introduced by Hans-Peter Beck and Ralf Hesse in [39], soon followed by [40], and finally accepted as a synchronverter in [9]. It is well known that SMs can synchronize with each other or with the grid autonomously without the need for external communications. Because hundreds of SMs penetrate the electric grid, researchers are developing strategies for power converters to mimic SM

dynamics. In emulating SMs, benefits include virtual inertia, self-synchronization properties, and damping [41].

An electro-thermal reliability assessment of the power semiconductor devices regulated by VSM control is lacking from the literature, and it is unknown as to whether there would be added or reduced thermal stress in comparison to conventional *dq* current regulation utilizing DG PLL synchronization. The reliability of power electronic conversion systems is primarily correlated to the thermal stress experienced by the semiconductor device materials [11], [12]. Lifetime degrades with high average junction temperatures and more emphatically with large junction temperature fluctuations experienced by the device [13]. Where *p*-*n* junction temperature magnitudes and fluctuations can be minimized, device reliability is improved. Numerous works have proposed various methods to improve converter reliability by such minimization utilizing various control strategies and modulation methods such as active thermal control (ATC) [21], [23], [24]. This work investigates the electro-thermal impacts of dynamic inverter responses upon a SiC power MOSFET when implementing either conventional or VSM control architectures.

3.2.1 Virtual Synchronous Machine Implementation

The examined inverter is a commonly used voltage source converter (VSC), two-level, three-phase, DG inverter connected to an equivalent grid via a LCL filter, as shown in Figure 18. The system parameters, given in Table 5, are based upon typical values for a residential scale three-phase inverter. The VSC inverter control system performs standard inner current control regulation and outputs *d*-axis and *q*-axis voltage references for pulse width modulation control as seen in (14)

and (15). Figure 19 depicts the synchronous *d-q* control structure and how it interfaces with the overall system.

$$v_{d-ref} = v_d - \omega L_1 i_q + (K_P + K_I/s)\left(i_d - i_{d-ref}\right) \tag{14}$$

$$v_{q-ref} = v_q + \omega L_1 i_d + (K_P + K_I/s)\left(i_q - i_{q-ref}\right) \tag{15}$$

Table 5: System Parameters for VSM Implementation

System Parameter	Value
AC Output Voltage (RMS)	120 V_{LN}
DC Input Voltage ($V_{DC}/2$)	275 V
Inverter Rated Power	9 kVA
Three Phase Load	9 kW
Grid Frequency f_G	60 Hz
Current Rating (RMS)	25 A
Filter Inverter-Side L_1	11.3 mH
Filter Grid-Side L_2	229.2 µH
Filter C_f	26.52 µF
Filter Damping R_f	0.97 Ω
Switching Frequency f_S	5 kHz
Source Inductance	0.1 mH
Source Resistance	6 µΩ

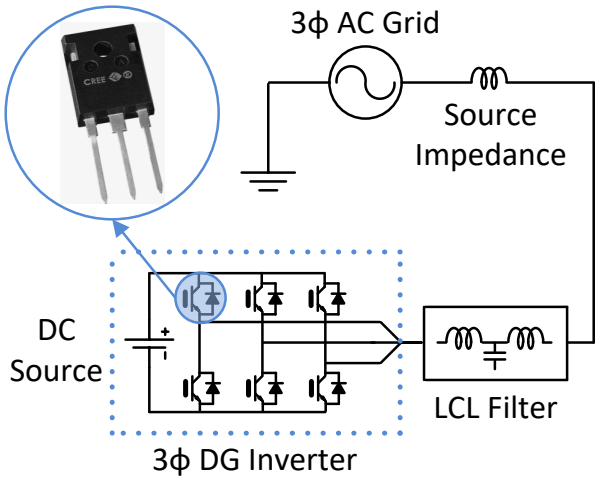


Figure 18: Modeled DG Inverter System

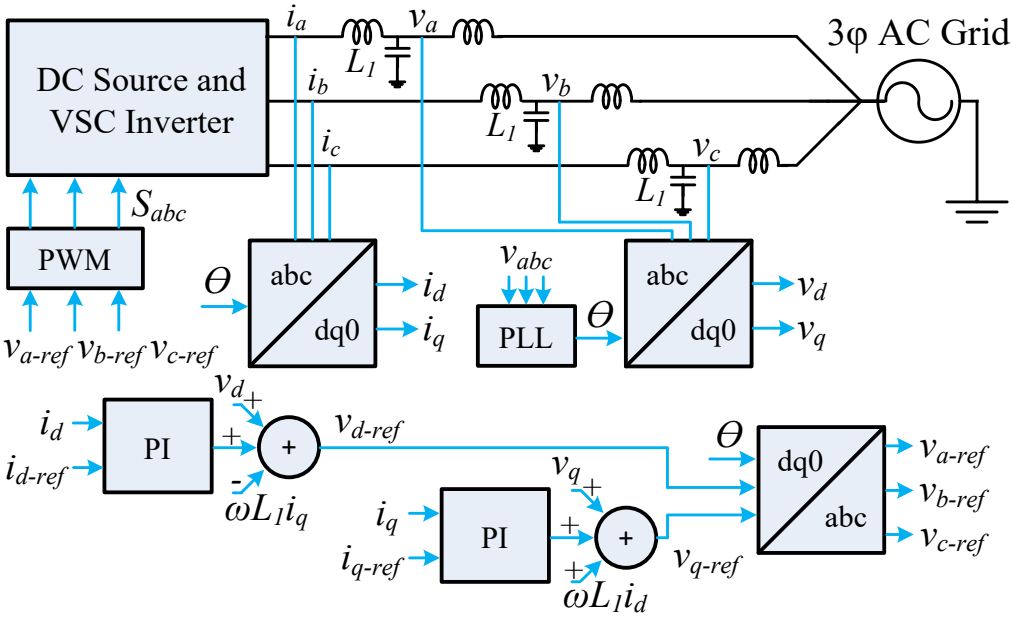


Figure 19: Voltage source converter *dq* control interfaced with system

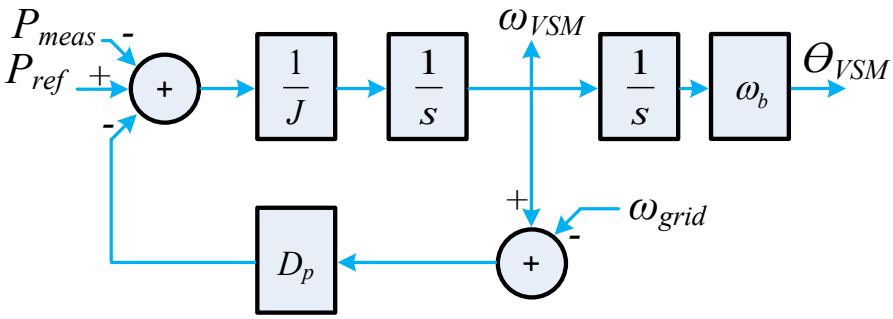


Figure 20: Swing equation implemented into system control architecture

Let us now address the syncronverter control and electrical frequency performance under phase disturbance. The VSM control architecture for an inverter mimics the dynamics of a SM by translating the swing equation, (16), into a control loop that generates the frequency and phase angle used to synchronize a DG inverter to the grid [9].

$$J\ddot{\theta} = T_m - T_e - D_p\dot{\theta} \quad with \quad T_e = pM_f i_f \langle i, \widetilde{\sin\theta} \rangle \tag{16}$$

The various parameters used in (26) are defined in Table 6, and J and D_p are degrees of freedom for the DG inverter operator. With the relationship between torque and power, as well as between phase angle and speed ($\dot{\theta} = \omega$), the mirror translation from SM parametric terms to the terms of an electrical inverter can be provided as in (17), [42].

$$\ddot{\theta}_{VSM} = \frac{1}{J}\left[P_{ref} - P_{meas} - D_p\left(\omega_{VSM} - \omega_{grid}\right)\right] \tag{17}$$

Table 6: VSM Control Parameter Definitions

Parameter	Description
$\theta, \dot{\theta}$	Rotor angle and rotor speed
J	Moment of inertia
T_m	Mechanical torque applied to rotor
T_e	Electromagnetic torque
D_p	Friction coefficient (damping constant)
p	Number of pairs of poles
M_f	Maximum mutual inductance
i_f	Rotor field excitation current
i	Stator current
$\langle -, - \rangle$	Conventional inner product
$\widetilde{\sin\theta}$	$[\sin(\omega t), \sin(\omega t - 2\pi/3), \sin(\omega t - 4\pi/3)]^T$

Table 7: VSM Control Parameter Values

Elements	Description	Value
J	Moment of inertia	{1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5}
D_p	Friction coefficient	{15, 20, 25, 30, 35, 40, 45, 50}
$-D_p/J$	Case ratio with k_{VSM}	-10
ω_{VSM}	VSM frequency/speed	variable (p.u.)
ω_{grid}	Grid freq. measured	variable (p.u.)
ω_b	Base angular frequency	377 (rad/s)
θ_{VSM}	VSM synch. angle	variable (radians)
P_{meas}	Power measurement	measured (p.u.)
P_{ref}	Power reference	1.0 (p.u.)

Obtaining the synchronization phase angle (θ_{VSM}) is sufficient for the virtual emulation of the swing equation into DG inverter control. Figure 20 depicts (4) implemented into a control architecture, which overlays Figure 19 replacing the PLL. All parameter values used for simulation of the synchronverter performance are given in Table 7.

With evaluation of the stability of the swing equation in the Laplace domain, a pole appears in the left-hand complex plane in terms of the moment of inertia and the friction coefficient $\left(s = -D_p/J\right)$ as shown in (18).

$$Js^2 + D_p s = T_m - T_e = 0 \quad \rightarrow \quad s\left(Js + D_p\right) = 0 \quad \rightarrow \quad Js = -D_p \quad \rightarrow \quad s = -D_p/J \quad (18)$$

This implies first of all that the system is inherently stable with a negative pole, but also that a decrease in D_p and J, the friction coefficient and the moment of inertia, will increase damping of the response. In Figure 21, both J and D_p are altered together as a constant ratio as in (28) to demonstrate the effects upon synchronization. The system is disturbed in such a way that the grid voltage will lead the current by 30 degrees at time 0.6 seconds. As the ratio of D_p and J decreases, the departure from nominal frequency is minimized. Similar to SM dynamics, any increase in J will result in higher stored kinetic energy in the rotor that is released when a system disturbance occurs.

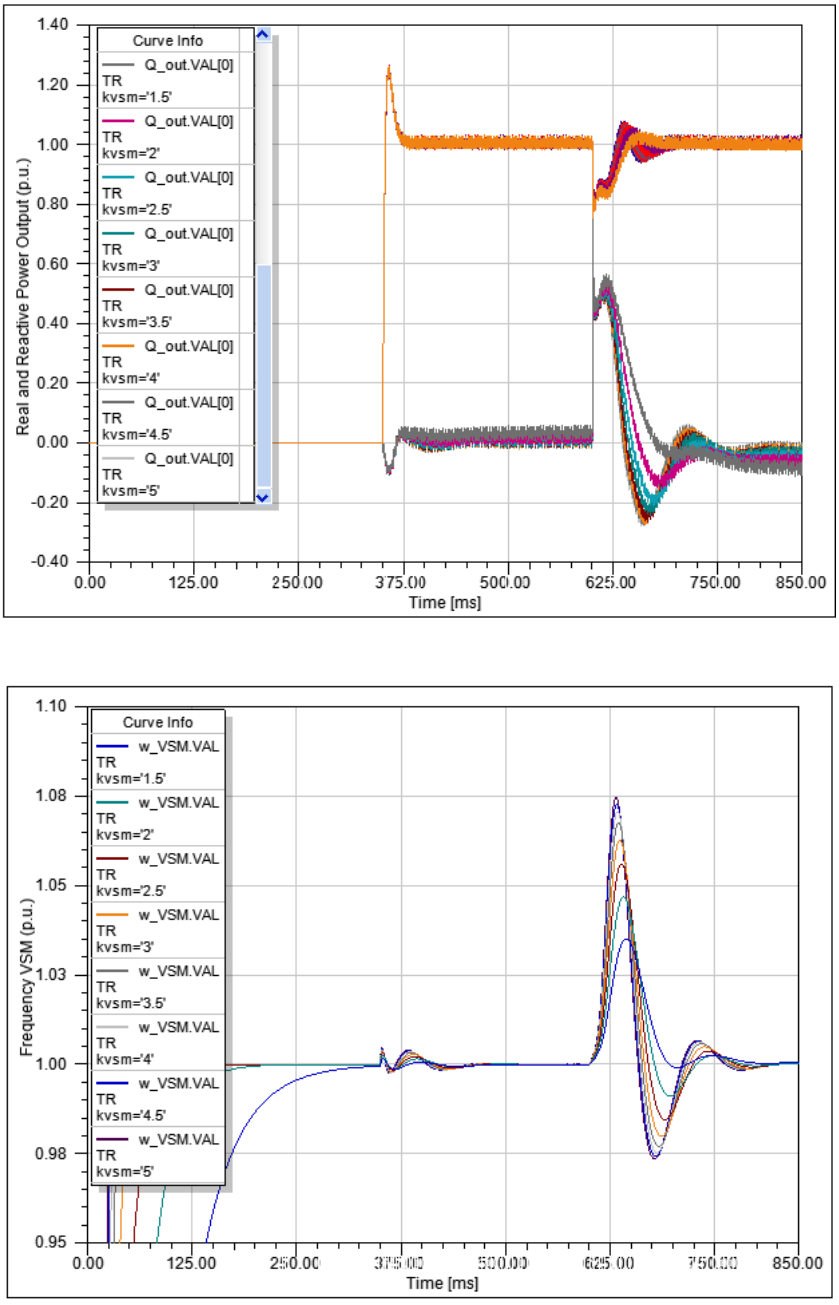


Figure 21: Real and reactive power output of inverter (top) and associated change in VSM frequency (bottom) for varying values of D_p, J.

3.2.2 Case Results

An assessment of thermal stress and a comparison of VSM to conventional *dq* current regulation with PLL frequency control are provided in Figure 22 and Figure 23. From left to right, the plots depict the real and reactive output power of the inverter, the frequency response with the corresponding control, and the thermal cycling for the SiC MOSFET in the upper arm of phase *A* (stress is similar for all devices and phases).

The sequence of simulation events is as follows:

1. [0.0ms to 350ms] The system initializes allowing for frequency to synchronize before requiring power from DG.
2. [350ms to 600ms] The reference power of 1.0 p.u. is requested of the DG and temperature achieves steady state.
3. [600ms to 850ms] The grid voltage phase angle is altered to lead the current by 30 degrees and the power electronic system frequency responds accordingly.

Less frequency deviation from nominal shows a performance benefit of VSM. The effect of the phase shift upon thermal stress is negligible for the devices of the DG inverter.

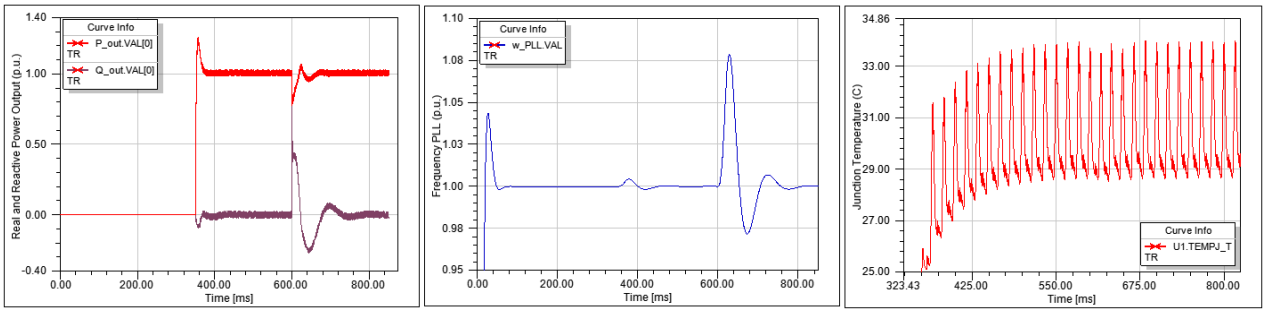


Figure 22: The *dq* current regulated PLL power, frequency, and thermal responses with a 30 degree phase shift on grid

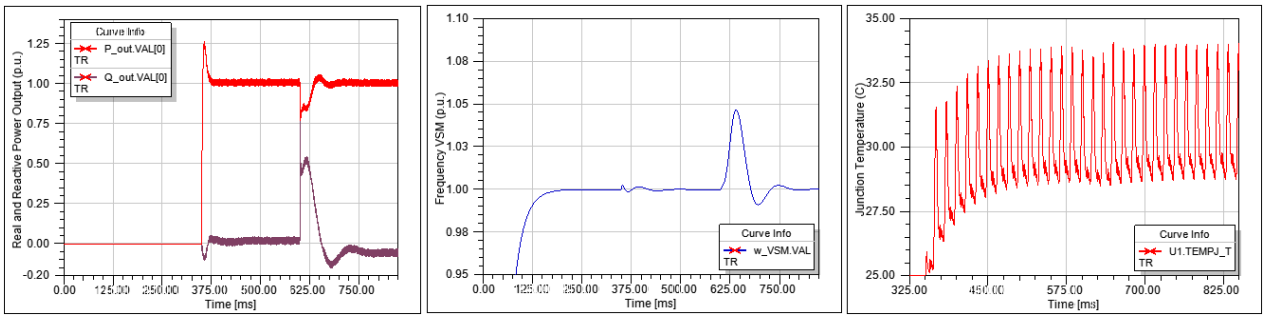


Figure 23: The VSM power, frequency, and thermal responses with a 30 degree phase shift on grid (D_p = 20, J = 2)

The thermal response is linked to the power loss (modeled by a dependent current source) through the transient thermal impedance of the device as depicted in Figure 5. A frequency deviation event has impact upon the real and reactive power drawn from the DG, but due to the transient (millisecond) time frame of the event, the thermal impact is negligible. In contrast, voltage instability events with changes of apparent load do have a significant thermal impact due to a direct link to the loss through the thermal impedance and due to the longer time frame for load change events. The magnitude of device temperatures are depicted in Figure 9 for varying amounts of load.

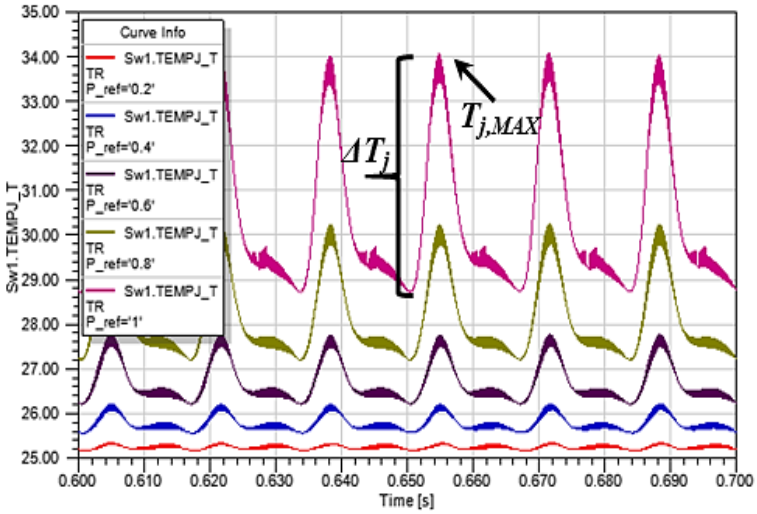


Figure 24: Junction temperature on phase *A* Upper SiC MOSFET for varying load requirements

3.2.3 Conclusions

When addressing the negative impacts of increasing DG penetration, synchronverter technology can help remedy frequency instability and does not have adverse impacts in its performance upon device stress. This is due to the shorter transient time frame associated with frequency deviation system phenomena and the limited effect that frequency deviations have upon currents through the converter control response. When assessing reliability of power electronic converters, one must distinguish between short and long-term events of added power loss translating to added thermal stress. Successful thermal stress minimization work in the literature apply only to long term switching loss minimization as in [21]. For similar reasons, manufacturer datasheets provide both pulse and steady state performance maximums, where devices can handle increased stress if only

subjected for a short duration. This work investigated a short-term event on the order of milliseconds as opposed to seconds or minutes. Because frequency instability is remedied quickly in DG inverters, synchronized by either VSM or PLL, small changes in loss from the base power electronic system losses only negligibly impact device junction temperatures.

In the grand scheme of the entire proposal, completing this syncronverter work was a time for reevaluation of the topic. A long-term thermal cycling analysis, in contrast to short-term, is an essential requirement before considering application of an active thermal control methodology. Therefore grid converter functions or various grid converter interaction will be a candidate for benefiting from active thermal control only if the thermal cycling dynamics on the order of seconds to minutes as opposed to milliseconds.

4.0 NATURAL SWITCHING SURFACE CONTROL THEORY FOR THE DAB

With the modernization of the electric grid, there are more grid interfacing power electronic converters. With more grid converters, there are more advanced converter features and dynamic functions. With more features and functions, there is the potential of significant added device stress. With added device stress, there is accelerated device degradation causing reduced lifespan expectancy. The key to preserving device lifetime within the context of this proposed work is a form of active thermal control (ATC). One form of ATC is to keep the devices from cooling down, effecting a smaller thermal cycle difference during long-term temperature fluctuations (ΔT_j). Implementing this minimization of thermal cycling is in this work effected by use of natural switching surface (NSS) control.

Building off of all presented content to this point, the conceptual roadmap of the proposed contribution is as follows. The DC-DC Dual Active Bridge (DAB), depicted in Figure 25, is increasingly prevalent on the electric grid and elsewhere for various applications such as electric vehicle charging. Natural Switching Surface (NSS) control is a recently developed and promising form of efficient control applied to the DAB. Active Thermal Control (ATC) is a proven method of extending the lifetime of power electronic devices by limiting how far the devices cool down, effectively reducing the thermal cycling on the junction of a semiconductor device, where deeper thermal cycling is linked to increased degradation of the device due to materials handling temperature stress differently. The benefits of NSS can be utilized for the preservation of device lifetime extension as a form of ATC. This is similar to the burst mode of Ordonez work for light load applications. This work involves some sort of tradeoff between device losses (efficiency) and device lifetime (reliability). ATC for long-term junction temperature fluctuations strikes that

balance. The crux of the research approach taken herein is the merging of the aforementioned benefits of active thermal control (ATC) for power electronic system reliability benefits [22], with the flexibility, efficiency and simplicity of design benefits offered by natural switching surface control methodology [43], [44], all for the purpose of preserving the life of power electronics. This approach is applied to the dual active bridge, as a subjective object and not as the particular objective.

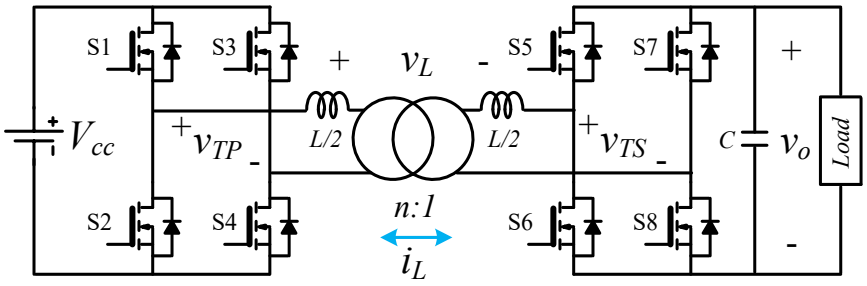


Figure 25: DC/DC Isolated Bidirectional Power Converter the Dual Active Bridge (DAB)

The concept of a dual active bridge (DAB) converter as an isolated bidirectional DC/DC converter (IBDC) was first introduced the early 1990s in [45], soon followed with [46], [47] and has since continuously increased in popularity due to its wide range of applicability to many applications as seen in [48], a good example of application to hybrid electric vehicles (HEV). The first development of a boundary control scheme (or natural switching surface) for the DAB is presented in [43]. The DAB-IBDC is gaining much attention largely due to its power density gains in utilizing high frequency transformers within power conversion systems [46], [47], [49]. Beyond power density benefits, a primary benefit of the DAB is the operational efficiency [50].The

technology has been further developed for efficiency gains when strategically employing natural state-plane trajectories to optimize efficiency specifically in light load conditions [44].

4.1 CONTROL MODE WITH FOUR SWITCHING SURFACES

The implementation of controlling the DC-DC dual active bridge along natural switching surfaces is presented here as a step closer to presenting ultimate contribution. The DAB topology has four switching structure configurations as seen in Figure 26. These circuit switching configurations mirror conventional DAB control.

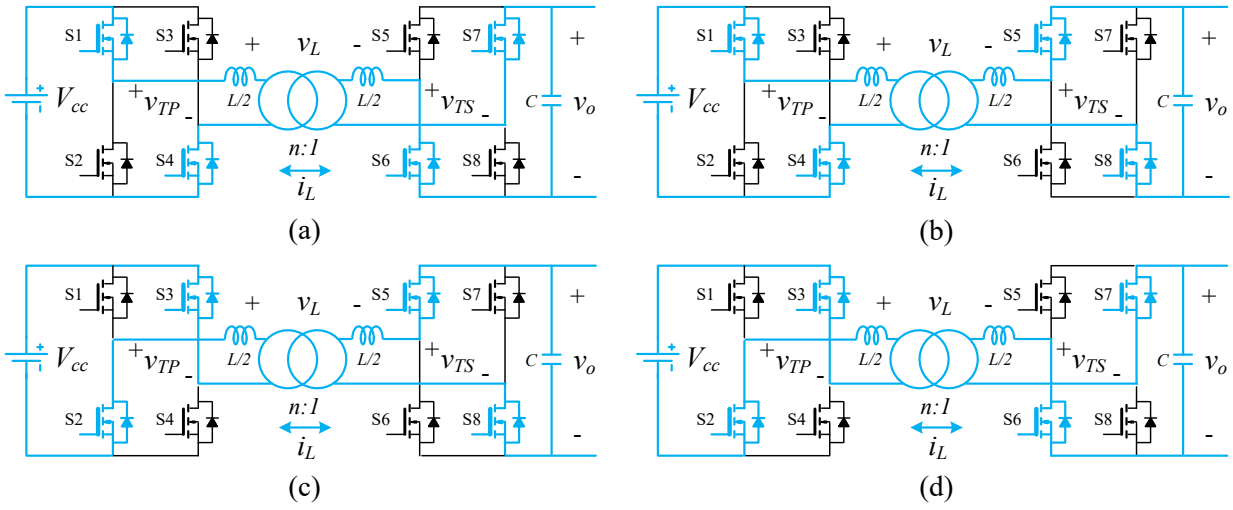


Figure 26: Four switching structures of the dual active bridge for power delivery

For simplified analysis of the dual active bridge, the transformer will be considered with an equivalent transformer inductance as seen in Figure 27, provided that the magnetizing inductance is assumed to be much larger than the leakage inductance.

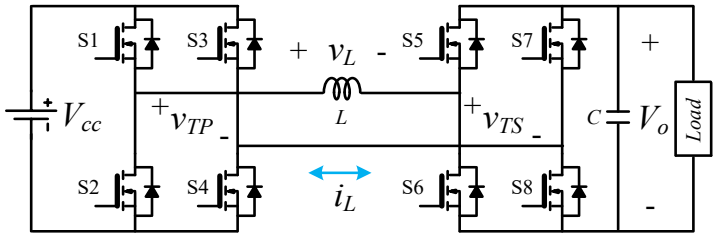


Figure 27: Dual Active Bridge Circuit Considering only Leakage Inductance for Simplified Analysis

Note that this analysis must be kept consistent by either considering n = 1 or accounting for the turns ratio within the representation of V_{cc} where $V_{cc} = V_o/n$. The voltage seen across the transformer equivalent inductance, corresponding to the four switching configurations, are given in (1) through (4) and correspond to Figure 26 (a) through (d) respectively.

$$v_L = V_{cc} + v_o \tag{1}$$

$$v_L = V_{cc} - v_o \tag{2}$$

$$v_L = -V_{cc} - v_o \tag{3}$$

$$v_L = -V_{cc} + v_o \tag{4}$$

The DAB operating state variables are as in (5) and (6).

$$C\frac{dv_o}{dt} = u_2 i_L - i_o \tag{5}$$

$$L\frac{di_L}{dt} = u_1 V_{cc} - u_2 v_o \tag{6}$$

Where $u_1 = 1, -1$, for $v_{T1} = V_{cc}, -V_{cc}$ respectively, and $u_2 = 1, -1$ for $v_{T2} = v_o, -v_o$. When normalized, these can be expressed as (7) and (8).

$$\frac{dv_{oN}}{dt_N} = 2\pi(u_2 i_{LN} - i_{oN}) \tag{7}$$

$$\frac{di_{LN}}{dt_N} = 2\pi(u_1 V_{ccN} - u_2 v_{oN}) \tag{8}$$

Where for normalization, $x_{xN} = y_x/V_r$, $i_{xN} = Z_0(i_x/V_r)$, $f_0 = 1/T_0 = 1/(2\pi\sqrt{LC})$, and V_r is the output voltage reference. When these two normalized state variables are combined into a second order differential equation, (9) results.

$$\frac{d^2 i_{LN}}{dt_N^2} = 4\pi^2 u_2 (i_{oN} - u_2 i_{LN}) \tag{9}$$

This second order differential equation can be manipulated into being expressed in the form of (10).

$$i_{LN} = Acos(\beta t_N) + Bsin(\beta t_N) + i_{oN} u_2 \tag{10}$$

Where $A = (i_{LN}(0) - u\_2 i_{oN}), B = (di_{LN}/dt_N)/\beta,$ and $\beta = 2\pi.$ Upon trigonometric manipulation, the natural switching surfaces are comprehensively expressed in (11) associated with all four switching configurations as in Figure 26 and in (1) through (4).

$$\begin{aligned} \lambda_{1,2,3,4} = (V_{ccn} u_1 - v_{0n} u_2)^2 - \left(i_{Ln,target} - i_{0n} u_2\right)^2 - (V_{ccn} u_1 - u_2)^2 \\ + (i_{Ln} - i_{0n} u_2)^2 \end{aligned} \tag{11}$$

Where $u_1 = 1, -1$ for $v_{T1} = V_{cc}, \ -V_{cc}$, and $u_2 = 1, -1$ for $v_{T2} = v_0, \ -v_0$. Table 8 aids in grasping the four switching surface (SS) converter configurations corresponding to the above equation (11), as well as corresponding to the four switching structures of Figure 26.

Table 8: Four Natural Switching Surface Configurations

SS	u_1	u_2
1	1	-1
2	1	1
3	-1	1
4	-1	-1

Each switching surface of *M4* can then be placed into the circular form of (12).

$$(x - x_o)^2 + (y - y_o)^2 = r^2 \tag{12}$$

Where $r = \sqrt{\left(i_{LN,T} - i_{oN}u_2\right)^2 + (V_{ccN}u_1 - u_2)^2}$, $x = -u_2 v_o$, $x_o = V_{ccN}u_1$, $y = i_{LN}$, $y_o = i_{oN}u_2$, and $i_{LN,T}$ is the target normalized current through the transformer. This circular form is consistent with the circular natural trajectories obtained from the DAB. These circular natural trajectories or surfaces are depicted conceptually in Figure 28 for the buck and boost modes of operation for the DAB [43]. Here the normalized current of the transformer inductance is plotted against the normalized output voltage on the output capacitance, the two state variables of choice for control of the converter. This type of plot is associated with what is known as state plane analysis. In this depiction, Δv_0 is the output voltage ripple, v_{0n} is the normalized output voltage, and V_{rn} is the normalized output voltage reference. The symbols λ_1 through λ_4 in Figure 28 represent the natural surfaces as described in equation (11). These surfaces are the paths along which the state variables ($C\frac{dv_o}{dt}$ and $L\frac{di_L}{dt}$) will naturally operate until a switching action is dictated.

Observing the state plane diagrams as a design tool alongside the time domain waveforms brings a unique advantage to the power electronics control engineer. State plane analysis brings an abstract yet intuitive approach to designing a converter control method to ones given purpose.

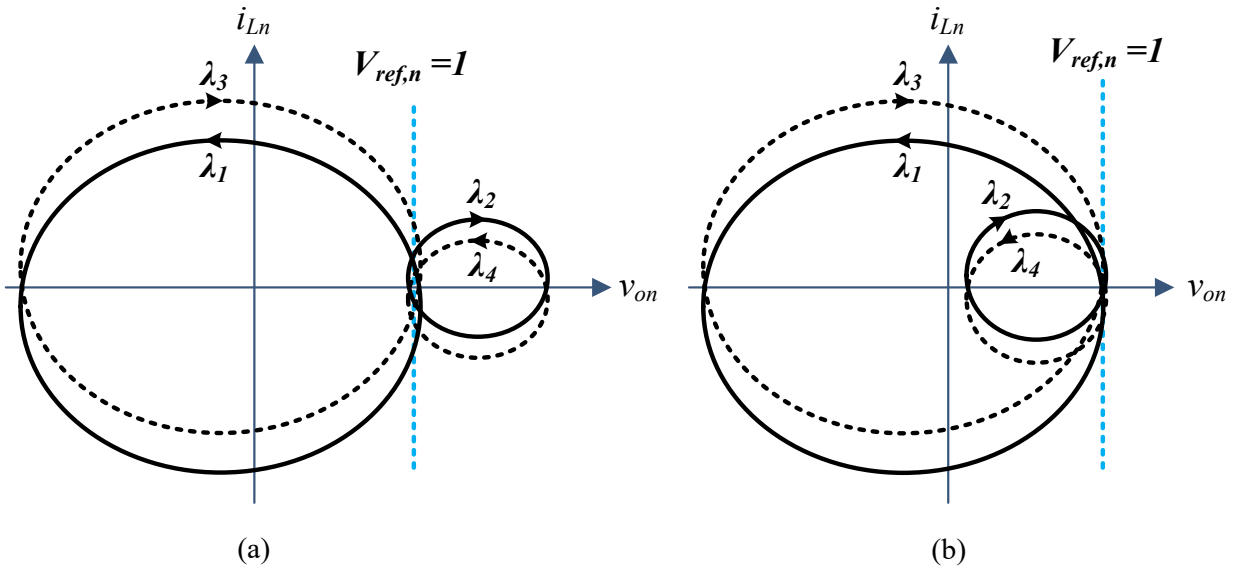


Figure 28: Normalized natural switching surfaces of the DAB in the (a) buck and (b) boost modes of operation

When zooming in upon the intersections of the circular trajectories in Figure 28, the control law (41) dictates a steady state operation where the natural switching surface trajectories conceptually will appear as in Figure 29. The connections between arcs in this diagram are the points at which a switching action occurs passing from one DAB switching configuration to another (Figure 26), passing from one natural surface to another (Figure 28). This control law that effects NSS control methodology follows the four-step switching sequence given in (13), associated with the four switching structures depicted in Figure 26.

$$\lambda_1 \rightarrow \lambda_2 \rightarrow \lambda_3 \rightarrow \lambda_4 \tag{13}$$

Passing through these four switching surfaces, $\lambda_{1,2,3,4}$, completes one switching cycle of the DAB.

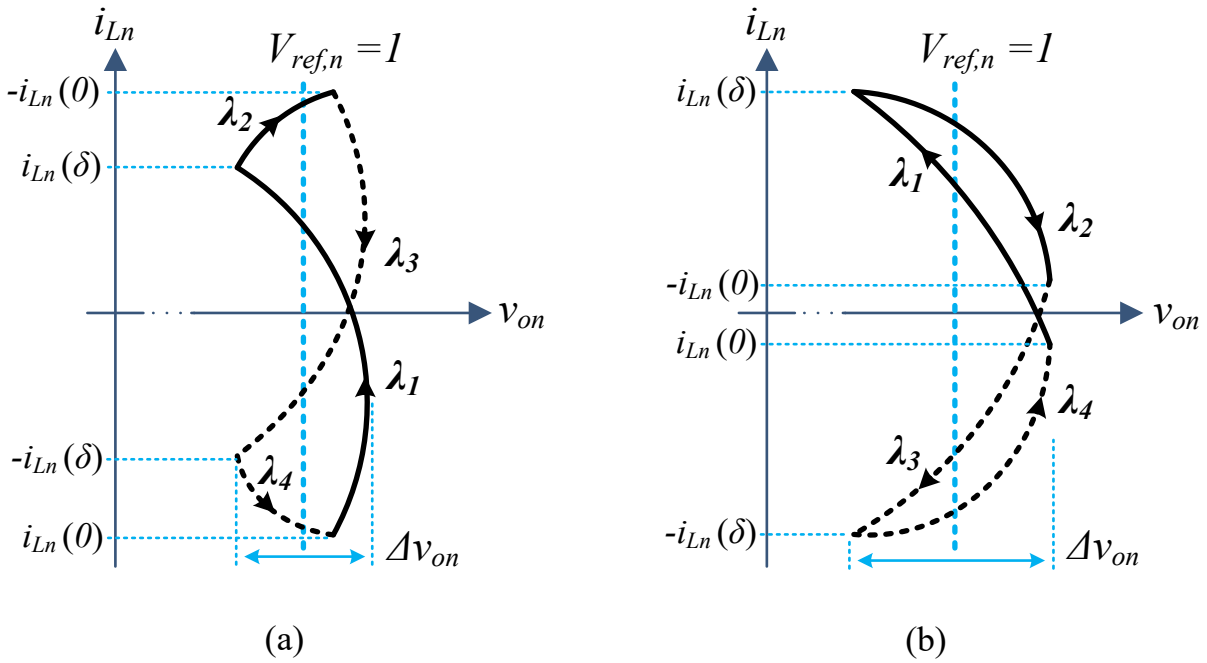


Figure 29: Steady state conceptually of normalized natural switching surfaces for the DAB in the (a) buck and (b) boost modes of operation

The control law dictates the transitions between surfaces by setting current targets upon the transformer inductance current. These current targets are calculated for each switching surface according to (14) through (17).

$$i_{Ln,Target}(\lambda_1) = -i_{0n} - \sqrt{(-V_{ccn}^2 - 2V_{ccn} - 1 + r_{\lambda_1}^2)} \tag{14}$$

$$i_{Ln,Target}(\lambda_2) = -i_{0n} + \sqrt{(-V_{ccn}^2 + 2V_{ccn} - 1 + r_{\lambda_2}^2)} \tag{15}$$

$$i_{Ln,Target}(\lambda_3) = -i_{Ln,Target}(\lambda_1) \tag{16}$$

$$i_{Ln,Target}(\lambda_4) = -i_{Ln,Target}(\lambda_2) \tag{17}$$

Where r_{λ_1} and r_{λ_2}, the radii for the first and second trajectories, are calculated as in (18) and (19).

$$r_{\lambda_1} = (1 + 2V_{ccn} + V_{ccn}^2 + (i_{LnB} - i_{on})^2) \tag{18}$$

$$r_{\lambda_2} = (1 - 2V_{ccn} + V_{ccn}^2 + (i_{LnB} - i_{on})^2) \tag{19}$$

Further detailed work and a more complete explanation concerning this delicate task of setting current targets is provided in [43], [51], and will be referenced for completion of this proposed

research. An example of such current targets in action can be seen in the steady state boost operation depiction in Figure 30, where a state plane diagram (a) and corresponding signal waveforms (b) are provided. Here v_{T1} and v_{T2} represent transformer voltage on the primary and secondary sides, respectively. The transition from one trajectory to another (λ_1 to λ_2) is triggered when the associated current target is met or satisfied ($i_{L\lambda_2,Target} = i_{Ln}(\delta)$).

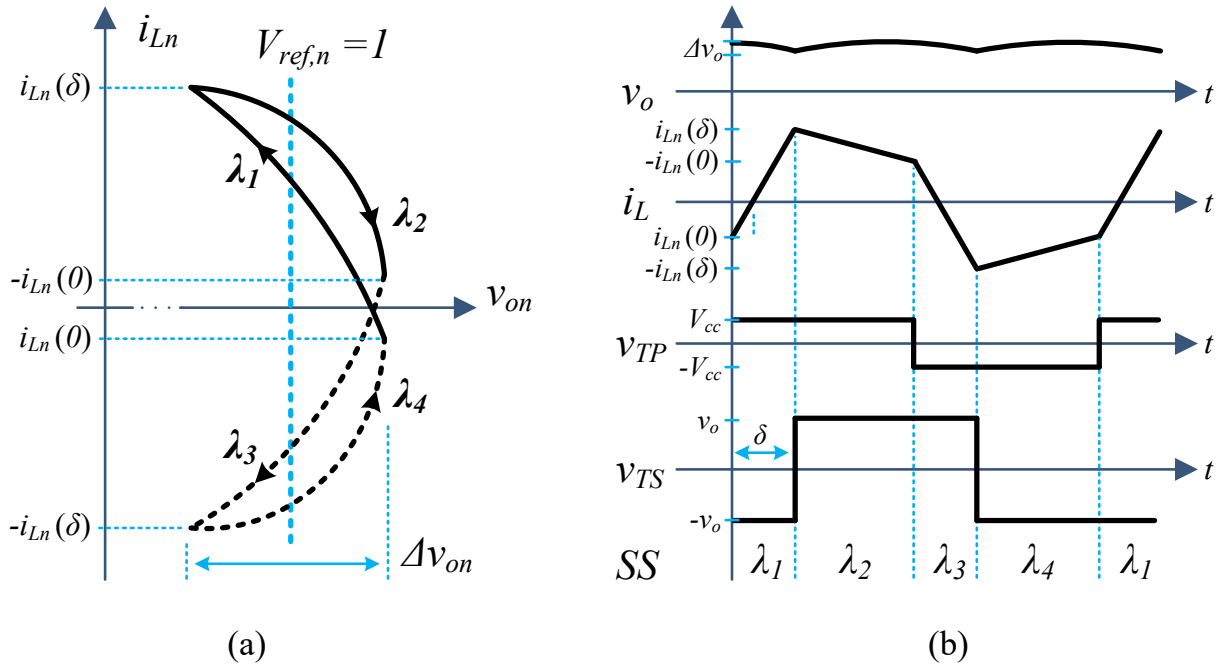


Figure 30: Steady state operation of the DAB in boost mode showing (a) state plane and (b) corresponding waveforms

Lastly, and importantly to this proposed work, there are degrees of freedom that can be taken advantage of in this NSS control. Manipulating the length of the radius described in equation (12) would be an example. This manipulation influences the transformer inductance current targets

described in (14) through (17), effectively influencing the switching frequency and converter losses. These current targets modifications by changing the radius of the associated surface on the state plane. Figure 31 shows such a modification made to surface λ_2, depicted both on the state plane as well as in the time domain. One can observe that with such radius modification, the effective switching frequency would consequently be altered. The modulation of the primary and secondary transformer voltages also experience consequence. The magnitudes of the current would also be altered and consequently losses. Pertinent to the active thermal control in this work's contribution, losses generate heat. Similar modifications have been designed for the preservation of device lifetime.

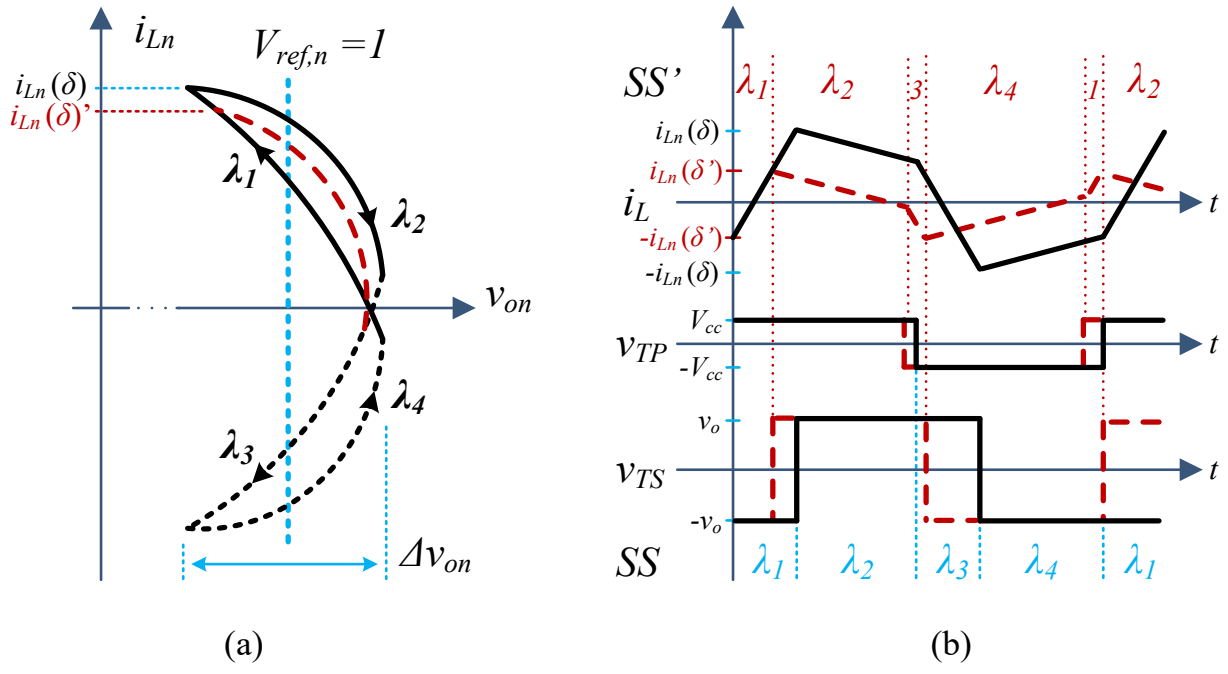


Figure 31: Modification of natural trajectory λ_2

4.1.1 Simulation Validation for the Four Trajectory Mode

Simulation results are provided here serving a purpose of validation for the *M4* NSS control methodology as well as familiarizing the reader with an implementation of the control. With the ratings of the system provided in Table 9, the case is a heavy loading condition. More explanation of parameter selections are provided, further up and further in. The following plots are simulation results achieved in the ANSYS software package.

Table 9: Parameters for Four Trajectory Validation Simulation

Parameter:	Value:	Description
M	*M4*	Mode of strategic trajectories
P_o	7.2kW	Output power demanded
V_{cc}	120	Input voltage
V_o	240	Output voltage (V_{ref})
d	$V_o/(nV_{cc})$	Conversion ratio (n = 1.5)
f_{sw}	4kHz	Switching frequency
m	1.0	Modulation index

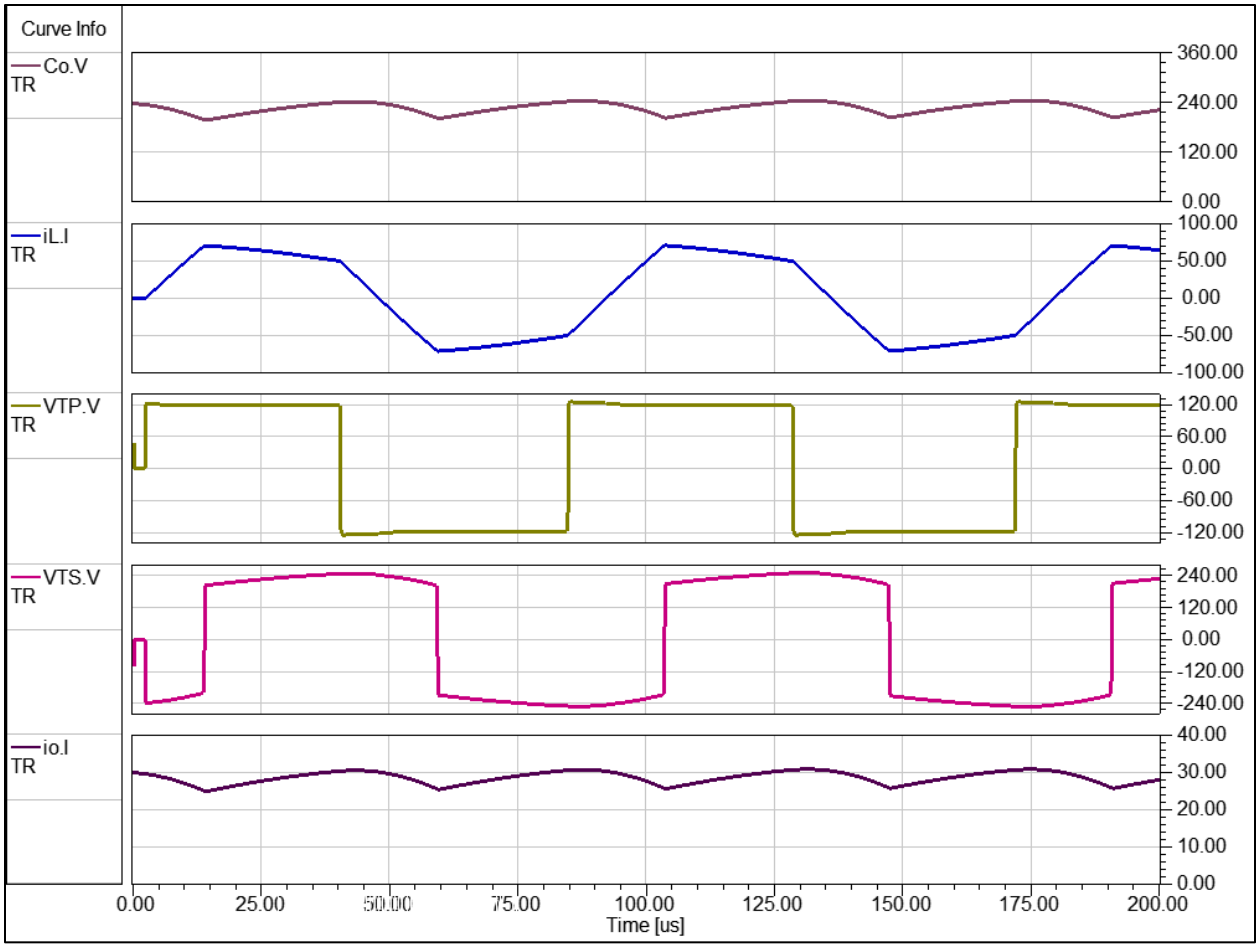


Figure 32: Results of output voltage, transformer current, primary and secondary voltage, and output current for Validation of *M4*

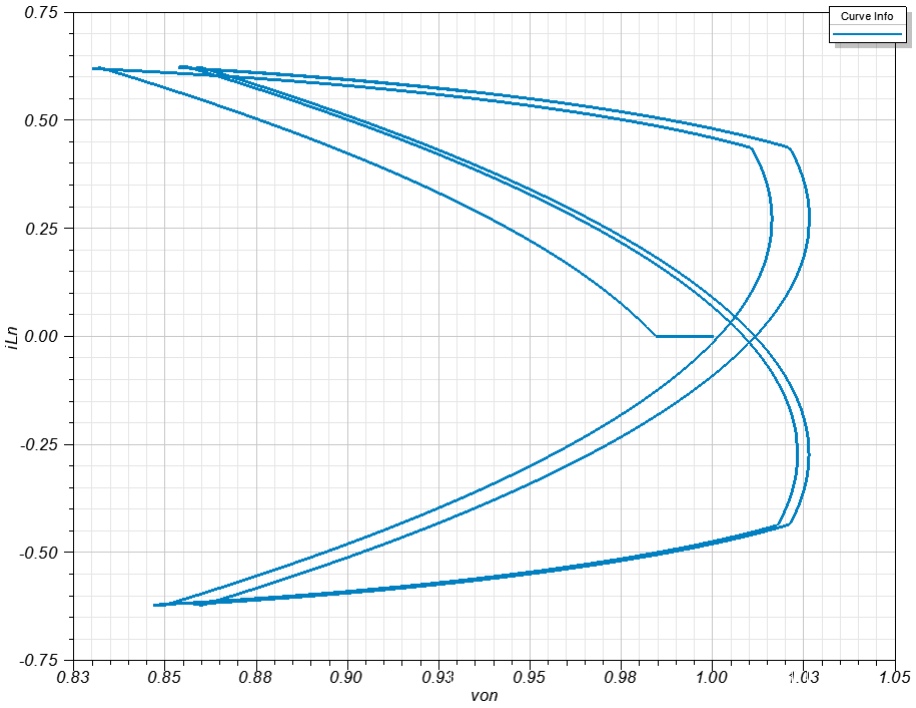


Figure 33: Normalized state plane result for *M4* operating under heavy loading

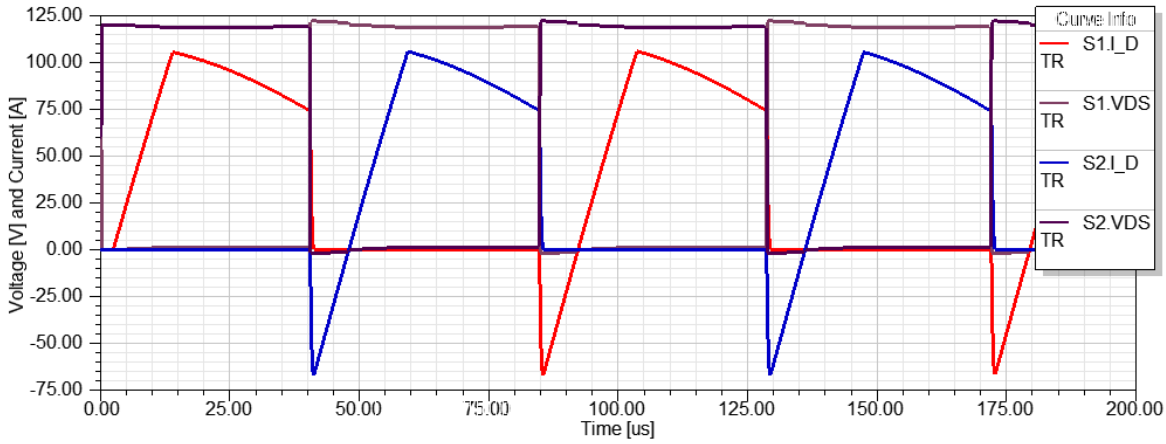


Figure 34: Voltage V_{DS} and Current I_D for both S_1 and S_2

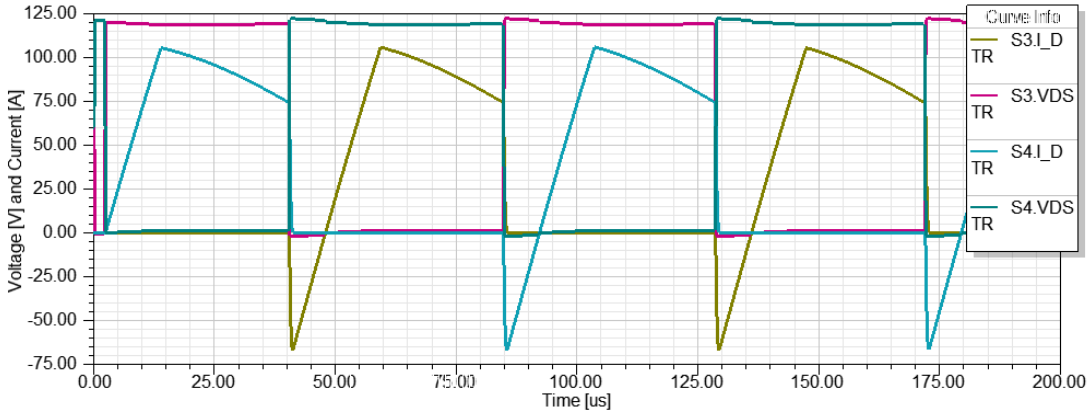


Figure 35: Voltage V_{DS} and Current I_D for both S_3 and S_4

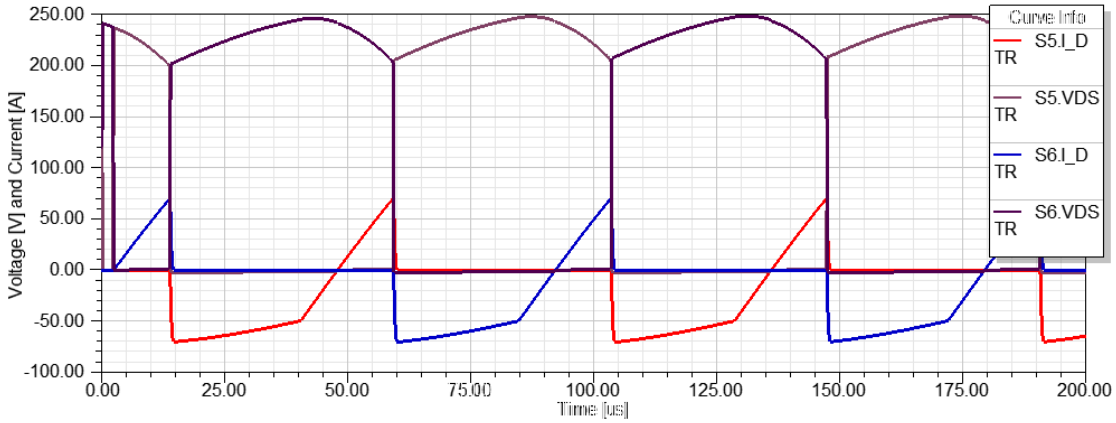


Figure 36: Voltage V_{DS} and Current I_D for both S_5 and S_6

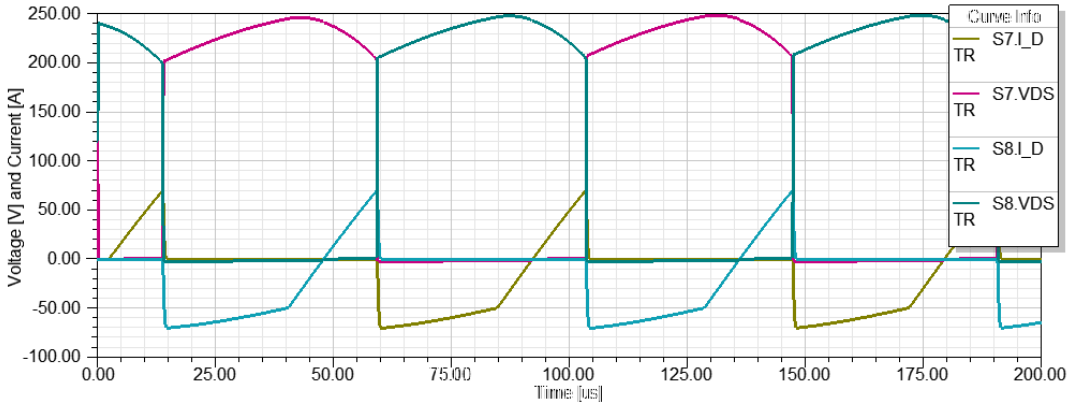


Figure 37: Voltage V_{DS} and Current I_D for both S_7 and S_8

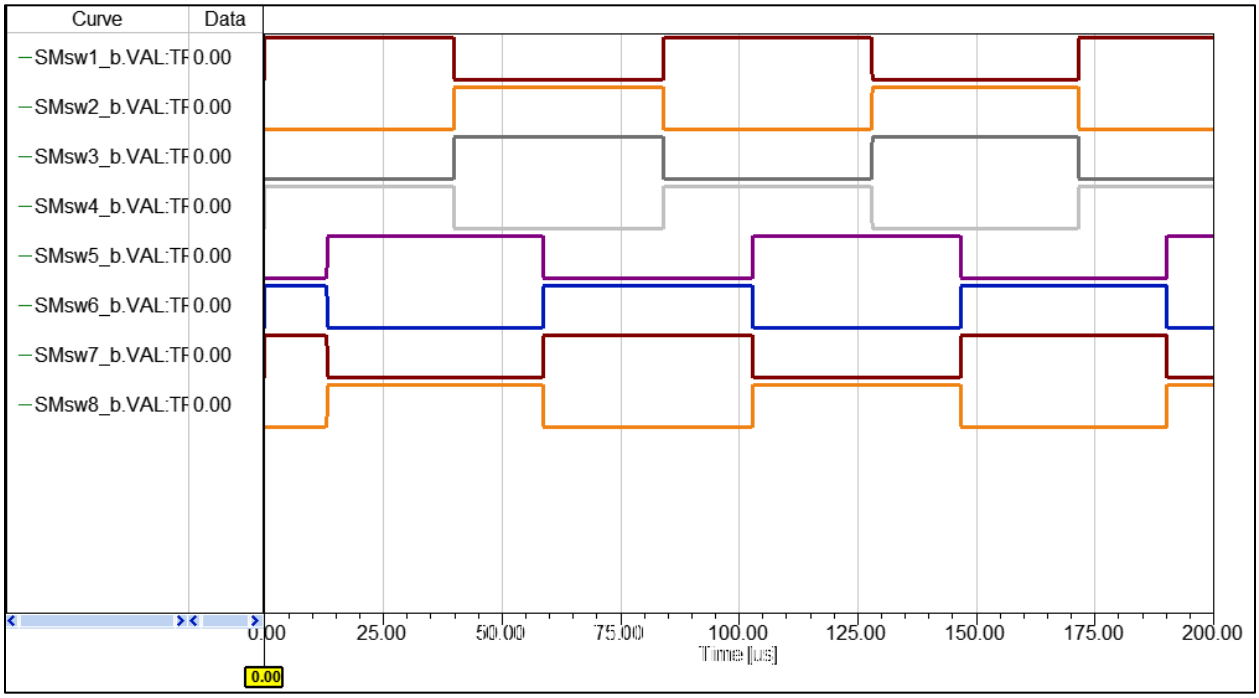


Figure 38: Binary Gate Signals to all Devices Demonstrating Conventional Dual Active Bridge Control with *M4*

4.2 CONTROL MODE WITH SIX SWITCHING SURFACES

Here a strategic mode of switching is presented with capability of extending the range of soft switching operation for the dual active bridge. This work is pioneered by German Oggier and others such as Martin Ordonez and was critical in realizing the contribution presented within this present work [51]–[53]. More information on soft switching will be presented in subsequent section. This six switching surface mode is presented due to its demonstration of the flexibility of NSS. Four of the surfaces employed in this mode are none other than those presented in the

previous section, demonstrated in Figure 26 and Figure 28. The two additional switching structures in boost mode operation are depicted in Figure 39.

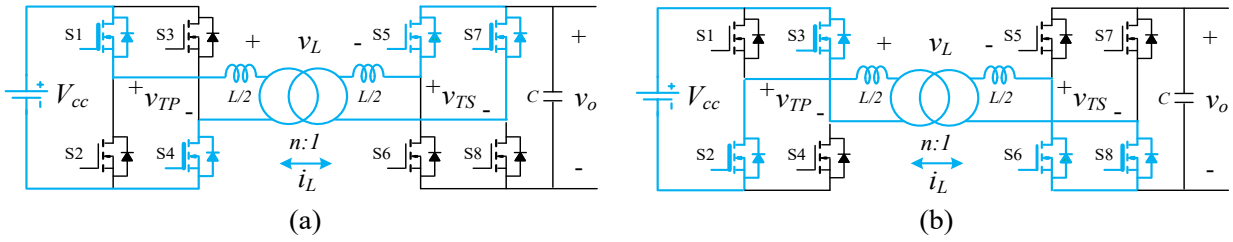


Figure 39: Additional Switching Structures Used in a Mode of Six Strategic Trajectories (*M6*)

In addition to the previously discussed four surfaces, these additional circuit configurations complete the *M6* conceptual state plane depiction as seen in Figure 40 for both the buck and the boost mode.

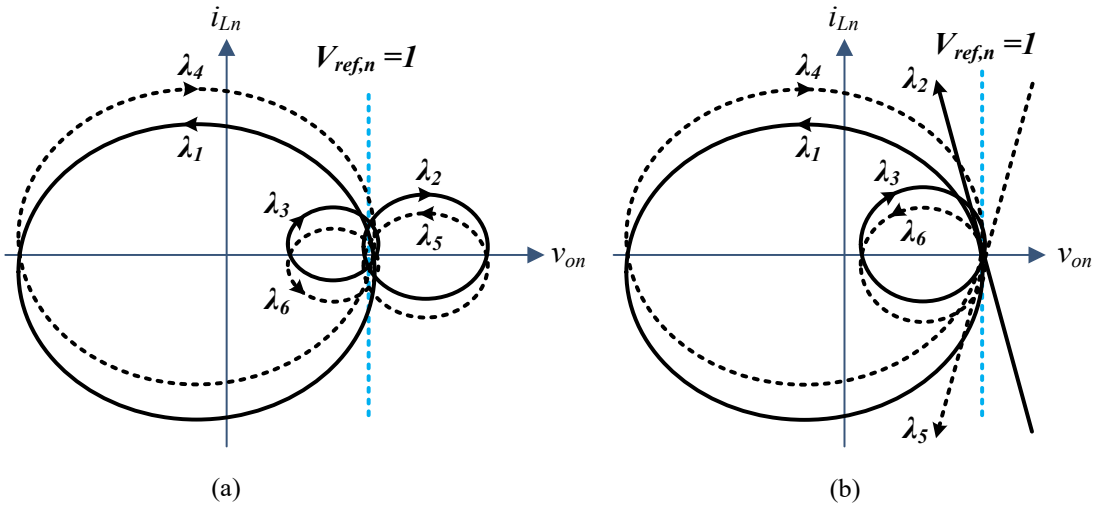


Figure 40: Normalized Natural Switching Surfaces of the Six Trajectory Strategy (*M6*) for buck (a) and boost (b)

Observing the state plane diagrams as a design tool alongside the time domain waveforms brings a unique advantage to the power electronics control engineer. State plane analysis brings an abstract yet intuitive approach to designing control to ones given purpose. The natural trajectories are as in (20) - (22) for buck and boost modes. For buck mode,

$$\lambda_{1,2,3,4,5,6} = (V_{ccn}u_1 - v_{0n}u_2)^2 - \left(i_{Ln,\lambda x} - i_{0n}u_2\right)^2 - (V_{ccn}u_1 - u_2)^2 + (i_{Ln} - i_{0n}u_2)^2 \quad (20)$$

And for boost mode,

$$\lambda_{1,3,4,6} = (V_{ccn}u_1 - v_{0n}u_2)^2 - \left(i_{Ln,\lambda x} - i_{0n}u_2\right)^2 - (V_{ccn}u_1 - u_2)^2 + (i_{Ln} - i_{0n}u_2)^2 \quad (21)$$

$$\lambda_{2,5} = i_{Ln} + v_{0n}\frac{V_{ccn}u_1}{i_{0n}} - i_{Ln,\lambda x} - \frac{V_{ccn}u_1}{i_{0n}} \quad (22)$$

Where i_{Ln} is the transformer current in real time and $i_{Ln,\lambda x}$ is a generalized variable for a target current. A target current is a form of threshold or boundary set to trigger a transition to the next strategic switching surface trajectory of chosen design. These targets will be derived for *M6*

shortly. Values for u_1 and u_2 to differentiate the switching surface (SS) trajectories are provided here in Table 10 and Table 11 and for the associated buck and boost modes.

Table 10: Six Natural Switching Surface Configurations for Buck Mode

SS	u_1	u_2
1	1	-1
2	1	1
3	0	1
4	-1	1
5	-1	-1
6	0	-1

Table 11: Six Natural Switching Surface Configurations for Boost Mode

SS	u_1	u_2
1	1	-1
2	1	0
3	1	1
4	-1	1
5	-1	0
6	-1	-1

The control law, the order of trajectories selected in real time is given in (23).

$$\lambda_1 \rightarrow \lambda_2 \rightarrow \lambda_3 \rightarrow \lambda_4 \rightarrow \lambda_5 \rightarrow \lambda_6 \tag{23}$$

When *M6* is implemented, the electrical waveforms are expected to appear as in Figure 41, a conceptual diagram for explanation purposes.

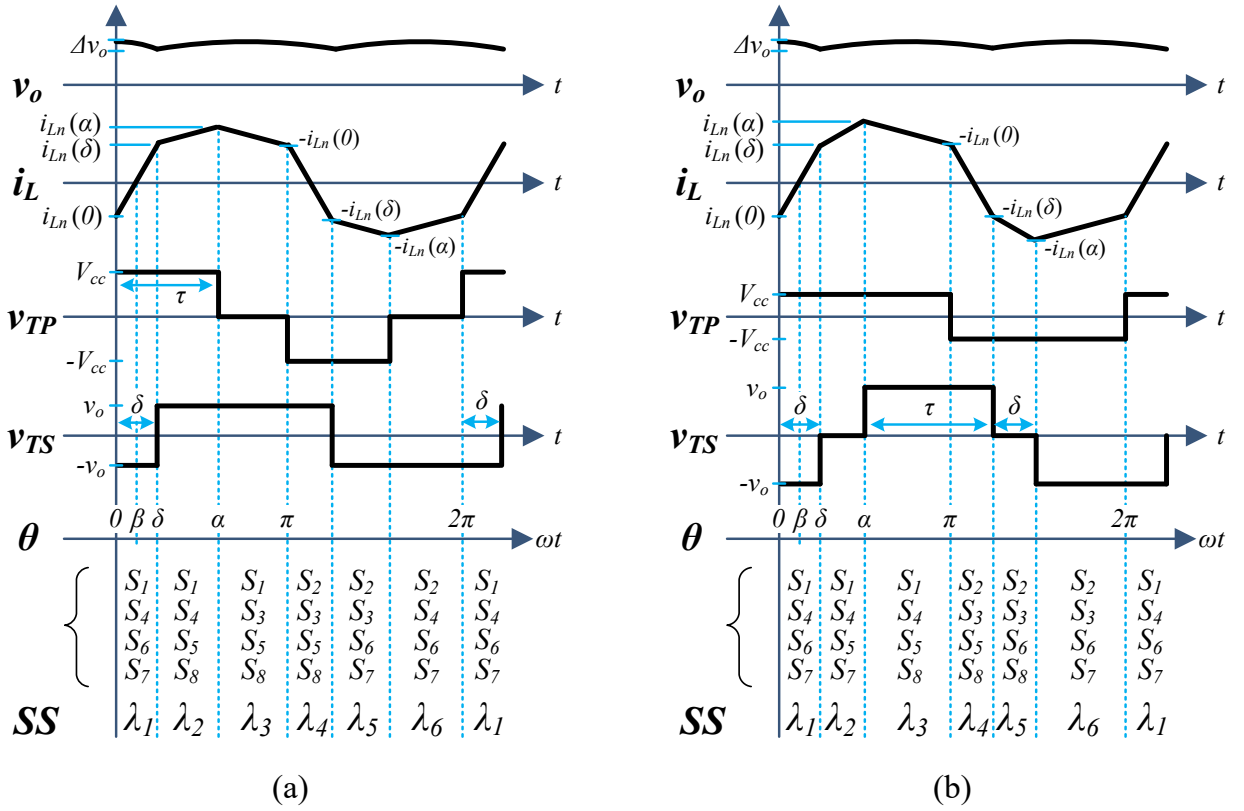


Figure 41: Steady state operating waveforms for the strategic trajectory case study showing (a) buck and (b) boost modes, showing the conducting switches per switching surface (SS)

Each interval of these waveforms is subdivided by angles to differentiate the moments in time that the next set of conducting switches configure. Considering the dual active bridge circuit, the current passing through the transformer inductance can be expressed as in (24).

$$\frac{di_L(t)}{dt} = \frac{v_{TP}(t) - v_{TS}(t)}{L} \tag{24}$$

Solving this equation for the pertinent angles specified in Figure 41, we find the following expressions. For the buck mode in the first three intervals, the current is defined as (25) for ($0 < \theta < \delta$), (26) for ($\delta < \theta < \alpha$), and (27) for ($\alpha < \theta < \pi$), respectively.

$$i_L(\theta) = \frac{V_{cc} + V_o}{\omega L}(\theta) + i_L(0) \tag{25}$$

$$i_L(\theta) = \frac{V_{cc} - V_o}{\omega L}(\theta - \delta) + i_L(\delta) \tag{26}$$

$$i_L(\theta) = \frac{-V_o}{\omega L}(\theta - \alpha) + i_L(\alpha) \tag{27}$$

And for the boost mode in the first three intervals, the current is defined as (28) for ($0 < \theta < \delta$), (29) for ($\delta < \theta < \alpha$), and (30) for ($\alpha < \theta < \pi$), respectively.

$$i_L(\theta) = \frac{V_{cc} + V_o}{\omega L}(\theta) + i_L(0) \tag{28}$$

$$i_L(\theta) = \frac{V_{cc}}{\omega L}(\theta - \delta) + i_L(\delta) \tag{29}$$

$$i_L(\theta) = \frac{V_{cc} - V_o}{\omega L}(\theta - \alpha) + i_L(\alpha) \tag{30}$$

Where L is the transformer equivalent inductance and ω is the angular form of the desired switching frequency f_{sw} ($f_{\text{sw}} = 2\pi/\omega$), a critical design parameter of which more will be discussed as needed. These definitions of transformer current come to specific use in the next section concerning the range of freedom that can be taken to manipulate the control methodology without leaving soft switching operation. For purpose within this section, this analysis leads to evaluating the transformer current at each subdivisional angle.

As seen in Figure 41, the angles $0, \delta, \alpha, \pi$ and so on through 2π mark each transition from one switching surface to another. The transformer current evaluated at each of these angles are the target currents that can be derived to enable a form of modulation with NSS control according to a desired switching frequency. NSS control was originally designed for fast transient response as the objective. Using these target currents for operation with the objective of high efficiency or reliability is a benefit that just so happened to be available with this robust design. As a function of switching frequency, these target currents are given in (31) through (33) for the buck mode [51].

$$i_L(0) = \frac{V_{cc}(d\pi - 2d\delta - m\pi)}{2\omega L} \tag{31}$$

$$i_L(\delta) = \frac{V_{cc}(d\pi + 2d - m\pi)}{2\omega L} \tag{32}$$

$$i_L(\alpha) = \frac{V_{cc}(d\pi + 2d\delta - 2dm\pi + m\pi)}{2\omega L} \tag{33}$$

And for the boost mode in (34) through (36).

$$i_L(0) = \frac{V_{cc}(dm\pi - 2d\delta - \pi)}{2\omega L} \tag{34}$$

$$i_L(\delta) = \frac{V_{cc}(dm\pi + 2\delta - \pi)}{2\omega L} \tag{35}$$

$$i_L(\alpha) = \frac{V_{cc}(dm\pi + 2\delta - 2m\pi + \pi)}{2\omega L} \tag{36}$$

Where *m* is the modulation index specific to *M6* thus far, and *d* is the voltage conversion ratio. For a full cycle through 2π, transformer current target definitions beyond α as they appear on Figure 41 consist of the negation of previous definitions. Conceptually, this makes sense due to the fact that the average value of i_L must be zero, assuming steady state conditions.

$$i_L(\pi) = -i_L(0) = -\frac{V_{cc}(dm\pi - 2d\delta - \pi)}{2\omega L} \tag{37}$$

$$i_L(\pi + \delta) = -i_L(\delta) \tag{38}$$

$$i_L(\pi + \alpha) = -i_L(\alpha) \tag{39}$$

Translated into target definitions for the *M6* strategy, the following results. These are expressed here for the boost mode only, since for the majority of this research the boost mode is focused upon. Each target marks the entrance into the labeled switching surface (λx).

$$i_{L,target,\lambda_1} = i_{L\lambda 1} = i_L(0) = \frac{V_{cc}(dm\pi - 2d\delta - \pi)}{2\omega L} \tag{40}$$

$$i_{L\lambda 2} = i_L(\delta) = \frac{V_{cc}(dm\pi + 2\delta - \pi)}{2\omega L} \tag{41}$$

$$i_{L\lambda 3} = i_L(\alpha) = \frac{V_{cc}(dm\pi + 2\delta - 2m\pi + \pi)}{2\omega L} \tag{42}$$

$$i_{L\lambda 4} = -i_L(0) \tag{43}$$

$$i_{L\lambda 5} = -i_L(\delta) \tag{44}$$

$$i_{L\lambda 6} = -i_L(\alpha) \tag{45}$$

These definitions are normalized according to (46).

$$i_{Ln\lambda x} = i_{L\lambda x}\left(\frac{Z_0}{V_{ref}}\right) \tag{46}$$

By manipulating the degrees of freedom provided inherently with NSS, these target currents can be defined for a desired switching frequency. These control handles are ultimately parameters *m* and δ found within in these definitions. More on that in the subsequent subsection 4.3.

It is noteworthy that the described modifications would require current sensors on the primary and secondary of the DAB transformer. This is not a significant hindrance of the control methodology though because sensing is becoming less expensive as time goes on and more

importantly because there are an ever-increasing number of benefits of including additional sensing in power converters, e.g. NSS control.

4.2.1 Simulation Example for the Six Trajectory Mode

Provided here is validation for the NSS six trajectory control methodology, *M6*. Given the ratings of the system given in Table 12, the case is a medium loading condition. With *M6* operation the system can operate with faster transient performance and higher efficiency. The following plots are simulation results achieved in the ANSYS software package.

Table 12: Parameters for Validation Simulation for Six Trajectory Mode

Parameter:	Value:	Description
M	*M6*	Mode of strategic trajectories
P_o	3.6kW	Output power demanded
V_{cc}	120	Input voltage
V_o	240	Output voltage (V_{ref})
d	$V_o/(nV_{cc})$	Conversion ratio (n = 1.5)
f_{sw}	10kHz	Switching frequency
m	0.5	Modulation index

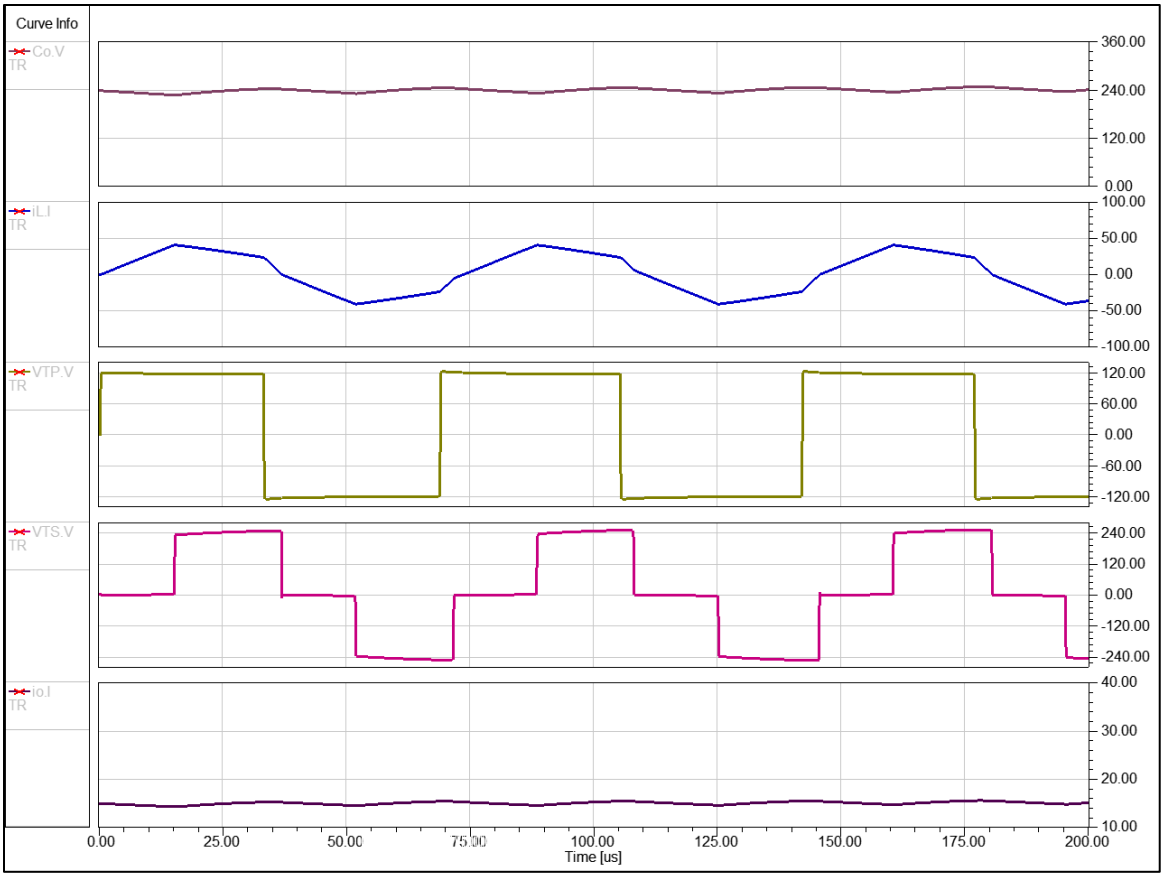


Figure 42: Results of output voltage, transformer current, primary and secondary voltage, and output current in *M4*

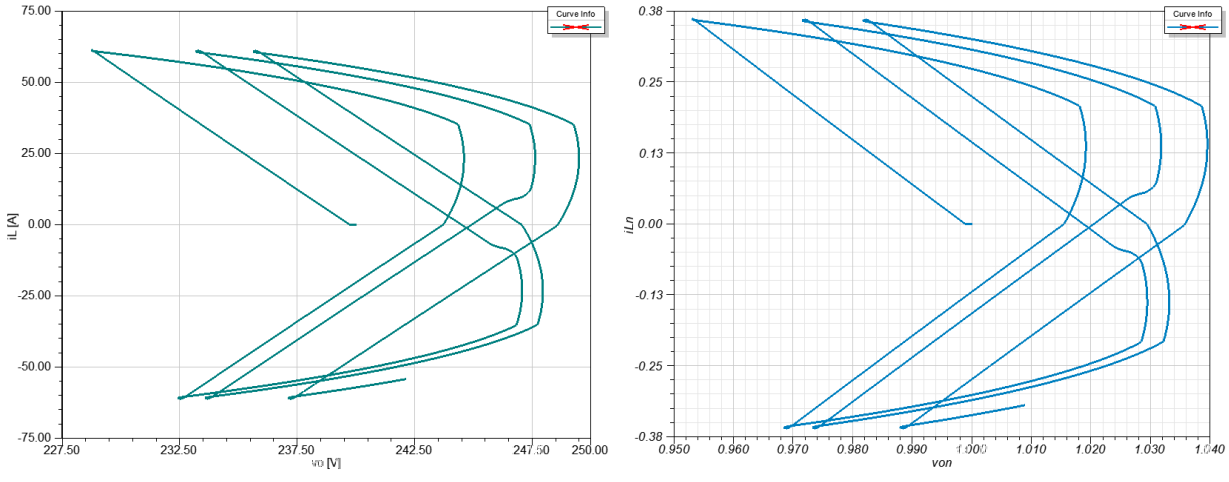


Figure 43: State plane results, both normalized and not, for *M6* operating under medium loading

4.3 DEGREES OF FREEDOM AND PARAMETER SELECTION

There are particular degrees of freedom possible with natural switching surface (NSS) control enabling fast transient performance. These are m and f_{sw} specifically. The flexibility and limitations on these freedoms are provided within this section. NSS has a significant benefit of fast transient performance due to an increased capability of soft switching over a significant portion of the converter's range of operation [43]. These ranges are specified through δ, the phase shift of voltage from primary to secondary sides of conversion. This section will provide the control limits determining the range of said soft switching region, also known as zero voltage switching.

Operating the DAB with soft switching is constrained by achieving the self-defined zero voltage switching. Provided in terms of the previously discussed NSS theory, soft switching is possible when the following criteria are satisfied (47), (48) [51].

$$i_L(\delta) > 0 \tag{47}$$

And

$$i_L(\pi) > 0 \tag{48}$$

For the primary and secondary bridges of the DAB, respectively. These condition are satisfied over the full range of operation only when $d = 1$ [45], [53].

Recall from Section 4.2 the expressions of transformer current given for each portion of a full cycle of current provided in equations (28) through (33). When evaluating (47) and (48) using

these expressions of the transformer current for each time interval, limitations upon the phase shift δ can be determined. For the buck mode, the limitations for the primary and secondary bridges are evaluated as in (49) and (50).

$$\delta > \frac{\pi}{2}(m - d) \tag{49}$$

$$\delta > \frac{\pi}{2}\left(1 - \frac{m}{d}\right) \tag{50}$$

And when operating in boost mode for the primary and secondary bridges as in (51) and (52).

$$\delta > \frac{\pi}{2}(1 - dm) \tag{51}$$

$$\delta > \frac{\pi}{2d}(dm - 1) \tag{52}$$

Such modes are modified by the desired switching frequency and the modulation index applied to the high side of the transformer. The present case study defines the strategic modes based upon how much power is demanded in real time, altering the control to optimize efficient operation with every load change.

Nonetheless, the degrees of freedom associated with f_{sw} and m have their own limits. In its essence, m effects a resulting phase shift between bridges, where the phase shift is the critical variable for power transfer in a DAB converter design. The limits upon the manipulation of m are as follows [51]. First of all, the maximum is a value of one by definition of a modulation index, and secondly there is a minimum m value bound by providing the necessary output power demanded as well as the voltage conversion ratio for a given converter design.

$$m_{min} < m < 1 \tag{53}$$

Where,

$$m_{min} = 1 - \frac{\sqrt{(V_{cc}d\pi)^2 - 4P_o d\omega L\pi}}{V_{cc}d\pi} \tag{54}$$

Even further, the DAB will only operate with soft switching if within the following additional upper (u) and lower (l) limits (55).

$$m_{min} < m_l < m < m_u < 1 \tag{55}$$

Where,

$$m_u = 1 - \frac{\sqrt{(V_{cc}\pi)^2(d^2 - 1) - 4P_o d\omega L\pi}}{V_{cc}\pi d} \tag{56}$$

$$m_l = \frac{\left((V_{cc}\pi d)(2 + d) + \sqrt{2\pi d(V_{cc}^2\pi d^2(1 + d) - 2aP_o\omega L)}\right)}{V_{cc}\pi da} \tag{57}$$

Where $a = 1 + 2d + 2d^2$ or $a = 2 + 2d + d^2$ for buck or boost modes of operation respectively. These calculations enable the engineer with designing NSS control according to desired operation. Within these limitations, m is a significant control handle for *M6*.

The controllable handle for the two additional switching trajectories in *M6* is the variable τ, the width of the modulated voltage value (+ / -). The variable τ is determined in terms of π and the modulation index in (58) according to previous definitions of *m*.

$$m = \frac{\tau}{\pi} \quad \rightarrow \quad \tau = \pi m \tag{58}$$

Therefore the limits of τ are given in (59).

$$\pi m_{min} < \tau < 1 \tag{59}$$

To operate these additional trajectories as an aid to remain in soft switching operation, this range of inequality can be adapted accordingly as in (60).

$$\pi m_l < \tau < \pi m_u \tag{60}$$

Regarding the limitations upon the desired switching frequency for operation of a dual active bridge, generally its maximum comes from device switching losses where increased f_{sw} results in more switching loss. While on the other hand its minimum would derive from maximum transformer magnetizing current. The magnetizing current is function of the *B-H* loop for the magnetic core, where the magnetizing current increases faster than induction. Core induction, *B*, has an inversely proportional relationship with switching frequency. Core loss will increase with f_{sw} while induction will decrease by a squared ratio [44]. Therefore, changing f_{sw} can also particularly impact transformer core losses, where total transformer losses, including eddy current and hysteresis losses, will decrease with increased switching frequency. Yet, it is of note that the resulting reduction in magnetizing current is by greater proportion than the reduction of core losses due to material properties. In the end, a higher switching frequency within reasonable limits will result in lower losses and lower magnetizing current. This comes as an operational benefit of the dual active bridge design with regards to efficiency and correlated heating. For the contribution of this work, increased switching frequency resulting in less heat generated by core losses is of note. Nonetheless, the research presented here, does not address the heat generated by the transformer when considering thermal cycling. For the scope of this work, heat generated by switching and conduction losses are considered within the electro-thermal modeling of devices. The only considered heat is the calculated junction temperature from said losses.

With taking into account each of these limitations, NSS control manipulation still has much flexibility at the disposal of the designer. All simulation designs of this work take these limitation into account and watch whether or not the designs operate with soft or hard switching. With that, operating in soft switching is not a critical aspect of the contribution of this work. What is helpful

here, is to grasp the limitations of altering the discussed degrees of freedom for the benefit of reduced thermal cycling, preserving the life of the power electronics.

To operate the dual active bridge at high efficiency and to utilize the full operating range, parameter selection is important as well as the handling of its degrees of freedom. With regards to selecting parameters for a DAB design, a few items need to be addressed. A switching frequency per power range should be selected as according to previous discussions within reasonable limits and with general protocol of lower f_{sw} for heavy load and higher f_{sw} for light load. This selection is linked to operating the converter in throughout more of its power operating range. The previously presented *M4* and *M6* are best suited to heavy loading and medium loading, respectively, as will be seen in the following case studies. The M6 is particularly helpful in extending the operating range and minimizing conversion losses due to the modulation factor enabling soft switching in an extended range, discussed further here [50]–[53]. When operating *M6*, an optimal modulation index can be determined with the aid of a developed algorithm found in [51]. This algorithm determines *m* within the restrictions of a required output power and the set conversion ratio (*d*). This determination of *m* will enable the DAB to transfer output power with minimum losses. On another note, the voltage conversion ratio should be selected within an approximate range of 0.9 and 1.5 for best DAB operation. This ratio is determined by the input and output voltages, V_{cc} and V_{ref}, for a given design coupled with an associated turns ratio, *n,* to achieve the step change in either the buck or boost mode of operation. In the design of the dual active bridge, the turns ratio and input and output voltage are to be chosen to determine the desired conversion ratio, $d = V_{ref}/(nV_{cc})$. With these design considerations addressed, let us now consider a case study of incorporating NSS control in a design for efficient operation over a large DAB operating range.

4.4 CASE STUDY OF BOUNDARY CONTROL FOR EFFICIENCY

A natural switching surface control methodology has been strategically designed for the sake of improved operational efficiency of the dual active bridge in [44]. In this work, differing modes of NSS control were utilized and designed for light, medium, and heavy loading conditions for improved efficiency of approximately 1% increase across the modes. For light load conditions, a burst mode was designed specifically manipulating said degrees of freedom. This case study is addressed here for two purposes. First, such an application familiarizes one with the degrees of freedom associated with NSS control in action. Second, this application among a few others germinated the contribution of this dissertation, to utilize the capabilities of boundary control methodology for strategic design with an end purpose in mind.

This case study incorporates a burst mode (*BM*) trajectory in addition to the four trajectory (*M4*) and the six trajectory (*M6*) modes previously presented in Sections 4.1 and 4.2. The three different modes are enabled for differing loading conditions, where each pairing improves efficiency, implementing *M4*, *M6*, and *MB* for each loading condition of heavy, medium and light loading, respectively. This burst mode successfully eliminates excessive switching in light loading conditions, saving on both switching and conduction losses. Modes *M4* and *M6* also improve upon operational efficiency due primarily to the controllability of switching frequency for varying load conditions and expanding the range within which the DAB can perform soft switching but also due to the faster transient performance featured by NSS control. The theoretical background presented here builds upon the theory presented thus far.

4.4.1 Efficient Burst Mode Design for Operation during Light Loading

When light loading exists, very little current is required in order to maintain rated output voltage and the demanded power. In [44], the authors found an opportunity here for more efficient operation. Instead of constantly running a small amount of current, small bursts of current were performed where all devices are turned off in between bursts. This burst mode was found sufficient for proper operation and cut on device losses and ultimate efficiency of the converter.

The burst mode (*MB*) is practically achieved when switching surfaces λ_1 and λ_4 of the boost mode *M6* progression as seen in Table 13 are swapped out for zero states. These zero states imply that all devices are literally turned OFF, not simply that there is zero power being delivered to the output capacitor and load. Zero power output can in fact be achieved with switches turned ON for a 'zero' trajectory – where u_1 and u_2 both equal zero. More on that later. For the burst mode, values for u_1 and u_2 are provided here to differentiate the switching surface (SS) trajectories for the six natural switching surfaces of *MB*. See Table 14 for the switching voltage progression of *MB*. Recall that $u_1 = 1, -1$ as nomenclature for $V_{cc} = 1, -1$ and $u_2 = 1, -1$ for $v_o = 1, -1$.

Table 13: Six Natural Switching Surface Configurations for *M6*

SS	u_1	u_2
1	1	-1
2	1	0
3	1	1
4	-1	1
5	-1	0
6	-1	-1

Table 14: Six Natural Switching Surface Configurations for Burst Mode (*MB*)

SS	u_1	u_2
1	0	0
2	1	0
3	1	1
4	0	0
5	-1	0
6	-1	-1

Combining Table 14 with previously provided Table 8 and Table 11, all modes of NSS operation are accounted for regarding the pertinent case study. All three modes are summarized in Table 15 for convenience of comparison, clarity and analysis. Each mode is ordered in its respective control law sequence. This table also allows for translation analysis of the overlap between modes of designed operation with the utilized trajectories listed. Note that these are not all of the possible trajectories but simply the possible trajectories utilized.

Table 15: Modes of Natural Switching Surface Trajectories Summarized for Efficiency Case Study

Possible	*M4*			*M6*			*MB*		
Trajectories	SS	u_1	u_2	SS	u_1	u_2	SS	u_1	u_2
I							λ_1	0	0
II	λ_1	1	-1	λ_1	1	-1			
III				λ_2	1	0	λ_2	1	0
IV	λ_2	1	1	λ_3	1	1	λ_3	1	1
V	λ_3	-1	1	λ_4	-1	1			
VI							λ_4	0	0
VII				λ_5	-1	0	λ_5	-1	0
VIII	λ_4	-1	-1	λ_6	-1	-1	λ_6	-1	-1

To achieve these surfaces in Table 14, switching surface λ_1 configures all switches OFF (S_{OFF}), λ_2 employs switches $S_{1,4,5,7}$, $\lambda_3 - S_{1,4,5,8}$, $\lambda_4 - S_{OFF}$, $\lambda_5 - S_{2,3,5,7}$, $\lambda_6 - S_{2,3,6,7}$. The normalized targets determined for transition between each specified switching configuration, are as follows.

$$i_{Ln,\lambda 1} = 0 \tag{61}$$

$$v_{on,\lambda 2} = \left(\frac{v_o - V_{o,min}}{V_{ref}}\right) = 1 - V_{on,min} \tag{62}$$

$$i_{Ln,\lambda 3} = \frac{V_{cc}(dm\pi + 2\delta - 2m\pi + \pi)}{2\omega L}\left(\frac{Z_0}{V_{ref}}\right) \tag{63}$$

$$i_{Ln,\lambda 4} = i_{Ln,\lambda 1} = 0 \tag{64}$$

$$v_{on,\lambda 5} = v_{on,\lambda 2} \tag{65}$$

$$i_{Ln,\lambda 6} = -i_{Ln,\lambda 3} \tag{66}$$

Where $V_{on,min}$, the normalized minimum permissible voltage, can be set by the designer to whatever amount of output voltage ripple is desired. Each of these switching surface targets have associated transition criteria for when operation should move from one trajectory to the next. These criteria are provided in Figure 44. Primarily demonstrated by Figure 44 is the overall control design of the efficiency case study summarized in a decision flowchart, demonstrating the relationship among the modes of operation and their associated loading level.

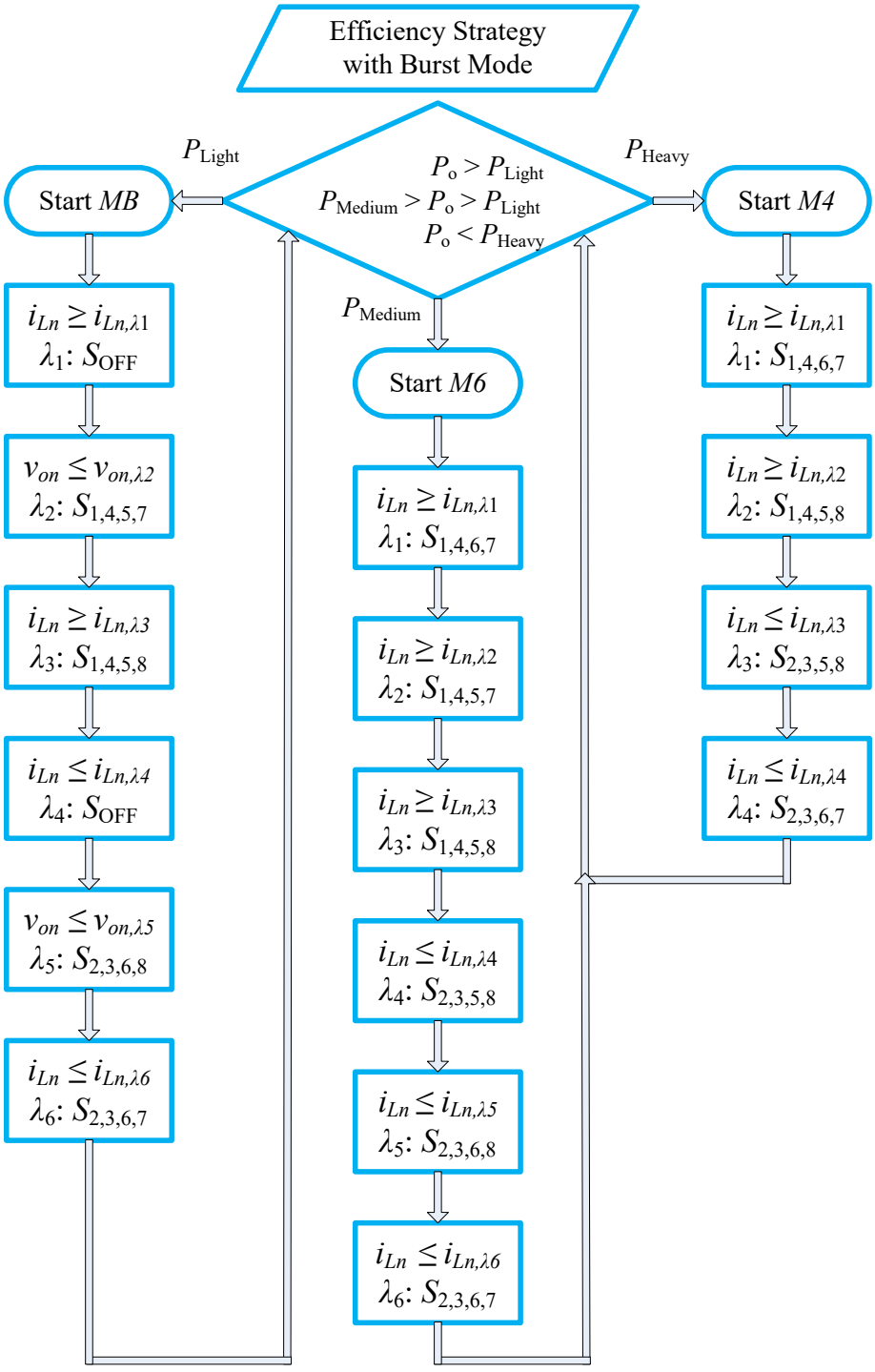


Figure 44: Flowchart Summarizing the Control Operation of *MB* Coupled *M4* and *M6* for Efficient Operation

4.4.2 NSS Burst Mode Case Study Results

All three of the presented strategic trajectory modes are validated in simulation using ANSYS Simplorer. The simulated parameters for this validation are provided in Table 16. More information regarding the selection of these parameters are provided further on in the document, when setting up validation and comparisons for the contribution of this dissertation. For now, the parametric information on its own will have to suffice.

Table 16: Parameters for Efficiency Case Study Simulation Implementing Three Strategic Modes

Parameter:	Value:	Description
M	[*MB, M6, M4*]	Modes of strategic trajectories
P_o	[600W, 3.6kW, 7.2kW]	Output power demanded
V_{cc}	120	Input voltage
V_o	240	Output voltage (V_{ref})
d	$V_o/(nV_{cc})$	Conversion ratio (n = 1.5)
f_{sw}	[10kHz, 10kHz, 4kHz]	Switching frequency per mode
m	[0.1, 0.5, 1.0]	Modulation index per mode

The simulation results for this efficiency case study are presented in Figure 45 and Figure 46. Included in Figure 45 are the waveform signals v_o, i_L, v_{TP}, v_{TS}, and i_o stacked from top to bottom. Figure 46 provides the normalized state plane in its totality for the duration of the simulation across all three modes (top left), as well as broken down for clarity of operation into each mode *MB, M6,* and *M4* from left to right and top to bottom.

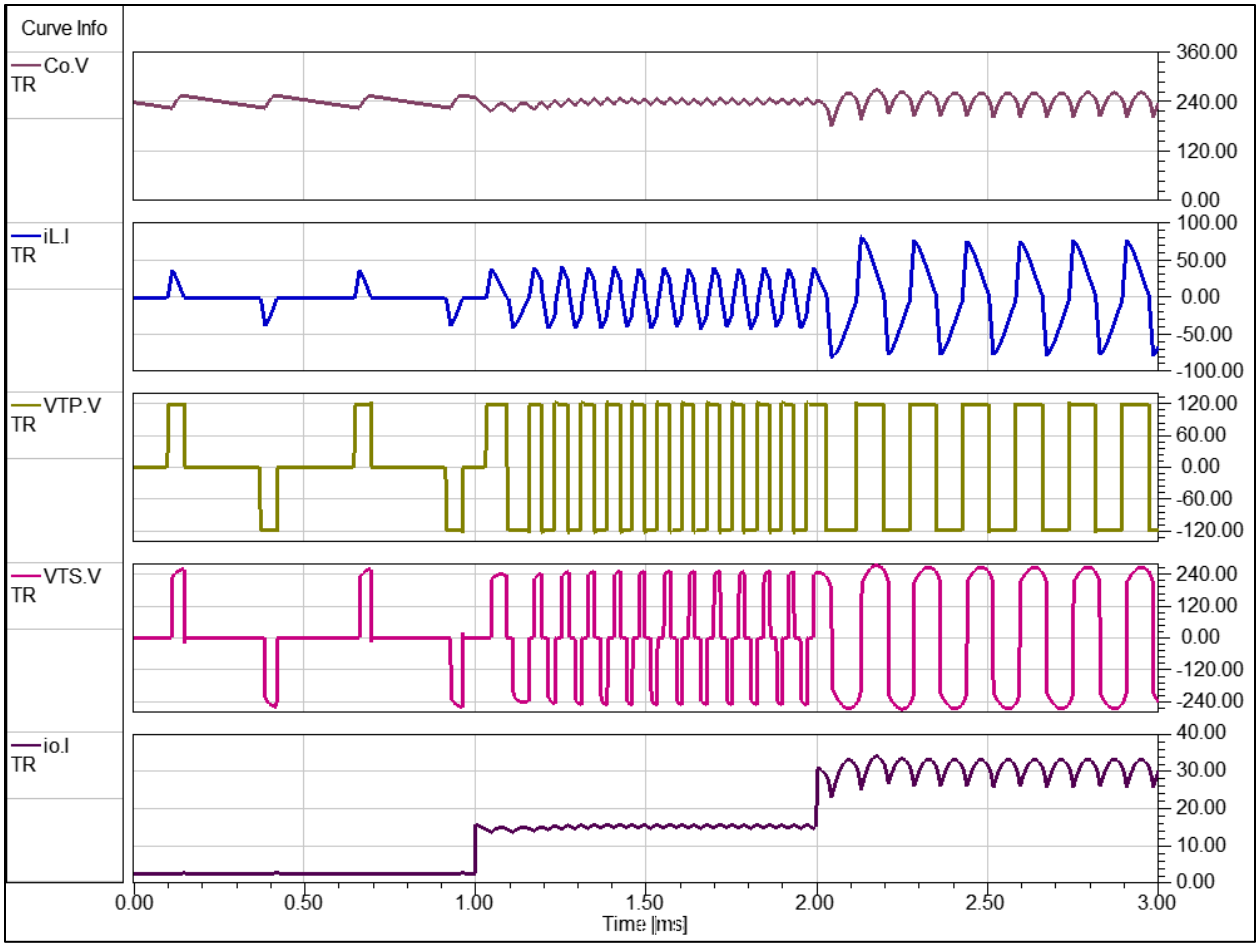


Figure 45: Outputs of Efficiency Case Study Performing Three Strategic Modes for Three Levels of Power Demand

Note the minimal current being produced during *MB* and yet, the demanded output is nonetheless satisfied. These results are reproduced from the work presented in [44]. Thanks to the normalization of design, this is a more seamless process.

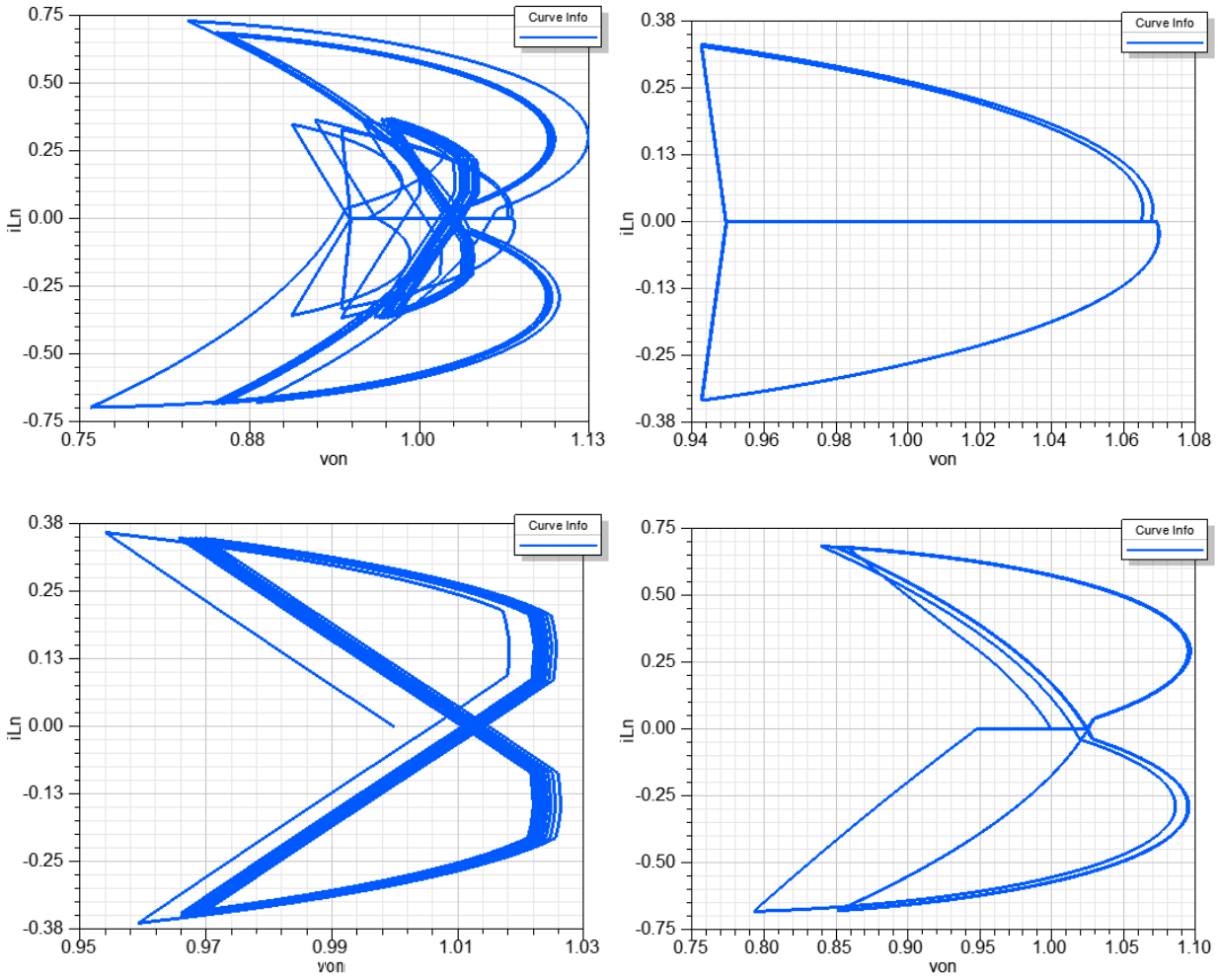


Figure 46: State Plane for Efficiency Case Study, in total and divided into differing modes *MB, M6,* and *M4*

One can see the consistency between the normalized state plane and the previous output waveforms for output voltage and transformer current. Notice the added trajectories from *M4* to *M6* as has already been theoretically described and depicted conceptually in Sections 4.1 and 4.2 and particularly in Figure 30. Seeing the resemblance of MB to its state plane is simpler since in essence there are simply bursts of current on repetition in opposite current directions.

5.0 BOUNDARY CONTROL AS ACTIVE THERMAL CONTROL

Employing natural switching surface control as a means to an end, a modulation technique is presented in this section for interval based loads, to preserve the reliability of the dual active bridge. Boundary control is used to actively control junction temperature dynamics by controlling conduction losses. Utilizing the previously described degrees of freedom (Section 4.3) with additional boundaries determined enables reduction of thermal cycling, implementing a form of active thermal control (ATC). As an example, when the current target magnitudes decrease an increase of the pseudo switching frequency will result, and vice versa. Also, a decrease of targets reduces the magnitude of current conduction and vice versa. These current targets placed upon the state plane as geometric boundaries can be informed by a power loss estimation technique similar to what is performed in [22]. In contrast to exclusively the ATC method of variation of the switching frequency as proposed in [22] or many other forms of ATC [21], the proposed method introduces the utilization of boundary control designed through state-plane analysis to reduce thermal cycling during interval based loads. The feedback of this control is implemented through measurement of voltage and current on the output. Such measurements are more costly and complex for converter design, but this is not a significant hindrance partially due to sensing becoming less expensive as time goes on and more importantly because there are an ever-increasing number of benefits of including additional sensing in power converters, e.g. NSS control capability and benefits. The method proposed effectively shepherds the desired conduction and heating to reduce thermal cycling in light loading conditions in addition to achieving zero voltage switching gains through natural switching surface control enabling a wider operating range for the dual active bridge. The method provides design flexibility and applicability to various topologies with appropriate design measures.

Increased reliability by ATC hinges upon added losses keeping the devices hot so that thermal cycling amplitudes are minimized. With the work in [44] decreasing losses for successful efficiency improvement, the design in this work is adapted in reverse by altering the switching surface trajectory strategy for increasing losses in light loading conditions and ultimately for life preservation by ATC.

A mode of NSS switching trajectories is designed for life preservation during the light loading of an interval based load. The design circulates current through the devices without charging the output capacitor or feeding the load more than is required during said light loading. The circulating current adds conduction loss desirably maintaining temperature on devices when cooling would accelerate device degradation. Coupling a circulating conduction mode of operation (*MC*) with the *M4* and *M6* strategies, an overall design for the full operating range of the dual active bridge is proposed for life preservation. This coupling of modes brings added efficiency in the medium and heavy loading conditions with reduced thermal cycling amplitudes over time when alternating to and from lighter load conditions. For any applications that expects or at least can predict periods varying load conditions, such a design would be of benefit for reliability of the power conversion systems.

Active thermal boundary control includes three modes of operation, incorporating newly designed life preservation mode (*ML*) in addition to the four trajectory (*M4*) and the six trajectory (*M6*) modes previously presented in Sections 4.1 and 4.2. Life mode is the strategic mode of NSS trajectories designed for improved reliability.

5.1 TRAJECTORY STRATEGY DESIGN FOR LIFE PRESERVATION

In order to preserve the lifetime of power cycling, the proposed control effectively minimizes thermal cycling on the junction of the device. This minimization is achived by keeping the devices from cooling down. In order to keep devices warm, heat is generated. From the domain of power electronics control, either switching or conduction loss could serve this purpose. Increased switching frequency would provide increased switching loss for heat. Higher magnitudes of conducting current for relatively long durations would increase conduction loss for heat. And yet, these approaches would often be mutually exclusive in power conversion design. Generating heat is especially hard during light loading conditions due to the low levels of current required by the load. The challenge here is that it is precisely at light loading that we need to prevent devices from cooling. Pertinent to the dual active bridge, transformer core losses also generate heat. Magnetizing current and core losses are in fact inversely proportional to switching frequency where an increase of switching frequency will reduce magnetizing current and core losses. On the other hand, condution and core losses would naturally be directly proportional. With these heating factors considered, the following key thoughts guided the realization of the proposed solution.

- Keep the devices hot through varied load conditions to minimize long-term thermal cycling
- NSS control offers design flexibility and inherently entails condition monitoring
- Circulating current through devices without delivering the full amount of power to the load
- Design a mode of strategic trajectories to achieve such circulation for life preservation

Note that the concept of circulating current without delivering said current is inspired from other active thermal control work where parallel inverters effectively circulated reactive current among themselves without delivering it to the grid [21]. By this technique thermal cycling was minimized.

To achieve an outcome from these key thoughts, the design process of the proposed life preservation strategy (*ML*) started from the burst mode strategy (*MB*) from [44] as its origin. This is the point at which state plane analysis serves its purpose. Analyzing *MB* operation as seen in Figure 47(a) within the context of the *M6* natural switching surfaces as seen in Figure 47(b), revealed a strategic combination for added current. If switching surfaces λ_1 and λ_4 of Figure 47(a) could be replaced with trajectories that are non-zero current we would be making progress. This observation led to the initial design step to borrow trajectories λ_2 and λ_5 from *M6* and replace trajectories λ_1 and λ_4 of the *MB* operation as seen to be superimposed from Figure 47(b) to Figure 48. The same is demonstrated in Table 17. These additional trajectories pass current through device pairs of S5,7 or S6,8 on the secondary side achieving zero voltage on the output for the duration of the switching configuration. Simply making this swap of trajectories did cause an incremental increase of transformer current, but this does not fully realize the substantial circulating current desired for heating purposes. As demonstrated conceptually in Figure 48, there will simply be twice as many bursts of current per cycle and will be reversing current for every burst. Even with that, there is no elegant control handle to manipulate duration of circulating current. Increased control flexibility is left to be desired.

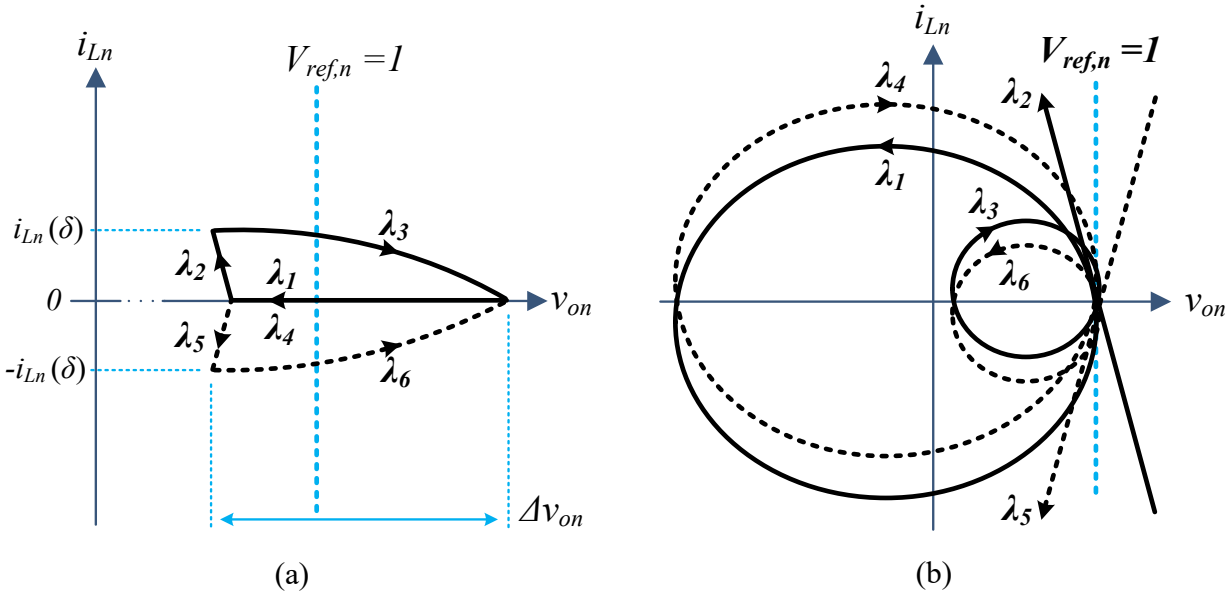


Figure 47: Conceptual diagrams of *MB* in operation (a) and the natural switching surfaces of boost mode (b)

Table 17: Switching Surface Alterations for Initial Step in Designing Life Preservation Mode

M6			*MB*			*MB**		
SS	u_1	u_2	SS	u_1	u_2	SS	u_1	u_2
1	1	-1	***1***	***0***	***0***	***1***	***-1***	***0***
2	***1***	***0***	2	1	0	2	1	0
3	1	1	3	1	1	3	1	1
4	-1	1	***4***	***0***	***0***	***4***	***1***	***0***
5	***-1***	***0***	5	-1	0	5	-1	0
6	-1	-1	6	-1	-1	6	-1	-1

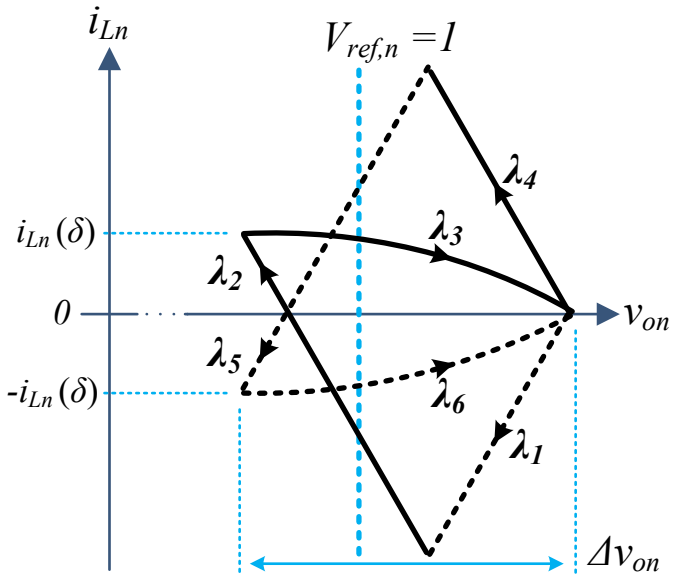


Figure 48: Conceptual State Plane Result of Modified *MB* for Increased Conduction Loss

The next step in the design process was to fully realize a controllable circulating current trajectory. This was ultimately achieved by adding two additional switching surfaces to the modified strategy (*MB**) one at the point between trajectories λ_1 and λ_2 as well as one between λ_4 and λ_5, resulting with an 8 trajectory strategy. These additional surfaces are 'OFF' states realized by the dual active bridge switching configurations depicted in Figure 49. In order to achieve these 'OFF' states, all switches are not simply turned off until the next state as is done for the original *MB*. The label 'OFF' simply substitutes for the output of the converter being off. In other words, power is not being delivered to the output capacitor during such a switching configuration. Adding 'OFF' states in this situation enables circulating currents to flow by strategic switching surface selection. The resulting mode of strategic trajectories is summarized in Table 17 and conceptually depicted on the state plane in Figure 50 with associated waveforms depicted in Figure 51.

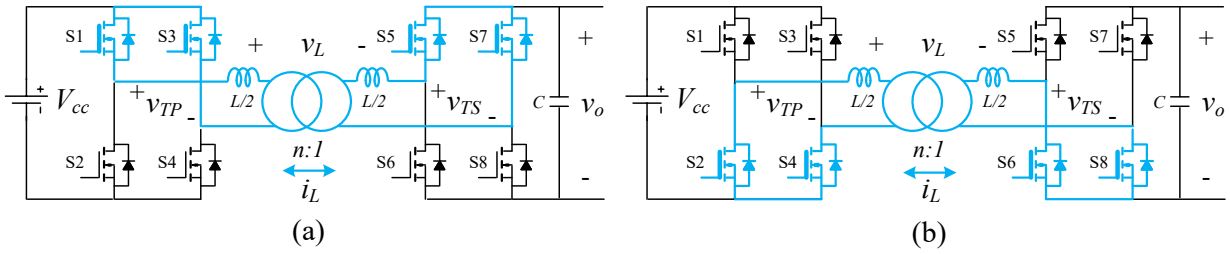


Figure 49: Switching Configurations for λ_4 (a) and λ_8 (b) of Life Mode Design Realizing Circulating Conduction

Table 18: Eight Natural Switching Surface Configurations for Life Preservation Mode (*ML*)

SS	u_1	u_2
1	1	0
2	1	1
3	1	0
4	0	0
5	-1	0
6	-1	-1
7	-1	0
8	0	0

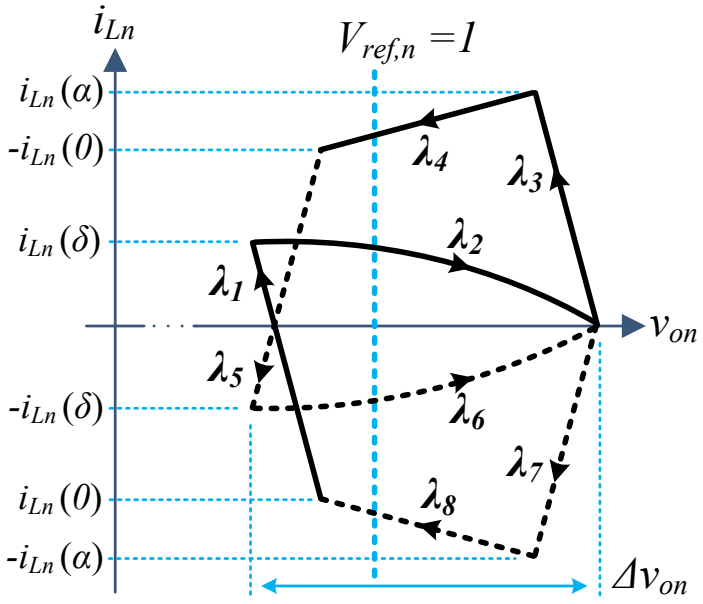


Figure 50: Conceptual State Plane of Life Preservation Mode Final Design in Boost Operation

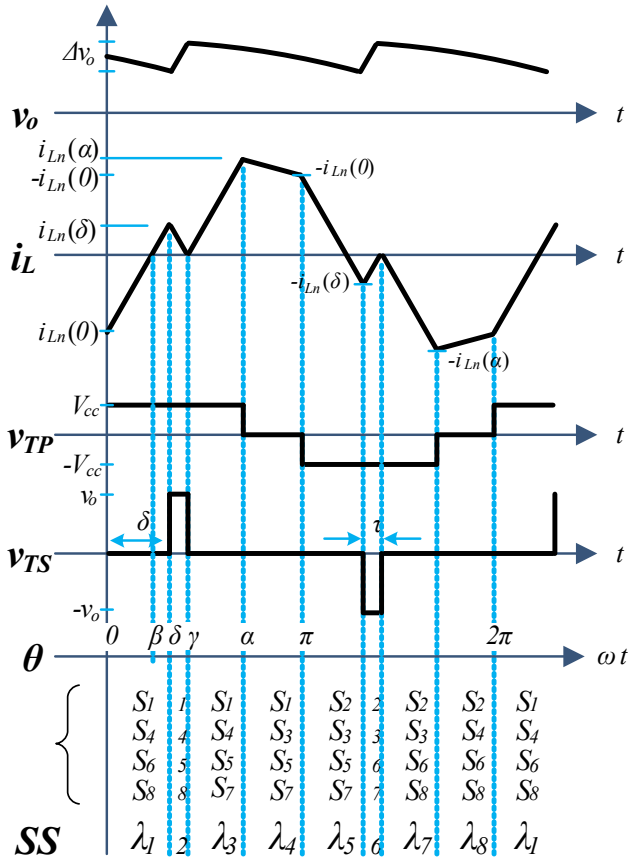


Figure 51: Steady state operating waveforms for life preservation mode, showing the conducting switches per switching surface (SS) in the boost operation

These trajectories bring about the sustained conduction losses desired for additional heat on the junction of the devices. Note also that between both of the circulating current switching surfaces, λ_4 and λ_8, every device of the DAB is utilized, balancing the amount of current among devices. This balancing is critical for system reliability, so that heating would not occur on some devices more than others. Respective to each circulating current switching surface, λ_4 utilizes $S_{1,3,5,7}$ while λ_8 utilizes $S_{2,4,6,8}$. Similar strategic balancing is performed for the other repeated pairs of switching surfaces λ_1, λ_3 and λ_5, λ_7. The zero state on the secondary is achieved with balanced device use, where λ_1 utilizes $S_{6,8}$, λ_3 utilizes $S_{5,7}$, λ_5 utilizes $S_{5,7}$, and λ_7 utilizes $S_{6,8}$.

In their normalized form, the targets designed for each trajectory are as follows.

$$i_{Ln}(0) \rightarrow v_{on,\lambda 1} = \left(\frac{v_o - V_{o,min}}{V_{ref}}\right) = 1 - V_{o,min}\% = 1 - 2\% = 98\% \tag{1}$$

$$i_{Ln}(\delta) = i_{Ln,\lambda 2} = \frac{V_{cc}(dm\pi + 2\delta - 2m\pi + \pi)}{2\omega L}\left(\frac{Z_0}{V_{ref}}\right) \tag{2}$$

$$i_{Ln}(\gamma) = i_{Ln,\lambda 3} = 0 \tag{3}$$

$$i_{Ln}(\alpha) = i_{Ln,\lambda 4} = I_{Ln,max} \tag{4}$$

$$i_{Ln}(\pi) \rightarrow v_{on,\lambda 5} = v_{on,\lambda 1} \tag{5}$$

$$i_{Ln}(\pi + \delta) = i_{L\lambda 6} = -i_{Ln,\lambda 2} = -\frac{V_{cc}(dm\pi + 2\delta - 2m\pi + \pi)}{2\omega L}\left(\frac{Z_0}{V_{ref}}\right) \tag{6}$$

$$i_{Ln}(\pi + \gamma) = i_{Ln,\lambda 7} = 0 \tag{7}$$

$$i_{Ln}(\pi + \alpha) = i_{Ln,\lambda 8} = -i_{Ln.\lambda 4} = -I_{Ln,max} \tag{8}$$

The state transitions associated with each of these targets are given here.

$$v_{on} \leq v_{on,\lambda 1} \tag{9}$$

$$i_{Ln} \geq i_{Ln,\lambda 2} \tag{10}$$

$$i_{Ln} \leq i_{Ln,\lambda 3} \tag{11}$$

$$i_{Ln} \geq i_{Ln,\lambda 4} \tag{12}$$

$$v_{on} \leq v_{on,\lambda 5} \tag{13}$$

$$i_{Ln} \leq i_{Ln,\lambda 6} \tag{14}$$

$$i_{Ln} \geq i_{Ln,\lambda 7} \tag{15}$$

$$i_{Ln} \leq i_{Ln,\lambda 8} \tag{16}$$

These targets were determined in combination with gauging the best use of NSS degrees of freedom. Along with the allowable voltage ripple set by $V_{o,min}$ to be selected by the designer, the dynamics of m and f_{sw} as inputs were strategically selected according to the desired trajectory. With this many moving variables, an optimization problem could be applied to this design, but for this work, optimization was left outside the scope. A summary of the three mode operation for all loading conditions while prioritizing device lifetime preservation is provided in Table 19.

Table 19: Summarized Modes of NSS Control Operation when Prioritizing Life Preservation

Utilized	*M4*			*M6*			*ML*		
Trajectories	SS	u_1	u_2	SS	u_1	u_2	SS	u_1	u_2
I	λ_1	1	-1	λ_1	1	-1			
II				λ_2	1	0	λ_1	1	0
III	λ_2	1	1	λ_3	1	1	λ_2	1	1
IV	λ_3	-1	1	λ_4	-1	1			
II*							λ_3	1	0
V							λ_4	0	0
VI				λ_5	-1	0	λ_5	-1	0
VII	λ_4	-1	-1	λ_6	-1	-1	λ_6	-1	-1
VI*							λ_7	-1	0
V*							λ_8	0	0

Note (*) that trajectories II, V and VI are utilized twice by *ML* where $\lambda_1 = \lambda_3$, $\lambda_4 = \lambda_8$, and $\lambda_5 = \lambda_7$, which is why there are not X but VII total trajectories that are utilized for this design. That being said, trajectory II is performed with different conducting switches when it is repeated at II* as can be seen consistent upon assessment of Table 19 and Figure 51.

When considering which losses directly affect junction temperatures we can start with (17).

$$P_{loss} = P_{sw} + P_{cond} = \frac{I_{on}V_{off}}{a} f\Delta t_{sw} + I_{on}^2 R_{DS(on)} \tag{17}$$

For both switching and conduction power losses, there are components to account for with each of the MOSFET and the Schottky diode consistent with (18).

$$P_{Total,cond} = P_{MOS,cond} + P_{Diode,cond} \tag{18}$$

In [51], these conduction losses for the MOSFET and the Schottky diode are provided as in (19) and (20).

$$P_{MOS,cond} = \frac{1}{T_S} \int_{\theta_1}^{\theta_2} |i_L|\ V_{DS} d\theta \tag{19}$$

$$P_{Diode,cond} = \frac{1}{T_S} \int_{\theta_1}^{\theta_2} |i_L| \; V_F d\theta \tag{20}$$

Where V_{DS} is the voltage from drop across the MOSFET in the ON state, V_F is the forward drop voltage across the diode, T_S is the switching period, and where θ_1 and θ_2 are the conducting limits of each interval. When these conduction limits are further apart, making the conduction period longer, and the transformer current is high in magnitude, these are the conditions for which conduction losses will increase significantly. The following expresses the junction temperature as a function of total losses.

$$T_j = T_{ambient} + P_{diss}(Z_{th,jc} + Z_{th,ca}) \tag{21}$$

Total power losses including both switching and conduction will affect the junction temperature. The point to be taken here is that the junction temperature is loss agnostic. One form of loss will not affect the junction temperatures more than another in a form of advantage here. Whichever amount of loss dominates in converter operation is the factor that will dominate affecting junction temperature.

Being able to circulate current flow through devices at a controlled level while not charging the output capacitor more than necessary allows for the design flexibility to control the amount of desired of conduction loss while maintaining the required power output with high power quality. Theoretically, the resulting losses can match whatever loss was existent before the reduction of

load occurred, and this way minimize the thermal cycling possibly to the point of elimination. For example, if the amplitude of transformer current is at 100 A during heavy loading, and the circulating current during light load matches that current, losses would be comparable between the two cases essentially eliminating thermal cycling. Life preservation mode proposed here achieves just that. Another design benefit is that with $i_{Ln}(\delta)$ as a target current still incorporated into the control law design, the modulation index is still capable of modulating even if hampered by the new progression of switching surfaces. More will be spoken on this in the next section.

The one main disadvantage seen at this time of life preservation mode is the amount of losses generated for efficiency's sake. Yes, these losses were performed on purpose, but they are undesired for the purpose of efficient performance. This is due to the impassable trade-off between reliability and efficiency that has come up a few times over the course of this document. While efficiency will suffer, the designer can control how inefficient and how reliable one might need to design for by use of the target current definitions inherent to this design.

5.1.1 Degrees of freedom and transient performance specific to Life Mode

The degrees of freedom that provide design flexibility for Life Mode are m, f_{sw}, $I_{Ln,max}$, and $V_{on,min}$. In this section, these variables are explored to gain familiarity of flexibility and limitations through a number of sensitivity analysis case results. For an example of such a manipulation of life preservation mode see the conceptual diagram in Figure 52 where $I_{Ln,max}$ is decreased resulting in the depicted variations to the state plane and associated system waveforms. We will find within this section that $I_{Ln,max}$ is of particular interest. For all assessments and sensitivity analyses found here, simulation parameters are shown in Table 20.

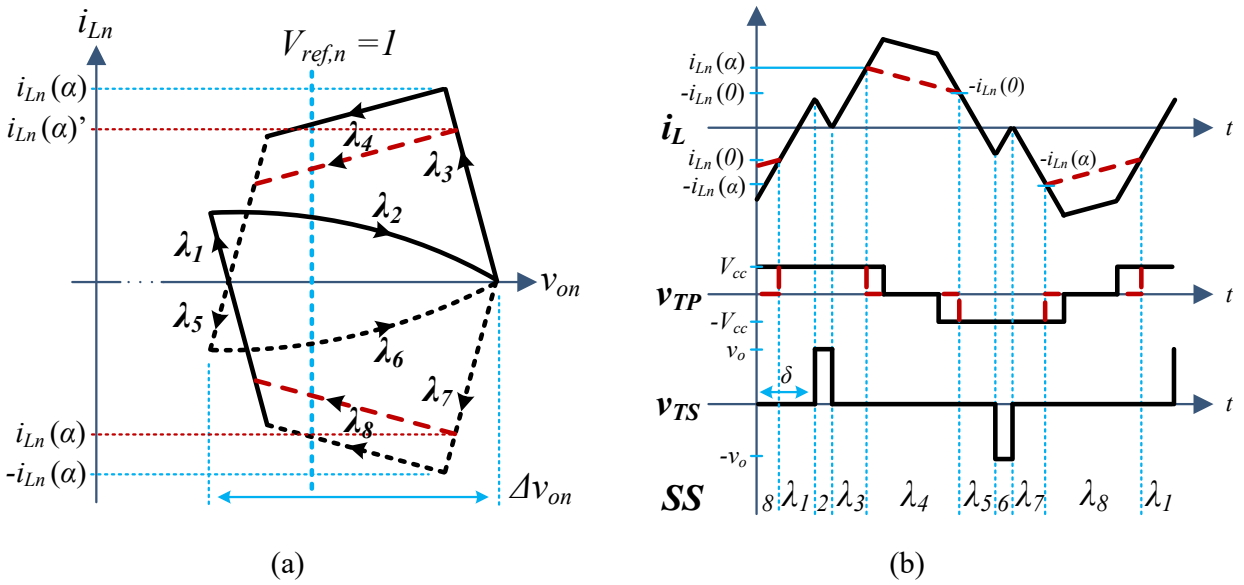
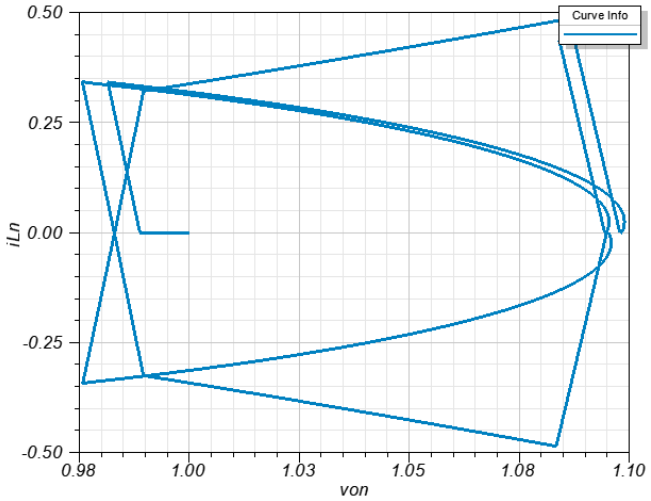


Figure 52: Conceptual Modification to Life Preservation Mode with $I_{Ln,max}$ as a Control Handle showing the Normalized State Plane and Associated System Waveforms

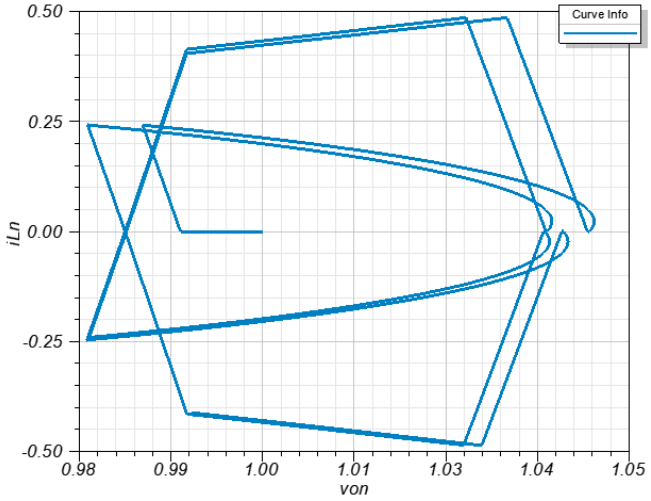
Table 20: Simulation Parameters for Degrees of Freedom and Transient Performance Assessments

Parameter:	Value:	Description
M	ML	Mode of strategic trajectories
P_o	600W	Output power demanded
V_{cc}	120	Input voltage
V_o	240	Output voltage (V_{ref})
d	$V_o/(nV_{cc})$	Conversion ratio (n = 1.5)

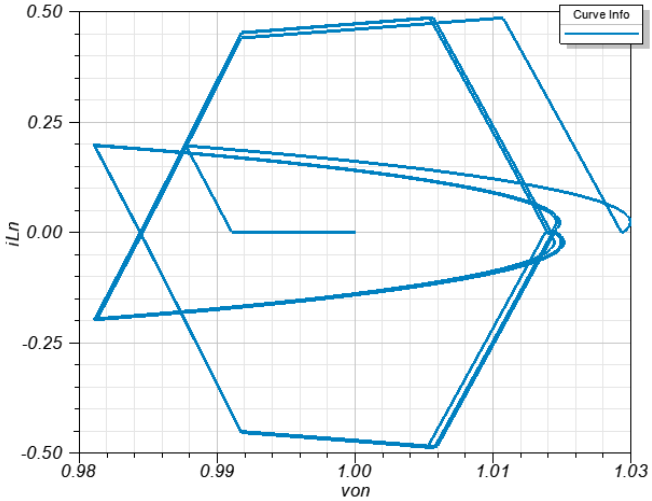
Variation of the modulation index as defined and implemented in previous sections for *M4* and *M6*, provides the range of performance as seen in Figure 53. The cases vary m from 0.1 to 0.4 with increments of 0.15 per case. The maximum current is set at i_L = 80A for this analysis. The design choice of m = 0.25 is a balance between voltage overshoot (decreasing m at 0.1) and minimization of conduction range (increasing m at 0.4).



(a)



(b)



(c)

Figure 53: Sensitivity state plane analysis of the impact of *m* variation where (a) m=0.1, (b) m=0.25, and (c) m=0.4

The results found in Figure 53 and Figure 54 demonstrate the transient performance of transitioning from heavy loading at 7.2kW to light loading at 600W. The performance is impeccably smooth due to the nature of natural switching surface control where the action to move from one mode to another, the ideal moment to transition is waited for. The fast transient performance of boundary control is discussed in depth in other work [43]. The demonstrated smooth transition speaks on to the fast transient performance associated with this design.

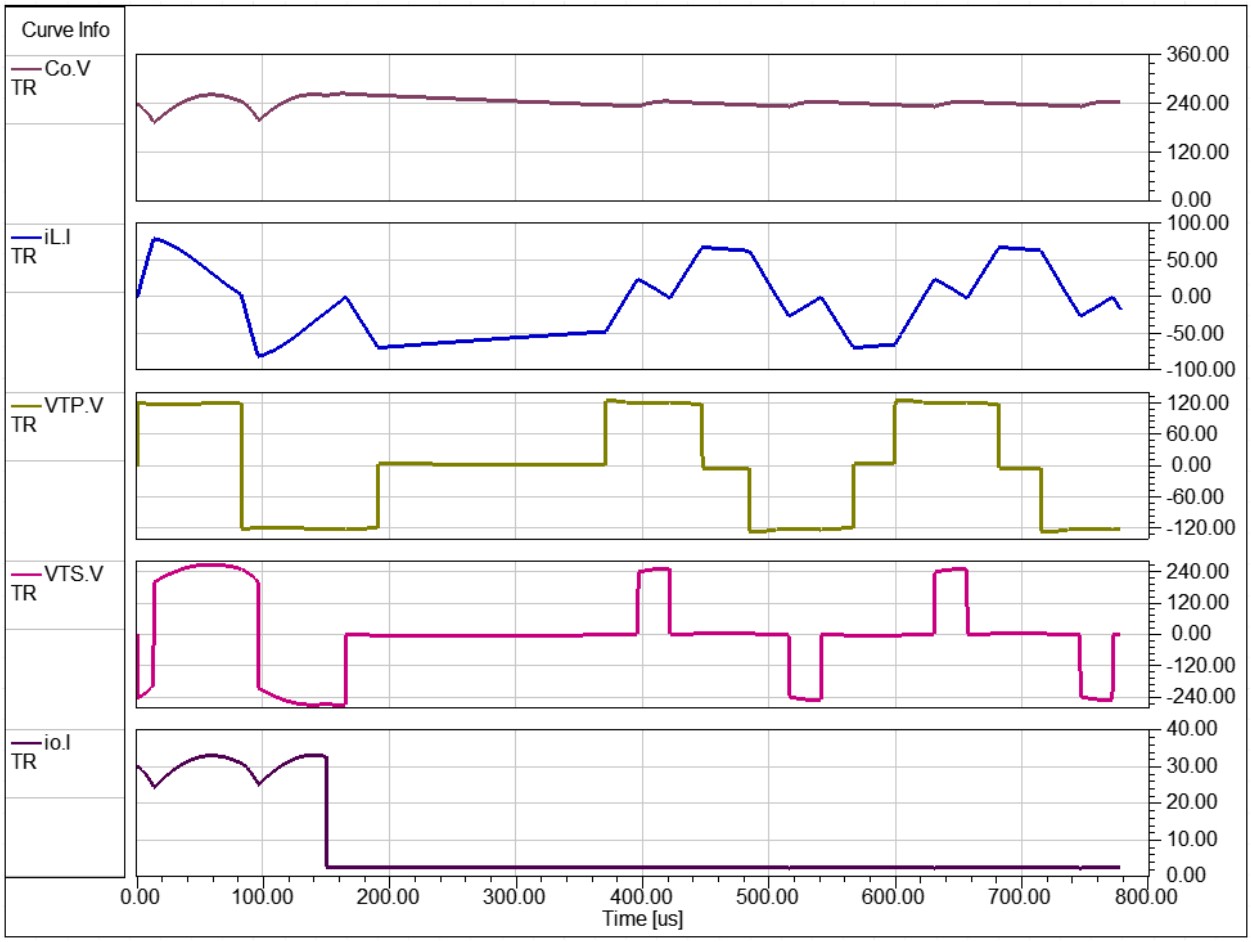


Figure 54: Transient performance of the life preservation mode showing a transition from *M4* to *ML* at loading conditions of 7.2kW and 600W respectively

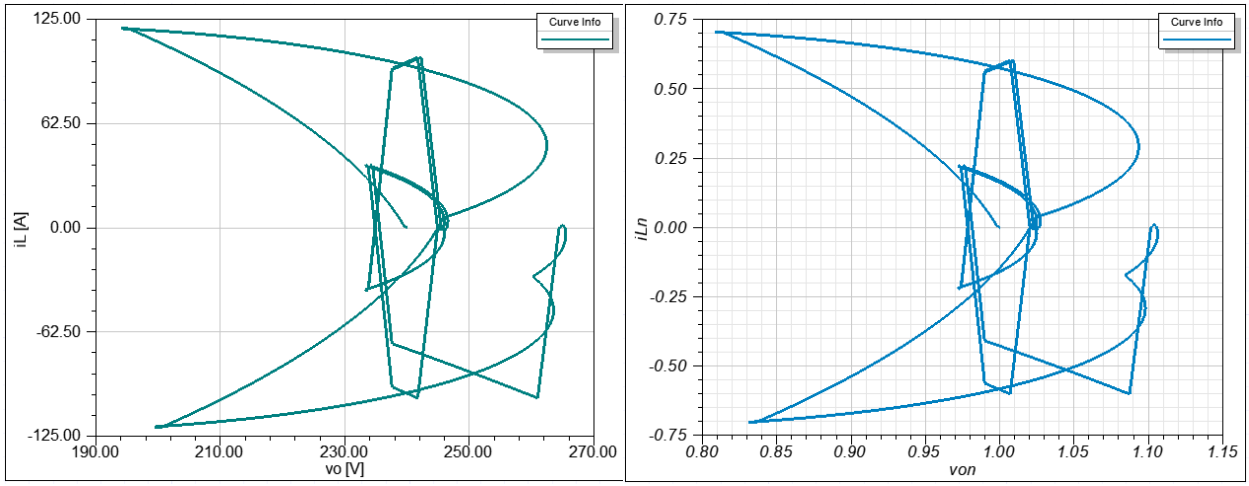
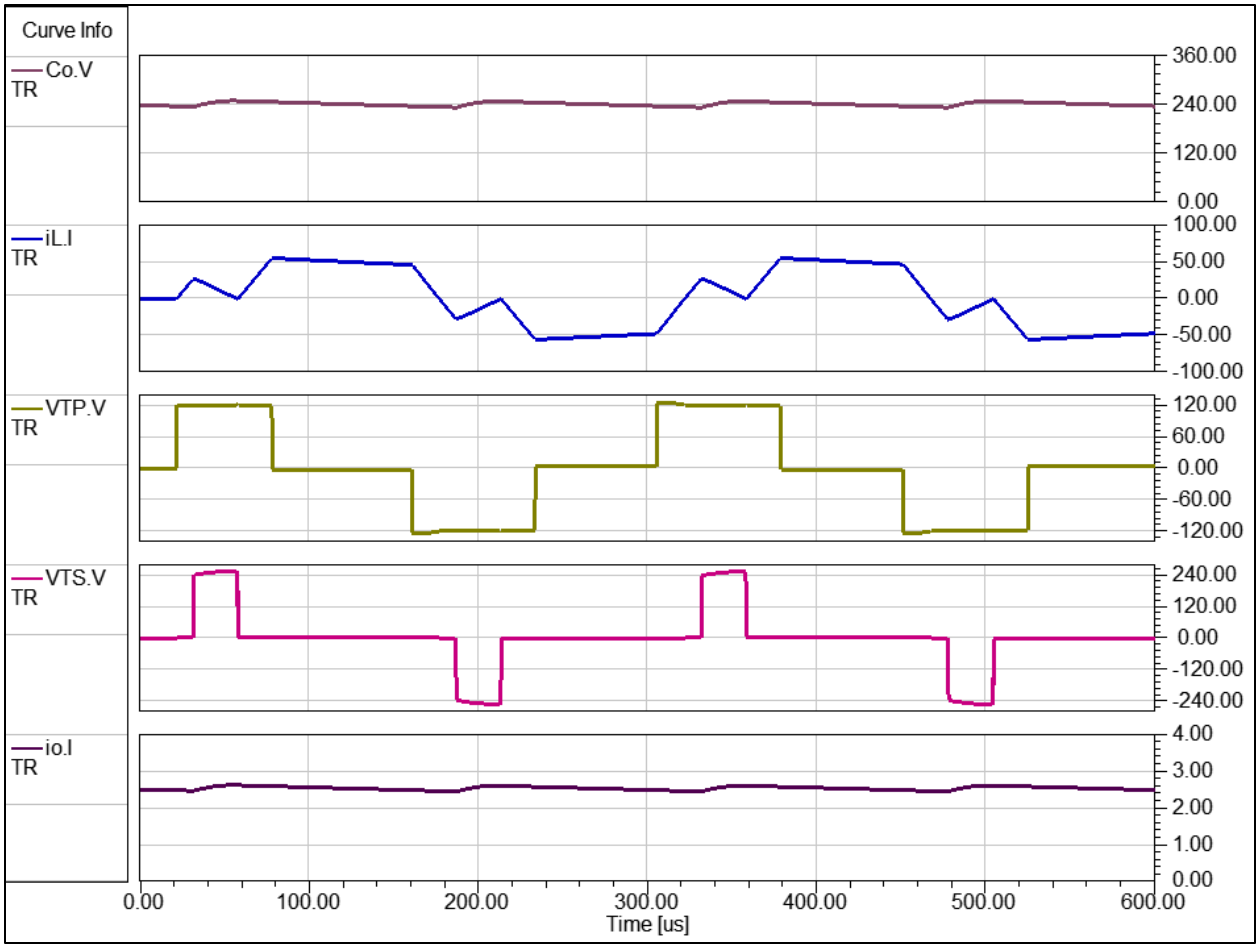


Figure 55: State plane nominal and normalized associated with transient performance transitioning from *M4* to *ML*

Saved for last due to length but not at all due to last importance, is a sensitivity analysis demonstrating the impact of varying each degree of freedom related to *ML*. The cases are designed for variable variation as in Table 21. The base case sets the foundation of the sensitivity analysis, and its results are presented in Figure 56 and Figure 57.

Table 21: Life Preservation Mode of Control Degrees of Freedom Parametric Sensitivity Analysis

Variable	Base	Case 1	Case 2	Case 3	Case 4	Case 5
$I_{L,max}$	80A	100A	50A	80	80	80
$V_{on,max}$	0.99	0.99	0.99	0.99	0.99	0.99
m	0.25	0.25	0.25	0.1	0.4	0.25
f_{sw}	10kHz	10kHz	10kHz	10kHz	10kHz	20kHz



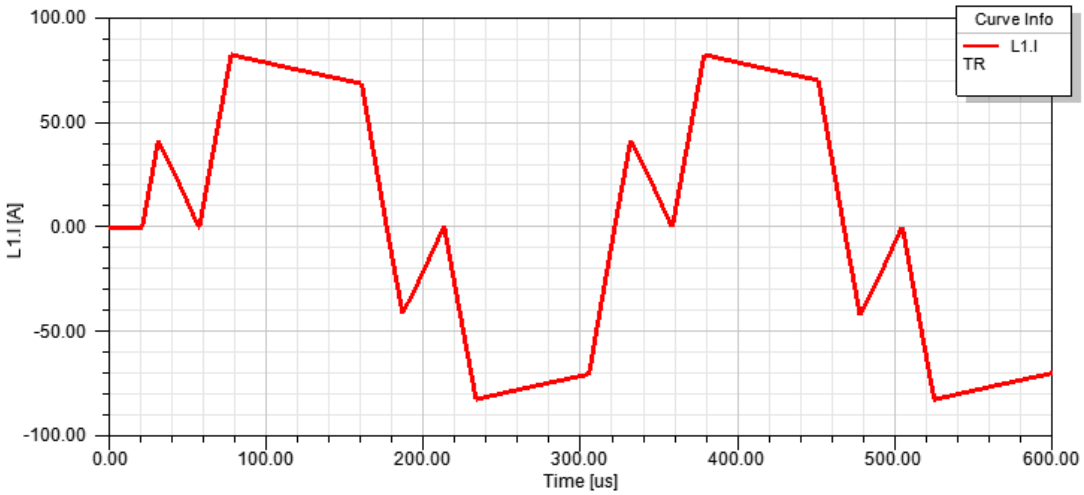


Figure 56: Base Case of *ML* Parametric Analysis

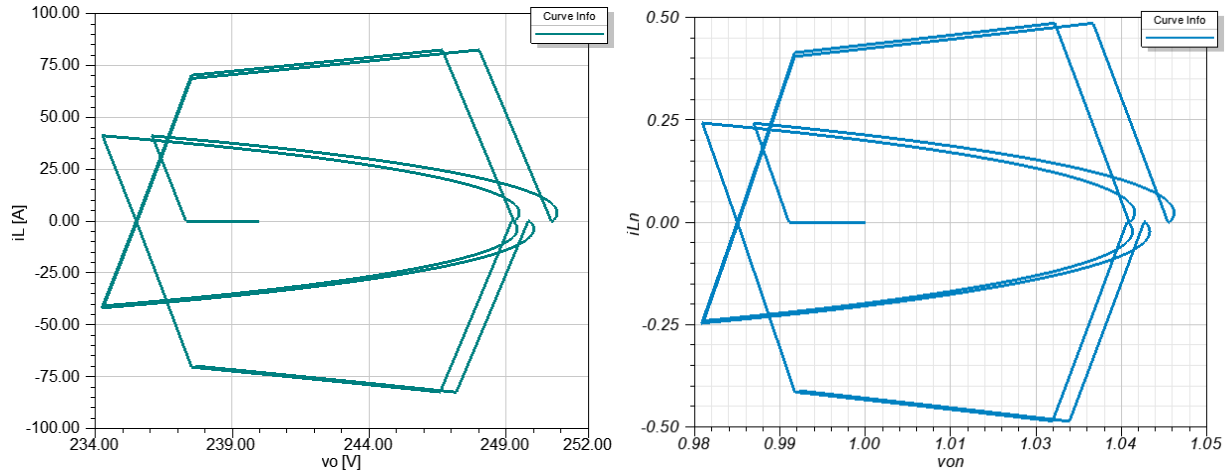
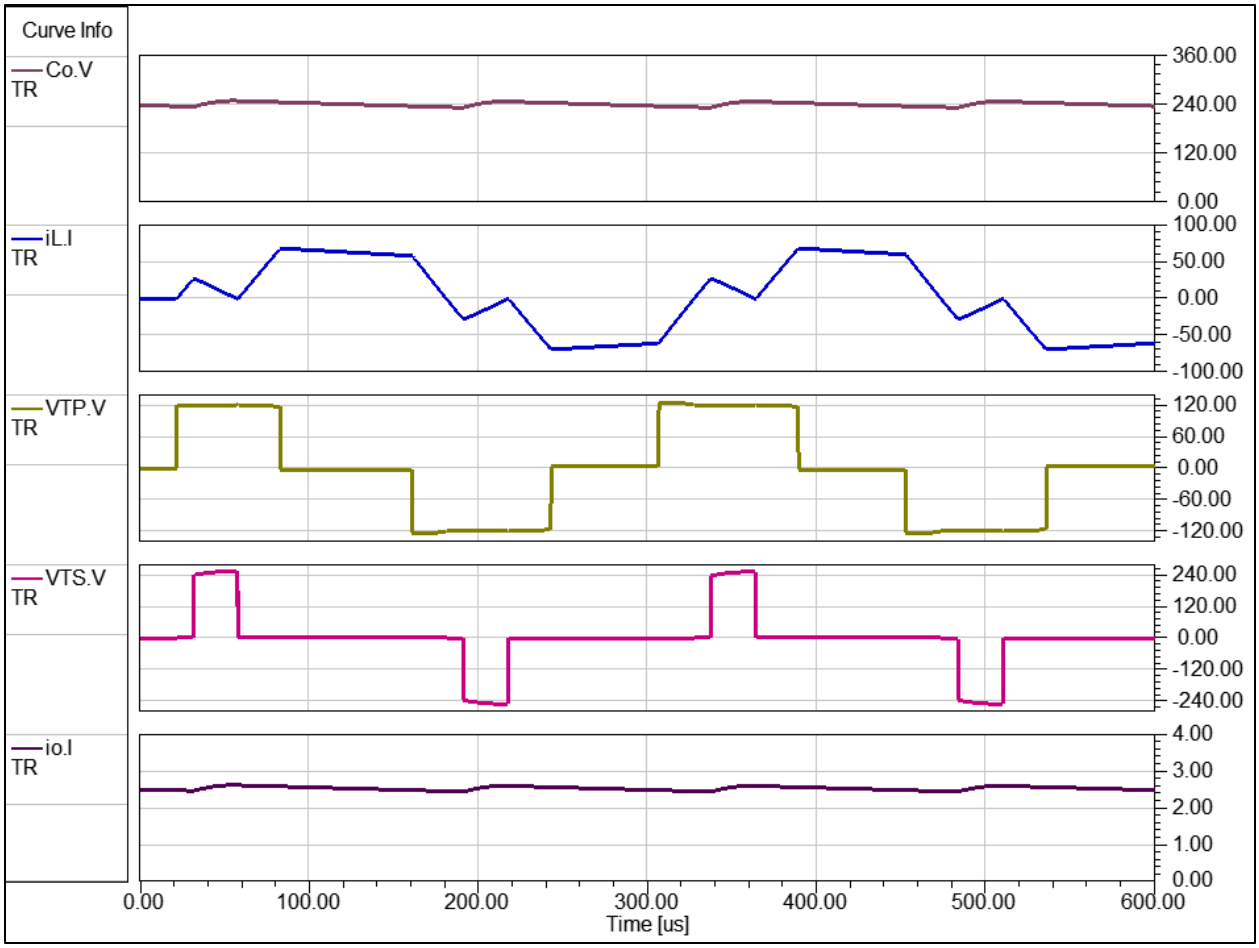


Figure 57: Base Case State Plane Analysis both Nominal and Normalized

This base case sets the tone. The signals included in Figure 56 are output voltage v_o, transformer current i_L, primary transformer voltage v_{TP} secondary transformer voltage v_{TP}, output current or load current i_o, and lastly a zoomed in shot of the transformer current for clarity of current magnitudes. Additionally both a nominal and normalized state plane are presented in Figure 57. Seeing the correlation between waveforms and state plane help us to familiarize ourselves with the method, as well as to aid us in comparing between cases of the sensitivity analysis. The same plots are shown for each case, highlighting each change from this base case. Case 1 is presented in Figure 58 and Figure 59.



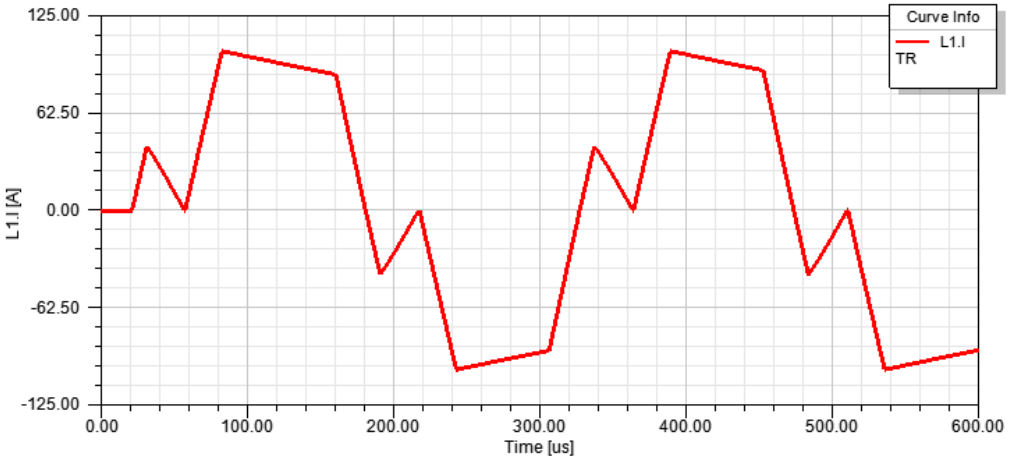


Figure 58: Case 1 of *ML* Parametric Analysis with Maximum Current Increased to 100A

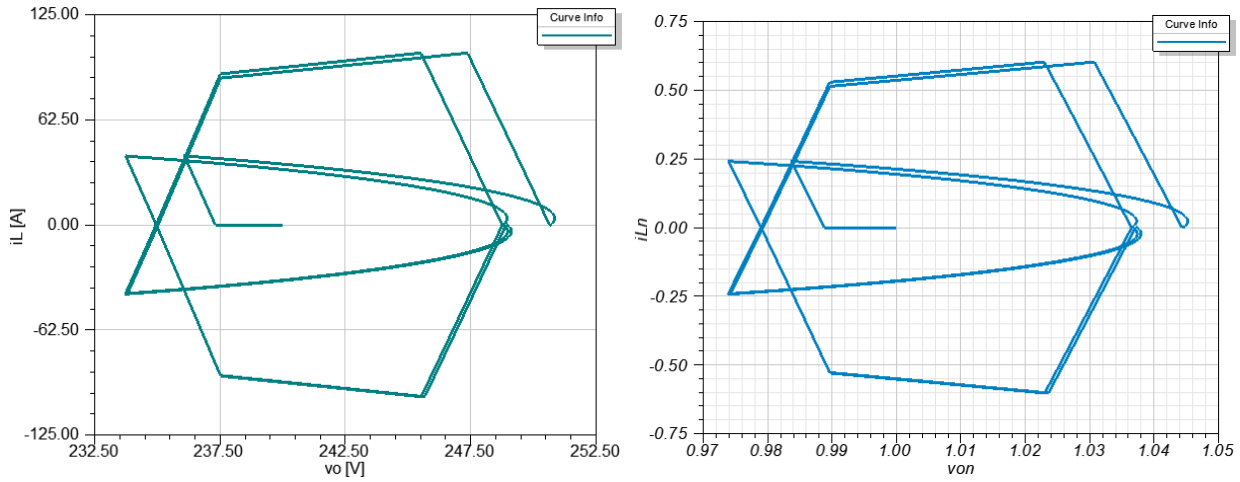
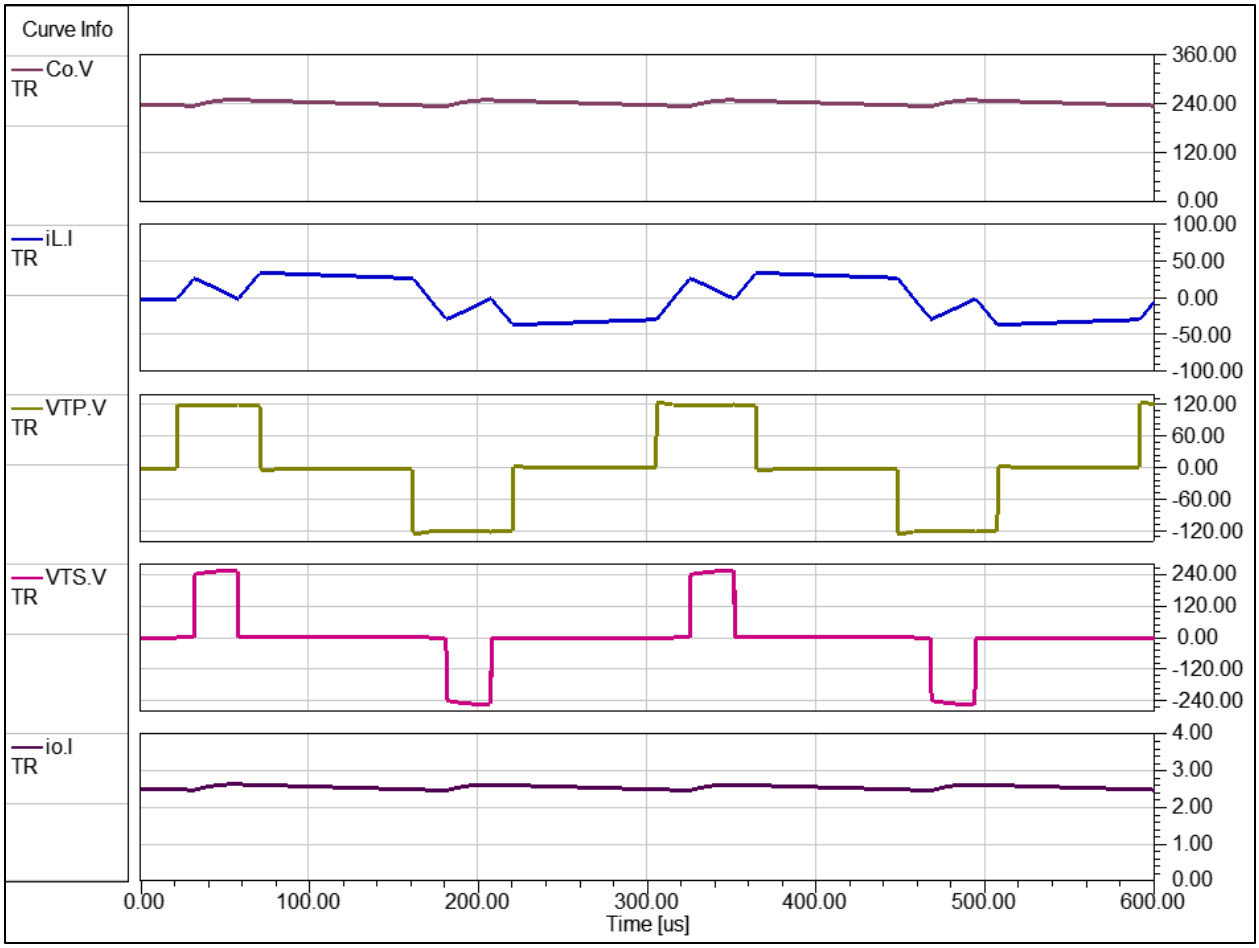


Figure 59: Case 1 State Plane Analysis both Nominal and Normalized with Maximum Current Increased to 100A

An increase of current maximum from 80A to 100A is made in Case 1. This increase shows that there will be higher magnitudes of current during the entire circulating conduction mode. This will result in a significant increase of heating on the devices. In comparison to the base case, peak magnitudes will reach an additional 20A to then slowly drop along the switching surface as circulating currents near the next trajectory change. This circulating current trajectory with associated conduction loss is the primary device warming mechanism of the design. Following this logic as well as observing results, $I_{L,max}$ is the control handle of choice for being the most effective facilitator of junction temperature change. Note that the parameters of this same case are later used for a validation simulation of ATBC assessing junction temperature dynamics throughout a change of loading conditions.



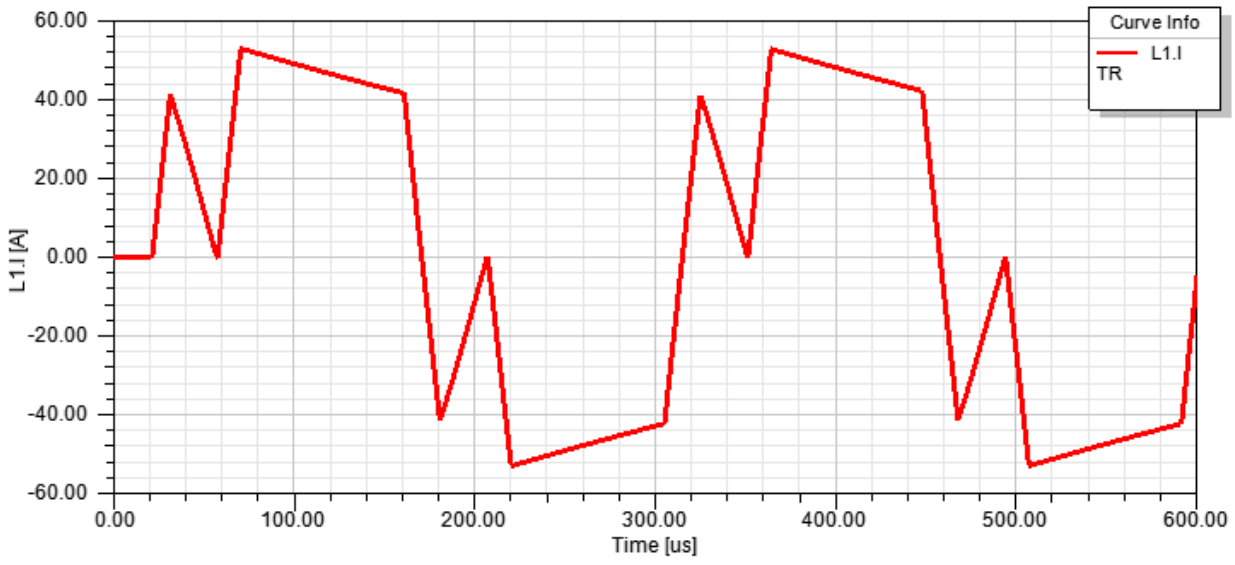


Figure 60: Case 2 of *ML* Parametric Analysis with Maximum Current Decreased to 50A

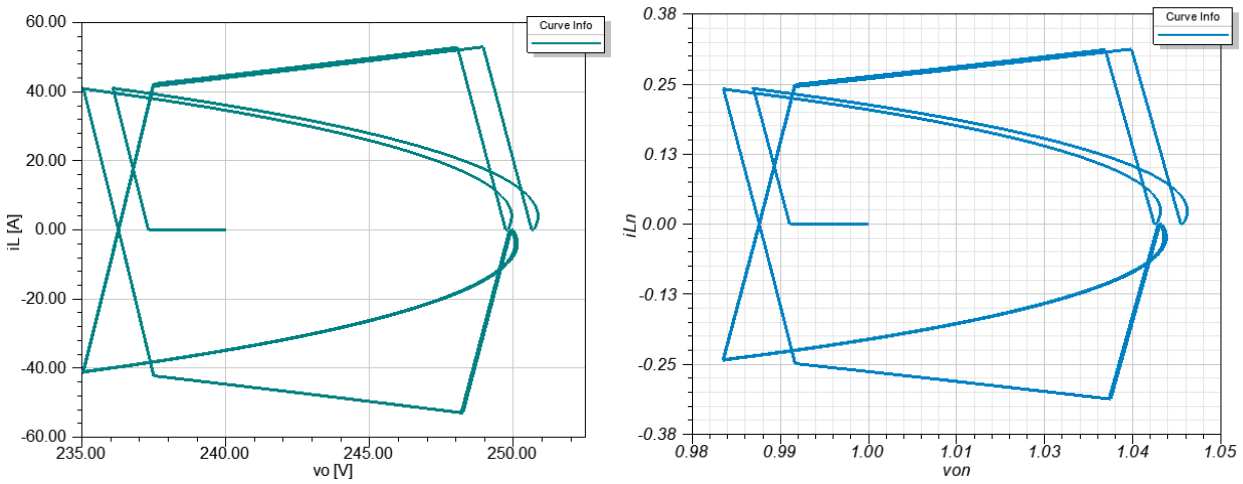
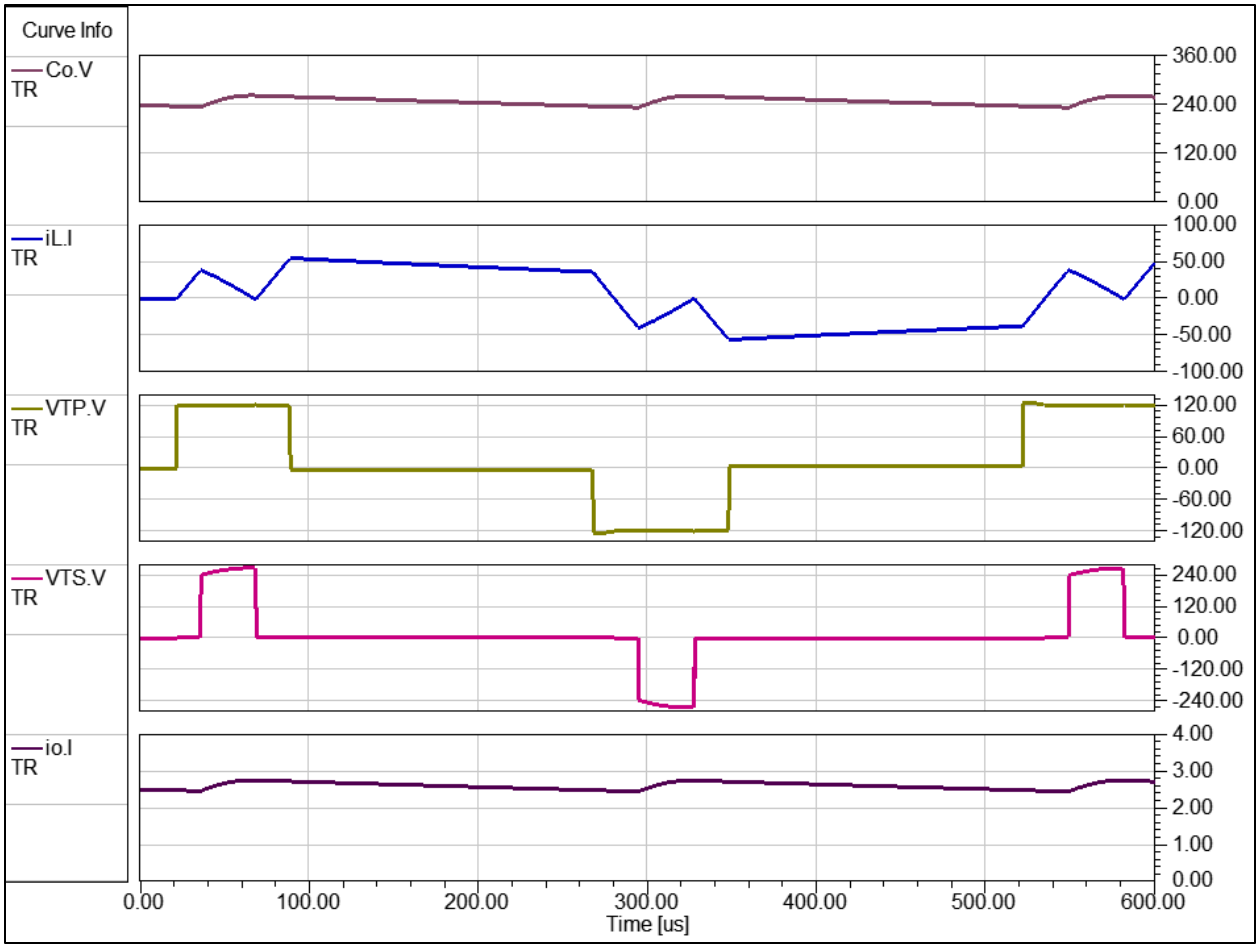


Figure 61: Case 2 State Plane Analysis both Nominal and Normalized with Maximum Current Decreased to 50A

A decrease of current maximum from 80A to 50A is made in Case 2. This decrease shows that there will reduced magnitudes of current during the entire circulating conduction mode. This will result in a significant decrease of heating on the devices in contrast to both cases above. Additionally, the parameters of this case are also later used for a validation simulation of ATBC.



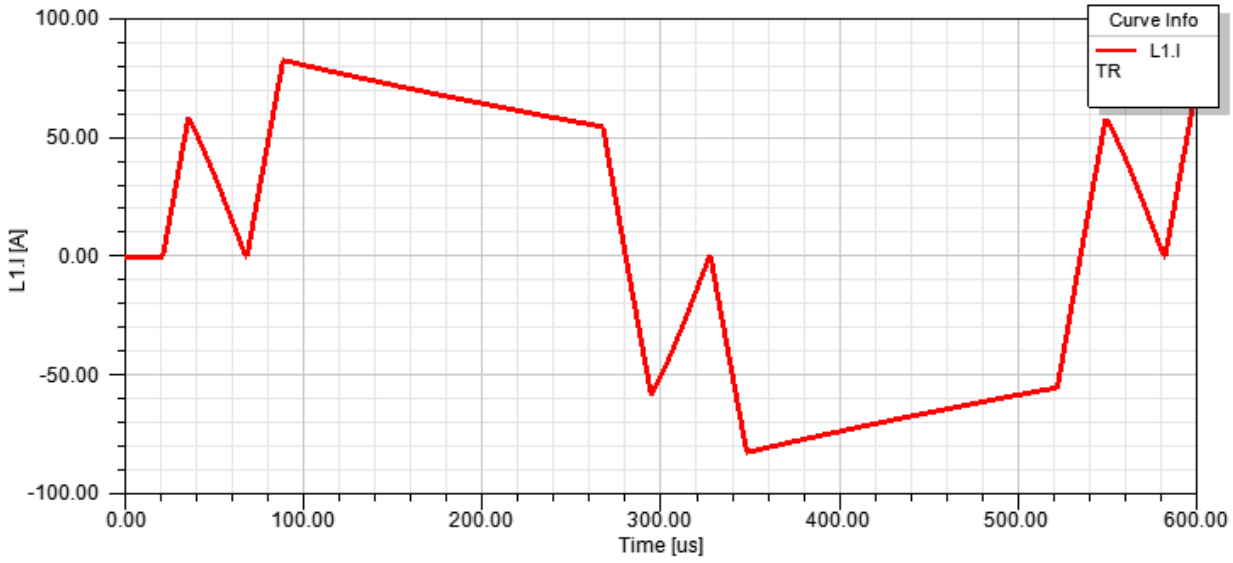


Figure 62: Case 3 of *ML* Parametric Analysis with the Modulation Index at 0.1

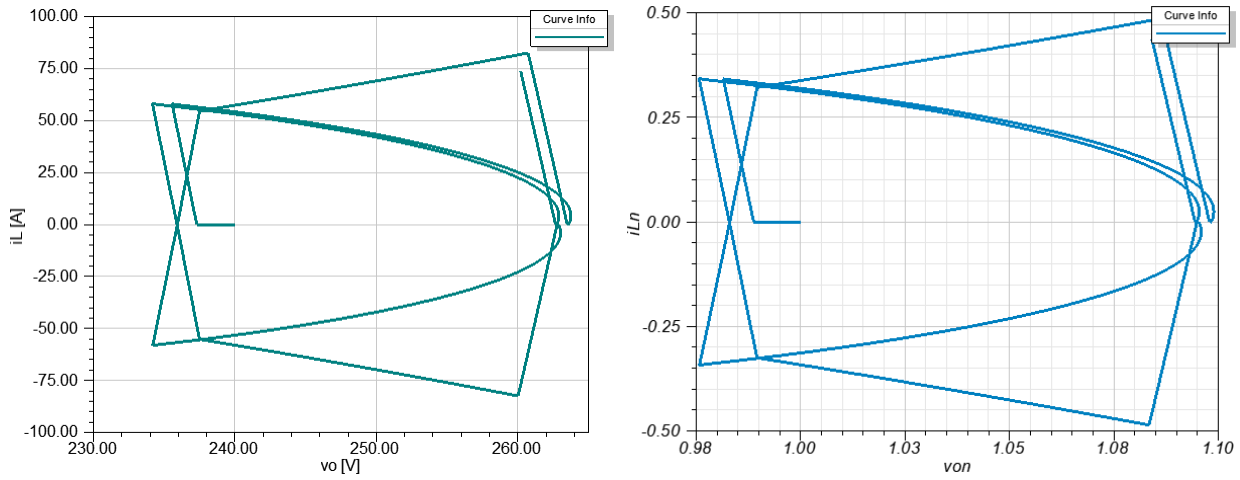


Figure 63: Case 3 State Plane Analysis both Nominal and Normalized with the Modulation Index at 0.1

Case 3 brings a change in the modulation index, decreasing it from 0.25 to 0.1. Note that the modulation index does not now entirely perform as originally intended, to modulate the high voltage side of the DAB for efficiency and full operating range utilization purposes. Here it acts still as a modulation index would, but the modulating capability has been hampered by the selection of trajectories of this design. The trajectories 4 and 8 are not at all affected by alteration of *m*, while 2 and 6 are significantly affected. This is particularly apparent in the comparison presented in Figure 53. Note that manipulation of *m* primarily affects how far life preservation mode overshoots unity of normalized output voltage.

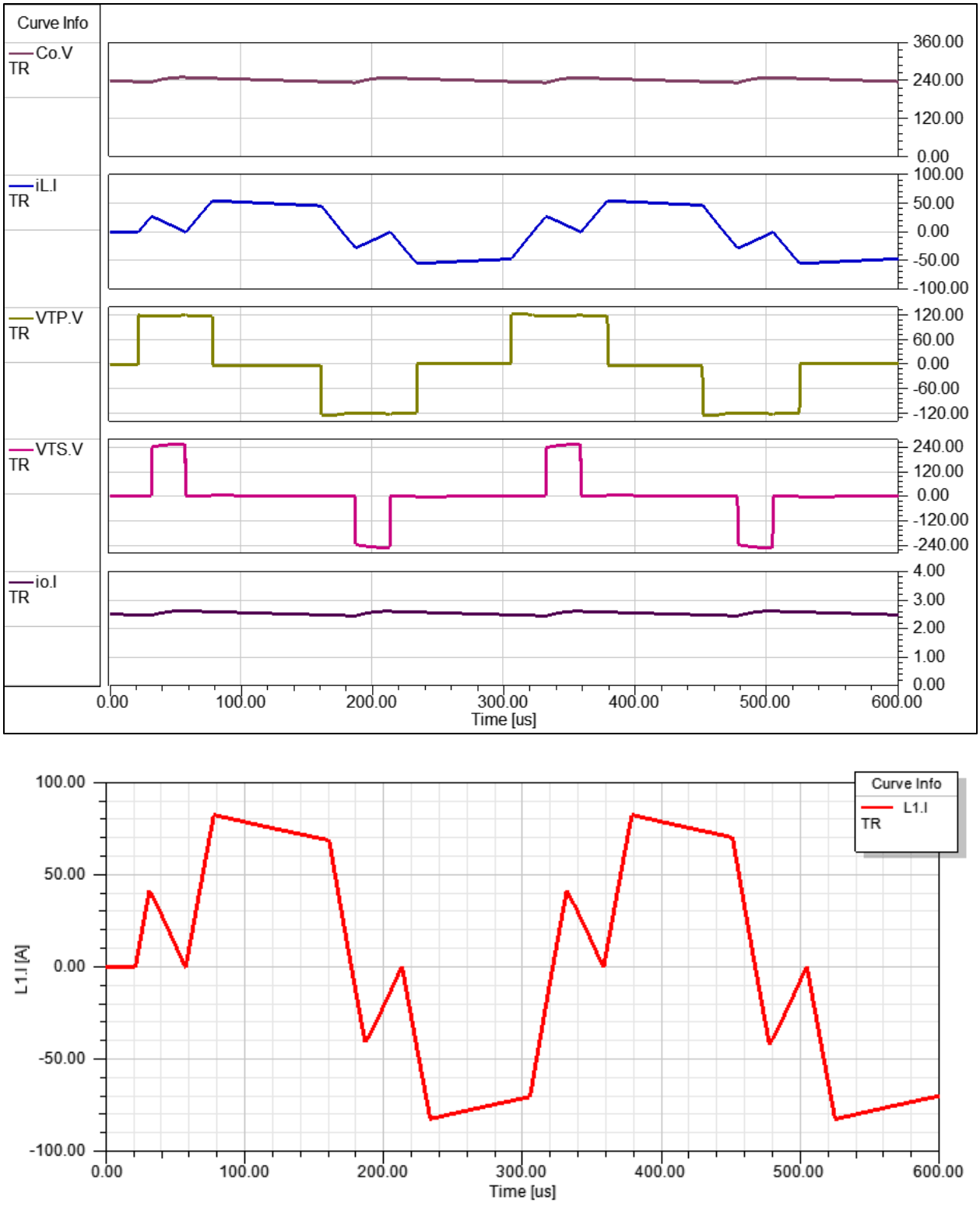


Figure 64: Case 4 of *ML* Parametric Analysis with the Modulation Index at 0.4

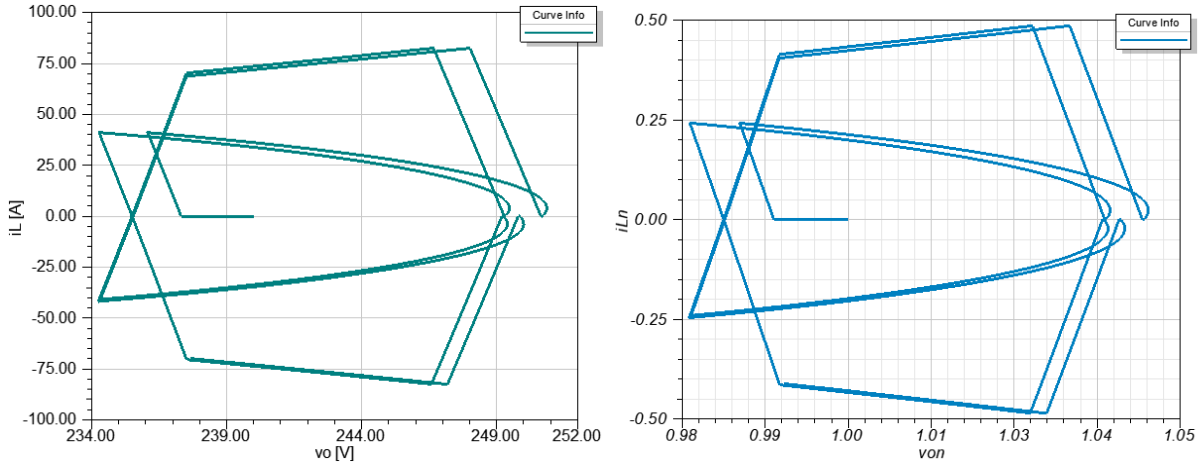
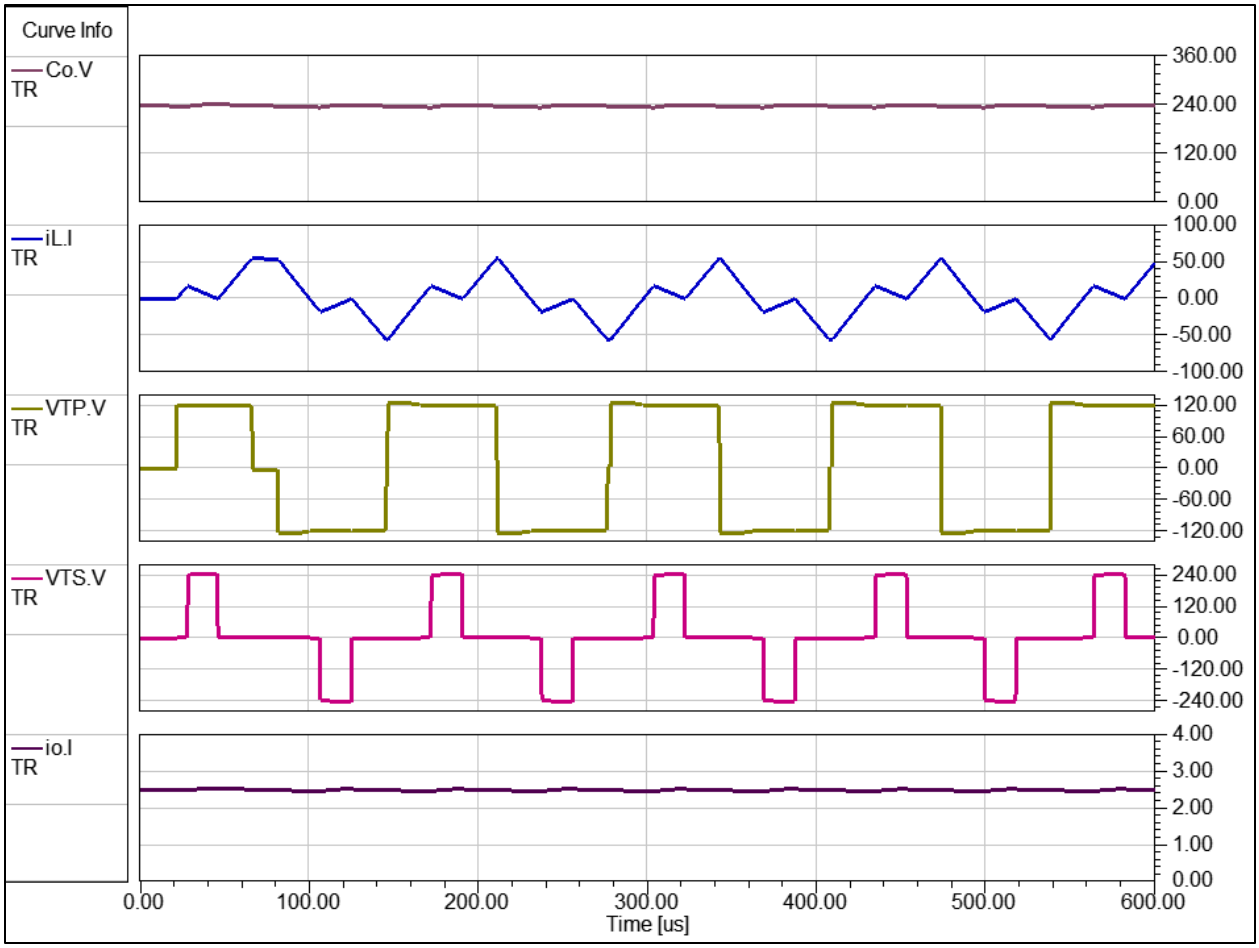


Figure 65: Case 4 State Plane Analysis both Nominal and Normalized with the Modulation Index at 0.4

Here with an increase of *m*, notice that the highest overshoot of voltage occurs. Even if it is still a minimal overshoot, this is the effect of an increased *m* has over life mode. This increased overshoot is due to the modification of thresholds for switching surfaces 2 and 6.



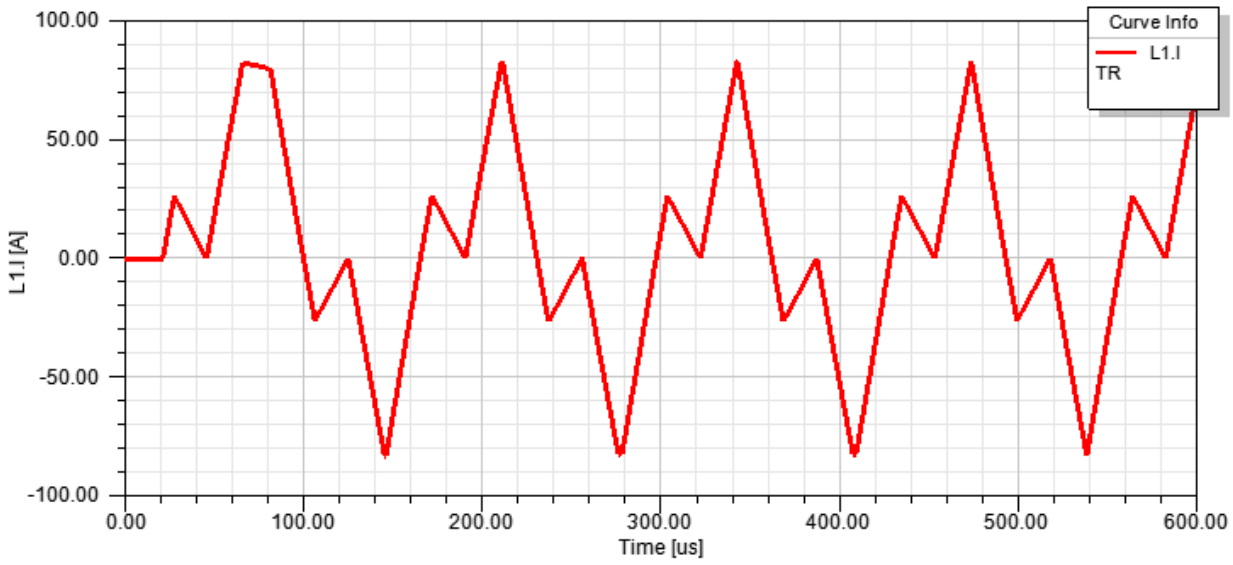


Figure 66: Case 5 of *ML* Parametric Analysis with the Switching Frequency at 20kHz

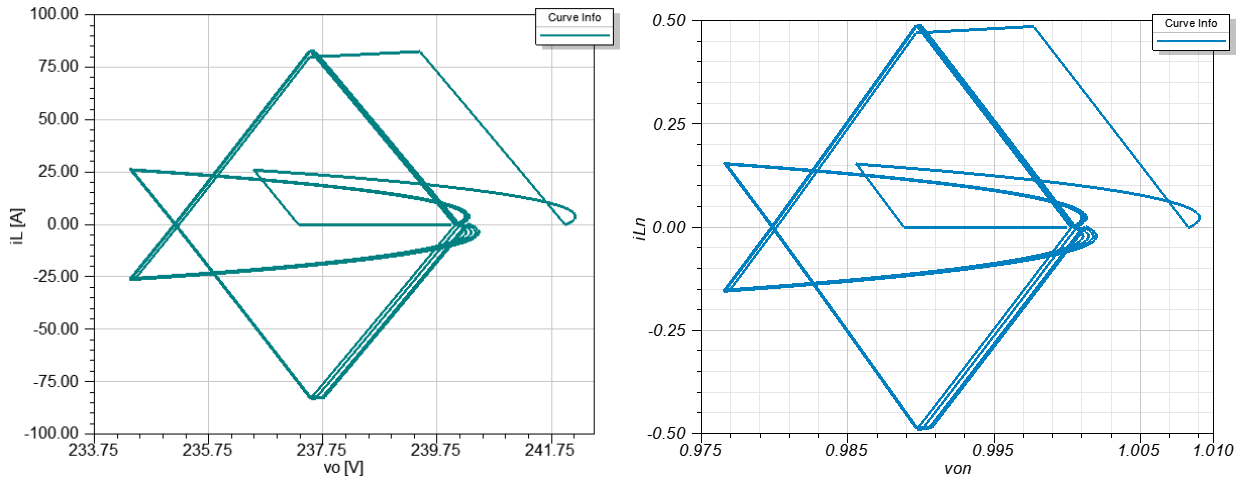


Figure 67: Case 5 State Plane Analysis both Nominal and Normalized with the Switching Frequency at 20kHz

Here is Case 5, the switching frequency is increased from 10kHz to 20kHz. Note that this is the same as the desired switching frequency previously defined, where an effective switching frequency may differ due to the nature of NSS. This is even truer for *ML* due to its design. An increase in switching frequency effectively reduces the length of time persisting in the circulating current trajectory. This overall will be undesirable since circulating current is what we are depending upon to keep the devices warm during light loading conditions. Unique to this trajectory of *ML*, conduction losses are occurring for heat while power is not being delivered. At some point on a spectrum of continuing to increase the switching frequency, the peak current values will also decrease. In the reverse, if switching frequency is decreased, the conduction trajectory will lengthen, and yet the longer the duration of this mode, a transition to another mode of *ML* will be delayed further and in some cases deviance from nominal voltage will hang for a longer period of time undesirably. Another method of achieving the same outcome is to have a faster switching frequency while simultaneously increasing the modulation index, since this will effectively alter the slope of switching surfaces λ_1, λ_3, λ_5, and λ_7 seen on Figure 50.

Note that all variables are changed in this sensitivity analysis except for $V_{on,max}$. This is due to the fact that altering the minimum allowed voltage only resulted in farther deviance from nominal voltage, which can be made sense of by assessing any of the state planes presented. This deviance is undesirable for the needs of this design where dropping from nominal 240V on the output will occur only too easily due to passing minimal current to the output capacitance.

In summary, the control handles of life mode perform the following capabilities. The upper limit on the output voltage is handled by the modulation index, m. The permissible drop of voltage is limited by the minimum voltage threshold, $V_{on,min}$. The frequency yes is controlled by the desired switching frequency handle, f_{sw}, but also the amount of time spent in circulating current conduction – a critical design parameter. Most effective in manipulating the time spent in circulating current conduction as well as the magnitudes of current circulating is simply $I_{L,max}$, the threshold set for the maximum allowable current while in life preservation mode.

5.2 ACTIVE THERMAL BOUNDARY CONTROL FOR BOOST MODE

Active thermal boundary control (ATBC) is made up of three different strategic trajectory modes for varying levels of load conditions – light, medium, and heavy load – so that efficient operation over a wide range of operation can be performed at medium and heavy loading but most importantly that the newly designed mode of trajectories performs life preservation for light loading conditions. Namely the three modes consist of *M6* and *M4* as previously discussed for medium and heavy loads and *ML* for light loads. Active thermal boundary control as a whole is summarized in Figure 68 as a decision flowchart, demonstrating the relationship among the modes of operation and their associated loading level. Also shown are the specific devices turned on per

trajectory as well as the condition triggering the entrance into each transition from one surface to the next of the control law. Notice that the initial switching surface of ML is λ_6 and not λ_1 as one might expect. Purposefully, λ_6 is selected as the best entrance for transient performance when transitioning from either *M6* or *M4* into *ML*. This switching surface is identical to λ_6 of *M6* and λ_4 of *M4*, making it the strategic selection in order to avoid unnecessary deviance from the nominally desired voltage or current during mode transitions.

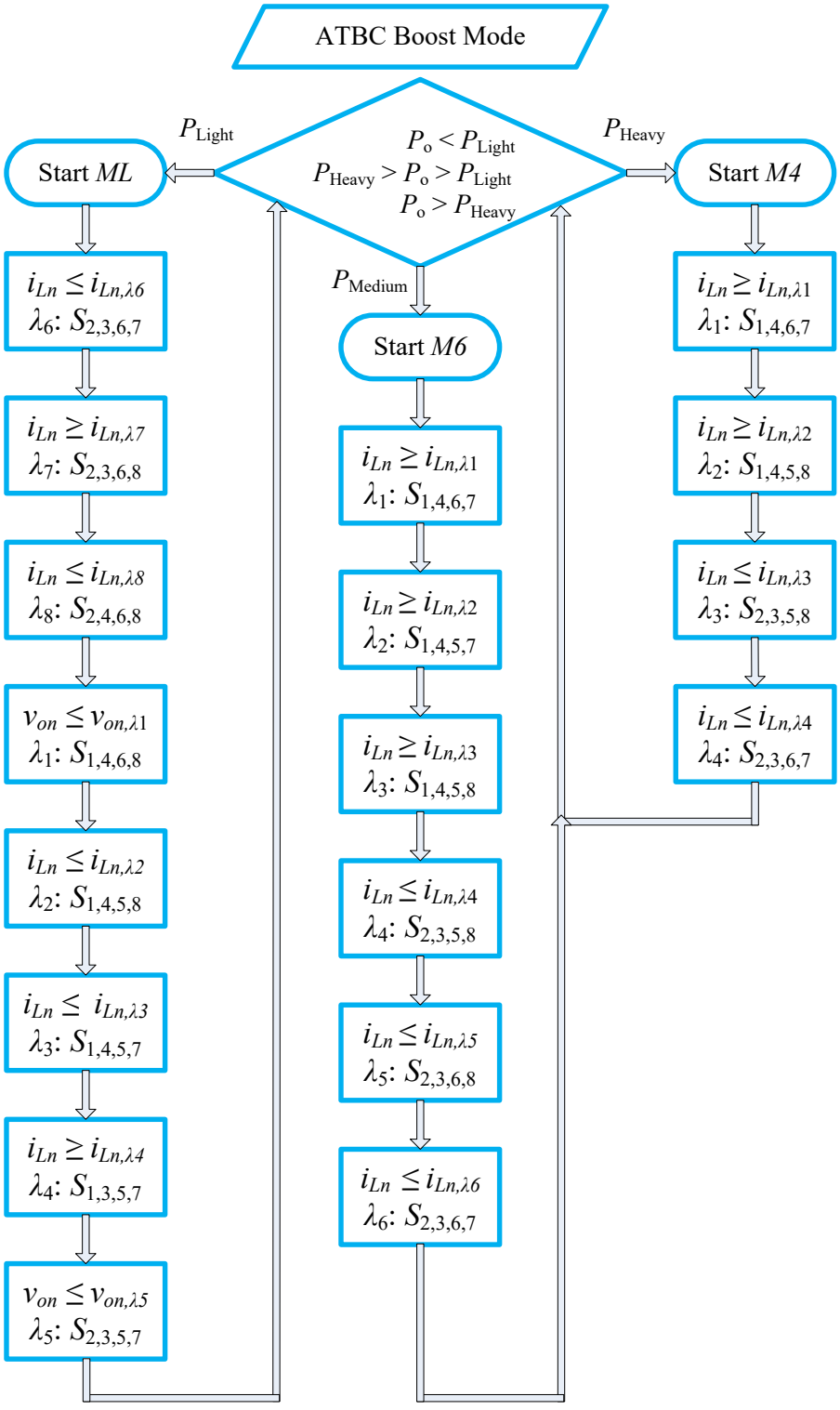


Figure 68: Flowchart of Active Thermal Boundary Control in Boost Mode of Operation

5.3 IMPACT ASSESSMENT OF ACTIVE THERMAL BOUNDRY CONTROL

The impact of active thermal boundary control (ATBC) upon device reliability is presented in this section. The boost mode operation is utilized for this analysis. A performance comparison is provided between the implementation of the case study prioritizing efficiency and the implementation of active thermal boundary control for a start. Thermal cycling is then observed through simulation for cases of heavy to light to heavy loading conditions for the following control implementations: burst mode combined with *M4* and *M6*, conventional DAB control, and lastly ATBC.

5.3.1 System Design Selections

The base parameters set for all validation simulations to follow are shown in Table 22. Any variation will be specified per case. These parameters were selected based upon the example of an electric vehicle charger or charging station expecting to experience intervals of heavy and light or even no load on a cyclical bases. If cycles of charging are expected maybe during set busy hours of the day, keeping the power electronics warmed up for reliability's sake would be a desirable design. Level 2 electric vehicle chargers are rated at 240V in the multiple kW range.

As for the electro-thermal semiconductor device selected for validation of active thermal boundary control, a SiC power MOSFET made by Microsemi (APTMC120AM20CT1AG [54]) fit the ratings of the design provided in Table 22. In addition to fitting my rated needs, the datasheet has all information necessary for characterization in ANSYS. The heat sink parameters implemented and consistent among all cases were common thermal capacitance and resistance. These heat sink values are 1e5 Watt-seconds per Kelvin for thermal capacitance and 1e-6 Kelvins

per Watt for thermal resistance. These parameters are integrated into the electro-thermal model as in from Figure 7 of Section 2.0 where the characterization of electro-thermal devices were addressed in more detail. Reference Section 2.0 for more information on the characterization process.

Table 22: Base Parameters for Validation Simulations Implementing Various Control Modes

Parameter:	Value:	Description
M	[*MB, M6, M4, ML, Conv.*]	Possible modes of strategic trajectories
P_o	[600W – 7.2kW]	Output power range
C_o	20 (μF)	Output capacitance
L_{Tx}	40 (μH)	Transformer equivalent inductance
V_{cc}	120 (V)	Input voltage
V_o	240 (V)	Output voltage (V_{ref})
d	$V_o/(nV_{cc})$	Conversion ratio (n = 1.5)
f_{sw}	[10kHz – 10kHz]	Switching frequency range
m	[0.1 – 1.0]	Modulation index range
T_{MOSFET}	-	Microsemi SiC MOSFET [54]
-	1200 (V)	Drain to source voltage V_{DS}
-	143 (A)	Drain current I_D
-	17 (mΩ)	Drain to source ON resistance $R_{DS(on)}$
R_{th}	1E-6 (K/W)	Heat sink thermal resistance
C_{th}	1E5 (Ws/K)	Heat sink thermal capacitance

5.3.2 Efficiency Case Study Comparison

Development of the active thermal boundary control for the dual active bridge depends upon a design for reliability. This design for reliabliity is in contrast to the case study presented previously, a design prioritizing efficiency. This case provides a comparison to observe the contrast between *ML* and *MB*. The timing sequence of this simulation is to operate in *ML* from 0 to 1ms, *M6* from 1 to 2ms, and *M4* through to 3ms. This same sequence as well as the same design parameters were

performed for implementing *MB* in Section 4.4. As seen in Table 23, note that the modulation index for *ML* is set to 0.25 in contrast to 0.1 for the efficiency case study results.

Table 23: Parameters for Efficiency Case Study Comparison Implementing *ML*

Parameter:	Value:	Description
M	[*ML, M6, M4*]	Modes of strategic trajectories
P_o	[600W, 3.6kW, 7.2kW]	Output power demanded
V_{cc}	120	Input voltage
V_o	240	Output voltage (V_{ref})
d	$V_o/(nV_{cc})$	Conversion ratio (n = 1.5)
f_{sw}	[10kHz, 10kHz, 4kHz]	Switching frequency per mode
m	[0.25, 0.5, 1.0]	Modulation index per mode

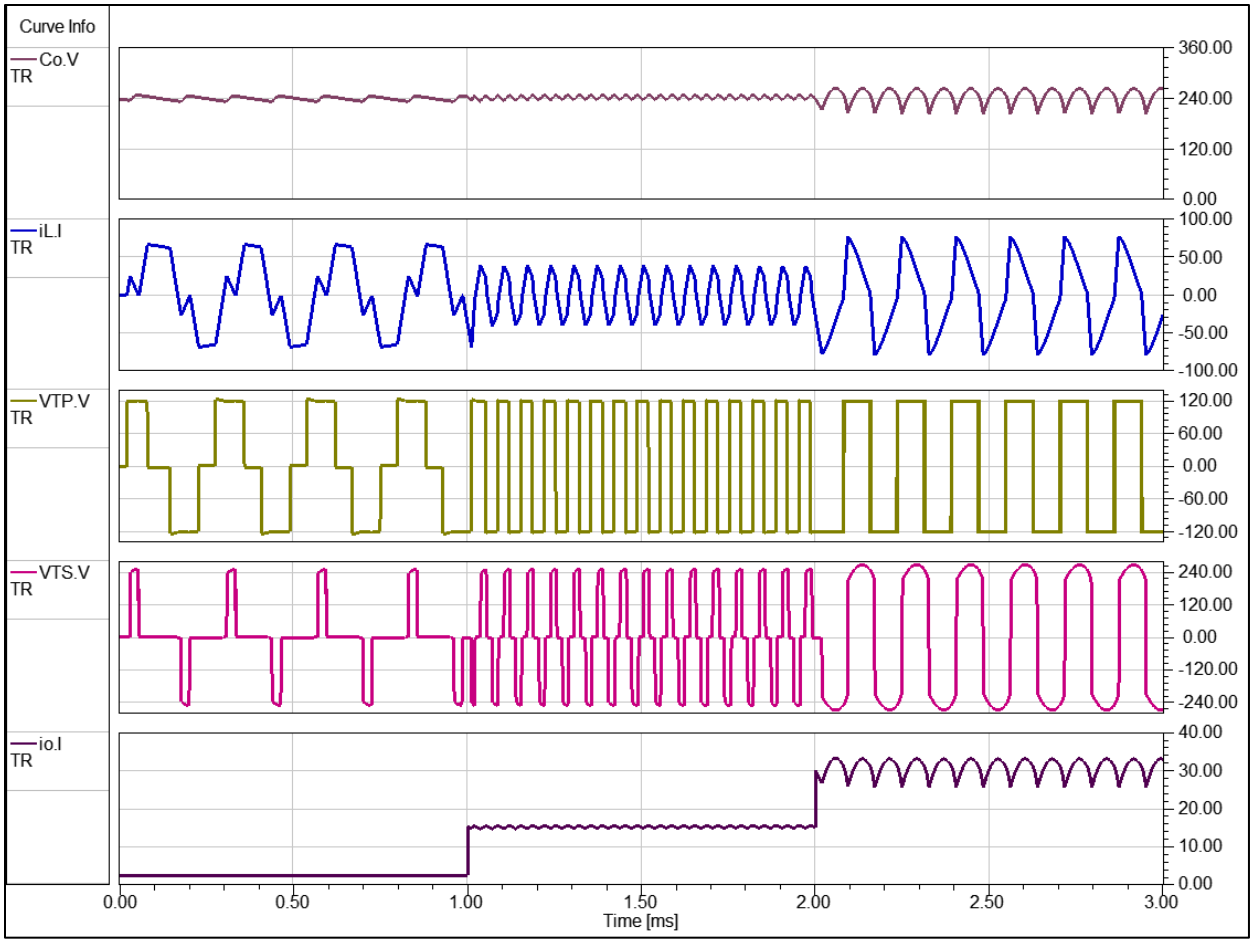


Figure 69: Comparative Study between Burst Mode for the Efficiency Case Study and Life Preservation Mode

Note the significantly increased current in *ML* in Figure 69 in contrast to MB in of Section 4.4. In Figure 70 the junction temperatures are presented, increasing and decreasing with every corresponding mode change. Figure 71 displays the binary gate signals come from the NNS control scheme effecting switching accordingly. Lastly, Figure 73 shows the subdivided normalized state plane for the duration of the case, and Figure 72 shows the nominal state plane for *ML* only. This case demonstrates the trade-off in control design between reliability and efficiency. The trade-off remains with the deisgn of *ML*, and the balanced priority is to be determined by the designer.

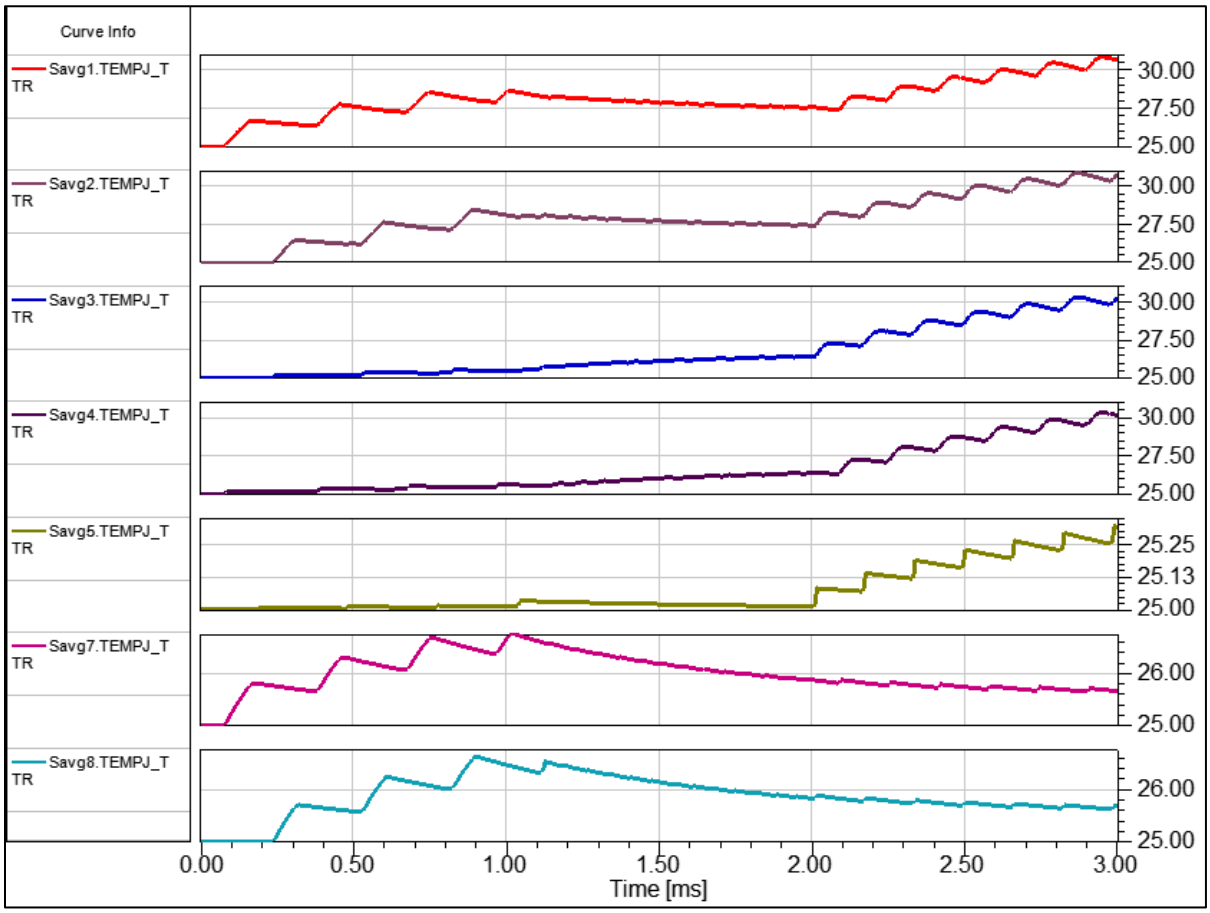


Figure 70: Junction Temperature per MOSFET for Case Study Comparison Employing *ML* in Light Loading

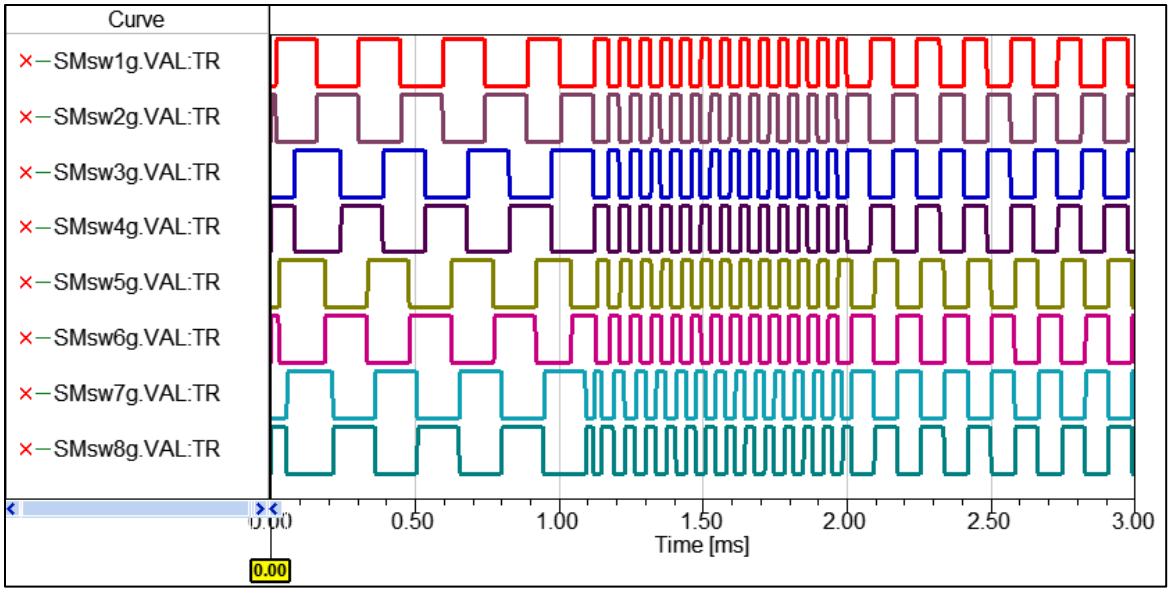


Figure 71: Binary Gate Signals for the Duration of the Case Study Comparison Employing *ML* in Light Loading

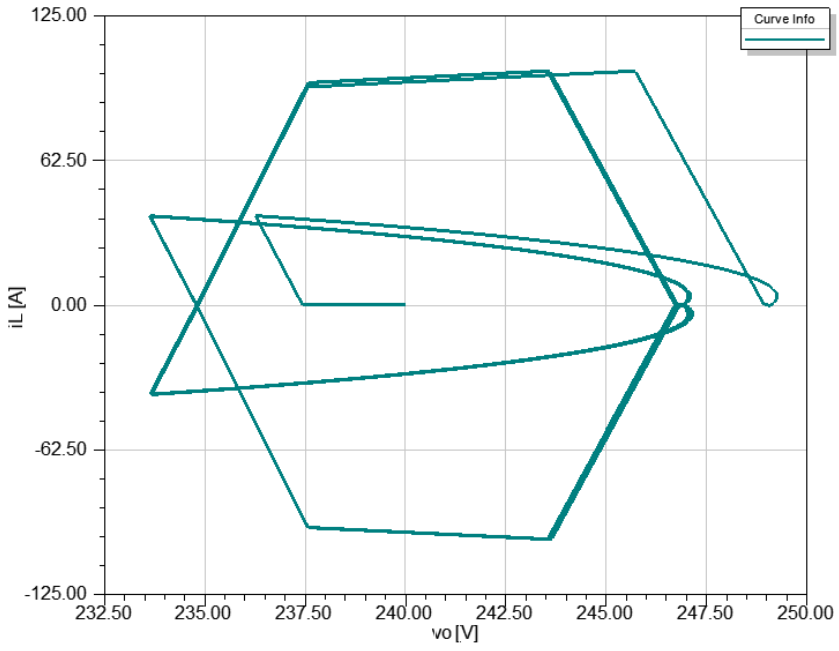


Figure 72: Nominal State Plane of *ML* for Case Study Comparison Employing *ML* in Light Loading

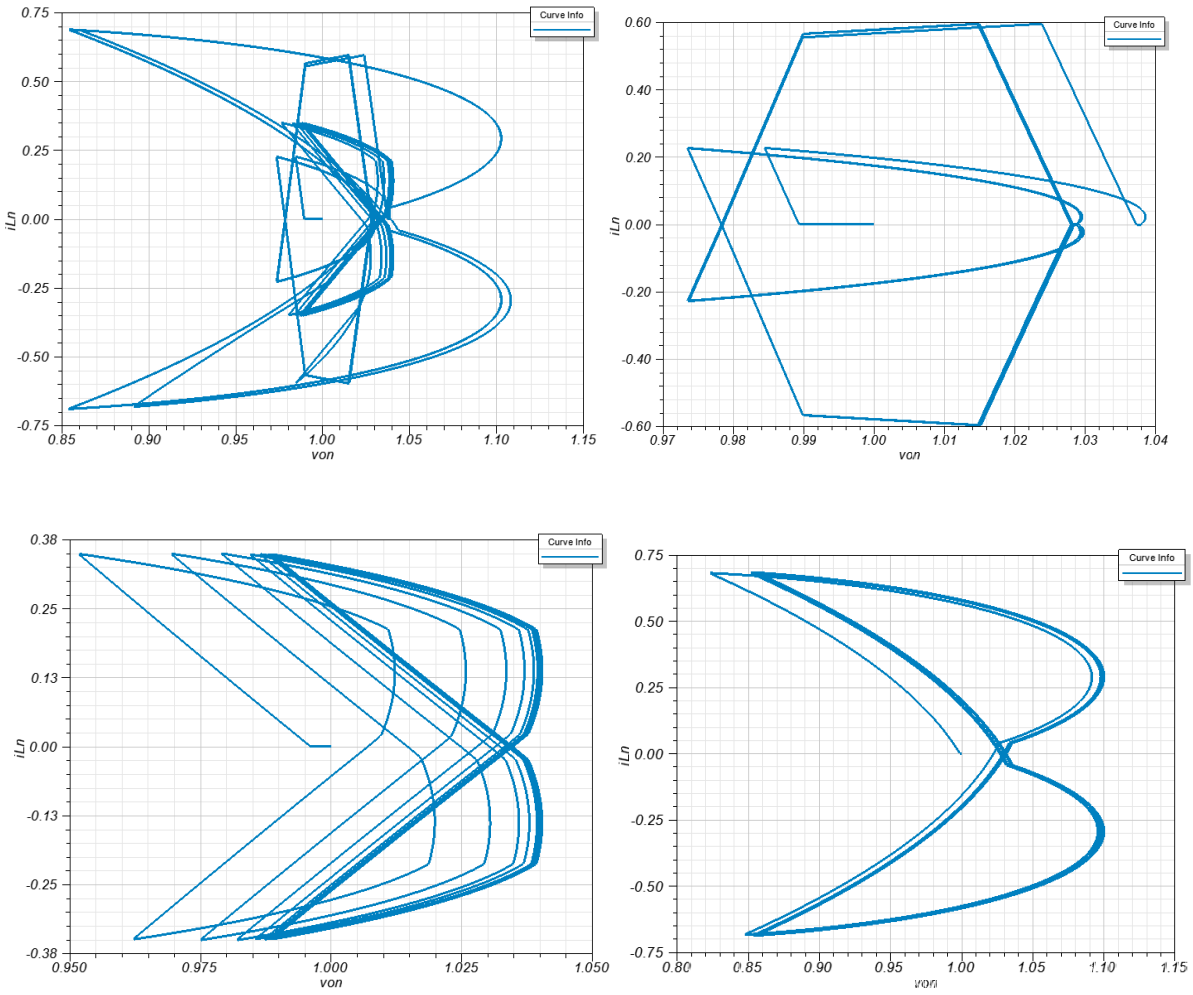


Figure 73: Normalized State Plane for Case Study Comparison Employing *ML* in Light Loading, Including Entire Duration (top left) and Subdivided State Planes per Trajectory Mode (left to right top to bottom)

5.3.3 Implementing Burst Mode for Interval Based Loading

The following results demonstrate the dramatic cooling effected by the burst mode operation when serving an interval based load. Burst mode is amazing for efficiency's sake, but as would be expected it increases thermal cycling. The timing sequence of this simulation is to operate in M4 from 0 to 7ms, in MB from 7 to 11.5ms. The operating parameters are provided in Table 24. The

figures provided here are comparable to what has been presented for previous cases, with specific descriptions found in captions as needed. It is noteworthy that the most significant thermal cycling magnitude from the measured performance on all devices is approximately 6.7 degrees Celsius as seen in Figure 75 or Figure 76.

Table 24: Parameters for Burst Mode Simulation in Thermal Cycling Assessment

Parameter:	Value:	Description
M	[*M4, MB*]	Modes of strategic trajectories in order
P_{o}	[7.2kW, 600W]	Output power demanded per interval
V_{cc}	120	Input voltage
V_{o}	240	Output voltage (V_{ref})
d	$V_o/(nV_{cc})$	Conversion ratio (n = 1.5)
f_{sw}	[4kHz, 10kHz]	Switching frequency per mode
m	[1.0, 0.25]	Modulation index per mode
$V_{\mathrm{on,min}}$	0.95	Minimum normalized output voltage

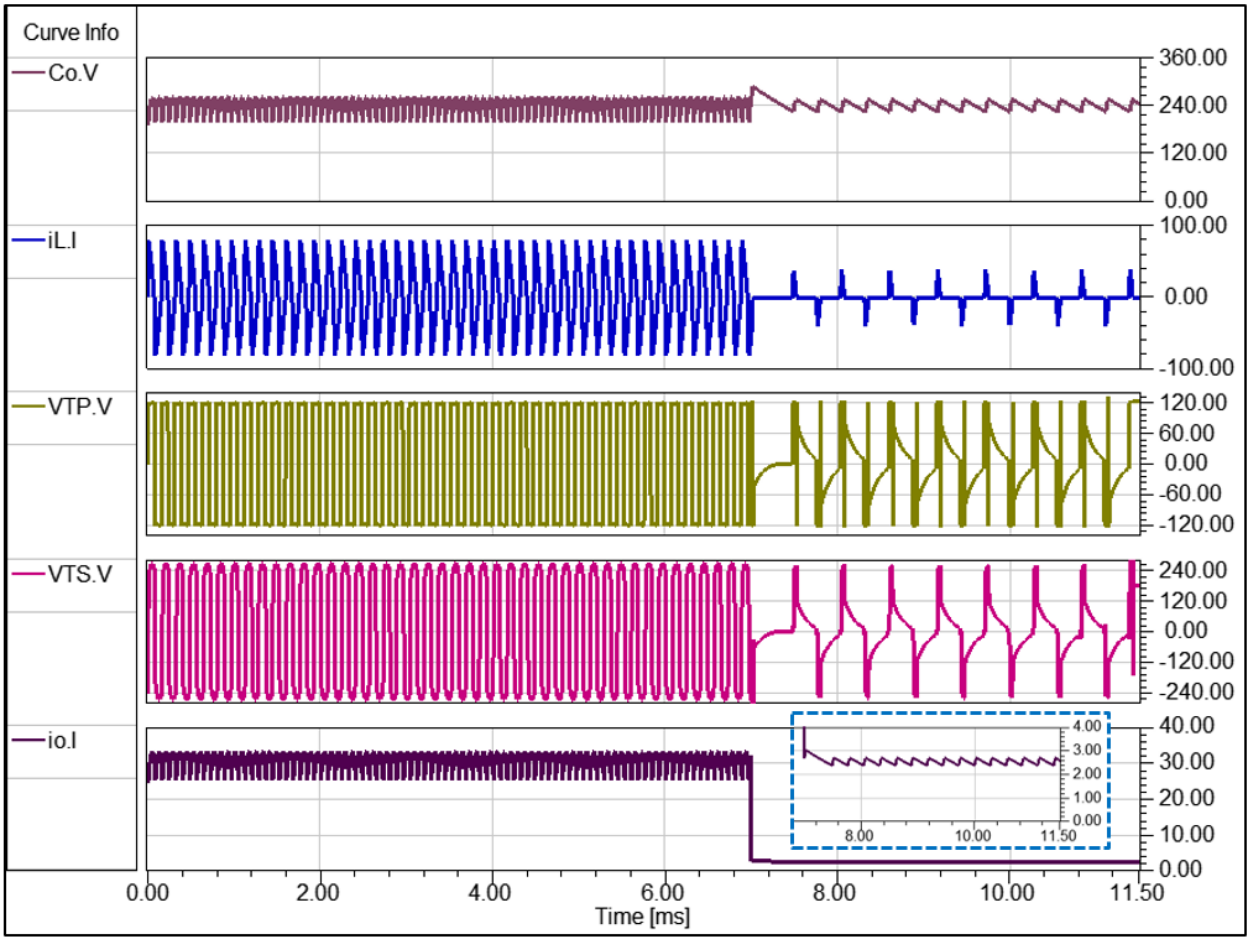


Figure 74: System Waveforms during Interval Loading Employing *MB* during Light Load

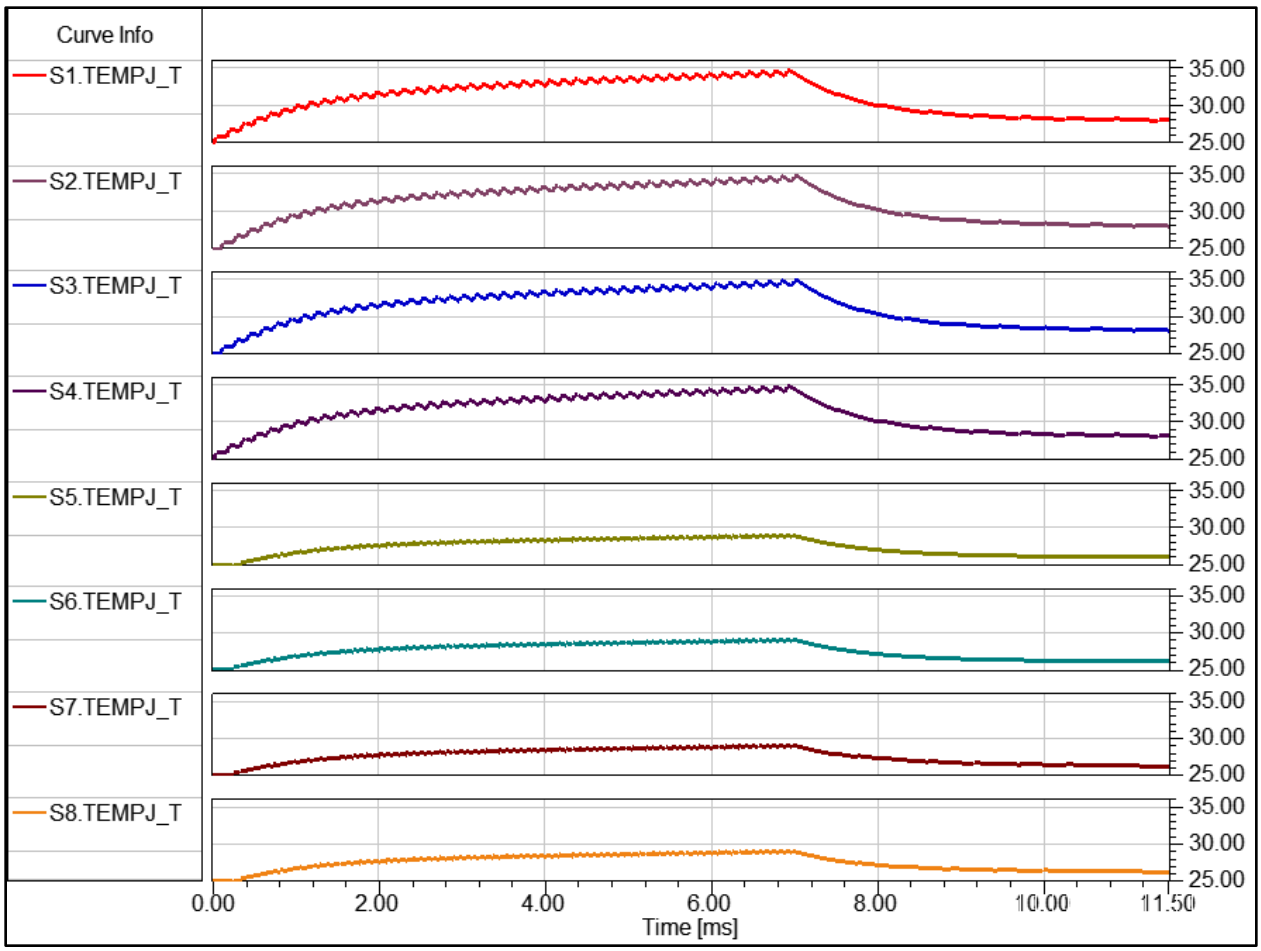


Figure 75: Junction Temperatures for Each MOSFET during Interval Loading Employing *MB* in Light Load

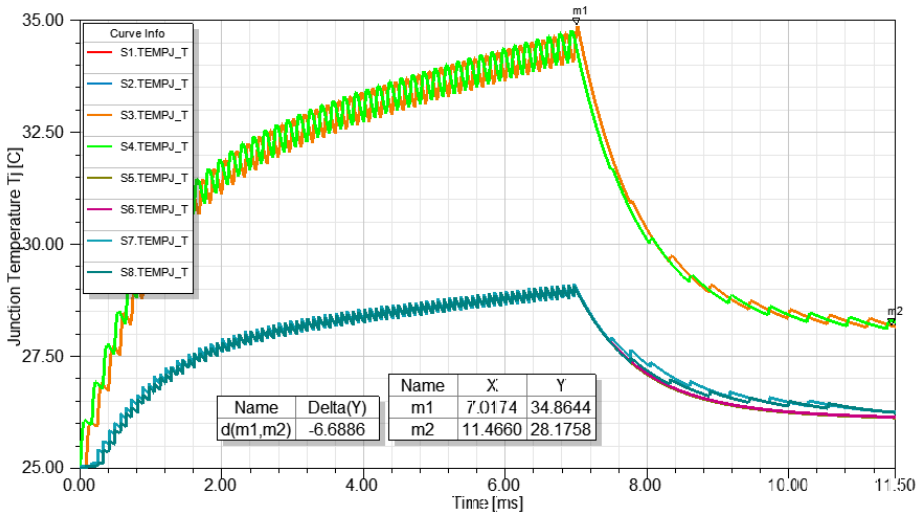


Figure 76: Junction Temperatures for all MOSFETs and ΔT_j during Interval Loading Employing *MB* in Light Load

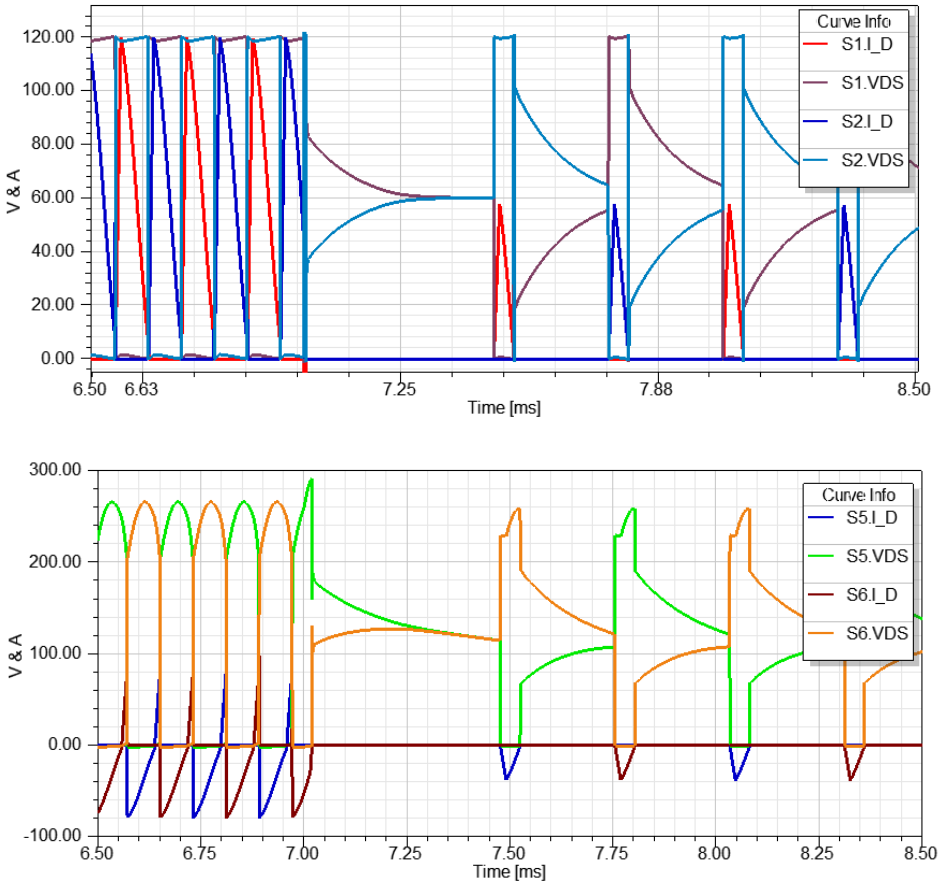


Figure 77: V_{DS} and I_D for switches S_1, S_2, S_5, and S_6 during *MB* operation

5.3.4 Implementing Conventional Control for Interval Based Loading

Critical for the sake of comparison, it is necessary to observe the impacts of conventional dual active bridge control upon thermal cycling. Two cases of results are provided – Case 1 for when heavy and light loading are operated at differingy switching frequencies, and Case 2 for when both heavy and light loading are run at the same switching frequency. Details are provided in Table 25 and Table 26. Conventional control can often function at a set switching frequency across its operating range. The varied switching frequency in addition to the constant case was performed for best comparison to other control mode operations.

Table 25: Parameters for Case 1 of Conventional Control in Thermal Cycling Assessment

Parameter:	Value:	Description
M	[*Conventional*]	Mode of control
P_{o}	[7.2kW, 1.2kW]	Output power demanded per interval
V_{cc}	120	Input voltage
V_{o}	240	Output voltage (V_{ref})
d	$V_o/(nV_{cc})$	Conversion ratio (n = 1.5)
f_{sw}	[4kHz, 10kHz]	Switching frequency per mode

Table 26: Parameters for Case 2 of Conventional Control in Thermal Cycling Assessment

Parameter:	Value:	Description
M	[*Conventional*]	Mode of control
P_{o}	[7.2kW, 1.2W]	Output power demanded per interval
V_{cc}	120	Input voltage
V_{o}	240	Output voltage (V_{ref})
d	$V_o/(nV_{cc})$	Conversion ratio (n = 1.5)
f_{sw}	[8kHz, 8kHz]	Switching frequency per mode

At the end of the day, these results show us differing deep thermal cycles of approximately 6.4 (Case 1) and 10.2 (Case 2) degrees Celsius. This difference is simply due to the fact that Case 2 ran the heavy loading at a higher switching frequency heating up devices by increased switching loss to 40 Celsius in contrast to 32 Celcius in Case 1 that only switched at 4kHz. This is the exact reasoning as to why Case 1 was run in the first place, for a better comparison to other control mode cases that all run heavy loading at 4kHz.

Case 1: Different Switching Frequencies for Heavy (4kHz) and Light (10kHz) Loading

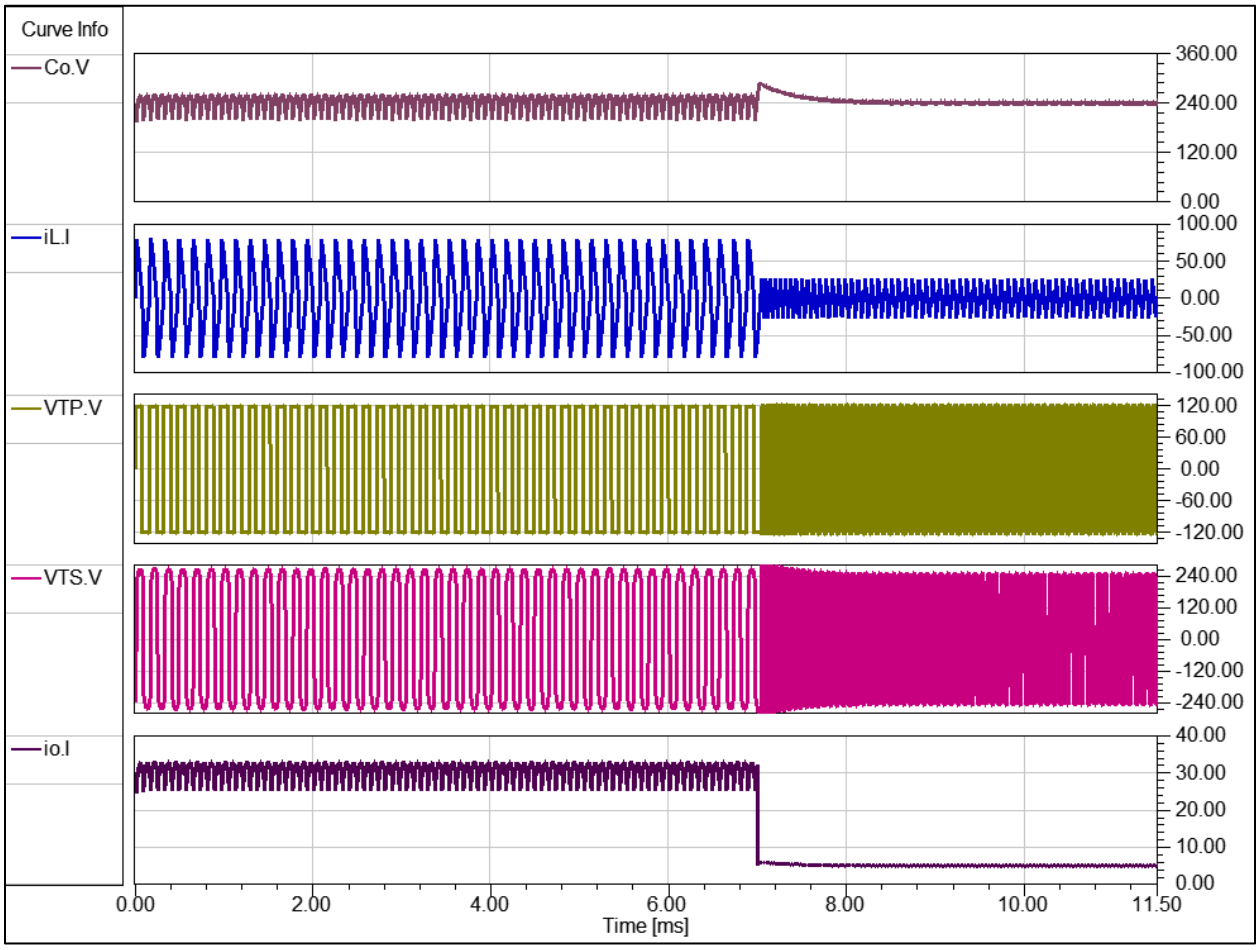


Figure 78: System Waveforms during Interval Loading Employing Conventional Control for all Loads Case 1

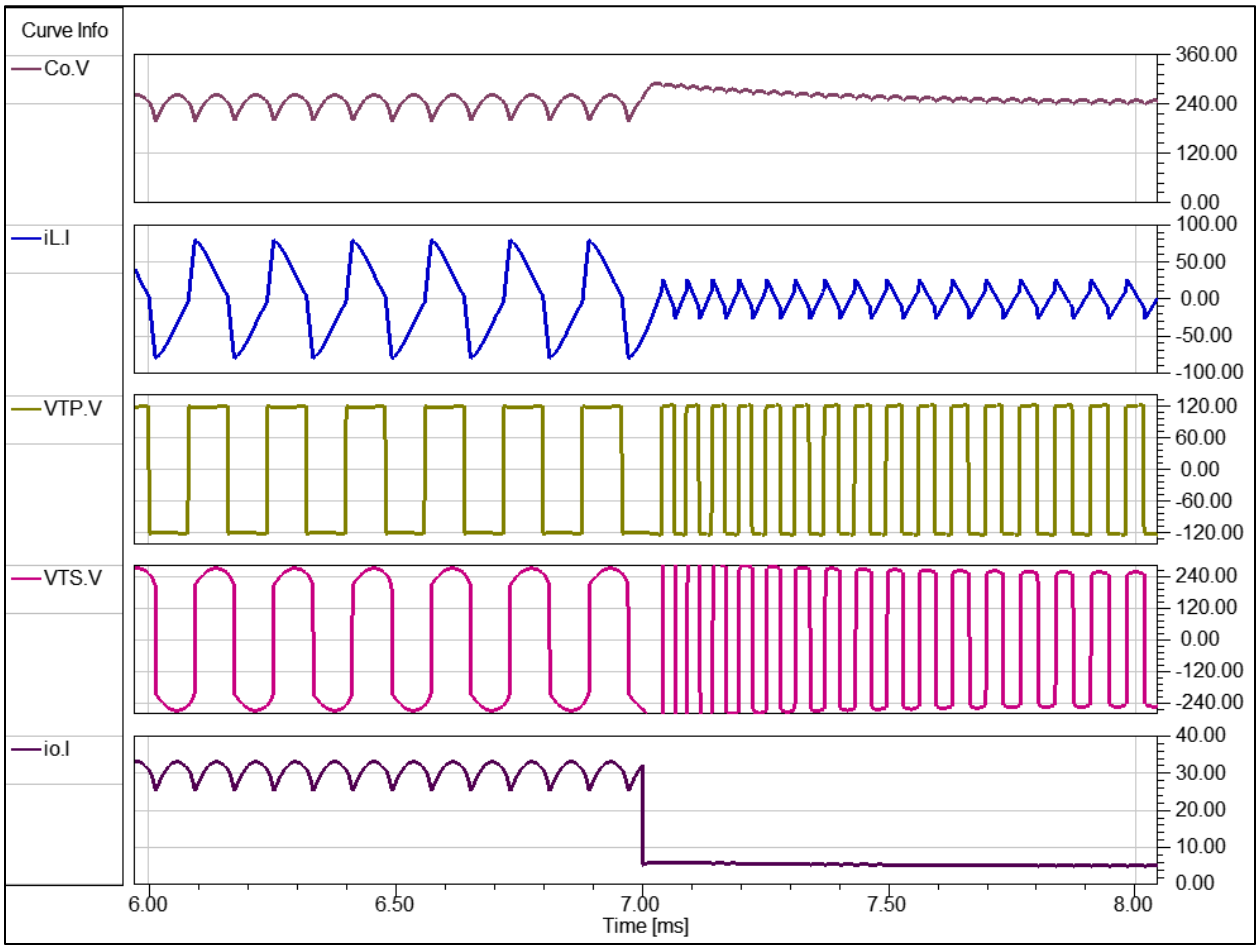


Figure 79: System Waveforms Transient Performance using Conventional Control Case 1

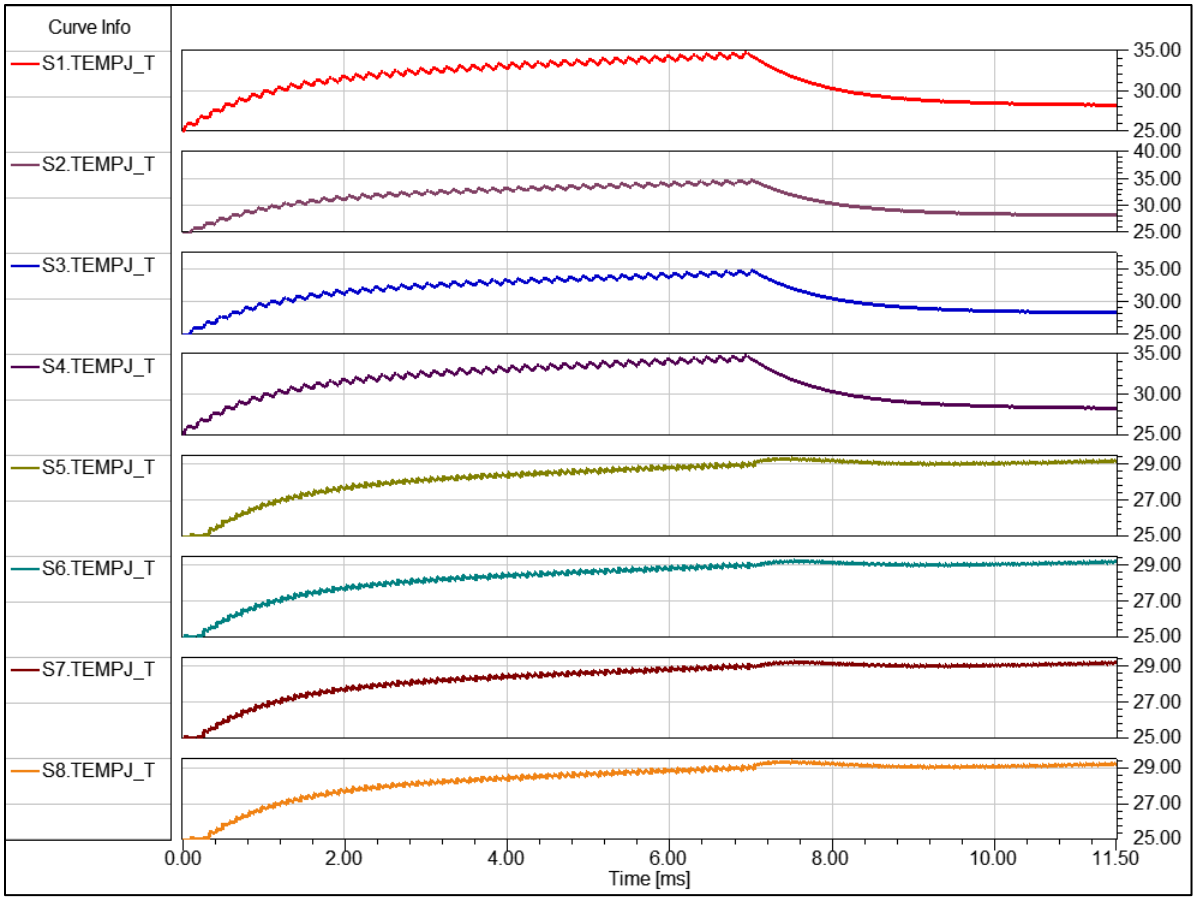


Figure 80: Junction Temperatures for each MOSFET Employing Conventional Control Case 1

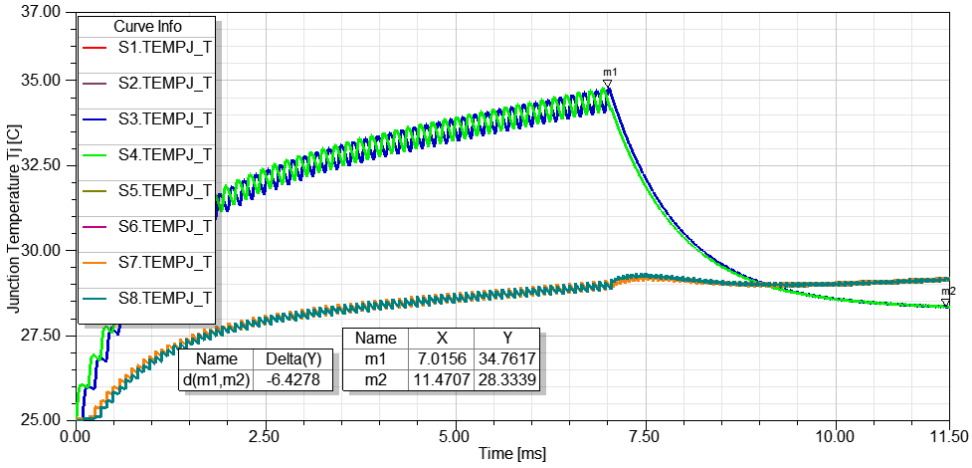


Figure 81: Junction Temperatures for each MOSFET Superimposed with Delta Marker Measurement Case 1

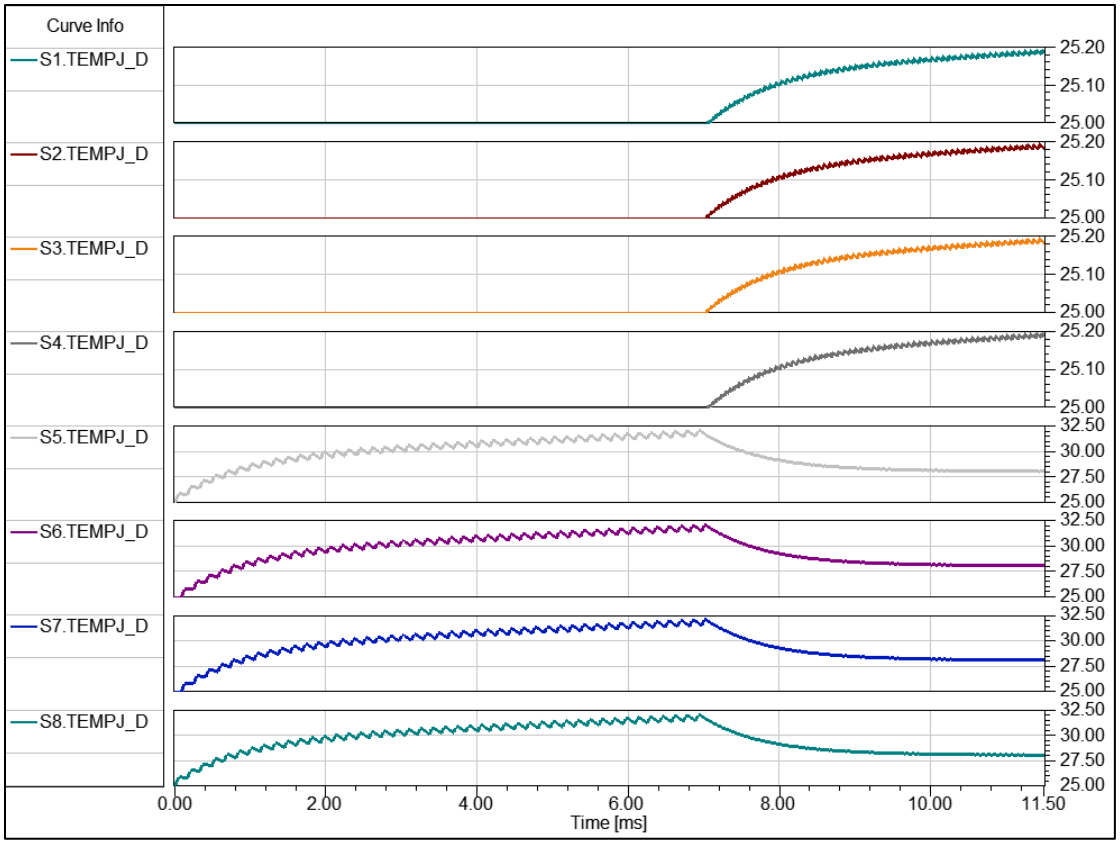


Figure 82: Junction Temperatures for each Schottky Diode Employing Conventional Control Case 1

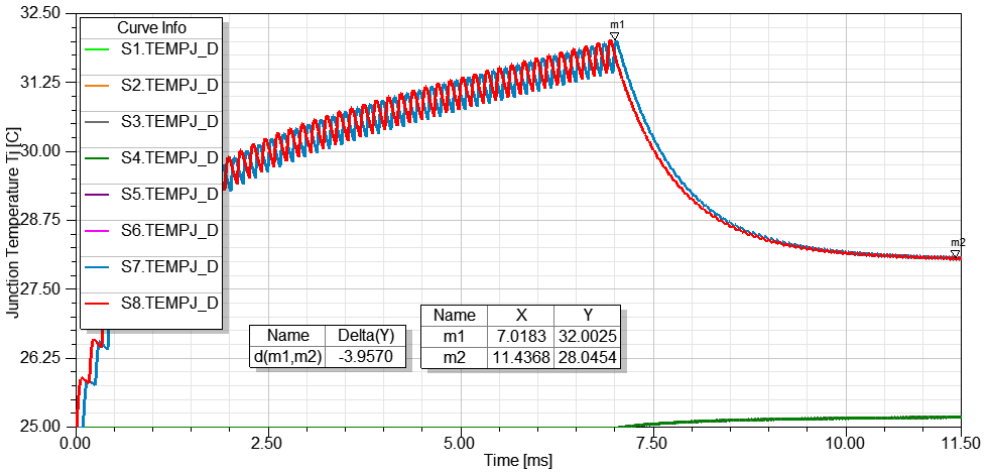


Figure 83: Junction Temperatures for each Diode Superimposed for Conventional Control Case 1

Case 2: Constant Switching Frequency at 8kHz

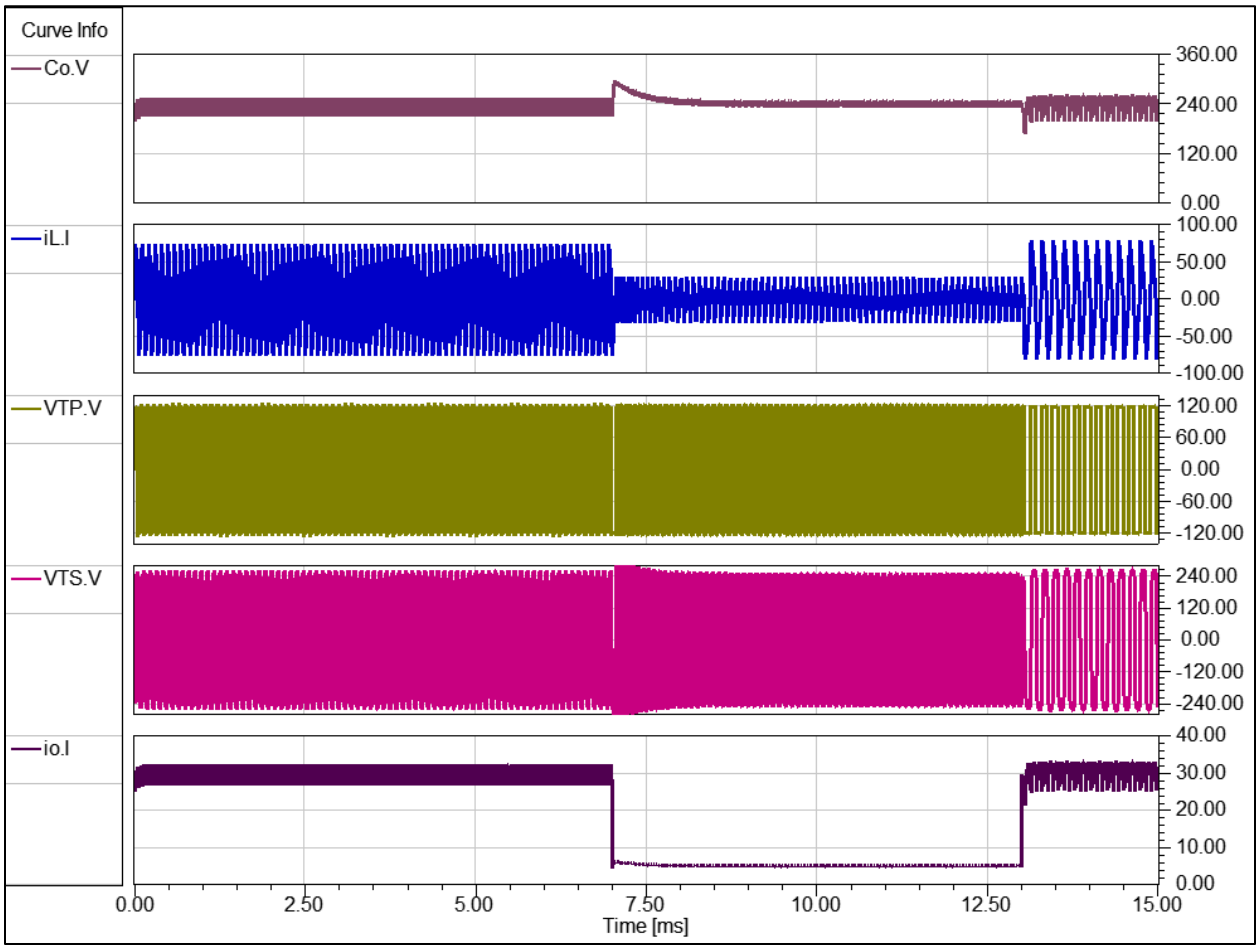


Figure 84: System Waveforms during Interval Loading Employing Conventional Control for all Loads Case 2

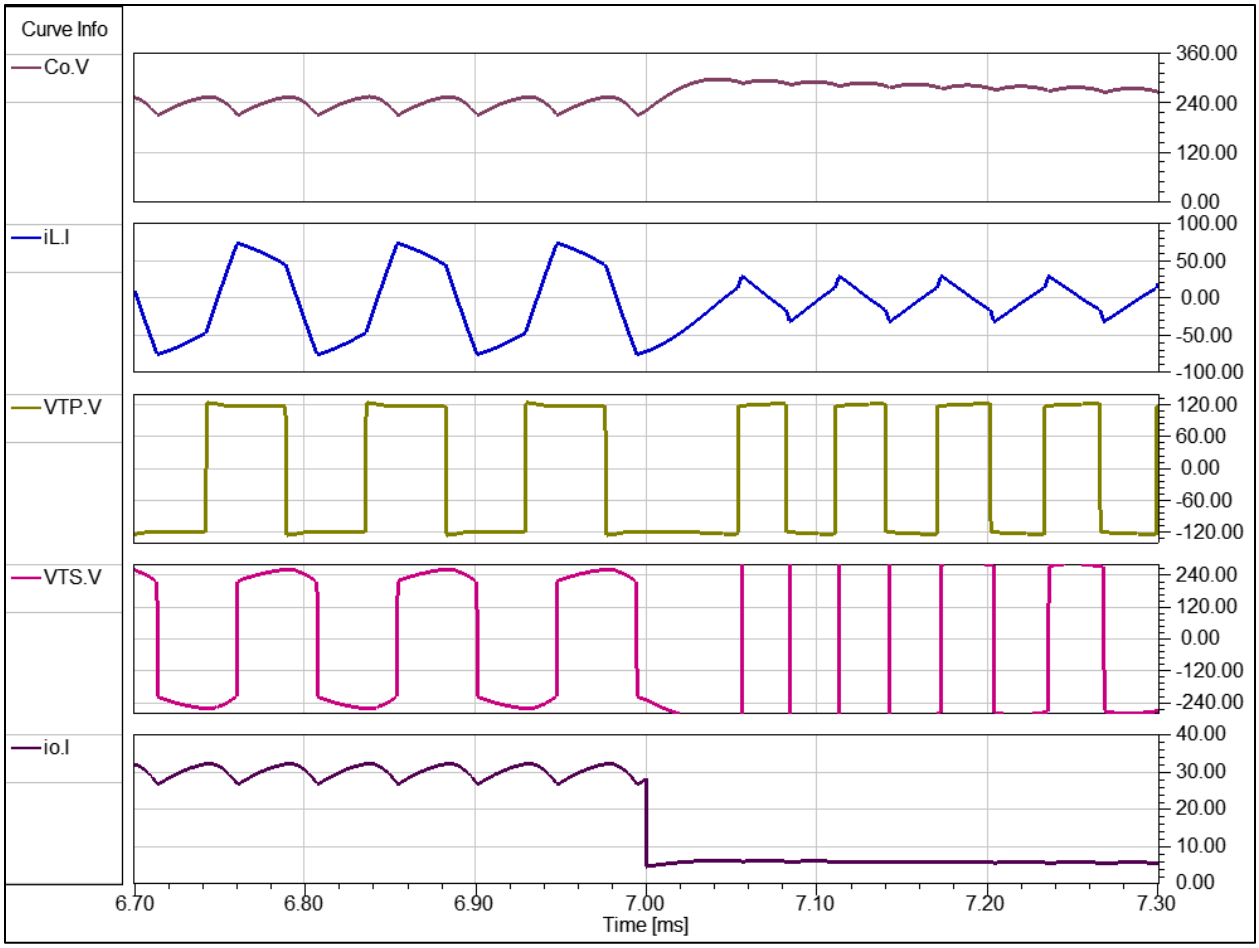


Figure 85: System Waveforms Transient Performance from Heavy to Light Loading Conventional Control Case 2

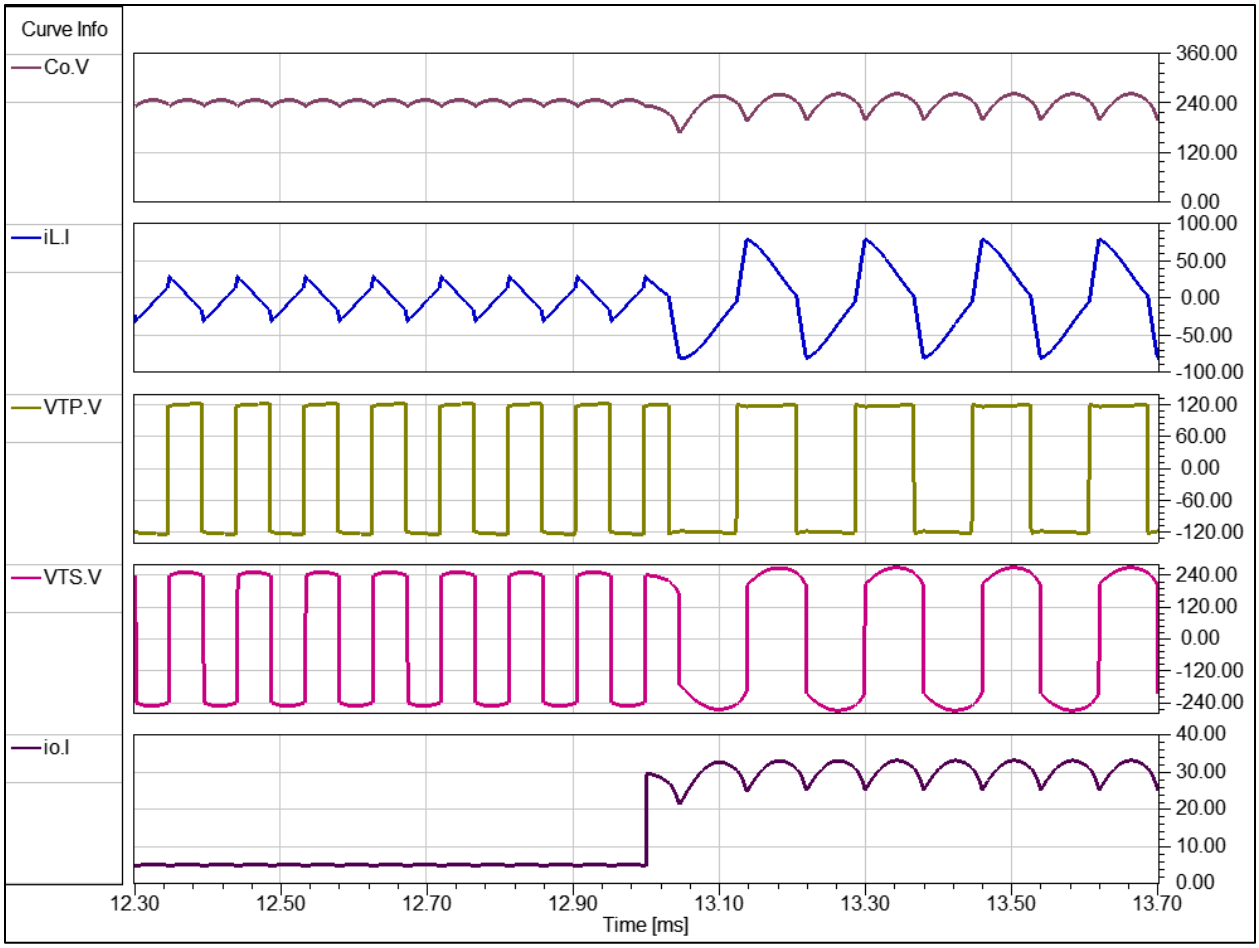


Figure 86: System Waveforms Transient Performance from Light to Heavy Loading Conventional Control Case 2

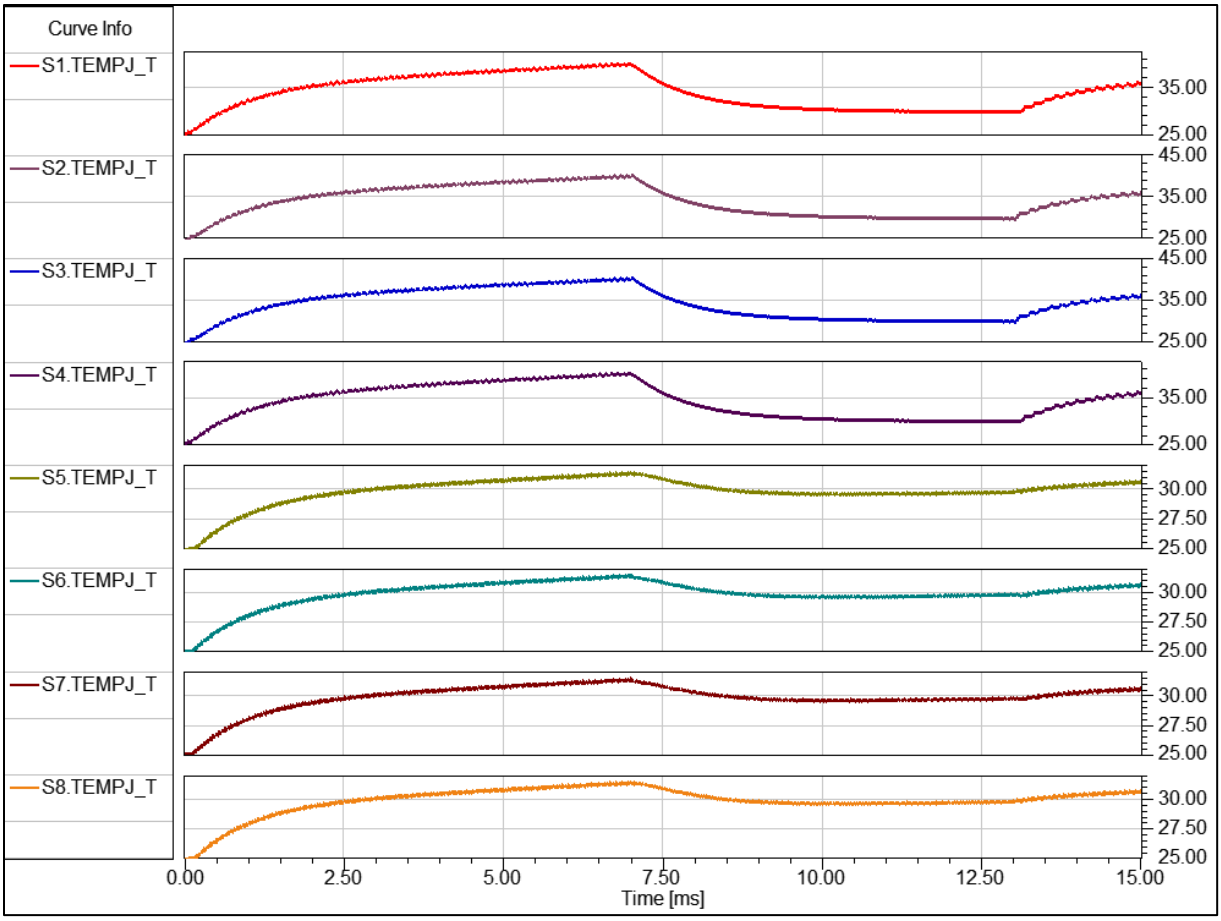


Figure 87: Junction Temperatures for each MOSFET Employing Conventional Control Case 2

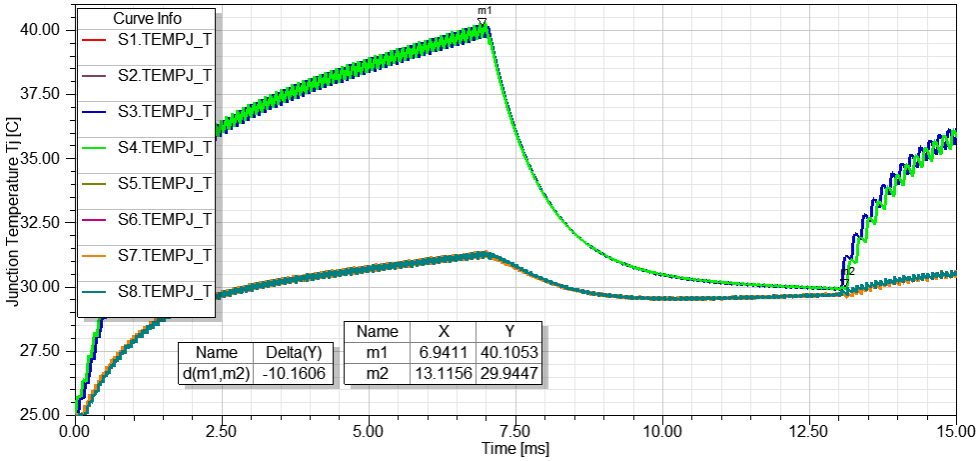


Figure 88: Junction Temperatures for each MOSFET Superimposed with Conventional Control Case 2

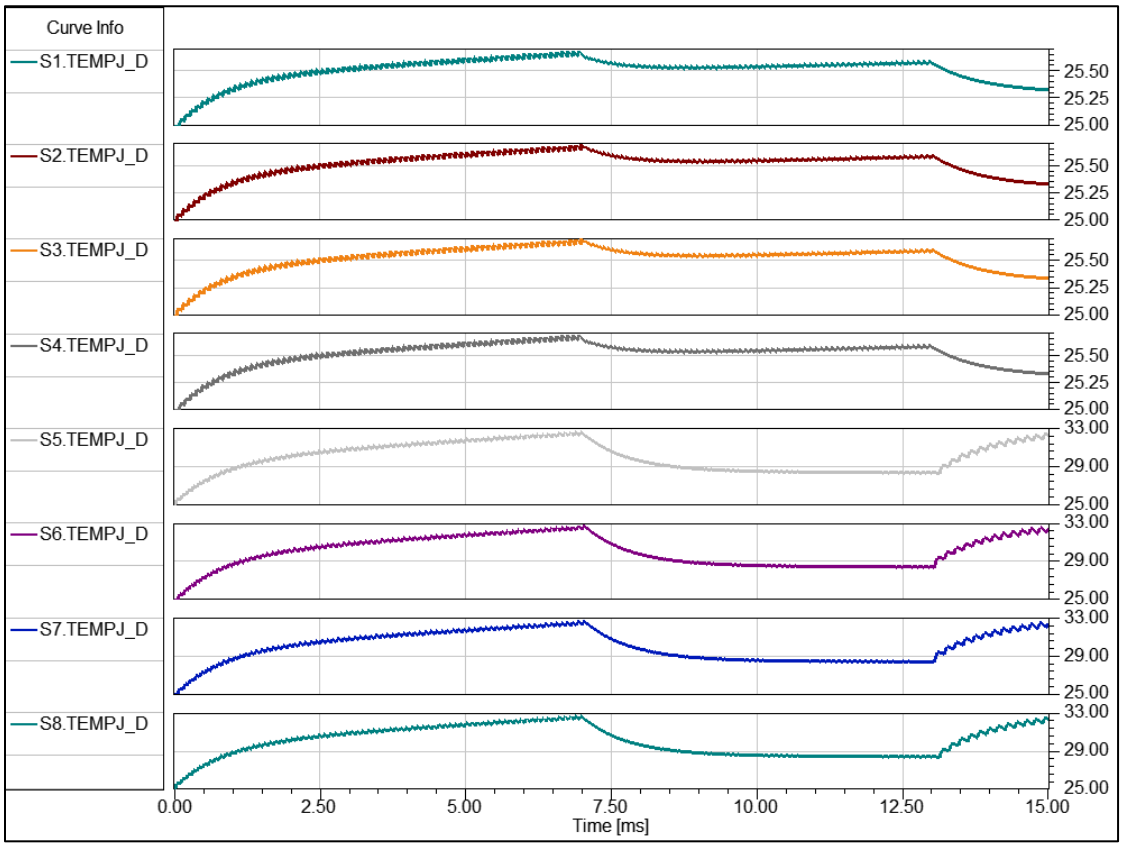


Figure 89: Junction Temperatures for each Schottky Diode Employing Conventional Control Case 2

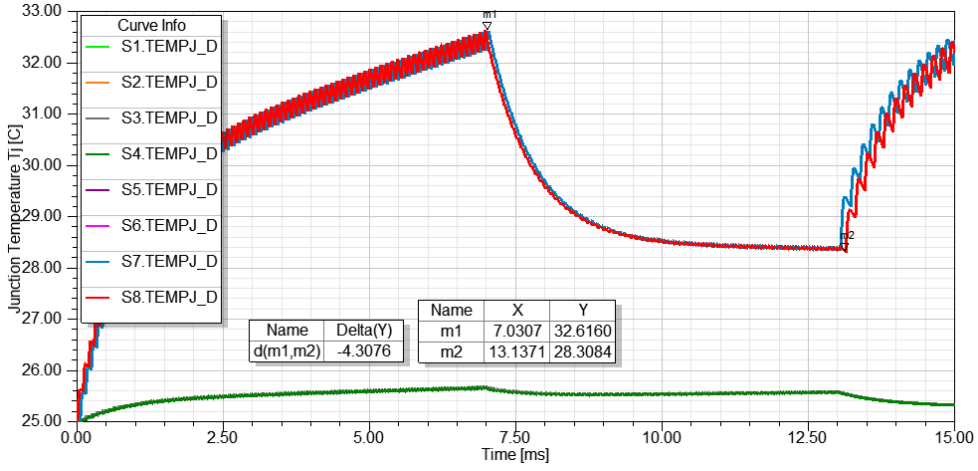


Figure 90: Junction Temperatures for each Schottky Diode using Conventional Control Case 2

5.3.5 Implementing ATBC for Interval Based Loading

The following results reveal the impact that active thermal boundary control has upon the thermal cycling of the devices. There are four cases demonstrating the flexibility of ATBC. These cases are differentiated by where the threshold $I_{L,max}$ is set, since this parameter is the most effective control handle of choice to control how much heating occurs on the junction of the devices. The four cases presented are for $I_{L,max}$ = [50A, 80A, 100A, 120A] and in that order labeled Case 1 through Case 4, respectively. All other pertinent system simulation parameters for each of these $I_{L,max}$ cases are defined in Table 27.

Table 27: Simulation Parameters for ATBC Implemented during Interval Based Loading Conditions

Parameter:	Value:	Description
M	[*M4, ML, M4*]	Modes of strategic trajectories per load
P_o	[7.2kW, 600W, 7.2kW]	Output power demanded per load
V_{cc}	120	Input voltage
V_o	240	Output voltage (V_{ref})
d	$V_o/(nV_{cc})$	Conversion ratio (n = 1.5)
f_{sw}	[4kHz, 10kHz, 4kHz]	Switching frequency per mode
m	[0.1, 0.25, 1.0]	Modulation index per mode
$V_{on,max}$	0.99	Normalized output voltage minimum

Case 1: $I_{L,max}$ = 50A

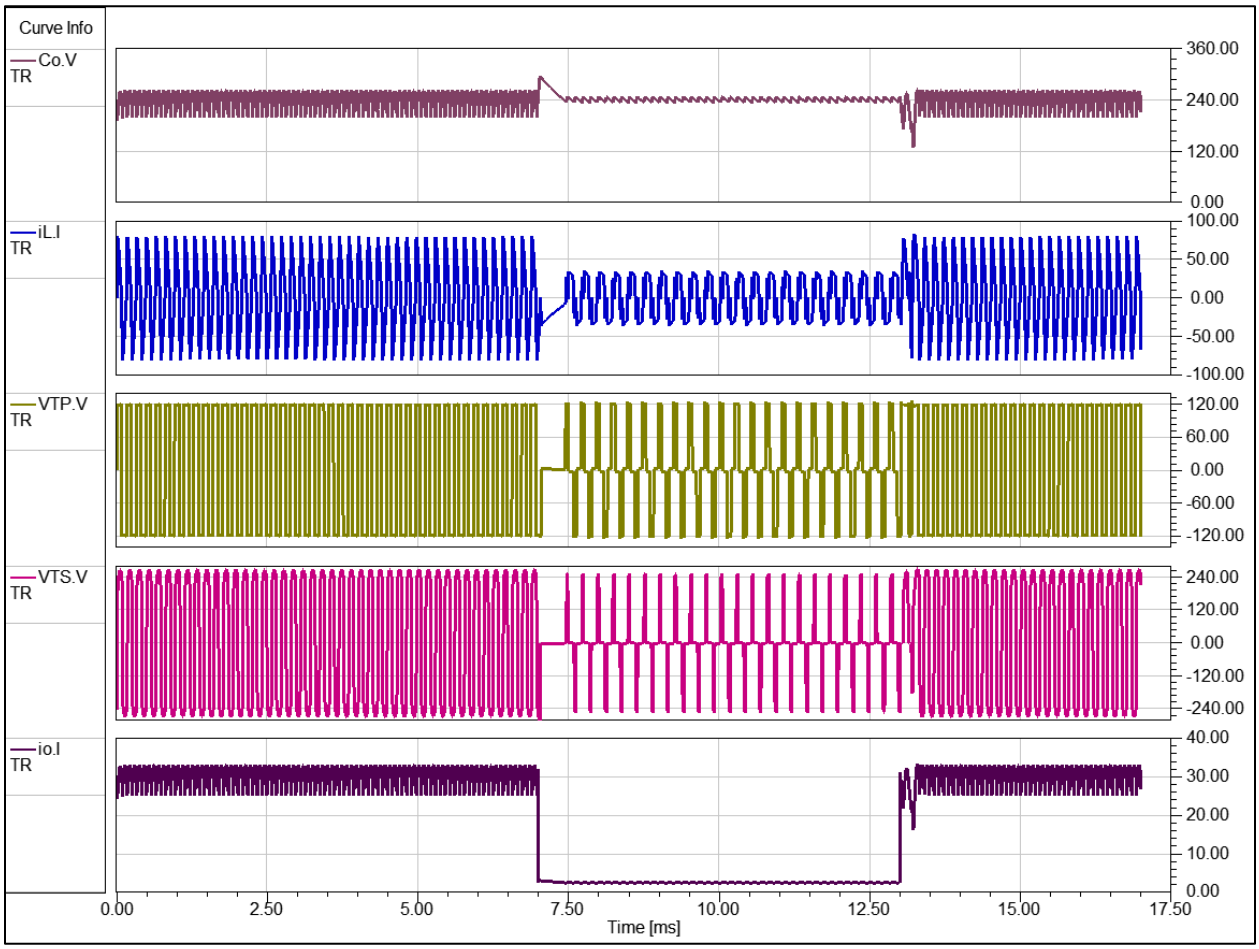


Figure 91: System Waveforms during Interval Loading with *ML* Maximum Current at 50A

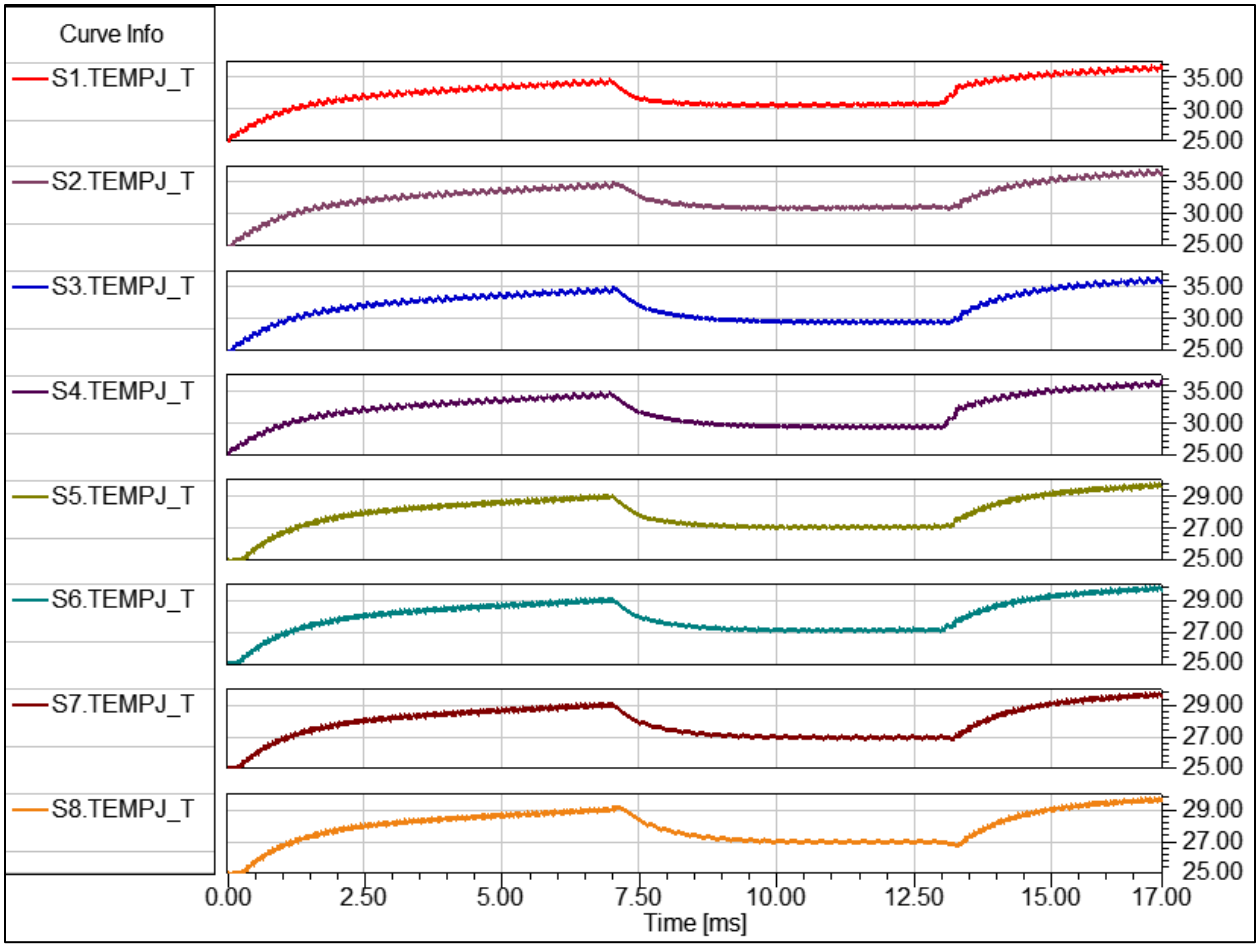


Figure 92: Junction Temperatures on each MOSFET during Interval Loading with *ML* Maximum Current at 50A

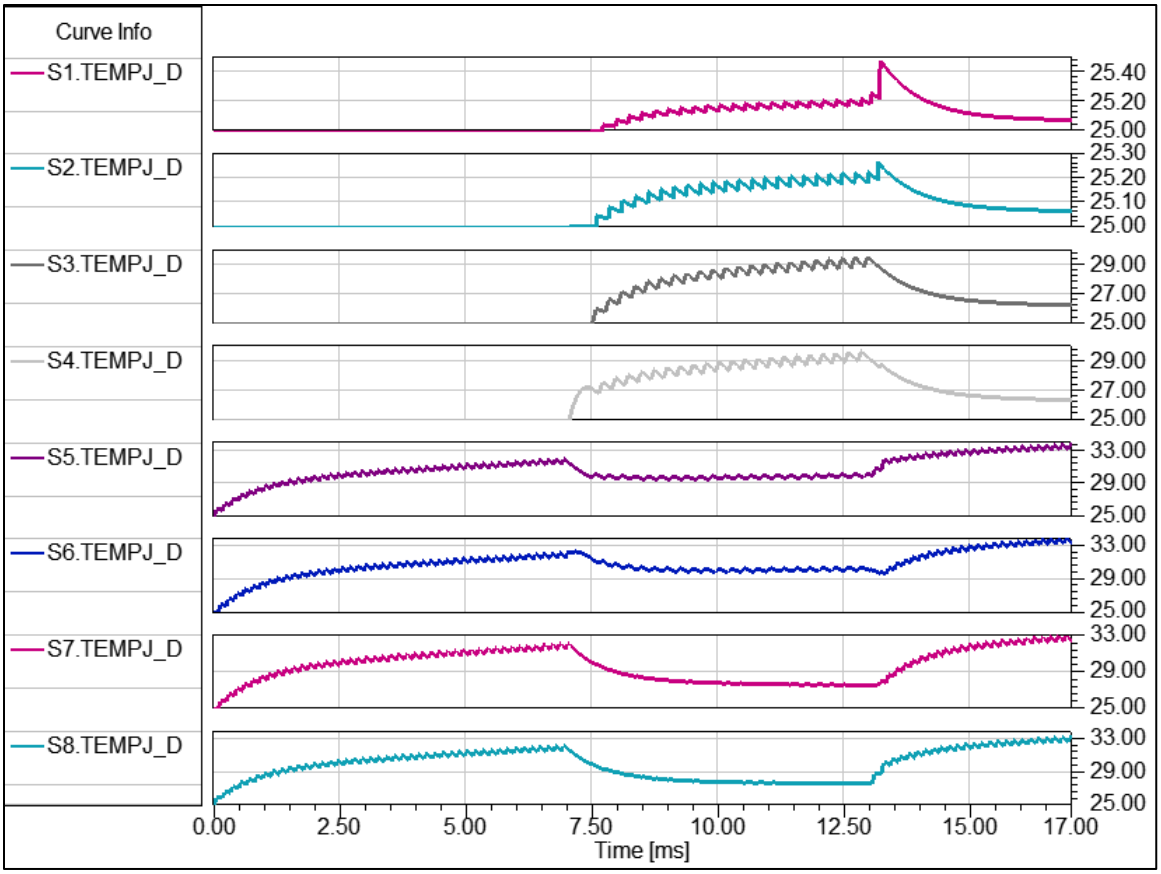


Figure 93: Junction Temperatures on each Schottky Diode during Interval Loading with *ML* Maximum Current at 50A

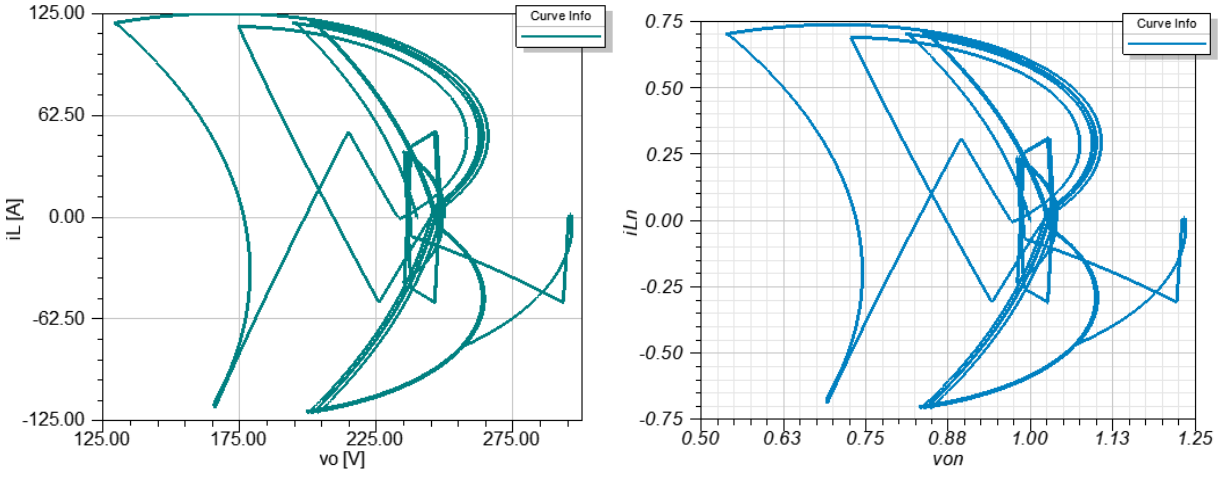


Figure 94: Nominal and Normalized State Planes during Interval Loading with *ML* Maximum Current at 50A

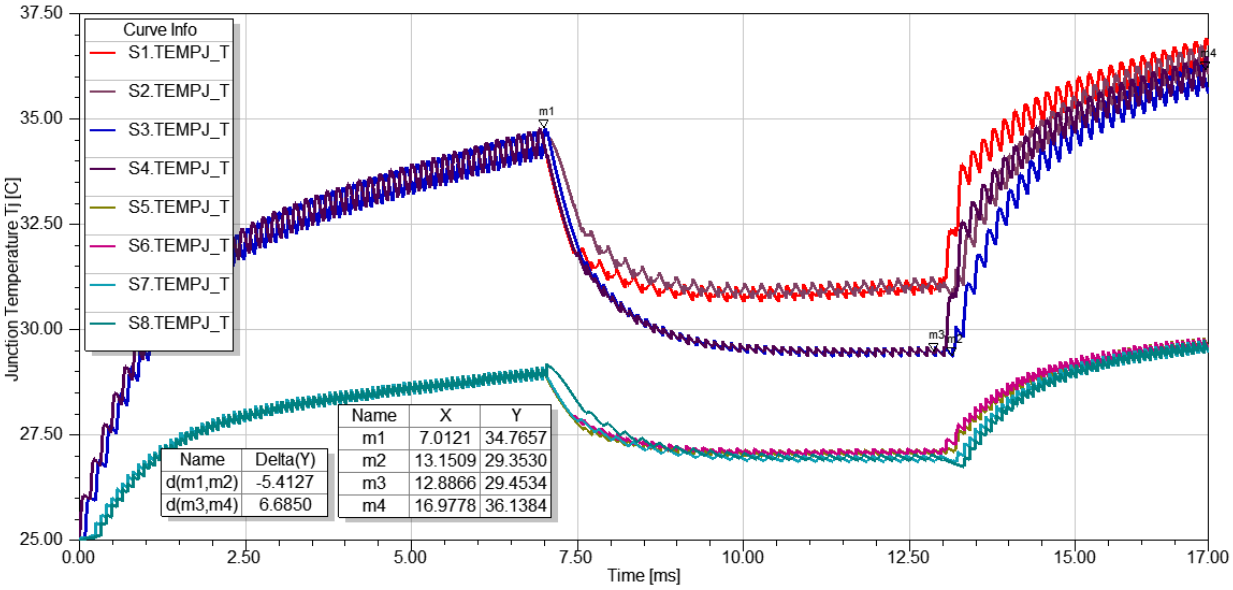


Figure 95: Junction Temperatures on each MOSFET Superimposed with *ML* Maximum Current at 50A

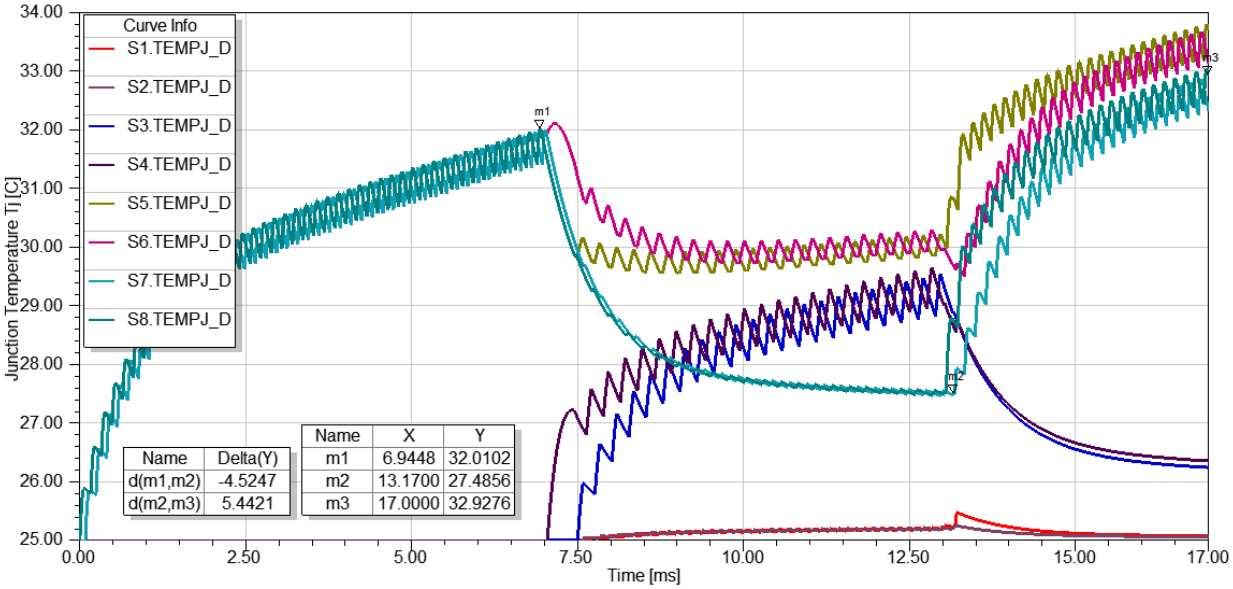


Figure 96: Junction Temperatures on each Schottky Diode Superimposed with *ML* Maximum Current at 50A

Case 2: $I_{L,max}$ = 80A

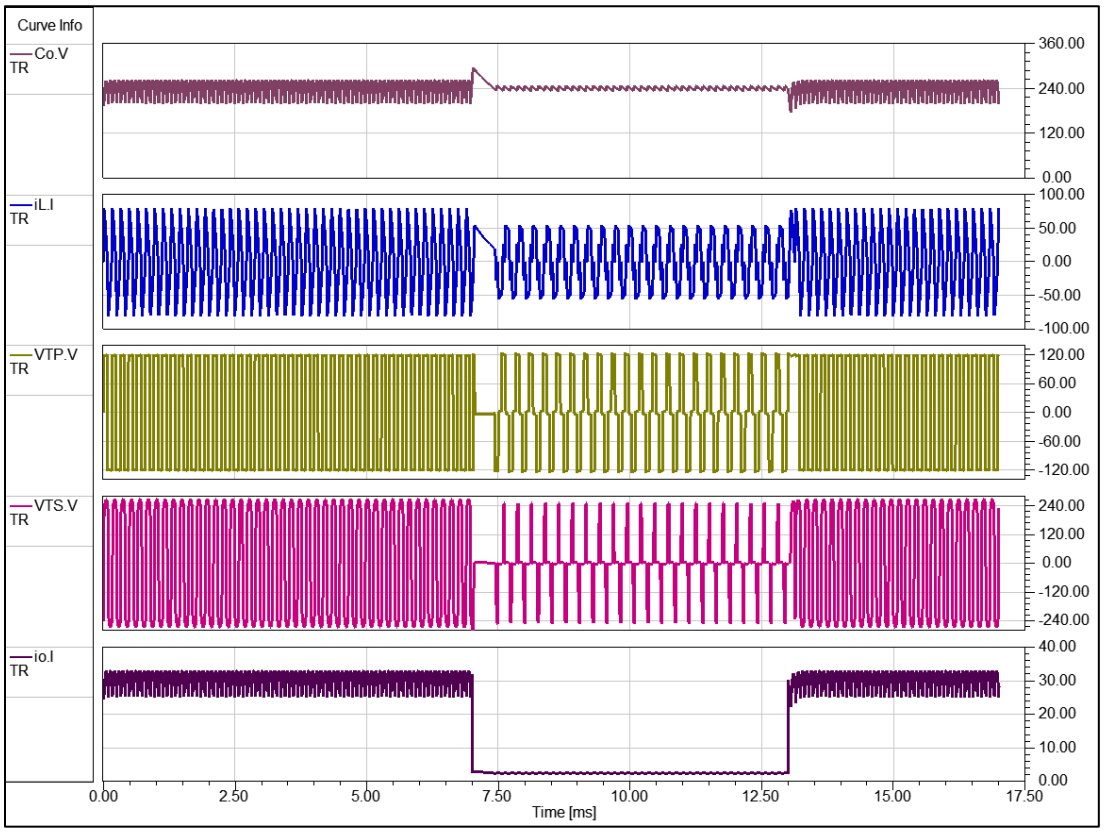


Figure 97: System Waveforms during Interval Loading with *ML* Maximum Current at 80A

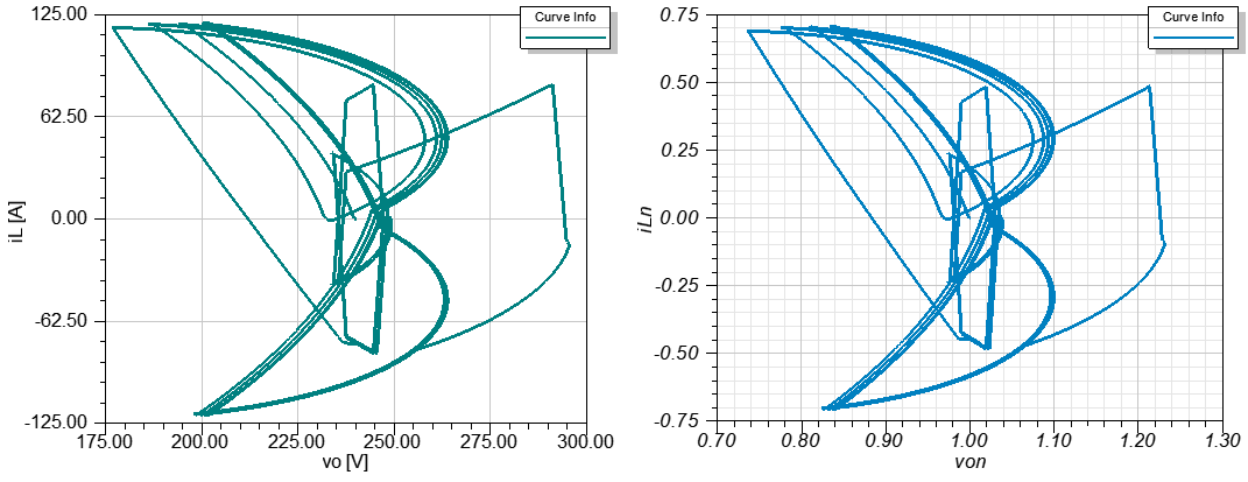


Figure 98: Nominal and Normalized State Planes during Interval Loading with *ML* Maximum Current at 80A

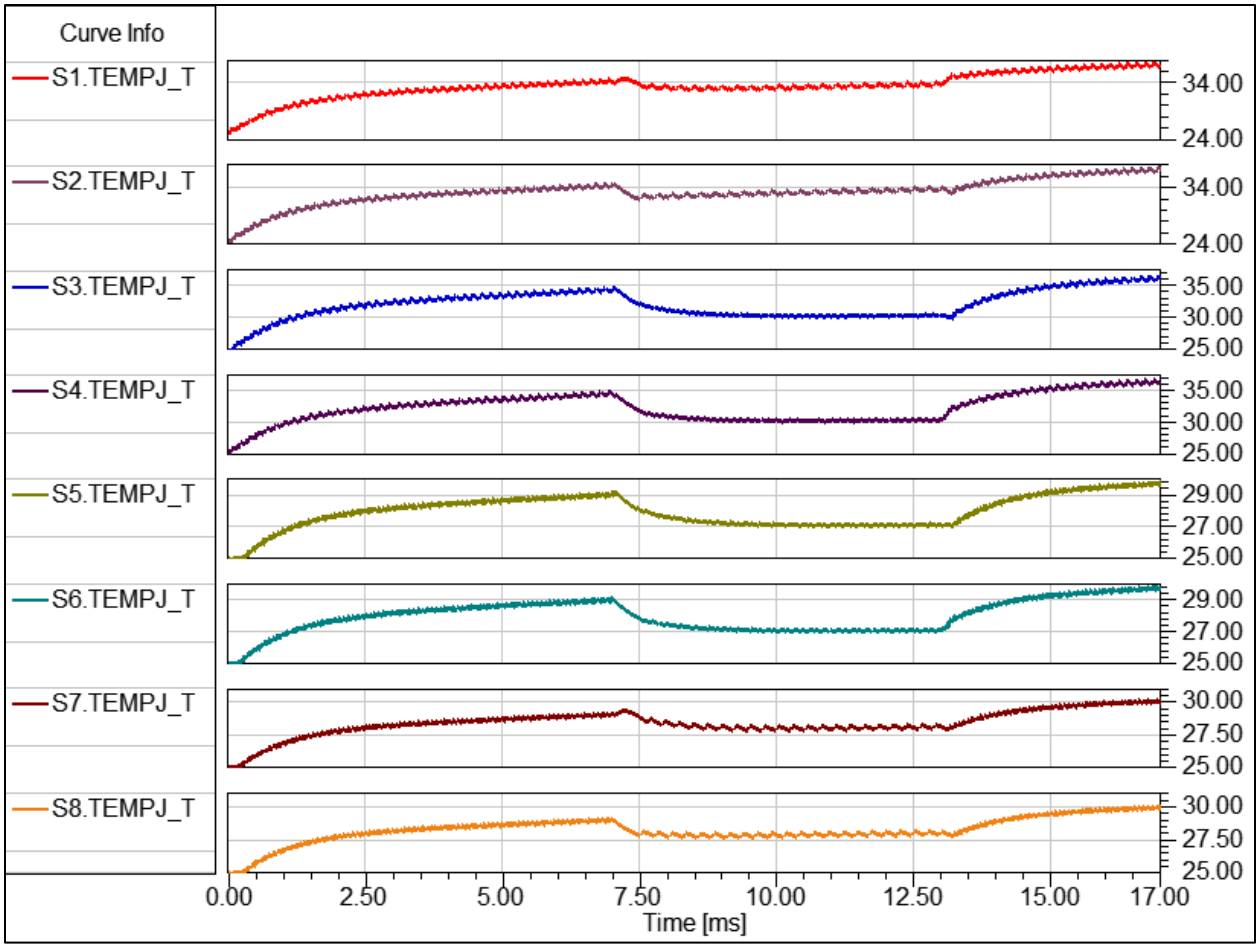


Figure 99: Junction Temperatures on each MOSFET during Interval Loading with *ML* Maximum Current at 80A

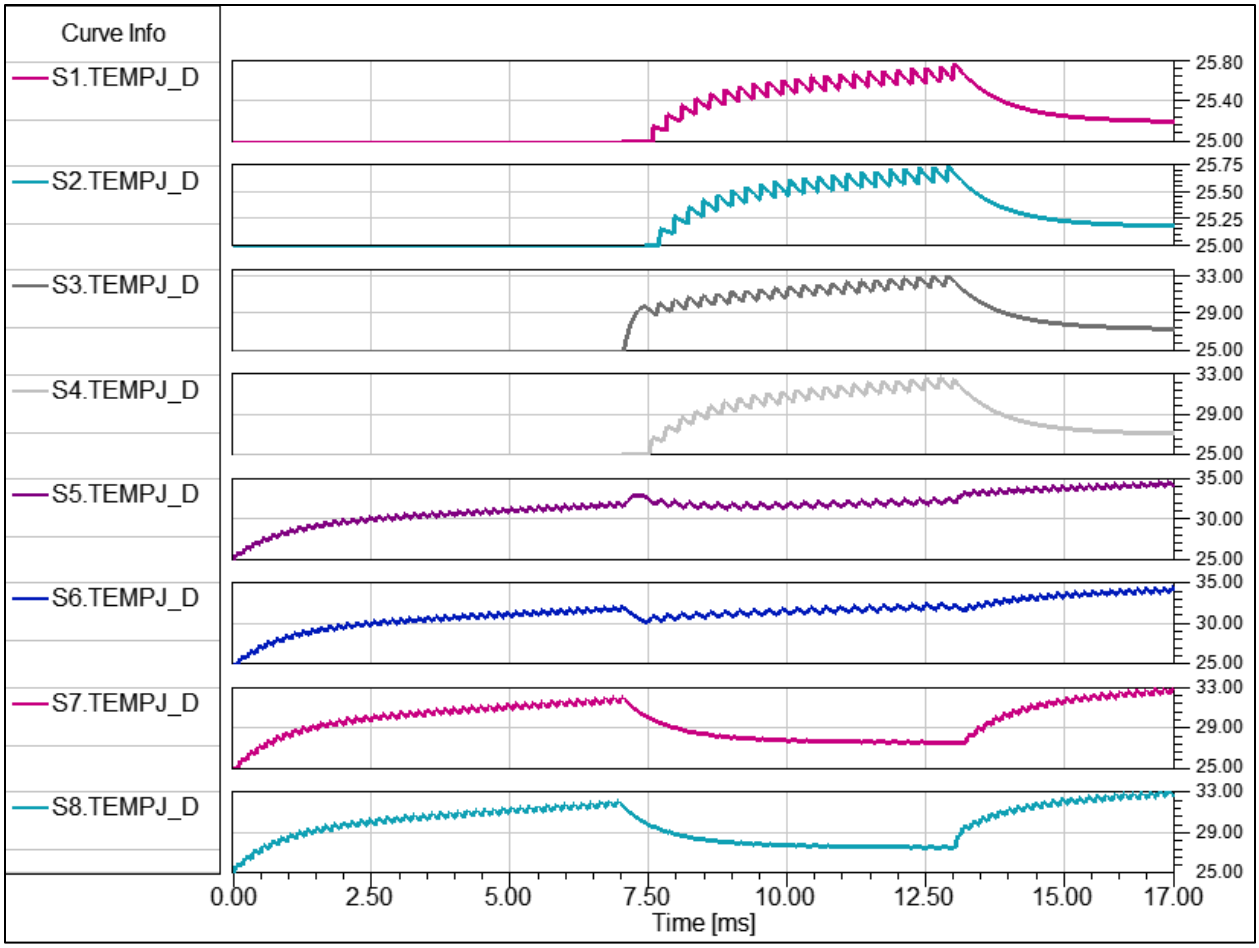


Figure 100: Junction Temperatures on each Schottky Diode during Interval Loading with *ML* Maximum Current at 80A

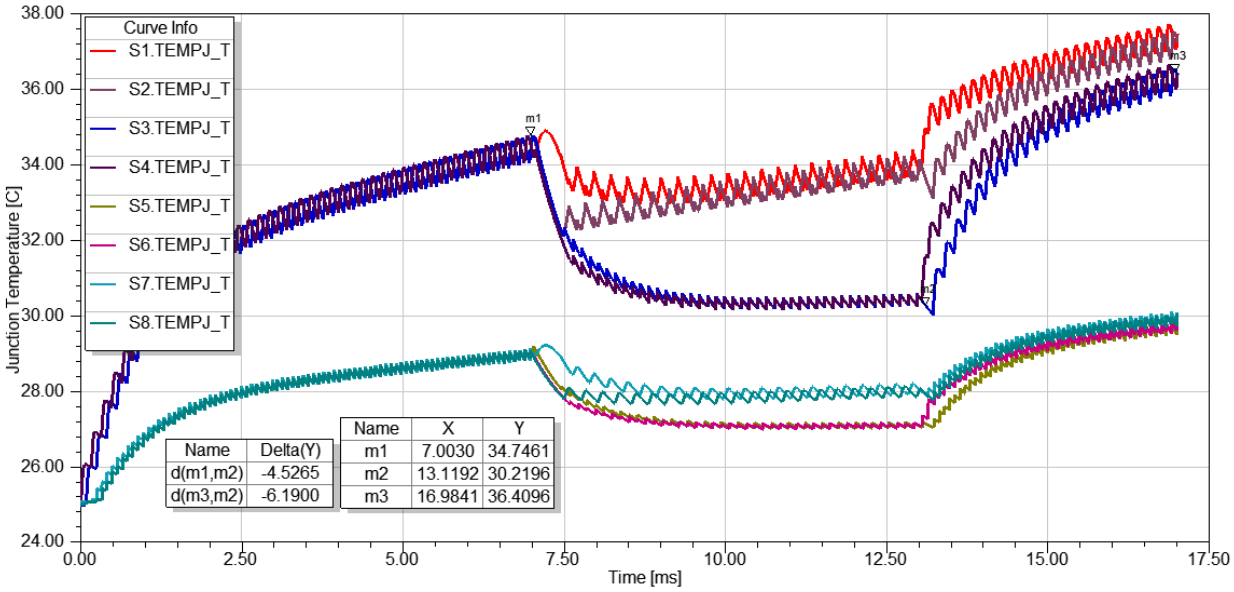


Figure 101: Junction Temperatures on each MOSFET Superimposed with *ML* Maximum Current at 80A

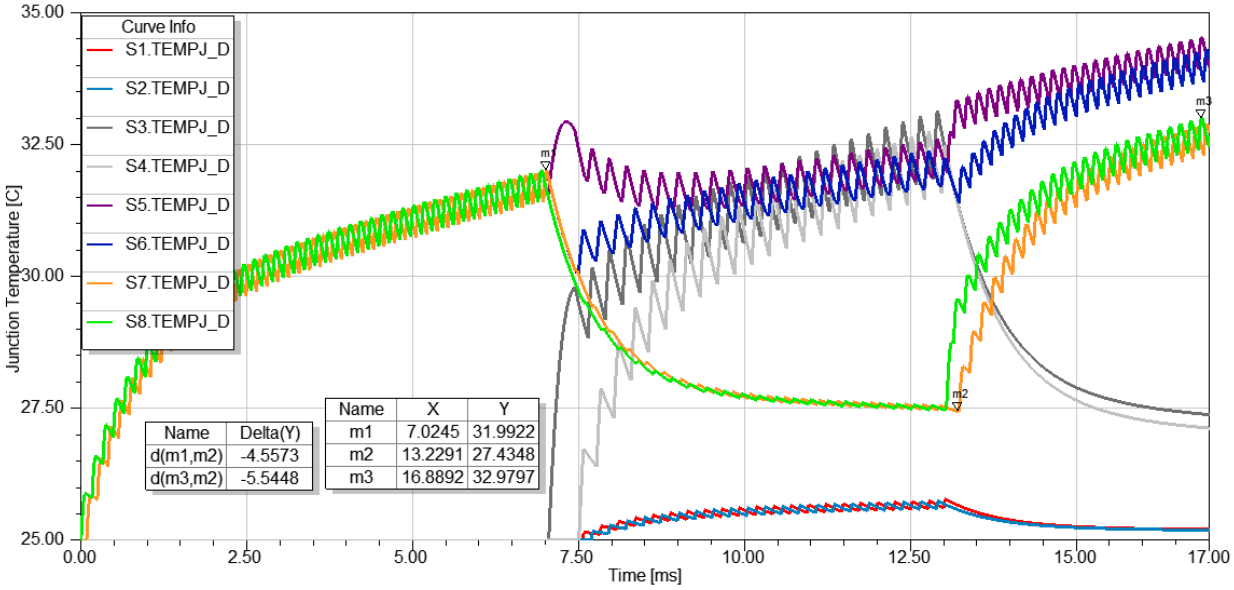


Figure 102: Junction Temperatures on each Schottky Diode Superimposed with *ML* Maximum Current at 80A

Case 3: $I_{L,max}$ = 100A

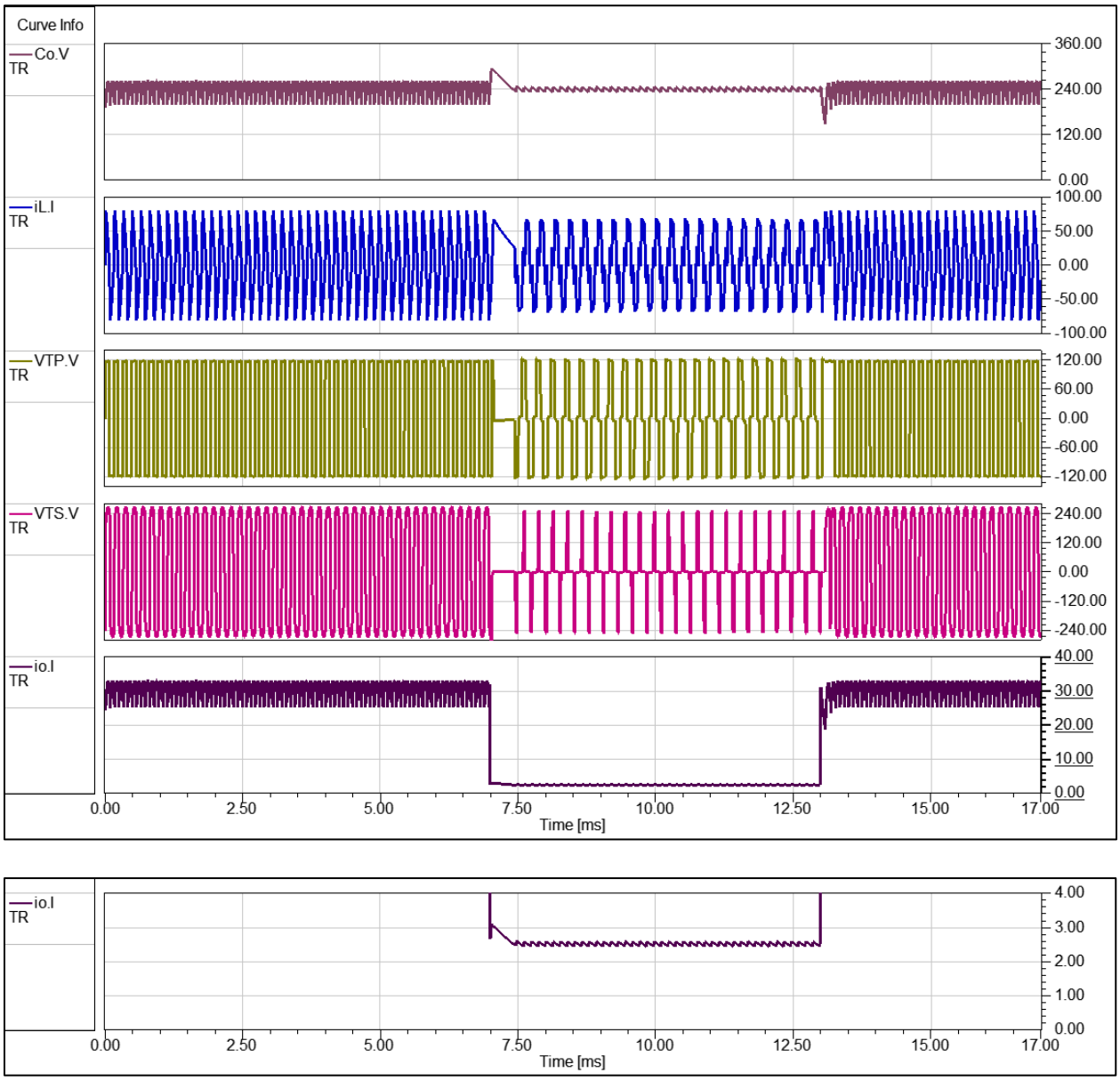


Figure 103: System Waveforms during Interval Loading Employing *ML* in Light Load with Max Current at 100A

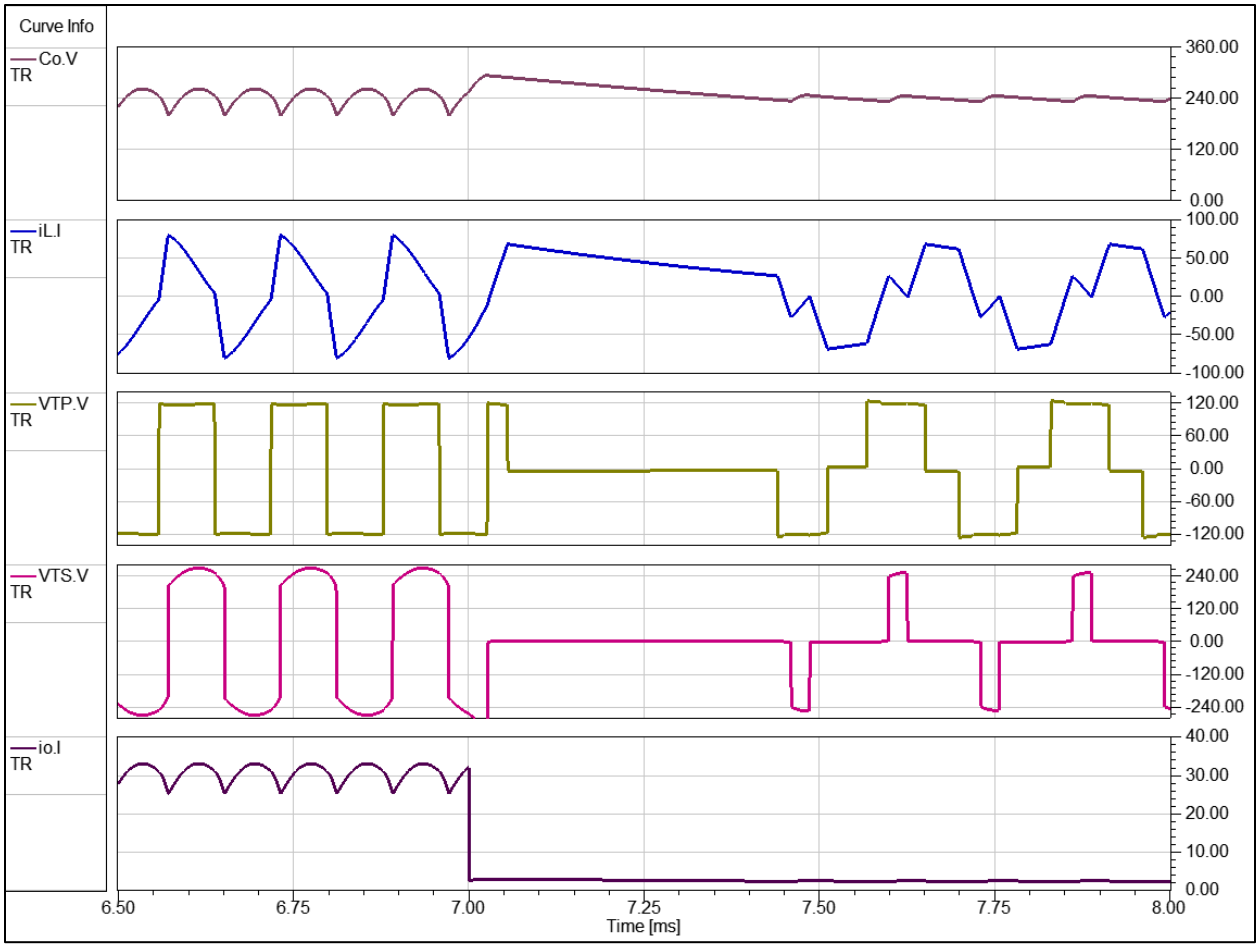


Figure 104: System Waveforms for Transient Performance from Heavy to Light Load with *ML* Max Current at 100A

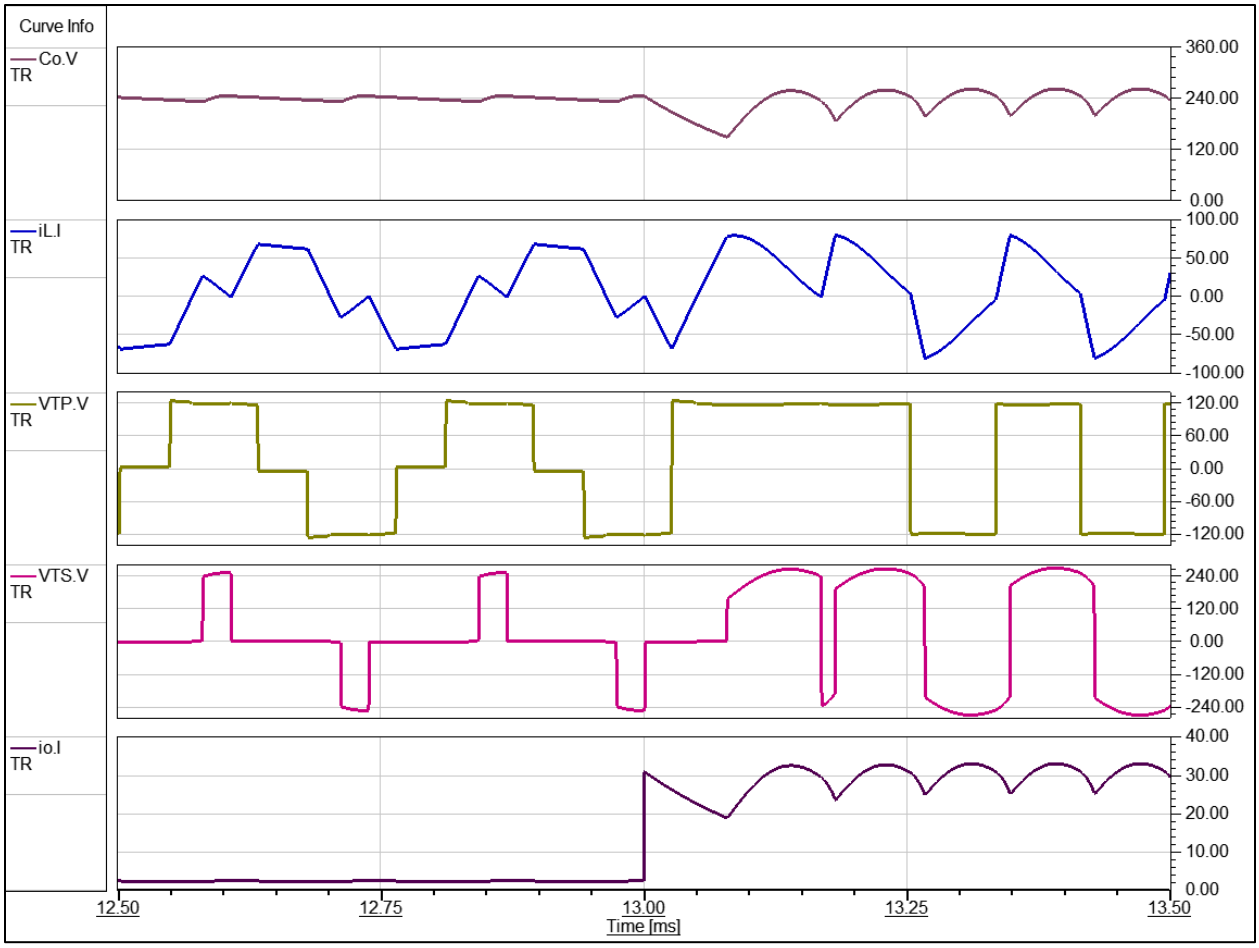


Figure 105: System Waveforms for Transient Performance from Light to Heavy Load with *ML* Max Current at 100A

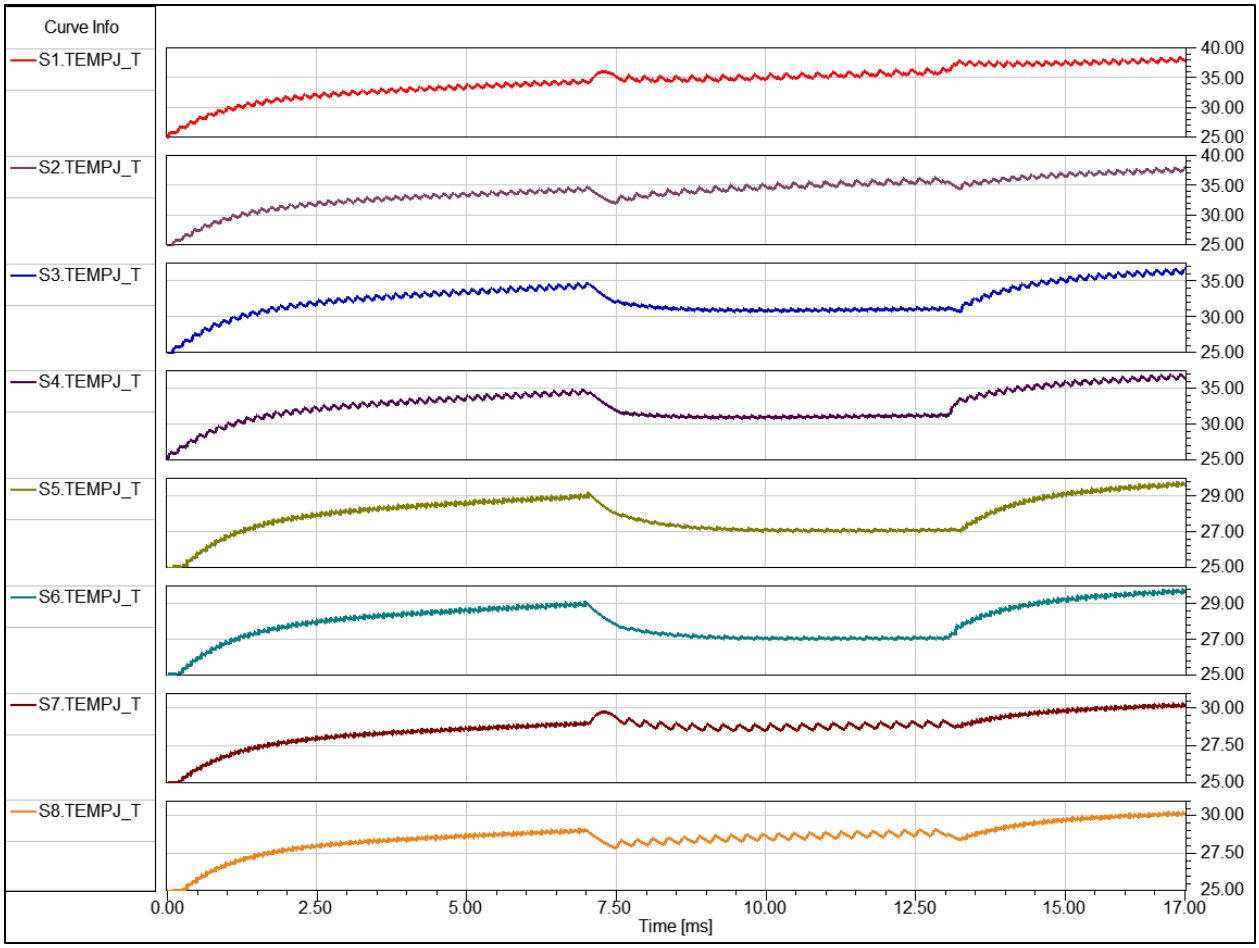


Figure 106: Junction Temperatures on each MOSFET during Interval Loading with *ML* Maximum Current at 100A

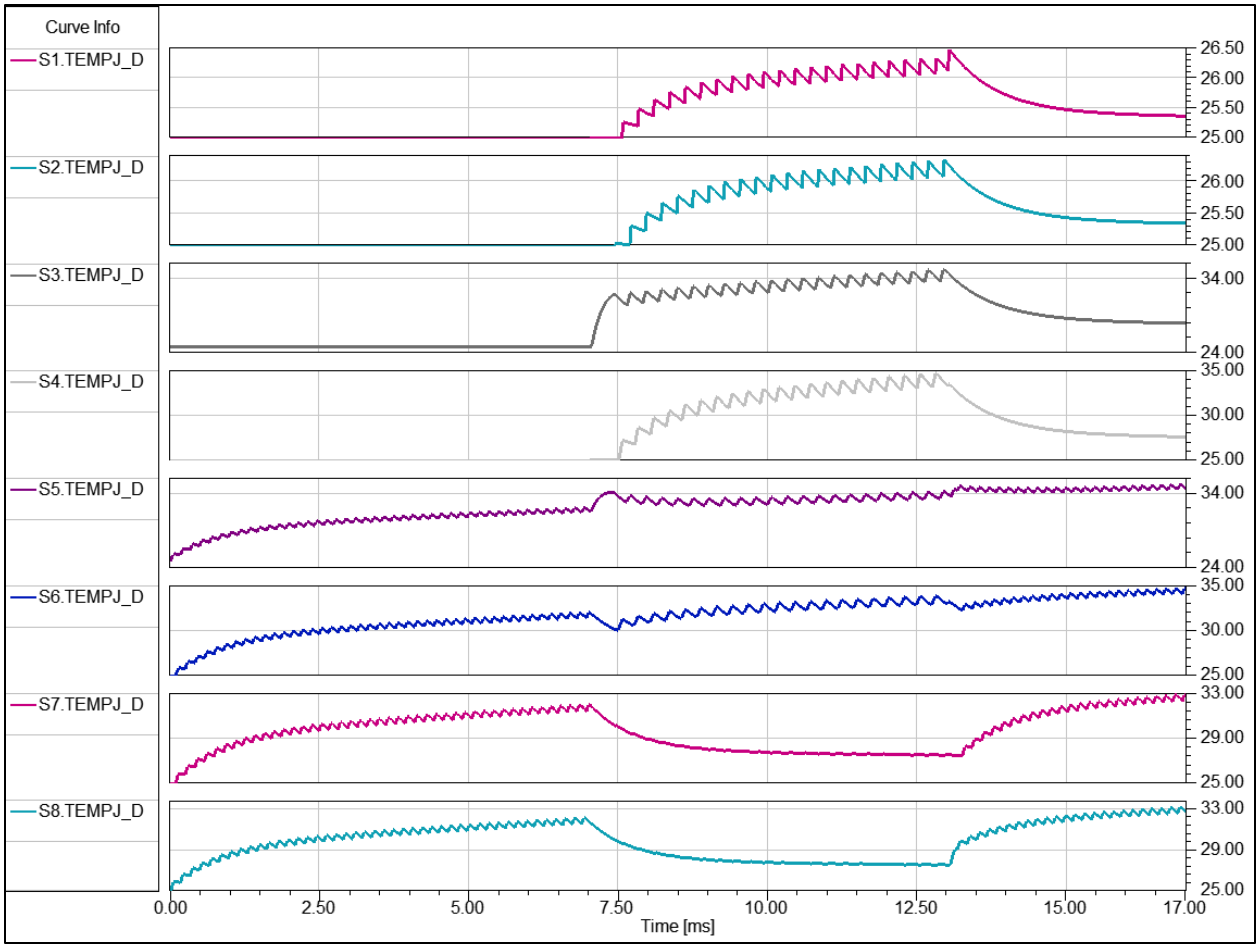


Figure 107: Junction Temperatures on each Schottky Diode during Interval Loading with *ML* Maximum Current at 100A

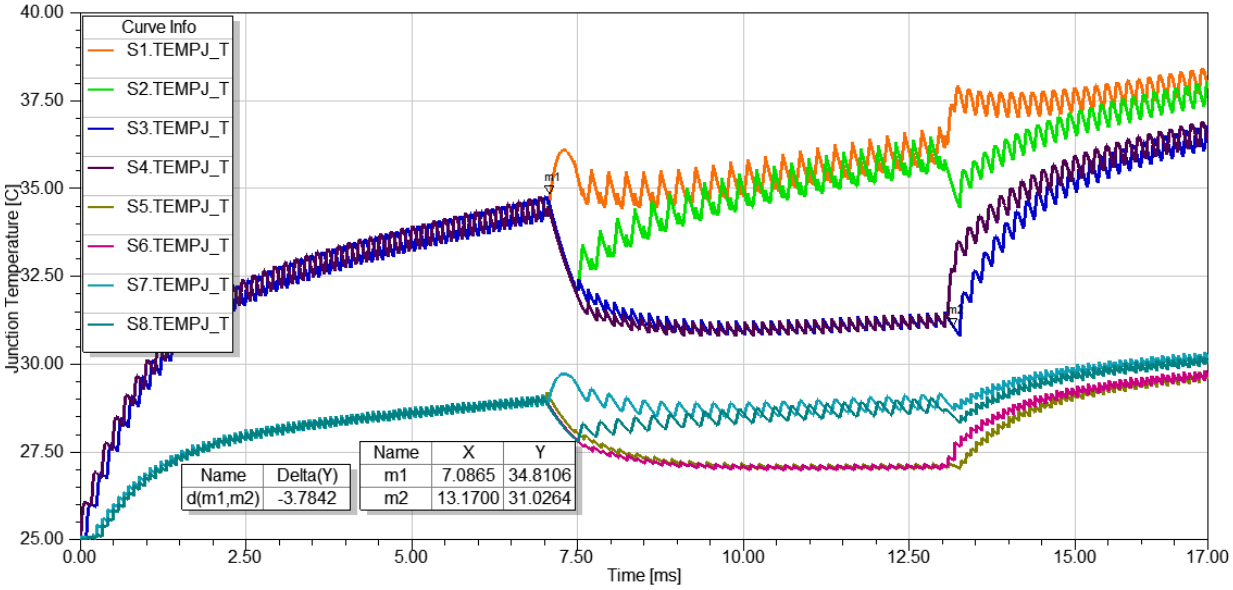


Figure 108: Junction Temperatures on MOSFET during Interval Loading with *ML* Maximum Current at 100A

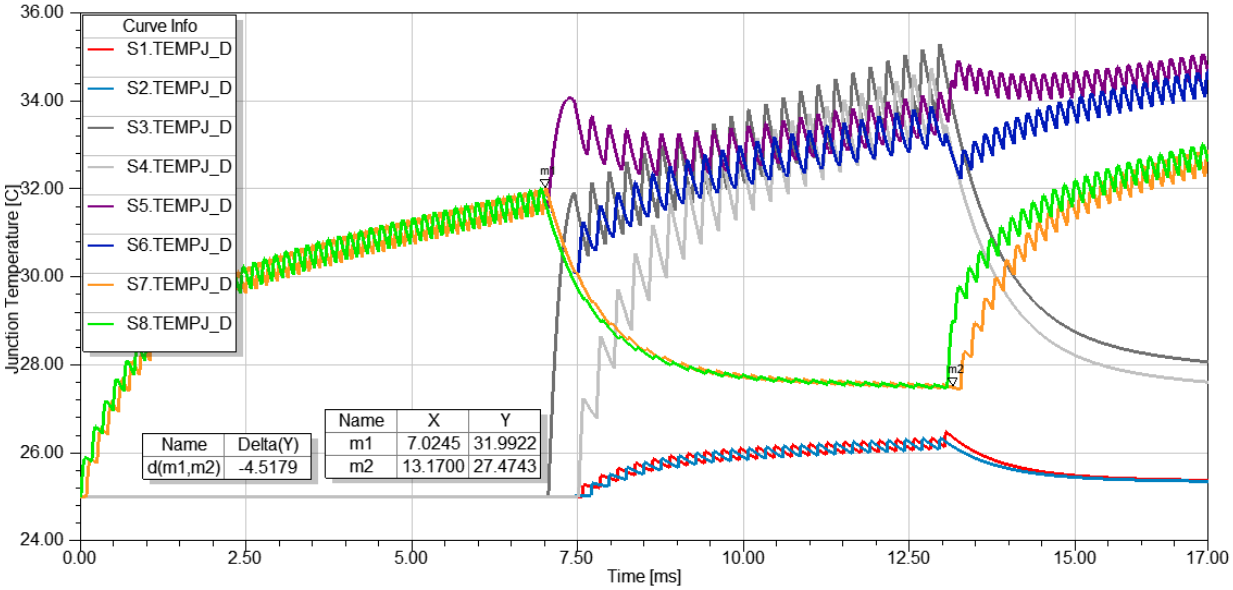


Figure 109: Junction Temperatures on Schottky Diode during Interval Loading with *ML* Maximum Current at 100A

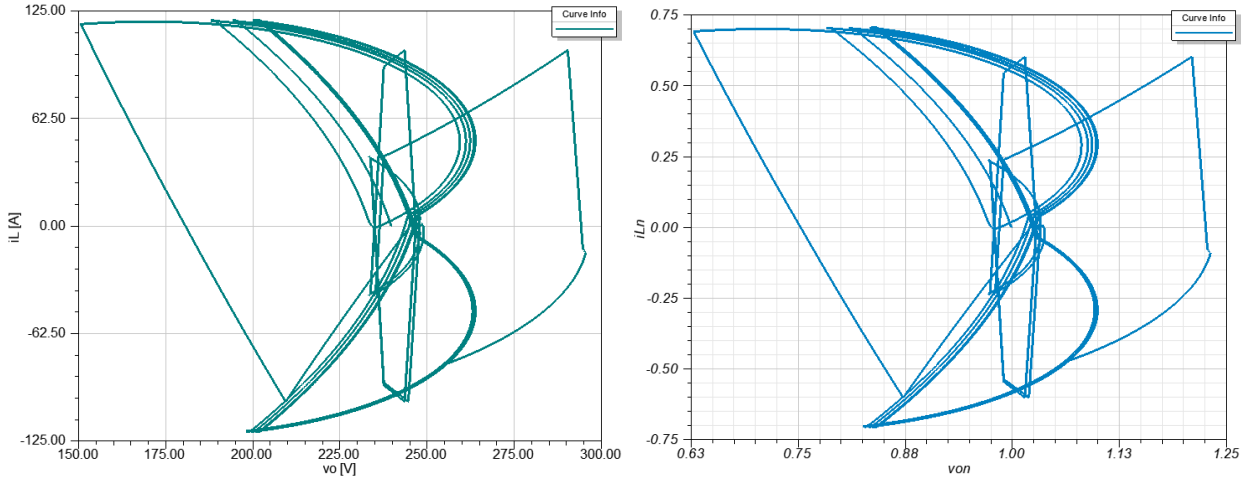
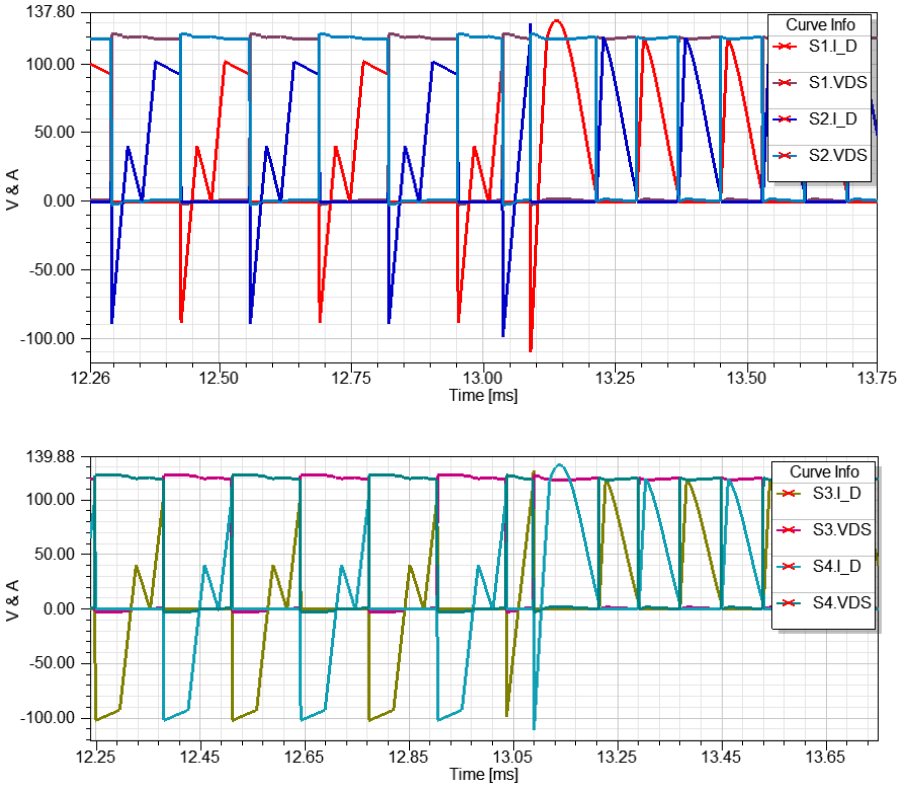


Figure 110: Nominal and Normalized State Planes during Interval Loading with *ML* Maximum Current at 100A



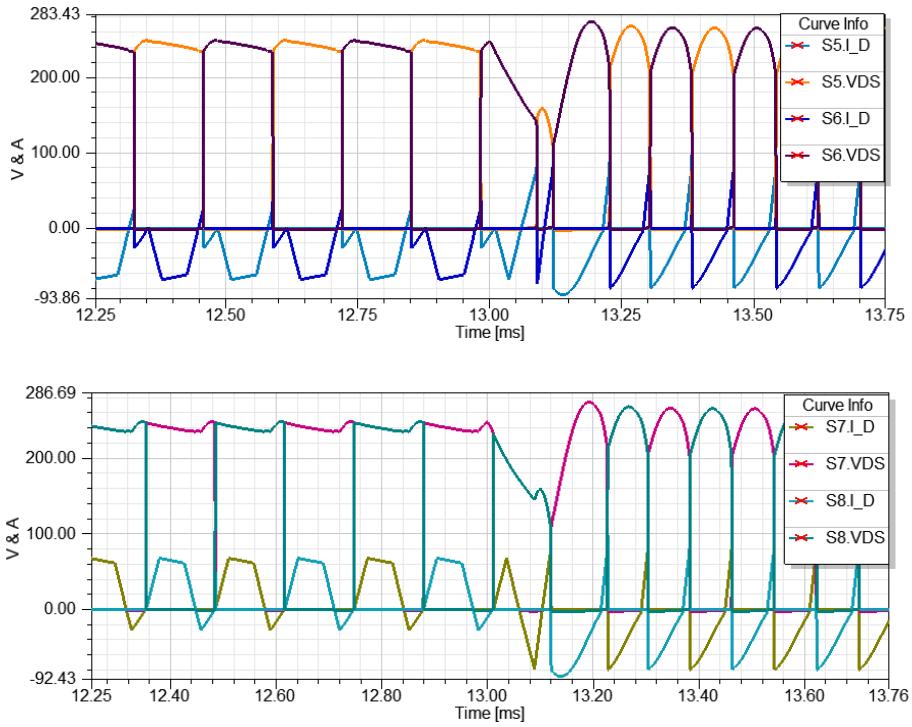


Figure 111: Voltage (DS) and Current (D) for all Devices during Interval Loading with *ML* Maximum Current at 100A

Case 4: $I_{L,max}$ = 120A

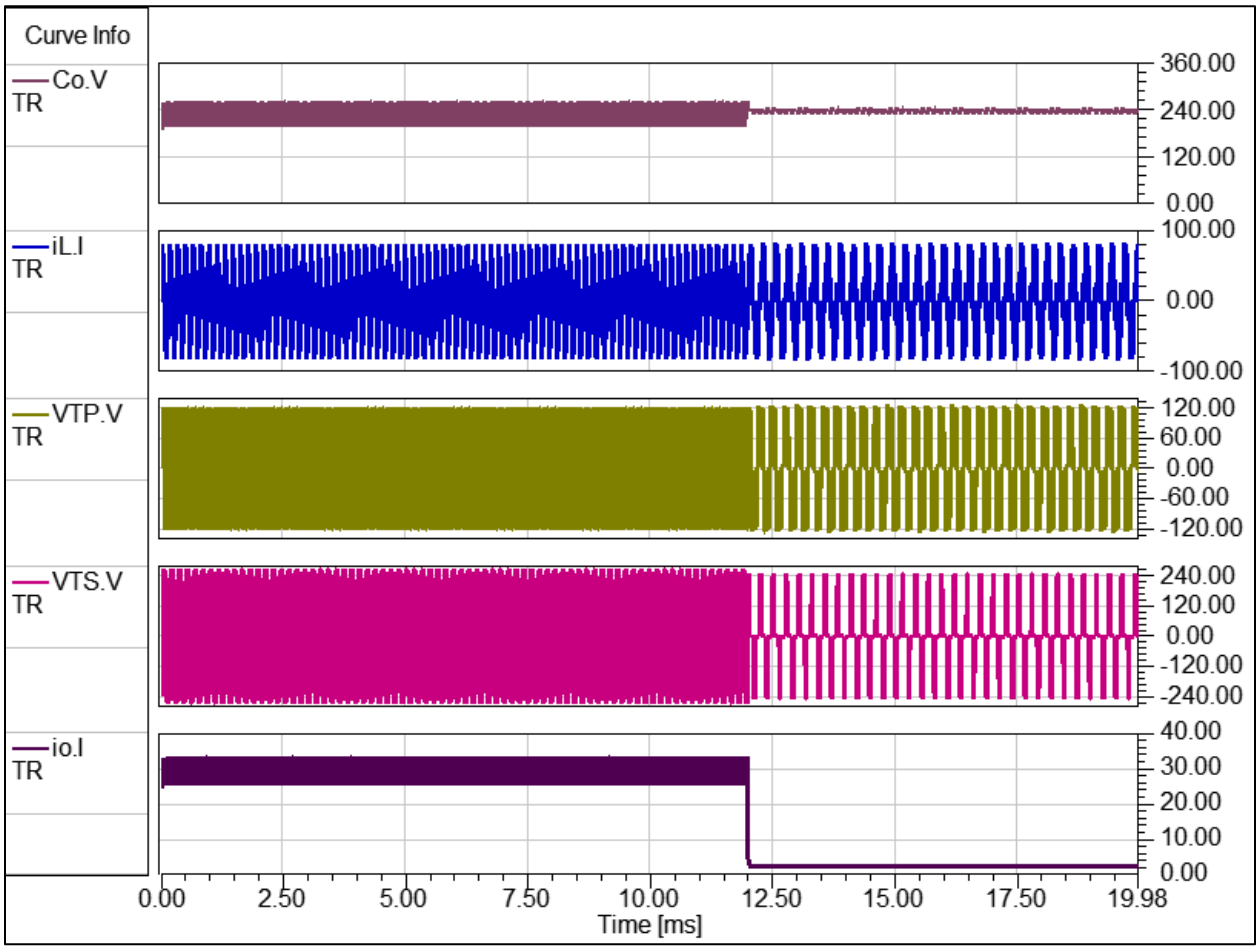


Figure 112: System Waveforms during Interval Loading with *ML* Maximum Current at 120A in Light Loading

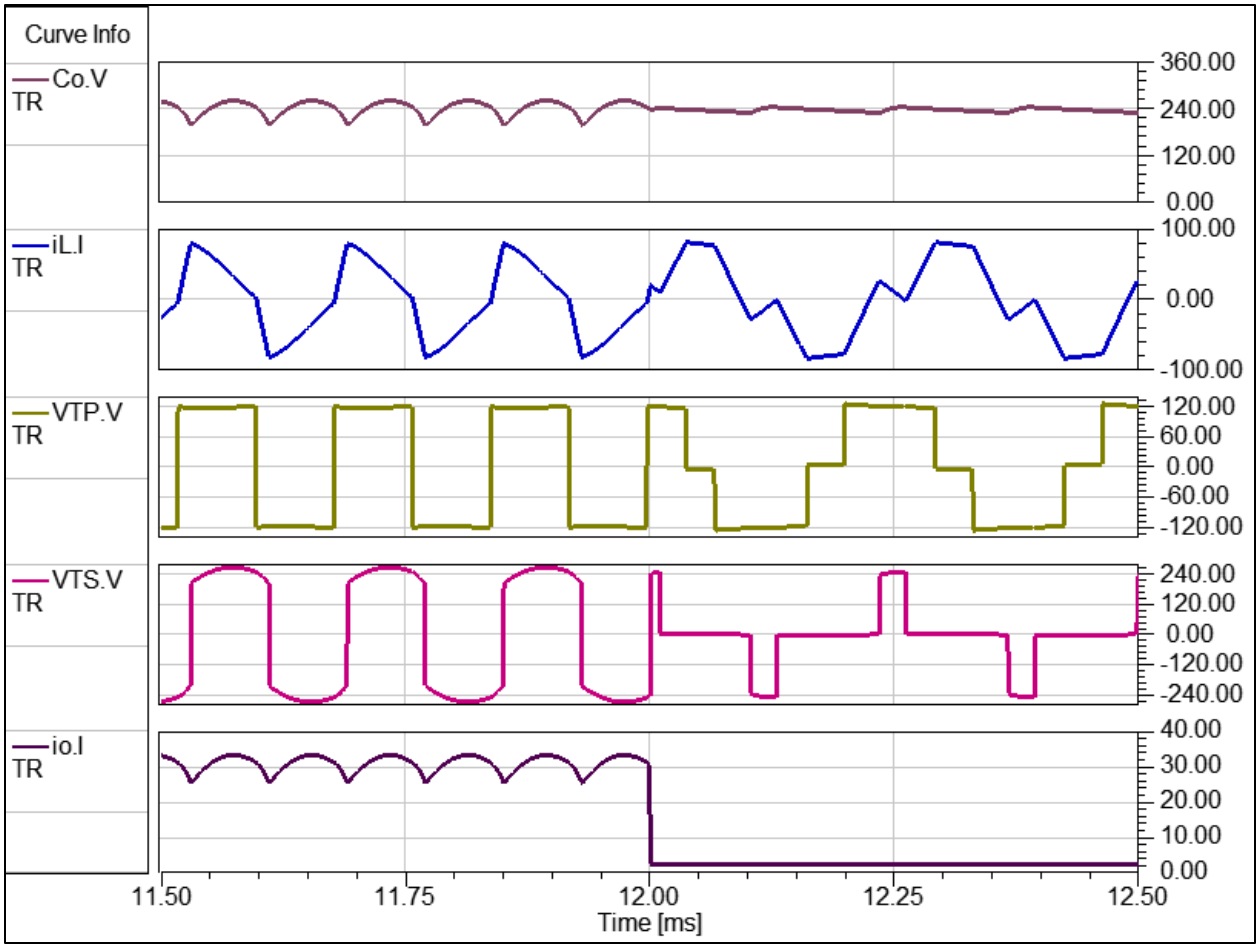


Figure 113: System Waveform Transient Performance from Heavy to Light Load with *ML* Maximum Current at 120A

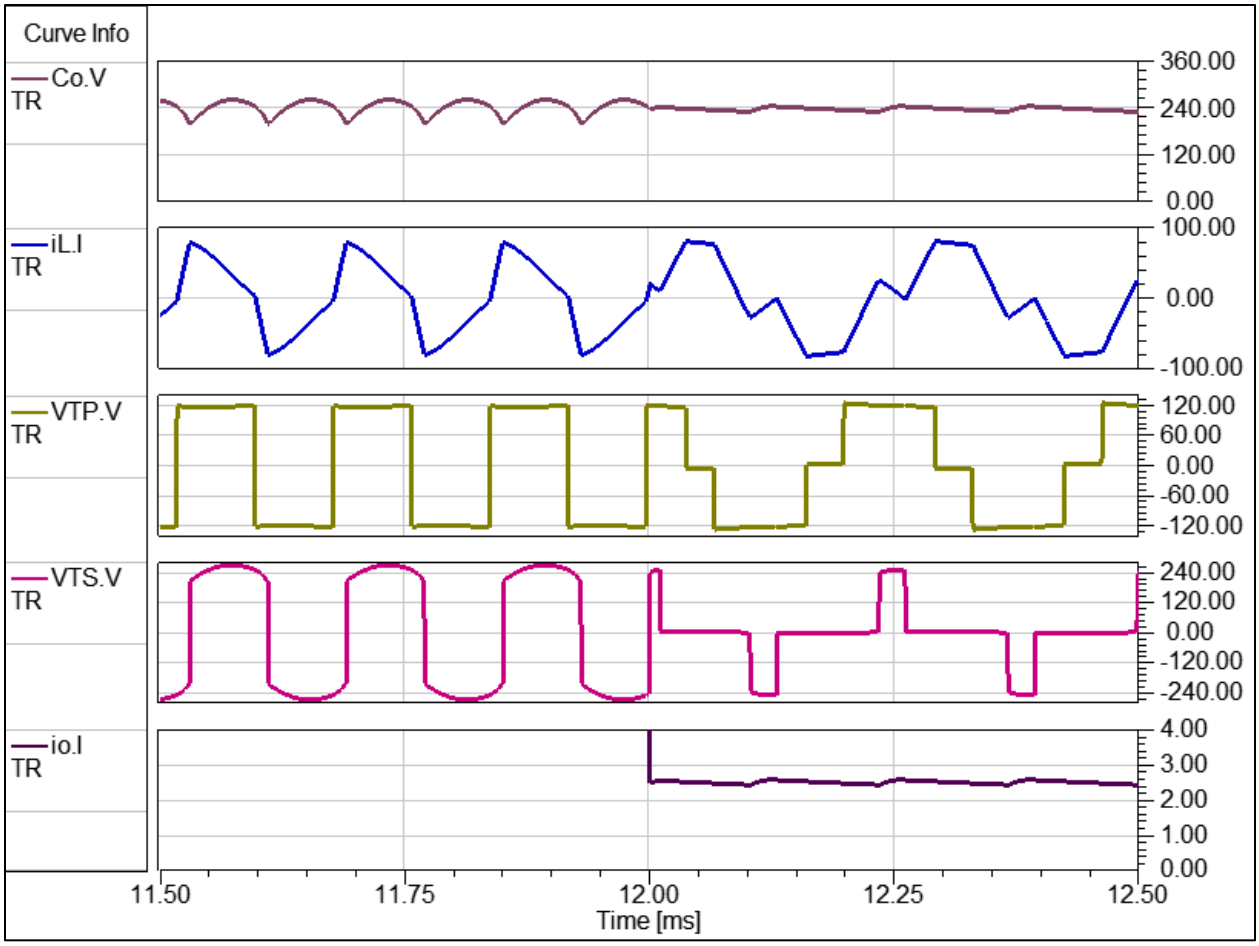


Figure 114: System Waveform Transient Performance from Light to Heavy Load with *ML* Maximum Current at 120A

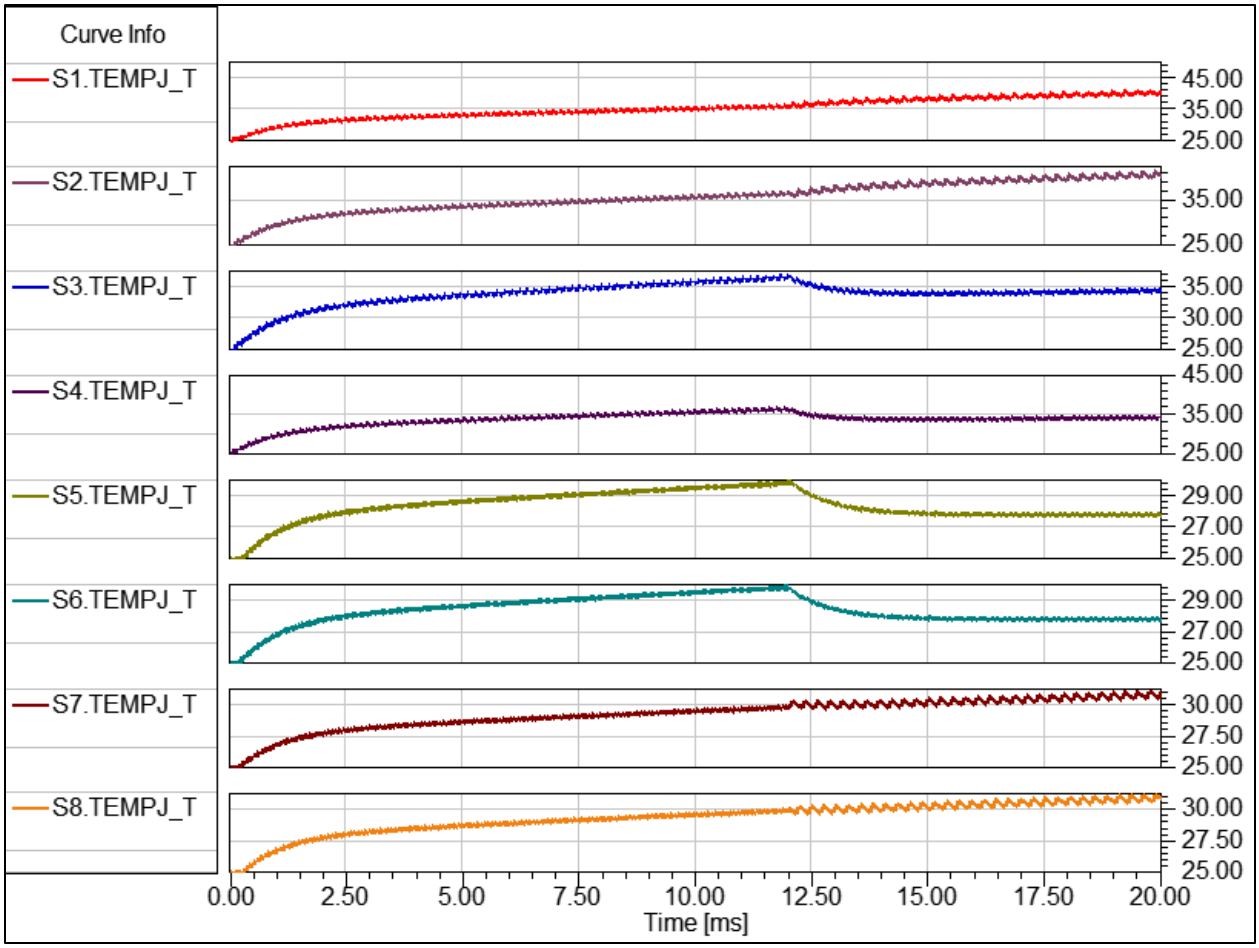


Figure 115: Junction Temperatures on each MOSFET during Interval Loading with *ML* Maximum Current at 120A

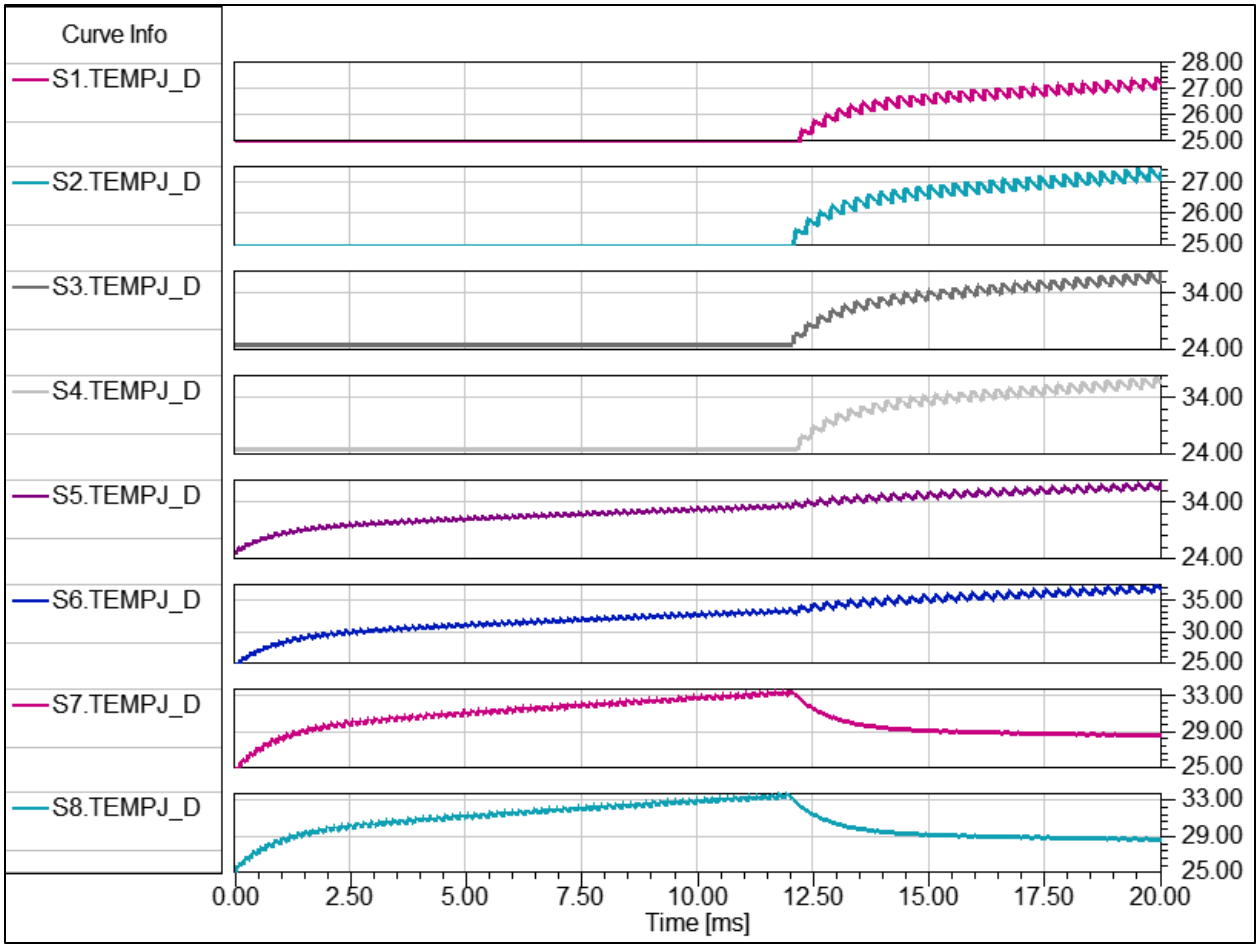


Figure 116: Junction Temperatures on each Schottky Diode during Interval Loading with *ML* Maximum Current at 120A

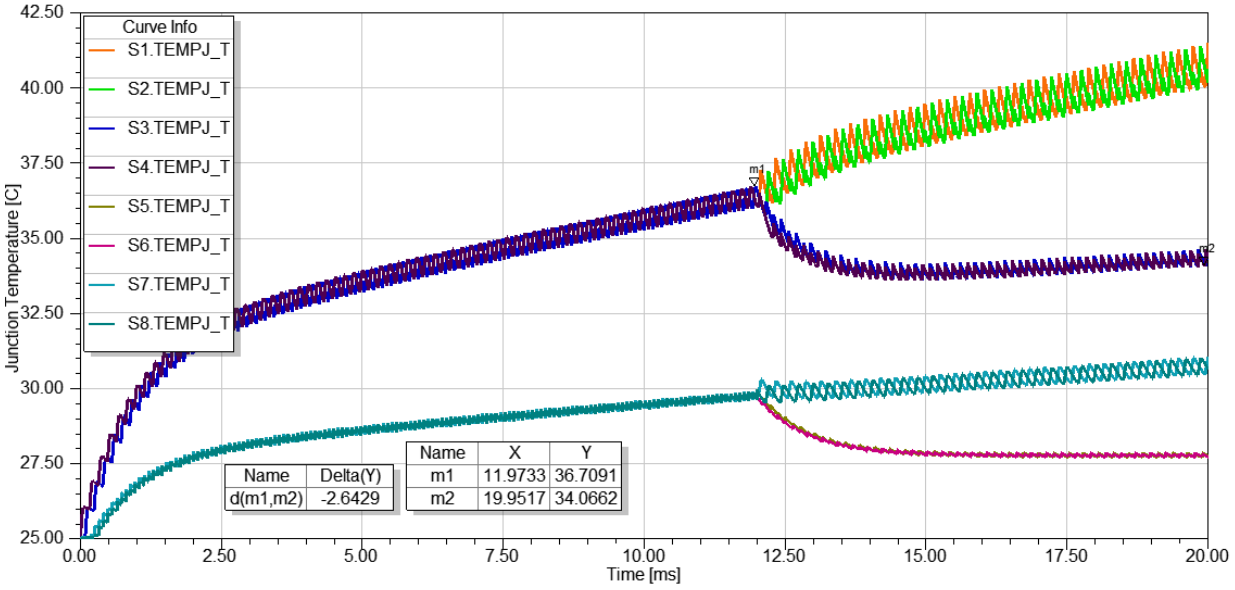


Figure 117: Junction Temperatures on each MOSFET during Interval Loading with *ML* Maximum Current at 120A

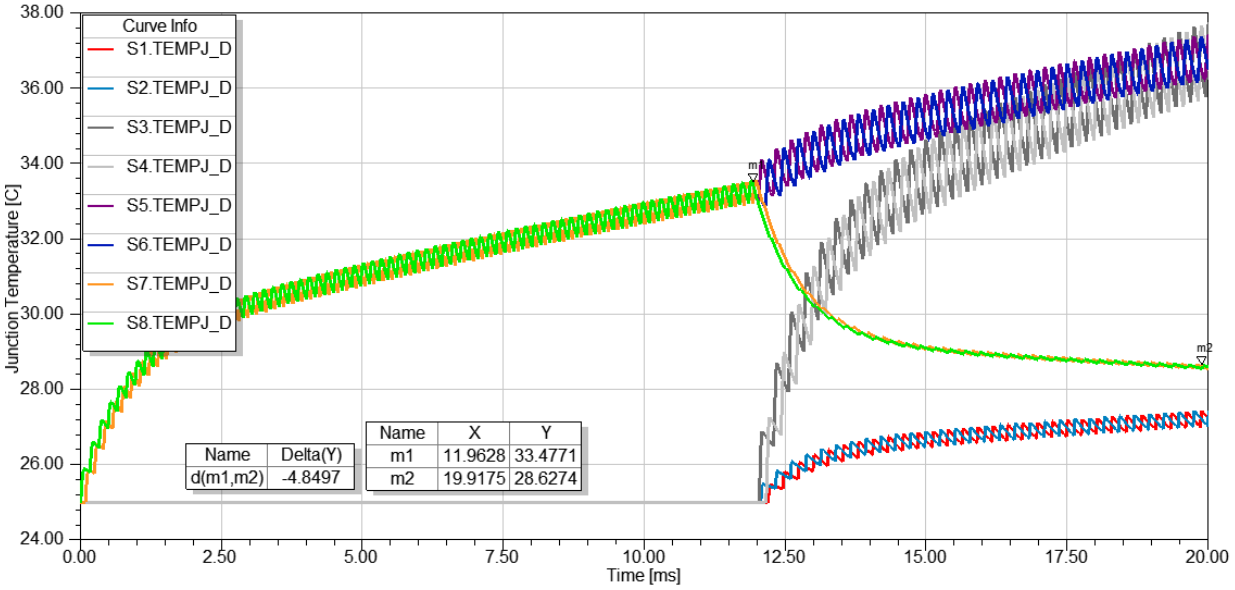


Figure 118: Junction Temperatures on each Schottky Diode during Interval Loading with *ML* Maximum Current at 120A

5.3.6 Concluding Impact Assessment

From the impact assessment cases presented, ATBC is capable of essentially eliminating any junction temperature fluctuations that would have been seen for a given interval based load. This result is due to effective design for circulating current (*ML*) at essentially whatever reasonable current level that might be desired. The current control target $I_{Ln,max}$ enables essential elimination of thermal cycling if all current maximums during light loading conditions are permissible for a given design, within rated values of device operation. In theoretical design, the target is capable of simply matching transformer current magnitudes from the heavy loading condition, carrying the same magnitudes for conduction losses into the light loading conditions as well. Collected from all impact assessment cases of comparable parametric conditions, the worst case thermal cycling results among the modeled power MOSFETs are collected in Table 28.

Table 28: Collected Worst Case Thermal Cycling Results for MOSFETS from Impact Assessment Cases

Control Mode:	Case Per Control Mode:	Junction Temperature Peak Magnitude:	Thermal Cycling Depth:
NSS (*BM)*	(7-11.5ms)	35 °C	6.7 °C
Conventional	4kHz, 10kHz (7-11.5ms)	35 °C	6.4 °C
-	8 kHz (7-13ms)	41 °C	10.2 °C
ATBC *(ML)*	50A (7-13ms)	34.5 °C	5.4 °C
-	80A (7-13ms)	35 °C	4.5 °C
-	100A (7-13ms)	34.5 °C	3.8 °C
-	120A (12-20ms)	37 °C	2.6 °C

Note the following additional information needed to couple with this table to come to correct conclusions. These are values only for the power MOSFET junction temperatures where the full picture is not known without the Schottky diode junction temperatures as well. If simply the body

diode was utilized instead of an added anti-parallel Schottky diode there would have been only one temperature measurement. The Microsemi module modeled in this work provides two transient thermal impedance graphs in its datasheet for the MOSFET and also for the Schottky diode just mentioned. Respectively, temperatures are calculated independentaly for each device consistent with the corresponding curve, accounting for the experienced switching and conduction losses. The Schottky diode thermal cycling results are provided in Table 29.

Table 29: Collected Worst Case Thermal Cycling Results for Schottky Diodes from Impact Assessment Cases

Control Mode:	Case Per Control Mode:	Junction Temperature Peak Magnitude:	Thermal Cycling Depth:
Conventional	4kHz, 10kHz (7-11.5ms)	32 °C	4.0 °C
-	8 kHz (7-13ms)	32.5 °C	4.3 °C
ATBC *(ML)*	50A (7-13ms)	32 °C	4.5 °C
-	80A (7-13ms)	32 °C	4.6 °C
-	100A (7-13ms)	32 °C	4.5 °C
-	120A (12-20ms)	33.5 °C	4.8 °C

When comparing the conventional methods of dual acive bridge control to ATBC, a current control target $I_{L,max}$ of 120A results in 18% and 11% thermal cycling minimization compared to fixed and varied conventional switching frequency, respectively. This is calculated by first calculating the worst case drop in temperature among devices for ATBC (22), to then be compared to the temperature drops of the fixed and varied switching frequency conventional cases (23) and (24).

$$1 - \frac{T_{j,peak} - \Delta T_j}{\Delta T_{j,peak}} = 1 - \frac{37°C - 2.6°C}{37°C} = 7\% \tag{22}$$

$$1 - \frac{T_{j,peak} - \Delta T_j}{\Delta T_{j,peak}} = 1 - \frac{41°C - 10.2°C}{41°C} = 25\% \tag{23}$$

$$1 - \frac{T_{j,peak} - \Delta T_j}{\Delta T_{j,peak}} = 1 - \frac{35°C - 6.4°C}{35°C} = 18\% \tag{24}$$

The percentage improvements in minimization of thermal cycling is calculated by simply the difference of the percentage drops in temperature from ATBC to conventional control as in (25) and (26) for fixed and varied conventional switching frequency, respectively.

$$25\% - 7\% = 18\% \tag{25}$$

$$18\% - 7\% = 11\% \tag{26}$$

The percentage improvements for each current control target $I_{\mathrm{Ln,max}}$ of 100A, 80A, and 50A are likewise calculated and provided in Table 31.

Table 30: Percentage Improvements using ATBC for Corresponding Current Control Targets

ATBC Current Control Target:	ATBC Percentage Temperature Drop:	Improvement Over Varied f_{sw} (18%):	Improvement Over Fixed f_{sw} (25%):
120A	7%	11%	18%
100A	11%	7%	14%
80A	13%	5%	12%
50A	16%	2%	9%

Even with a current control target, $I_{L,max}$, of 50A there is improvement over conventional control operation. The flexibility of ATBC to alter the thermal cycling depth is demonstrated through the target modificaiton. Overall, even though losses are increased for the set purpose we can conclude that the proposed control method achieves the set objective to minimize thermal cycling during interval-based power processing.

5.4 ACTIVE THERMAL BOUNDARY CONTROL FOR BUCK MODE

All of the design explanation and assessment up until this point has been in relation to the boost mode of dual active bridge operation. This was due to both the chronological design process as well as for ease of clear conceptual explanation. Here the strategic design is presented also for the buck mode operation. The same approach of design was taken, and the final design is provided. Life preservation mode for buck operation was designed with six strategic trajectories as initially summarized with Table 31 in terms of u_1 and u_1, the voltage orientation of the primary and secondary sides of the dual active bridge.

Table 31: Six Natural Switching Surface Configurations of Life Preservation Mode for Buck Operation

SS	u_1	u_2
1	1	-1
2	0	1
3	0	0
4	-1	1
5	0	-1
6	0	0

The conceptual normalized state-plane diagram of life preservation mode in buck operation is depicted in Figure 119. The corresponding steady state waveforms including associated conducting switches are conceptually depicted in Figure 120. Additionally, Figure 121 provides visualization of the switching configurations per specified natural switching surface that are utilized in life preservation mode in buck operation.

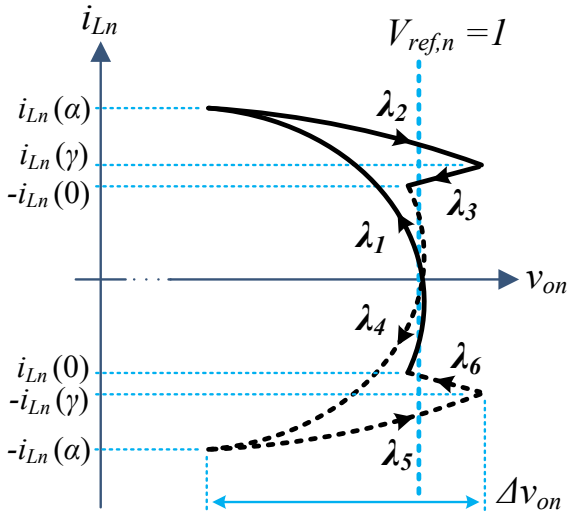


Figure 119: Conceptual Normalized State Plane of Life Preservation Mode for Buck Operation

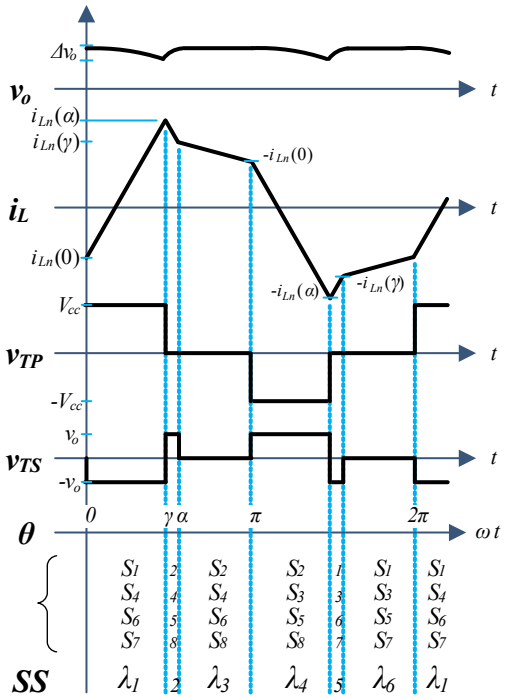


Figure 120: Steady State Operating Waveforms for Life Preservation Mode in Buck Operation

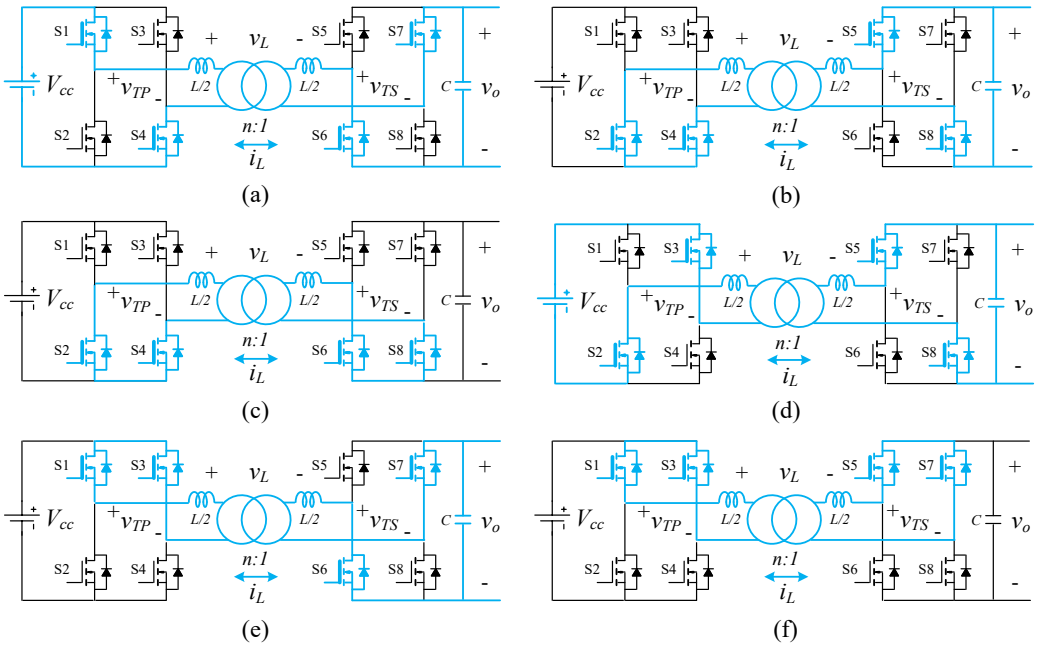


Figure 121: Switching Configurations of *ML* in Buck Operation for Switching Surfaces 1 through 6

With the aid of Figure 119 and Figure 120 for visualization, the targets designed for each trajectory are as follows in their normalized form. Equation (23) comes from equation (31) of Section 4.2, one of the targets defined for *M6*.

$$i_{Ln}(0) \rightarrow v_{on,\lambda 1} = \left(\frac{v_o - V_{o,min}}{V_{ref}}\right) = 1 - V_{o,min}\% = 1 - 1\% = 99\% \tag{22}$$

$$i_{Ln}(\alpha) = i_{Ln,\lambda 2} = \frac{V_{cc}(d\pi - 2d\delta - m\pi)}{2\omega L}\left(\frac{Z_0}{V_{ref}}\right) \tag{23}$$

$$i_{Ln}(\gamma) = i_{Ln,\lambda 3} = (i_{Ln,\lambda 2})60\% \tag{24}$$

$$i_{Ln}(\pi) \rightarrow v_{on,\lambda 4} = v_{on,\lambda 1} = 99\% \tag{25}$$

$$i_{Ln}(\pi + \alpha) = i_{Ln,\lambda 5} = -i_{Ln,\lambda 2} = -\frac{V_{cc}(d\pi - 2d\delta - m\pi)}{2\omega L}\left(\frac{Z_0}{V_{ref}}\right) \tag{26}$$

$$i_{Ln}(\pi + \gamma) = i_{Ln,\lambda 6} = -i_{Ln,\lambda 3} = -(i_{Ln,\lambda 2})60\% \tag{27}$$

With life mode (*ML*) defined as such, active thermal boundary control for buck operation additionally incorporates the six and four trajectory modes (*M6* and *M4*). These additional modes are incorporated for medium and heavy loading conditions as is done for boost operation. A summary in terms of u_1 and u_1 for the three mode buck operation design is provided in Table 32. Lastly, ATBC in buck mode operation with all transitions and conducting switches specified is provided in a flowchart diagram in Figure 122.

Table 32: Summarized Design of NSS Control Operation when Prioritizing Life Preservation in Buck Operation

Utilized	*M4*			*M6*			*ML*		
Trajectories	SS	u_1	u_2	SS	u_1	u_2	SS	u_1	u_2
I	λ_1	1	-1	λ_1	1	-1	λ_1	1	-1
II	λ_2	1	1	λ_2	1	1			
III				λ_3	0	1	λ_2	0	1
IV							λ_3	0	0
V	λ_3	-1	1	λ_4	-1	1	λ_4	-1	1
VI	λ_4	-1	-1	λ_5	-1	-1			
VII				λ_6	0	-1	λ_5	0	-1
IV*							λ_6	0	0

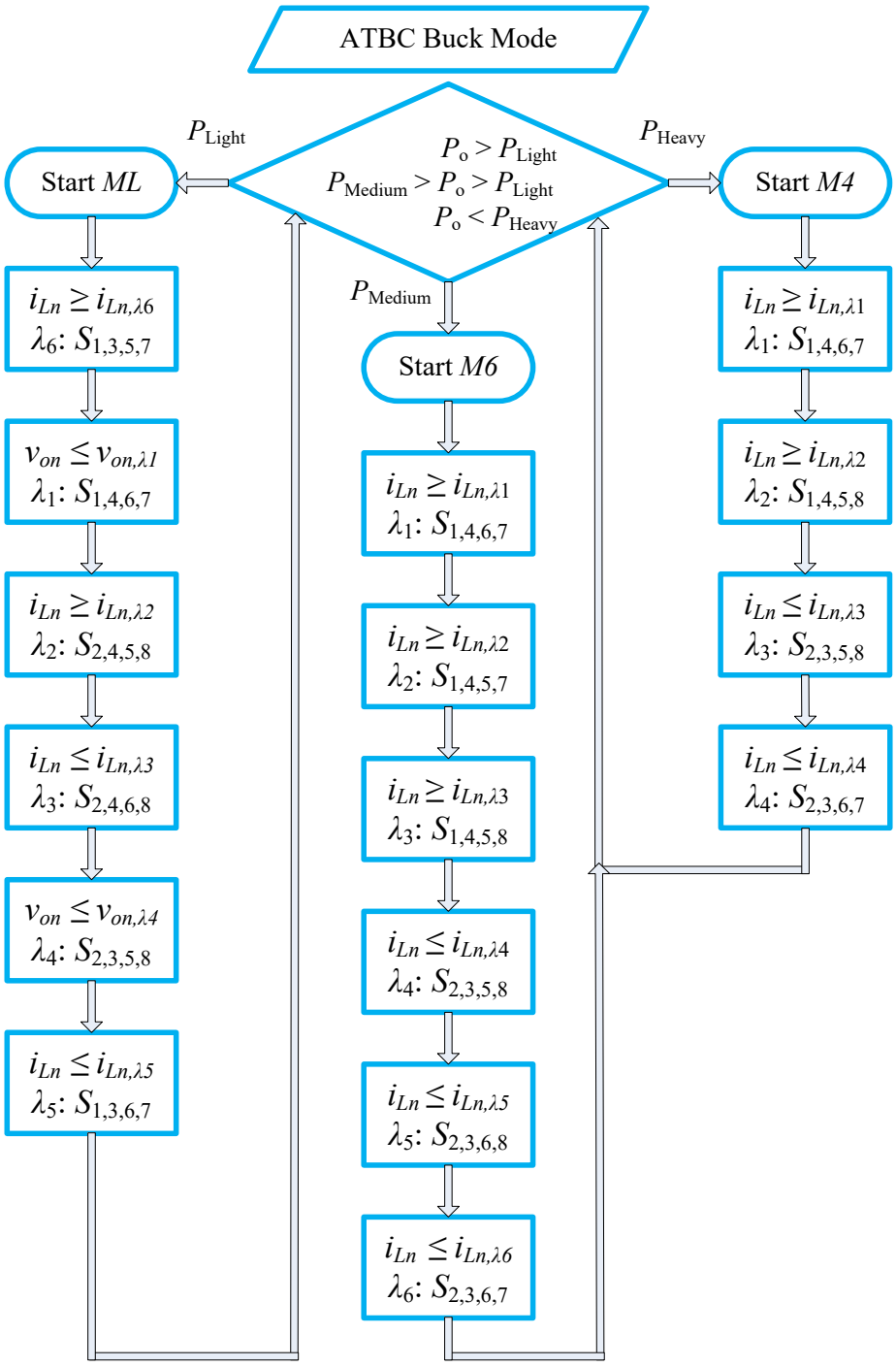


Figure 122: Flowchart of Active Thermal Boundary Control in Buck Mode of Operation

5.4.1 Simulation Example of Life Preservation Mode in Buck Operation

Provided here is validation for *ML* control of the DAB in buck operation. Given the ratings of the system in Table 22, the given case is a light loading condition for the purpose of demonstrating *ML* operation. The following plots are simulation results obtained in the ANSYS software package.

Table 33: Parameters for Validation Simulation for ML in Buck Operation

Parameter:	Value:	Description
M	*ML* (Buck)	Mode of strategic trajectories
P_o	600W	Output power demanded
V_{cc}	240	Input voltage
V_o	120	Output voltage (V_{ref})
d	$V_o/(nV_{cc})$	Conversion ratio (n = 2/5)
f_{sw}	4kHz	Switching frequency
m	1	Modulation index
$v_{on,min}$	99%	Minimum voltage threshold
L	40µH	Equivalent transformer inductance
C	50µF	Output capacitance

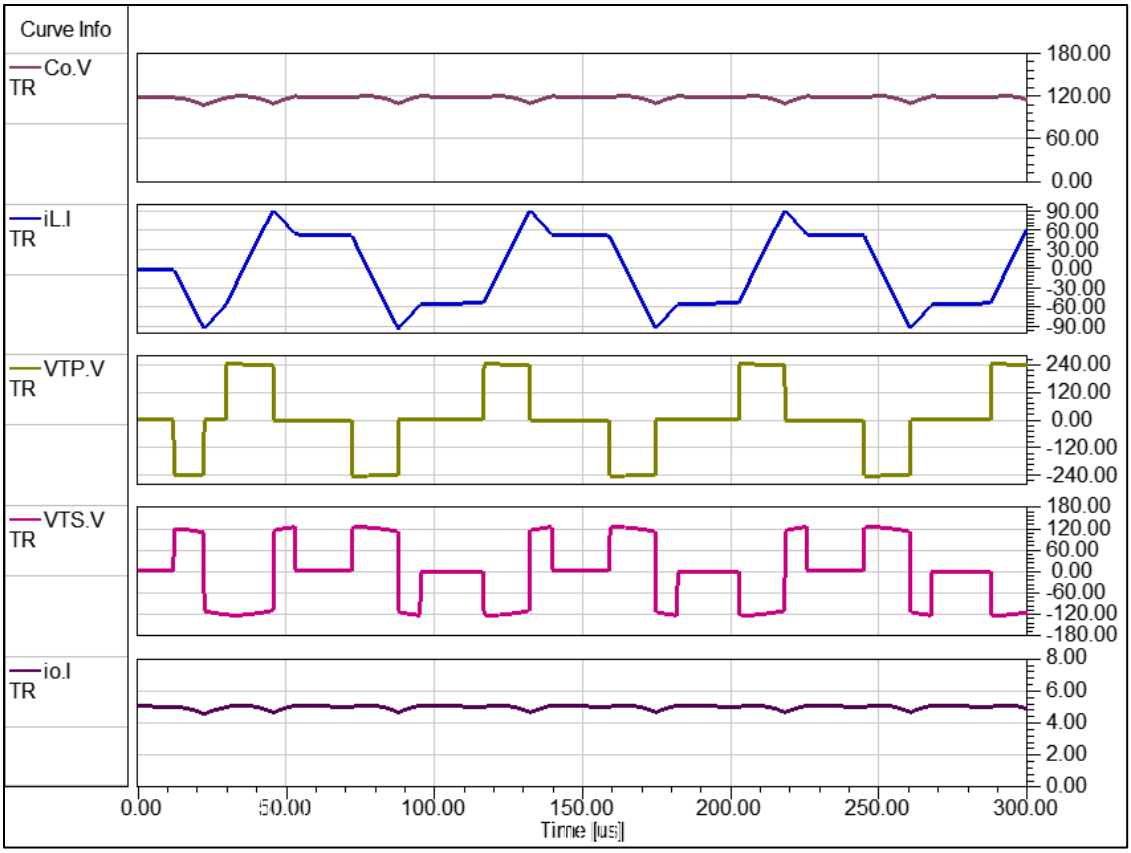


Figure 123: Steady State Waveforms of Life Preservation Mode Designed for Buck Operation

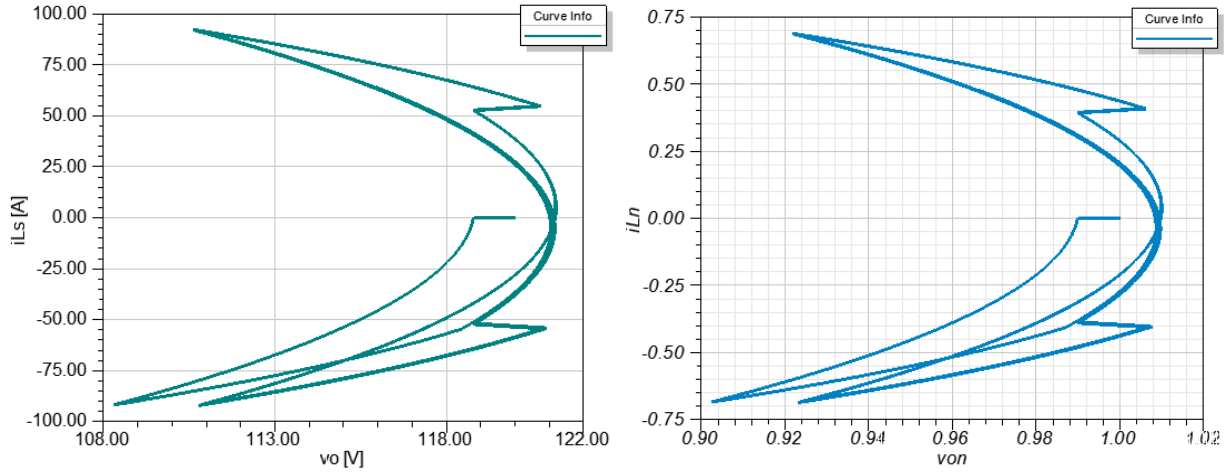


Figure 124: Nominal and Normalized State Planes of Life Preservation Mode Designed for Buck Operation

6.0 CONCLUSIONS

This dissertation presented the implementation of natural switching surface (NSS) control as a tool for active thermal control (ATC) improving the preservation of power electronic device reliability. The contribution of this work is twofold: 1) enlightenment of the thermal consequence of electrical performance and 2) a design for mediating action using boundary control. There is contribution of note in simply raising awareness in the power electronic engineering community concerning the thermal impacts of various electrical performance requirements upon device lifespan. The assessed thermal consequences led to a control methodology that addresses holistically the trade-off between reliability and performance. As the primary contribution, active thermal boundary control is proposed. The approach taken in designing ATBC for the dual active bridge could be applied to various topologies given that appropriate design measures are taken. This shows a selling point of the methodology, its general approach for application to topologies other than the dual active bridge. A significant benefit, consistent with the objective set at the onset, is that the proposed methodology minimizes the negative impacts of thermal behavior all the while maintaining converter performance of desired output power. This methodology in no way hinders the DAB from providing the load required of it, and neither does ATBC negatively affect transient performance but in fact adds improvement. An additional benefit of ATBC in contrast to other ATC methods, is that there is no need to perform condition monitoring of the junction temperature, often performed by temperature calculation estimations of T_j in real time due to the difficulty of the task [55], [56]. Adding temperature monitoring to a device module can reduce the reliability of the device which is counterproductive in the present endevour. In addition to exact junction temperatures being mostly innaccessable to measurement in real-time, there are common struggles to even utilize the less desirable case temperatures within control feedback loops due to the lag of

infrared cameras and thermocouples. For ATBC, knowing simply what the steady state current of the previous heavy load interval the current target $I_{Ln,max}$ can easily be set to match said current for significant reduction of thermal cycling magnitudes. The main disadvantage of this method if it would be so called is the added loss in light loading conditions decreasing converter efficiency that comes with the operation of life preservation mode. Yet inherent to the objective is a trade-off between reliability and performance. A second disadvantage is the need for current and voltage monitoring in real time, but this is becoming less of a hindrance over time due to decreasing costs to implement such designs but also do to the increasingly more numerous benefits to include such real time sensing for power electronics control and condition monitoring purposes. All in all, the contribution satisfies our original objective. The proposed control method utilizes NSS for an ATC method effectively contributing a control design for reliability of power electronics applicable to interval based power processing interconnections. Designed for the dual active bridge in this work, ATBC reduces if not eliminates event based thermal cycling on the junction of power electronic devices during cyclical load or generation changes.

6.1 RESEARCH DIRECTIONS AND APPLICATIONS

For future directions to take this research, an apparent choice is to develop active thermal boundary control methodology for various types of converter topologies such as grid inverters or variable-speed machine drives. Boundary control methodology has been explored also for grid inverters within the literature [57]. With a similar approach taken in this work, active thermal boundary control could be developed for a three phase DG grid inverter application. Such control could support smart inverters featuring reactive compensation as grid voltage stability support,

preserving the life where the feature would have otherwise increased degradation unabated. The aim would be to develop a form of active thermal boundary control that elegantly balances grid support performance with lifetime preservation of power electronics. This example of more performance being required of power electronics is one of many that exist and are to come.

There are a number of applications that come to mind for active thermal boundary control. There is a current drive towards electrification with power electronic systems across multiple industries including aerospace, automotive as well as maritime, not to mention the evolving electric grid. This electrification is often DC-based as well. Anywhere within these industries and others where there is an interval based load, as discussed and demonstrated throughout this work, that is where ATBC is applicable. There is the example of the electric vehicle charging station, the inspiration for the simulated design parameters of this work. Another example would be cranes on construction sites where they are used on an interval basis, off and on throughout a work day [22]. An application explored by experts in the ATC topic is wind power plants [6], [58]. Lastly, a challenge that I have had more recent exposure to is that of new additions of pulsed power loads on next generation naval ship grid designs, which require power quality and stability assessment [59]. These naval designs are looking to incorporate these loads through a DC integrated power system design [60], [61]. A pulsed power load is one that demands a high amount of power over a short time period and likely on a cyclical or interval basis. Examples of these loads are high power radar systems, directed energy lasers, and electromagnetic railguns. Critical to naval engineering is the prevention of returning to dock for maintenance due to a premature failure. The automotive and aerospace industries are experiencing stricter reliability constraints in general, making the topic of power electronics reliability increasingly important. In addition to these examples, the electric grid is also evolving rapidly with continually increasing penetrations of distributed

generation and load, most of which are becoming interfaced through power electronic conversion. With increasingly ubiquitous electrification, this control is applicable to any interval based power processing whether it be load or generation. As power electronics engineers, let us not allow unnecessary degradation of life for lack of acting. Put up boundaries for the life preservation. Efficiency is important, but design holistically. Remember reliability.

APPENDIX A

MATLAB CODE FOR NATURAL SWITCHING SURFACES

The following code was generated for analysis of the natural switching surfaces during design work. Plotting of the natural switching surfaces is implemented for both the buck and the boost modes of the dual active bridge, dependent upon the variables capable of being set as desired at the beginning of the script.

```
% 11/6/18
% Patrick T. Lewis
% Purpose: Ploting natural switching surfaces of M4 and M6
% for analysis and for aiding design process

% ***** BUCK MODE *****
tau = 0.5*pi;
m = tau/pi; % modulation index applied to high voltage winding/side (tau/pi)
fs = 10000; % Desired Switching frequency - degree of freedom for design
Ts = 1/fs; % Switching period
omega = 2*pi*fs; % angular switching frequency
L = 40e-6; %transformer equivalent inductance (H)
C = 20e-6; % output capacitance (F)
f0 = 1/(2*pi*sqrt(L*C)); % natural frequency
T0 = 1/f0; % period of natural frequency
Po = 3600; % Output power demand
Vref = 240; % Reference output voltage by design
Vo = Vref; % Output voltage
Vcc = 120; % Input Voltage --> d = V2/(nV1) where n = 2
n = 1.5; % Transformer turns ratio --- CHANGE PER BUCK OR BOOST MODE!!!
d = Vo/(n*Vcc); % Voltage conversion ratio
io = (Po/Vo);
R = Vo^2/Po;

% Phase shift from vT1 to vT2
dd = pi*m/2-sqrt(2*m*(Vcc*d*pi).^2-(Vcc*d*pi*m).^2-...
    4*Po*d*omega*L*pi)/(2*Vcc*d);

% Limits on m for boost mode
% Minimum m to achieve required Po and d
m_min = 1-sqrt((Vcc*d*pi)^2-4*Po*d*omega*L*pi)/(Vcc*d*pi);
% Lower limit on soft switching region
```

```
a2 = 2+2*d+d^2; % for boost mode - buck mode differs
m_lower = ((Vcc*pi*d)*(2+d)+...
    sqrt(2*pi*d*(Vcc^2*pi*d^2*(1+d)-2*a2*Po*omega*L)))/(Vcc*pi*d*a2);
% Upper limit on soft switching region
m_upper = 1-sqrt((Vcc*pi)^2*(d^2-1)-4*Po*d*omega*L*pi)/(Vcc*pi*d);
% Maximum m possible by definition of modulation index - unity
m_max = 1;

% Normalization and plotting
Z0 = (L/C)^(1/2); % Base Impedance
von = Vo/Vref; % Normalized Output Voltage
ion = io*Z0/Vref; % Normalized Output Current
Vccn = Vcc/Vref; % Normalized Input Voltage
t = linspace(0, T0, 1000); % time series
tn = t*f0; % normalized time

% iL target calculations for M6
iL_target1 = Vcc*(m*d*pi-pi-2*d*dd)/(2*omega*L);
iL_target2 = Vcc*(m*d*pi-pi+2*dd)/(2*omega*L);
iL_target3 = Vcc*(pi+m*d*pi-2*m*pi+2*dd)/(2*omega*L);
iL_target4 = -iL_target1;
iL_target5 = -iL_target2;
iL_target6 = -iL_target3;

% RMS current on transformer
ILrms = Vcc*sqrt(3*pi*(d^2*pi^3+12*dd^2*m*pi*d-8*d*dd^3+...
    12*dd*d*m*pi^2-6*m^2*d*pi^3-12*d*dd*(m*pi)^2+4*d*(m*pi)^3+...
    3*pi*(m*pi)^2-2*(m*pi)^3))/(6*omega*L*pi);

% Normalization of current targets
iLn_target1 = iL_target1/(Vref/Z0);
iLn_target2 = iL_target2/(Vref/Z0);
iLn_target3 = iL_target3/(Vref/Z0);
iLn_target4 = -iLn_target1;
iLn_target5 = -iLn_target2;
iLn_target6 = -iLn_target3;

% Plotting Natural Switching Surface Trajectories for DAB Buck Mode:
Limits = [-3,3]; % Limits placed on the axes of plots
Beta = 2*pi; % Associated angle related to iL zero crossing

u1 = 1;
u2 = -1;
A = iLn_target1 - ion*u2;
B = Vccn*u1 - u2;
iLn1 = A*cos(Beta*tn)+B*sin(Beta*tn)+ion*u2;
lambda1= @(von,iLn1) (Vccn*u1-von*u2).^2-(iLn_target1-ion*u2)^2-...
    (Vccn*u1-u2)^2+(iLn1-ion*u2).^2;
fimplicit(lambda1, Limits)
title('State Plane of Natural Switching Surfaces - Boost Mode');
xlabel('von');
ylabel('iLn');
hold on
```

```
u1 = 1;
u2 = 0;
A = iLn_target2- ion*u2;
B = Vccn*u1 - u2;
iLn2 = A*cos(Beta*tn)+B*sin(Beta*tn)+ion*u2;
lambda2 = @(von, iLn2) iLn2+Vccn*u1*von/ion-iLn_target2-Vccn*u1/ion;
fimplicit(lambda2, Limits)

u1 = 1;
u2 = 1;
A = iLn_target3 - ion*u2;
B = Vccn*u1 - u2;
iLn3 = A*cos(Beta*tn)+B*sin(Beta*tn)+ion*u2;
lambda3 = @(von, iLn3) (Vccn*u1-von*u2).^2-(iLn_target3-ion*u2)^2-...
    (Vccn*u1-u2)^2+(iLn3-ion*u2).^2;
fimplicit(lambda3, 'c', Limits)

u1 = -1;
u2 = 1;
A = iLn_target4 - ion*u2;
B = Vccn*u1 - u2;
iLn4 = A*cos(Beta*tn)+B*sin(Beta*tn)+ion*u2;
lambda4 = @(von, iLn4) (Vccn*u1-von*u2).^2-(iLn_target4-ion*u2)^2-...
    (Vccn*u1-u2)^2+(iLn4-ion*u2).^2;
fimplicit(lambda4,'r--',Limits)

u1 = -1;
u2 = 0;
A = iLn_target5 - ion*u2;
B = Vccn*u1 - u2;
iLn5 = A*cos(Beta*tn)+B*sin(Beta*tn)+ion*u2;
lambda5 = @(von, iLn5) iLn5+Vccn*u1*von/ion-iLn_target5-Vccn*u1/ion;
fimplicit(lambda5,'g--',Limits)

u1 = -1;
u2 = -1;
A = iLn_target6 - ion*u2;
B = Vccn*u1 - u2;
iLn6 = A*cos(Beta*tn)+B*sin(Beta*tn)+ion*u2;
lambda6 = @(von, iLn6) (Vccn*u1-von*u2).^2-(iLn_target6-ion*u2)^2-...
    (Vccn*u1-u2)^2+(iLn6-ion*u2).^2;
fimplicit(lambda6,'b--',Limits)
hold off
```

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