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# Pinned Photodiode CMOS Image Sensor TCAD Simulation: in-Depth Analysis of in-Pixel Pinning Voltage Measurement for a Diagnostic Tool

O. Marcelot, *Member, IEEE,* V. Goiffon, *Member, IEEE,* F. Nallet, and P. Magnan, *Member, IEEE*

***Abstract*—TCAD simulations are conducted on a pinned photodiode (PPD), with the aim to reproduce the pinning voltage measurement developed by Tan *et al*. A thermionic model is proposed and detailed in order to explain the exponential injection occurring at an injection voltage higher than the pinning voltage, and the correct method to extract the transfer gate inversion voltage is given. Then, various non idealities are simulated, such as doping variations or doping layer shifts, the goal being to get a PPD diagnostic tool based on the pinning voltage measurement. Finally, the pinned photodiode is simulated in a real reading mode, and a charge partition mechanism is demonstrated in specific conditions.**

***Index Terms*—CMOS Image Sensors, CIS, Simulation, Deep Submicron Process, CMOS, pinned photodiode, PPD, pinning voltage, transfer gate, TG, EFWC, solid-state image sensor.**

## I. INTRODUCTION

NOWADAYS, pinned photodiode CMOS image sensors (CIS) are widely used for commercial and scientific applications, because they have achieved very competitive performances [1], [2]. Despite PPD devices are commonly used [3], [4], characterizing, extracting the key parameters and simulating them is still not straightforward. Indeed, the pinned photodiode is placed within a pixel integrated inside an array, and experimenter cannot directly access basic parameters like the photodiode capacitance, the Full Well Capacity (FWC), or the pinning voltage ($V_{\mathrm{pin}}$).

To overcome this difficulty, special test structures were developed by various authors [5], [6], [7], [8], [9], [10], in order to access to the pinning voltage for instance. However, it appears that results are delicate to interpret because the electrical or the physical environment is not the same. Recently, a measurement technique was proposed to extract PPD parameters directly on a CIS pixel array, without the need of an associated test structure [8]. This method allows the extraction of the pinning voltage, the Full Well Capacity, the photodiode capacitance, and in some case the threshold voltage of the Transfer Gate [9], [11], [12]. Analyzing the full behavior of the experimental curve is not elementary, and the extraction of key parameters might be affected by non-idealities, which have been attributed to charge partition or even thermionic injection [11], [12], [13]. However, a disagreement is still existing on the different regimes and mechanisms explored by this technique.

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Therefore, the first goal of this work is to validate the mechanisms involved in the pinning voltage measurement proposed in [8] such as the thermionic injection and the charge partition, using TCAD simulations. The second goal of this work is to study the influence and the consequence of conception artifacts (non-idealities) like non-optimized implantation or incorrectly placed designed layer on the pinning voltage characteristic. These results should help the community to exploit the $V_{\mathrm{pin}}$ measurement as a diagnostic tool and possibly to optimize a design or a process. Finally, a last goal is to simulate the PPD in the normal reading condition, and to demonstrate the presence of the charge partition mechanism.

## II. DEVICE AND TEST DESCRIPTION

### A. Studied Device

All the simulations shown in this work are based on experimental results published in [11]. These results were obtained on a 4T CMOS image sensor. The pixel is based on a pinned photodiode with its readout circuitry composed of a Transfer Gate (TG) and the three additional transistors needed for resetting the pixel, amplifying the signal and for selecting the pixel [14]. The reference pixel studied in this work is a square PPD of 2.5 x 2.5 $\mu\mathrm{m}^2$ with a long TG on one side. The biases used are compatible with CMOS technology, between 0 V and 3.3 V.

### B. Test Description

The pinning voltage measurement method developed in [8] consists in a special readout mode of the imager. Indeed, it requires to inject charge in the PPD via the floating node by means of a modification of the reset drain bias ($V_{\mathrm{ddRST}}$). To do so, an injection phase is added to the basic timing diagram, before the reset of the floating node [8], [11] by lowering the $V_{\mathrm{ddRST}}$ to a polarization $V_{\mathrm{inj}}$. The $V_{\mathrm{pin}}$ characteristic is obtained by sweeping $V_{\mathrm{inj}}$ from -1.0 V to 3.3 V, the other electrical commands inside the pixel remaining at $V_{\mathrm{low}}$ = 0.0 V or $V_{\mathrm{high}}$ = 3.3 V. The full experimental details are reported in [11].

An example of experimental curve obtained for the $V_{\mathrm{pin}}$ measurement is given in the Fig. 1. At high injection voltage, when $V_{\mathrm{inj}}$ is higher than the TG inversion voltage $V_{\mathrm{inv}}$, no charge can be injected in the PPD and the output characteristic is null and flat (region "C"). Indeed, in this situation, the

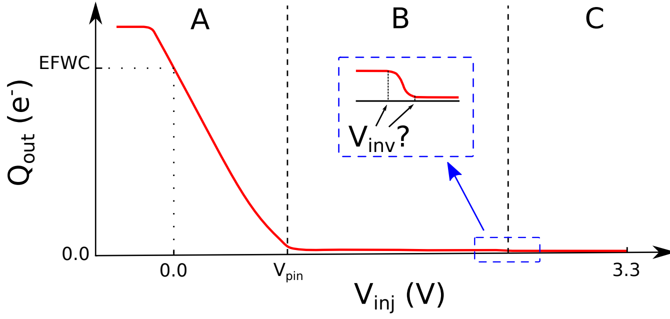


Fig. 1. Example of experimental curve obtained for the $V_{\text{pin}}$ measurement, modified from [11]. The identification of the $V_{\text{pin}}$ and the Equilibrium Full Well Capacity values are shown and two extractable values of the TG inversion voltage ($V_{\text{inv}}$) are given.

electron quasi Fermi level is higher than $V_{\text{pin}}$ and the channel potential under TG. An intermediate regime appears between $V_{\text{inv}}$ and $V_{\text{pin}}$ and the characteristic looks like a plateau (region "B"). The root cause of this phenomena is the presence of charge under TG because the electron quasi Fermi potential is below $V_{\text{inv}}$. When the TG is switched off, some electrons drift also toward the PPD and electrons are thus injected. This charge injection effect is called the charge partition [11], [15], [16]. If the injection voltage is inferior to $V_{\text{pin}}$, a linear injection takes place and the amount of injected electrons raises with the reduction of $V_{\text{inv}}$ (region "A"). In this condition, the electron quasi Fermi potential is identical in the PPD, under the TG and in the floating diffusion. For a low injection level, a plateau may be visible. If the plateau is visible for $V_{\text{inj}} \geq 0$ this observation may be due to a TG leakage because its channel potential is not enough low when the TG is off [12], or because of a saturation of the floating node. If it is visible for $V_{\text{inj}} \leq 0$, it is probably due to a too high junction forward current which prevents additional charge injection in the PPD and discharge it [11].

Around $V_{\text{pin}}$, the regime transition is not abrupt, and an exponential charge injection is established between the linear injection and the charge partition regime. This observation is attributed to thermionic injection, as it will be discussed hereafter. The Fig. 1 is also showing two points where the TG inversion voltage may be extracted. The TCAD simulation will help to understand what happens in this part and to discriminate the right inversion voltage.

A similar device and the same test set up is simulated in the following.

## III. TCAD SIMULATION

### A. Simulated Device

TCAD simulations are conducted using the Synopsys Sentaurus software. All simulations are conducted in 2D, as the transfer effects observed in this paper are only subjected to 2D effects. Nevertheless a 3D device was simulated in order to check that the $V_{\text{pin}}$ characteristic was in good agreement with the equivalent 2D device. The 2D simulated device is composed of a PPD with its transfer gate and a floating diffusion, and of a reset transistor allowing a floating state of the floating simulated node. The layers dimensions were taken

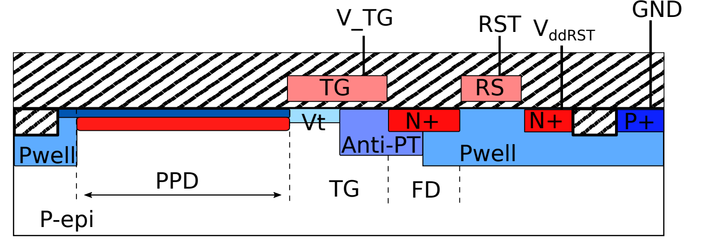


Fig. 2. Schematic cross-section of the 2D simulated device. TG is the transfer gate, RS the reset gate, N+ and P+ the drain implantations, Vt the threshold adjust implantation, and Anti-PT is the anti-punch-through implantation.

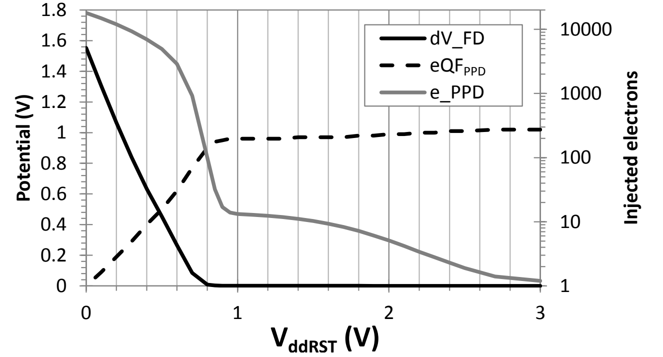


Fig. 3. TCAD simulation of the $V_{\text{pin}}$ measurement. The voltage drop of the floating diffusion (dV_FD) and the electron quasi Fermi level ($eQF_{\text{PPD}}$) are reported on the left axis, and the amount of injected electrons in the PPD (e_PPD) is reported on the right axis.

from the real device characterized in [11]. As it is generally the case, the PPD comprises the following layers, displayed in the Fig. 2:

- the N-PPD and the pinning P-PPD implantations
- the Pwell, isolating the circuitry from the bulk
- the N-plus layer, used for source or drain
- an anti-punch-through (APT), preventing leakage current between the floating node and the PPD
- a Vt adjust layer avoiding the presence of a barrier between the PPD and the APT layer
- a P-plus layer is used here as a ground contact (GND).

All doping profiles were obtained by SIMS measurement, and the 2D device is created by Sentaurus Structure Editor. The gate spacers width is fixed at 80 nm. An additional doping profile is used on the reset transistor to adjust its threshold voltage.

### B. Simulated test

The $V_{\text{pin}}$ measurement is simulated with the same condition as in II-B. After a reset of the PPD, electrons are injected in the PPD by means of a timing diagram similar to the one used in [8], [11]. At the end of this step, the number of injected electrons and the electron quasi Fermi potential in the PPD is read. Then, electrons are transferred in the reset floating node, and its potential is evaluated. This simulation sequence is performed for several $V_{\text{ddRST}}$ between 0.0 V to 3.3 V. During the electrical simulation, the following recombination models are activated in Sdevice: Auger, SRH(doping dependence) and Band2Band [17].

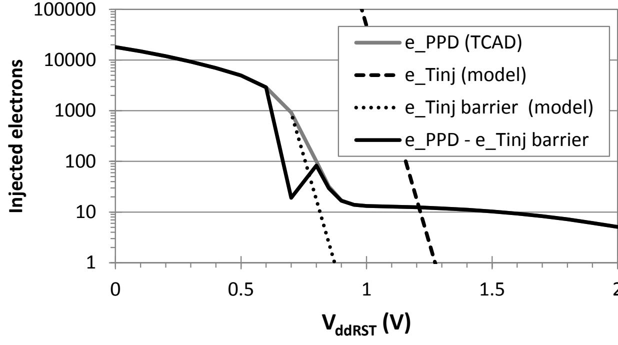


Fig. 4. TCAD simulation of the $V_{\rm pin}$ measurement and analytical model of the thermionic injection without (e_Tinj) and with potential barrier (e_Tinj barrier). The curve *e_PPD-e_Tinj barrier* is the TCAD injected electrons in the PPD minus the thermionic injected electrons analytical model, which shows a quasi suppression of the exponential injection.

The Fig. 3 is showing the simulation result for the $V_{\rm pin}$ measurement. As it can be seen, the simulated curve looks like the experimental one. At $V_{\rm ddRST} = 0$ V, the voltage drop of the floating diffusion is the highest, and it linearly decreases with the increase of $V_{\rm ddRST}$ until $V_{\rm ddRST} = V_{\rm pin} \approx 0.7$ V. For higher $V_{\rm ddRST}$, almost no more charge is injected in the PPD and the voltage drop remains flat. At $V_{\rm ddRST} = 0$ V, the electron quasi Fermi potential of the PPD is equal to 0.0 V because the PPD is at the Equilibrium Full Well Capacity (EFWC) [11], [18], and the amount of injected electrons is 18000. Then, between $V_{\rm ddRST} = 0.0$ V and $V_{\rm ddRST} \approx 0.7$ V, the electron quasi Fermi level in the PPD ($eQF_{\rm PPD}$) linearly increases as the amount of injected electrons decreases. And, between $V_{\rm ddRST} \approx 0.7$ V and $V_{\rm ddRST} \approx 0.9$ V, the electron quasi Fermi level still rises until $eQF_{\rm PPD} = 1$ V following a different law. Indeed, in this regime the amount of injected electrons exponentially decreases until approximately a dozen of electrons. This particular regime is due to the presence of thermionic emission, which is an exponential function of the electrostatic barrier seen by electrons [19], [20]. Finally, between $V_{\rm ddRST} \approx 0.9$ V and $V_{\rm ddRST} \approx 3.0$ V, the electron quasi Fermi level slightly increases of 0.05 V and the number of injected electrons slightly decreases until the full depletion of the PPD. This last regime corresponds to the charge partition regime, as mentionned in [11]. Therefore, as concluded in [13], in TCAD simulation two different extractions of $V_{\rm pin}$ may be done: the higher one (here, 0.9 V) gives the electron quasi Fermi level of the PPD when it is fully depleted as defined by Krymski [21], and the lower one (here, 0.7 V) is accessible experimentally, represents the electrostatic potential minimum of the PPD achieved when the depleted volumes contact. In the following, $V_{\rm pin}$ will represent the lowest value, accessible experimentally.

In the next part, the TCAD simulation and an analytical model are used to understand the mechanism at the origin of the thermionic injection.

### C. Thermionic injection

*1) Without barrier:* Firstly, the thermionic injection is modeled without any potential barrier between the PPD and the region under the TG. In this condition, it is supposed that the thermionic injection only occurs from the TG to the PPD when $V_{\rm pin} \geq V_{\rm inj}$. The amount of injected charge is then [20]:

$$Q_{\rm th} = KT^2 \exp(-\frac{q}{kT}(V_{\rm inj} - V_{\rm pin})) \times t_{\rm inj} \qquad (1)$$

$$K = A_{\rm R} \times {\rm Area_{inj}}\ ,\ A_{\rm R} = \frac{4\pi mqk^2}{h^3} \qquad (2)$$

In this work ${\rm Area_{inj}}$ is taken as $10\ {\rm nm} \times 1\ \mu{\rm m}$ and $K \approx 1.2 \times 10^{-8}\ {\rm Am^{-2}K^{-2}}$. The Fig. 4 is showing the $V_{\rm pin}$ measurement with the theoretical thermionic injected electrons using the calculated parameters for $V_{\rm ddRST} \geq 0.7$ V. As it can be seen, the amount of injected charge is much too high. In order to fit more suitable values, ${\rm Area_{inj}}$ should be reduced by seven orders of magnitudes. Consequently, the hypothesis ”without barrier” is unsuitable.

*2) With barrier:* A potential barrier $\phi$ is introduced between the PPD and the region under the TG. Electrons can go through this barrier from the TG and from the PPD. The amount of thermionic charge injected from the TG to the PPD is:

$$Q_{\rm thTG} = KT^2 \exp(-\frac{q}{kT}(V_{\rm inj} - V_{\rm pin} + \phi)) \times t_{\rm inj} \qquad (3)$$

At first, the amount of thermionic charge injected from the PPD to the TG should be:

$$Q_{\rm thPPD} = KT^2 \exp(-\frac{q}{kT}\phi) \times t_{\rm inj} \qquad (4)$$

However, compared to the reservoir of charge under the TG, the reservoir of charge in the PPD is extremely limited, because only few electrons have passed the barrier from the TG to the PPD. Therefore, the amount of electrons which can go through the barrier from the PPD to the TG must be balanced by a factor called here $\alpha$, which depends on the amount of electrons located in the PPD:

$$Q_{\rm thPPD}\,(\alpha) = \alpha KT^2 \exp(-\frac{q}{kT}\phi) \times t_{\rm inj} \qquad (5)$$

If the amount of charge in the PPD is high, or if $Q_{\rm thTG}$ is high, the factor $\alpha$ has to approach 1.0. In opposition, if the amount of charge in the PPD is very low, or if $Q_{\rm thTG}$ is low, the factor $\alpha$ has to approach 0.0. For this reason, the factor $\alpha$ is expressed as follows:

$$\alpha = A \times \frac{Q_{\rm thTG}}{Q_{\rm thPPD}} \qquad (6)$$

where $A$ is a constant.

The theoretical amount of thermionic injected electrons using an energetic barrier is displayed in the Fig. 4 (curve *e_Tinj barrier*), by taking a barrier $\phi = 100$ mV. By adjusting the $A$ constant (in this work $A = 0.9999928$) it is possible to figure out the thermionic part of injected electrons. To illustrate it, the number of injected electrons in the PPD is plotted minus the thermionic injected electrons, and it can be seen that the exponential part of the injected electrons curve has disappeared. This shows that the thermionic injection is a bidirectional injection between the PPD and the TG around a small potential barrier.

To gain a better insight on how the thermionic injection occurs, the Fig. 5 is showing a potential diagram under three

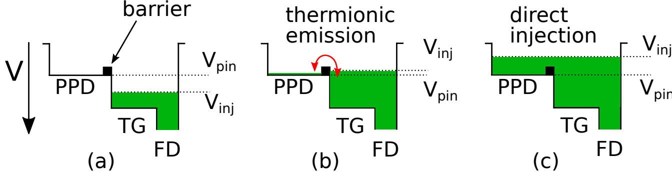


Fig. 5. Simplified electrostatic potential diagram of the PPD, TG, and FD for several injection bias conditions. (a) $V_{\rm inj}$ is too high, no thermionic injection. (b) $V_{\rm inj} \approx V_{\rm pin}$, bidirectional thermionic injection. (c) $V_{\rm pin} \leq V_{\rm inj}$, direct injection.

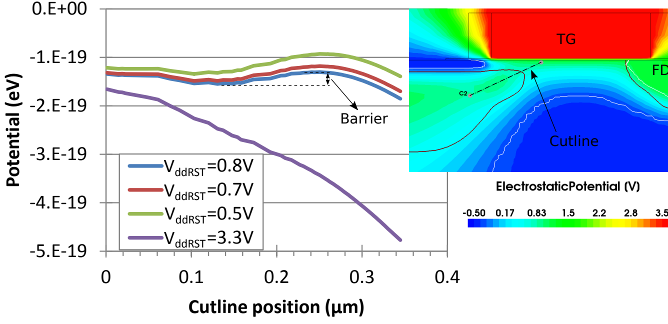


Fig. 6. TCAD simulation of potential under the TG when TG is "ON". A 2D electrostatic potential distribution is shown at $V_{\rm ddRST} = 0.7$ V, and cutlines for 4 $V_{\rm ddRST}$ are displayed in the graph. In real reading mode, $V_{\rm ddRST} = 3.3$ V.

conditions. Firstly (a), if $V_{\rm ddRST}$ is too high, no thermionic injection is detectable. When $V_{\rm ddRST}$ is around $V_{\rm pin}$ (b) the thermionic injection takes place and few electrons are injected in the PPD. Then, if $V_{\rm ddRST} \leq V_{\rm pin}$ the potential is lower than the energetic barrier and electrons are linearly injected in the PPD (c).

This confirms that $V_{\rm pin}$ must not be extracted at the point where the curve seems to meet the horizontal axis. $V_{\rm pin}$ can be extracted from a linear extrapolation from the EFWC condition or by an integral extrapolation [11].

It is important to note that the potential barrier introduced in this part for the $V_{\rm pin}$ measurement does not affect the charge transfer from the PPD to the floating node in a real reading mode. Indeed, as shown by the Fig. 6, the potential barrier is pulled toward the much higher floating node potential and no potential barrier is visible.

*3) Influence of TG pulse duration:* In order to check the reliability of the TCAD model with the thermionic injection, the simulation is performed with various TG pulse durations during the injection phase. According to experimental results, the longer the TG pulse duration, the higher the contribution of the thermionic injection is [11], because the thermionic emission is directly time dependent (see equation (1)). As it can be seen on the Fig. 7, for very short TG duration the thermionic injection becomes negligible. And, by increasing the TG pulse duration, the thermionic injection is more and more visible. This observation validates the TCAD simulation and the presence of thermionic injection.

### D. Extracting a potential barrier from a curve shift

The potential barrier previously introduced does not affect the transfer from the PPD to the floating node in a reading mode. Let us suppose now that this potential barrier is strong enough and disturbs the PPD read-out. This could be the case if the bottleneck or the "corridor" between the photodiode and the TG is long enough, creating an electrostatic barrier [11]. In this situation, the voltage at which the injection starts is reduced because of the presence of the potential barrier, and electrons remain in the PPD, causing Charge Transfer Inefficiency (CTI). Consequently, the $V_{\rm pin}$ curve is shifted to the left (Fig. 8), and by knowing the PPD capacitance [11] it is then possible to calculate the height of the potential barrier:

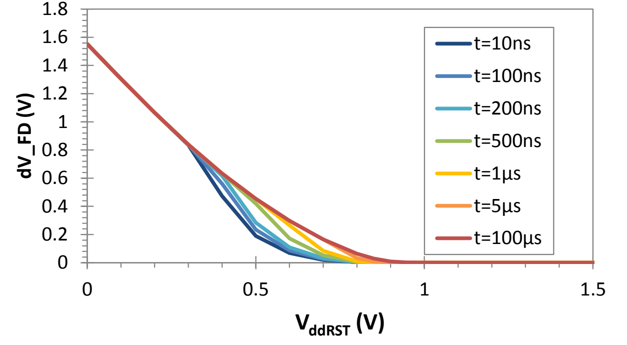


Fig. 7. $V_{\rm pin}$ characteristics simulated for several TG pulse duration during the injection phase.

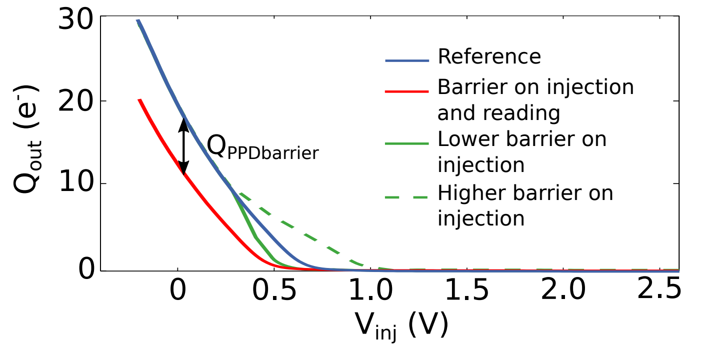


Fig. 8. $V_{\rm pin}$ characteristics modified by the presence of a potential barrier during the injection mode and possibly in the reading mode. $Q_{\rm PPDbarrier}$ is the amount of electrons blocked in the PPD by the potential barrier.

$$Q_{\rm PPDbarrier} = \int_{V_{\rm pin}}^{V_{\rm barrier}} C_{\rm PPD} dV \qquad (7)$$

where $Q_{\rm PPDbarrier}$ is the amount of electrons blocked in the PPD by the potential barrier extracted from Fig. 8, $V_{\rm barrier}$ is the height of the potential barrier, and $C_{\rm PPD}$ is the PPD capacitance. In a similar way, other works mention a shift of the photon transfer curve because of a potential barrier under the TG which is present in the reading mode [22], [23]. Electrons remain in the PPD and cannot be transferred due to this potential barrier, and authors propose an extraction of their quantity from the curve shift.

As shown by Fig. 8, two kinds of potential barrier in the vicinity of TG may induce two different behavior on the $V_{\rm pin}$ curve. If the barrier is present in injection and reading mode, it induces a curve shift and a higher CTI. If the barrier is

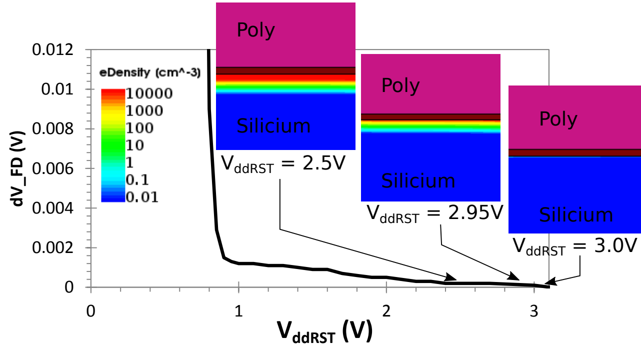


Fig. 9. Zoom in of a simulated $V_{\mathrm{pin}}$ characteristic, and a selection of 2D electrons density distribution under the TG for $V_{\mathrm{ddRST}} = 2.5\ V$, $V_{\mathrm{ddRST}} = 2.95\ V$ and $V_{\mathrm{ddRST}} = 3.3\ V$. TG inversion is visible for $V_{\mathrm{ddRST}} \leq$ 2.95 V.

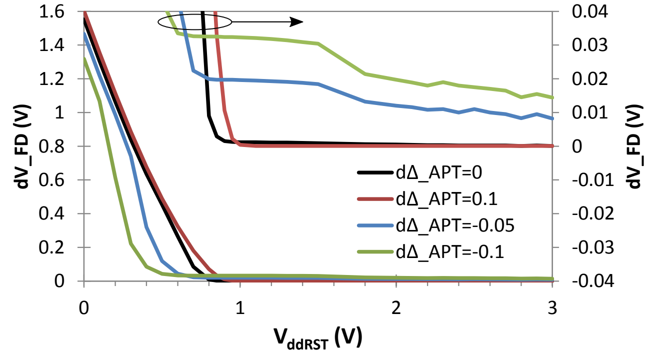


Fig. 10. TCAD simulation of $V_{\mathrm{pin}}$ characteristics of the PPD with variation on the anti-punch-through implantation (APT) position. A magnification of the characteristic shows a transfer of residual electrons which were not discharged in a previous reset of the PPD, commonly referred as lag.

TABLE I
TCAD EXTRACTION OF THE TG INVERSION VOLTAGE FOR SEVERAL $V_{\mathrm{TGhigh}}$.

| $V_{highTG}$ (V) | 3.5 | 3.3 | 3.1 | 2.9 | 2.7 | 2.5 | 2.3 |
|---|---|---|---|---|---|---|---|
| $V_{inv}$ (V) | 2.95 | 2.95 | 2.8 | 2.65 | 2.45 | 2.25 | 2.1 |

only present in injection mode, it influences the thermionic injection and should not increase the CTI.

### E. Charge partition

Charge partition is an effect which is visible when $V_{\mathrm{pin}} \leq V_{\mathrm{inj}} \leq V_{\mathrm{inv}}$ [11]. Indeed, when $V_{\mathrm{inj}}$ is below $V_{\mathrm{pin}}$, an inversion channel appears under the TG, and a charge partition mechanism between the PPD and the FD occurs when the TG is turned off. As a consequence, a plateau is visible in the $V_{\mathrm{pin}}$ characteristic between $V_{\mathrm{pin}}$ and $V_{\mathrm{inv}}$ (Fig. 1). This plateau is also visible in the TCAD simulation (see Fig. 9). Although this effect is well identified, extracting the TG inversion voltage from this curve is not obvious [12]:

- at the intersection of the $V_{\mathrm{pin}}$ characteristic with the horizontal axis (at about 2.8 V in Fig. 9)
- at the end of the plateau (somewhere between 1 V and 2 V in Fig. 9)

To clarify this aspect, some TCAD pictures were recorded at several $V_{\mathrm{inj}}$, TG being on. As shown by the Fig. 9, the inversion channel is visible under the TG if $V_{\mathrm{ddRST}}$ is lower than 2.95 V. Therefore, the TCAD simulation shows that the TG inversion voltage should be extracted at the intersection of the $V_{\mathrm{pin}}$ characteristic with the horizontal axis. Further TG inversion voltages are extracted for various $V_{\mathrm{TGhigh}}$ by means of 2D electron density TCAD pictures on the TG region. In this exercise, the high $V_{\mathrm{TG}}$ value is changed from 3.3 V to other $V_{\mathrm{highTG}}$ values, $V_{\mathrm{lowTG}}$ remaining at 0.0 V. All the extracted values are summarized in the Tab. I. Using the methodology proposed in [11], it is possible to estimate the channel doping level from the different inversion voltage extraction. An average doping concentration of $4.0 \times 10^{16}\ \mathrm{at/cm^3}$ is found from the values in the Tab. I, which is in a good agreement with the acceptor concentration used for the TCAD simulation (around $6.0 \times 10^{16}\ \mathrm{at/cm^3}$).

## IV. Study of Conception Artifacts: Development of a Diagnostic Tool

Once the TCAD model gives good confidence in reproducing Vpin experiment and all the $V_{\mathrm{pin}}$ characteristic behavior, it can be used to study artifacts introduced by process or design parameters on the $V_{\mathrm{pin}}$ characteristic. The aim is to elaborate a diagnostic tool based on the comparison of the $V_{\mathrm{pin}}$ curve with a reference one, which can help the designer to find a root cause of a possible problem on PPD design or process. With the aim of reaching this goal, three different conception modifications are introduced in the TCAD simulation, and their consequences are studied.

### A. Modification of anti-punch-through implantation

In the first part, the anti-punch-through implantation position is modified around the reference position which is defined by the foundry. TCAD simulations of the $V_{\mathrm{pin}}$ measurement are shown in the Fig. 10 for various shifts of the implantation. $\Delta_{\mathrm{APT}} \leq 0$ means that the implantation is moved in the direction of the PPD, and $\Delta_{\mathrm{APT}} \geq 0$ means that it is shifted in the opposite direction. As it can be seen, the closer to the PPD the implantation is, the lower the apparent $V_{\mathrm{pin}}$ is, the lower the thermionic injection is, and the higher the lag is. The lag is identified by the amount of residual electrons not discharged in a previous PPD transfer and visible in the magnification of the curve in Fig. 10, as a potential deviation of the floating node due to the lag transfer. The reason is the increase of ”P” type doping between the PPD and the floating diffusion which leads to a higher potential barrier and a lower transfer quality. Thus, if the anti-punch-through implantation is too closed to the PPD, the whole curve is shifted, it shows a more pronounced drop before $V_{\mathrm{pin}}$ which prevents the right $V_{\mathrm{pin}}$ extraction (Fig. 10). In opposition, moving away from the PPD the anti-punch-through implantation improves the transfer but may increase the parasitic collection of the floating node and its leakage current with the PPD.

Secondly, the anti-punch-through doping is changed. Simulations results are displayed in Fig. 11. Compared to the anti-punch-through shift, similar effects are visible on the $V_{\mathrm{pin}}$ curves by changing the implantation doping. The lower the

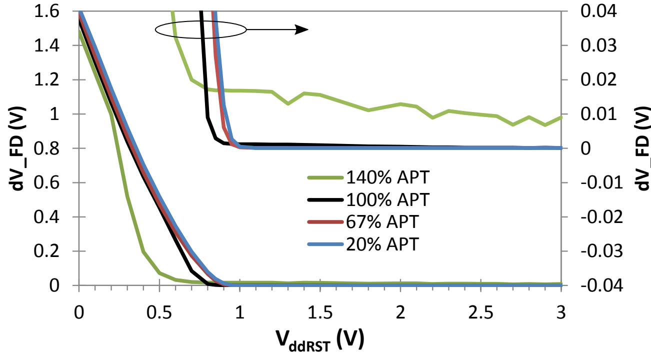


Fig. 11. TCAD simulation of $V_{\text{pin}}$ characteristics of the PPD with variation on the anti-punch-through implantation (APT) doping. A magnification of the characteristic shows a transfer of residual electrons which were not discharged in a previous reset of the PPD, commonly referred as lag.

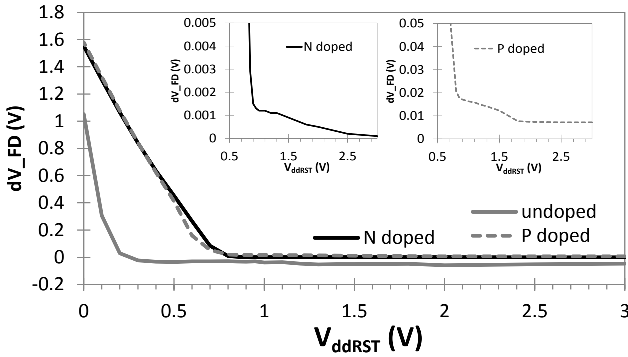


Fig. 12. TCAD $V_{\text{pin}}$ characteristic of the PPD with the reference N-doped TG, an undoped TG and a P-doped TG. A magnification of the characteristic shows the charge partition and the lag.

doping is, the higher the thermionic injection is. And the higher the doping is, the lower the apparent $V_{\text{pin}}$ is, and the higher the lag is. With a too high anti-punch-through doping, the potential barrier between the PPD and the FD is too high and the charge transfer is seriously affected. Moreover, as previously, $V_{\text{pin}}$ cannot be extracted.

To conclude, a too highly doped or a too closed APT implantation can be detected from the $V_{\text{pin}}$ measurement. Indeed, in this case, the PPD will have an important lag, and the $V_{\text{pin}}$ curve will show a apparent reduced $V_{\text{pin}}$ with a more pronounced drop before $V_{\text{pin}}$ and almost no thermionic injection.

### B. TG doping

In this situation, the transfer gate doping is modified. Firstly, the gate is let undoped, as if the "N" type doping implantation has been skipped. Secondly, the gate is "P" doped. The Fig. 12 is showing the simulated results. With an undoped gate, the voltage drop across the gate becomes significant and the resulting potential difference at the bottom of the gate between the "on" and the "off" state is getting small. As a consequence, it is extremely difficult to transfer charge to and from the PPD, and the $V_{\text{pin}}$ characteristic is strongly shifted to the small $V_{\text{ddRST}}$ values. If the TG is "P"-doped, the global $V_{\text{pin}}$

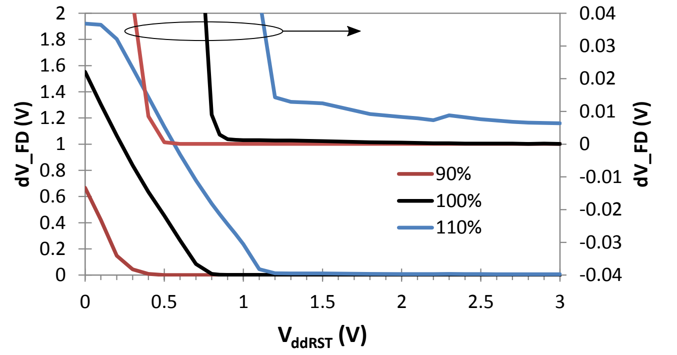


Fig. 13. TCAD $V_{\text{pin}}$ characteristic of the PPD with variation on the "N" sensor implantation doping. 100% means the reference implantation doping. A magnification of the characteristic shows the charge partition and the lag.

characteristic looks similar to the reference one. However, if a magnification of the "P"-doped characteristic closed to the horizontal axis is observed, it is possible to see a strong charge partition effect and a lower inversion voltage due to the TG "P" type doping which decreases the flatband voltage. Moreover, resulting electrons attributed to the lag are also visible, because the "P"-doped gate has lower flatband voltage and it is then more difficult to transfer efficiently electrons between the PPD and the floating diffusion.

Finally, an undoped gate can be detected with a $V_{\text{pin}}$ measurement because the apparent $V_{\text{pin}}$ is abnormally low. A "P" doped gate can be identified by extracting an abnormally low TG inversion voltage, associated with a higher lag compared to the "N" doped gate PPD.

### C. NPDD doping

Finally the impact of the "N" sensor doping concentration on the $V_{\text{pin}}$ characteristic is evaluated. As expected and shown by the Fig. 13, a reduction of the "N" sensor doping concentration leads to a shift of the $V_{\text{pin}}$ curve to the left, because $V_{\text{pin}}$ and the EFWC are reduced. In opposition, a higher "N" sensor doping concentration increases the $V_{\text{pin}}$ and therefore the EFWC. For the smallest values of $V_{\text{ddRST}}$ the simulation shows a plateau, because of the saturation of the floating node. A higher "N" sensor doping concentration also causes a higher lag because the PPD is more difficult to fully deplete.

Therefore, a change in the "N" sensor doping concentration is also detectable by the $V_{\text{pin}}$ measurement by means of the curve shift. A higher doping should also induce a higher lag.

### D. Conclusion

To conclude this part, the TCAD simulations show that at least three kinds of conception anomalies can be detected by observing the $V_{\text{pin}}$ characteristic. This study based on simulations highlights which part of the $V_{\text{pin}}$ characteristic is affected by the anomaly, and it can be used as a diagnostic tool based on the observation of the pinning voltage measurement.

## V. PPD IN REAL OPERATING MODE

As the simulated PPD is now verified and calibrated, a TCAD study of the PPD in its standalone mode is performed.

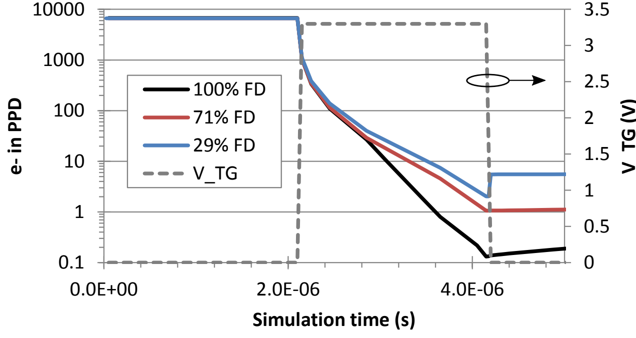


Fig. 14. TCAD simulation of the PPD in a real reading mode. At $t = 0$, electrons are already injected in the PPD. After a reset phase, TG is ON at $t = 2.1$ $\mu$s and OFF at $t = 4.2$ $\mu$s, using a rise time and a fall time of 50 ns. Electrons stored in the PPD are monitored during the transfer phase for three floating diffusion sizes.

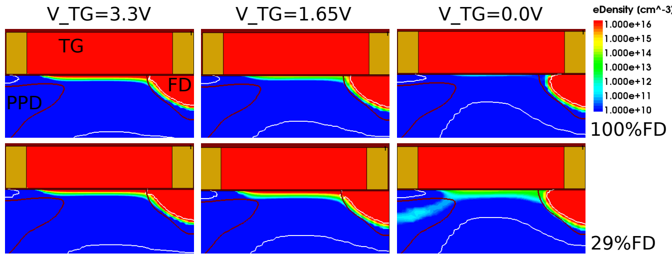


Fig. 15. 2D TCAD electron density distributions around the TG during a real reading mode at the end of the transfer step and before TG is switched off ($V_{\mathrm{TG}} = 3.3$ V), at mid ramp ($V_{\mathrm{TG}} = 1.65$ V) and when TG reaches zero ($V_{\mathrm{TG}} = 0.0$ V). The reference PPD (100% FD) and the PPD with a reduced floating node (29% FD) are shown.

With the aim to study how the charge partition phenomena may occur in a PPD operated in real reading mode, the electrical simulation is modified. To do so, the injection phase using the reset transistor is suppressed in the timing diagram and replaced by an optical illumination. The illumination is characterized by a wavelength of $\lambda = 700$ nm and a power of $10$ $\mu\mathrm{W/cm^2}$, which generates about 6600 electrons in the PPD. The rising and falling times of the electrical commands are $50$ ns and the plateau during the transfer phase is $2$ $\mu$s long. The monitoring of electrons stored in the PPD during the transfer phase is displayed in the Fig. 14 for three floating node lengths:

- 100% of the reference length, as previously
- 71% of the reference length
- 29% of the reference length

If the floating diffusion is not reduced, all electrons stored in the PPD are transferred in the floating node, and no electrons are reinjected in the PPD when the TG is switched off. If the floating node area is reduced at 71% of the reference, its capacity is reduced and about one electron remains in the PPD because the floating node potential rises faster. At 29% of the reference area two electrons remain in the PPD at the end of the transfer plateau, and when TG is switched off more than three electrons are sent back in the PPD due to charge partition.[1]

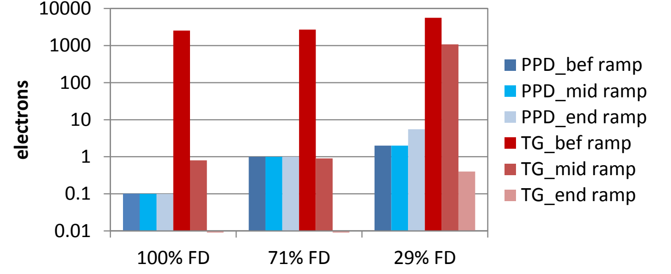


Fig. 16. TCAD simulation of the amount of electrons in the PPD or under TG at the end of the transfer step for three floating node sizes. The amount of electrons are shown before the falling ramp, at the half of the falling ramp, and at the end of the falling ramp.

2D electron density pictures of the PPD with the highest and smallest FD are displayed in Fig. 15 at the end of the transfer step and before the falling ramp, at half of the falling ramp and at the end of the falling ramp. In addition, the amount of electrons integrated in the PPD and under the TG are reported in the Fig. 16 at the same time steps. When no charge partition is detectable in the simulation (100% FD and 71% FD), almost all electrons under the TG are transferred to the floating node before the half of the ramp down. In the PPD simulated with the smallest FD, a high amount of electrons under the TG is still not transferred to the floating node at the half of the falling ramp and the charge partition occurs in the last falling ramp part together with the transfer of the remaining electrons under TG.

This result shows that the charge partition mechanism may also occur in a PPD operated in a real reading mode, if the floating node is not sized correctly. Indeed, in this case, the floating node saturates before reaching the required FWC and electrons under the TG may go back to the PPD when TG is switched off. This mechanism occurs in the last part of the falling ramp of the TG, as a high amount of electrons has not been transferred to the floating node.

## VI. Conclusion

TCAD simulations were conducted on a pinned photodiode in order to reproduced the pinning voltage measurement developed by Tan [8]. TCAD results reproduce well experimental behaviors, and show the charge partition effect. By analyzing electrons distributions, these simulations have shown that the inversion voltage must be read at the intersection of the $V_{\mathrm{pin}}$ characteristic with the horizontal axis. In addition, it was shown that a thermionic bilateral injection process occurs through a potential barrier at $V_{\mathrm{ddRST}} \geq V_{\mathrm{pin}}$.

By using this TCAD setup, conception artifacts were simulated in order to operate the $V_{\mathrm{pin}}$ characteristic as a diagnostic tool for PPD design or process issues, by comparing the reference measurement with the one showing one or several problems. Therefore, TCAD simulations have shown that a 40% more doped or a 50 nm too closed APT implantation can

[1]The same simulation was conducted with 300 electrons and did not show any spilled back electrons. It validates that the CTI is not degraded in the 29% FD device.

be detected thanks to an important lag, a $V_{\rm pin}$ curve showing a apparent reduced $V_{\rm pin}$ with a more pronounced drop before $V_{\rm pin}$ and almost no thermionic injection. Then, an undoped gate can be detected because the apparent $V_{\rm pin}$ is extremely low. A "P" doped gate can be identified by means of a lower TG inversion voltage, associated with a higher lag compared to the "N" doped gate PPD. Finally, TCAD shows that a variation of 10% of PPD dose can be easily detected with Vpin measurements by observing a shift of the $V_{\rm pin}$ curve and eventually a much higher lag for a higher "N" sensor doping concentration.

The PPD was also simulated in a real reading mode, as it is used in an imager. The TCAD simulator has shown that the charge partition mechanism may also be present in this case, in particular if the floating node has a small capacity. In this situation, the charge partition occurs at the end of the falling ramp of the TG.

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