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Marcelot, Olivier and Goiffon, Vincent and Rizzolo, Serena and Pace, Federico and Magnan, Pierre Dark Current Sharing and Cancellation Mechanisms in CMOS Image Sensors Analyzed by TCAD Simulations. (2017) IEEE Transactions on Electron Devices, 64 (12). 4985-4991. ISSN 0018-9383

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Dark Current Sharing and Cancellation Mechanisms in CMOS Image Sensors Analyzed by TCAD Simulations

O. Marcelot, *Member, IEEE,* V. Goiffon, *Member, IEEE,* S. Rizzolo, *Member, IEEE,* F. Pace, *Student Member, IEEE,* and P. Magnan, *Member, IEEE*

***Abstract*—TCAD simulations are conducted on a 4T PPD pixel, on a conventional gated photodiode, and finally on a radiation hardened pixel. Simulations consist in demonstrating that it is possible to reduce the dark current due to interface states brought by the adjacent gate, by means of a sharing mechanism between the photodiode and the drain. The sharing mechanism is activated and controlled by polarizing the adjacent gate at a positive *off* voltage, and consequently the dark current is reduced and not compensated. The drawback of the dark current reduction is a reduction of the full well capacity of the photodiode, which is not a problem when the pixel saturation is limited by the readout chain. Some measurement performed on pixel arrays confirm the TCAD results.**

***Index Terms*—CMOS Image Sensors, CIS, Simulation, Deep Submicron Process, CMOS, pinned photodiode, PPD, Dark current, solid-state image sensor, STI.**

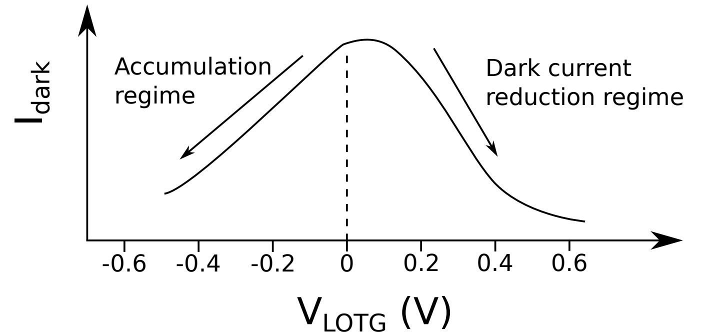

Fig. 1. Example of dark current evolution with the transfer gate off voltage (V_{LOTG}). Two main regimes are visible: accumulation regime, and a dark current reduction regime

I. Introduction

THANKS to the latest technological progress, CMOS Image Sensor (CIS) are now widely used for commercial and scientific applications. The photo-sensitive element is either a conventional photodiode, or a Pinned Photodiode (PPD) [1], [2], [3], and is associated to a readout circuitry based on 3 to 4 and even more transistors [4], the whole forming a pixel. Contrary to conventional photodiodes, pinned photodiodes are built by a buried N-doped layer, which is not in contact with the surface, and a very narrow and highly P-doped layer between the surface and the buried N-layer, preventing any contact between the depletion extension from the photodiode and the oxide, which insures a dramatic dark current reduction compared to conventional photodiodes [3].

PPDs have been extensively studied in order to understand all the transfer mechanisms between the photodiode and the floating diffusion, the PPD key feature parameters and its access [5], [6], [7]. Although many dark current measurements of pinned photodiodes have been presented, to our knowledge, no study explains and demonstrates the possibility of dark current reduction by sharing mechanisms between adjacent PN junctions. Indeed, if a dark current curve versus the *off* Transfer Gate (TG) voltage (V_{LOTG}) is analyzed [8], [9], it shows 2 different regimes (Fig. 1):

- accumulation regime, at negative V_{LOTG}
- a dark current reduction regime, at positive V_{LOTG}

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At V_{LOTG} = 0 V, depletion extensions of the PPD and the transfer gate are merged, leading to a high dark current due to interface states below the TG. When V_{LOTG} is lowered to negative values, the transfer gate is accumulating, and the depletion region of the PPD does not reach the interface states below the TG any more. Therefore, dark current is highly reduced. If V_{LOTG} is too low, the TG accumulation may extend into the PPD vicinity, and it may lead to a high leakage current called Gate Induced Drain Leakage (GIDL), similar to the one found in MOSFET [10]. For positive V_{LOTG} values, a dark current reduction can be observed, and can be even more important than during the TG accumulation regime.

The purpose of this work is to demonstrate that a dark current reduction is possible at positive V_{LOTG}, and does not consist in a dark current compensation. To do so, TCAD simulations will be conducted on a 4T PPD, in order to analyze the dark current electron displacements and the eventual parasitic collection by the positive transfer gate *off* voltage. Then, other applications of this dark current reduction will be presented, like conventional 3T photodiode and radiation hardened pixels. First of all, and for a better understanding, conventional dark current sources of 4T PPD pixels are given.

II. Different dark current sources

In a 4T photodiode, several dark current sources may be identified. One can describe the following current contributions [11], [12], [13], [14] (Fig. 2):

- interface states generation at the Silicon - Oxide interface (I_1)

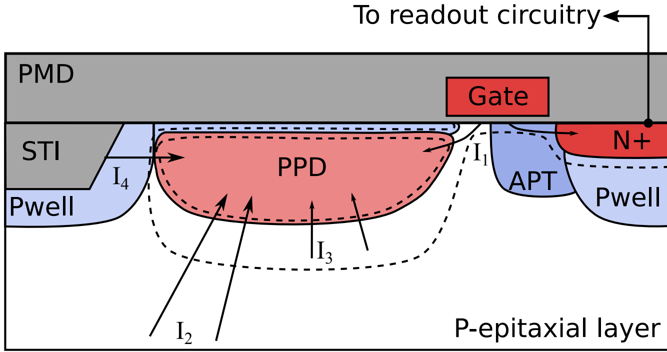

Fig. 2. Schematic view of a 4T PPD pixel showing the different dark current contributions. The readout circuitry is not shown (reset transistor, source follower, row selector), and APT is for the Anti-Punch Through implantation. The dashed lines represent the depletion extension of the photodiode, for a depleted transfer gate. In order to illustrate the dark current sharing mechanism, the I_1 current generated under TG is shared between the PPD and the FD.

- minority carrier diffusion from the bulk (I_2)
- electron-hole pair generation in the depletion region (I_3)
- sidewalls and edges of Shallow Trench Isolation (STI) (I_4), and PMD

In a pinned photodiode, the pinned layer prevents any contact between the depletion extension of the photodiode and the surface, avoiding interface states generation dark current. However if the transfer gate is in depletion regime, the depleted TG channel merges with the photodiode depletion extension and an intense dark current due to interface states appears (I_1). The electron-hole pair generation in the space charge region is supposed to be low, because of the very weak defects concentration (I_3). Subsequently, the impact of sidewalls and edges of STI is negligible because of the depletion extension which is not supposed to merge with the STI due to the Pwell passivation.

In a pinned photodiode operated with an Anti-Blooming (AB) gate, the main dark current contributor remains the interface states at the silicon - oxide interface under the gate. It is proposed to study this contribution in this paper using a positive V_{LOTG}, as described in the following parts.

III. Study of 4T PPD dark current reduction by sharing mechanisms

A. Principle of the sharing mechanism

Exchange of charge by means of punch-through mechanisms between adjacent and depleted nodes have been already studied for more and fully-depleted photodiodes array in very high resistive substrates [15], [16]. In these papers, the depletion extension of adjacent photodiodes in highly resistive substrate may be merged and therefore leads to leakage current between photodiodes, depending on the potential barrier along the leakage path and the photodiode potential. Consequently, electrons stored in adjacent photodiodes are shared until an equilibrium is reached. In these applications this phenomenon has to be avoided. In our case, dark current electrons generated under the gate in the depleted channel are shared between the drain and the photodiode, but unlike the punch-through phenomenon, integrated electrons in the PPD and electrons in the FD are not shared.

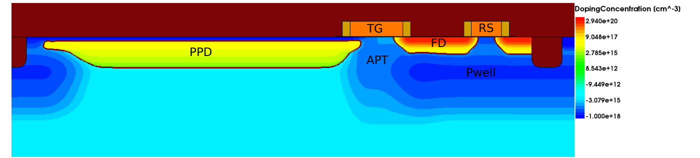

Fig. 3. TCAD doping distribution of the 4T simulated PPD showing the different layers: PPD, Transfer Gate (TG), Reset Gate (RS), Pwell implantation, Anti-Punch Through (APT) implantation. FD is the Floating Diffusion.

In a 4T photodiode, the TG is put in depletion for positive V_{LOTG} in *off* state. The photodiode depletion extension merges with the TG depletion region and the floating diffusion depletion region. Thus, the dark current generated by interface states under the TG can be shared between the photodiode (as it is generally the case) and the floating diffusion (Fig. 2), which leads to a dark current reduction. In this situation the floating diffusion does not directly collect photo-generated electrons thanks to the Anti-Punch Through (APT) implantation, but may discharge the photodiode by means of a punch-through current, depending on the potential barrier between the PPD and the FD. The ratio of dark current captured by the floating diffusion over the total dark generated current depends on the V_{LOTG} voltage, as long as the floating diffusion does not collect photo-generated electrons, which would result in loss of QE.

On the following part, a 4T PPD pixel is studied by means of TCAD simulation, in order to identify the benefits and the drawbacks of the dark current sharing mechanisms.

B. Dark current reduction on a 4T PPD photodiode

A 4T PPD is simulated, using the Synopsys Sentaurus 2015 software. The simulation is performed in two dimensions, and the doping distribution is built from Secondary Ion Mass Spectrometry (SIMS) doping profiles. The electrical study is performed with the Sdevice tool, activating the following models: recombination using Shockley Read Hall with doping dependance, Auger and Band to band. The 2D simulated device is composed of a PPD with its transfer gate and a floating diffusion, and of a reset transistor allowing a floating state of the floating simulated node. The photodiode is 4 μm long, and the 4T PPD device comprises the usual layers [17]: a P+ pinning and a N+ photodiode layer, an APT layer preventing leakage between the PPD and the floating node, a Vt adjust layer in the first part of the TG channel, a N+ layer used for the floating diffusion, and a Pwell isolating the floating diffusion and the reset transistor from the bulk (Fig. 3).

Firstly, the PPD is emptied thanks to the activation of the reset and the transfer gate. Then, the TG is biased at V_{LOTG}, and the distribution of electron quasi Fermi energy (eQF) is plotted (Fig. 4). The 2D distribution of eQF shows that the potential increases in the TG channel from the PPD side to the FD side, which is favorable to a dark current discharge towards the floating diffusion. Actually, dark current generated in the TG channel at the vicinity of the PPD may be captured by

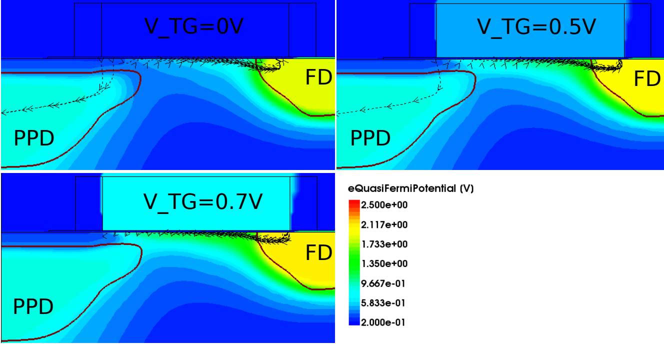

Fig. 4. TCAD electron quasi Fermi energy distribution of the 4T simulated PPD at V_{LOTG} = 0 V, V_{LOTG} = 0.5 V, and V_{LOTG} = 0.7 V. Streamlines driven by the gradient of electron quasi Fermi are also plotted. Each streamline is spaced apart 15 nm, 15 nm under the gate oxide. The red line represents the junction line.

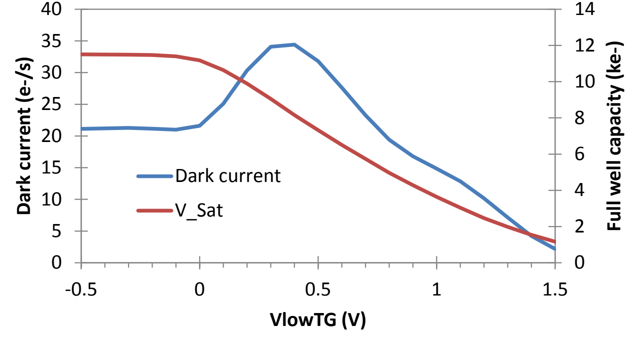

Fig. 6. Dark current and full well capacity measurements performed at 22 C on 4T PPD pixels for various V_{LOTG}.

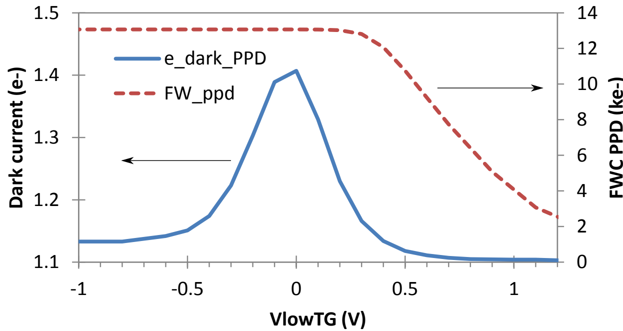

Fig. 5. In blue line, TCAD simulation of the amount of dark current electrons integrated in the PPD during 10 μs. A hole trap model is used with a concentration of 5×10^9 traps.cm^{-2} and a capture cross sections of 1×10^{-15} cm^2. The curve without hole trap model is also shown for comparison. In red dashed line, TCAD simulation of the FWC of the PPD for various V_{LOTG}.

the PPD because the photodiode implantations extend slightly under the TG and the PPD potential competes with the TG channel potential. In the Fig. 4, curves (streamlines) tangents to the gradient of eQF [18] are displayed, because they show the path followed by dark current electrons in the TG channel. At V_{LOTG} = 0 V, dark current electrons generated in the PPD vicinity are captured by the PPD. And, by increasing V_{LOTG} until 0.7 V, all dark current electrons are drained from the gate channel to the floating diffusion: the dark current is reduced. Consequently, increasing the TG polarization increases the channel potential and drives effectively all the dark current, even the part generated in the vicinity of the PPD.

To go further, a dark current integration of the PPD is simulated. In a same way as in [19], a hole trap model in specified in Sdevice and emulates the dark current generation. It is defined at all silicon-oxide interfaces, with a concentration of 5×10^9 traps.cm^{-2} and a capture cross sections of 1×10^{-15} cm^2. After emptying the photodiode, the TG is biased at V_{LOTG}, and the photodiode integrates dark electrons during 10 μs. The amount of integrated dark electrons is reported in the Fig. 5 for various V_{LOTG}. The dark current shape is similar to the one presented in Fig. 1, and shows a maximum centered at 0 V. The position of this maximum depends on the process and on the design. Therefore in the following the increase ΔV_{LOTG} of the *off* polarization of the TG will be referenced to the dark current maximum position V_{LOTG} = 0 V. This result clearly shows a high reduction of the dark current by increasing ΔV_{LOTG}. For an increase of 0.5 V, the residual amount of electrons in the PPD is even lower than in the accumulation regime, which means that the dark current coming from the interface states of the TG is canceled.

The parasitic collection due to the positive polarization of V_{LOTG} is also a matter of the greatest concern. In order to analyze the impact of the sharing mechanism on the parasitic collection, the Full Well Capacity (FWC) of the PPD is analyzed against V_{LOTG}. Indeed, if the PPD is at the equilibrium and full of electrons, its potential approaches zero, and by increasing V_{LOTG} the potential barrier between the PPD and the floating node disappears, and a leakage current can flow from the PPD to the floating node, performing like an anti-blooming system. As the potential barrier between the PPD and the FD decreases, the saturation level of the PPD decreases as well. In the Fig. 5 the FWC is extracted by monitoring the amount of electrons in the PPD at the beginning of the simulation, V_{LOTG} being biased and the PPD not reset. For an increase of $\Delta V_{\mathrm{LOTG}} \geq 0.3$ V, the FWC starts to decrease. As the FWC reduction is conditioned by the potential barrier mitigation between the PPD and the FD, it may occur at a different V_{LOTG} compared with the dark current reduction.

Therefore, TCAD simulations have shown that operating the PPD with TG at a positive voltage in *off* state leads to a cancellation of the dark current coming from the interface states under TG. By doing so, it seems possible to achieve similar or even better dark current reduction compared to PPD operated in accumulation regime, for an increase of $\Delta V_{\mathrm{LOTG}} \geq 0.5$ V. However, the increase of ΔV_{LOTG} to positive voltage causes a reduction of the FWC of the PPD. This consequence is not a problem if the pixel has a high CVF or if the pixel saturation is limited by the readout circuitry.

C. *Measurement of dark current reduction by sharing mechanism*

A dark current measurement is performed on 7 μm 4T PPD pixels implemented in an array, manufactured using a sub-micrometer imaging CMOS process identical to the one used for the TCAD study. The measurement is done at 22 C for various polarization of V_{LOTG} (Fig. 6).

The maximum dark current is achieved at V_{LOTG} = 0.4 V, and decreasing V_{LOTG} leads to a dark current reduction, the TG being accumulated. The dark current reduction occurs until V_{LOTG} = 0 V from which a plateau is visible. Then, if V_{LOTG} is increased beyond 0.4 V a dark current reduction by sharing mechanism is visible. At 0.8 V, the dark current level is comparable to the one achieved in accumulation regime. The same figure also shows the measured full well capacity of the PPD. As it can be seen, for positive polarization of V_{LOTG}, the saturation level monotonously decreases until 10 % of the Equilibrium FWC (EFWC) at V_{LOTG} = 1.5 V. At V_{LOTG} = 0.9 V, i.e at ΔV_{LOTG} = 0.5 V, the FWC is at 35 % of the EFWC, which is a bit lower than the TCAD simulation. Compared to the simulation, curves are shifted, and the PPD saturation decreases for smaller V_{LOTG}. The root cause is supposed to be the imprecision of the doping profiles simulated in the transfer gate region, as the threshold adjust implantation and the tooling applied on APT and sensor implantations were deducted from experimental observations. Indeed, small variations on these implantation positions or concentrations have strong impacts on charge transfer and PPD FWC [17].

This measurement confirms the TCAD results: increasing V_{LOTG} at positive voltage leads to a dark current reduction, and this performance is accompanied by a decrease of the PPD FWC. Again, if the pixel has a high CVF or if the pixel saturation is limited by the readout circuitry saturation, the reduction of FWC is not a particular issue.

IV. Other applications of the dark current reduction by sharing mechanism

A. *Dark current reduction on a conventional 3T photodiode*

In spite of the development of high performance pinned photodiode, conventional 3T CMOS image sensors are still used for commercial and scientific applications, because they don't need an advanced CMOS images process, they offer a better full well capacity and the possibility to design large pixel pitches [14], [20] without transfer issue. Therefore, the study of dark current reduction in conventional photodiodes is still an active topic. For instance, some works have been done on the photodiode design by surrounding the pixel by a p-well [21], or by introducing dark current compensation mechanisms [22], [23], [24], [25], [26], [27]. Some of these concepts of dark current compensation consist in subtracting a calibrated dark frame by means of a shielded dummy pixel, or even by controlling a negative feedback using the reset transistor. Hence, these methods rely on the addition of a current in order to compensate the dark current, but they do not reduce the dark current shot noise and the dark current non uniformity. As depleted extremities of conventional 3T

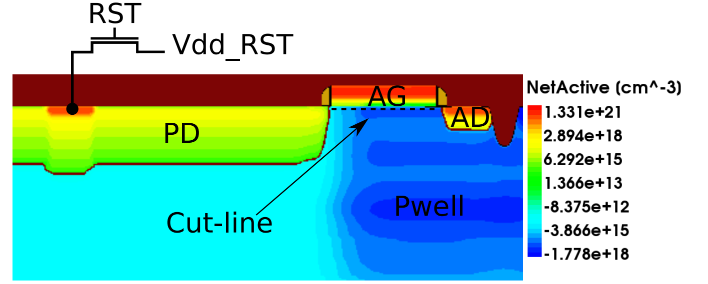

Fig. 7. TCAD doping distribution of the conventional simulated photodiode showing the different layers: PD, Adjacent Gate (AG), Adjacent Drain (AD), Pwell implantation. The electrical simulation is performed in mixed mode and the schematic of the reset transistor modeled with a spice model is shown.

photodiodes are known dark current sources, one approach is also to use gated diodes [28]. Besides, in [28], the authors show that the dark current of irradiated gated diodes can be reduced by increasing the gate voltage, but they do not go into details concerning what happens on the other side of the gate. On the following, a gated diode is studied, and considering the results previously obtained on a 4T PPD, the concept of dark current reduction by sharing mechanisms is applied on it.

A 2D 5 μm long gated photodiodes is simulated with a 1 μm adjacent gate (called here Adjacent Gate, AG) next to a drain (Adjacent Drain, AD) (Fig. 7). The electrical simulation is performed in Mixed Mode, and a reset transistor allowing a floating state of the photodiode is connected to the conventional photodiode. The spice model of the reset transistor is the one given by the founder. Firstly, a reset phase is applied to the photodiode by means of the reset transistor, and the adjacent drain is biased at 3.3 V. Then, the adjacent gate is biased at V_{AG}.

In order to analyze the lateral electric field distribution in the gate channel, a cross-section along a cut-line 15 nm below the surface oxide from the left side to the right side of the AG is performed (see the representation of the cut-line in Fig. 7). The cross-sections of the lateral electric field for various V_{AG} are shown in the Fig. 8. The gate channel is divided into two sections in which the electric field opposes. Indeed, even at V_{AG} = 0 V, a potential gradient tends to push the charge to the photodiode in the left part of the gate channel, and from about L = 0.45 - 0.5 μm, the point where the electric field polarity changes, and another potential gradient drives the charge to the adjacent drain. By increasing the adjacent gate voltage, the lateral electric field grows from negligible values to about 500 V/cm all along the gate channel until the drain, which should efficiency lead the dark current electrons towards the drain.

As in the part dealing with the 4T PPD, a dark current integration of the PPD is simulated by means of the introduction of a hole trap model at the silicon-oxide interface. The same trap model parameters are used and the net excess of dark electrons generated by the trap model is plotted in the Fig. 9. The simulation clearly shows a high reduction of the dark current by increasing the V_{AG} voltage. However, V_{AG} cannot be too much increased without degradation of

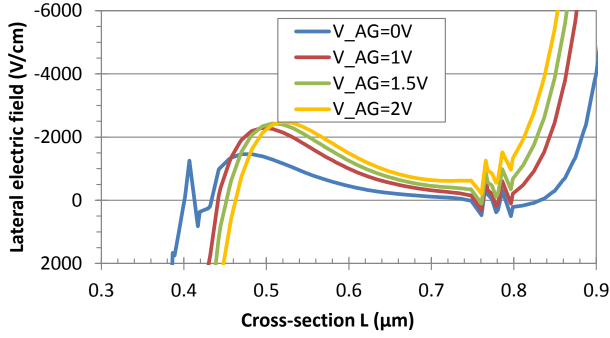

Fig. 8. TCAD cross-section along the cut-line of the lateral electric field for various V_{AG}.

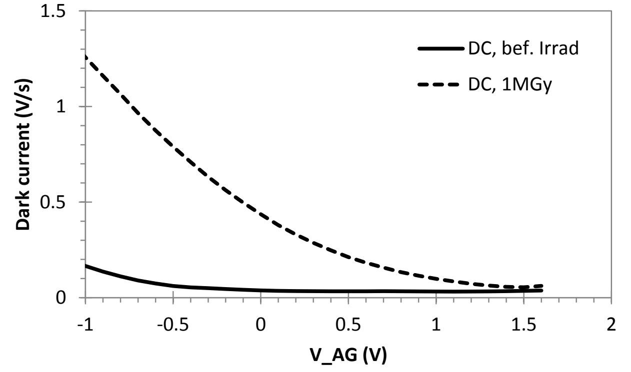

Fig. 10. Dark current measurements performed at 22 C on a radiation hardened pixel including a gated photodiode for various V_{AG}. In straight line before irradiation, and in dashed line after an irradiation at 1 MGy.

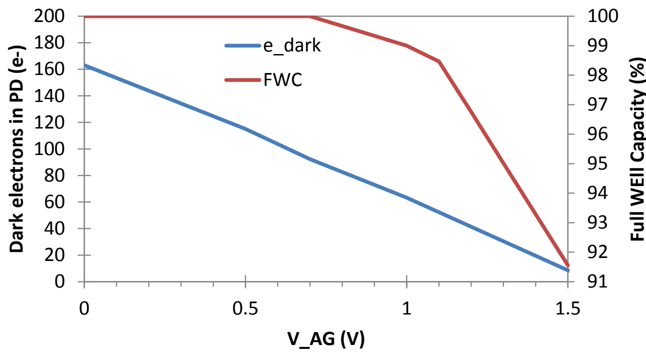

Fig. 9. TCAD simulation of the amount of dark current electrons integrated in the photodiode during 10 μs, and full well capacity of the photodiode vs V_{AG}. A hole trap model is used to simulate the dark current generation with a concentration of 5×10^{9} $\mathrm{traps.cm}^{-2}$ and a capture cross sections of 1×10^{-15} cm^{2}.

the collection properties of the photodiode. This aspect is also studied in the same Fig. 9, and the evolution of the FWC of the photodiode according to V_{AG} is plotted. The FWC remains constant until V_{AG} = 1.0 V, where the dark current contribution due to interface states under the AG is reduced by 60 %. For $V_{\mathrm{AG}} \geq 1.0$ V, the FWC slightly decreases as the potential barrier starts to be weak between the photodiode and the AD, and a leakage current appears reducing the photodiode saturation. Therefore in order to avoid a modification of the FWC, from these TCAD results, it is recommended not to exceed V_{AG} = 1 V. But, as wrote before, if the pixel has a high CVF or if its saturation is limited by the readout chain, it seems possible to increase V_{AG} at 1.5 V and to take advantage of a quasi-cancellation of the dark current brought by the AG.

From these results, TCAD simulation have shown that it possible to reduce the dark current generated by gates surrounding a conventional photodiode, without affecting the quantum efficiency of the pixel. Like the 4T PPD, a special attention has to be taken on the surrounding gate voltage, as a compromise has to be found between dark current reduction and current leakage between the photodiode and the adjacent drain.

B. Dark current reduction on a hardened photodiode

Radiation hardening techniques usually rely on design optimization, and especially by surrounding the photodiode by a gate [29] which is responsible for an increase of dark current, due to interface states. In addition, Total Ionizing Dose (TID) irradiation induces interface states at silicon oxide interfaces, which increases the dark current still more [31]. By considering the previous sections, it seems possible to reduce the dark current brought by the additional gate by using the principle of sharing mechanisms. Moreover, a measurement using this idea was already published in [30], and one of the conclusion is that the gate isolated pixel exhibits a much lower dark current than the other designs after irradiation if the gate voltage is increased until 1.5 V. Besides, the authors explain that the dark current can be reduced like if the pixel was not irradiated. In order to illustrate these statements, the Fig. 10 is showing measurements performed on a chip including hardened pixels with gated photodiodes (design similar to the one in Fig. 11). After a 1 MGy irradiation, the dark current is highly increased at V_{AG} = 0 V, but by increasing V_{AG} until 1.5 V the dark current returns to its minimal value before irradiation. One of the explanation given by the authors in [30] is a presence of a sharing mechanism between the photodiode and the drain which reduces the photodiode collection of thermally generated dark current, without direct leakage current between the photodiode and the drain. Indeed, after irradiation, a high amount of positive trapped charge is located at silicon-oxide interfaces [13], [31] and create a weak inversion, that is a depleted volume around the STI. This depleted volume extends from the gate channel to the drain, and a part of the dark current is evacuated through this way. The purpose of this part is therefore to demonstrate the accuracy of this explanation.

A doping distribution of the simulated device is presented in the Fig. 11. The simulated device is similar to the one measured in [30] and has a conventional photodiode (PD), an additional 1 μm long adjacent gate (AG) and a adjacent drain (AD). As previously the simulation is run in mixed mode, and a spice modeled reset transistor is connected to the conventional photodiode. Firstly, a reset phase is applied

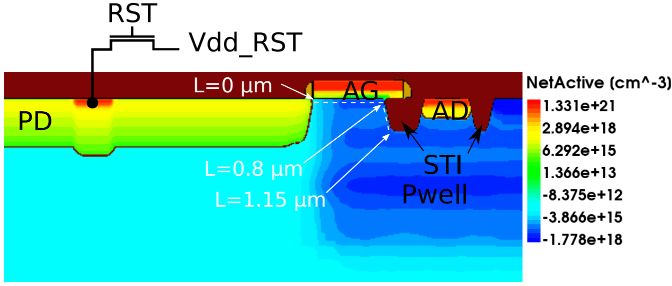

Fig. 11. TCAD doping distribution of the radiation hardening photodiode showing the different layers: PD, Adjacent Gate (AG), Adjacent Drain (AD), Pwell implantation. The electrical simulation is performed in mixed mode and the schematic of the reset transistor modeled with a spice model is shown. An illustration of the cut-line chosen for the eQF cross-section is also shown in white dashed line.

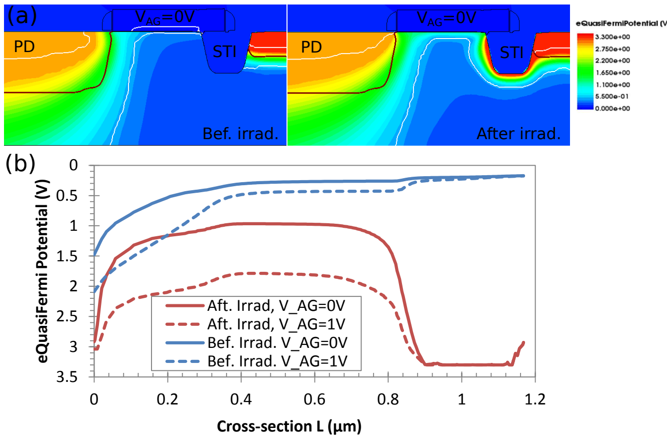

Fig. 12. (a) TCAD 2D distributions of electron quasi Fermi potential before and after irradiation, (b) Plot of the eQF along the cut-line of the pixel before and after irradiation, and for V_{AG} = 0 V and V_{AG} = 1 V.

to the photodiode, and the drain is biased at 3.3 V. Then, the adjacent gate is biased at V_{AG}, and the two dimensional distributions of the electron quasi Fermi energy is analyzed. In order to reproduce the defects induced by the irradiation in the oxide, an uniform distribution of positive fixed charge is implemented at the silicon-oxide interface. The surface concentration of positive fixed charge is adjusted in a way that the STI edges can be depleted, that is a charge concentration of $5.0 \times 10^{12} cm^{-2}$.

The Fig. 12 is showing the two dimensional distributions of the eQF centered on the adjacent gate. The distributions are shown before irradiation at V_{AG} = 0 V, and after irradiation, which means that the charge defect model is activated at oxide interfaces. Moreover, for a better analyze of the potential gradient, a cross-section (see Fig. 11) of the eQF is plotted along the depleted channel in Fig. 12 (b). After irradiation the charge defect model allows a depletion around the STI, leading to a fully depleted channel from the photodiode to the adjacent drain. Without irradiation, a potential gradient is oriented from the gate channel to the photodiode for both adjacent gate polarization, and any generated dark current electrons is drained from the gate channel to the photodiode, leading to a dark current increase. After irradiation, or when the charge defect model at oxide interface is activated, the eQF is kept close to the drain potential along the STI sides because of the depletion. Hence, a new attractor pole for dark current electrons generated in the gate channel is created. The eQF cross-sections displayed in the Fig. 12 clearly show that in the first part of channel gate, from L = 0 μm to L = 0.4 μm, there is a potential gradient which drives the dark current electrons from the channel to the photodiode. Then, from L = 0.4 μm, the potential gradient is oriented in the opposite direction and drives the charge from the gate channel to the adjacent drain. Increasing V_{AG} = 0 V to V_{AG} = 1 V results in a higher channel potential, which should improve the charge collection by the depleted channel. These observations from the TCAD simulation clearly demonstrate that in the case of an irradiated pixel, an important part of dark current electrons generated in the gate channel can be captured by the adjacent drain instead of the photodiode. As observed in [30], it leads to a dark current reduction.

The above TCAD simulations demonstrate that the dark current generated by a gate surrounding the photodiode can be reduced, after irradiation, by polarizing the gate at a positive voltage. However, as in the previous sections, a tradeoff has to be found between the dark current reduction (the adjacent gate polarization) and the leakage current between the photodiode and the adjacent gate.

V. Conclusion

TCAD simulations has been performed firstly on a 4T PPD pixel, and the principle of dark current reduction by sharing mechanisms is demonstrated. To do so, the *off* polarization of the TG is put at a positive voltage and dark current electrons generated under the gate by interface states can be efficiently drive toward the floating node instead of the PPD. Simulations under illumination show that V_{LOTG} must be kept in the range of 0.5 - 0.7 V otherwise the full well capacity is decreased. A measurement performed on a pixel array confirms the principle.

Then, this idea is applied on a conventional gated photodiode. By polarizing the adjacent gate to a positive voltage, the TCAD simulation is showing a real cancellation of the dark current generated by interface states, and not just a compensation. Again, V_{LOTG} has to be increased to a reasonable value (here 1 V) in order to avoid a leakage current between the photodiode and the drain. At V_{LOTG} = 1 V the dark current generated by interface states under the gate is reduced by 60 %, and at V_{LOTG} = 1.5 V it is nearly canceled at the expense of a slight full well capacity reduction.

Finally, a TCAD simulation is performed on a radiation hardened pixel, in which a measurement shown a reduction of dark current on an irradiated pixel by increasing positively the adjacent gate voltage. The simulation is used to verify that the dark current by sharing mechanisms is the root cause of this observation, as supposed in the original study.

Therefore, this work shows that it is possible to cancel and not to compensate the dark current contribution brought by a transfer gate in the case of a 4T PPD, or by adjacent gates in conventional gated photodiodes, by applying a positive voltage

on the adjacent gate. The higher the gate voltage, the higher the dark current reduction, but the higher the risk of leakage current between the photodiode and the drain is. A tradeoff has to be found, depending on the application.

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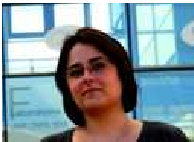

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