Investigation of Tm_2O_3 as a Gate Dielectric for Ge MOS Devices

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In this work atomic layer deposited Tm_2O_3 has been investigated as a high-k dielectric for Ge-based gate stacks. It is shown that when Tm_2O_3 is deposited on high-quality Ge/GeO_2 gates, the interface state density of the gate stack is degraded. A series of post-deposition anneals are studied in order to improve the interface state density of $Ge/GeO_x/Tm_2O_3$ gates, and it is demonstrated that a rapid thermal anneal in O_2 ambient can effectively reduce the interface state density to below $5 \cdot 10^{11}$ $cm^{-2}eV^{-1}$ without increasing the equivalent oxide thickness. Fixed charge density in $Ge/GeO_x/Tm_2O_3$ gates has also been investigated, and it is shown that while O_2 post-deposition anneal improves the interface state density, the fixed charge density is degraded.

Introduction

Germanium (Ge) has been intensively investigated as a high-mobility channel material alternative to silicon (Si). Formation of a high quality interfacial layer between the dielectric and Ge substrate is one of the crucial challenges regarding the fabrication of Ge metal-oxide-semiconductor (MOS) devices (1). Therefore, achieving a Ge gate stack with interface state density D_{it} compared to Si is essential for the competitive device performance. GeO_2 has been identified as a potential candidate for an interfacial layer (IL) due to effective Ge surface passivation with D_{it} in the range of 10^{11} $cm^{-2}eV^{-1}$ (1). In order to achieve scaled effective oxide thickness (EOT) a combination of GeO_2 IL and a high-k dielectric is needed. However, it was shown that employing a conventional high-k dielectric such as HfO_2 degrades the electrical properties of Ge gate stacks due to intermixing of GeO_2 and HfO_2 (2). On the other hand, low interface state density in the range of 10^{11} $cm^{-2}eV^{-1}$ has been achieved while employing Al_2O_3 barrier (3) as well as rare earth oxides such as Y_2O_3 (4). Therefore, a high-k rare-earth oxide with sufficient band offsets could be a good candidate for a high-k dielectric in Ge/GeO_2 gate stacks.

Rare-earth thulium oxide (Tm_2O_3) provides a high dielectric constant k~16 (5) and sufficient valence (3.05 eV) and conduction (2.05 eV) band offsets (6) for a high-k dielectric layer on Ge. In this work we investigate the effect of Tm_2O_3 deposition on high-quality Ge/GeO_2 interfaces. The impact of the post-deposition anneal (PDA)

ambient, temperature and time on the interface state density, capacitance equivalent thickness (CET) and fixed charge in the gate stack is examined.

Experiments

MOS capacitors were fabricated to evaluate the electrical properties of $Ge/GeO_x/Tm_2O_3$ gate stacks. The process flow is depicted in Figure 1.

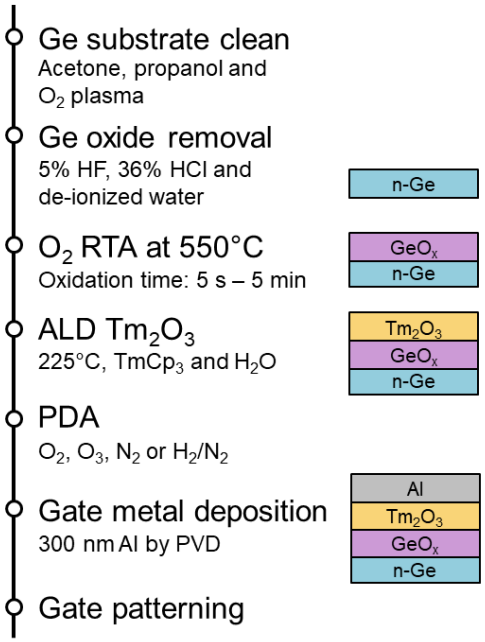

Figure 1. Process flow of $Ge/GeO_x/Tm_2O_3$ MOS capacitors. $Ge/GeO_x/Tm_2O_3$ gate stacks are formed by thermal oxidation and subsequent Tm_2O_3 deposition. The gates are then subjected to PDA at different ambients (O_2, O_3, N_2 or H_2/N_2) and temperatures (350 - 550 °C depending on the ambient).

In order to fabricate MOS capacitors, n-type Ge (100) substrates with doping concentration of $\sim 10^{15}$ cm^{-3} were cleaned with acetone, propanol and O_2 plasma. After native germanium oxide was removed with aqueous HF and HCl solutions and de-ionized water, the samples were immediately loaded into the rapid thermal anneal (RTA) chamber where oxidation was carried out at 550 °C for 5 s to 5 min. The temperature in the chamber is controlled by a pyrometer which is calibrated to a Si wafer, and oxidation is performed by placing a Ge substrate piece on a Si carrier wafer. The temperature of the Ge sample is thus lower than that of the Si wafer. After oxidation, the samples were loaded to atomic layer deposition (ALD) chamber where 40 cycles (~7 nm) of Tm_2O_3 were deposited using $TmCp_3$ and H_2O as precursors. Then some of $Ge/GeO_x/Tm_2O_3$ gate stacks were annealed in different ambients (O_2, O_3, N_2 and H_2/N_2) and temperatures (350 – 550 °C). Reference samples without Tm_2O_3 deposition or without PDA were also fabricated. Al gate metal was deposited by physical vapor deposition and patterned.

MOS capacitors were electrically characterized with capacitance-voltage (CV) measurements. Interface state density in the midgap was evaluated from CV curves using a method described in (7). Some of the samples were investigated by X-ray photoelectron

spectroscopy (XPS) measurement in a chamber with a base pressure of $5 \cdot 10^{-10}$ mbar and using Al Kα X-ray (1486.6 eV) source. The Ge 3p spectra were calibrated using a measured GeO_2/Ge substrate, and the position of its elemental germanium peak was used as a reference for all samples.

Results and Discussion

The impact of Tm_2O_3 deposition on Ge/GeO_2 gates

Germanium MOS capacitors with Ge/GeO_2 gates and interface state density in the midgap below $5 \cdot 10^{11}$ $cm^{-2}eV^{-1}$ have already been realized by thermal oxidation in RTA chamber (7). The influence of Tm_2O_3 deposition by ALD on these high-quality Ge/GeO_2 interfaces was determined by depositing a Tm_2O_3 layer on Ge/GeO_2 stacks with varying GeO_2 thicknesses. Interface state density values in the midgap were extracted from the MOS capacitor CV measurements and are displayed in Figure 2. Tm_2O_3 deposition degrades D_{it} in the midgap up to 5 times for low GeO_2 thickness (total CET < 5 nm). However, even for thick GeO_2 (total CET ≥ 9 nm) D_{it} is ~$9 \cdot 10^{11}$ $cm^{-2}eV^{-1}$ which is around two times higher than in reference MOS capacitors with Ge/GeO_2 gate stack. It is clear that the ALD Tm_2O_3 layer deposition has a detrimental effect on the Ge/GeO_2 interface quality.

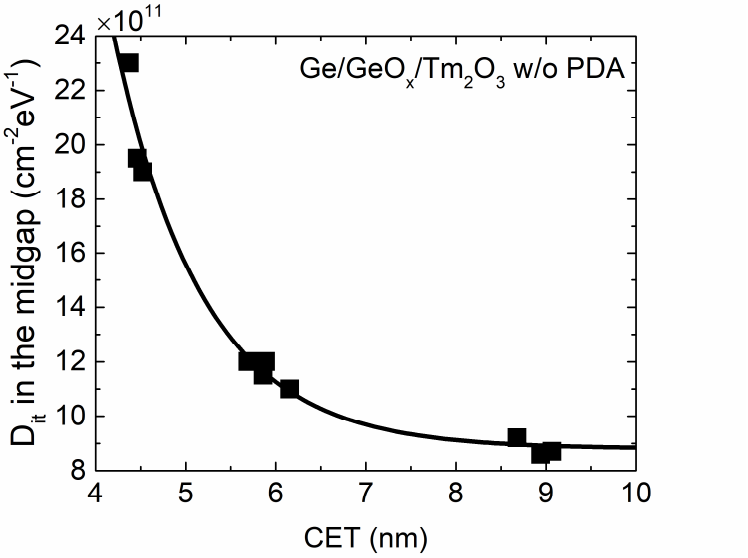

Figure 2. D_{it} in the midgap values for Ge/GeO_x/Tm_2O_3 gate stacks with varying GeO_x thickness. D_{it} decreases with increasing GeO_x thickness and reaches ~$9 \cdot 10^{11}$ $cm^{-2}eV^{-1}$. The line is an indicative guide for the eye.

PDA influence on Ge/GeO_x/Tm_2O_3 gates

Series of post-deposition anneals were performed on Ge/GeO_x/Tm_2O_3 gates in order to investigate their impact on interface state density and capacitance equivalent thickness. PDAs in various ambients (O_2, O_3, N_2 or H_2/N_2) and temperatures (350 – 550 °C) were

carried out on the gate stacks with thin GeO_x (GeO_x thickness < 3 nm, total CET ~4.5 nm in Figure 2). The impact of the anneals on D_{it} and CET is summarized in Figure 3.

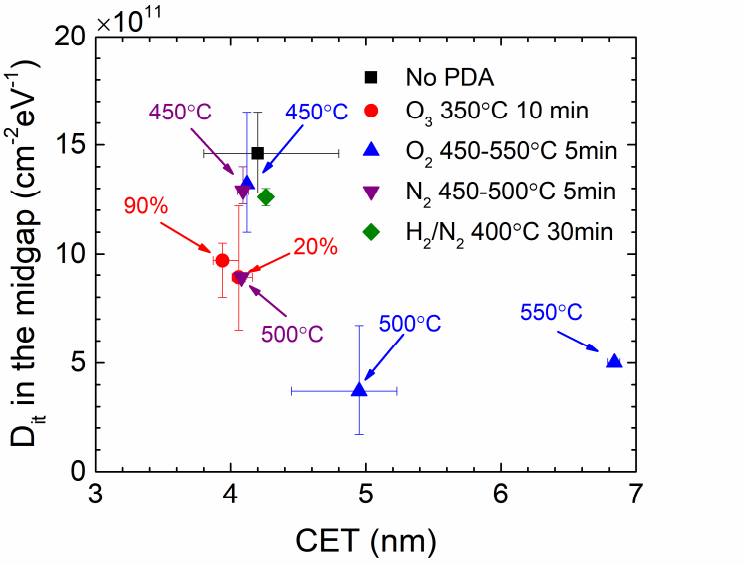

Figure 3. D_{it} in the midgap and CET values for $Ge/GeO_x/Tm_2O_3$ gate stacks after various post-deposition anneals. The anneals were performed in O_2, O_3, N_2 or H_2/N_2 ambient and at 350 – 550 °C. O_2 anneal at 500 °C gives lowest D_{it} but with an increase in CET.

It was found that PDA in N_2, H_2/N_2 or O_2 at temperatures below 500 °C does not significantly influence neither D_{it}, nor CET. PDA in ozone at 350 °C or N_2 at 500 °C slightly reduces D_{it} to ~$1 \cdot 10^{12}$ $cm^{-2}eV^{-1}$ without an increase in CET. On the other hand, O_2 anneal at 500-550 °C significantly reduces the interface state density to similar values as in Ge/GeO_2 gates. O_2 PDA, however, increases the CET of the samples, and to a higher extent for higher PDA temperatures suggesting that GeO_x growth occurs during oxidation. This is further confirmed by XPS measurement of $Ge/GeO_x/Tm_2O_3$ stacks before and after O_2 PDA at 500 °C. The obtained Ge 3p spectra are displayed in Figure 4. The ratio between GeO_x peak and Ge elemental peak in Ge 3p spectra grows after PDA in O_2 confirming the growth of GeO_x. Moreover, in both spectra, before and after PDA, the difference between GeO_x peak and Ge elemental peak did not change suggesting that germinate was not formed after anneal. The binding energy difference is 2.6 eV which corresponds to Ge^{3+} oxidation state.

Even though O_2 PDA at 500 °C offers the lowest D_{it} values, a 5 min anneal also increases the CET of the gate stack, which is unwanted for scaled MOS devices. Therefore, the impact of the anneal time was investigated. The results are shown in Figure 5 where D_{it} and CET values versus PDA time are displayed. It is shown that 1 min anneal is sufficient to decrease D_{it} to $<5 \cdot 10^{11}$ $cm^{-2}eV^{-1}$, and further oxidation does not improve the interface quality. CET also remains approximately the same after 1 min anneal but eventually starts increasing when oxidation continues. Therefore, O_2 PDA at 500 °C for 1 min is concluded to be appropriate for $Ge/GeO_x/Tm_2O_3$ gates since low D_{it} values can be achieved without increasing CET.

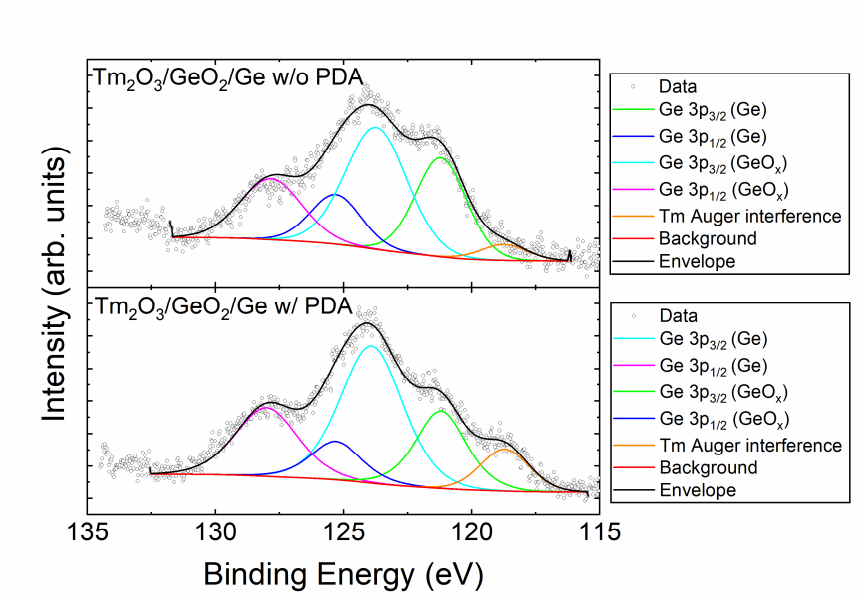

Figure 4. Ge 3p and spectra obtained by XPS measurements for $Ge/GeO_x/Tm_2O_3$ gate stacks without (top) and with (bottom) O_2 PDA at 500 °C. The shift between Ge elemental and GeO_x peaks corresponds to Ge^{3+} oxidation state. The ratio between Ge elemental and GeO_x peaks suggests GeO_x growth during O_2 PDA.

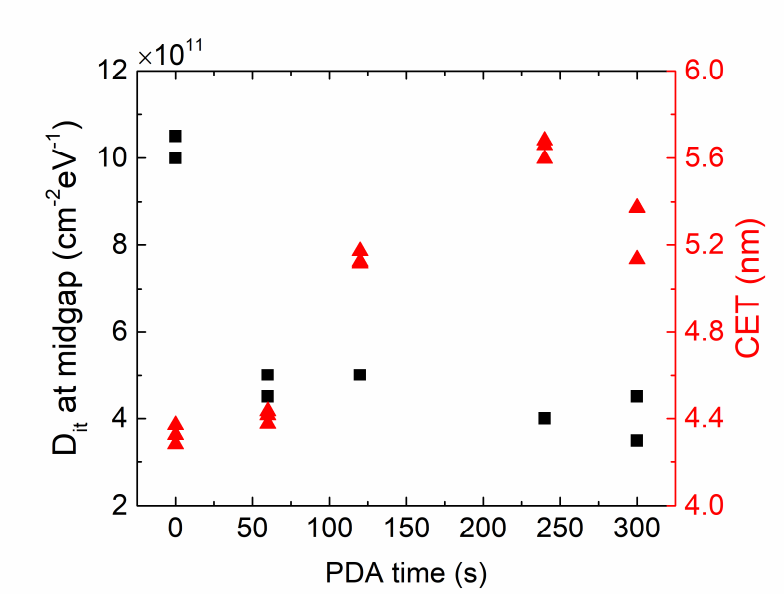

Figure 5. D_{it} in the midgap and CET values for $Ge/GeO_x/Tm_2O_3$ gate stacks after O_2 PDA at 500 °C for 0 – 5 min. D_{it} decreases already after 1 min while CET only starts increasing after 2 min.

Fixed charges in Ge/GeO_2 and $Ge/GeO_x/Tm_2O_3$ gates

Work function of Al electrode as well as fixed charge density N_f of Ge/GeO_2 gates were calculated from flatband voltage V_{FB} versus EOT plot which is displayed in Figure 6. The intercept is 0.11 V implying that Al work function is 4.34 eV which is in line with values calculated from $Si/SiO_2/Al$ MOS capacitors using the same method (8). Fixed charge extracted from the slope of the fitted line is ~$5 \cdot 10^{11}$ cm^{-2}, and the linear

shape of V_{FB} vs. EOT dependence suggests that the fixed charge is located at Ge/GeO_2 interface.

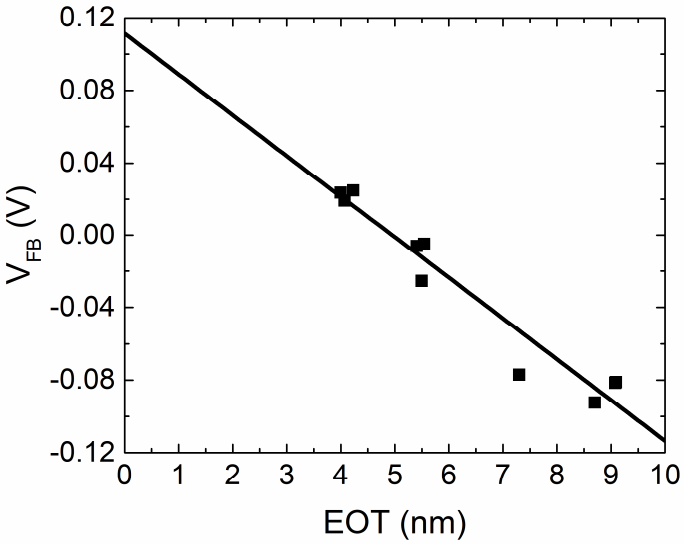

Figure 6. Flatband voltage V_{FB} vs. equivalent oxide thickness EOT of Ge/GeO_2 gate stacks with varying GeO_2 thickness. The amount of fixed charge density extracted from the slope of the linear fit is $\sim 5 \cdot 10^{11}$ cm^{-2}.

Fixed charge density in $Ge/GeO_x/Tm_2O_3$ gate stacks with and without O_2 PDA at 500 °C was calculated assuming the previously estimated Al work function. Positive fixed charge of $Ge/GeO_x/Tm_2O_3$ stack before PDA is $\sim 1 \cdot 10^{12}$ cm^{-2}, and increases to $\sim 2.5 \cdot 10^{12}$ cm^{-2} after O_2 anneal. Positive fixed charge could be associated with Ge^{3+} oxidation state since an oxygen vacancy in GeO_2 has been shown to be responsible for positive fixed charge near Ge/GeO_x interface (9). The shift of the CV curve due to increased fixed charge is displayed in Figure 7a.

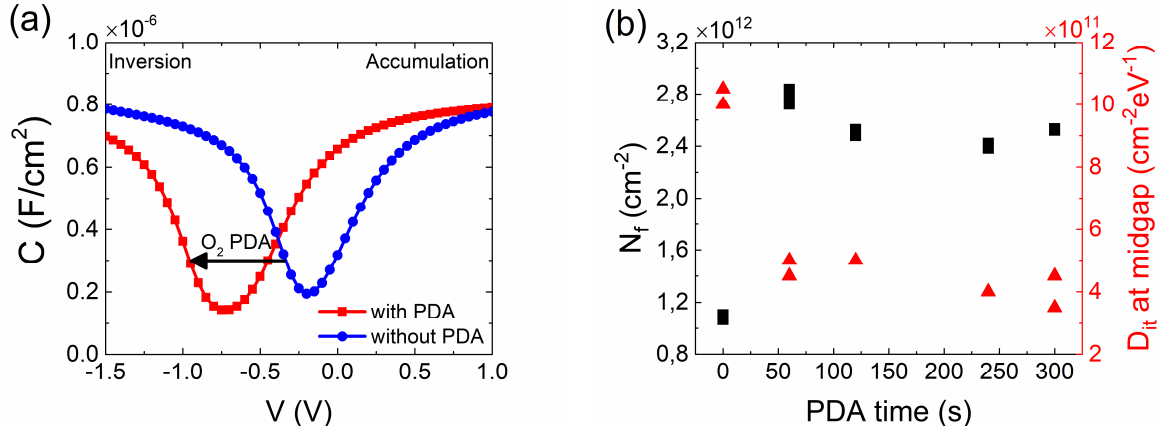

Figure 7. The influence of O_2 PDA at 500 °C on the fixed charge in $Ge/GeO_x/Tm_2O_3$ gate stacks: (a) CV characteristics before and after O_2 PDA for 1 min showing a shift to the left as the positive Q_f increases after PDA, (b) D_{it} decreases to $<5 \cdot 10^{11}$ $cm^{-2}eV^{-1}$ whereas Q_f increases to $\sim 2.5 \cdot 10^{12}$ cm^{-2} and does not significantly change for longer PDA.

Fixed charge reaches ~$2.5 \cdot 10^{12}$ cm^{-2} already after 1 min anneal (see Figure 7b) during which time D_{it} drops to $<5 \cdot 10^{11}$ $cm^{-2}eV^{-1}$. Longer PDA does not significantly influence the fixed charge density. The correlation between decreasing interface state density and increasing fixed charge density suggests that the defects that were caused by ALD might be responsible for both, and PDA changes the energy level of the defects which turns interface states into fixed oxide charge.

Conclusion

It has been shown that Tm_2O_3 layer deposition by ALD increases D_{it} in high quality Ge/GeO_2 interfaces ($D_{it} < 5 \cdot 10^{11}$ $cm^{-2}eV^{-1}$). While interface state density is increased at least two times in all $Ge/GeO_x/Tm_2O_3$ MOS capacitors with varying GeO_x thickness, this effect is much greater for the ones with thinnest GeO_x (< 3 nm) when D_{it} increases up to 5 times. Nevertheless, optimized annealing conditions (O_2 RTA at 500 °C for 1 min) can reverse this effect and provide $Ge/GeO_x/Tm_2O_3$ gate stacks with low interface state density in the midgap ($D_{it} < 5 \cdot 10^{11}$ $cm^{-2}eV^{-1}$) without increasing CET. While this PDA decreases D_{it}, it has an opposite effect on the amount of fixed oxide charge which is increased to ~$2.5 \cdot 10^{12}$ cm^{-2}. This result suggests that the defects introduced during ALD are responsible for both interface states and fixed oxide charge.

Acknowledgments

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References

1. H. Matsubara, T. Sasada, M. Takenaka, and S. Takagi, *Appl. Phys. Lett.*, **93**(3), 32104 (2008).
2. S. Ogawa, R. Asahara, Y. Minoura, H. Sako, N. Kawasaki, I. Yamada, T. Miyamoto, T. Hosoi, T. Shimura, and H. Watanabe, *J. Appl. Phys.*, **118**(23), 235704 (2015).
3. R. Zhang, J. Lin, X. Yu, M. Takenaka, and S. Takagi, *IEEE Trans. Electron Devices*, **61**(2), 416–422 (2014).
4. C. H. Lee, C. Lu, T. Tabata, W. F. Zhang, T. Nishimura, K. Nagashio, and A. Toriumi, *Tech. Dig. - Int. Electron Devices Meet. IEDM*, 40–43 (2013).
5. E. D. Litta, P.-E. Hellstrom, C. Henkel, S. Valerio, A. Hallen, and M. Ostling, *J. Electrochem. Soc.*, **160**(11), D538–D542 (2013).
6. I. Z. Mitrovic, S. Hall, M. Althobaiti, D. Hesp, V. R. Dhanak, A. Santoni, A. D. Weerakkody, N. Sedghi, P. R. Chalker, C. Henkel, E. Dentoni Litta, P.-E. Hellström, M. Östling, H. Tan, and S. Schamm-Chardon, *J. Appl. Phys.*, **117**(21), 214104 (2015).
7. L. Zurauskaite, P.-E. Hellström, and M. Östling, *2017 IEEE Electron Devices Technol. Manuf. Conf. Proc. Tech. Pap.*, 164–166 (2017).
8. W. M. Werner, *Solid State Electron.*, **17**(8), 769–775 (1974).
9. H.-C. Chang, S.-C. Lu, T.-P. Chou, C.-M. Lin, and C. W. Liu, *J. Appl. Phys.*, **111**(7), 076105 (2012).