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Research Article

Sub-15 nm Silicon Lines Fabrication via PS-*b*-PDMS Block Copolymer Lithography

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This paper describes the fabrication of nanodimensioned silicon structures on silicon wafers from thin films of a poly(styrene)-*block*-poly(dimethylsiloxane) (PS-*b*-PDMS) block copolymer (BCP) precursor self-assembling into cylindrical morphology in the bulk. The structure alignment of the PS-*b*-PDMS (33 k–17 k) was conditioned by applying solvent and solvothermal annealing techniques. BCP nanopatterns formed after the annealing process have been confirmed by scanning electron microscope (SEM) after removal of upper PDMS wetting layer by plasma etching. Silicon nanostructures were obtained by subsequent plasma etching to the underlying substrate by an anisotropic dry etching process. SEM images reveal the formation of silicon nanostructures, notably of sub-15 nm dimensions.

1. Introduction

Continuing miniaturisation of microelectronics and nanoelectronics devices strongly demands controlled high density nanodimensioned structures in wafer scale [1–4]. Feature size reduction is conventionally achieved following the usage of UV, e-beam, and X-ray lithographic processes, for obtaining sub-22 nm device structures [5]. These top-down methodologies of device fabrication are already well established in silicon industries for chip miniaturisation in large scale [6]. They utilize highly expensive light sources [7], while attainment of smaller length-scale features is getting increasingly challenging and time consuming due to the intrinsic serial nature of the top-down methodology [8]. Alternative intrinsically parallel methodologies based on bottom-up approaches that exploit block copolymer (BCP) self-assembly as nanostructure generator are becoming increasingly attractive among researchers [9]. The potential of such approaches is to generate predictable sub-10 nm structures at low costs [10, 11]. BCPs like polystyrene-*b*-polymethylmethacrylate (PS-*b*-PMMA), polystyrene-*b*-polylacticacid (PS-*b*-PLA), polystyrene-*b*-polydimethylsiloxane (PS-*b*-PDMS), and polystyrene-*b*-polyethyleneoxide (PS-*b*-PEO) of lamellar, cylindrical, or spherical morphology in combination with different strategies for control of substrate surface chemistry and pattern alignment have been used as precursors for nanolithographic masks [12, 13]. Many applications have been demonstrated for nanostructures made by these BCPs, for example, in the fields of magnetic, metal oxide, and metallic device fabrication [14]. However, challenges exist in getting highly packed device features [15] generated through BCPs.

Nanolithographic mask fabrication from BCPs often requires lamella or cylinder alignment perpendicular to the substrate, and this has been achieved by rendering the substrate surface energy neutral relative to the two blocks [16, 17]. Covalent anchoring of hydroxyl-terminated homopolymers or random copolymers onto substrate is one

Table 1: Details of synthesised polymer characteristics used for the present work.

Molecular weight, M_n, g/mol	Polydispersity, M_w/M_n	Molecular weight of PS, $M_{n(PS)}$, g/mol	Volume fraction of PS, f_{PS}	Description
50000	1.03	17000	0.64	PS-*b*-PDMS
11000	1.05	—	—	PS-OH

of the most effective techniques of surface modification for perpendicular alignment of BCPs [18]. It should be noted that the majority of the studies has been devoted to BCPs like PS-*b*-PMMA, PS-*b*-PLA, and PS-*b*-PEO. However, PS-*b*-PDMS is of particular interest due to its relatively large Flory-Huggins interaction parameter ($\chi \sim 0.26$), larger than the interaction parameters of the BCPs mentioned above [19, 20]. These BCPs allow for smaller minimum feature size dimensions that are certainly below the feature size realized by the established UV-lithography method [21–23]. The fabrication of sub-15 nm and possibly sub-10 nm feature size structures becomes possible by appropriate design of nanolithographic masks from PS-*b*-PDMS.

In this paper, we demonstrate the fabrication of sub-15 nm silicon nanowires from a synthesized PS-*b*-PDMS (33 k–17 k) of total molecular weight of 50 kg/mol and a hydroxyl terminated PS brush. Device structures are formed using plasma dry etching where BCP patterns act as a mask and are transferred into the underlying substrate. It should be noted that PS-*b*-PDMS self-assembly results in the formation of sandwich structures with wetting PDMS layers at the substrate-polymer and polymer-air atmospheres [24]. This involves a prior selective etch process of an upper PDMS layer followed by silicon etch.

2. Materials and Methods

2.1. Materials. Silicon ⟨100⟩ wafers (p-type) were used with a native oxide layer ~2 nm. A hydroxyl-terminated polystyrene, denoted as PS-OH brush, and a block copolymer poly(styrene)-*block*-poly(dimethylsiloxane) (PS-*b*-PDMS) were synthesised in our own lab by "living" anionic polymerisation [25, 26]. Detailed characteristics of the polymers are summarized in Table 1. Toluene (99.8%) was purchased from Sigma-Aldrich and used without further purification. Deionised (DI) water was used wherever it was essential.

2.2. Preparation of PS-OH Brush Anchored Substrates. Substrates were cleaned in SPTS inductively coupled plasma (ICP) etch tool by an oxygen plasma of flow rate 30 sccm for 180 s at 2.0 Pa with 1500 W and 200 W of ICP and reactive-ion-etch (RIE) power. This effectively removes organic contaminants from the substrates. Hydroxyl-terminated PS solution of 1.0 wt% in toluene was spin-coated onto silicon substrates at 3200 rpm for 30 s. Samples were baked at 443 K s for 4 h, which resulted in the formation of a polymer brush anchored onto substrates due to condensation reaction between hydroxyl groups of PS-OH and of silicon native oxide layer.

2.3. PS-b-PDMS Deposition on Brush Anchored Substrates. PS-*b*-PDMS solution of 1.0 wt% in toluene was spin-coated on silicon substrates modified with the PS-OH brush at 3200 rpm for 30 s. The substrates covered with BCP thin film on top of the brush layer were then solvent-annealed in a glass jar under saturated toluene environment at 298 K or at 323 K for four different annealing times (varied from 3 h to 12 h). Samples were removed from oven immediately after annealing and allowed to dry at ambient conditions.

2.4. Dry Plasma Etching of BCP Thin Films. After solvothermal annealing PS-*b*-PDMS films were subjected to removal of upper PDMS layer (and partial removal of PS matrix) using CF_4 and O_2 plasma with 15 sccm and 30 sccm for 15 s with ICP and RIE powers of 1200 W and 30 W at 1.6 Pa pressure. The oxidised PDMS cylinders act as hard mask for subsequent silicon etching by SF_6 and C_4F_8 plasma at 70 sccm and 35 sccm flow rate with ICP and RIE powers of 1200 W and 200 W at 1.9 Pa pressure.

2.5. Scanning Electron Microscopy (SEM). Top-down and cross-sectional SEM images of polymer mask templates and silicon nanostructures were obtained by using a high resolution field emission Zeiss Ultra Plus SEM with a Gemini column operating at an accelerated voltage of 3 keV.

3. Results and Discussion

The PS-*b*-PDMS BCP used in the study possesses a total molecular weight of 50 kg mol^{-1} and a PS volume fraction of 64% and shows a thermodynamic equilibrium structure of cylindrical PDMS domains in a PS matrix. BCP self-assembly of PS-*b*-PDMS (33 k–17 k) was achieved by techniques of solvent annealing and solvothermal annealing in saturated toluene environment at 298 K and 323 K with varying anneal time. Figures 1(a)–1(h) show top-down SEM images of PS-*b*-PDMS patterns after solvent annealing at 298 K and solvothermal annealing at 323 K for a set of four different timings (3 h–12 h).

The upper PDMS layer formed during self-assembly has been removed by using CF_4 and O_2 plasma for 15 s after which the nanopatterns became clearly visible in the SEM images (Figures 1(a)–1(h)). A schematic illustration of the workflow for the nanostructuring process is shown in Scheme 1.

Figures 1(a)–1(d) show top-down SEM images after etching of the upper PDMS wetting layer of solvothermal annealed samples at 298 K for 3 h, 6 h, 9 h, and 12 h, respectively, while Figures 1(e)–1(h) show images of similar samples after solvothermal annealing at 323 K for 3 h, 6 h, 9 h, and 12 h, respectively. It is clearly seen from Figure 1 that the sample annealed at 323 K for 3 h gives (Figure 1(e))

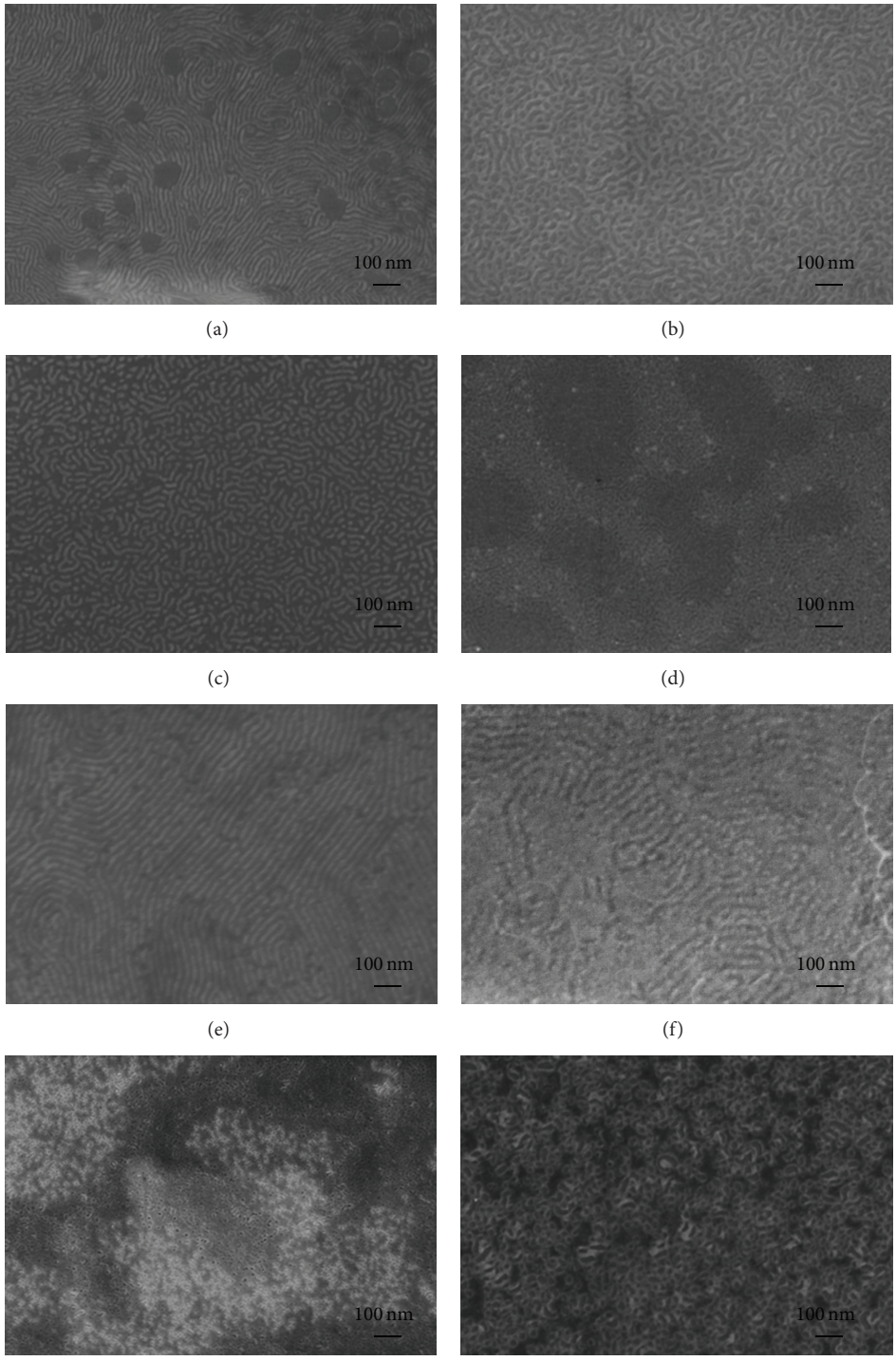
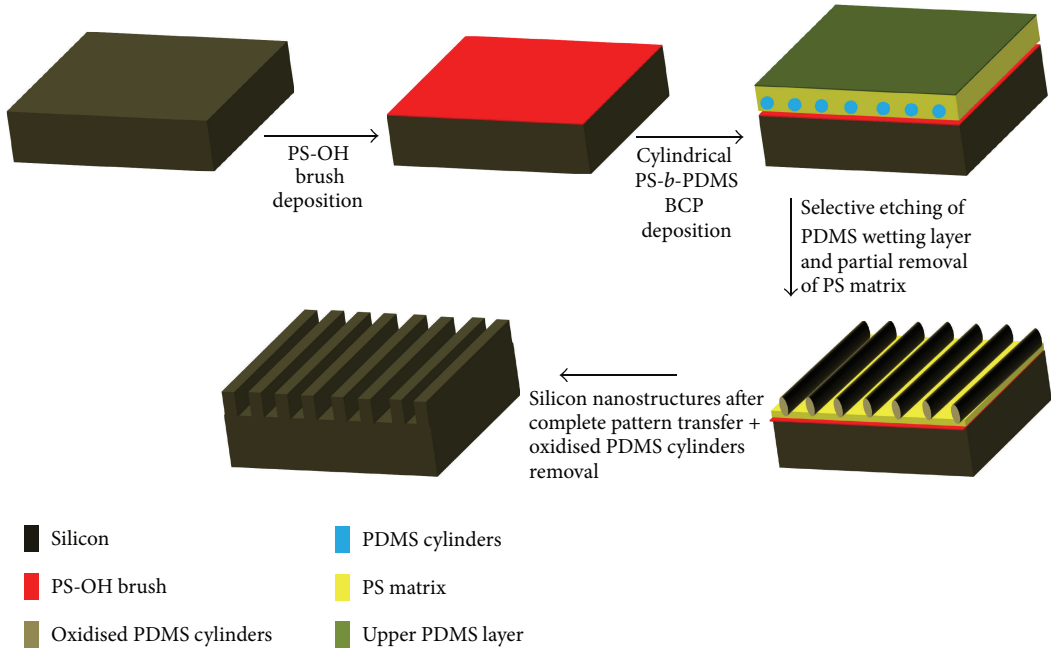


FIGURE 1: Top-down SEM images of self-assembled PS-*b*-PDMS on top of PS-OH anchored silicon substrates after treatment with $CF_4 + O_2$ plasma. The plasma removes upper PDMS wetting layer and part of the PS matrix. All samples were annealed under toluene environment: (a) at 298 K for 3 h; (b) at 298 K for 6 h; (c) at 298 K for 9 h; (d) at 298 K for 12 h; (e) at 323 K for 3 h; (f) at 323 K for 6 h; (g) at 323 K for 9 h; and (h) at 323 K for 12 h.

the best alignment of cylinders horizontal to the substrate. The mean PDMS cylinder spacing, L_0, and line width, $\langle d \rangle$, were about 31 nm and 15 nm.

Among the tested annealing conditions it seems evident that the annealing for 3 h at 323 K produces best results in terms of cylindrical structure alignment and persistence



Scheme 1: Schematic of BCP self-assembly on top of PS-OH brush layer anchored on the surface of silicon substrates and subsequent plasma etching for silicon nanostructures fabrication [18].

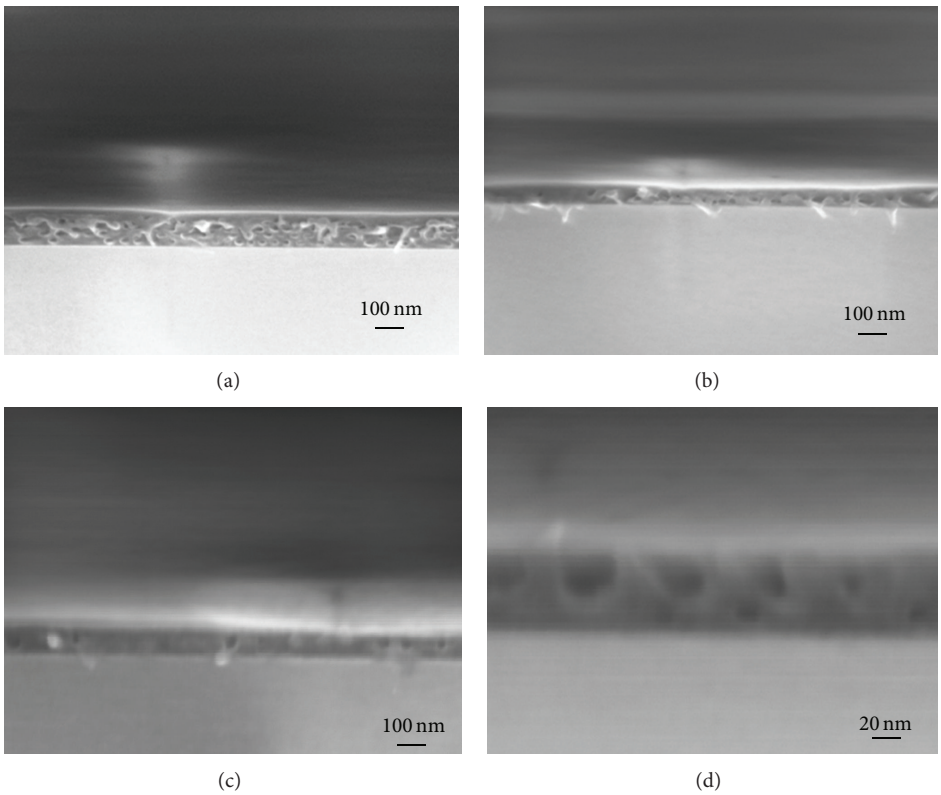


Figure 2: Cross-sectional SEM images of cylindrical structure of PS-*b*-PDMS after solvothermal annealing at 323 k for 3 h. No prior PDMS etch was done and most probably the thin top layer is the expected low surface energy PDMS wetting layer. (a) Multilayer, (b) bilayer, and (c) monolayer regions of PS-*b*-PDMS patterns. (d) High resolution cross-sectional image of cylindrical structures.

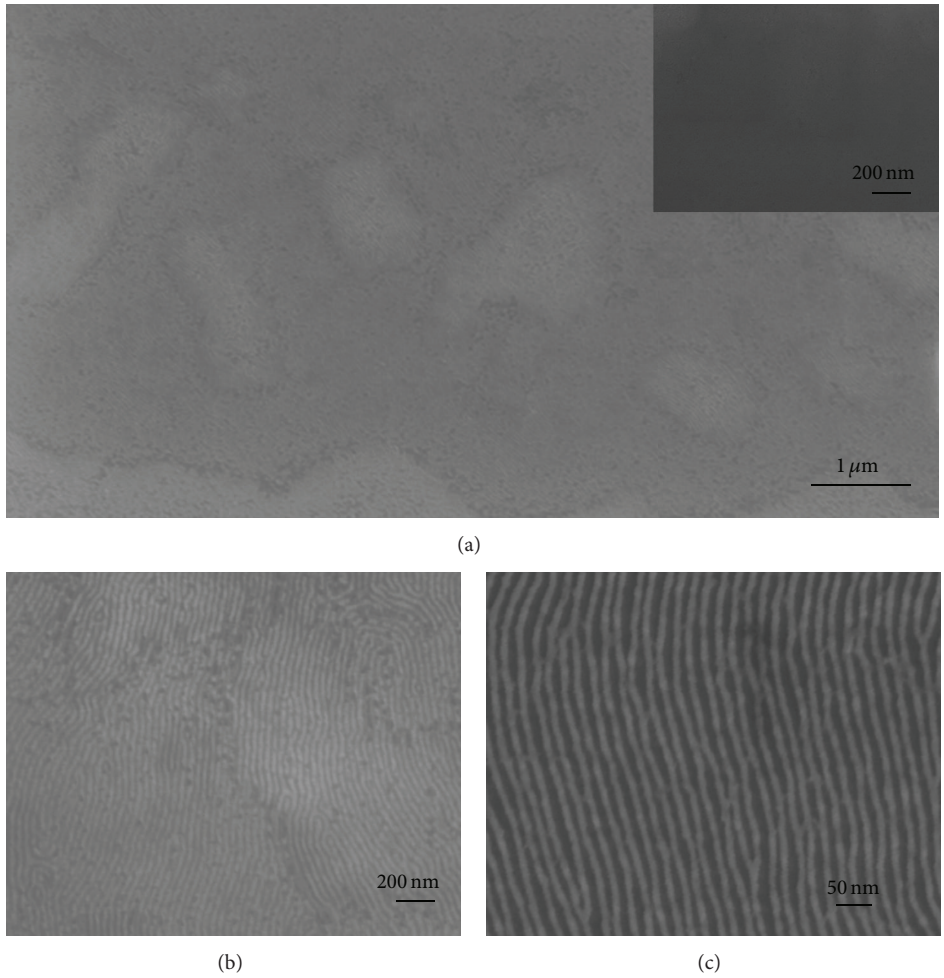


Figure 3: Top-down SEM images of PS-*b*-PDMS on 4″ wafer. (a) Top-down SEM image of PS-*b*-PDMS after PDMS removal; inset shows PS-*b*-PDMS before removal of upper PDMS with no nanopattern visible. (b) Low resolution and (c) high resolution images of oxidised PDMS cylinders.

length. Annealing times above 6 h at 323 K favour short range structures and micelle formation, as seen in Figures 1(f)–1(h).

PS-*b*-PDMS samples prepared at 323 K and 3 h solvothemal annealing were studied in more details. In order to get a better understanding of the cylindrical morphology of PS-*b*-PDMS, cross-sectional SEM images prior to any PDMS removal were taken as shown in Figure 2. Dewetting is one of the major issues in high χ BCP systems such as PS-*b*-PDMS, and this leads to multilayer formation in different regions upon solvothermal annealing process. Multilayer regions are clearly seen by cross-sectional SEM images (Figures 2(a)-2(b)). Figure 2(a) shows the multilayer formation of PDMS cylinders in PS matrix horizontal to the planar substrates with a thin upper PDMS layer. However, most of the areas were covered with monolayer of PDMS cylinders shown in SEM images of Figure 2(c). A good pattern transfer to the underlying silicon substrate is expected on the monolayer regions. The wafer scale production of device structures using PS-*b*-PDMS (33 k–17 k) was examined on a 4-inch wafer. A 4-inch wafer cleaned with oxygen plasma was spin-coated firstly with PS-OH and baked and secondly with PS-*b*-PDMS and annealed at 323 K for 3 h in toluene environment. After the removal of the upper PDMS layer large area coverage of BCP patterns could be observed under SEM as shown in Figure 3(a) with minor dewetting. The PDMS cylinders get oxidised while removing upper PDMS layer by CF_4 and O_2 plasma, which results into a strong mask for a good pattern transfer to the silicon substrate.

Low resolution and high resolution images of oxidised PDMS cylinders are seen in Figures 3(b) and 3(c). The feature size of cylinders was ~13 nm in the shown projection. The film regions nanopatterned by the oxidised PDMS threads were used as mask for pattern transfer in the silicon substrate. Silicon nanostructures were fabricated after a silicon etch of 15 s and 20 s using CF_4 and SF_6, respectively, with ICP and RIE powers of 600 W and 40 W under 1.2 Pa chamber pressure. Later the substrates were sonicated in 40% HF for 5 min to remove oxidised PDMS cylinders and the results are shown in Figures 4(a) and 4(b). Silicon nanostructures were regular with feature size of about 12–15 nm for 15 s Si etch

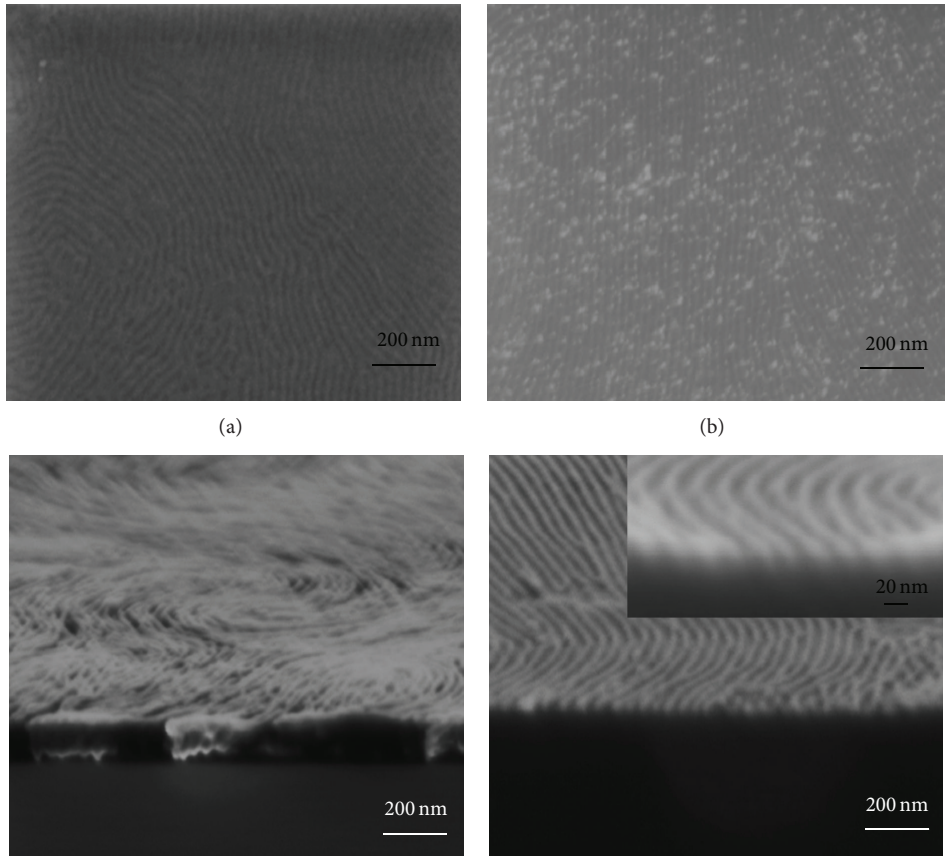


Figure 4: SEM images of silicon nanostructures. (a) Silicon nanowires after 15 s silicon etch. (b) Silicon nanostructures after 20 s silicon etch. (c) No pattern transfer in bilayer and multilayer regions. (d) Complete pattern transfer in monolayer regions of PS-*b*-PDMS template. Inset (d) shows the high resolution image of nanowires.

(Figure 4(a)), whereas at 20 s etch time silicon structures were partially destroyed as shown in the top-down SEM image of Figure 4(b). There was no successful pattern transfer to the underlying silicon at the regions covered by multilayers as seen in the image of Figure 4(c). The multilayer structure prevents the plasma to strike down to the silicon substrate due to misalignment of PDMS cylinders in the different layers. It is clear from Figure 4(d) that there was an isotropic silicon etch resultant into the formation of silicon nanowires; the inset shows the high resolution SEM image of transferred nanostructures.

The minimum exposure of BCP film under toluene environment has a very little swelling or deformation of BCP patterns for shorter annealing time for 3 h at 323 K. The orientation and coherence length of the film are also affected by the exposure time to toluene vapours. The silicon wires fabricated by this synthesised PS-*b*-PDMS block copolymer lie in the region of sub-15 nm. Although the results shown in this paper are similar to the literature reports (with respect to etch and feature size of wires), no literature has yet shown the self-assembly and subsequent pattern transfer of an in-lab synthesised PS-*b*-PDMS. This indicates a gateway for very low cost production of device structures for microelectronics industries.

4. Conclusions

We have presented a qualitative and quantitative analysis of a solvent and solvothermal process for the fabrication of nanolithographic masks from PS-*b*-PDMS BCP of cylindrical morphology. The BCP was spin-casted on silicon wafer substrates surface modified by grafting of a PS-OH brush layer. The solvothermal annealing process was applied at two temperatures and four annealing times for each temperature. The conditions that produced line patterns with highest correlation length were 3 h annealing at 323 K. The method showed a promising BCP self-assembly on planar silicon substrate. It must be notified that the obtained results on the thin film self-assembly of the synthesised PS-*b*-PDMS (33 k–17 k) were similar with the literature reports. Nanopattern transfer to underlying silicon substrates in the form of sub-15 nm wires for nanodevice fabrication via BCP self-assembly was demonstrated.

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