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All-optical 10 Gb/s AND logic gate in a silicon microring resonator

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Abstract: An all-optical AND logic gate in a single silicon microring resonator is experimentally demonstrated at 10 Gb/s with 50% RZ-OOK signals. By setting the wavelengths of two intensity-modulated input pumps on the resonances of the microring resonator, field-enhanced four-wave mixing with a total input power of only 8.5 dBm takes place in the ring, resulting in the generation of an idler whose intensity follows the logic operation between the pumps. Clear and open eye diagrams with a bit-error-ratio below 10^{-9} are achieved.

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1. Introduction

All-optical signal processing is recognized as a key approach to break the speed limitations of electronics in future high capacity and ultrafast communication networks [1,2]. As important basic functions for signal processing techniques, all-optical logic gates have potential applications for bit-error monitoring [3], address and payload separation [4], switching triode [5] etc. Nonlinear effects in semiconductor optical amplifiers (SOAs) [6,7], highly nonlinear silica fibers (HNLFs) [8,9] and periodically-poled lithium niobate (PPLN) waveguides [10,11] have been intensely investigated to realize different logic gate functions. 10 Gb/s and

40 Gb/s logic gates based on four-wave mixing (FWM) in SOAs [12] and HNLFs [9], respectively, have been demonstrated with relatively complex configurations. However, the slow recovery time of carriers in SOAs results in pattern effects and thus limits high speed operation. Long interaction lengths and high input powers are needed for HNLFs to generate sufficiently strong nonlinear effects. The requirements for precise temperature control in PPLN waveguides make them less attractive for practical use.

Silicon-based devices, well known for their compact sizes, make monolithic integration for multi-functional components possible. All-optical signal processing based on strong nonlinearities induced by the high Kerr index and the small effective areas [13,14] of silicon-on-insulator (SOI) waveguides has been widely studied in the last decade. Functionalities such as parametric amplification [13,14], wavelength conversion [15,16], signal regeneration [17,18] and modulation format conversion [19] have been successfully demonstrated. Recently, all-optical logic gates based on two-photon absorption (TPA) [20], free-carrier effects [21] and FWM [22] in silicon nanowires have been reported. To decrease the power consumption, a cavity resonator such as a microring resonator (MRR) is often adopted. However, logic gates based on free carrier dispersion without any active carrier sweeping method [23] or on the thermo-optic effect [24] in silicon MRRs are limited to low operation speeds (2~310 Mb/s). Other materials, such as III-V semiconductors, also present a high Kerr nonlinearity and, in some cases (e.g. InGaP or AlGaAs) are free from TPA at telecommunication wavelengths around 1550 nm. They could therefore constitute a promising platform for the demonstration of all-optical logic based on FWM. Nevertheless, silicon-based devices have the advantage of compatibility with conventional microelectronics fabrication processes and benefit from a highly mature fabrication technology. AND logic gates at 40 Gb/s [25] and 160 Gb/s [26] based on enhanced FWM in passive InGaAsP/InP MRRs have been proposed. However, the results have been obtained through simulations based on a theoretical analysis with, to the best of our knowledge, no experimental demonstration reported to date. Alternatively, the generation of free-carriers induced by TPA can also be used to switch the resonance frequencies of an MRR and perform optical logic. This approach has been followed in [27], where 30 Gb/s AND/NAND logic gates have been demonstrated in GaAs MRRs. The scheme is however limited by the carrier lifetime and no full system penalty measurements have been reported in [27].

In this paper, we demonstrate all-optical AND logic gate operation between two 50% return-to-zero on-off keying (RZ-OOK) signals at 10 Gb/s. The scheme relies on field-enhanced FWM in a silicon MRR with a Q-factor of 12000 and a free spectral range (FSR) of 1.73 nm. Clear eye diagrams after the logic operation and small power penalty are achieved with only 5.5 dBm input power for each pump. As a comparison, we also analyze the logic performance of a silicon straight waveguide (WG) with same length as the bus of the MRR. Compared with the WG, 3 dB larger FWM conversion efficiency and 1 dB smaller power penalty can be experimentally achieved in the MRR.

2. Operation principle

Figure 1 shows the principle of an AND logic gate based on enhanced FWM in an MRR. Two RZ-OOK signals with center wavelengths centered on adjacent resonances of the MRR, i.e. λ_1 and λ_2, are launched into the ring. FWM between these data streams generates two idlers at λ_{i1} and λ_{i2}, as shown in Figs. 1(a)-1(c). Provided the effect of the dispersion of the waveguide in the ring can be neglected over the frequency range where signals and idlers are present, the idlers will coincide with MRR resonances on each side of the input signals Thus the signals and idlers all benefit from field enhancement in the ring cavity [28]. The intensity of each generated idler is proportional to the product of the intensity of the farther RZ-OOK signal and the square of the intensity of the closer RZ-OOK signal Therefore, since binary OOK modulation is used for the signals, the idler will carry the logic "1" state if both input data simultaneously have the logic "1" state, and the logic "0" state if at least one of the signals

carries the logic "0" state, which corresponds to the logic AND operation whose truth table is illustrated in Fig. 1(d). It has to be noted that the fact that the signal carrying the result of the logic operation is at a different wavelength than that of the input signals introduces some constraint on the potential use of the scheme for cascaded logic operation. However, this limitation is shared by many of the physical processes used to demonstrate all-optical logic so-far.
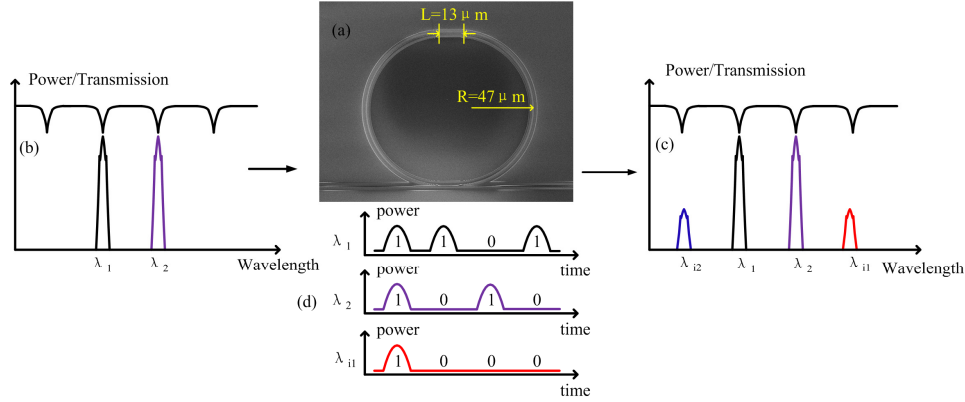

Fig. 1. Principle of the AND logic gate. (a) Scanning electron microscope (SEM) picture of the top view of the MRR. (b) Spectra of the input RZ-OOK signals and transmission function of the MRR. (c) Spectra of the output RZ-OOK signals along with the converted AND idlers. (d) Truth table of the AND logic gate.

3. Device fabrication

As shown in Fig. 1(a), a racetrack all-pass MRR with a radius of 47 μm and a bus waveguide 3.5 mm long was fabricated on a SOI wafer with top silicon thickness of 250 nm and buried silica of 3 μm. The width and height of both straight and ring waveguides are 540 nm and 250 nm, respectively, which results in a predicted dispersion value of −3 ps^2/m for the TE mode around 1550 nm, as numerically calculated by a full-vectorial finite-difference mode solver. MRRs with smaller radii have lower power requirements due to their smaller mode volumes, which however also make the free carriers build up faster and hence result in increased nonlinear loss and a lower conversion efficiency (CE) [29]. High Q-factor (small coupling coefficient) MRRs enable the demonstration of FWM with ultra-low pump energies, but meanwhile suffer from narrow bandwidths which limit the data rate at which optical signal processing is achievable [28]. In order to make the MRR applicable for signal processing at a bit rate of 10 Gb/s, a field coupling coefficient from the straight waveguide to the ring around 0.6 (corresponding to a bandwidth of about 25 GHz, which is sufficient for 10 Gb/s use) is preferred. The Q-factor of the MRR is around 12000 with this coupling coefficient, which is high enough to generate obvious field enhancement [28]. Using the 3-D full vectorial film mode matching method (FMM) and coupled mode theory (CMT) [30], the required coupling length and gap between the ring and the bus waveguide were consequently designed as 13 μm and 90 nm, respectively.

To compare the FWM conversion efficiency and logic gate performance, a straight waveguide with the same length as the bus of the MRR, i.e. 3.5 mm, was chosen. The MRR and WG were fabricated using electron-beam lithography followed by inductively-coupled plasma reactive ion etching. A silicon nano-taper covered by a layer of polymer (SU8-2005) waveguide was adopted to decrease the coupling loss between the device and tapered optical fibers [31,32]. The transmission spectrum of the MRR will be shown in the next section.

4. Experimental results and discussion

The experimental setup for AND logic gate demonstration based on FWM in the silicon MRR is shown in Fig. 2. Continuous waves (CW) centered on two adjacent resonances of the MRR, i.e. at 1550.97 nm and 1552.70 nm, were generated from two distributed feedback (DFB) lasers. The CW lights were combined in a 3 dB polarization maintaining coupler and modulated in a single Mach-Zehnder modulator (MZM) pulse carver driven by a 10 GHz radio frequency clock followed by another MZM driven with a 10 Gb/s pseudo-random pattern originating from a bit-pattern generator (BPG), resulting in the generation of two 50% RZ-OOK signals at 10 Gb/s with pseudo-random bit sequence (PRBS) length of 2^7-1. Two erbium-doped fiber amplifiers (EDFA) were used between and after the MZMs, respectively, to compensate their insertion loss. The two RZ-OOK data streams were then duplicated by a 3 dB coupler and selected according to their wavelength by 0.3 nm and 0.5 nm bandpass filters (BPF), respectively. One of the data streams was delayed with respect to the other using an optical delay line. Each RZ-OOK signal was amplified by an EDFA followed by a narrow band filter to suppress out-of-band amplified spontaneous emission (ASE) noise. Before being injected into the MRR, the two signals were combined again in a 3 dB coupler and their states of polarization were aligned to the TE mode of the waveguide with a polarizer (Pol.) placed between two polarization controllers (PCs). The average power of each signal in the MRR was 5.5 dBm. After the MRR, one of the two idlers carrying the AND logic result between the input RZ-OOK signals was filtered out using a 3 nm BPF, amplified in an EDFA, and detected in a pre-amplified receiver. The conversion efficiency of the idler was analyzed using an optical spectrum analyzer (OSA), and its quality was evaluated using a 70 GHz sampling oscilloscope and an error analyzer (EA). The AND logic performance of the straight waveguide with the same length as the bus of the MRR was also evaluated using the same experimental set-up.
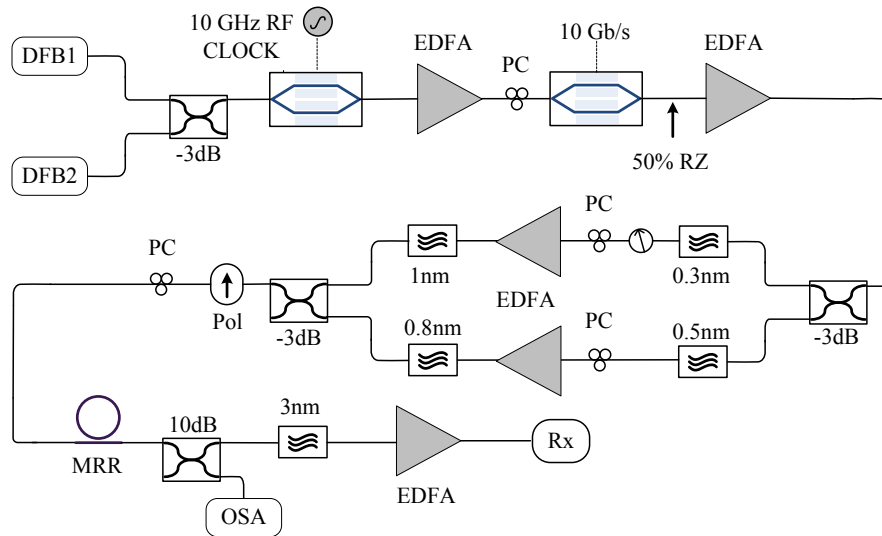

Fig. 2. Experimental setup for AND logic gate demonstration.

Figure 3(a) shows the measured transmission spectrum of the MRR. The total fiber-to-fiber insertion loss of both MRR and WG is 6 dB. The FSR and extinction ratio (ER) of the MRR are 1.73 nm and 1.2 dB, respectively, corresponding to a field coupling coefficient of 0.58 and a Q-factor of 12000. The propagation loss of the WG is 2.6 dB/cm. The bandwidth of the MRR, defined as the full-width of the resonance at the average value between the maximum and minimum of the transmission function, is 25 GHz, as shown in the inset of Fig. 3(a). Figures 3(b)-3(d) show the spectra of the signals launched into and received from the

MRR and WG. Very weak idler light can be seen at the input of the device, as shown in Fig. 3(b). This is due to incomplete suppression of the non-desired signal by the 0.3 nm (respectively 0.5 nm) BPF, followed by FWM in the following EDFA. Fortunately, those idlers generated before the MRR (WG) are not strong enough to affect the AND logic results. Replacing the BPFs with e.g. an arrayed waveguide grating demultiplexer (AWG) with steep transfer function edges could separate the two RZ-OOK signals completely, and thus prevent FWM from occurring in the EDFA. Figures 3(c) and 3(d) present the output spectra of the RZ-OOK signals as well as the converted AND idlers generated at 1549.25 nm and 1554.44 nm in the MRR and WG, respectively, showing conversion efficiencies of −34 dB and −37 dB, respectively. Thanks to the field enhancement in the resonant cavity of the MRR, a 3 dB improvement of the conversion efficiency is achieved compared to the WG. Higher absolute values of the conversion efficiency could be obtained using active removal of carriers as demonstrated in [33,34].
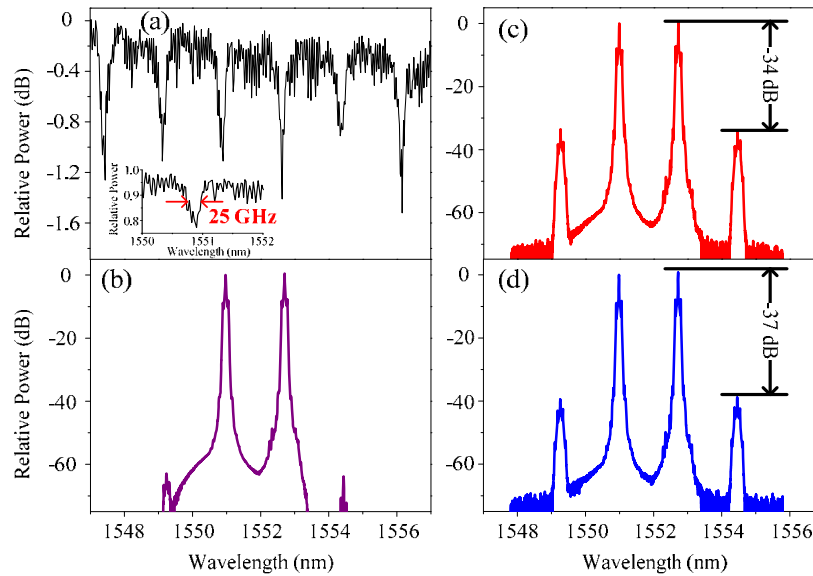

Fig. 3. (a) Transmission function of the MRR; inset: detail around the MRR resonance coinciding with one of the signals (represented using a linear scale). Measured spectra of (b) the two input RZ-OOK signals, (c) the output from the MRR, and (d) the output from the WG. The resolution bandwidth is 0.01 nm for all spectra.

Figures 4(a)-4(d) show the temporal pulse traces of the two input RZ-OOK signals along with the converted idlers obtained from the MRR and the WG. Note that both idlers generated by FWM carry the AND logic results of the input OOK signals. The idler at 1554.44 nm was selected in our experiment. The corresponding eye diagrams are shown in Figs. 4(e)-4(h). The recorded pulse sequences and the clear and open eye diagrams of the idlers validate the AND logic operation of the scheme. It is observed that the pulse width of the output logic signal is narrower than that of the input 50% RZ-OOK signals, especially in the case of the idler generated from the WG. This is partly due to the fact that the recorded idler power is proportional to the product of the square of the power of the signal at λ_2 by the power of the signal at λ_1, hence to $P^3(t)$, where $P(t)$ is the pulse shape of the signals, when a pulse is created in the idler. For 50% RZ-OOK signals, this effect reduces the duty cycle of the idler pulse to 36%. It should be noted that, when a sequence of consecutive "1" is obtained from the MRR, the intensity of the latter pulse is higher than that of the former one. This is because part of the previous pulse is still circulating in the MRR, which helps enhancing the FWM, when the next pulse is injected.
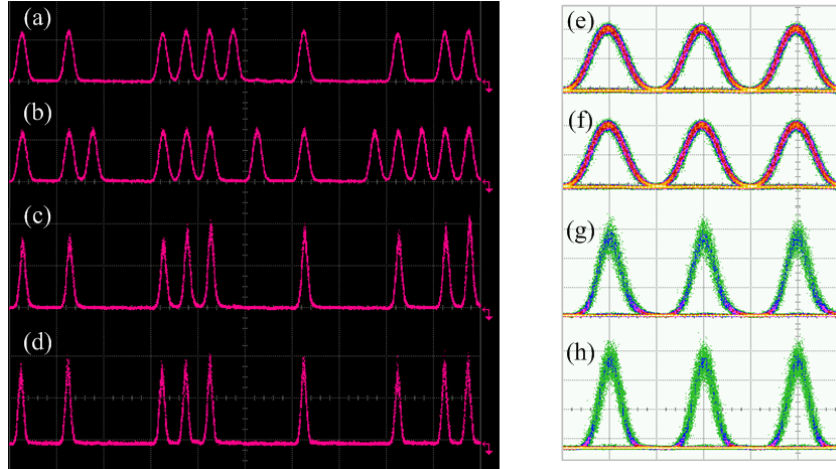
Fig. 4. Pulse traces of (a) input RZ-OOK signal at 1550.97 nm, (b) input RZ-OOK signal at 1552.70 nm, (c) AND logic output idler from the MRR at 1554.44 nm, (d) AND logic output idler from the WG at 1554.44 nm, and their corresponding eye diagrams (e)-(h).

Figure 5 shows the results of BER measurements for the implementations of AND logic gates using the MRR and the WG. It can be seen that error-free performances are obtained for both MRR and WG (the widely accepted definition of error-free, corresponding to BER values below 10^{-9} with no forward error correction (FEC) is adopted here). Due to the fact that, for the logic AND signal, the "1" to "0" ratio (25%) and the pulse duty cycle (36%) are smaller than in the original PRBS signal, little power penalty is measured for the idler generated from the MRR, relatively to back-to-back operation. Since the FWM conversion efficiency in the WG is 3 dB lower than that in the MRR, 1 dB power penalty can be seen for the AND idler generated in the WG.
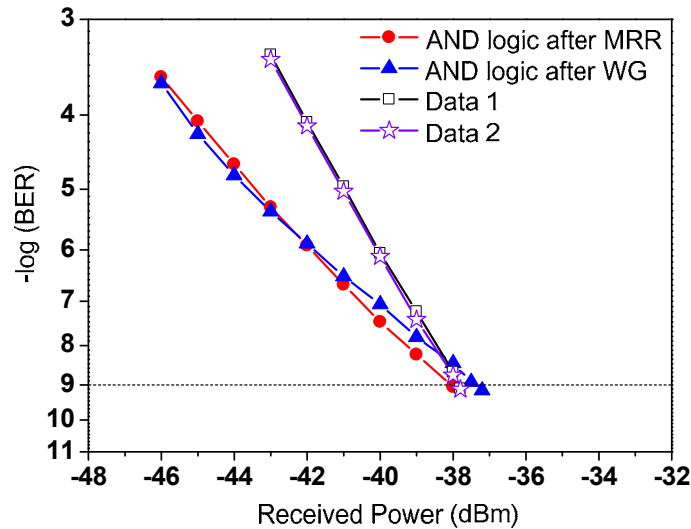

Fig. 5. BER measurements for the input RZ-OOK signal at 1550.97 nm (black) and at 1552.70 nm (purple), as well as for the AND logic idler generated in the MRR (red) and WG (blue) at 1554.44 nm.

An AND logic gate based on FWM in an SOA has been demonstrated with RZ signals at 10 Gb/s in [12]. The reported conversion efficiency was −16 dB and the scheme presented

regenerative characteristics with a power penalty of −2 dB, which shows better performance than our work. This is because the signals and logic idler benefit from amplification in the SOA, which is a more complex and costly active component compared to a silicon MRR. Furthermore the scheme may not be arbitrarily scalable to higher bit rates, as is the case for a scheme relying on the ultra-fast Kerr nonlinearity. AND logic at 30 Gb/s has been demonstrated based on TPA and free-carrier absorption (FCA) in an InP MRR [27]. The operation speed was higher than that in our work, but the scalability to higher bit rates also depends on the carrier lifetime in this scheme. Based on FWM in an HNLF, an AND logic gate operating between two 10 Gb/s polarization-shift keying (PolSK) signals has been reported with nearly 3 dB power penalty and a total average power of about 15.2 dBm [35]. However, the employed modulation format is notoriously difficult to detect in practical optical fiber links.

Compared with the WG, the field enhancement effect introduced by the MRR also gives rise to higher TPA and TPA-induced FCA in the ring. The enhanced nonlinear losses may limit the conversion efficiency improvement in our experiment. However, with lower input power, the superiority of the MRR compared to the WG can be much more significant with respect to the FWM conversion efficiency [29]. Higher bit rate operation could be achieved in MRRs by utilizing coupled resonator optical waveguide (CROW) devices to broaden the device bandwidth [36].

5. Conclusion

We have demonstrated an AND logic gate operating with two RZ-OOK data streams at 10 Gb/s in a silicon microring resonator with an FSR of 1.73 nm and a Q-factor of 12000. Good logic performance with clear eye diagrams and operation at a BER better than 10^{-9} have been obtained. The MRR has been shown to result in 3 dB enhanced conversion efficiency compared to a straight waveguide of the same length as the bus waveguide.

Acknowledgments