DC-DC Interleaved Boost Converter using FPGA

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Abstract— This paper presents the design of dc to dc Interleaved Boost Converter (IBC) which is controlled using Field Programmable Gate Array (FPGA). The output voltage can be controlled by Pulse Width Modulation (PWM) switching technique which is implemented on the Altera DE2-70 Board. An eight bit Analog to Digital Converter circuit is used to monitor the output current. The simulation is carried out using Matlab Simulink software and simulation on the designed waveform is conducted using Quartus II software tools. The frequency of the PWM output voltage is set to 40 kHz. Various detailed analysis has been done to investigate the benefits of IBC compared to conventional boost converter. Meanwhile, theoretical analysis and hardware prototype has been done to validate the result.

Index Terms— Pulse Width Modulation (PWM), Interleaved Boost Converter (IBC).

I. INTRODUCTION

In general, this paper presents a design of IBC for renewable energy application. The converter is used in various range of application such as renewable energy, communication and electric drives. The hardware consists of Altera DE2-70 board, ADC 0804 circuit and driver circuit. The IBC is designed to boost from 12 volt to 24 volt output. In this system, Altera DE2-70 board is used as a controller. PWM switching signal is designed using Quartus II software. Insulated Gate Bipolar Transistor (IGBT) is used as a switch power in the IBC circuit because it has several advantages such as high switching frequency and high current handling capability. It also combines in it all the advantages of the bipolar and MOS field effect transistor (MOSFET). In addition, interleaving provides high power capability, modularity and improved reliability [1]. With simple and handy design, the IBC is very suitable for EV application due to its increase in efficiency, improving electric performance, reduction in size, and has greater reliability [2]. It has high voltage step up, reducing voltage ripple at the output, low switching loss, reduces electromagnetic interference and also faster transient response [3,5].

II. LITERATURE REVIEW

Altera DE2-70 board used Development and Education board is a modified version of the DE2-70 board with a larger FPGA and more memory. It is an excellent medium for learning about digital logic, computer organization, and FPGAs. Featuring an Altera Cyclone II 2C70 FPGA, the

Altera DE2-70 board is designed for university and college laboratory use. User can program using various types of programming language through Quartus II software. Analysis and synthesis of HDL designs which enables the developer to compile their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer. Driver circuit is used to step up the input voltage from 3.3volt to 15volt in order to trigger the IGBTs. The driver circuit is designed to operate in high switching frequency up to 100kHz.

The IGBT is a three-terminal power semiconductor device primarily used as an electronic switch. In newer devices, it is noted for combining high efficiency and fast switching. It switches electric power in many modern appliances: electric cars, trains, variable speed refrigerators, air-conditioners and even stereo systems with switching amplifiers. In this project, the IGBTs is chosen as the switching device. This is because the IGBT has several advantages such as low duty cycle, low frequency which is less than 20kHz, narrow or small line or load variations as well as has high-voltage applications which is greater than 1000Volt compared to other switching devices [2]. Presently, some of the newest IGBTs can offer competitive performance which can operate at 100 kHz and above.

The IBC system developed involves several elements which are PWM technique from Altera DE2-70 and driver circuit. It consists of a number of boost converters that are connected in parallel and controlled by interleaved method which has the same frequency and phase shift [4]. The components used in IBC are IGBT module, power diode, inductor and capacitor. The capacitor is used as a filter to reduce the output voltage ripple in IBC. The activation allows the IBC to function and has produced the desired output voltage. The output voltage can be regulated by varying the duty cycle of the PWM.

III. METHODOLOGY

A. Matlab Simulink Software

This phase is associated with the implementation of projects to be developed through software and hardware. The parameters of each component are calculated. Simulation of the IBC had been done using Matlab/Simulink. Figure 1 shows the IBC circuit design using Matlab/Simulink software.

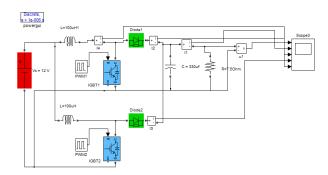


Figure 1. Simulation of IBC circuit using Matlab/Simulink

B. Quartus II software

The PWM signal for interleaved switching was programmed using Quartus II with combination of block diagram (*.bdf) and Very High Description Language (*.vhd). As in Figure 2, the block diagram consists of *altpll* which is able to generate a 25 MHz clock output from the 50 MHz internal clock of the Altera DE2-70 board. The altpll megafunction can be used to generate other clocks as well. Also, it can be set to operate at multiples frequencies. The clock divider is applied to divide the internal clock of Altera DE2-70 board into several frequency ranges. For example, the internal clock frequency can be divided into 25 MHz, 1 MHz, 100 kHz, 1 kHz and etc. Then, the 1 MHz output frequency of the clock divider is connected to the lpm counter which counts from 0 to 50 over one complete cycle. This means, one cycle of this frequency represents a period of 1 µs. The *lpm counter* megafunction is a binary counter that can be set to count upwards, downwards, or up and down simultaneously. Output from lpm counter will be compared with comparator circuit which generates the PWM switching signal. Two PWM switching signal output will be generated by Altera DE2-70 to trigger the IGBT in the IBC circuits. The dead time between pwm1 and pwm2 is being adjusted in the VHDL program. The dead time mainly depends on the characteristics of power devices and gate drive circuit [6]. The effects of dead time include output voltage loss and current distortion [7].

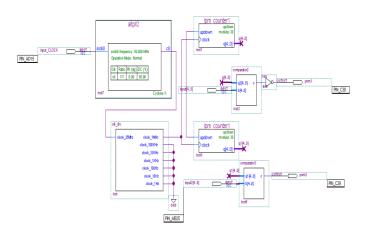


Figure 2. Block diagram of PWM signal generator by using Quartus II.

C. Hardware design and implementation.

IBC circuit is designed based on the calculation. Several parameters such as the switching frequency, duty cycle, input voltage and output voltage is set to be fixed value in order to calculate the suitable value of inductance and resistance. Through calculation the output voltage and current are also being considered. If the ripple amplitude of the current is high, the inductor may be completely discharged before the end of a whole commutation cycle. Table I shows the parameters values obtained from the calculation.

PARAMATERS VALUE	
Symbol	Value
V _{in}	12V
V _{out}	24V
С	330µF
L	100µH
F	40kHz
D	0.5
	Symbol V _{in} V _{out} C L F

A prototype of IBC has been designed in order to verify the simulation results. The power circuit consists of two boost connected in parallel with IGBT's and diode. The 12 volt lithium ion battery is used as an input supply. The driver circuit amplifies the signal from 3.3volt to 15 volt. The PWM switching signal from the driver circuit will trigger the IGBT's. Figure 3 shows the hardware experimental setup.

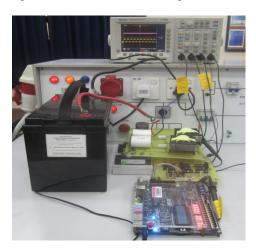


Figure 3. Hardware experiment setup of IBC

Oscilloscope Tektronix TDS 3042B is used to measure the output voltage, voltage and current ripple and etc. The recorded measurements are then being compared with the simulation and the calculation values.

IV. RESULT AND ANALYSIS

A. Simulation result using Matlab Simulink

As per the design specification, a two-phase IBC simulation model is developed using Matlab/Simulink. Ideal IGBTs and diodes are used in the model using PWM technique of interleaved to switching. Figure 4 shows the simulation result of the output voltage for 0.5 duty cycle.

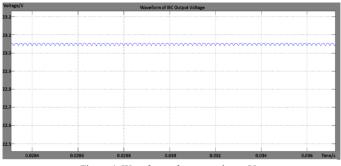


Figure 4. Waveform of output voltage, Vout.

The output voltage ripple calculated is equal to 0.03% which is settled at 23.07 Volt for 0.5 duty cycle. The output voltage is slightly less than the calculated value equal to 24 Volt. The voltage can be regulated from the changing of duty cycle. Table II shows the simulation results of output voltage with different duty cycle.

TABLE II. SIMULATION RESULTS			
Interleaved	Interleaved Duty Cycle		
Duty Cycle 1	Duty Cycle 2	(V)	
0.00	0.00	11.31	
0.14	0.14	13.13	
0.25	0.25	15.14	
0.33	0.33	17.01	
0.40	0.40	19.04	
0.45	0.45	20.80	
0.50	0.50	23.07	

B. Simulation result using Quartus II

imu	lation m	ode: Timing										
2	Master	Time Bar:	16.8	ns	• • Po	inter:	22.47 us	Interva	ıt 22	2.45 us	Start	
A E L		Name	V. 1	0 ps 16.8 ns	167.772 us	335.544 us	503.316 us	671.089 us	838.861 us	1.007 ms	1.17 <mark>,4</mark> ms	1.342 n
•		input_CLOCK		in the second								
	@ 1	pwm1										
•	@2 @3	pwm2 input		\vdash					L	15		

Figure 5.Simulation for PWM generator using Waveform Editor

Figure 5 shows the generated PWM signal using Waveform Editor (*.vwf). At this point, the on-off switching times of displayed PWM waveforms are compared with their calculated value and any deviation notes for correction.

C. Experimental results

Figure 6 shows the PWM switching signal. Ch1 and Ch2 is the PWM signal from Altera DE2 board. Ch3 and Ch4 is the PWM switching signal from driver circuit.

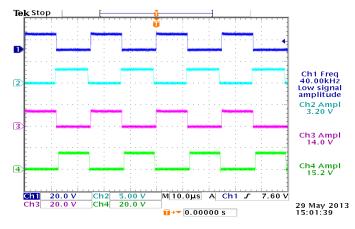
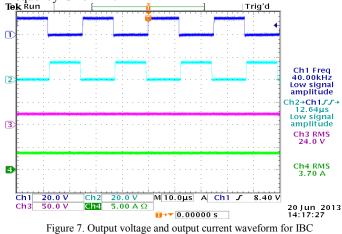


Figure 6. PWM switching signal and driver circuit

Waveform shows that the PWM output signal from gate driver circuit boosts from 3.3 V to 15 V. The switching frequency is 40 kHz.



Ch3 and Ch4 in the Fig. 7 show the output voltage and current respectively. The output voltage is slightly less than the calculated value equal to 24 Volt. In this situation, the duty cycle is adjusted to be 0.5 modulation index. By controlling the duty cycle on both sides of the phase, voltage change occurs. Accordingly, the output voltage is controllable. Table III shows the experimental results that have been obtained.

Interleaved Duty Cycle		Output Voltage,	
Duty Cycle 1	Duty Cycle 2	(V)	
0.00	0.00	11.18	
0.14	0.14	13.94	
0.25	0.25	15.87	
0.33	0.33	17.92	
0.40	0.40	19.95	
0.45	0.45	21.98	
0.50	0.50	23.90	

Table IV shows the comparison of output voltage between the calculation; simulation and experimental results.

TABLE IV. COMPARISON OF OUTPUT VOLTAGE

	Output Voltage, V _{out} (V)			
Duty Cycle	Calculation	Simulation	Experimental	
0.00	12	11.14	11.18	
0.14	14	13.51	13.94	
0.25	16	15.82	15.87	
0.33	18	17.59	17.92	
0.40	20	19.73	19.95	
0.45	22	21.32	21.98	
0.50	24	21.90	23.90	

It shows a slight difference in the value of the output voltage produced by experiments and simulations. It can be proved that the development of IBC has met all the desired objectives because it has been able to produce an output voltage that is close to the desired voltage of 24. After all results are taken, the difference between IBC and Conventional Boost converter has been made to find out the advantages of IBC compared to Conventional Boost converter. Table V shows the comparison between the IBC and Conventional Boost converter.

TABLE V. COMPARISON BETWEEN IBC AND CONVENTIONAL BOOST

	JOINVERIER	
Parameters	IBC	Conventional Boost
Input Voltage	12 Volt	12 Volt
Output Voltage	23.9 Volt	21.9 Volt
Switching Frequency	40kHz	40kHz
Output Ripple Current	1.65%	18.7%
Output Ripple Voltage	3.32%	5%
Efficiency	99.58%	91.25%

The results of the difference between the IBC and conventional boost converter indicates that the IBC has several advantages compared to the Conventional Boost converter because it has higher efficiency, lower voltage ripple, lower ripple current and high reliability.

CONCLUSIONS

In this paper, a simulation and hardware implementation of IBC was presented. By using this IBC, the output voltage can be adjusted by varying the duty cycle of the PWM switching. The performance of the IBC system under various duty cycles has been investigated. Comparison between the IBC and conventional boost converters shows that the IBC produces higher efficiency and reduced ripple. It is also found that interleaved boost has the ability in input current sharing as well as reducing the ripple current.

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