Fabrication and Characterization of Ion-Sensitive Field-Effect Transistors using Silicon-on-Insulator Technology

Inauguraldissertation

zur
Erlangung der Würde eines Doktors der Philosophie
vorgelegt der
Philosophisch-Naturwissenschaftlichen Fakultät
der Universität Basel

von

Kristine Bedner
aus Kronstadt, Rumänien

Basel, 2013

Genehmigt von der Philosophisch-Naturwissenschaftlichen Fakultät
auf Antrag von
Prof. Dr. Christian Schönenberger
Prof. Dr. Christofer Hierold
Dr. Matthias Streiff

Basel, den 23. April 2013

Prof. Dr. Jörg Schibler
Dekan

Contents

Contents iii

An Introduction to Sensing v

1 Ion-Sensitive Field-Effect Transistor as Sensing Element 1
- 1.1 Fundamentals of Semiconductors 1
- 1.2 The Transistor, a Semiconductor Device 3
  - 1.2.1 Transistor Basics 4
  - 1.2.2 Transfer Characteristics 12
  - 1.2.3 Metal-Semiconductor Junction 13
- 1.3 Ion Sensitive Field Effect Transistors 15
  - 1.3.1 From MOSFETs to ISFETs 15
  - 1.3.2 The Solid-Liquid Interface 15
  - 1.3.3 pH Response of ISFETs 17
- 1.4 Introduction to Noise 21
  - 1.4.1 Thermal Noise 21
  - 1.4.2 Shot Noise 21
  - 1.4.3 Generation and Recombination Noise 22
  - 1.4.4 1/f Noise 23
- 1.5 1/f Noise Models 24
  - 1.5.1 Gate Fluctuations 24
  - 1.5.2 Intrinsic Channel Fluctuations 25

2 Fabrication of Silicon Nanowire Sensors 27
- 2.1 Sensor Design 28
- 2.2 Silicon On Insulator as Substrate 28
- 2.3 Thermal Oxidation of Si Device Layer 28
- 2.4 Alignment Markers for Electron Beam Lithography 29
- 2.5 Sensor Patterning by Electron Beam Lithography 30
- 2.6 Dry and Wet Etching of the Sensor Pattern 31
- 2.7 Source-/and Drain Contact Implantation 33
- 2.8 Thermal Activation of Dopants 35
- 2.9 ALD Deposition of Gate Oxide 36

2.10 Contact Metallization and Annealing 37
2.11 Bonding and Packaging 38
2.12 Process Flow 40
2.13 Challenges in the Fabrication Process 41
2.14 Summary 41

3 Characterization of Silicon Nanowire Sensors 43
3.1 SiNW-ISFETs in Liquid Environment 43
3.1.1 Measurement Setup 43
3.1.2 Electrical Characterization 45
3.1.3 Impact of the SiNW Width on pH Sensing 49
3.2 Quality Tests performed in Liquids and in Air 52
3.2.1 Leakage Currents 52
3.2.2 Transfer Curves: Reproducibility and Hysteresis . . . 53
3.2.3 Ohmic Contact Characterization 54
3.3 Noise Investigations 56
3.3.1 Measurement Setup 56
3.3.2 1/f Noise in SiNW-ISFETs 57
3.4 Summary 62

4 Additional Investigations 65
4.1 Reference Electrode 65
4.2 Differential and Selective Ion Detection 67
4.2.1 Potassium Detection 67
4.2.2 Sodium Detection 68
4.3 Summary 68

5 Conclusions and Outlook 71

A Characterization of ALD Oxides 73

B Conductance Maps 77

C Fabrication Protocols 79

Bibliography 87

Publication List 97

Acknowledgements 99

An Introduction to Sensing

A sensor is a device used to translate an information, such as the ion concentration into an analytical signal. [1, 2] In general, the species being sensed, called target or analyte, binds to the sensor surface and thereby changes the surface properties. This change is detected by the sensor and translated into a measurable signal.
Most of the sample solutions in real life contain more species than the target. Ideally, the sensor responds only to the binding of the wanted target, and not to other species. This is known as *selectivity*. [2] A common method to achieve selectivity is to modify the sensor surface with immobilized receptors, that bind selectively the wanted target. A simultaneous detection of more than one target in the same sample solution, called *multiplexing*, is complicated but also possible. For a multiplexed detection, the sensor design is divided in different regions, that are functionalized with different receptors. The trouble with this approach is that one target can bind to multiple receptors, which is known as *cross-sensitivity*. In addition, for miniaturized sensors it is complicated to integrate a large number of differently functionalized regions on the same sensor, due to the limited sensor size. Nevertheless, multiplexing is an attractive sensor feature, as it reduces costs, sample volume and time for the analysis and more research is ongoing on this subject.
For a sensor one of the most important figure of merit is the *limit of detection*, defined by the smallest concentration or amount of target that can be reliably sensed. [3] A parameter determining the detection limit is noise.
Apart from noise, the signal can be distorted by many other factors, such as drift, temperature or non-specific adsorption. Such disturbances of the signal can be eliminated or minimized by *differential measurements*, where a reference and a sensing element are used. Ideally, the reference element is insensitive to the analyte, but otherwise it has similar properties to the sensing element. [4, 2] The signal results then from the difference between the signal of reference and sensing element.

The change in surface properties can be detected by different techniques, classified in mechanical, optical or electrical methods.
Mechanical sensors rely on a mechanical signal. For example, the quartz

crystal microbalance sensor detects a shift in the resonance frequency after the target binding. [5] The signal can be recorded by a frequency counter. [5] Another mechanical technique is to detect the bending of a cantilever, having one cantilever side functionalized with receptors. The interaction between the target and the receptor causes a surface stress, that results in a measurable bending of the cantilever. The bending is a function of the number of targets bound to the surface and can be detected by optical or electrical methods. [6] Plenty of difficulties have to be overcome before cantilever sensors will give a reliable analytical result. Some of the challenges are e.g. the increase of the response and the improvement of the mechanical robustness of the cantilever. [6]

The physical phenomena exploited for optical sensing are, e.g., fluorescence or surface plasmon resonance (SPR).

Surface plasmons are coherent electron oscillations existing at interfaces e.g. between metals and dielectrics. [7] Nowadays, mainly arrays of gold or silver nanoparticles surrounded by water or air are studied. [7] SPR is sensitive to the local environment, as changes in the refractive index influence the SPR peak position or magnitude. This property is used for chemical and bio-sensing. A strength of this sensor principle is that the binding reactions can be monitored in real-time, which allows to study the binding kinetics of different reactions. From the technical point of view, the main drawback for optical sensors is that they require optical components, which are difficult to integrate on a low-cost and portable system.

The second main class of optical sensors are based on fluorescence. This type of sensor needs - in contrast to the previous examples - labelled targets. The label is a fluorescent dye, attached to the target. After reaction with the target, the dye changes its fluorescent properties, expressed e.g. by a change in intensity or a shift in the wavelength of excitation or emission. [8] A disadvantage of intensity-based fluorescence sensors is, that intensity changes with time, which is known as bleaching. [8] The target labelling itself is a further disadvantage, as it is an expensive and time-consuming process, which may alter the target affinity to the receptor and thereby influence the signal. [8]

One candidate from the class of electro-chemical sensors is e.g. the impedance sensor. Impedance sensors detect the target binding by changes in the surface impedance. This type of sensor requires a potentiostat and three electrodes - a working, counter and a reference electrode - which are immersed in an electrolyte, in analogy to the three-electrode cell. [9] The surface of the working electrode is functionalized with receptors and thereby the sensing element. The impedance changes at the working electrode correlate with the number of targets bound to the receptors. However, the mechanism why the impedance changes is poorly understood and there is need for more

experimental and theoretical work. [2]

In this work we study the ion sensitive field effect transistor (ISFET), a potentiometric device that operates similar to the metal-oxide field effect transistor (MOSFET). A transistor contains three terminals: source, drain and gate. The source and drain contacts are separated by a channel, which is capacitively coupled to the gate. By applying a source drain voltage, a current flow through the channel is facilitated. The conductance can be controlled by a voltage applied to the gate. To convert a transistor into a sensor, the surface of the gate has to be chemically modified with receptors. When charged targets bind to the receptors, they act similar to an applied gate voltage, which results in a conductance change.
The working principle of ISFETs was first reported by Bergveld in 1970. [10] In the last decades the ISFET principle was applied to nanoscaled devices, such as carbon nanotubes [11, 12], graphene [13] and silicon nanowires (SiNWs). [14, 15] The advantages of nanostructures are manifold, as they allow e.g. to build a miniaturised and portable, low-cost sensor with a dense integration of differently functionalized nanostructures, enabling multiplexed detection. Experiments with silicon nanowire ISFETs (SiNW-ISFETs) have been performed in various fields ranging from pH-sensing [15, 16, 17, 18], to chemical [19, 20] and bio-sensing. [21, 22, 23, 24, 25]

The motivation of this work is to develop a platform for a (bio-) chemical sensor, based on SiNW-ISFETs. The growing need for sensors, e.g. in personalized medicine requires low-cost and portable sensing devices with a rapid and highly sensitive response. Among a deep understanding of the working principle for SiNW-ISFETs, a reliable response also requires a high signal-to-noise ratio and a differential read-out with an on-chip reference to correct drift and non-specific interactions. Some of these aspects will be addressed in this work.
Chapter 1 introduces to fundamentals of semiconductors and transistors and explains the concept of ISFETs. In **chapter 2** we describe the fabrication process of SiNW-ISFETs, based on silicon on insulator wafers, following the top down approach. In **chapter 3** we present the electrical and sensing performance of the sensors, measured in pH solutions and air. The sensor accuracy and the noise source were investigated in a noise analysis. **Chapter 4** includes additional investigations going towards the differential and selective measurements of alkali ions. In **chapter 5** we conclude the thesis and give an outlook.

1 Ion-Sensitive Field-Effect Transistor as Sensing Element

The ion-sensitive field-effect transistor (ISFET) indicates already in its name that the sensor is an electrical devices, utilizing a field-effect transistor (FET) as sensing element. In this chapter fundamentals of semiconductors and FET physics will be introduced since they are building blocks for ISFETs. Many ISFET characteristics are related to the FET behaviour. Based on the transistor operations, the concept of the ISFET will be presented. Typically, ISFETs are operated in electrolytes and for their better understanding the electrical double layer theory and site-binding model are required, which will be briefly reviewed.

1.1 Fundamentals of Semiconductors

Materials such as metals, insulators or semiconductors have different electrical properties due to their electronic band structure. In semiconductors there exist forbidden energy states in an energy band gap E_g. Allowed energy levels form bands below and above the band gap, referred to as the valence and conduction band, respectively. Typically, in a semiconductor the energy of the band gap E_g is smaller than 2 eV and the thermal energy at room temperature or the excitation from visible light can give electrons enough energy to move from the valence band to the conduction band. [26](p.16). Silicon

has a band gap of 1.12 eV. Insulators have a wider gap e.g. 9 eV for SiO_2 [26] (p.16), thereby electrons cannot cross the band gap at room temperature. *Intrinsic* semiconductors do not have impurity atoms and charge carriers are generated and annihilated by generation-recombination processes. In thermal equilibrium each electron in the conduction band forms a hole in the valence band and thus the concentration of electrons n equals that of holes p. This is why in intrinsic semiconductors the Fermi level lies in the middle of the band gap. The intrinsic charge carrier density of silicon is $1.5{\cdot}10^{10}\,\mathrm{cm}^{-3}$ [27] at room temperature and in thermal equilibrium $n{=}p{=}n_i$ holds. [27] To increase the number of charge carriers it is a common method to implant impurities such as doping atoms into the semiconductor which are later referred to as *extrinsic* semiconductors. Dopants in the intrinsic semiconductor generate allowed energy states within the band gap which are very close to the valence or the conduction band, depending on the type of doping atoms. In silicon, e.g., the boron energy level is separated from the valence band by 45 meV [27], which means a small energy is necessary to ionize the dopants and to create free charge carriers. At room temperature nearly all dopants are ionized. [28] Fig. 1.1 shows dopants, substituting silicon atoms in the crystal lattice. In intrinsic silicon each atom shares its four valence electrons with adjacent silicon atoms by forming covalent bonds. Doping atoms have either three or five valence electrons. Boron has only three valence electrons and when substituting a silicon atom in the crystal lattice, it accepts an additional electron and becomes ionized. Therefore, boron is known as an acceptor. When boron is ionized, a positively charged hole is generated in the valence band. The hole is a mobile and free charge carrier, participating in p-type conductance, whereas the boron ion stays fixed in the silicon crystal. Doping increases the hole concentration in the valence band relative to the electrons in the conduction band. Thus, "the Fermi level shifts towards the valence band". [29] The number of electrons decreases with increasing hole concentration and therefore the mass-law action $np{=}n_i^2$ [27] holds for intrinsic and extrinsic semiconductors. For n-type conductance the silicon is doped with doping atoms having five valence electrons, such as phosphorus or arsenic. The extra valence electron is donated to the lattice and a free electron is generated in the conduction band. For silicon the doping concentrations vary between $10^{13}\,\mathrm{cm}^{-3}$ and $10^{19}\,\mathrm{cm}^{-3}$. In extrinsic semiconductors the Fermi level is not in the middle of the band gap any more, as it moves with increasing doping concentration closer to the valence or conduction band. For very high doping concentrations the Fermi level lies in the valence or conduction band. This is known as a degenerate semiconductor. Degenerate semiconductor have electrical properties comparable to metals and thus, they are used to form Ohmic contacts in silicon, as described in the following sections. For silicon a doping concentration

above $\sim 10^{19}\,\mathrm{cm}^{-3}$ is considered as degenerated at room temperature. Relative to the number of silicon atoms of $\sim 5{\cdot}10^{22}\,\mathrm{cm}^{-3}$, this seems to be a low concentration .

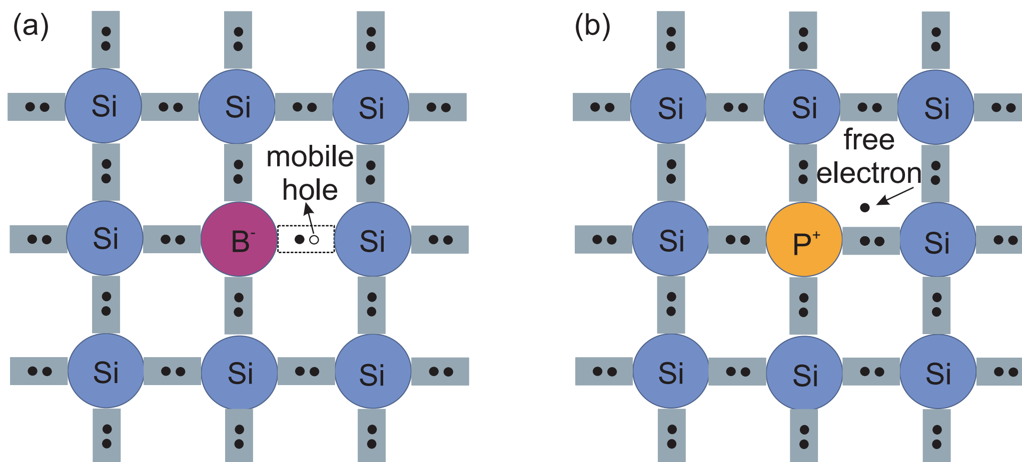


Figure 1.1: (a) Silicon lattice with a boron ion substituting a silicon lattice. The boron ion is negatively charged as it has three valence electrons and it accepted a forth electron from a silicon atom. When the boron is ionized a positively charged hole is generated in the valence band, which participates in the p-type conductance. Boron is known as an acceptor. (b) Phosphorous ion replaces a silicon lattice atom. Phosphorous is a donor as it has five valence electrons and the extra valence electron is donated to the lattice which generates a free electron in the conduction band.

1.2 The Transistor, a Semiconductor Device

These days semiconductors are intensively consumed in order to fabricate electrical devices, such as transistors. In this section, the transistor is introduced. Two types of transistors exist: the current controlled bipolar transistor and the voltage controlled field-effect transistor (FET). In 1925 Julius E. Lilienfeld patented the first basic principle for a FET. However, it was only in 1959 that Atalla und Kahng from the Bell Labs achieved a successful fabrication of a metal oxide field-effect transistor (MOSFET). For the first point contact bipolar transistor Shockley, Bardeen and Brattain from the Bell Labs obtained the Nobel price in physics in 1956.
A transistor has three terminals, known as source, drain and gate. Typically, MOSFETs have a fourth terminal at the substrate. Source and drain contacts are highly conductive and separated by a channel. Providing, that charge carriers are present in the channel a current can flow from the source to the drain contact when a source-drain voltage V_{sd} is applied. The conductance through the channel can be modified by the gate voltage V_g. The gate is usually made from a metal or poly-silicon layer.

A modern generation of FETs are the silicon-on-insulator (SOI) transistors as shown in Fig. 1.2. In contrast to the classical bulk MOSFET which utilize reversed pn-junctions to isolate the device from the bulk substrate, the SOI transistors are isolated by a buried oxide below a silicon device layer. The advantage of SOI transistors is that the channel and the source drain contacts can have the same polarity. Thereby, the transistor can be operated in accumulation e.g. p^+ - p - p^+, without the need for pn-junctions.

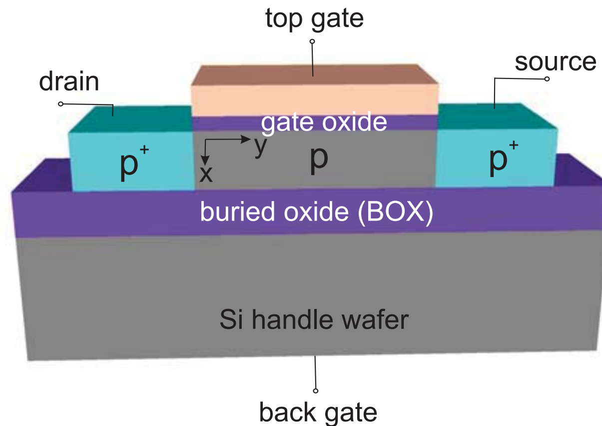


Figure 1.2: Structure of a p-type accumulation mode silicon-on insulator field-effect transistor (SOI MOSFET) shows the source and drain contacted which are separated by a channel. The channel contains dopants of the same polarity as the semiconductor region in which it is built. The channel is lightly doped and capacitively coupled to a gate. When applying a negative gate voltage V_g holes become attracted and an accumulation layer forms in the channel. Then, the transistor is in the accumulation mode. When a source-drain voltage V_{sd} is applied a source-drain current I_{sd} flow through the channel is facilitated. I_{sd} can be modulated by V_g.

1.2.1 Transistor Basics

In this section a p-type accumulation-mode transistor will be introduced, as such devices are used in this work. The physics of SOI MOSFETs is determined by the thickness of the silicon device layer and its doping concentration. Two types of SOI material can be distinguished: partially depleted and fully depleted silicon device layers. [30]
Before applying a gate voltage the bands of the semiconductor in a transistor are not flat, but bent. Generally, if a semiconductor is combined with a gate, that is separated by an oxide, then the bands are bent due to work function difference between the semiconductor ϕ_s and the gate material ϕ_m and oxide charges Q_{ox} in the gate oxide. [28] (p.312). To achieve a flatband condition as shown in Fig. 1.3 a a flatband voltage V_{fb} has to be applied at the gate [30]

$$V_{fg} = V_{th,acc} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} \tag{1.1}$$

where $\phi_{ms} = \phi_m - \phi_s$ is the difference between the gate workfunction ϕ_m and the semiconductor workfunction ϕ_s, Q_{ox} are charges in the oxide and C_{ox} is the gate oxide capacitance. For accumulation mode transistors the flatband voltage V_{fb} is equivalent to the beginning of the formation of a surface accumulation layer. Thereby, V_{fb} is equal to the threshold voltage for accumulation $V_{th,acc}$. Fig. 1.3 a shows the bandstructure of a p-type MOSFET in flatband condition. p-type transistors have a hole conductance and therefore to increase the number of holes a negative gate has to be applied (Fig. 1.3 b). The negative voltage causes the valence band to bend upwards near the gate oxide-semiconductor surface. The band bending reduces the energy difference E_F-E_V, resulting in an increase of the charge carrier density in the valence band. The potential at the oxide-semiconductor interface with respect to the intrinsic Fermi level E_i is called the surface potential ψ_s. At flatband condition ψ_s is zero and negative when the bands bend upwards. [28] In the bulk of the semiconductor the bands are not influenced by the interface, this region remains neutral. The potential in the bulk is referred to as the bulk potential ψ_B with $e\psi_B$=$(E_i - E_F)$. In the bulk the charge carrier density is described by Boltzmann statistics $n_i = N_A exp(e\psi_B/k_BT)$. Therefore the bulk potential is equal to $\psi_B = (k_BT/e)ln(N_A/n_i)$. When applying a small positive voltage, then the bands bend downwards and the channel becomes depleted from holes. At full depletion of the channel the surface potential ψ_s becomes positive and no current is supposed to flow. A surface potential larger than zero forms a depletion region at the oxide-semiconductor interface. We assume that in the depletion region no free charge carriers exist, since they are repelled by the electric field. Furthermore, we assume that all dopants are ionized and we have an abrupt doping profile. The charge in the depletion region is ρ= -eN_A. By solving the Poisson equation in the depletion region ($0 \leq$ x $\leq W_d$) [27] (Fig. 1.3 c)

$$E(x) = -\frac{\mathrm{d}\psi(x)}{\mathrm{d}x} = \frac{-\rho}{\varepsilon_0 \varepsilon_{Si}} \tag{1.2}$$

we obtain the electric field distribution in the semiconductor $E_{Si}(x) = eN_A(W_d - x)/\varepsilon_0\varepsilon_{Si}$, where W_d is the width of the depletion layer. The electric field in the semiconductor changes linearly with x and approaches zero at the end of the depletion region W_d. To find the potential distribution $\psi(x)$ we integrate the electric field $E_{Si}(x)$ over the depletion region. Then, we obtain the surface potential ψ_s at the oxide-semiconductor interface at

$\psi(x = 0)$

$$\psi_s = \frac{eN_A W_d^2}{2\varepsilon_0 \varepsilon_{Si}} \tag{1.3}$$

Rearranging the equation gives the depletion width W_d [27] (Fig. 1.3 c)

$$W_d = \sqrt{\frac{2\varepsilon_0 \varepsilon_{Si} \psi_s}{eN_A}} \tag{1.4}$$

The calculated field and potential distributions are only valid in the depletion regime. In accumulation regime there is no depletion layer.
For higher positive gate voltages the bands bend even more and when the intrinsic Fermi level E_i crosses the Fermi level E_F the channel starts to become populated with electrons at the oxide-semiconductor interface. At some point the number of electrons is larger than that of holes in a p-type semiconductor, which is known as inversion. In strong inversion the potential of the band bending ψ_s equals to $2\psi_B$ and the depletion width reaches its maximum value of $W_{d,max}$ (Fig. 1.3 d)

$$W_{d,max} = \sqrt{\frac{2\varepsilon_0 \varepsilon_{Si} 2\psi_B}{eN_A}} \tag{1.5}$$

The SOI material used in this work has a silicon device thickness t_{Si} of max. 85 nm and a resistivity ρ between 8.5 - 11.5 Ω·cm, which is related to a doping concentration between $N_A = 4.5 \cdot 10^{15}\text{cm}^{-3}$ - $6.1 \cdot 10^{15}\text{cm}^{-3}$. This results in a depletion width between 375 nm and 431 nm. As the depletion width is larger than the Si device layer, we work with fully depleted SOI material.

For small V_{sd} the transistor can be considered as a resistor with a channel conductance G

$$G = \sigma \frac{A}{L} \tag{1.6}$$

where σ is the conductivity, L the channel length and A the channel cross-section. Here we assume a homogeneous carrier density over the cross-section. The channel cross-section A can be replaced by the product $W \cdot t$, where W and t are the width and thickness of the channel, respectively. The conductivity σ is given by the product of the number of the charge carriers ne and their mobility μ. [27]

$$\sigma = ne\mu \tag{1.7}$$

In the linear regime the number of charge carriers ne per volume induced in the channel is determined by the product $\Delta V_g(C_{ox}^{\square}/t)$, where V_g is the

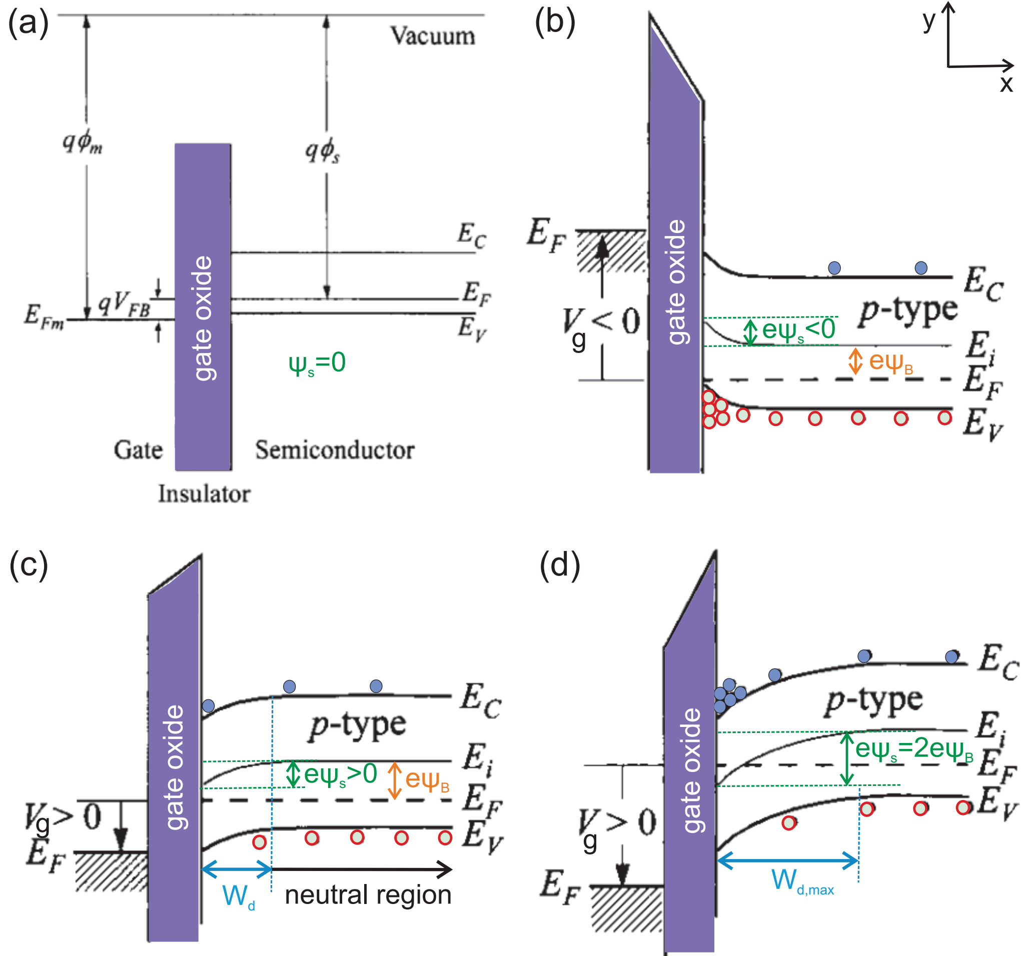


Figure 1.3: Figures adapted from Ref. [28]. (a-d) Bandstructure of a p-type bulk MOSFET. (a) Bands are in flatband condition. E_V and E_C denote the valence band and the conduction band energy. E_F represents the Fermi energy. $q\phi_m$ is the workfunction to extract an electron with a Fermi energy of E_{Fm} from the gate material. $q\phi_s$ is the workfunction of the semiconductor. qV_{fb} is the flatband energy. (b) A negative gate voltage V_g is applied and the bands bend upwards. ψ_s is the surface potential at the oxide-semiconductor interface. ψ_B is the bulk potential in the neutral region of the semiconductor. ψ_s>0 and therefore the p-type MOSFET is in accumulation. (c) A positive gate voltage is applied and the bends bend downwards. The p-type MOSFET is in depletion. A depletion width W_d forms at the oxide-semiconductor interface. (d) A higher positive voltage is applied and the bands bend even more downwards. When the intrinsic Fermi level E_i crosses the Fermi energy, then the oxide-semiconductor becomes populated with electrons in the p-type semiconductor. Therefore this situation is known as inversion. At strong inversion ψ_s equals to $2\psi_B$ and the maximum depletion width $W_{d,max}$ is reached.

gate voltage, t the channel thickness and $C_{ox}^{\square}$ is the gate oxide capacitance per area. Equation 1.6 can be rewritten as follows:

$$G = \frac{W}{L} C_{ox}^{\square} \mu V_g \tag{1.8}$$

where $C_{ox}^{\square}$ is the gate oxide capacitance per area. This yields a source-drain current $I_{sd,acc}$ [30]

$$I_{sd,acc} = \frac{W}{L} C_{ox}^{\square} \mu V_g V_{sd} \tag{1.9}$$

When considering the threshold voltage V_{th} (equ. 1.1), we obtain [30]

$$I_{sd,acc} = \frac{W}{L} C_{ox}^{\square} \mu (V_g - V_{th}) V_{sd} \tag{1.10}$$

This equation considers the source-drain current $I_{sd,acc}$ in the surface accumulation layer, induced by the gate voltage V_g. In accumulation mode transistors the charge carriers in the bulk silicon device layer can also contribute to the current, if the bulk is not depleted. The bulk current I_{bulk} can be derived from Ohm‘s law [30]

$$I_{bulk} = V_{sd} G = V_{sd} \sigma \frac{W t_{Si}}{L} = \frac{W t_{Si}}{L} e N_A \mu_B V_{sd} \tag{1.11}$$

with μ_B as the bulk mobility and t_{Si} is the thickness of the silicon device layer.

The total source-drain current I_{sd} is the sum of

$$I_{sd} = I_{sd,acc} + I_{bulk} \tag{1.12}$$

For small V_{sd} it is assumed that the accumulation layer has a constant thickness along the source-drain direction (y-direction in Fig. 1.2) and a pinch-off of the channel is not considered as those cases are unlikely to happen with a small V_{sd}=0.1 V, used in the experiments. Therefore, two extreme cases can be found in our experiments:

1. The silicon device layer is fully depleted and no accumulation or body current flows (Fig. 1.4 a): to achieve full depletion the depletion width has to extend over the total silicon device thickness t_{Si}. This case is achieved when the top gate voltage $V_{g,top}$ is larger than the sum of the flatband voltage at the top oxide-silicon interface $V_{fb,top}$ and the gate voltage with respect to flatband necessary to obtain a depletion width V_{depl}. This results in $V_{g,top} > V_{fb,top} + V_{depl}$. [30]

$$V_{depl} = \frac{e N_A t_{Si}^2}{2 \varepsilon_{Si} \varepsilon_0} + \frac{e N_A t_{Si}}{C_{ox}^{\square}} \tag{1.13}$$

The first term equals to the surface potential ψ_s and the second term contains the depletion charge $Q_d = e N_A t_{Si}$. In both terms the silicon device layer thickness equals to the depletion width, $t_{Si} = W_d$.

2. The silicon device layer is in accumulation and both, accumulation and

bulk currents flow (Fig. 1.4 b): to achieve this case following conditions have to be met $V_g - V_{fb,top} < 0$ and $V_{g,top} - V_{fb,top} - V_{sd} < 0$. The negative voltage is necessary to attract holes in the silicon device layer.

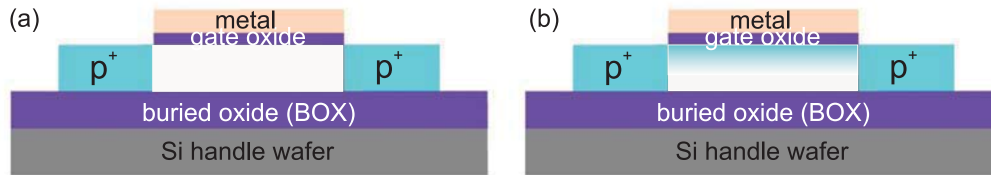


Figure 1.4: Figure adapted from Ref. [30] showing the cross section of a p-type accumulation mode transistor made from a SOI wafer in different conditions. (a) The silicon device layer is fully depleted. No accumulation or bulk current flows. (b) The silicon device layer is in accumulation and an accumulation and bulk current flows.

A negative back gate voltage V_{bg} can be applied during operation of a SOI MOSFET. [30] (p.223). The back gate voltage influences the subthreshold region in a way that the subthreshold swing increases with increasing negative back gate voltage. (Fig. 1.5 a) The subthreshold swing S will be explained in the following section.

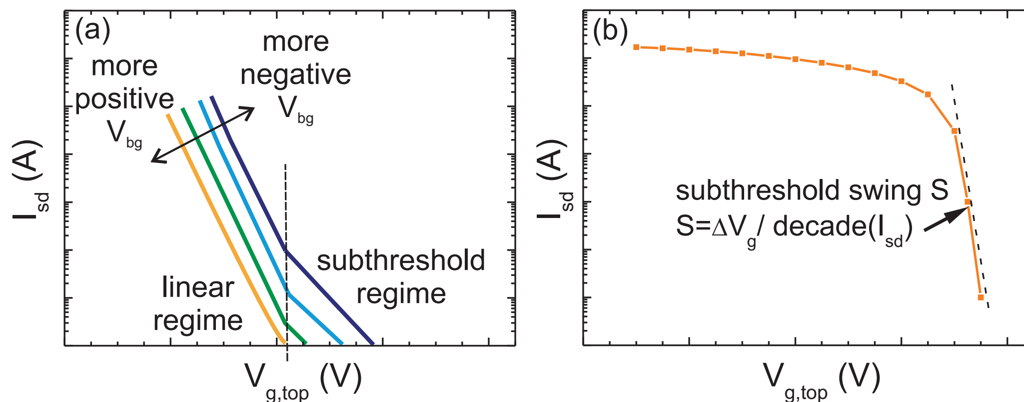


Figure 1.5: (a) Figure adapted from Ref. [30] (p.223). Source-drain current I_{sd} vs. top gate voltage $V_{gate,top}$ with the back gate voltage V_{bg} as parameter. For increasingly higher negative back gate voltage the current in the subthreshold regime increases. (b) Source drain current I_{sd} of the orange curve in Fig. 1.5 a on the logarithmic scale vs. gate voltage V_g. In the logarithmic representation the linear slope is known as the subthreshold swing $S{=}\Delta V_g/\text{decade}(\text{I}_{sd})$.

Below the threshold voltage V_{th} the transistor is in depletion and no current flow is expected. However, a small current referred to as the subthreshold current exists, that depends exponentially on the surface potential $I \propto exp(e\psi_s/k_BT)$. [28] The transfer characteristics plotted with the source-

drain current I_{sd} on the logarithmic scale shows the subthreshold current (Fig. 1.5 b). The inverse of the subthreshold slope, known as subthreshold swing S describes, how much gate voltage has to be applied to change I_{sd} by one order of magnitude. [30] In fully depleted SOI material the coupling between the top and back oxide has to be considered. [30] To determine the subthreshold swing for fully depleted SOI MOSFETs that are controlled by the top gate voltage $V_{g,top}$ following relation holds (the back gate voltage is constant):

$$S = \frac{\mathrm{d}V_g}{\mathrm{d}log(I_{sd})} = \frac{ln(10)}{\frac{\mathrm{d}ln(I_{sd})}{\mathrm{d}V_g}} \tag{1.14}$$

with

$$\frac{\mathrm{d}ln(I_{sd})}{\mathrm{d}V_g} = \frac{1}{I_{sd}}\frac{\mathrm{d}I_{sd}}{\mathrm{d}V_g} = \frac{1}{I_{sd}}\frac{\mathrm{d}I_{sd}}{\mathrm{d}\psi_{s,1}}\frac{\mathrm{d}\psi_{s,1}}{\mathrm{d}V_g} = \frac{k_B T}{e}\frac{\mathrm{d}\psi_{s,1}}{\mathrm{d}V_g} \tag{1.15}$$

where ψ_{s1} is the surface potential at the top silicon oxide interface, due to the top gate voltage. To determine $dV_g/d\psi_{s1}$ the capacitance model shown in Fig. 1.6 can be used. Generally, the oxide-semiconductor interface contains interface trap states, as explained below. For high interface trap state densities D_{it} the trap state capacitance per area $C_{it}^{\square}$, degrades the subthreshold swing. This results in a subthreshold swing S [30]

$$S = ln(10)\frac{k_B T}{e}\frac{C_{ox,1}^{\square} + C_{it,1}^{\square} + \frac{C_{Si}^{\square}(C_{it,2}^{\square} + C_{ox,2}^{\square})}{C_{it,2}^{\square} + C_{ox,2}^{\square} + C_{Si}^{\square}}}{C_{ox,1}^{\square}} \tag{1.16}$$

where $C_{ox,1}^{\square}$ and $C_{ox,2}^{\square}$ represent the top and back gate capacitance per area and $C_{it,1}^{\square}$ and $C_{it,2}^{\square}$ are the trap state capacitances per area from the top and back gate oxide, respectively. $C_{Si}^{\square}$ is the silicon device layer capacitance per area defined by $C_{Si}^{\square} = \varepsilon_0\varepsilon_{Si}/t_{Si}$.

The subthreshold current is regarded as an undesired leakage current and a limiting factor for device down-scaling, since it becomes a main reason for power consumption. An ideal subthreshold swing of $ln(10)(k_B T/e) = 59.5\,\mathrm{mV/dec}$ at 300 K can only be achieved theoretically in the extreme case for $C_{ox} \rightarrow \infty$.

Knowing the trap state capacitance per area $C_{it}^{\square}$ from the subthreshold swing, the trap state density D_{it} in $eV^{-1}cm^{-2}$ can be determined by $e^2 D_{it} = C_{it}^{\square}$. [30] Interface traps degrade the transistor performance when they are electrically active, which means they can trap and release charge carriers [28]. The charge of interface traps Q_{it} exists within the forbidden

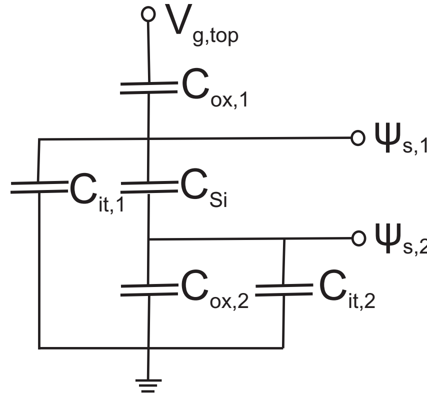


Figure 1.6: Capacitor model for a fully depleted SOI MOSFET showing the top and back gate capacitance per area $C_{ox,1}$ and $C_{ox,2}$ and the associated trap state capacitances per area $C_{it,1}$ and $C_{it,2}$, respectively. C_{Si} is the capacitance of the silicon channel and $\psi_{s,1}$ and $\psi_{s,2}$ are the surface potential at the top and back silicon oxide interface, respectively. The device is controlled by a top gate voltage $V_{g,top}$. [31]

band gap E_g. [28](p.213). The reason for the formation of traps is that atoms are missing at the surface of the silicon crystal and thereby the four silicon valence electrons are not always paired or saturated. Unpaired valence electrons are known as dangling bonds and they can form electrically active traps. Interface traps have an amphoteric character. Trap states located closely above the valence band are considered as donor-like since they are positively charged when empty and electrically neutral when occupied with an electron. Acceptor-like traps are located closely below the conduction band and they are electrically neutral when empty and negatively charged when occupied with an electron. [28] Interface trap states can be reduces by surface oxidation as dangling bonds become paired with oxygen atoms or by annealing in hydrogen atmosphere. [28] (p.214). For very clean silicon-oxide interfaces the trap state density can be reduced to about D_{it}=10^{10}cm^{-2}eV^{-1}. [28] Interfaces with high-k material have higher trap state densities. [32] A change of the interface trap charge occurs when a voltage is applied and the Fermi level moves up or down relative to the energy level of the interface traps. Then the trap states can be filled or emptied.
Apart from interface traps further trapped charges Q_{ox} exist in the oxide such as fixed oxide charges, mobile ionic charges and oxide trapped charges. Fixed oxide charges are located very close to the oxide-semiconductor interface, usually they are positively charged and the density is not affected by the oxide thickness. Mobile ionic charges such as K^+ can move within the oxide layer. Oxide trapped charges originate from defects in the SiO_2. In the beginning these traps are neutral and become charged when a current passes through the oxide layer. [28]

1.2.2 Transfer Characteristics

As mentioned in the previous sections the conductance G through the channel can be controlled by the gate voltage V_g. The curve with the conductance on the linear scale vs. the gate voltage is known as the transfer characteristics. In the linear representation the transfer curve displays three regimes: the subthreshold regime, the linear regime and the non-linear regime as shown in Fig. 1.7 a. In the latter regime the conductance deviates from linearity due to the source-drain contact resistance and mobility degradation. The subthreshold regime was introduced in the section above. In the following section more details about the linear will be given.

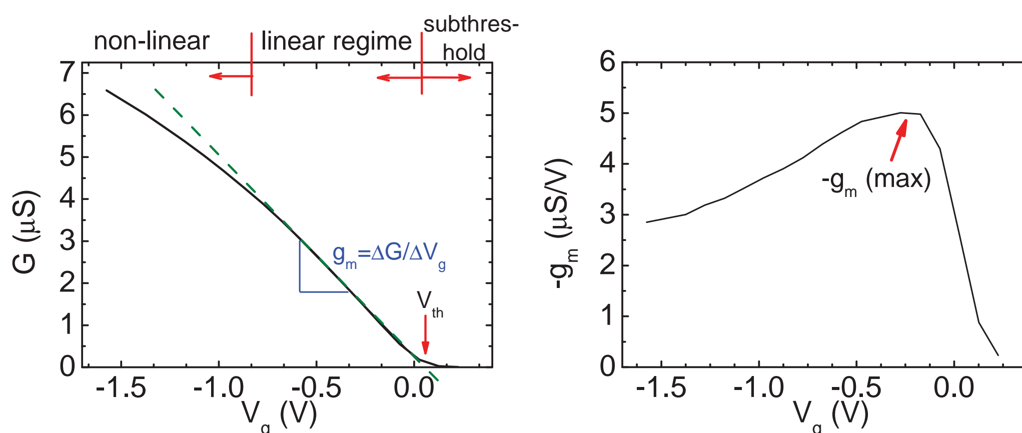


Figure 1.7: (a) Transfer characteristics with conductance G on the linear scale vs. gate voltage V_g. The gate voltage when a current flow is facilitated, is referred to as the threshold voltage V_{th}. The slope in the linear regime is known as transconductance $g_m = \Delta G / \Delta V_g$. (b) The first derivative of conductance G with respect to gate voltage V_g results in the transconductance curve g_m. The graph of the derivative increases until it reaches a peak value of $g_{m(max)}$. This value corresponds to the transconductance in the linear regime. Then, the graph of the derivative decreases due to source-drain contact resistance and mobility degradation.

For small V_{sd} and $V_g > V_{th}$ the transfer curve with G on the linear scale has a linear regime as shown in Fig. 1.7 a. This regime can be used to determine the transconductance g_m and the threshold voltage V_{th}. To extract the latter one a linear fit to the conductance G is extrapolated and the intersection point with the V_g-axis is equal to V_{th}. [28] (p.312). The transconductance g_m describes how efficient the gate voltage V_g induces charge carriers in the channel that contribute to the source-drain conductance G. [33] g_m can be extracted from the first derivative $\partial G / \partial V_g$ of the conductance G with respect to the gate voltage V_g. (Fig. 1.7 b). The graph of the first derivative shown in Fig. 1.7 b increases until it reaches a peak value of $g_{m(max)}$. The maximum corresponds to the transconductance in the linear regime. Then, the graph of the first derivative decreases due to source-drain contact

resistance and mobility degradation. The bulk current from equation 1.11 amounts to 174 pA with V_{sd}=0.1 V and can be neglected compared to the accumulation current in the linear regime. Therefore, equation 1.10 can be used and by rearranging we obtain in the linear regime

$$g_m = \frac{\partial G}{\partial V_g} = \frac{W}{L} C_{ox}^{\square} \mu \tag{1.17}$$

where $C_{ox}^{\square}$ is the gate oxide capacitance per area, μ the mobility of the charge carriers and W and L are the width and length of the channel, respectively. When the geometrical dimensions of the structure and the gate oxide capacitance per area are known, the mobility μ can be extracted.

The mobility μ is related to the drift velocity ν_D by [27]

$$\nu_D = \mu E \tag{1.18}$$

where E is the applied electric field. Charge carriers in an electric field are accelerated by the force F=eE to the drift velocity

$$v_D = \frac{eE\tau_c}{m} \tag{1.19}$$

where m is the mass and τ_c is the momentum relaxation time between scattering events. Thus, μ is equal to $e\tau_c/m$. The mobility in semiconductors is limited by different scattering mechanisms such as bulk phonon scattering, acoustic phonon scattering, surface roughness scattering and Coulomb scattering. Phonon and Coulomb scattering are temperature dependent. With increasing temperature the lattice vibrations increase and the mobility is reduced. However, the thermal velocity increases and carriers have less time to interact with ionized impurities which results in a reduced Coulomb scattering. [34]
In accumulation mode transistors, charge carriers of the bulk current experience less scattering events and therefore they have a higher mobility compared to the transport in inversion or accumulation layers, where confined charge carriers encounter a higher scattering rate due to surface roughness at the oxide-silicon interface.

1.2.3 Metal-Semiconductor Junction

The above section describes conductance changes through the channel due to applied gate voltages. One has also to consider the influence of the source drain contacts on the conductance. Therefore, this section deals with the metal-semiconductor junctions, needed to form source drain contacts.
The difference between the Fermi level and the vacuum level is denoted

as the workfunction ϕ. Usually, metals and semiconductors have different workfunctions, known as ϕ_m and ϕ_s, respectively. When a metal is in contact with a semiconductor the electrons will flow from the material with the lower workfunction until the Fermi level is the same in both materials. Thereby, the material with the lower workfunction (metal) will become positively charged, while that with the higher workfunction (p-type semiconductor) will become negative.

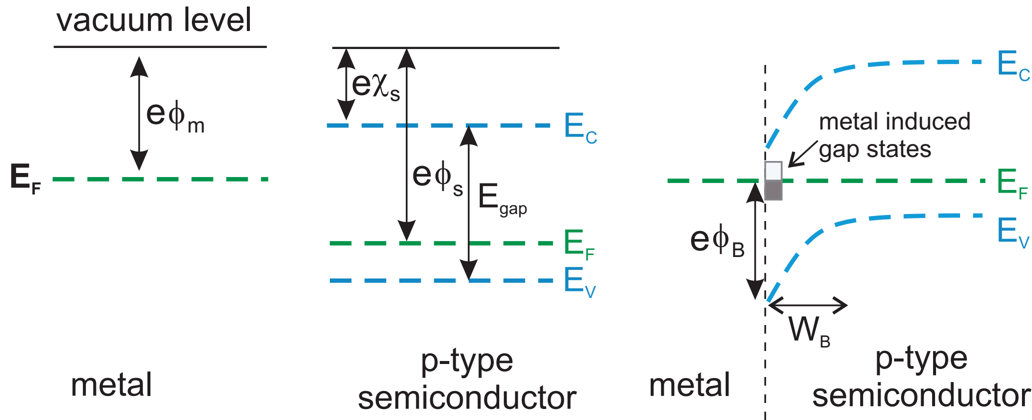


Figure 1.8: Band diagram of a metal and p-type semiconductor both separated and combined, showing the Fermi energy, the workfunction and the electron affinity E_F, ϕ, χ_s, respectively. When a metal and semiconductor are combined, electrons will flow from the material with the lower workfunction until the Fermi level is the same in both materials. Metal induced gap states pin the Fermi level, which results in a band bending and the formation of a barrier $e\phi_B$. Charge carriers from the metal have to overcome the barrier to enter the semiconductor. The barrier width W_B can be significantly reduced by high doping concentrations in the semiconductor.

Additionally, when a metal is combined with a semiconductor the metallic wavefunction does not stop abruptly, but it decays exponentially into the semiconductor and forms a separate band in the semiconductor band gap. The states are known as metal-induced gap states (Fig. 1.8), which have properties similar to those of interface states (section 1.2.1). The high density of gap states fix the Fermi level close to the charge neutrality level, since the charge carrier density in the semiconductor is too small to counterbalance little changes in the metal-induced gap state density. This results in a Fermi level pinning [27, 35] and a band bending, which forms a barriers $e\phi_B$ (Fig. 1.8). In electrical devices, charge carries from the metal have to overcome this barrier. By high doping concentrations in the semiconductor the barrier width can be reduced. This allows the formation of Ohmic contacts, which are characterized by a linear and symmetric source drain current vs. source drain voltage.

1.3 Ion Sensitive Field Effect Transistors

The working principle of a FET is briefly reviewed in the previous sections and in this section the ion-sensitive field-effect transistor (ISFET) will be introduced. The idea to use an ISFET as a sensor was first reported by Bergveld in 1970 [10] and based on that work plenty of publications followed.

1.3.1 From MOSFETs to ISFETs

The ISFET can be viewed as a MOSFET in which the metal gate is replaced by a liquid gate, which is typically an electrode immersed in an electrolyte solution (Fig. 1.9). The electrolyte is the solution under test, containing charged particles such as charged (bio)-molecules or ions e.g. protons. The gate oxide is directly exposed to the electrolyte solution and usually it is modified with receptors, allowing the specific detection of target species. For applications of pH sensing it is sufficient to have a bare gate oxide with hydroxyl groups (-OH) as receptor, since they interact with the protons in the solution. When the target species react with the receptors, the charged particles create an ion-sensitive surface potential ψ_0 on the sensor surface that acts similar to an applied gate voltage V_g. The ion-sensitive surface potential ψ_0 shifts the threshold voltage V_{th} as shown in the following equation, apdapted from Ref. [36] for p-type MOSFETs.

$$V_{th,acc} = E_{ref} - \psi_0 + \chi^{sol} - \frac{\phi_{Si}}{e} - \frac{Q_{ox}}{C_{ox}} \tag{1.20}$$

where E_{ref} is the constant potential of the reference electrode, ψ_0 the ion-sensitive surface potential, χ^{sol} the surface dipole potential of the solvent and ϕ_{Si} the workfunction of silicon. The charge Q_{ox} denotes trapped charge in the oxide and C_{ox} is the oxide capacitance.
Note, the threshold voltage is not determined by the metal workfunction ϕ_m as it is known for MOSFET (equ. 1.1) but by the ion-sensitive surface potential ψ_0. All terms are constant except for the ion-sensitive surface potential ψ_0 that depends on the interaction of the target species with the receptors. Thus, the shift of the V_{th} is the characteristic electrical signal of the sensor. Typical transfer curves showing a V_{th} shift as a function of the pH value are shown in section 3.1.3.

1.3.2 The Solid-Liquid Interface

When immersing a solid material in a solution usually a surface charge forms due to differences in the electrochemical potentials between the solid material and the electrolyte. The surface charge is an excess or deficiency of electrons

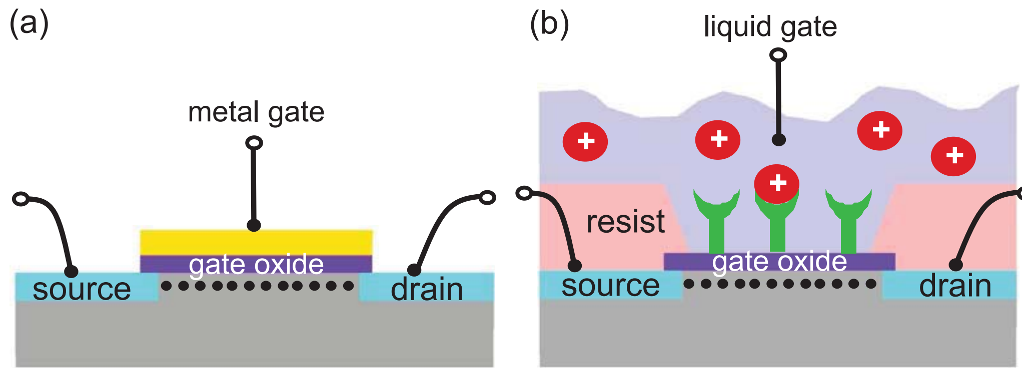


Figure 1.9: (a) Structure of a MOSFET showing the metal gate which is used to modulate the channel conductance. (b) Structure of an ion-sensitive field-effect transistor (ISFET) showing that the metal gate of the MOSFET is replaced by a solution under test, containing charged target species (red circles). The gate oxide is functionalized with receptors (green structures) and directly exposed to the solution. When the target species react with the receptors a surface potential builds up that shifts the threshold voltage V_{th}. The V_{th} shift depends on the interaction of the target species with the receptors and it is the electrical output signal of the ISFET.

at the solid surface that attracts counter ions from the electrolyte. To keep the system electrically neutral the net charge of the counter ions is equal to the net surface charge, but of opposite sign. Typically, the counter ions are surrounded by an aggregate of water molecules. The water molecules are attracted by the charge of the counter ions since water molecule are dipoles with an asymmetric charge distribution. When the solid material exhibits zero net surface charge in the electrolyte the pH value is referred to as the point of zero charge (pzc) or iso-electric point for that specific material. Usually, the pH value is used to determine the *pzc* as protons and hydroxyl ions influence the surface charge for most of the materials [**?**].
Counter ions which compensate the surface charge form a double layer that is structured in different sections. The layer closest to the bulk solution is called the Gouy-Chapman double layer [37] as shown in Fig. 1.10. In this layer, ions are not fixed but they tend to diffuse. The counter ions create an electrostatic potential in the electrolyte that can be described by combining the Poisson equation with the Boltzmann statistic. [38] The Poisson equation describes the electrical potential for a given charge distribution and the Boltzmann statistics is used to determine the ion distribution in the electric field. The Gouy-Chapman double layer is followed by the Stern layer which is formed by counter ions in direct vicinity to the solid-electrolyte interface. The counter ions are surrounded by the water aggregate and the closest distance to the interface is known as the outer Helmholtz plane (OHP). [37] In the Stern layer the potential drops linearly. Additionally to the Gouy-Chapmann-Stern theory the specific adsorption of ions on the surface also

influences the potential in the double layer. [37] Typically, these ions got rid of the water aggregates and therefore they can approach the surface much closer, to a distance known as the inner Helmholtz plane (IHP). The length over which the potential decays into the bulk solution is denoted as the Debye length L_D. [38] It is the characteristic length of the diffusive layer thickness and inversely proportional to the square root of the ion concentration as shown in the following equation

$$L_D = \sqrt{\frac{\varepsilon_r \varepsilon_0 k_B T}{2 L_A e^2 I_c}} \tag{1.21}$$

L_A is the Avogadro constant and I_c the ionic strength. The ionic strength is defined as $I_c = 1/2 \sum c_i z_i^2$, where c_i is the molar ion concentration and z_i the charge number of the ion. [39]

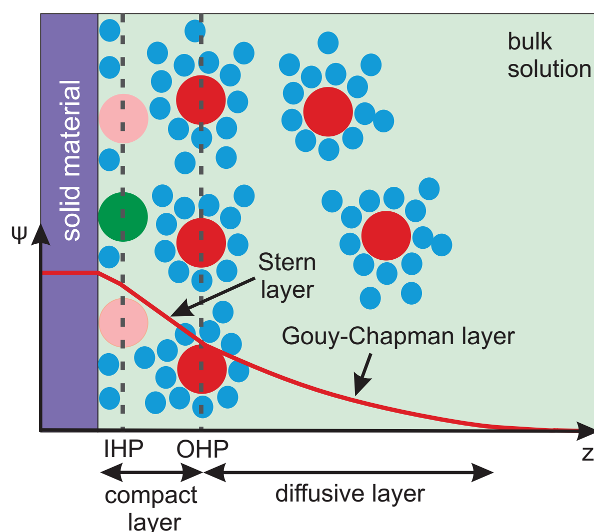
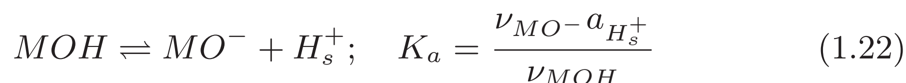


Figure 1.10: Figure adapted from Ref. [37]. Schematics of the double layer formed at a solid material that is immersed in a solution. Due to electrochemical differences between the material and the electrolyte a surface charge forms which is compensated by counter ions (red circles) in the solution. The counter ions are surrounded by water molecules (blue circles) forming a water aggregate. The ions create a potential drop in the solution that is shown by the red solid line. The length over which the potential V decays into the bulk solution is known as the Debye length, the characteristic length for the thickness of the diffusive layer. The closest approach of ions containing the water aggregate is known as the outer Helmholtz plane (OHP). Specific adsorption of ions without the water aggregate approach the surface to a distance known as the inner Helmholtz plane (IHP).

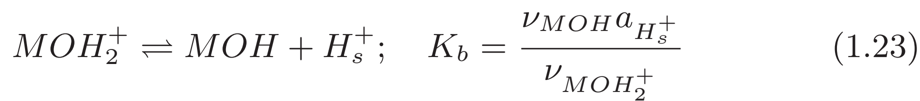
1.3.3 pH Response of ISFETs

The pH response of ISFETs can be described by the Gouy-Chapman-Stern theory and the site-binding model (SBM). The later one describes the charg-

ing mechanism of oxide surfaces, submersed in solutions. The SBM was first introduced by Yates et al. [40] and later improved by Healy et al. [41], Bousse et al. [42] and van Hal et al. [43]. A review about the development of the ISFET theory during the last decades was published by Bergveld. [36] As mentioned in the section about the double layer, a surface charge builds up when a solid material is submerged in a solution. The pH value can be measured with insulators used in semiconductor technology such as SiO_2 or Al_2O_3. Nowadays the sensing properties of high-k materials e.g. HfO_2 are investigated. In the SBM it is assumed that the oxide surface is hydrated which means it is covered with hydroxyl groups (OH-groups) and these groups have an amphoteric character as they have the ability to accept or donate protons (Fig. 1.11). Therefore, the oxide surface contains surface hydroxyl groups which are neutral MOH, or protonated (positively charged, MOH_2^+) or deprotonated (negatively charged, MO^-), depending on the pH of the bulk solution. M represents the parent material of the oxide and the corresponding surface reactions are: [42, 43]



$$MOH \rightleftharpoons MO^- + H_s^+; \quad K_a = \frac{\nu_{MO^-} a_{H_s^+}}{\nu_{MOH}} \tag{1.22}$$



$$MOH_2^+ \rightleftharpoons MOH + H_s^+; \quad K_b = \frac{\nu_{MOH} a_{H_s^+}}{\nu_{MOH_2^+}} \tag{1.23}$$

where K_a and K_b are the dimensionless dissociation constants, ν_i the number of sites per area and $a_{H_s^+}$ the activity of the surface protons. The activity a is proportional to the concentration c and defined as $a_i = \gamma_i c_i$, where c_i is the molar ion concentration and γ_i is the activity coefficient. [44]

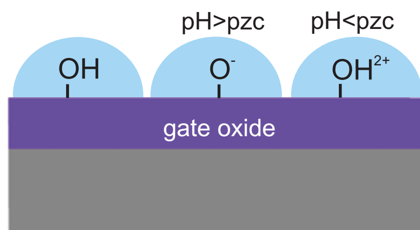


Figure 1.11: Hydroxyl groups (-OH) on an oxide surface can react in three different ways when the oxide is submerged in a pH solution. If the pH value of the solution matches the pH value of the point of zero charge (pzc), then the net surface charge will be zero, which means the number of MO^- and MO_2^+ is equal. If the pH value is larger than the pzc then the hydroxyl groups are deprotonated and negatively charged. If the pH value is smaller than the pzc then the hydroxyl groups are protonated and positively charged.

The total number of surface sites N_s per unit area is given by the sum [42, 43]

$$N_s = \nu_{MOH} + \nu_{MO^-} + \nu_{MOH_2^+} \tag{1.24}$$

The protonated MOH_2^+ and deprotonated MO^- sites generate a surface charge σ_0 [42, 43]

$$\sigma_0 = e(\nu_{MOH_2^+} - \nu_{MO^-}) \tag{1.25}$$

The surface charge σ_0 creates an ion-sensitive surface potential ψ_0 that causes a difference in the proton activity between the surface $a_{H_s^+}$ and the bulk solution $a_{H_B^+}$ due to the Boltzmann statistics [42, 43]

$$a_{H_s^+} = a_{H_B^+} exp(-e\psi_0/k_B T) \tag{1.26}$$

This can be translated into the Nernst equation

$$\psi_0 = 2.3\frac{k_B T}{e}(pH_s - pH_B) \tag{1.27}$$

where the pH is defined by pH=-log(a_{H^+}).

The surface charge σ_0 in equation 1.25 can be written as a function of the $a_{H_s^+}$ and the total number of available surface sites N_s by combining equation 1.22 - 1.24 as follows [43]

$$\sigma_0 = eN_s \frac{a_{H_s^+}^2 - K_a K_b}{K_a K_b + K_b a_{H_s^+} + a_{H_s^+}^2} \tag{1.28}$$

When altering the surface pH by an infinitesimal value the surface charge changes by [36, 45]

$$\frac{\partial \sigma_0}{\partial pH_s} = -e\beta_{int} \tag{1.29}$$

where β_{int} is the intrinsic buffer capacity of the oxide surface. β_{int} expresses the ability of the surface to buffer little changes in the surface pH, but not in the pH of the bulk solution. This results in a surface buffer capacitance C_s

$$C_s = \frac{e^2 \beta_{int}}{2.3 k_B T} \tag{1.30}$$

The surface buffer capacitance C_s is specific for each oxide type e.g. Al_2O_3 has a higher C_s than SiO_2. [46]

Due to the charge neutrality the charge in the double layer σ_{DL} is equal to the charge on the oxide surface, but of opposite polarity as expressed by

following equation [43]

$$\sigma_{DL} = -C_i\psi_0 = -\sigma_0 \tag{1.31}$$

with C_i being the integral double layer capacitance resulting form the Gouy-Chapman-Stern model. The ability of the surface to store charges due to changes in the potential is represented by the differential double layer capacitance C_{dl} [43]

$$\frac{\partial\sigma_0}{\partial\psi_0} = -\frac{\partial\sigma_{DL}}{\partial\psi_0} = C_{dl} \tag{1.32}$$

Combining equation 1.29 and 1.32 results in the expression for the surface potential change as a response to little changes in the surface pH [43]

$$\frac{\partial\psi_0}{\partial pH_s} = \frac{\partial\Psi_0}{\partial\sigma_0}\frac{\partial\sigma_0}{\partial pH_s} = \frac{-e\beta_{int}}{C_{dl}} \tag{1.33}$$

The Nernst equation relates pH_s to pH_B

$$\frac{\partial\psi_0}{\partial pH_s} = 2.3\frac{k_BT}{e}(1-\frac{\partial pH_B}{\partial pH_s}) = -\frac{e\beta_{int}}{C_{dl}} \tag{1.34}$$

$$\frac{\partial pH_B}{\partial pH_s} = \frac{e^{\beta}_{int}}{2.3k_BTC_{dl}} + 1 \tag{1.35}$$

$$\frac{\partial\psi_o}{\partial pH_s} = \frac{\partial\psi_0}{\partial pH_B}\frac{\partial pH_B}{\partial pH_s} \tag{1.36}$$

The pH response of the surface oxide can be expressed by

$$\frac{\partial\psi_0}{\partial pH_B} = \frac{\partial\psi_0}{\partial pH_s}\frac{\partial pH_s}{\partial pH_B} = \frac{-e\beta_{int}}{C_{dl}}(\frac{e^2\beta_{int}}{2.3k_BTC_{dl}}+1)^{-1} \tag{1.37}$$

$$\frac{\partial\psi_0}{\partial pH_B} = -2.3\frac{k_BT}{e}\alpha \quad with \quad \alpha = (\frac{2.3k_BTC_{dl}}{e^2\beta_{int}}+1)^{-1} = (\frac{C_s}{C_{dl}+C_s}) \tag{1.38}$$

α is a dimensionless parameter that varies between 0 and 1, depending on the differential double layer capacitance C_{dl} and the surface buffer capacitance C_s. If α equals one then the maximum pH response of 59.5 mV/pH at 300 K will be achieved, which is also known as the Nernst limit. As equation 1.38 shows, α reaches one only if $C_s \gg C_{dl}$. This condition is not fulfilled by all gate oxides, e.g. SiO_2 has a small surface buffer capacitance compared to Al_2O_3 or HfO_2 and therefore ISFETs with SiO_2 as gate oxide achieve typically a pH response of $\sim$30 mV/pH [36, 47], whereas the

counterparts with Al_2O_3or HfO_2 exhibit a full Nernstian pH response of 59.5 mV/pH at 300 K. [17, 18]

1.4 Introduction to Noise

In the previous sections we mainly focus on the signal of SiNW-ISFETs and we completely neglect the influence of noise. This is careless, as noise is a random and uncorrelated fluctuation of the signal over time and it can be observed in all conductive materials. [34] For electronic systems, especially for sensors, noise is a fundamental issue as it determines the resolution of the signal. The generation of noise can be categorized in two groups: external sources originating e.g. from AC power lines or mechanical vibrations and internal sources such as oxide traps, lattice defects and charge scattering. [34] External noise sources can be removed, however internal noise cannot be eliminated - unwanted internal noise effects can only be minimized. Therefore, it is essential to have a better understanding of the different noise components and their mechanisms. In this section internal noise components are introduced such as thermal noise, shot noise, generation and recombination noise and $1/f$ noise. Typically, these noise components have different magnitudes and the total noise is a sum over all of them. The mechanisms behind $1/f$ noise is an ongoing controversial debate and the community agreed on few models, that will be briefly discussed in the following section.

1.4.1 Thermal Noise

Thermal noise, or Johnson-Nyquist noise is caused by thermodynamic fluctuations of charge carriers in a material. A resistor with R at non-zero temperature generates a thermal noise, regardless if a source-drain voltage is applied. The power spectral density of the voltage fluctuations S_V due to thermal noise is given by [34]

$$S_V = 4k_BTR \tag{1.39}$$

The unit of the power spectral density for voltage noise is V^2/Hz. Thermal noise is frequency independent and called *white* noise (Fig. 1.12).

1.4.2 Shot Noise

Shot noise is produced when charge carriers cross a potential barrier such as Schottky barriers or pn-junctions independently of each other and at

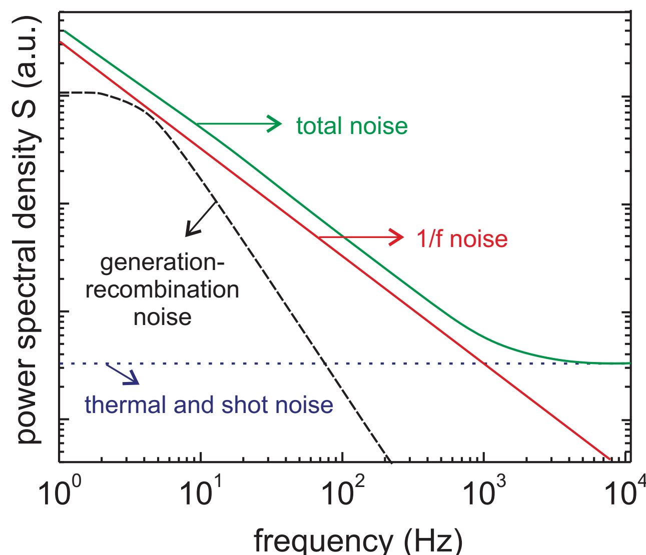


Figure 1.12: Figure adapted from Ref. [34]. For the characterization of noise it is a common method to translate the fluctuations in the time domain by Fourier transformation to a noise spectrum with the power spectral density S vs. frequency f. Different types of noise sum up to the total noise (green line). Thermal and shot noise are frequency independent, which is in contrast to $1/f$ noise and the generation and recombination noise.

random. [34] The current crossing the barrier generates a current noise with a power spectral density S_I of

$$S_I = 2eI \tag{1.40}$$

where I is the DC current across a barrier. [34] The unit of the power spectral density for current noise is A^2/Hz. Shot noise is, like thermal noise, independent of the frequency, as shown in Fig. 1.12. Shot noise is less relevant for MOSFETs and therefore not considered in this work.

1.4.3 Generation and Recombination Noise

Generation and recombination noise in semiconductors is caused by random trapping and releasing of charge carriers in trap states located close to the semiconductor-oxide interface, which results in fluctuations in the number of free charge carriers. Charge carriers can be captured only, if the Fermi level is located few $k_B T$ away from the trap states. Otherwise the traps are full or empty for most of the time and do not significantly contribute to noise. [34] The power spectral density of generation and recombination noise has a Lorentzian shape [34]

$$S \propto \frac{\tau}{1 + (2\pi f)^2 \tau^2} \tag{1.41}$$

as shown in Fig. 1.12, where τ is the time constant of charge carriers.

Two special cases of generation and recombination noise exist:
1. If only few trap states are involved in the generation and recombination noise, the fluctuations show a random switching between two or few discrete levels, similar to a telegraph signal with on/off-states. This special form of noise is known as random telegraph signal (RTS).
2. A superposition of generation and recombination noise with certain time constants τ produces $1/f$ noise, as discussed in the section below.

1.4.4 1/f Noise

$1/f$ noise, or flicker noise is characterized by a power spectral density S

$$S \propto f^{-\gamma} \tag{1.42}$$

where γ is in the range between 0.7-1.3 [34] (Fig. 1.12).

$1/f$ noise is present in semiconductors, metals and superconductors under bias. The superposition of generation and recombination noise from a large number of traps can generate $1/f$ noise, as demonstrated in Fig. 1.13 by an example with four Lorentzians superimposed to $1/f$ noise. [34]

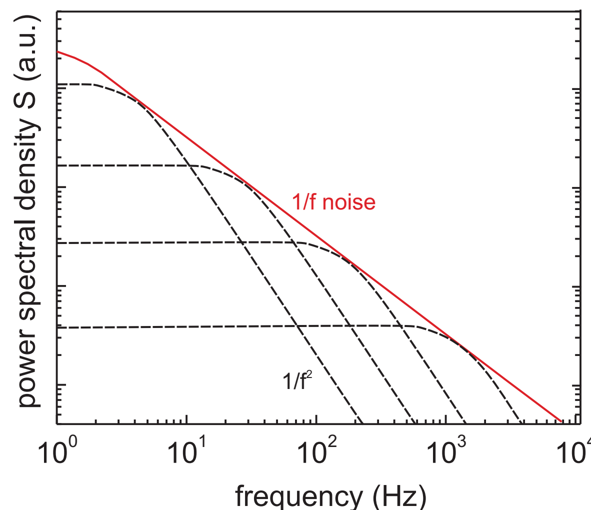


Figure 1.13: Figure adapted from Ref. [34]. Noise spectrum with the power spectral density S vs. frequency f shows the superposition of four Lorentzians with $1/f^2$ behaviour, resulting in a $1/f$ dependence.

1.5 1/f Noise Models

To explain the $1/f$ resistance fluctuations in transistors two approaches can be pursued:
1. fluctuations in the resistance due to fluctuations in the gate
2. intrinsic channel resistance fluctuations
These two approaches are the reason, why the origin of $1/f$ is still under discussion. For both approaches experimental data was found and different models were developed which will be introduced in the following section.

1.5.1 Gate Fluctuations

Behind the gate fluctuations, two different mechanisms exist:

Trap State Noise Model

In this model, tapping and detrapping of individual charge carriers into trap states close to the semiconductor-oxide interface cause $1/f$ noise. This $1/f$ model was first formulated by McWhorter [48], who observed at the germanium-oxide interface $1/f$ noise. In 1957, he claimed that, $1/f$ noise is a surface phenomena for samples with a conductance close to the surface, as the quality of the surface determines the noise density. [49]
Trap state that randomly catches and releases charge carriers generates a fluctuation in the gate oxide charge with a power spectral density $S_{Q_{ox}}$. This results in fluctuations of the power spectral density of the flatband voltage $S_{V_{fb}}$ in the units V^2/Hz as follows [34]

$$S_{V_{fb}} = \frac{S_{Q_{ox}}}{C_{ox}^2} \tag{1.43}$$

Equation 1.43 can be rearranged into

$$S_{V_{fb}} = \frac{S_{Q_{ox}}}{C_{ox}^2} = \frac{e^2 N_{ot}}{WLC_{ox}^{\square 2}} \frac{1}{f} \tag{1.44}$$

where N_{ot} are the trap state density per area in cm^{-2}. The relations $S_{Q_{ox}} = eN_{ot}WL/f$ and $C_{ox} = C_{ox}^{\square}WL$ were used.
In this model, the power spectral density of the flatband voltage fluctuations $S_{V_{fb}}$ is a constant and independent of the applied gate voltage V_g. This is the main characteristics of $1/f$ noise, originating from gate fluctuations.
The power spectral density of the flatband voltage fluctuations $S_{V_{fb}}$ is equivalent to the gate referred voltage noise S_{VG} in the units V^2/Hz. [50] S_{VG}

is a mathematical construction and it represents the external noise, that one would have to put on the gate to obtain the same source drain current noise. [50] S_{VG} can be related to the source drain current noise S_{Isd} in the units A^2/Hz as follows [50]

$$S_{V_{fb}} = S_{VG} = \frac{S_{Isd}}{g_{m,Isd}^2} \tag{1.45}$$

where $g_{m,Isd}$ is the transconductance given by $g_{m,Isd} = \partial I_{sd}/\partial V_{gate}$.

By combining equation 1.45 with equation 1.44 and rearranging, we obtain a source drain current noise S_{Isd}

$$S_{Isd} = S_{V_{fb}} g_{m,Isd}^2 = \frac{e^2 N_{ot}}{WLC_{ox}^{\square 2}} \frac{1}{f} g_{m,Isd}^2 \tag{1.46}$$

It is a common method to normalize the source drain current noise S_{Isd} by the source drain current squared I_{sd}^2.

$$\frac{S_{I_{sd}}}{I_{sd}^2} = \frac{e^2 N_{ot}}{WLC_{ox}^{\square 2}} \frac{1}{f} \frac{g_{m,Isd}^2}{I_{sd}^2} \tag{1.47}$$

Dielectric Polarization Noise Model

In this model the gate fluctuations are explained by the dielectric polarization noise model, reported by Clement et al. [51]. In the dielectric polarization noise model, the noise originates from thermal fluctuations of dipoles in the gate oxide. Thus, S_{VG} is based on thermal noise, with the resistance R replaced by the real part of the impedance $Re(z)$

$$S_{VG} = 4k_B T Re(Z) = \frac{2k_B T tg\delta}{\pi C_{ox} f} \tag{1.48}$$

where $tg\delta$ is the dielectric loss tangent of the dielectric, defined by $tg\delta = Re(Z)/|Im(Z)| = 2\pi f C_{ox} Re(Z)$. In this model, the initially white thermal noise obtains a $1/f$ characteristics due to the complex impedance of the dielectric material.

1.5.2 Intrinsic Channel Fluctuations

The intrinsic channel fluctuations can be explained by Hooge‘s empirical relation for $1/f$ noise. Hooge‘s empirical formula states that for a homogeneous sample the resistance and thereby further quantities fluctuate as [49]

$$\frac{S_R}{R^2} = \frac{S_{Isd}}{I_{sd}^2} = \frac{S_{V_{sd}}}{V_{sd}^2} = \frac{\alpha_H}{Nf} \tag{1.49}$$

where N is the number of charge carriers and α_H is the dimensionless Hooge parameter.
Noise following Hooge‘s empirical relation is "inversely proportional to the total number of free charge carriers". [52] For transistor noise, N is replaced by the number of charge carriers in the channel [49] $N = WLQ^{\square}/e$, where W and L are the width and length of the channel, respectively and $Q^{\square}$ is the charge per area. The normalized source drain current noise S_{Isd}/I_{sd}^2 is thus given by [53]

$$\frac{S_{Isd}}{I_{sd}^2} = \frac{e\alpha_H}{fWLQ^{\square}} \tag{1.50}$$

Equation 1.50 can be rearranged into

$$\frac{S_{Isd}}{I_{sd}^2} = \frac{e\alpha_H \mu R}{fL^2} \tag{1.51}$$

where the relation $Q^{\square}=C_{ox}^{\square}V_g$ and equation 1.9 were used.

The gate referred voltage noise can be obtained from combining equation 1.51 with $S_{VG} = S_{Isd}/g_{m,Isd}^2$ (compare equation 1.45)

$$S_{VG} = \frac{e\alpha_H \mu V_{sd} I_{sd}}{fL^2 g_{m,Isd}^2} \tag{1.52}$$

In this model the gate referred voltage noise contains the source drain current I_{sd} that depends on the gate voltage V_g. Thus, it is not constant as in the gate fluctuation model.

2

Fabrication of Silicon Nanowire Sensors

For the fabrication of SiNW sensors several techniques are published in literature [14, 15], which, however are divided in two main categories: the bottom-up or top-down approach. In the bottom-up approach nanowires are chemically synthesized from precursor gases and metallic nanoparticles are used as catalyst. [14] The diameter of the nanowire is defined by the diameter of the catalyst. The advantage of the bottom-up approach is that nanowires with well-controlled doping concentrations and electrical properties and diameters $<20\,\text{nm}$ can be grown. [54] However, a precise control over the diameter is lacking. Furthermore, the formation of Ohmic contacts, as well as the technique to assemble grown nanowires into functional devices are obstacles which have to be overcome in the future. Starting from a bulk material and "carve" it into the desired shape by using conventional semiconductor fabrication techniques like lithography and etching procedures is referred to as the top-down approach. The top down approach allows a precise control over the dimensions and position. The down-scaling to nanostructures is restricted by the limitations of lithography, which is usually a cost-intensive fabrication step. In this work SiNW-ISFETs were fabricated following the top down approach, as described in this chapter. Detailed process parameters are given in the appendix C.

2.1 Sensor Design

The SiNW-ISFET shown in Fig. 2.1 has 48 SiNWs per sample which are arranged in four arrays. Each array contains twelve SiNWs, sharing the same common drain contact as shown in the red square of Fig. 2.1 a and the enlarged view in Fig. 2.1 b. Twelve SiNWs are subdivided in six SiNWs having the same SiNW width. In total, eight different SiNW widths ranging from 100 nm to 1 μm are integrated on one sample. Each SiNW can be addressed individually by one of the 48 source contacts. The source and drain contacts are implanted and metallized as described in the following sections. The dark green regions in Fig. 2.1 a represent the metallization pattern. To electrically isolate the contact leads from the liquid environment, SU-8 microchannels are formed on top of the SiNWs, as shown in Fig. 2.1 d. Only the area within the opening of the microchannel is exposed to the environment. Fig. 2.1 c shows alignment marker used for electron beam lithography and optical lithography.
The large number of 48 SiNWs integrated on one sensor allows to carry out diverse experiments. Some of them will be presented in this thesis, e.g., the systematic study on the influence of the SiNW width on the pH response and the noise properties. Additionally, the surface of the as-fabricated SiNWs can be modified with receptors that are sensitive to selective species like K^+ or Na^+ ions. Different functionalization of individual arrays can be realized by sending solutions of surface chemistry through a PDMS microfluidic system, integrated on top of the SiNWs. Typically, the PDMS microfluidic system shown in Fig. 2.1 a is used to conduct the analyte over the SiNWs.

2.2 Silicon On Insulator as Substrate

As substrate material we used a silicon on insulator (SOI) wafer from Soitec [55], fabricated with the Smart Cut [55] process technology. A SOI wafer consists of three layers: the Si device layer on top, the Si handle wafer at the bottom and in between a buried SiO_2 layer. The material used had a 88 nm thick p-type (100) Si device layer with a resistivity of 8.5-11.5 Ω·cm on top of a 145 nm thick buried thermal SiO_2 layer. The Si handle wafer had a low p-type doping with a resistivity of 8-22 Ω·cm.

2.3 Thermal Oxidation of Si Device Layer

In the first step we oxidized the Si device layer in order to grow 10 nm thermal oxide. The thermal oxidation of Si was performed at a temperature of 1050 $^\circ$ C with molecular oxygen O_2, instead of water vapour. Therefore,

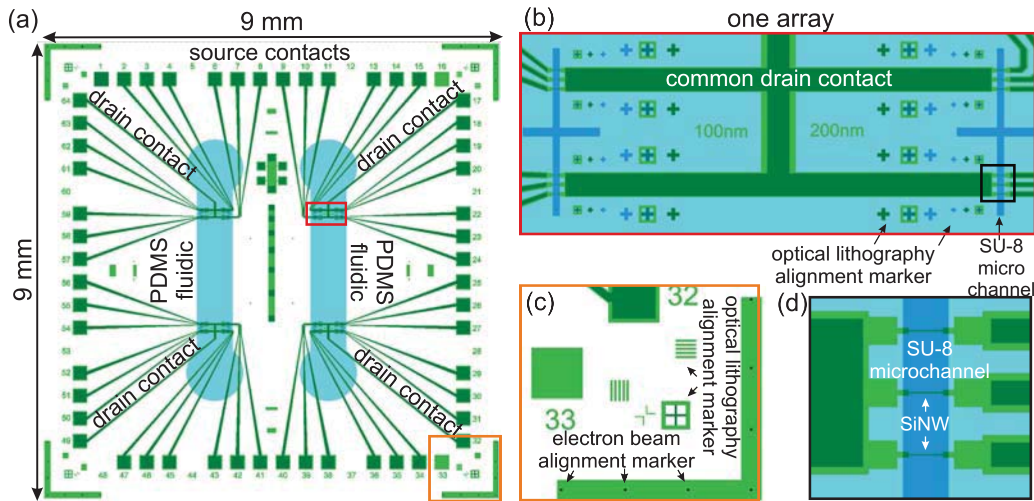


Figure 2.1: (a) Design of the SiNW-ISFET. One sensor contains 48 SiNWs which are arranged in four arrays with twelve SiNWs sharing the same drain contact. The SiNWs can be addressed individually. On top of the SiNWs a PDMS microfluidic system is integrated to conduct the analyte over the SiNWs. The red and orange squares mark the position of Fig. b and Fig. c, respectively. (b) One array with twelve SiNWs connected to the common drain contact is shown. Black arrows indicate the optical lithgraphy marker and the SU-8 microchannel, aligned to the SiNWs. The black square shows the position of Fig. d. (c) Black arrows indicate alignment markers, needed for the overlay exposures done by optical and electron beam lithography. (d) Three SiNWs embedded in a SU-8 microchannel are shown. Only the SiNWs are exposed to the analyte. The contacts are covered by the SU-8 layer and thereby electrically isolated.

the growing method is known as "dry oxidation" and the chemical reaction is as follows:

$$Si + \mathrm{O}_2 \rightarrow \mathrm{SiO}_2 \tag{2.1}$$

The oxidation reaction takes place at the Si/SiO_2 interface, meaning that Si is consumed while the SiO_2 thickness grows. [56] (p.94). The Si thickness shrinks by 44 % of the final oxide thickness. Thus, the thermal growth of 10 nm SiO_2 reduces the Si device layer thickness by 4.4 nm down to approx. 84 nm. The SiO_2 layer was used as an etch mask, described in the following sections.

2.4 Alignment Markers for Electron Beam Lithography

For the sensor fabrication we used the electron beam writer Vistec EBPG 5000+, that was operated at a fixed acceleration voltage of 100 keV. Electron beam lithography (EBL) is an important technique to define nanostructures. The complex structure of a SiNW-ISFET requires more than one ELB step. Therefore, alignment markers are required which allow a precise alignment

of overlay exposures. As subsequent process steps did not allow metallic markers, we defined the electron beam markers shown in Fig. 2.1 c by 1 μm deep trenches, etched into the substrate.
The electron beam alignment markers were aligned to the Si <110> direction, in order to align all following exposures along this direction. To fabricate 1 μm deep trenches we had to etch from the top side of the SOI wafer into the Si handle wafer. Silicon and SiO_2 are etched in plasma, based on fluorine gases such as SF_6, CF_4, CHF_3 and SiF_4. The etch rate depends on the concentration of atomic fluorine as Si and SiO_2 reacts with the fluorine to a volatile gas SF_x. [57] (p.134). The oxide layers and the Si layer were etched with plasma containing CHF_3 gas and a gas mixture of CHF_3 and SF_6, respectively.

2.5 Sensor Patterning by Electron Beam Lithography

In the next step, the sensor pattern was defined relative to the alignment marker by EBL in the negative type resist nLOF 2000 series.
During EBL an electron beam is accelerated down a column and focused by electrostatic and electromagnetic lenses. The fine focus is done near the end of the column. For the pattern definition a focused electron beam interacts with resist, coated on a sample.
The resolution of the EBL is mainly limited by the resist chemistry, the diameter of the electron beam and the scattering of electrons in the resist and substrate. Scattering is an undesired process as electrons from the exposure of a structure also contribute to the exposure of the adjacent structures. This process is called proximity effect. Two scattering processes are responsible for the proximity effect:
In forward scattering the incident electron collides with an electron from the atom of the exposed material. Both electrons interact in an inelastic scattering event, that causes the incident electron to change the direction of the trajectory. The scattering angle is usually small.
In backscattering the electrons collides with the heavy nucleus which results in elastic scattering. This means, the incident electron changes its direction, possibly in a large angle. If the elastic scattering events occur in the substrate, the electron can even be backscattered into the resist, with a significant distance to the originally exposed area. Backscattered electrons also expose the resist that results in deviations from the dimensions and a reduced contrast between exposed and unexposed regions.

The LayoutBeamer software GenISys was used to convert the sensor pattern into a compatible file for the electron beam writer. The software also includes a function to correct the dose distribution for proximity effects, as

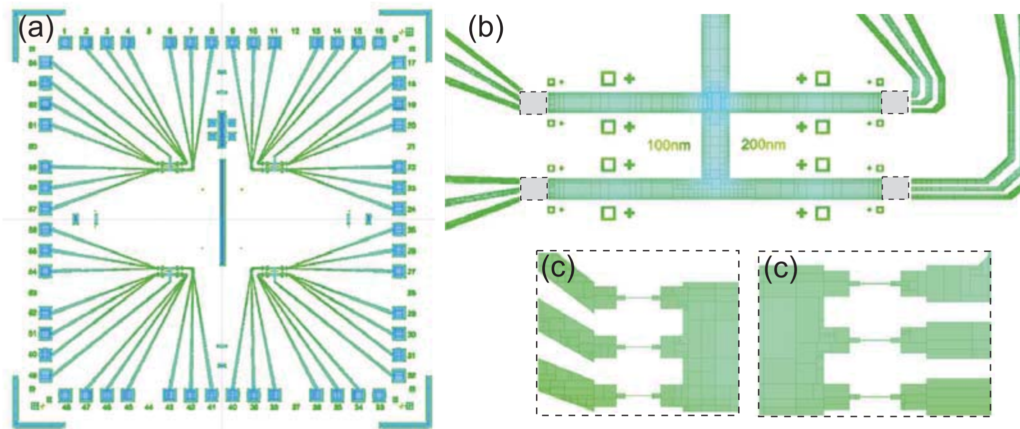


Figure 2.2: (a) Exposure dose distribution simulated with LayoutBeamer for the whole sensor design and corrected for proximity effects, which appear due to backscattered electrons, exposing adjacent regions. Blue colour represents a smaller dose, mainly used for the centre of large structures, such as contact pads and leads. (b) Large structures are exposed with a high beam current of 50 nA. Black squares indicate extracted regions which contain high-resolution structures in the design. (c) The pattern of extracted regions in Fig. b. includes fine structures, such as SiNWs which are exposed with a smaller beam current of 2 nA to achieve a higher resolution. Due to the narrow and isolated features of SiNWs it is not necessary to correct the exposure dose for proximity effects. Thereby the exposure dose is homogeneously distributed along the SiNW.

shown in Fig. 2.2. Mainly the dose distribution in large structures like the contact pads and leads was corrected in a way that the dose in the centre of large structures was reduced (Fig. 2.2 b). Narrow and isolated structures like the pattern of the SiNWs are not affected by the proximity effect correction (Fig. 2.2 c). Due to the proximity effect correction in large structures, the low exposure dose of 168 $\mu C/cm^2$ for nLOF in combination with a high beam current of approx. 50 nA it was feasible to expose with the electron beam writer on the wafer scale level.
Up to 28 devices, arranged in unit cells of 2 x 2 sensors as shown in Fig. 2.3 were exposed in one EBL step during three hours. The exposure of smaller structures such as shown in Fig. 2.2 c was more time consuming as the beam current was reduced to 2 nA to expose with a smaller beam diameter which is necessary for higher resolutions. After exposure, the nLFO resist was baked to finish cross-linking and developed. Only the cross-linked resist remained on the sample, acting as a mask for the following process step.

2.6 Dry and Wet Etching of the Sensor Pattern

The resist pattern, defined in nLOF by EBL, was transferred by reactive ion etching (RIE) into the 10 nm thick thermal SiO_2 layer. Typically, SiO_2 is etched with plasma gases containing fluorine. [57] The presence of fluorine

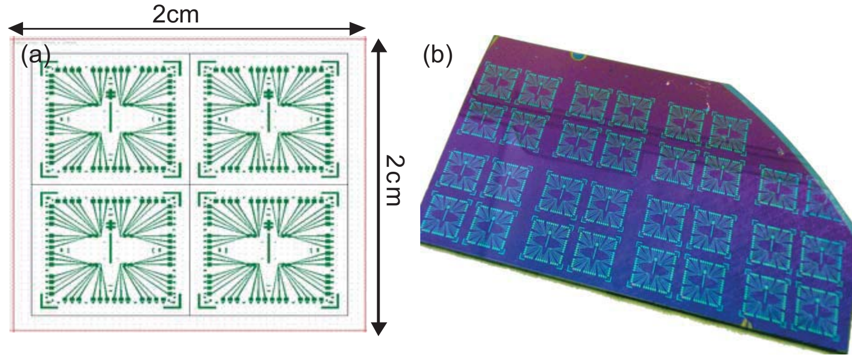


Figure 2.3: (a) Unit cell of 2cm x 2cm, containing 2 x 2 sensor designs. (b) Photograph shows wafer scale fabrication of seven unit cells (2 cm x 2 cm), resulting in 28 sensors. All unit cells were exposed in one lithography step.

forms fluorcarbon polymers during the etching process which deposit at the sample surface and passivate it. [57] (p.165). This hinders further chemical reactions. Fluorcarbon residues cannot be easily removed by plasma chemistry, but by sputtering process. [57] (p.167). Therefore, a gas mixture of CHF_3 and Ar was introduced for the SiO_2 etching. The additional Ar is a chemically inert gas, reacting neither with fluorcarbon residues nor with SiO_2. However, due to the applied voltage in the RIE chamber, the highly energetic and heavy Ar ions impinge the sample surface and remove material that is hit by the bombarding ions, comparable to a sputter process. Sputtering is a non-selective process and apart from the fluorcarbon polymers also the resist and the SiO_2 are attacked.

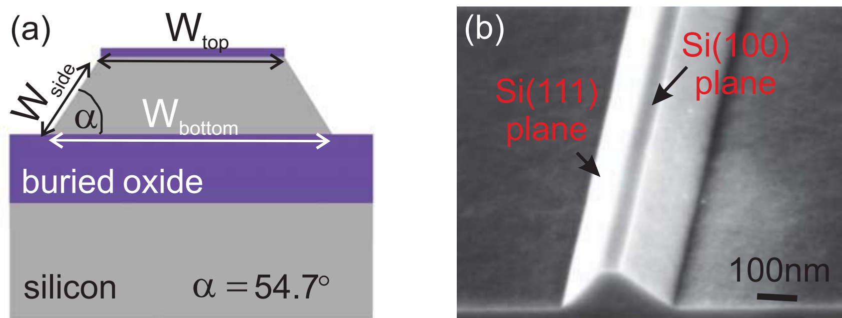


Figure 2.4: (a) Schematic cross-section of a wet etched SiNW fabricated from a (100) silicon on insulator (SOI). It shows the top and bottom width of the SiNW, W_{top} and W_{bottom}, respectively. The sidewalls are denoted as W_{side}. (b) Scanning electron micrograph shows the cross-section of a wet etched SiNW. The arrows indicate the Si (100) plane on top and the SiNW walls fromed by Si (111) planes.

Then the sample was dipped in buffered hydrofluoric acid for a few seconds to remove the remaining oxide. Directly afterwards the Si was wet chemically etched in tetramethylammonium hydroxide (TMAH) and 10 vol.% iso-

propanol (IPA). During this step, the patterned SiO_2 served as etch mask. The additional IPA in the etchant supported a smooth etching of the surface planes. nLOF resist could not be used as mask material for the wet etching of Si as nLOF is not resistant to basic solutions, such as TMAH. The wet etching of Si depends on the crystallographic orientation of the silicon planes, known as anisotropic etching. The Si(111) planes are etched about 100 times slower than other planes, resulting in a trapezoidal shape of the nanowire cross-section. The Si(111) planes form the side walls of the SiNWs under an angle of 54.7 ° with respect to the Si(100) plane. [56] (p.168) (Fig. 2.4 a-b). In the following, the width of the SiNW will be referred to as the top width W_{top}, as illustrated in Fig. 2.4 a. As the design is orientated along the Si <110> direction, the underetch of the SiNWs was negligible, leading to structure dimensions in conformity with the design as shown in Fig. 2.5 a-d.
An alternative to the wet etching of the SiNW is the reactive ion etching. This approach was not pursuit as it was shown by Ref. [58] that reactive ion etching degrades the device performance.

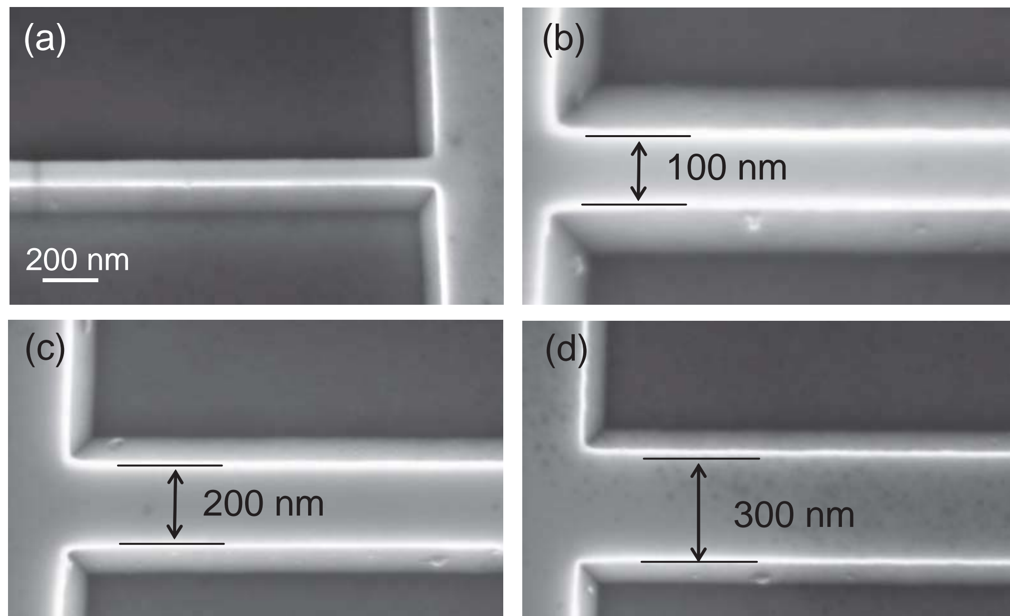


Figure 2.5: (a-d) Scanning electron micrograph of wet etched SiNWs from a tilted and a top view with widths ranging from W_{top}=100 nm to 300 nm.

2.7 Source-/and Drain Contact Implantation

In the following step, source and drain contacts were formed. To form contacts to Si the number of free charge carriers in Si has to be increased. In our

case, this was achieved by implanting doping ions into Si (see section 1.1). During implantation the whole sample was exposed to the ion beam. We intended to implant only the selected area of the source/drain contacts and contact leads. The area which should not be implanted had to be protected by an implantation mask. As mask material we used the positive tone resist poly(methyl methacrylat) PMMA, patterned by EBL in an overlay exposure, according to the design of the source and drain contact pads and contact leads shown in Fig. 2.1.
Implantation energy, penetration depth of ions and the PMMA thickness required for a substantial masking effect were simulated with the open-access software package SRIM (stopping and range of ions in matter) [59]. The implantation profile is shown in Fig. 2.6. It shows that an energy of 43 keV is required to implant BF_2^+ ions into the 85 nm thick Si device layer with 10 nm SiO_2 on top. The implantation dose was $2.3 \cdot 10^{15}$ atoms/cm^2. The 10 nm of SiO_2 remained on the sample to reduce channeling effects.
Channeling of doping ions can occur due to the crystalline structure of Si. It means, that ions travel along a crystallographic direction, e.g. the Si <100> direction, where they collide nearly elastic [60, 61]. The small energy loss causes ions to travel long distances and they stop mainly due to electronic drag. The uncontrolled travel leads to considerable differences in the implantation depth. Methods to reduce channeling effects are to deposit a thin oxide, causing a scattering collisions of the ions before entering the lattice, or to implant off-axis, at an angle of 7 ° between the ion implantation direction and the surface normal. [61] To ensure that the doping ions stop in the Si device layer both methods were used.
As doping ions we used the compound of boron with fluorine. In fact, only boron increase of the number of free charge carriers in Si. However, the compound makes the doping ion heavier and heavy ions knock Si atoms easily out of the lattice and make the implanted area amorphous. The high degree of amorphization is needed for the electrical activation of the doping ions, as they can only contribute to conduction, if they replace a Si atom in the crystal lattice (see section 1.1).
Fig. 2.7 shows a scanning electron micrograph of the sample after implantation. The dark regions inside of the Si contact leads indicate the amorphous region, which are damaged during the bombardment with doping ions.

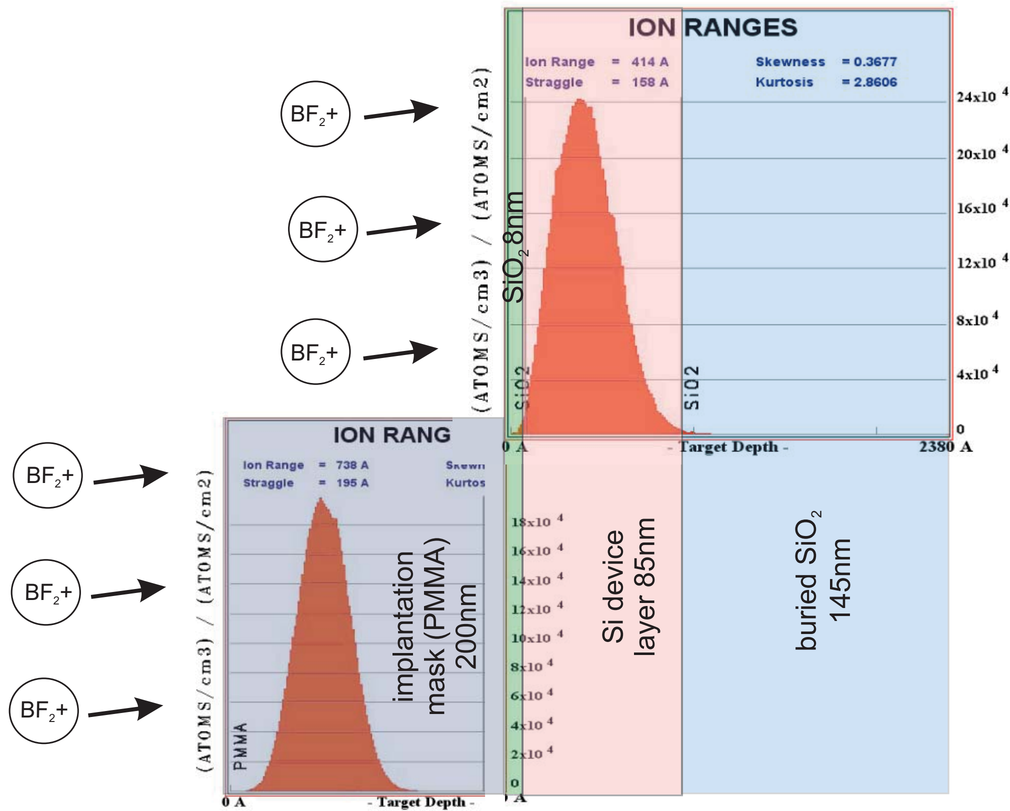


Figure 2.6: Stopping and range of ions in matter (SRIM) simulation shows the implantation profile of BF_2^+ doping ions, having an implantation energy of 43 keV. The y-axis shows (atoms/cm^3) / (atoms/cm^2) and multiplied by the implantation dose (atoms/cm^2) it gives the ion concentration (atoms/cm^3). The x-axis shows the penetration depth in the target. The simulation shows that an energy of 43 keV is required to implant BF_2^+ ions into the 85 nm thick Si device layer. The 10 nm thick thermal SiO_2 layer on top of the Si device layer avoids a channeling of doping ions. In PMMA resist the doping ions reach a penetration depth of 200 nm. To achieve that only source/drain contacts and contact leads became implanted, a PMMA implantation mask covered regions, such as the SiNWs which had to retain the original doping concentration. The simulation shows that a PMMA thickness of 200 nm is sufficient to prevent ions penetrating into the Si device layer.

2.8 Thermal Activation of Dopants

The electrical activation of dopants requires a thermal annealing, as dopants can only contribute to the electrical conductance if they replace a Si atom in the crystal lattice. The annealing temperature provides energy to repair the implantation damage by recrystallization of the amorphous regions. During recrystallization, dopants diffuse through the material in order to find an appropriate site to replace a Si atom in the crystal lattice. To estimate the distance over which the dopants diffuse we use following equa-

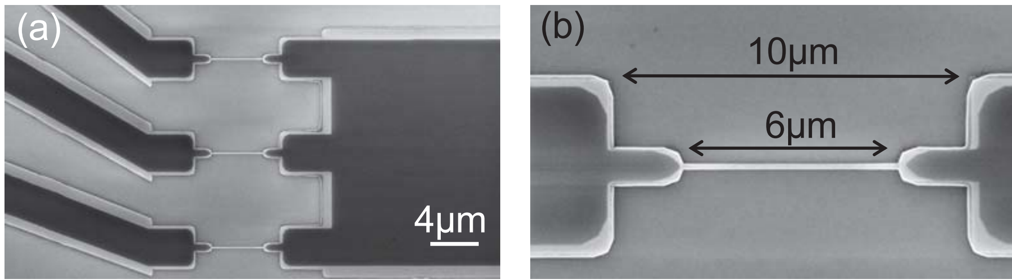


Figure 2.7: (a-b) Scanning electron micrographs show SiNWs connected to implanted source and drain contact leads. The dark pattern indicates amorphous regions due to implantation damage. SiNWs are not implanted.

tion: $L = 2\sqrt{Dt}$ [62], where L is the diffusion length, t the annealing time and D the diffusion constant. D depends on the temperature as follows: $D(T) = D_0 exp(-E_A/k_b T)$. [62] D_0 is the diffusion coefficient, E_A is the activation energy, T the temperature and k_B the Boltzmann constant. D_0 and E_A are influenced by the dopant concentration and the implantation damage.
The samples were annealed in a rapid thermal annealing (RTA) oven at 950 ° C in forming gas atmosphere for 6 minutes. Using values for D_0 and E_A from Ref. [62] in combination with the used process parameters, a diffusion length of 22 nm is estimated in crystalline Si. In amorphous regions the diffusion length increases to 930 nm. In fact, the equations provide an approximation between the real and the estimated diffusion length. However, the result implies that the diffusion length is much closer to the smaller value of 22 nm for dopants diffusing away from the implanted area in crystalline regions - without damages. Thus, we assume that SiNWs retained the original resistivity.
During the annealing step the fluorine volatilized.

2.9 ALD Deposition of Gate Oxide

Following thermal activation of dopants, the whole sample was covered with the gate oxide, grown by atomic layer deposition (ALD) which is known for a conformal coating, with a high quality thin film and a low pin hole density. The atomic layer-by-atomic layer deposition allows a precise control of the film thickness. [63] We could select between two high-k oxides, Al_2O_3 and HfO_2. The term high-k refers to the dielectric constant k which is higher than 3.9 for SiO_2. Further advantage of HfO_2 is its chemical inertness to acidic or basic solutions, apart from hydrofluoric (HF) acid based solutions. Directly, prior to the ALD deposition the samples were cleaned according to the Radio Corporation of America (RCA) cleaning procedure [64, 65]

(see appendix C), starting with a Piranha etch to remove organic contaminants, followed by standard RCA 1 and 2 cleaning to remove organic and metallic contaminants, respectively. [56] Between the Piranha and the RCA 1 cleaning the samples were immersed in buffered hydrofluoric acid to remove the thermal oxide, used as etch mask and screening oxide during the implantation. After the standard RCA 1 cleaning the samples were dipped again in buffered hydrofluoric acid to remove the native oxide that formed in the cleaning bath due to the oxidizing nature of the chemicals. No further buffered dip was done after the standard RCA 2 cleaning.

2.10 Contact Metallization and Annealing

To complete the contact fabrication the pattern of the contacts was defined by optical lithography in the nLOF series 2000 resist.
Optical lithography uses UV light and a photomask for the exposure of resist. The image is produced on the sample as the light transmits transparent areas on the photomask but it is blocked by the opaque ones. [56] (p.17).
The pattern was aligned by markers designed for optical lithography, typically in a cross-shape as shown in Fig. 2.1 c. The optical lithography markers were fabricated into the Si device layer in the same process steps as the sensor pattern (see section 2.5, 2.6).
Following the lithography, contact windows in the ALD gate oxide were opened by buffered HF etching. The etch rate of Al_2O_3 is comparable to that of thermal SiO_2, whereas HfO_2 etches 14 times slower. Directly after etching, the opened contact windows were metallized with 300 nm Al-Si(1%) in a lift-off process.
The formation of the ohmic contacts was completed in a thermal annealing process in forming gas at 450°C. In the same step the ALD oxides were also post annealed. It is known that the post annealing of the ALD oxides in forming gas has the effect to reduce the density of interface states, D_{it} as they are passivated by hydrogen. [66] Also the dielectric constants of the oxides are influenced as the oxide structure changes from amorphous to (poly)-crystalline, according to the annealing temperature (appendix A). However, the ALD oxides have a large excess of O_2 as they are grown in an oxygen-rich environment. Therefore, there is the risk that during the post annealing the excessive O_2 diffuses to the Si where it leads to a growth of the interfacial SiO_2 layer [66, 67] that already formed between the Si substrate and the ALD oxide during the ALD deposition. [66] The smaller dielectric constant of 3.9 for SiO_2 will reduce the total dielectric constant of the ALD layer.

2.11 Bonding and Packaging

The metallized contact leads were electrically isolated to the environment by the negative, epoxy type resist SU-8, patterned by optical lithography. Only the area of the SU-8 channel, aligned perpendicular to the SiNWs, is exposed to the environment as shown in Fig. 2.8 a-b.
Afterwards the sample was diced in chips of 9 mm x 9 mm. The chips were then glued in a chip carrier with silver paste and wire bonded to create the electrical connection between the sample and the chip carrier (Fig. 2.8 d). The wire bonding was a critical step as the bonding force has to be moderate to avoid damaging of the buried oxide by the bonding tip, which would result in leakage currents. On the other hand the applied force has to be strong enough to form a bond between wire and contact pad.
In a final step the contact pads and the bonding wires were sealed with epoxy. Optionally, a polydimethylsiloxane (PDMS) microfluidic system was integrated on top of the sensors, with microchannels aligned vertically to the SiNWs as shown in Fig. 2.8 c. The latter step was done by the group of Prof. Dr. Christian Schönenberger.

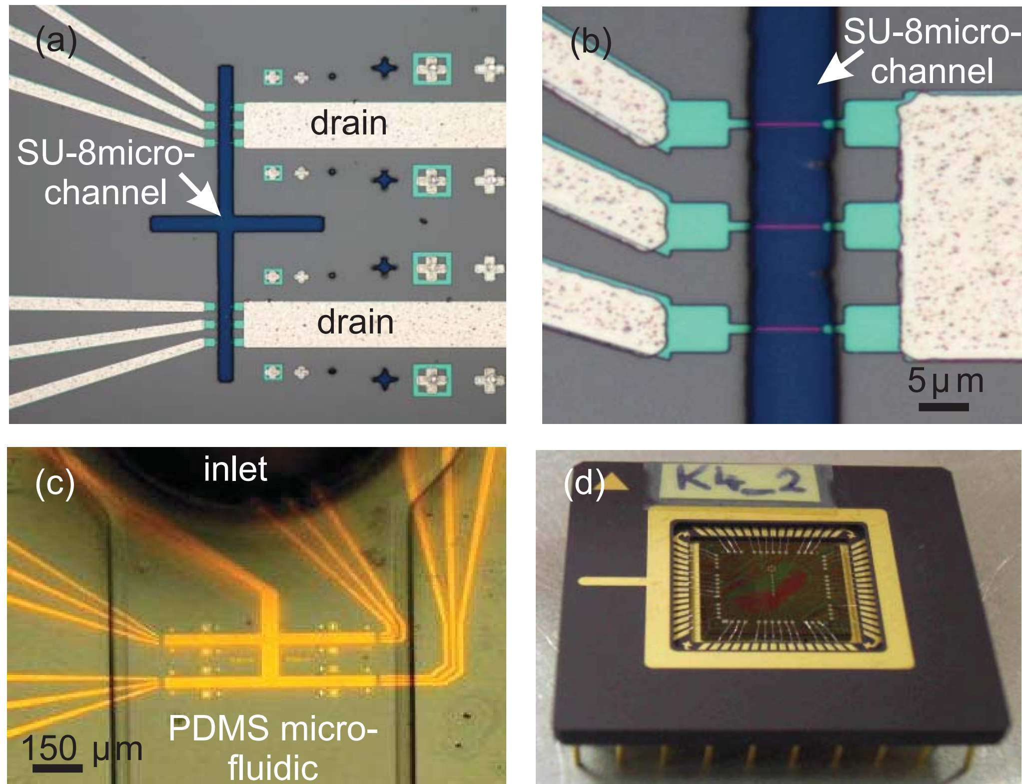


Figure 2.8: (a) Optical microscope image shows SiNWs (W_{top}=100 nm) connected to the common drain and individual source contact. The contact leads are implanted and metallized with AlSi (white structures). The unmetallized part of the contact leads consists of highly doped Si with a thickness of 85 nm (green structure). The sample is covered with SU-8 apart from the vertical SU-8 microchannel, aligned on top of the SiNWs (blue structure). Only the area within the SU-8 channel is exposed to solutions. Crosses have the function of alignment marker for optical lithography. (b) Optical microscope image shows three SiNWs (red lines) connected to the source/drain leads and embedded in a SU-8 microchannel (blue structure). (c) Optical microscope image shows a 500 μm wide PDMS channel aligned on top of the SiNW sensor with a Si device layer of 65 nm (yellow structures). (d) SiNW chip is bonded to a chip carrier.

2.12 Process Flow

The process flow below shows the main process steps of the SiNW-ISFET fabrication, used in this work.

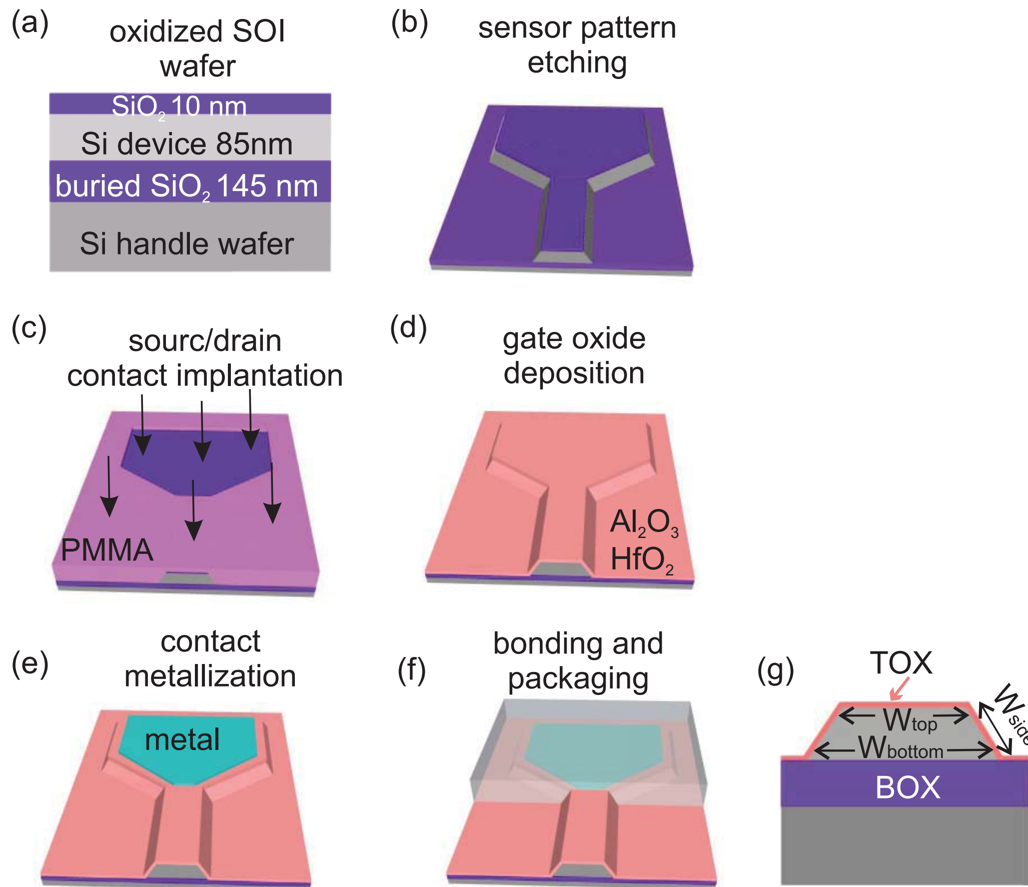


Figure 2.9: (a) Thermal oxidation of a silicon on insulator (SOI) wafer. (b) Pattern definition by electron beam lithography (EBL) and pattern transfer by riective ion etching (RIE) to the thermal oxide. The thermal oxide is used as etch mask for the wet etching of the Si device layer, defining the sensor. (c) Implantation of source and drain contacts with BF_2^+ ions. PMMA resist is used as implantation mask to avoid that regions different to contact pads and leads are implanted. After implantation, the doping ions are thermally activated. (d) Radio Corporation of America (RCA) cleaning of the sensor. Afterwards the sample is covered with Al_2O_3 or HfO_2 used as gate oxide, grown by atomic layer deposition (ALD). (e) Contact metallization with AlSi(1%) and annealing. (f) Bonding of the sensor to the chip carrier and implementation of the microfluidic. (g) Cross-section of a wet etched SiNW. It shows the top and bottom width of the SiNW, W_{top} and W_{bottom}, respectively. The width of the SiNW is referred to the top width W_{top}. The sidewalls are denoted as W_{side}. The top gate oxide and the buried oxide are denoted as TOX and BOX.

2.13 Challenges in the Fabrication Process

During the sample processing we encountered several critical fabrication steps. In the following section, a brief description of the challenges is given. 1. The first critical step is to transfer the sensor pattern into the Si device layer by dry and wet chemical etching (section 2.6). Here, the speciality is to avoid the formation of fluorcarbon polymers during the reactive ion etching of the SiO_2, as they mask the surface and avoid the wet chemical etching of the Si device layer. An example of a sample with a passivated surface is shown in Fig. 2.10.

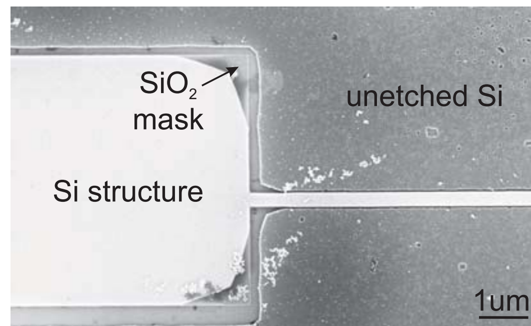


Figure 2.10: Scanning electron micrograph shows the failure to transfer the SiNW-ISFET into the Si device layer by wet chemical etching, as the surface is passivated by fluorcarbon polymers.

2. For the formation of Ohmic contacts (section 2.10) it is necessary to open contact windows in the ALD Al_2O_3 or HfO_2 layer that covers the whole sensor surface. Usually, the opening of the contact window is done by buffered hydrofluoric acid and especially the etching of HfO_2 is challenging due to the slow etch rate. Since the etch times are long, the resist has to adhere properly on the sample surface in order to ensure a selective etching. If the resist peels off, then the buried oxide will be etched by buffered HF, which results in an electrical short cut between the top and back gate.
3. At the end of the process line the wire bonding is the next delicate task (section 2.11). During bonding there exists the risk that the force of the bonding tip is too large and the tip penetrates the buried oxide layer. The damage of the buried oxide is irreversible and it causes an electrical short cut between the top and back gate.

2.14 Summary

Fabrication techniques such as electron beam and optical lithography, wet etching of the SiNWs and ion implantation of source drain contacts were used to process successfully SiNW-ISFETs from SOI wafers, following the

top down approach. The SiNW width ranged from 100 nm to 1 μm. As top gate oxide we used Al_2O_3 or HfO_2, grown by atomic layer deposition. The SiNW chip was packaged into a chip carrier (Fig. 2.8 d) and a PDMS microfluidic system (Fig. 2.8 c) was integrated on top of the SiNWs. Different PDMS microchannels allow to functionalize SiNW arrays with different receptors, which is required for multiplexed detections.

3 Characterization of Silicon Nanowire Sensors

In this chapter, the pH response of differently wide SiNWs, coated with Al_2O_3 or HfO_2 was studied. In terms of electrical performance the transconductance, mobility and subthreshold swing will be extracted and discussed. To determine the accuracy of the sensors a noise analysis was performed. Based on the acquired data the noise source was determined. Parts of this chapter are submitted for publication. [68, 69]

3.1 SiNW-ISFETs in Liquid Environment

3.1.1 Measurement Setup

Fig. 3.1 a-d shows the main elements of the measurement setup used to perform experiments with the SiNW sensor in liquid environment. A standard pH buffer solution (Titrisol, Merck) was used as analyte and pumped to the liquid cell (Fig. 3.1 c), that contained the SiNW chip mounted on a printed circuit board (Fig. 3.1 d). The liquid cell also accommodated a calomel reference electrode and a liquid gate electrode in form of a platinum wire, immersed in the buffer solution. The device was operated at a source-drain voltage V_{sd} of 0.1 V and the conductance G through the device was measured. The conductance was modulated by a top liquid gate voltage V_{lg} that was applied to the platinum wire. This is known as liquid gating.

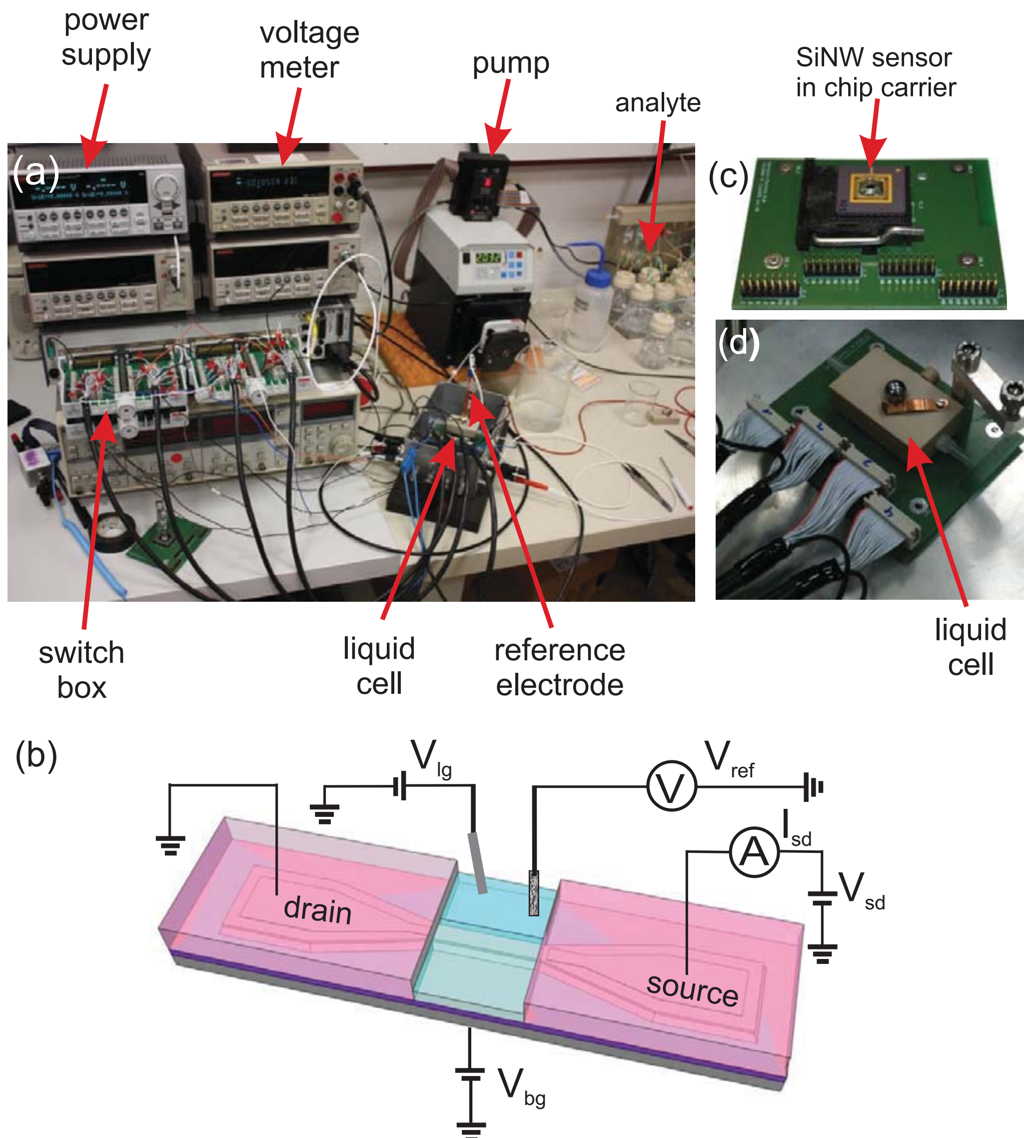


Figure 3.1: (a) Measurement setup in Basel. The instruments were controlled by a LabView program to run measurements automatically. 48 SiNWs could be addressed individually and automatically by the switch box and ten different analyte solutions could be pumped automatically to the liquid cell. (b) Schematic view of the measurement setup. The source-drain voltage V_{sd} sent a source-drain current I_{sd} through the SiNW. The conductance of the SiNW could be modulated by a voltage applied to the liquid gate V_{lg} or to the back gate V_{bg}. The calomel reference electrode measured the actual potential V_{ref} in the liquid. (c) SiNW embedded in a chip carrier that is mounted on the printed circuit board. (d) Liquid cell contained inside the chip carrier with the SiNW sensor. (Figure a,c and d by courtesy of group of Christian Schönenberger)

The calomel reference electrode measured the effective potential V_{ref} in the buffer solution. Additionally, a back gate voltage V_{bg} could be applied to the back side of the sample to modify the conductance. The measurement setup was controlled by a LabView program, which allowed to address 48 SiNWs

individually by a switch box, to change pump valves automatically and to transport the analyte solution to the sample.

3.1.2 Electrical Characterization

The transfer characteristics of SiNW sensors was mainly characterized in liquid environment, since this is the standard operating condition. Fig. 3.2 shows the transfer curve from a SiNW (W_{top}=1 μm, Fig. 2.4) with the conductance G on a linear and logarithmic presentation vs. the gate voltage V_{ref} in the solution. The transfer curve was measured at a fixed source-drain voltage V_{sd}=0.1 V in a buffer solution of pH 8. The SiNWs has a low p-type doping, which means holes are the free charge carriers and contribute to the conductance. As a negative gate voltage V_{ref} is applied, the electric field attracts holes in the SiNW and thereby increases the conductance. As the SiNW is lightly p-doped, the device operates in accumulation.

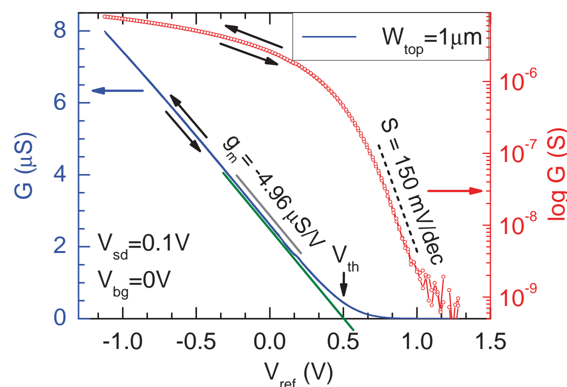


Figure 3.2: Transfer curve with conductance G on the linear (blue) and logarithm scale (red) vs. reference voltage V_{ref}, measured with a SiNW with W_{top}=1 μm at V_{sd}= 0.1 V in pH 8 solution. The grey line shows the transconductance g_m=dG/dV_{ref}. The dotted line indicates the subthreshold swing S extracted from the linear regime on the logarithmic scale. V_{ref} is changed in forward and backward direction, as indicated by the black arrows next to the curves. The hysteresis is $<$ 5mV. The solid line is an extrapolation of the conductance fit line. The intersection with the voltage-axis defines the threshold voltage V_{th}.

Based on the conductance, presented on the linear and logarithmic scale, several transistor parameters can be extracted. The logarithmic representation has the advantage that it clearly displays the subthreshold current. The slope of the line in Fig. 3.2 (dashed line) is called the subthreshold swing S and it gives the gate voltage, needed to change the conductance by one decade. The thermal limit of $ln(10)k_BT/e$ = 60 mV per decade at 300 K cannot be defeated by transistors, without tunneling conductance. Typically, the subthreshold swing of the fabricated sensors had a range between 120

and 180 mV/dec. In Fig. 3.2 the subthreshold swing is 150 mV/dec. The logarithmic presentations also reveals an on-off-current ratio I_{on}/I_{off} of 10^4. From the linear regime the threshold voltage V_{th} can be determined by the classical method, which means extrapolating the linear conductance fit to the gate voltage axis. The intercept of the fit with the voltage axis gives the threshold voltage, in our example the threshold voltage $V_{th} = 0.5$ V. Moreover, the transconductance $g_m = \partial G/\partial V_{ref}$ can be extracted from the linear regime which amounts to 5 μS/V in Fig. 3.2.

SiNW-ISFETs with different SiNW Widths and Gate Oxides

In this section, we present a systematic study on the transconductance of SiNWs with different widths and with Al_2O_3 or HfO_2 as gate oxide. The findings will be needed for a comparison of the pH response of differently wide SiNWs in the linear regime (see section 3.1.3).
A comparison between different SiNW widths requires a normalization of the conductance, because the conductance changes with the SiNW size and shape [70, 71], as illustrated in Fig. 3.3 a for two SiNWs with W_{top} of 100 nm and 1 μm . Different methods could be assumed like normalization by the cross sectional area of the wire, by the top width W_{top}, by the top perimeter $W_{eff} = W_{top} + 2W_{side}$, the bottom width W_{bottom} (Fig. 2.4), or even the full perimeter of the wire $W_{eff} + W_{bottom}$. It is not clear a priori which method is the best. However, as we can gate the SiNW asymmetrically and thereby accumulate more carriers at the top surface as compared to the bottom surface, or vice versa, we assume that the current scales with the top perimeter (Fig. 2.4)

$$W_{eff} = W_{top} + 2W_{side} \tag{3.1}$$

This assumption is motivated by the gating scheme via the liquid gate (top gate), which is used in the experiments in this work (V_{bg}=0V). It is further justified, because the electrolyte is in contact simultaneously with both the top and the side face.

In Fig. 3.3 b the transfer curves normalized by W_{eff} are shown for two SiNWs with W_{top} of 100 nm and 1 μm at different pH values. The linear regime of both normalized transfer curves are very similar, which indicates an identical scaled transconductance for different SiNW widths.
Moreover, the scaled transconductance values for a set of SiNWs with different W_{top} and HfO_2 or Al_2O_3 as gate oxide are shown in Fig. 3.4. The error bars result from an average over two SiNWs with an equivalent W_{top}. All SiNWs show a similar scaled transconductance, independent of the SiNW

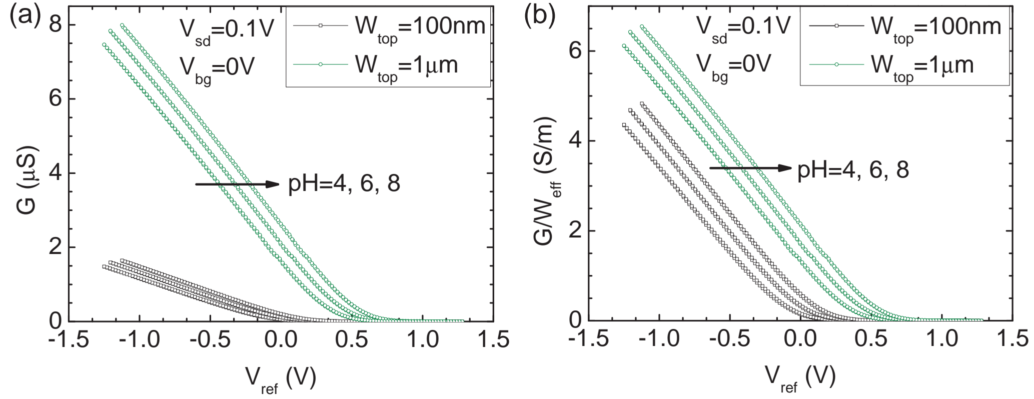


Figure 3.3: (a) Transfer curve of two SiNWs with W_{top}=100 nm and 1μm, covered with 20 nm Al_2O_3 and measured at pH 4, 6 and 8. The SiNW with W_{top}=100 nm has a smaller transconductance g_m, compared to the larger SiNW. (b) Transfer curve of SiNW shown in (a), with conductance G normalized by $W_{eff}=W_{top}+2W_{side}$. The normalized transconductance of both SiNWs is similar.

width.
Although the scaled transconductance values are constant for SiNWs of different widths, we have to understand the different g_m/W_{eff} values for different top oxides. In the linear regime, g_m is determined by the mobility μ of the charge carriers and the liquid gate capacitance per unit area, $C_{lg}^{\square}$:

$$g_m = \mu C_{lg}^{\square} W_{eff}/L. \tag{3.2}$$

Here, L denotes the length of the SiNWs, which was constant for all wires. We assume, that for one sample the mobility is constant for all wires of different widths, as it is indicated by the constant value of the scaled transconductance. Sample to sample variations in the mobility may still occur in the fabrication process.
Therefore, the scaling of g_m with W_{eff} will then equally be reflected in the capacitance. As a consequence, the value of the scaled transconductance g_m/W_{eff} should be determined by C_{lg}. The liquid gate voltage is applied to the SiNW through the liquid via the top oxide (TOX) (Fig. 2.9). It therefore involves the double layer C_{dl} in the electrolyte and the top oxide capacitance C_{TOX} connected in series. Due to the high ion concentration in the electrolyte of 67 mM, we have $C_{dl} \gg C_{TOX}$. In the series connection this leads to $C_{lg} \approx C_{TOX}$ and

$$g_m/W_{eff} = \mu C_{TOX}^{\square}/L. \tag{3.3}$$

where $C_{TOX}^{\square}$ is the top oxide capacitance per area.

Looking at Fig. 3.4, one would naively expect a factor of two difference

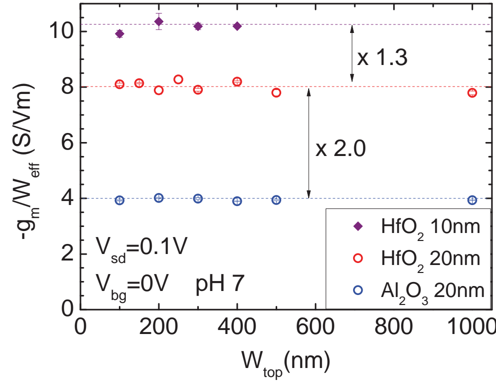


Figure 3.4: Transconductance normalized by W_{eff} for SiNWs with W_{top} ranging from 100 nm to 1 μm. The SiNWs are covered with either 10 or 20 nm HfO_2 or 20 nm Al_2O_3. Due to the high ion concentration in the electrolyte the double layer capacitance can be neglected. Thereby, the transconductance reflects the top gate oxide capacitance. Since the dielectric constants are thickness-dependent, the transconductance of the 10 and 20 nm HfO_2 changes by only a factor of 1.3, instead of 2.

between the measured g_m/W_{eff} values for the HfO_2 samples with 10 and 20 nm thickness. Instead, we obtained a value of 1.3.
To resolve this discrepancy we determined the dielectric constants ε_r by capacitance-voltage (C-V) spectroscopy. The HfO_2 layers were grown and characterized in the group of Prof. Dr. Adrian Ionescu from EPFL (École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland). Dielectric constants of 12 and 17 for HfO_2 layers with 10 and 20 nm thickness, respectively were obtained. The 20 nm thick Al_2O_3 layer had a dielectric constant of $\varepsilon_r \sim 7.0$. Our results are comparable to reported values of ε_r = 10-18 [72] and ε_r = 4-10 [67] for HfO_2 and Al_2O_3, respectively.
From our C-V measurements we see that the dielectric constants are thickness dependent as suggested by the g_m values of the HfO_2 data in Fig. 3.4. The reason for this might be the presence of an interfacial SiO_2 layer of max. 2 nm that grows during the ALD process [66] between the silicon substrate and the ALD oxides. It reduces the dielectric constant of the total layer, according to the series capacitance of the SiO_2 and the ALD oxide layer.
Knowing the dielectric constants of HfO_2 layers we estimated a C_{TOX} capacitance ratio of 1.4 between the 10 and 20 nm thick HfO_2 samples. Indeed, this result shows, that we cannot expect a factor of two difference in the measured g_m/W_{eff} values in Fig. 3.4. The slight discrepancy between the C_{TOX} capacitance ratio which amounts 1.4 and the ratio of 1.3 for g_m/W_{eff} can be attributed to slight differences in the mobility between both samples. Based on our data we estimated a mobility of 58 and 62 cm^2/Vs for the 10 nm and 20 nm thick HfO_2 samples, respectively. For the Al_2O_3 sample

we obtained an estimated hole mobility of 75 cm^2/Vs. The mobility values are in good agreement with reported hole mobilities for SOI wafers in accumulation mode (50-139 cm^2/Vs) [15], with similar doping concentrations. The slightly reduced mobility observed in both samples covered with HfO_2 is in agreement with previous results in the literature which report a mobility degradation in MOSFETs fabricated with high-κ materials. [32]

3.1.3 Impact of the SiNW Width on pH Sensing

Several publications addressed the topic whether the nanowire width [22, 15, 73, 74] or thickness [75, 76] has an influence on the pH response, however with inconsistent results. An influence of the SiNW width on the response in pH sensing experiments has been shown in Ref. [73, 74]. Elfström et al. [73] observed an increasing threshold voltage shift for a decreasing SiNW width. No pH response was found for SiNW widths $>$ 150 nm. Vu et al. [22] reported preliminary results for single 80 nm and 400 nm wide wires which exhibit the same threshold voltage shift of 41 mV/pH.
Moreover, the ideal working point showing the highest pH response is also a controversial discussion in the literature. Gao et al. [47] demonstrates an enhancement of the pH response in the subthreshold regime compared to the linear regime, whereas preliminary results in Ref. [22] suggest the same pH response in both regimes.
To clarify these disagreements, we explored in a systematic manner the influence of the SiNW width of SiNW-ISFETs on the pH response with widths ranging from 1 μm down to 100 nm in both operating modes, the subthreshold and the linear mode. In addition, we study the sensing properties of the SiNW-ISFET coated with Al_2O_3 and HfO_2 grown by atomic layer deposition (ALD). The pH sensing data was acquired with the measurement setup illustrated in Fig. 3.1.

Fig. 3.5 shows the conductance G on a logarithmic scale as a function of the reference voltage V_{ref} for SiNWs with W_{top} of 100 nm and 1 μm at different pH values. The transfer curves shift to more positive V_{ref} values if the pH is increased, which is in agreement with the site-binding model. [36] In this work, to determine the pH response, we do not extract the threshold voltage V_{th} according to one of the classical methods [30], as we are not interested in the absolute V_{th} values. It is sufficient to know the relative shift of the transfer curves. Therefore, we defined V_{th} as the reference potential V_{ref} at any source drain conductance value in the subthreshold regime. In our experiments, this value was 20 nS as indicated by the dashed line in the semi-logarithmic plot of Fig. 3.5. Consequently, the threshold voltage shift ΔV_{th} was replaced by ΔV_{ref}.

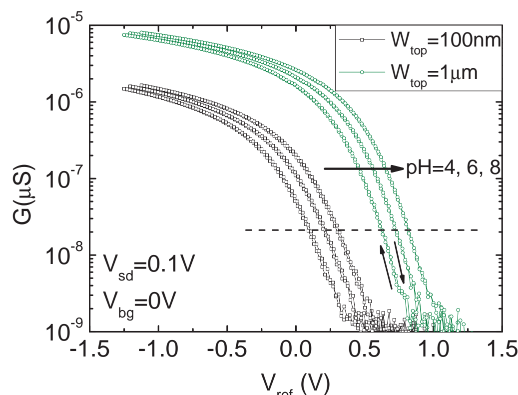


Figure 3.5: Logarithmic conductance G versus reference voltage V_{ref} for two SiNW (W_{top}=100 nm and 1 μm), coated with 20 nm Al_2O_3 and measured at pH 4, 6 and 8. The transfer curves shift to the right direction with increasing pH values, as predicted by the site-binding theory.

As an example, a set of V_{ref} values at 20 nS for different pH values are presented for four SiNW widths in Fig. 3.6 a.
The pH measurements were performed in buffer solutions with pH values ranging from 3 to 9 and from 3 to 10, for Al_2O_3 and HfO_2, respectively. For Al_2O_3 the highest pH value was 9, since the Al_2O_3 is etched at higher pH values. This limitation is not valid for HfO_2, due to its chemical inertness to acidic or basic solutions (apart from hydrofluoric (HF) acid based solutions), which makes HfO_2 a promising candidate for bio-sensing experiments. To conduct the experiment, we started with the buffer at pH 3 and exchanged sequentially the buffers with steps of ΔpH= 1, until the buffer with the highest pH value was reached. We then returned stepwise to pH 3.
As shown in Fig. 3.6 a, a linear dependence is found over the whole pH range. Moreover, a small negligible hysteresis in the forward and backward sweep of the pH values is observed. The slope of a linear fit to the data defines the pH response of the SiNW in mV/pH. These slopes are shown in Fig. 3.6 b for SiNWs with W_{top} ranging from 100 nm to 1 μm (Fig. 2.4). All SiNWs show an ideal Nernstian behavior of 60 mV/pH at 300 K, independent of the SiNW width and the investigated gate oxide types.

In an application it is convenient to measure a large conductance. Therefore it is beneficial to operate the ISFETs in the linear regime and not in the subthreshold regime as shown in Fig. 3.5. In the linear regime the measured signal is the conductance change $\Delta G(pH)$ at constant V_{ref}. It can be converted to a voltage shift ΔV_{ref} using the transconductance $g_m = \partial G/\partial V_{gate}$:

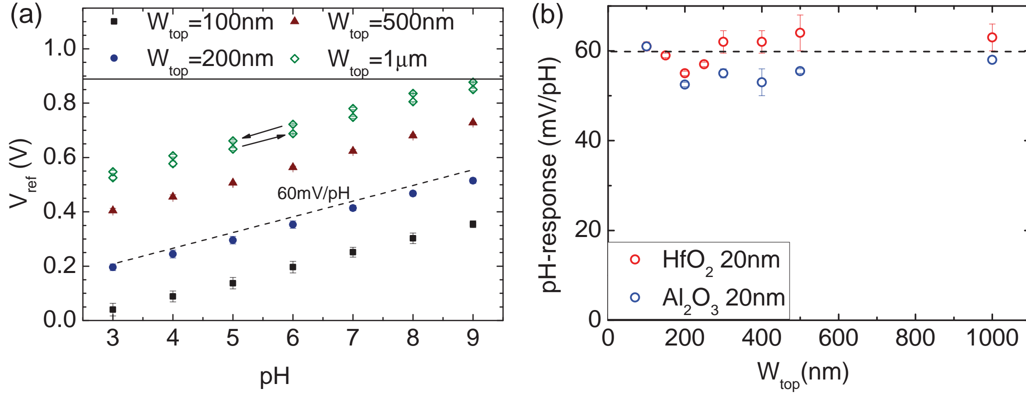


Figure 3.6: (a) The liquid potential V_{ref} extracted at 20 nS (Fig. 3.5 dashed line) is plotted as a function of pH. A linear dependence is found over the whole pH range. The pH response is defined by the slope of the best fit line. The SiNW with W_{top}=1 μm shows the pH response for pH values measured from 3 to 9 and back to 3 with a negligible hysteresis. (b) The pH response of SiNWs with W_{top} ranging from 100 nm to 1 μm is close to the Nernst limit of 59.5 mV/pH at 300 K (black, dashed line). An influence of the SiNW width or the investigated gate oxide types on the pH response is not observed.

$$\Delta G(pH) = g_m \Delta V_{ref}. \tag{3.4}$$

Since the voltage shift as a function of pH value (Fig. 3.6) and the normalized transconductance (Fig. 3.4) are the same for different SiNW widths, it is obvious from equation 3.4 that in the linear regime the pH response is also independent of the wire width.
Thereby, this systematic study demonstrates no influence of the operating regime and a clear absence of any size dependence on pH sensing properties of SiNWs.

In brief, the observed ideal pH response confirms recent results showing that ALD-grown Al_2O_3 [46] and HfO_2 [18] are excellent pH sensing interfaces, due to the high density of active surface groups that buffer the pH changes in the bulk solution. Within the site-binding model [36], this oxide property is called the surface buffer capacity. As long as the oxide-electrolyte interface of the surface of the SiNW provides a large surface buffer capacity for protons (equ. 1.30) no size dependence is expected. Our observation is therefore in strong contrast to the work by Ref. [73, 75, 76, 74]. Additionally, the results prove that one can fabricate SiNW sensors with ideal Nernstian behaviour with SiNWs down to 100 nm width and an operation in the linear and the subthreshold regime is favourable.

3.2 Quality Tests performed in Liquids and in Air

Prior to the experiments, the quality of the SiNW-ISFETs was tested, in terms of leakage currents, hysteresis, reproducibility and Ohmic contact characteristics.
The quality tests were carried out with the setup illustrated in Fig. 3.1 in liquid environment, but also with the SiNW-ISFET exposed to air. For measurements in air, the same setup was used, however, the liquid gate - including the liquid cell - was removed and the SiNW-ISFET was only gated by the back gate voltage. If the SiNWs was exposed to liquids, then the back gate voltage remained at a constant value and the liquid gate voltage was changed.

3.2.1 Leakage Currents

The operating tests include measurements of leakage currents. Leakage currents are unwanted effects as the current takes paths different to the designated one which goes from the input contact through the SiNW to the output contact. In general, leakage currents result in a complete failure. In our SiNW sensor three leakage paths exist as illustrated in Fig. 3.7 a:
Path 1: leakage into the SiNW through the ALD oxide
Path 2: leakage into the SiNW through the buried oxide and
Path 3: short circuit between the liquid and back gate

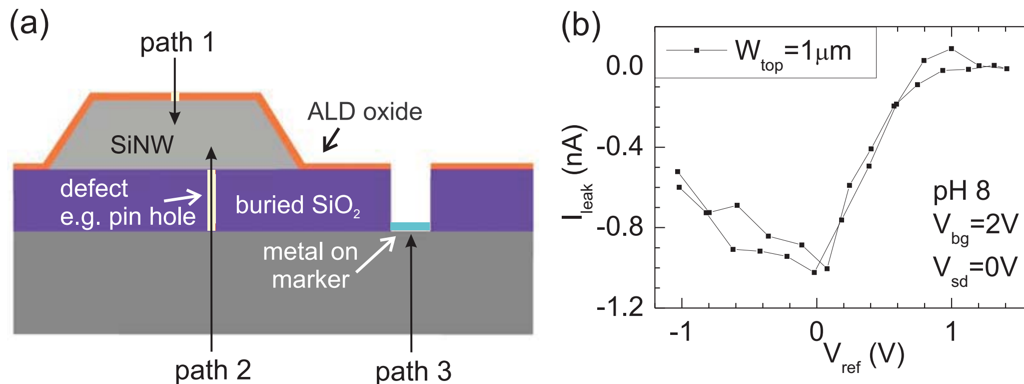


Figure 3.7: (a) Schematic view of three paths of leakage currents. Path 1 occurs if the ALD oxide has a defect. Path 2 can be found if the buried oxide fails e.g. by defects such as pin holes or due to damages during wire bonding. Path 3 can happen at the position of the optical alignment marker nearby the SiNWs. (b) Current vs. V_{ref}. V_{sd} is zero and no current flow through the SiNW is expected. The measured currents are leakage currents, taking path 1 and 2 in Fig. 3.7 a, due to the applied V_{ref} and V_{bg}. The max. leakage current of 1 nA is not critical, since I_{sd} is orders of magnitudes higher.

The first two cases occur, if one of the oxide layers has a defect, such

as pin holes. Additionally, the back gate oxide can be damaged during the contact bonding, if the applied force of the bonding tip is too strong, when it forms the bond at the contact pad. If the force is too strong, the tip will penetrate through the SOI layers and damage the buried oxide.
The third leakage current path can be encountered when both, the ALD and the buried oxide layers are etched at the position of markers used to align the optical lithography (Fig. 2.1). These markers are very close to the SiNWs and also exposed to the liquid gate. A complete etching of both oxide layers results in a short circuit between the liquid and the back gate.
The ALD oxide at the marker position can be completely etched, when the source/drain contact windows are opened by buffered HF acid. If the etch time is exceeded, then the acid will continue to etch the buried oxide.

Fig. 3.7 b shows the current I_{leak} into the SiNW. V_{sd} is zero and thus no current is supposed to flow through the SiNW. However, when applying a back gate or liquid gate voltage a leakage current can flow into the SiNW, if the ALD or the buried oxide is defect (path 1 or 2 in Fig. 3.7 a). The detected leakage current of max. 1 nA can be tolerated, as the source drain current I_{sd} is orders of magnitudes larger. To check for short circuits between both external gates (path 3 in Fig. 3.7 a), we monitored, if the measured reference potential V_{ref} corresponds to the applied liquid gate voltage V_{lg}. A voltage off-set identical to the applied back gate voltage would indicates that there is no isolating oxide underneath the alignment marker and both gates would be short circuited.

3.2.2 Transfer Curves: Reproducibility and Hysteresis

Reproducibility describes the ability to obtain the same experimental results "with the same method on identical test material, but under different conditions" [77] such as "different operators, different apparatus or after different intervals of time". [77] Only reproducible data sets are reliable to confirm findings.
For our sensor platform with 48 SiNWs the reproducibility of electrical properties is crucial for further experiments, especially for differential measurements, as discussed in section 4. Reproducibility and hysteresis are tested with the SiNWs in liquid environment and air.

Fig. 3.8 a and b show transfer curves, measured with three different SiNWs with W_{top}=1 μm, integrated on the same sensor chip. In Fig. 3.8 a the SiNW was measured in air and controlled by the back gate, whereas in Fig. 3.8 b the conductance was controlled by the liquid gate in liquid environment.
In both diagrams, the transfer curves are aligned on top of each other,

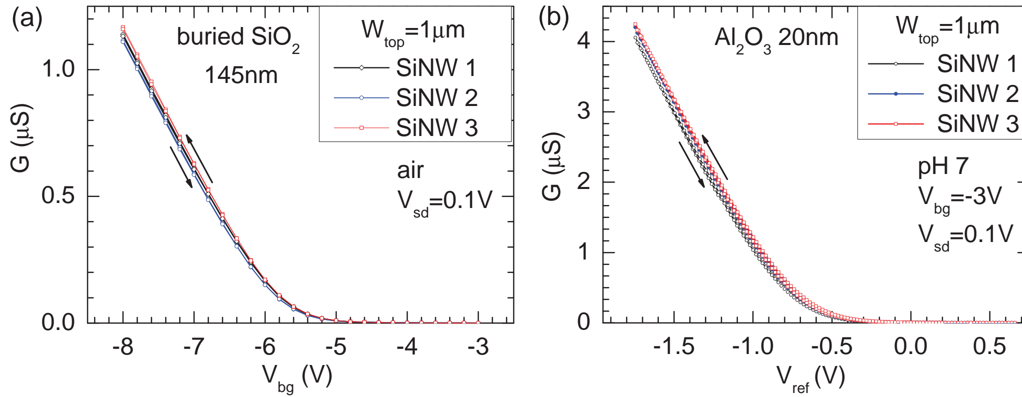


Figure 3.8: (a-b) Transfer curves of three 1 μm SiNWs. The curves are aligned on top of each other, demonstrating an excellent reproducibility. The black arrows indicate that the transfer curves are measured in the forward and backward gate direction. The hysteresis is very small with max. 5 mV. (a) Transfer curves measured in air and gated through the buried back oxide. (b) Transfer curve measured in pH 7 and gated through the ALD top oxide.

demonstrating excellent reproducibility. The transfer curves were measured in a forward and backward gate direction, as indicated by the black arrows. The curves in both direction are identical due to the small hysteresis, amounting to max. 5 mV. These results proves the high electrical quality of the device.

3.2.3 Ohmic Contact Characterization

An Ohmic contact is a highly conductive element formed from a semiconductor and a metal. The current through the contact is proportional to the voltage across it, according to Ohm‘s law. [28, 35](p.187,85).
We characterized the Ohmic contacts in air and therefore we measured the source-drain current I_{sd} vs. source-drain voltage V_{sd}, with the back gate voltage V_{bg} as a parameter. Two examples of the so-called output curves are shown in Fig. 3.9 a-b for a SiNW with W_{top}=100 nm and 500 nm. In both diagrams the curves show a nearly linear behaviour, which is typical for Ohmic contacts.

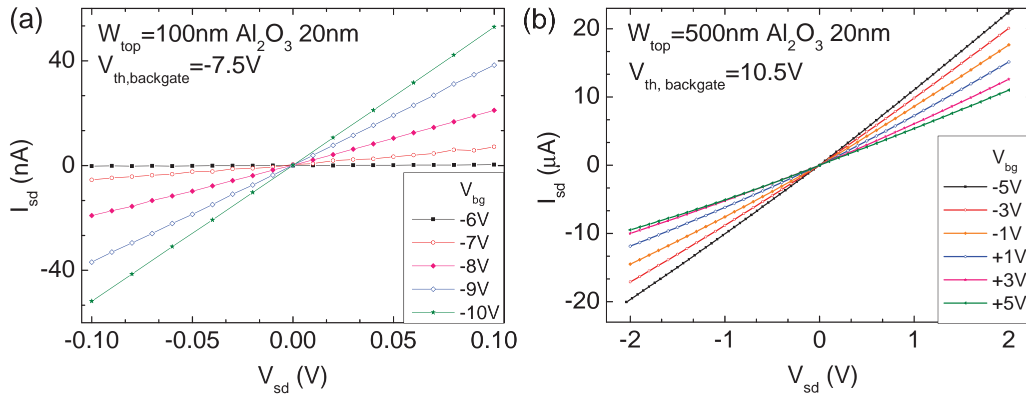


Figure 3.9: (a-b) Output curves with source drain current I_{sd} vs. source drain voltage V_{sd}, measured at different back gate voltages V_{bg}. In both diagrams is I_{sd} proportional to V_{sd}, which is characteristic for Ohmic contacts. (a) Output curve of a SiNW with W_{top}=100 nm. (b) Output curve of a SiNW with W_{top}=500 nm.

3.3 Noise Investigations

Additional to the sensor signal, noise is a fundamental issue, as it determines the resolution. Noise is the random fluctuation of the electrical signal over time and it can be observed in most conductive materials. In semiconductor devices a common type of noise is $1/f$ noise, also called flicker noise, caused by resistance fluctuations. $1/f$ noise is characterized by a power spectral density inversely proportional to the frequency f. In general, the resistance fluctuations are explained by two approaches: intrinsic resistance fluctuations in the channel or gate fluctuations, that are extrinsic. The latter originate from either trapping and detrapping of charge carriers near the semiconductor-oxide interface [48, 78, 79, 80, 58, 81] or from thermally fluctuating dipoles in the gate oxide. [51] The intrinsic resistance fluctuations are based on Hooge‘s empirical relation for $1/f$ noise. [52, 49, 82]
s Here, we compare experimental data of SiNW-ISFETs with these noise models in order to find out which model applies to the sensor. To investigate the $1/f$ noise source we analysed the gate referred voltage noise of SiNW-ISFETs with different gate capacitances and different widths in various physical environments. Our data suggests that tapping and detrapping of charge carriers at the gate is the dominant source of noise. Based on the data, we determined the sensor accuracy.

3.3.1 Measurement Setup

Fig. 3.10 presents a schematic view of the measurement set-up, used to perform the noise analysis. A DC source-drain voltage V_{sd} of 100 mV was applied and the conductance G through the nanowire was recorded. By applying a gate voltage, the SiNW-ISFET was adjusted to different conductance values, at which the time-dependent resistance fluctuations were measured and converted into a voltage fluctuation by a current-voltage amplifier. Via fast Fourier transform the time dependence was translated to a noise spectrum. In a dual-gate configuration the conductance can be modulated by a back gate voltage, V_{bg} or a liquid gate voltage, V_{lg}, applied to the backside of the handle wafer or to a Pt wire immersed in the pH buffer solution, respectively. A calomel reference electrode measured the actual potential, V_{ref} in the solution. The noise analysis was performed in a 67 mM pH 7 buffer solution (Merck), deionized water or in an argon/air atmosphere. When the SiNW-ISFETs were exposed to an aqueous media the device was controlled by the liquid gate voltage V_{lg}, whereas the sensor was gated by the back gate voltage V_{bg} in argon/air.

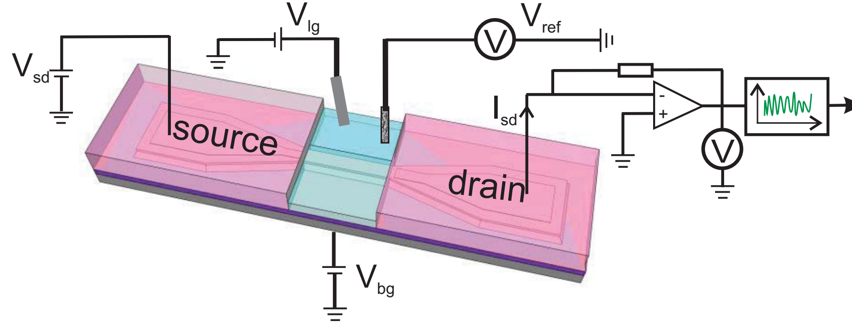


Figure 3.10: Schematic of the noise measurement setup showing the liquid gate and the back gate voltage, V_{lg} and V_{bg}, respectively. A calomel reference electrode determines the actual potential V_{ref} in the solution. A DC source drain voltage V_{sd} of 0.1 V is applied.

3.3.2 1/f Noise in SiNW-ISFETs

Fig. 3.11 a shows the transfer characteristics of differently wide SiNWs, e.g., the conductance G as a function of the gate voltage V_{gate}. The gate voltage was applied to adjust the SiNW-ISFETs to different conductance values along the transfer curve where simultaneously the noise analysis was performed. An example of a power spectral density of the voltage fluctuations S_V vs. frequency f obtained for a SiNW with W_{top}= 100 nm is shown in Fig. 3.11 b. In the analysed conductance regimes $S_V(f)$ follows the $1/f$ law at low frequencies, as indicated by the dashed line. The open squares show the experimentally obtained thermal noise for the SiNW gated to 321 kΩ. Thermal noise is not frequency dependent and therefore called *white* noise. The theoretical value of the thermal noise S_V=$4k_BTR$ [34] at 321 kΩ, where k_B is the Boltzmann constant and T the temperature is presented by the black line which agrees with the experimental data.

To determine the noise source we compared the data with three noise models. The trap state noise model and the dielectric polarization noise model are caused by gate fluctuations, which are extrinsic. Thereby the gate referred voltage noise S_{VG} is independent of the gate voltage. Formally, the gate referred voltage noise represents the external noise, that one would have to put on the gate to obtain the same source drain current noise. [50] In the trap state noise model, the origin of noise is a fluctuating charge carrier density in the gate oxide, as charges are caught and released by trap states near the semiconductor-oxide interface. S_{VG} is given by [78]

$$S_{VG} = \frac{S_{Isd}}{g_{m,Isd}^2} = \frac{e^2 N_{ot}}{f W_{eff} L C_{ox}^{\square 2}} \tag{3.5}$$

where $S_{I_{sd}}$ is the source drain current noise, e is the elementary charge,

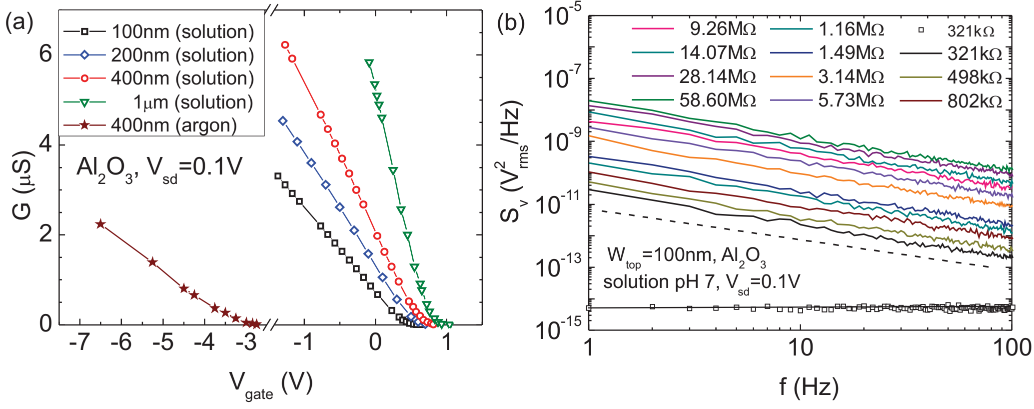


Figure 3.11: (a) Conductance G vs. gate voltage V_{gate}, measured with SiNWs with W_{top} ranging from 100 nm to 1 μm. The experiments were performed with a liquid gate voltage in a pH 7 buffer solution (open symbols). The SiNW with W_{top}= 400 nm was additionally investigated in an argon/air gas mixture (full symbols), when gated by the buried oxide. (b) Power spectral density of the voltage fluctuations S_V vs. frequency f. By applying a liquid gate voltage, the SiNW was gated to several resistance values R. The black dashed line indicates $1/f$ characteristics. Black open symbols show the thermal noise for the SiNW gated to 321 kΩ. The theoretical value is indicated by the black solid line.

N_{ot} the trap state density per area in cm^{-2}, W_{eff}=W_{top}+2W_{side}, $C_{ox}^{\square}$ the oxide capacitance per area and $g_{m,Isd}$ is the transconductance defined by $g_{m,Isd}$=$\partial I_{sd}/\partial V_{gate}$.
In the dielectric polarization noise model the noise originates from thermal fluctuations of dipoles in the gate oxide. Thus, S_{VG} is based on thermal noise, with the resistance R replaced by the real part of the impedance $Re(z)$ [51]

$$S_{VG} = 4k_BTRe(Z) = \frac{2k_BTtg(\delta)}{\pi C_{ox}f} \tag{3.6}$$

where C_{ox} is the gate oxide capacitance and $tg(\delta)$ is the dielectric loss tangent of the dielectric, defined by $tg(\delta) = Re(Z)/|Im(Z)| = 2\pi f C_{ox} Re(Z)$. In this model, the initially white thermal noise obtains a $1/f$ characteristics due to the complex impedance of the dielectric material.
According to the intrinsic resistance fluctuation model, noise is generated by intrinsic resistance fluctuations in the channel, e.g., due to mobility fluctuations. The normalized source drain current noise is given by

$$\frac{S_{I_{sd}}}{I_{sd}^2} = \frac{e\alpha_H\mu V_{sd}}{fL^2I_{sd}} \tag{3.7}$$

where α_H is the dimensionless Hooge constant, μ the mobility and L the SiNW length.
In Fig. 3.12 a we plot the power spectral density of the source drain cur-

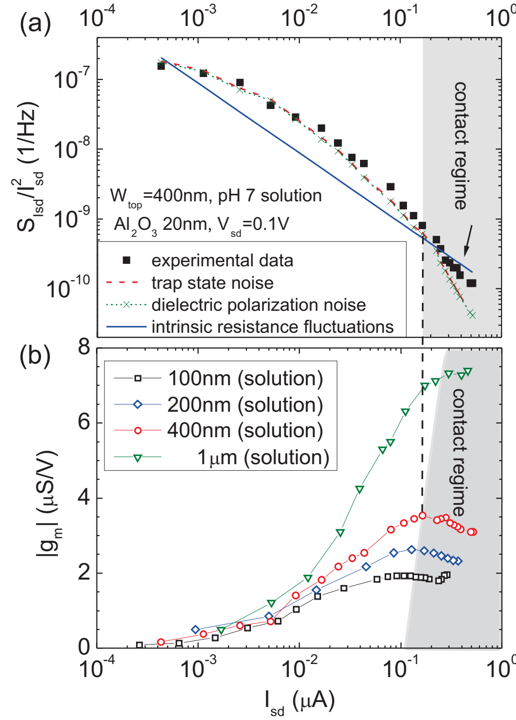


Figure 3.12: (a) Normalized source drain current noise S_{Isd}/I_{sd}^2 vs. source drain current I_{sd}. The black symbols show the experimental data. The blue solid represent the calculated data using the intrinsic resistance fluctuation model, respectively. The latter does not fit to the experimental results. The trap state noise model (red dashed line) and the dielectric polarization noise model (green dotted line) agree with the data in the SiNW regime (subthreshold and linear regime). For large source drain currents the noise deviates from the model, due to additional noise generated by the contacts (contact regime). (b) Absolute value of the transconductance $g_m = \partial G/\partial V_{gate}$ vs. the source drain current I_{sd}, obtained from the transfer curves shown in Fig. 3.11 a. The transconductance reaches a maximum and then the contact regime starts. The dashed black line marks the transition between the SiNW regime and the contact regime.

rent fluctuations S_{Isd} normalized by the squared source drain current I_{sd} at 10 Hz as a function of source drain current I_{sd} in order to compare the experimental data with the three noise models. To calculate S_{Isd}/I_{sd}^2 at 10 Hz in the resistance fluctuation model we used equation 3.7 and for the gate fluctuation models we combined equation 3.5 or equation 3.6 with $S_{I_{sd}}/I_{sd}^2 = S_{VG}\, g_{m,Isd}^2/I_{sd}^2$, where $g_{m,Isd}$ is the transconductance defined by $g_{m,Isd}$.
For the calculations, the experimental data of g_m and I_{sd} were used. In the resistance fluctuation model a Hooge constant of $\alpha_H = 3 \cdot 10^{-4}$ was assumed. However, as shown in Fig. 3.12 a, the resistance fluctuation model does not agree with the measurements, because it predicts a normalized source drain current noise proportional to $1/I_{sd}$, which is not seen in the experiments.
For both, the trap state noise model and the dielectric polarization noise

model, a very good agreement was achieved with a trap state density per area of N_{ot}= $2.5 \cdot 10^8 \text{cm}^{-2}$ and $tg(\delta)$=0.0075, respectively. Both parameters are in the expected range. [78, 51] For I_{sd} larger than 0.1 μA a small deviation from the model is found, as the experimental noise is larger compared to the theoretical expectations (see arrow in Fig. 3.12 a).

To explain this discrepancy we looked more carefully into the transconductance $g_m = \partial G/\partial V_{gate}$. Fig. 3.12 b shows the absolute value of the transconductance $|g_m|$, derived from the curves shown in Fig. 3.11 a. When the transconductance starts to saturate after the max. value, then a transition from the SiNW regime to the contact regime occurs. The black dashed line in both graphs of Fig. 3.12 marks this transition for the SiNW with W_{top}= 400 nm. Interestingly, the deviation from the model occurs at the same source drain current when the contact regime starts. This result shows that noise in SiNW-ISFET is increased in the contact regime. The finding is in agreement with previous studies reported by Tarasov et al. [83], who studied $1/f$ noise in similar devices with annealed source drain contacts. Due to implanted contacts used in this work, the contact regime is however less noisy and the low-noise regime is extended over a larger range.

The agreement of S_{Isd}/I_{sd}^2 in the SiNW regime between the experimental and calculated data using the gate fluctuation models, suggests that noise is dominantly generated by the gate. To investigate if the motion of ions in the 67 mM buffer solution generates the noise, we performed noise characterizations in deionized water and in an argon/air mixture. This time we focus on the gate referred voltage noise S_{VG}, in order to obtain more information about the noise source. Fig. 3.13 a shows the gate referred voltage noise S_{VG} for the SiNW with W_{top}= 400 nm, measured in deionized water and compared to S_{VG} obtained in the buffer solution. In both experiments the same SiNW covered with a top oxide of 20 nm Al_2O_3 was used. The noise level in the SiNW regime is similar, which suggests that ions contained in the buffer solution do not influence significantly the noise behaviour. Additionally, S_{VG} was characterized with the same SiNW, this time exposed to a gaseous argon/air mixture and gated by the back gate oxide. The reason for the higher S_{VG} in the dry environment is the smaller gate capacitance, due to the control of the SiNW-ISFET by the back gate.

In all three experiments S_{VG} is constant in the SiNW regime and independent of the resistance (or the gate voltage). In the contact regime S_{VG} increases slightly. This result is further confirmed by Fig. 3.13 b, showing S_{VG} for SiNWs with W_{top} ranging between 100 nm and 1 μm. In Fig. 3.13 b we normalized S_{VG} relative to the SiNW with W_{top}= 1 μm, since we used this width as a reference. Interestingly, the normalized data sets for the differently wide SiNWs are very similar. For sensors S_{VG} or rather $\sqrt{S_{VG}}$ is an important figure of merit, as it indicates how accurate a sensor can mea-

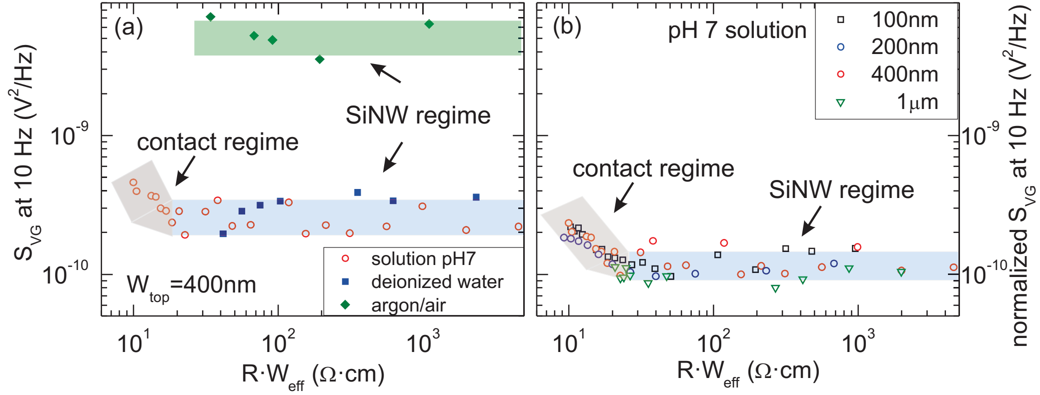


Figure 3.13: (a) Gate referred voltage noise S_{VG} at 10 Hz of the SiNW with W_{top} = 400 nm vs. resistance times effective SiNW width $R \cdot W_{eff}$, measured in pH 7 buffer solution, deionized water and an argon/air mixture. The SiNW was top-gated when exposed to solutions and gated by the buried oxide in dry environment. Shaded areas indicates the SiNW and the contact regime. (b) Gate referred voltage noise S_{VG} at 10 Hz normalized by W_{eff} relative to the SiNW with W_{top} = 1 μm vs. $R \cdot W_{eff}$, measured at pH 7 buffer solution. The SiNW regime and the contact regime are indicated by coloured bars and black arrows.

sure. The lowest $\sqrt{S_{VG}}$ of $1 \cdot 10^{-5}$ V/Hz$^{1/2}$ corresponds e.g. to an accuracy of 0.017% of an ideal pH shift of 60 mV/pH.
The constant gate referred voltage noise S_{VG} is the main characteristics for gate fluctuations. However, we still do not know, whether the intrinsic resistance fluctuation model or the trap state noise model holds, as in Fig. 3.12 a both models fit to the experimental data. Therefore, we analysed the noise of two SiNW-ISFETs with W_{top} = 400 nm and coated with 20 nm and 40 nm thick Al_2O_3 layer as top oxide. Both samples were fabricated in the same process run. Thereby, it is reasonable to assume a similar trap state density for both samples. The sample with 40 nm thick Al_2O_3 has a two times smaller gate oxide capacitance, compared to the 20 nm thick Al_2O_3 sample, as shown in Fig. 3.14 a. Considering the changes in the oxide capacitance, a difference of two in S_{VG} is expected according to the dielectric polarization model and a difference of four, if the trap state noise model holds (compare equation 3.5 and 3.6). Fig. 3.14 b shows S_{VG} for both samples as a function of resistance times effective SiNW width $R \cdot W_{eff}$. The difference in S_{VG} is close to the factor four, suggesting that the noise originates from trap state fluctuations and not from the dielectric polarization noise.
In Fig. 3.14 b S_{VG} is larger compared to the data shown in Fig. 3.13 a, although W_{top} of the SiNW is similar. The discrepancy can be explained by batch-to-batch variations in the trap state density.
The results obtained with SiNW-ISFETs covered with ALD grown Al_2O_3 demonstrate, that S_{VG} scales as $1/C_{ox}^2$. This is in agreement with the trap

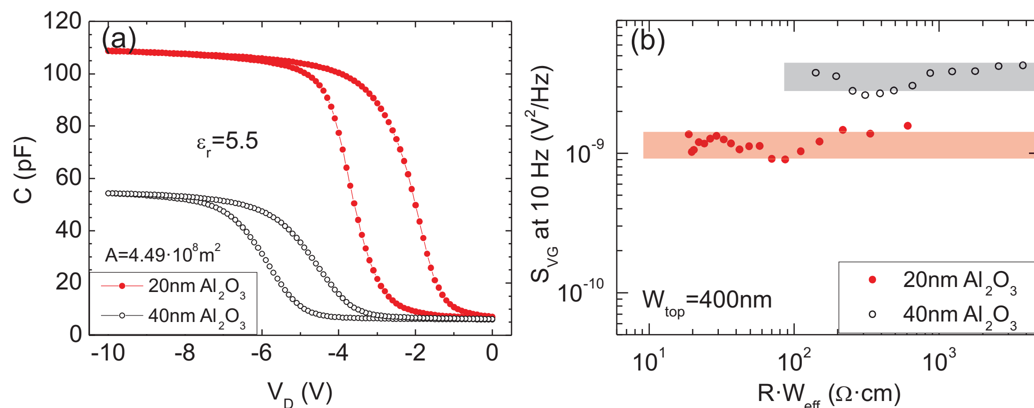


Figure 3.14: (a) Capacitance-voltage characteristics of the 20 nm and 40 nm thick Al_2O_4 layers, deposited on a Si wafer (ρ=10-20Ω·cm) in the same ALD run as the SiNW-ISFETs samples. (b) Gate referred voltage noise S_{VG} at 10 Hz for two SiNW with W_{top}= 400 nm vs. $R \cdot W_{eff}$. The SiNWs are covered with 20 nm and 40 nm thick Al_2O_3. S_{VG} differs by a factor of about four, in agreement with the trap state model.

state noise model, that states that trap states close to the silicon-oxide interface are the dominant source of $1/f$ noise. This means that for identical geometrical dimensions, S_{VG} is determined by the gate oxide capacitance C_{ox} and the trap state density N_{ot}.

3.4 Summary

In this chapter we characterized the SiNW-ISFETs in terms of noise and electrical and sensing properties. Leakage currents below 2 nA, reproducible transfer curves with negligible hysteresis and Ohmic contact formation, are the result of reliable fabrication techniques. Hole mobilities and dielectric constants are in good agreement with values from literature.
Not only the electrical properties but also the sensing characteristics are excellent. The pH response, determined by the voltage shift ΔV_{ref} of the transfer curves exhibit an ideal and linear Nernstian response of 60 mV/pH at 300 K with Al_2O_3 and HfO_2 as gate oxide, independent of the operating regime. To compare the pH response of differently wide SiNWs in the linear regime we normalized the conductance by the full top perimeter. This scaling method resulted in a constant transconductance for all SiNW widths and thereby in a constant pH response for all SiNW widths.
No influence of the SiNW width was observed on the pH response. This result is in strong contrast to previous publications. However, as long as SiNWs provide the same surface buffer capacitance per area for protons, no size dependence of the pH response is expected.

From the noise investigations we determined trap states close to the silicon oxide interface as the dominant 1/f noise source for SiNW-ISFETs covered with Al_2O_3. We demonstrated that the gate referred voltage noise is constant as long as the SiNW resistance is dominant (SiNW regime). When the contact resistance cannot not be neglected (contact regime) the noise increases slightly. The SiNW-ISFETs achieved a best accuracy of 0.017% of an ideal pH shift of 60 mV/pH. Moreover, the noise analysis shows that with decreasing gate capacitance and SiNW width the gate referred voltage noise increases and thereby the accuracy degrades. Therefore, we suggest to enhance accuracy with a parallel connection of multiple SiNWs, covered with a high capacitive and high quality oxide.

4 Additional Investigations

Apart from pH detection, the fabricated samples were used for further experiments, which will be briefly presented in this section. The following results are a collaborative work with the group of Prof. Dr. Christian Schönenberger from the Physics Department, University of Basel and further partners from the SiNW project (funded by the Swiss agency NanoTera) and the European HYSENS project. Parts of this chapter have been published elsewhere [4, 84, 85, 86] or will be submitted for publication. Most of the findings will be discussed in the PhD thesis of Mathias Wipf and Ralph Stoop (Uni Basel).

4.1 Reference Electrode

Portable sensor systems require a miniaturized reference electrode, usually integrated on the chip. Ideally, a reference electrode should sense the electrostatic potential in the liquid solution, but should not respond to species in the environment, such as ions. Different candidates for reference electrode materials are considered e.g. gold or graphene. Fu et al. [13] showed that graphene is insensitive to pH changes after a particular pre-treatment. However, graphene processing is still delicate and not established in industrial processes. The alternative is to use gold structures such as shown in Fig. 4.1. Here, we discovered that the gold film is pH sensitive and thereby not suitable for a stable reference electrode. More details about the pH

response of gold films will be given in the PhD theses of M. Wipf and R. Stoop (Uni Basel).

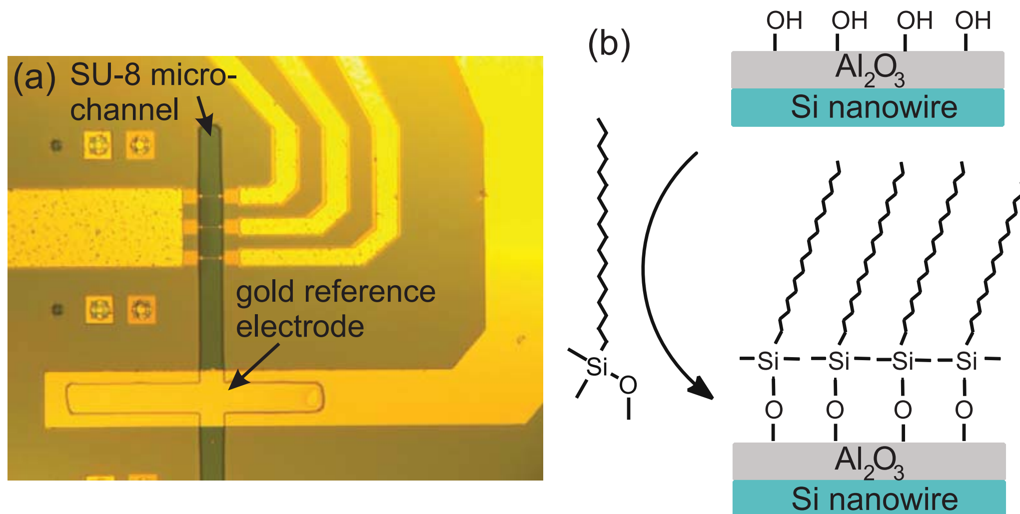


Figure 4.1: (a) Optical microscope image shows the cross-shaped SU-8 channel (vertical: dark blue bar; horizontal: yellow bar), aligned to three silicon nanowires (SiNWs) and the gold reference electrode. Only the area in the cross-shaped SU-8 channel is exposed to the analyte. We observed that gold films are sensitive to pH changes and thereby not suitable for a reference electrode. (b) SiNW coated with Al_2O_3 is passivated with octadecyldimethylmethoxysilane, (C 18 long alkyl chain). The passivation turns the sensing SiNW into a reference field-effect transistor (RFET). Similar electrical properties between the sensing SiNW and RFET enable differential measurements. The surface passivation and experiments were done by the group of Prof. Dr. Schönenberger and published in Ref. [4] (Figure 4.1 b by courtesy of A. Tarasov)

The next approach was to passivate the gate oxide surface of the SiNW with a self-assembled monolayer of silanes with long alkyl chains (C 18), in order to suppress the pH sensitivity by eliminating the proton-sensitive OH-groups (section 1.3.3). The surface passivation, measurements and analysis were performed by the group of Prof. Dr. Schönenberger (Uni Basel). In the following, the passivated SiNW is denoted as reference field-effect transistor (RFET). The electrical properties of the RFETs were similar to those of the sensing counterparts. However, the pH response was suppressed by two orders of magnitude. To use a passivated SiNW as a RFETs brings several advantages. Primarily, the reference electrode is integrated on the SiNW sensor as an on-chip electrode, which is required for a portable sensor system. Additionally, the similar electrical properties between the sensing SiNW and RFET - integrated on one sample - enable differential measurements, which can be used to correct undesired features of SiNWs, such as drift or non-specific adsorption. Further details about the RFET can be found in Ref. [4] and the PhD thesis of Alexey Tarasov.

4.2 Differential and Selective Ion Detection

To detect other species than pH, the surface of the SiNW has to be functionalized with receptors. The receptors immobilize charged targets close to the surface and thereby the charge causes a shift of the threshold voltage. A common receptor for alkali ions are crown ethers. The selectivity to particular ions is obtained by tailoring the cavity diameter of the crown ether. For example, the crown-5 ether is selective to sodium ions (Na^+). To become sensitive to the larger potassium ion (K^+), the diameter has to be enlarged to a crown-6 ether. The crown ethers were synthesized by the group of Prof. Dr. E. Constable at the University of Basel.

4.2.1 Potassium Detection

The amine-terminated crown-6 ether shown in Fig. 4.2 a does not have a high affinity to the oxide surface of SiNWs. A linker is needed, that connects the sensor surface with the receptor. In this example, the oxide surface was silanized with (3-Glycidoxypropyl)triethodysilane (GOPS). In a second reaction the amine-terminated crown ether was attached to the linker. The surface functionalization and the following ion detection experiments were done by the group of Prof. Dr. Schönenberger.

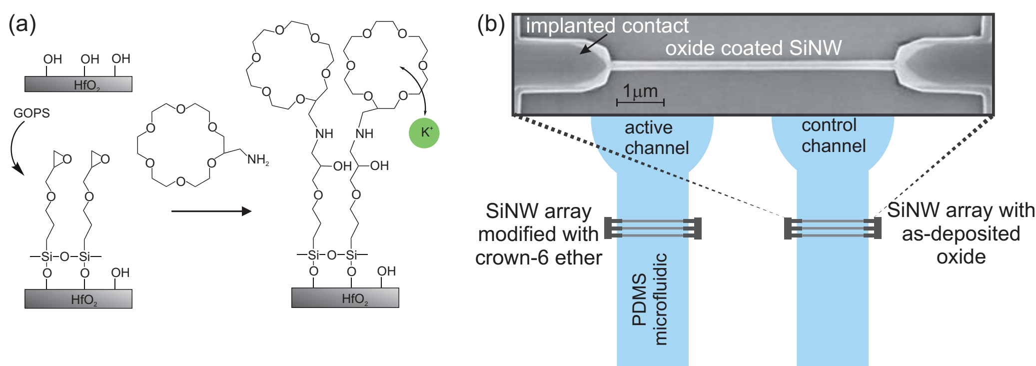


Figure 4.2: (a) HfO_2 surface is silanized by GOPS ((3-Glycidoxypropyl)-triethodysilane). The amine-terminated crown-6 ether is then attached to the modified oxide surface. The crown-6 ether is a common receptor for potassium ions. (b) SEM micrograph shows a SiNW coated with 20 nm thick HfO_2. The individual SiNW is part of a SiNW array shown in the sketch. When functionalized with crown-6 ether, the SiNWs are sensitive to potassium ions and accommodated in the PDMS microchannel, denoted as active channel. For differential measurements a second SiNW array - located in the control channel - exists with as-deposited HfO_2. The crown ethers were synthesized by the group of Prof. Dr. E. Constable at the University of Basel. The surface functionalization and ion detection experiments were done by the group of Prof. Dr. Schönenberger. (Figures by courtesy of M. Wipf).

Fig. 4.2 b shows half of the sensor design with SiNW arrays embedded in two PDMS microchannels. In the active channel a SiNW array functionalized with crown-6 ethers is accommodated. In the control microchannel a second SiNW array exists without surface modifications and an as-deposited oxide. This array is used as a reference for differential measurements. The functionalized SiNW array detected different potassium concentrations in KCl solutions. A differential signal of -40 mV/dec(mol/l) was obtained between the modified SiNW array and the array with as-deposited oxide. The negative sign shows that the threshold voltage shifts to more negative gate voltages with increasing KCl concentration, which indicates the adsorption of the positively charged potassium ions. The differential measurement minimized drift effects and corrected the unspecific adsorption of chlorine ions on the oxide surface. [84] In a second measurement the cross-sensitivity to sodium ions was tested with a NaCl solution. No response to sodium ions was observed. The experiments were performed by Mathias Wipf and Ralph Stoop and more details and findings will be given in their PhD theses.

4.2.2 Sodium Detection

For the sodium ion detection a thiol-terminated crown-5 ether was used as shown in Fig. 4.3 a. Thiol has a strong affinity to noble metals, such as gold. In order to improve the reaction of the thiol-terminated crown-ether with the SiNW surface, we covered the gate oxide with a 20 nm thick gold film in a lift-off process, based on e-beam lithography.

As shown in Fig. 4.3 b the gold coated and functionalized SiNW arrays are located in the active channel, whereas in the control channel the gold film remained unchanged. The experiments were preformed in NaCl solutions of different concentrations. The differential threshold voltage shift amounted to -45 mV/dec(mol/l). The negative signal confirms the adsorption of the positively charged sodium ion. The unspecific binding of chlorine ions was also observed with gold layers and corrected by the differential signal. In a control measurement no sensitivity to KCl was found. More details and findings will be given in the PhD theses of Mathias Wipf and Ralph Stoop.

4.3 Summary

The SiNW-ISFETs are not only sensitive to pH changes, but also to different species, depending on the surface functionalization. In this chapter, the SiNW surface was modified with crown-ethers and a selective detection

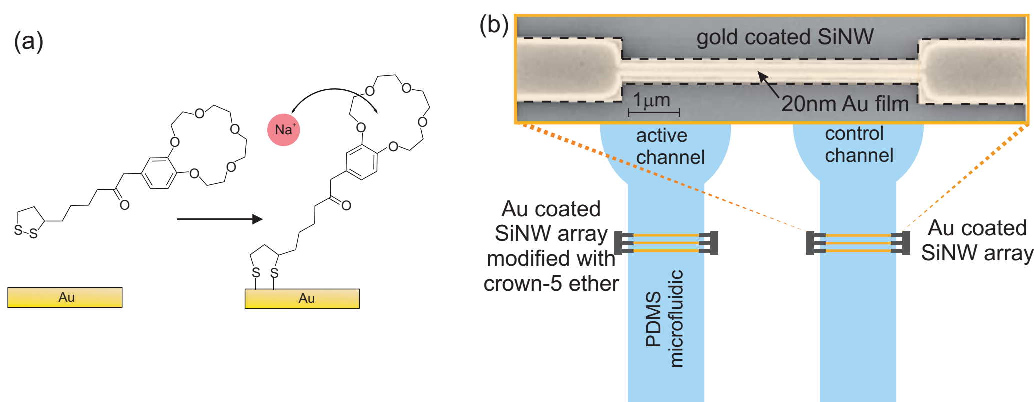


Figure 4.3: (a) Crown-5 ethers are sensitive to sodium ion and can be attached via thiol-chemistry to gold surfaces. (b) SEM micrograph shows a SiNW coated with oxide and a 20 nm thick oxide layer. The gold coated SiNW arrays are functionalized with crown-5 ether and embedded in the PDMS microchannel, denoted as active channel. For differential measurements a second gold coated SiNW array - located in the control channel - exists with unmodified gold films. The crown ethers were synthesized by the group of Prof. Dr. E. Constable at the University of Basel. The surface functionalization and ion detection experiments were done by the group of Prof. Dr. Schönenberger. (Figures by courtesy of M. Wipf).

of potassium and sodium ions was successfully demonstrated by differential read-out. The future goal is the multiplexed detection of both alkali ions, which means the sample contains both receptors in the same microchannel to detect sodium and potassium ions simultaneously. With respect to the differential read-out, there is the need for more investigations to find out, whether the signal of the unmodified and modified SiNW is similar in terms of pH response, unspecific interaction and drift, as only similar signals can be used for differential measurements.
A sensitivity to pH changes and chlorine ions was observed for gold, which therefore, cannot be used as a material for a reference electrode. Also, the signal of gold coated SiNWs had to be corrected by differential measurements.

5
Conclusions and Outlook

In this thesis we present a successful fabrication process for SiNW-ISFETs, based on SOI wafers, following the top down approach. One sensor contained 48 SiNWs with widths ranging from 100 nm to 1 μm and a constant length of 6 μm. The source drain contacts were highly doped and as gate oxide we used Al_2O_3 or HfO_2, grown by atomic layer deposition (ALD).
The SiNW-ISFETs demonstrate excellent electrical properties, such as reproducible transfer curves with a negligible hysteresis of $<$5 mV and leakage currents below 2 nA. Mobilities and relative permittivities of the ALD oxides are in the expected range and agree with literature values.
By investigating the noise, we determined the sensor accuracy and the origin of 1/f noise in SiNW-ISFETs covered with Al_2O_3. Based on our findings, we suggest that gate fluctuations are the dominant noise source. As noise data fits to the trap state noise model, we state that the gate fluctuations originate form trap states close to the silicon oxide interface. Interestingly, we observed two regimes with different noise levels. In the regime, where the source drain contact dominates, the noise level is slightly increased. This result is in agreement with previous observations. Operating the SiNW in a regime, where the contact resistance can be neglected is favourable in terms of noise, as the noise level is smaller. In the low noise regime the sensor accuracy was determined as 0.017% of 60 mV/pH for the SiNW with W_{top} =1 μm. With decreasing capacitance and SiNW width the accuracy degrades. Therefore, we suggest to enhance accuracy with a parallel con-

nection of multiple SiNWs, covered with a high capacitive and high quality oxide.
In a systematic study on the influence of the SiNW width on the pH response we obtained a result close to the ideal Nernstian limit of 60 mV/pH at 300 K, independent of the SiNW width or the operating regime. To compare the pH response of differently wide SiNWs in the linear regime we normalized the conductance by the area that is exposed to the liquid gate (as the length is constant we normalized by the full top perimeter). This scaling method resulted in a constant transconductance for all SiNW widths and thereby in a constant pH response for all SiNW widths. In brief, no influence of the SiNW width or the operating regime was observed on the pH response. These results are in contrast to previous publications. However, no size dependence is expected, as long as all SiNWs provide the same surface buffer capacitance per area for protons.
The sensitivity to pH requires only SiNWs covered with a bare gate oxide as sensing surface. To become sensitive to ions other than protons the surface of the SiNW has to be modified with receptors. The functionalization of individual SiNW arrays became possible with the integration of the PDMS microfluidic system. This technical accomplishment is of importance as it paves the way for differential and multiplexed detection. The surface of two SiNW arrays was functionalized with crown-5 ethers or crown-6 ethers, which are known to be sensitive to Na^+ or K^+, respectively. Two arrays remained unfunctionalized in order to perform differential measurements. An advantage of differential measurements is that disturbances of the signal, such as drift or unspecific adsorption can be minimized or even eliminated. The experiments performed in different concentrations of NaCl and KCl demonstrated a differential signal of -40 mV/dec(mol) and -45 mV/dec(mol) for potassium and sodium ions, respectively. In future, the next main step will be to extend the sensitivity to other ions, such as Ca^{2+} and to detect alkali ions in a multiplexed mode, meaning one sample can detect several ions simultaneously.
The obtained results demonstrated that our sensor platform is a powerful tool for analytical measurements. Therefore, the next goal is to go towards (bio-) chemical experiments.

Characterization of ALD Oxides

Capacitance-voltage (C-V) spectroscopy is a widely used method to characterize oxides. Typically, metal-oxide-semiconductor (MOS) capacitors are fabricated for the oxide characterization. They contain a silicon wafer, with an unpatterned oxide layer on top, which is then metallized with a patterned metal layer. The back side is metallized by an patterned layer, as illustrated in Fig. A.1. The interface between the semiconductor and the oxide has to be clean to reduce the number of interface trap states. A clean surface is achieved by the RCA cleaning and a prompt oxidation of the semiconductor.

For the measurements, the metal contacts at the top and bottom side of the sample are connected with an analyzer and a DC voltage V_{DC} with a superimposed sinusoidally oscillating AC voltage is applied (Fig. A.1). Typically, the frequency f of the AC voltage is in the range between 100 kHz and 13 MHz. The analyzer measures the AC voltage, the phase angle and the AC current through the sample. With the acquired data the capacitance C is calculated by $C = Itg(\delta)/(2\pi f V_{AC,s})$, where I is the magnitude of the AC current through the test sample, f the frequency, $V_{AC,s}$ the magnitude of the measured AC voltage and δ the phase angle. [87]

The applied DC voltage is changed gradually to drive the MOS capacitor from accumulation into depletion (and into inversion), as shown in Fig. A.2 a. When a large negative DC voltage is applied to the p-type Si wafer, then holes in the substrate start to accumulate near the oxide-semiconductor in-

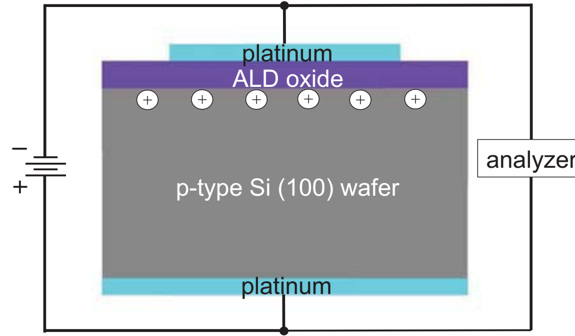


Figure A.1: Schematic picture of a MOS capacitor, showing the oxide, grown by atomic layer deposition (ALD) on top of a highly doped silicon wafer. The size of the MOS capacitor is defined by the dimensions of the top platinum square. When a DC voltage with a superimposed AC voltage is applied, the AC voltage and phase angle and the AV current through the sample are measured by the analyzer in order to calculate the capacitance. The DC voltage drives the semiconductor to accumulation, as indicated by the white circles.

terface. In accumulation, the capacitance is at its max. value and reflects the oxide capacitance C_{ox} (see Fig. A.2 a). When the DC voltage is decreased a depletion layer forms. The charge carriers are no longer close to the interface and the total capacitance consists of the series connection of the oxide capacitance and the depletion layer capacitance. Thereby, the minimum capacitance C_{min} (see Fig. A.2 a) is influenced by the doping concentration of the substrate.
Besides the determination of the relative dielectric constant ε_r the C-V curves give information about the quality of the oxides in terms of fixed oxide charges and interface trap states. Fixed oxide charges cause a shift of the flatband voltage $V_{fb} = \phi_{ms} - Q_{ox}/C_{ox}$ as shown in Fig. A.2 a [28] (p.224). The shift from the ideal flatband voltage, given by the difference in the workfunctions ϕ_{ms} to the experimental flatband voltage reveals the number of fixed charges Q_{ox} (equ. 1.1). Trap states cause a "stretch-out" of the C-V curves as shown in Fig. A.2 b, due to the less effective modulation of the surface potential ψ_s by the applied DC voltage. [28](p.217).

The MOS capacitors were fabricated from highly doped p-type Si (100) wafers with a resistivity of 0.002-0.005 Ω·cm and Al_2O_3 on top, grown by atomic layer deposition (ALD, Savannah S 100 Cambridge NanoTech). Prior to the oxide deposition, the Si wafer was RCA cleaned. Afterwards, a metal layer was deposited on the top and bottom side of the sample. The metal layer on top was structured in squares. For the measurement the sample was bonded into a chip carrier and the contact pins were connected to the test fixture of the LF impedance analyzer 4192A (Hewlett Packard).
The oxide thickness was determined by the scanning electron microscope.

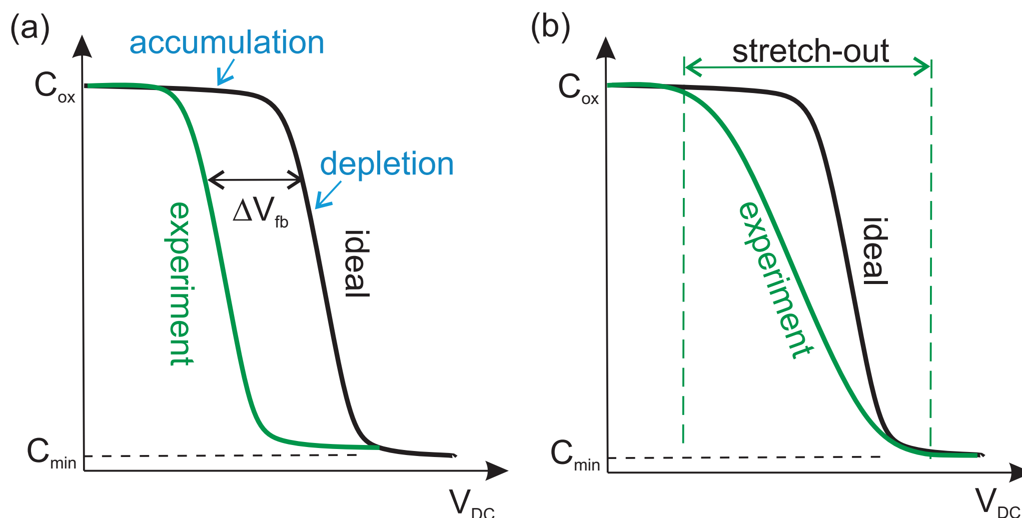


Figure A.2: (a) Capacitance C as a function of the DC voltage V_{DC}. The DC voltage is changed gradually to drive the MOS capacitor from accumulation into depletion. The max. capacitance is achieved at accumulation and it reflexes the oxide capacitance C_{ox}. The min. capacitance is reached when the depletion width has its largest extension. The total capacitance is then given by the series connection of the oxide and the depletion layer capacitance. The ideal flatband voltage V_{fb} is given by the workfunction difference ϕ_{ms} between the metal and semiconductor. The experimental flatband voltage shifts due to fixed charges Q_{ox} in the oxide. (b) The experimental C-V curve is distorted and stretched-out due to the presence of interface trap states.

The micrograph in Fig. A.3 shows the cross sections of the Al_2O_3 layer. 200 ALD cycles yield about a 20 nm thick layer.

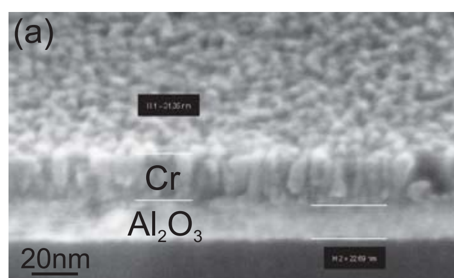


Figure A.3: Scanning electron micrograph shows the cross section of samples coated with Al_2O_3, grown by atomic layer deposition (ALD) on highly doped silicon wafer. For better imaging conditions the oxide layer is coated with a 30 nm thick chromium layer. The thickness of Al_2O_3 layer amounts to 20 nm.

Fig. A.4 a-b shows the C-V measurement of MOS capacitors with Al_2O_3. In Fig. A.4 a a MOS capacitor was measured with as-grown oxides, while in Fig. A.4 b the sample was annealed for 10 min. at 450 °C in forming gas atmosphere. The annealed MOS capacitor has an increased dielectric

constant and thereby the annealing of the ALD oxides was integrated in the fabrication process. The curves exhibit a stretch-out and a large C-V hysteresis in the forward and backward direction, which might be attributed to interface trap states. [88]

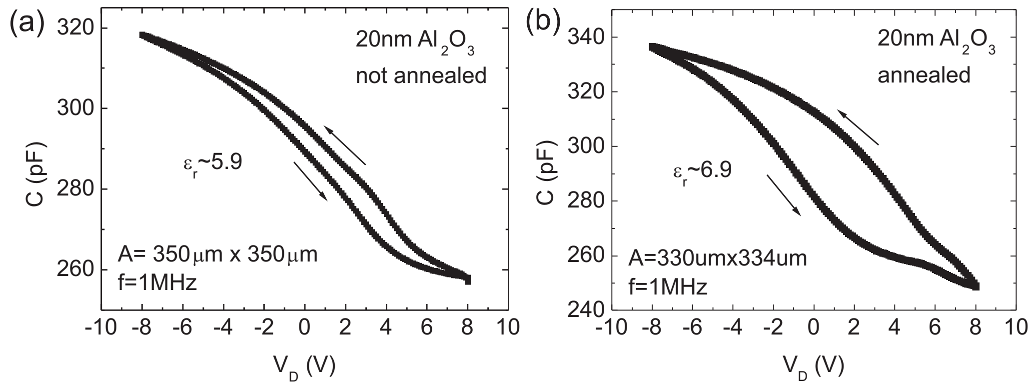


Figure A.4: (a-b) C-V curves measured with Al_2O_3 MOS capacitors. The data measured in the forward and backward direction exhibits a large C-V hysteresis which might indicate the presence of interface trap states. (a) Al_2O_3 MOS capacitor was not annealed and a relative dielectric constant of 5.9 was extracted. (b) Al_2O_3 MOS capacitor was annealed and a relative dielectric constant of 6.9 was obtained.

In an additional C-V control measurement we also characterized the buried oxide from the SOI wafer, as shown in Fig. A.5. The extracted relative dielectric constant of 3.4 is close to the literature value of 3.9. In the forward and backward voltage sweep we do not observe hysteresis, which indicates the high quality of the buried oxide layer of the SOI wafer.

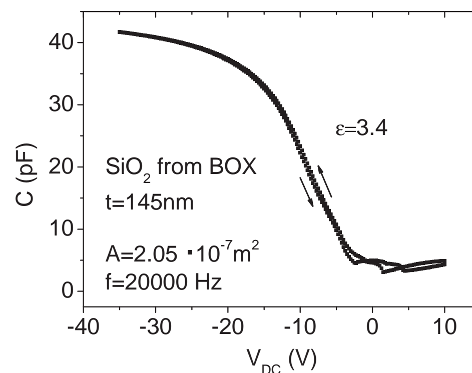


Figure A.5: C-V curve measured from the buried oxide of the SOI wafer. A relative dielectric constant of 3.4 was extracted that is close to the literature value of 3.9.

B Conductance Maps

Two-dimensional conductance maps as shown in Fig. B.1 are generated by sweeping both, the back and the liquid gate and measuring the conductance. A cut through the map at a fixed V_{bg} e.g. at -2 V (white, dashed line, in Fig. B.1 a) results in a transfer curve as shown in Fig. B.1 b. 2d-maps give an overview over the characteristics of the conductance in different voltage ranges and can be therefore used to find out the preferred operating regime. The slope in the maps, indicated by black lines, is determined by the ratio of the gate coupling capacitances C_{bg}/C_{lg} [16], where C_{bg} is the buried oxide capacitance and C_{lg} is the series connection of the top oxide capacitance C_{TOX} (see Fig. 2.9 g) and the double layer capacitance C_{dl}. As $C_{dl} \gg C_{TOX}$, we assume $C_{lg} \approx C_{TOX}$. Thereby, C_{TOX} is reflected in the slope.
This can be clearly seen in Fig. B.1 a, c-d showing the slope for samples with 20 nm Al_2O_3 and 10 and 20 nm HfO_2. The sample with 20 nm Al_2O_3 has a slope of 0.07, which is higher compared to the 0.02 slope of the sample with 20 nm HfO_2. This is explained by the capacitance differences between both materials, due to the dielectric constants of $\varepsilon_r \approx 7$ and ≈ 17 for Al_2O_3 and HfO_2, respectively. The 10 nm thick HfO_2 sample has a slope two times smaller compared to the counterpart with 20 nm. This is in qualitative agreement with the capacitance ratio, as it shows the right trend. However, the thickness dependence of the dielectric constant of HfO_2, discussed in section 3.1.2 is not demonstrated. From CV-measurements we obtained $\varepsilon_r \approx 12$ and 17 for 10 and 20 nm thick HfO_2 layers. The CV-measurements

were done in the group of Prof. Dr. Adrian Ionescu at EPFL, Lausanne. Therefore we conclude, that the slope gives the right trend for the capacitance ratio C_{bg}/C_{lg}, however for a quantitative determination of the dielectric constants this method is not as precise as CV-measurements.
Moreover, Fig. B.1 a, c-d show that the slope is constant over a wide voltage range, which indicates that the conductance is mainly determined by the charge carrier density in the SiNW and an influence of the source drain contacts is minimized. This means, that constant conditions over a wide operating range are given. This is an improvement with regards to samples having low doped source drain contacts such as published in Ref. [16].

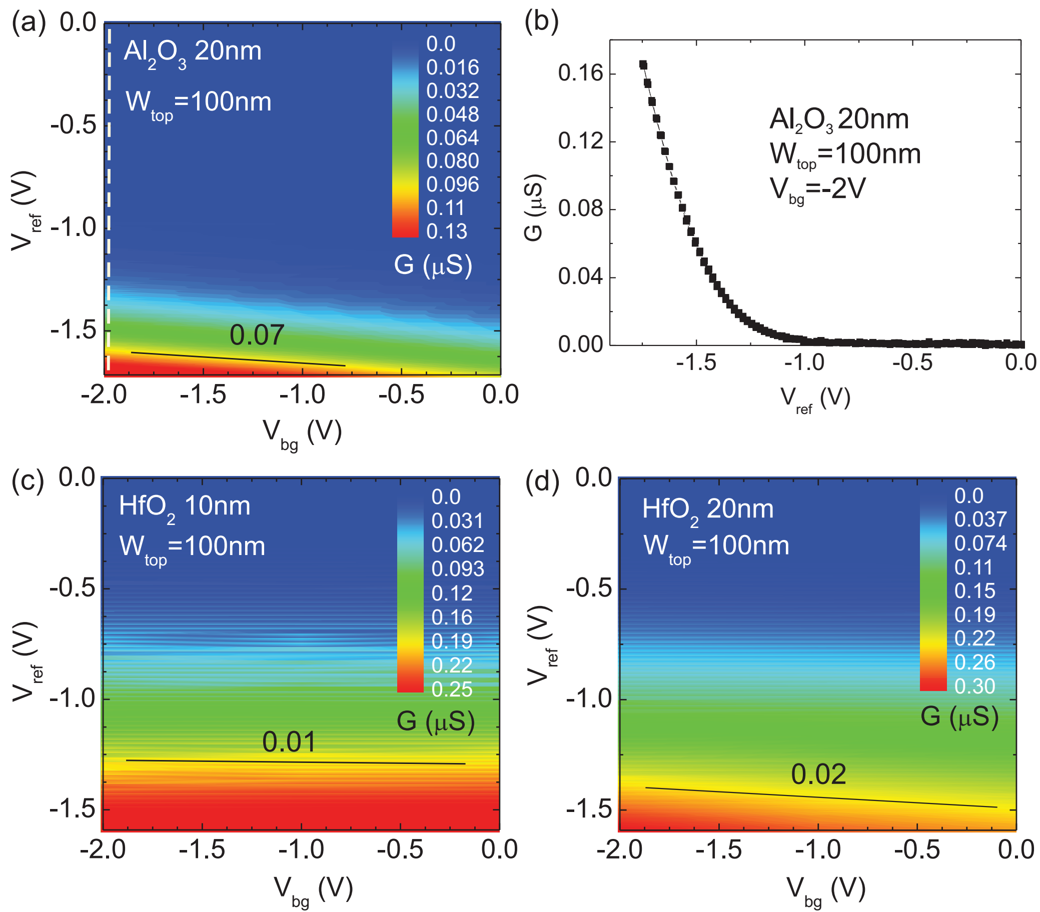
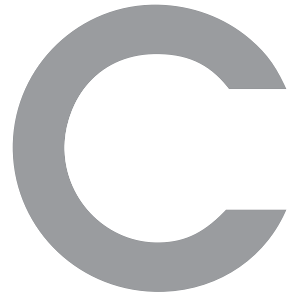


Figure B.1: (a-b) Two dimensional conductance map vs. reference voltage V_{ref} and back gate voltage V_{bg}, measured with a SiNW coated with 20 nm Al_2O_3. The black line indicates the slope, referring to the capacitance ration C_{bg}/C_{lg}. The dashed, white line shows the cut through the 2d map, that results in the transfer curve shown in Fig. b. (c-d) Two dimensional conductance maps vs. the reference voltage V_{ref} and the back gate voltage V_{bg}, measured with SiNWs coated with 10 nm (c) and 20 nm (d) HfO_2.



Fabrication Protocols

Device Fabrication

SOI wafer characteristics

Wafer:	8“ silicon-on-insulator (SOI)
Supplier:	SOITEC France
Device layer:	
Orientation:	(100)
Dopant:	p-type, boron
Resistivity:	8.5-11.5 Ωcm
Thickness:	88 nm
Buried oxide (SiO_2):	
Thickness:	145 nm
Silicon handle wafer:	
Type:	CZ, p-type
Resistivity:	8-22 Ωcm
Thickness:	725 μm

- **Thinning**
  1. sample cleaning:
     – Piranha solution: H_2O_2:H_2SO_4 2:1 for 10 min at 95°C
     – HF dip
  2. thermal oxidation of silicon device layer

- **Alignment marker fabrication**
  1. spin coating:
     PMMA 672.11, 1500 rpm, thickness $\sim 3\mu m$
     bake on hotplate for 5 min at 175°C
     gradual cooling of the sample to avoid cracks in PMMA
  2. electron beam lithography: Vistec EBPG 5000$^+$
     resolution=0.03μm, beam step size=0.03μm
     beam current= 150 nA, dose=1000$\mu C/cm^2$
     marker size 10 μm x 10 μm
  3. development: Hamatech
     IPA:MIBK 3:1, time=2 min; then rinse in IPA, time=30 sec
  4. reactive ion etching (RIE): Oxford RIE 100
     – top SiO_2: CHF_3 12 sccm, Ar 38 sccm, 30 mTorr, 100 W, 300 K, V_{DC}=485 V time=2 min
     – device Si layer: CHF_3 30 sccm, SF_6 4 sccm, O_2 3 sccm, 50 mTorr, 100 W, 300 K, V_{DC}=365 V time=5 min
     – buried SiO_2: CHF_3 12 sccm, Ar 38 sccm, 30 mTorr, 100 W, 300 K, V_{DC}=485 V time=8 min
     – Si handle wafer: CHF_3 30 sccm, SF_6 4 sccm, O_2 3 sccm, 50 mTorr, 100 W, 300 K, V_{DC}=365 V time=21 min
     – resulting alignment marker depth: $\sim 1\ \mu m$
  5. sample cleaning: remove PMMA in acetone and then in Piranha solution
     H_2O:H_2SO_4 2:1 for 10 min at 95°C Piranha

- **Electron beam lithography: device pattern**
  1. spin coating:
     Ti Primer, 4000 rpm, bake for 1 min at 110°C
     nLOF:EBR 1:4, 4000 rpm; bake: 1 min at 110°C
  2. exposure:
     – for SiNWs: resolution=0.005μm, beam step size=0.005μm
     beam current 2 nA, dose=180$\mu C/cm^2$
     – for large structures: resolution=0.005μm, beam step size=0.03μm
     beam current 50 nA, dose=165$\mu C/cm^2$
  3. post exposure bake: 1 min at 110°C
  4. development: AZ MIF 826 for 25 sec; then rinse in DI-water

- **Device etching**
  1. RIE etching of top oxide: Oxford RIE 100
     top SiO_2: CHF_3 12 sccm, Ar 38 sccm, 30 mTorr, 100 W, 300 K, V_{DC}=485 V time=27 sec
  2. dip in buffered HF to remove the remaining oxide
  3. wet chemical etching of silicon device layer
     tetramethylammonium hydroxide (TMAH) and 10 vol% isopropanol, time=2 min at 45°C
  4. sample cleaning: Piranha solution:
     H_2O_2:H_2SO_4 2:1 for 10 min at 95°C
- **Contact fabrication I**
  1. spin coating
     PMMA 672.08, 3000 rpm
     bake for 30 min at 175°C, gradual cooling of the sample
  2. electron beam lithography: Vistec EBPG 5000^{+}
     – for SiNWs: resolution=0.005μm, beam step size=0.005μm
     beam current 2 nA, dose=850$\mu C/cm^2$
     – for large structures: resolution=0.005μm, beam step size=0.03μm
     beam current 190 nA, dose=850$\mu C/cm^2$
  3. development: Hamatech
     IPA:MIBK 3:1, time=2 min; then rinse in IPA, time=30 sec
  4. ion implantation at Ion Beam Services (IBS), Peynier, France
     BF_2^+, energy=43 keV, dose= $2.3 \cdot 10^{+15} cm^{-2}$
  5. removal of PMMA implantation mask in acetone
  6. sample cleaning
     RIE O_2, 40 sccm, 200 mTorr, 30 W
     Piranha solution
  7. thermal activation of dopants: PPC Process Product Corporation annealing oven
     annealing for 6 min at 950°C in forming gas and N_2
- **RCA cleaning and ALD deposition**
  1. Piranha solution:
     H_2O_2:H_2SO_4 2:1 for 10 min at 95°C
  2. buffered HF for 35 sec to remove the thermal top oxide layer

3. RCA 1 cleaning:
   H_2O:H_2O_2:NH_4OH 20:4:1 for 10 min at 65°C
4. buffered HF dip
5. RCA 2 cleaning:
   H_2O:H_2O_2:HCl   20:1:1 for 10 min at 65°C
6. atomic layer deposition (ALD) at 225 °C for Al_2O_3 and at 200 °C for HfO_2

- **Contact fabrication II**
  1. dehydration bake for 10 min at 200°C
  2. spin coating:
     HMDS, 4000 rpm, bake for 1 min at 110°C
     nLOF:EBR 1:0.5, 6000 rmp, bake for 1 min at 110°C
  3. optical lithography: (Karl Süss MJB 3)
     time=6 sec
  4. post exposure bake: 1 min at 110°C
  5. development:
     AZ MIF 826, time=80 sec
  6. opening of the contact window in the gate oxide:
     for Al_2O_3 200 deposition cycles: buffered HF 35 sec
     for HfO_2 200 deposition cycles: buffered HF 5 min.
  7. directly afterwards evaporation: electron beam evaporation with BAK 600
     AlSi(1 %) 300 nm
  8. lift-off in n-methyl-2-pyrrolidon (NMP) at room temperature
  9. annealing of contact metal and ALD oxide:
     annealing for 10 min at 450°C in forming gas

- **SU-8 microchannel**
  1. dehydration bake for 10 min at 200°C
  2. spin coating:
     SU-8 2002, 4000 rpm, bake 1 min at 95°C
  3. optical lithography: (Karl Süss)
     time=18 sec
  4. post exposure bake: 1 min at 95°C

5. development:
   EC 11 time=90 sec; then rinse in IPA
6. hard bake of SU-8 on hotplate:
   bake sample for 25 min at 180°C ; then gradual cooling of the sample

- **Dicing**
  1. spin coating:
     microposit S1813, 1000 rpm, bake 2 min at 110°C
  2. sawing: Disco DAT 341 or Esec 8003
     sample size 9 mm x 9 mm
  3. removal of resist with acetone

- **Packaging**
  1. scratch back side of the sample with diamond scriber
     glue the sample with silver paste in 64 pins chip carrier (IPK64F1-2219A, NTK Technologies Inc.)
  2. wire wedge bonding: MEI Marpet Enterprises Inc.
     wire material: Al
     – bond on chip carries: power 2.5, time 4.5
     – bond on sample: power 1.0, time 7.5

Au-film for ion and bio-detection

1. spin coating:
   O_2 plasma: O_2 40 sccm, 200 mTorr, 30 W, 300 K, V_{DC}=87 V
   time=30 sec
   PMMA 669.04, 6000 rpm, thickness ∼220 nm
   bake on hotplate for 3 min at 175°C
2. electron beam lithography: Vistec EBPG 5000$^+$
   resolution=0.01μm, beam step size=0.01μm
   beam current= 2 nA, dose=850μC/cm^2
3. development: Hamatech
   IPA:MIBK 3:1, time=2 min; then rinse in IPA, time=65 sec
   O_2 plasma: O_2 40 sccm, 200 mTorr, 30 W, 300 K, V_{DC}=87 V
   time=8 sec
4. evaporation: electron beam evaporation with UNIVEX
   Cr 5 nm, Au 20 nm
5. lift-off in acetone for several hours

SU-8 molds to form PDMS Microfluidics

SU-8 structures on a Si wafer as substrate were used as mold to fabricate a PDMS microfluidic system as shown in Fig. 2.8 c. SU-8 is a negative tone epoxy type resist, sensitive to UV light and electron beam exposure. In the process the pattern of the microfluidic was defined in a SU-8 layer of 50 μm or 100 μm thickness by electron beam lithography, enabling us to be very flexible in the design as no mask for optical lithography was required. The thickness of the SU-8 layer defined later the height of the microchannel. After EBL, the SU-8 was baked and developed, according to the fabrication protocol below. Then, the Si wafer with SU-8 structures on top were covered with a thick and fluid PDMS layer that was thermally cured to obtain a cross-linked and solid PDMS structure. After cooling, the PDMS layer was peeled-off from the substrate and the reverse pattern of the SU-8 mold was transferred to the solid PDMS part.

Fabrication of SU-8 molds

1. dehydration bake for 10 min at 200°C
2. spin coating:
   SU-8 50, 1250 rpm for 100 μm and 2000 rpm for 50 μm thick SU-8 molds
3. bake for 10 min at 65°C and for 60 min at 95°C, gradual cooling of sample
4. electron beam lithography: Vistec EBPG 5000$^+$
   resolution=0.05μm, beam step size=0.05μm
   beam current= 1 nA, dose=5 μC/cm^2
5. post exposure bake: 10 min at 95°C
6. development:
   EC 11 time=12 min; then rinse in IPA
7. hard bake: 20 min at 180°C, gradual cooling of the sample

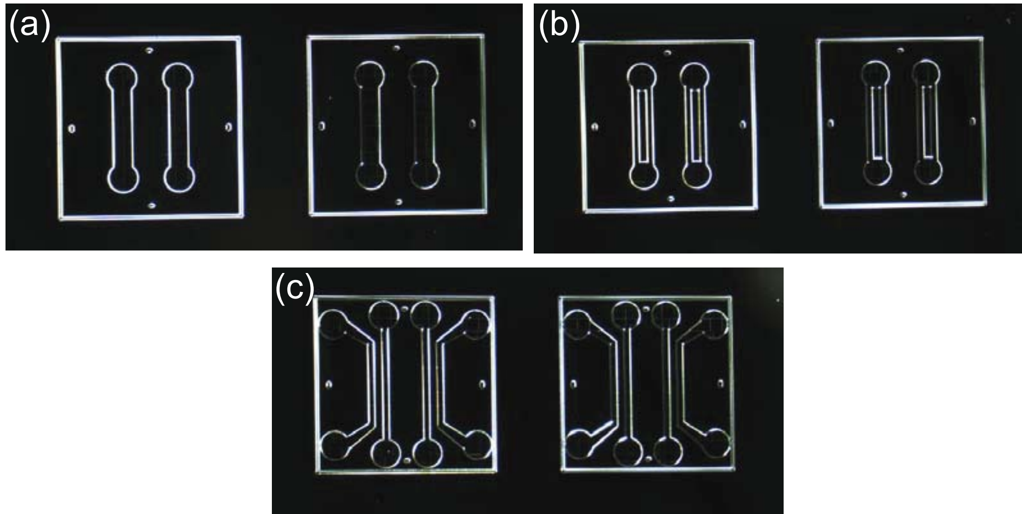


Figure C.1: (a-c) Optical microscope pictures show SU-8 molds with different designs. The SU-8 molds were used to transfer the reverse pattern to the PDMS microfluidic.

Optical mask fabrication: photomask blank 4“ with Cr 100nm

1. mask cleaning:
   Piranha solution: H_2O_2:H_2SO_4 2:1 for 10 min at 95°C
2. spin coating:
   O_2 plasma: O_2 40 sccm, 200 mTorr, 30 W, 300 K, V_{DC}=87 V time=30 sec
   HMDS, 2000 rpm, bake at 110°C for 90 sec
   nLOF:EBR 1:0.5, 2000 rpm, bake at 110°C for 90 sec
3. electron beam lithography: Vistec EBPG 5000^+
   resolution=0.03μm, beam step size=0.03μm
   beam current= 20 nA, dose=165 μC/cm^2
4. post exposure bake: 90 sec at 110°C
5. development:
   AZ MIF 826 for 2 min; then rinse in DI-water
6. Cr-etching: BMP
   time=280 sec
7. removal of nLOF resist with Piranha solution:
   H_2O_2:H_2SO_4 2:1 for 35 min at 95°C

Bibliography

[1] D. R. Thevenot, K. Toth, R. A. Durst, and G. S. Wilson. Electrochemical biosensors: recommended definitions and classification. *Biosensors & Bioelectronics*, 16(1-2):121–131, January 2001.

[2] Jonathan S. Daniels and Nader Pourmand. Label-free impedance biosensors: Opportunities and challenges. *Electroanalysis*, 19(12):1239–1257, June 2007.

[3] D. A. Armbruster, M. D. Tillman, and L. M. Hubbs. Limit of detection (LOD) limit of quantitation (LOQ) - comparison of the empirical and the statistical, methods exemplified with GC-MS assays of abused drugs. *Clinical Chemistry*, 40(7):1233–1238, July 1994.

[4] A. Tarasov, M. Wipf, K. Bedner, J. Kurz, W. Fu, V. A. Guzenko, O. Knopfmacher, R. L. Stoop, M. Calame, and C. Schönenberger. True reference nanosensor realized with silicon nanowires. *Langmuir*, 28(25): 9899–9905, June 2012.

[5] Elke Prohaska Hans Wolf Stefan Dübel Sabine Hauck, Stephan Drost. *Analysis of Protein Interactions Using a Quartz Crystal Microbalance Biosensor*. Chapter 15, 2002.

[6] Ram Datar, Seonghwan Kim, Sangmin Jeon, Peter Hesketh, Scott Manalis, Anja Boisen, and Thomas Thundat. Cantilever sensors: Nanomechanical tools for diagnostics. *MRS Bulletin*, 34(6):449–454, June 2009.

[7] Matthew E. Stewart, Christopher R. Anderton, Lucas B. Thompson, Joana Maria, Stephen K. Gray, John A. Rogers, and Ralph G. Nuzzo. Nanostructured plasmonic sensors. *Chemical Reviews*, 108(2):494–521, February 2008.

[8] Alexander P. Demchenko. *Introduction to Fluorescence Sensing*. Springer, 2009.

[9] Derek Pletcher. *First Course in Electrode Processes*. The Royal Society of Chemistry, Thomas Graham House, 2009.

[10] P. Bergveld. Development of an ion-sensitive solid-state device for neurophysiological measurements. *IEEE Transactions On Biomedical Engineering*, BM17(1):70–71, 1970.

[11] Cristina C. Cid, Jordi Riu, Alicia Maroto, and F. Xavier Rius. Ion-sensitive field effect transistors using carbon nanotubes as the transducing layer. *Analyst*, 133(8):1001–1004, 2008.

[12] Kenzo Maehashi and Kazuhiko Matsumoto. Label-free electrical detection using carbon nanotube-based biosensors. *Sensors*, 9(7):5368–5378, July 2009.

[13] Wangyang Fu, Cornelia Nef, Oren Knopfrnacher, Alexey Tarasov, Markus Weiss, Michel Calame, and Christian Schönenberger. Graphene transistors are insensitive to pH changes in solution. *Nano Letters*, 11 (9):3597–3600, September 2011.

[14] Y. Cui and C. M. Lieber. Functional nanoscale electronic devices assembled using silicon nanowire building blocks. *Science*, 291(5505): 851–853, February 2001.

[15] Eric Stern, James F. Klemic, David A. Routenberg, Pauline N. Wyrembak, Daniel B. Turner-Evans, Andrew D. Hamilton, David A. LaVan, Tarek M. Fahmy, and Mark A. Reed. Label-free immunodetection with CMOS-compatible semiconducting nanowires. *Nature*, 445(7127):519–522, February 2007.

[16] O. Knopfmacher, A. Tarasov, Wangyang Fu, M. Wipf, B. Niesen, M. Calame, and C. Schönenberger. Nernst limit in dual-gated Si-nanowire FET sensors. *Nano Letters*, 10(6):2268–2274, June 2010.

[17] Songyue Chen, Johan G. Bomer, Edwin T. Carlen, and Albert van den Berg. Al2O3/silicon nanoISFET with near ideal nernstian response. *Nano Letters*, 11(6):2334–2341, June 2011.

[18] Sufi Zafar, Christopher D'Emic, Ali Afzali, Benjamin Fletcher, Y. Zhu, and Tak Ning. Optimization of pH sensing using silicon nanowire field effect transistors with HfO2 as the sensing surface. *Nanotechnology*, 22 (40):405501, October 2011.

[19] V. Rocher, N. Jaffrezic-Renault, H. Perrot, Y. Chavelier, and P. Leperchec. Nitrate-sensitive field-effect transistor with silica gate insulator modified by chemical grafting. *Analytica Chimica Acta*, 256(2):251–255, January 1992.

[20] Linbao Luo, Jiansheng Jie, Wenfeng Zhang, Zhubing He, Jianxiong Wang, Guodong Yuan, Wenjun Zhang, Lawrence Chi Man Wu, and Shuit-Tong Lee. Silicon nanowire sensors for Hg2+ and Cd2+ ions. *Applied Physics Letters*, 94(19):193101, May 2009.

[21] G. F. Zheng, F. Patolsky, Y. Cui, W. U. Wang, and C. M. Lieber. Multiplexed electrical detection of cancer markers with nanowire sensor arrays. *Nature Biotechnology*, 23(10):1294–1301, October 2005.

[22] Xuan Thang Vu, Jan Felix Eschermann, Regina Stockmann, Ranjita GhoshMoulick, Andreas Offenhäusser, and Sven Ingebrandt. Top-down processed silicon nanowire transistor arrays for biosensing. *Physica Status Solidi A-applications and Materials Science*, 206(3):EnFI; VDE VDI Soc Microelect, Micro & Precis Engn, March 2009.

[23] Xuexin Duan, Yue Li, Nitin K. Rajan, David A. Routenberg, Yorgo Modis, and Mark A. Reed. Quantification of the affinities and kinetics of protein interactions using silicon nanowire biosensors. *Nature Nanotechnology*, 7(6):401–407, June 2012.

[24] Xiaojie Duan, Ruixuan Gao, Ping Xie, Tzahi Cohen-Karni, Quan Qing, Hwan Sung Choe, Bozhi Tian, Xiaocheng Jiang, and Charles M. Lieber. Intracellular recordings of action potentials by an extracellular nanoscale field-effect transistor. *Nature Nanotechnology*, 7(3):174–179, March 2012.

[25] Y. Cui, Q. Q. Wei, H. K. Park, and C. M. Lieber. Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species. *Science*, 293(5533):1289–1292, August 2001.

[26] J.P. Colinge and C. A. Colinge. *Physics of Semiconductor Devices*. Kluwer Academic Publishers, 2002.

[27] H. Ibach and H. Lüth. *Festköperphysik, Einführung in die Grundlagen*. Springer Verlage, 2002.

[28] Simon M. Sze and Kwok. K. Ng. *Physics of Semiconductor Devices*. John Wiley & Sons, 2006.

[29] Hitendra K. Malik and A. K. Singh. *Engineering Physics*. Tata McGraw Hill, 2012.

[30] Jean-Pierre Colinge. *Silicon-on-insulator technology, 3rd edition*. Springer, 2004.

[31] D. J. Wouters, J. P. Colinge, and H. E. Maes. Subthreshold slope in thin-film SOI MOSFETs. *IEEE Transactions On Electron Devices*, 37 (9):2022–2033, September 1990.

[32] J. R. Watling, L. F. Yang, A. Asenov, J. R. Barker, and S. Roy. Impact of high-k dielectric HfO2 on the mobility and device performance of sub-100-nm nMOSFETs. *IEEE Transactions On Device and Materials Reliability*, 5(1):103–108, March 2005.

[33] Jean-Pierre Colinge. *FinFETs and Other Multi-Gate Transistors*. Springer, 2006.

[34] M. Ostling M. von Haartman. *Low-Frequency Noise in Advanced MOS Devices*. Springer, 2007.

[35] Thomas Heinzel. *Mesoscopic Electronics in Solid State Nanostructures*. Wiley-VCH, 2010, third edition.

[36] P. Bergveld. Thirty years of ISFETOLOGY - what happened in the past 30 years and what may happen in the next 30 years. *Sensors and Actuators B-chemical*, 88(1):IMCS, January 2003.

[37] M. Waleed Shinwari, M. Jamal Deen, and Dolf Landheer. Study of the electrolyte-insulator-semiconductor field-effect transistor (EISFET) with applications in biosensor design. *Microelectronics Reliability*, 47 (12):2025–2057, December 2007.

[38] Brian J. Kirby. *Micro- and Nanoscale Fluid Mechanics, Transport in Microfluidic Devices*. 2010.

[39] Eric Stern, Robin Wagner, Fred J. Sigworth, Ronald Breaker, Tarek M. Fahmy, and Mark A. Reed. Importance of the Debye screening length on nanowire field effect transistor sensors. *Nano Letters*, 7(11):3405–3409, November 2007.

[40] D. E. Yates, S. Levine, and T. W. Healy. Site-binding model of electrical double-layer at oxide-water interface. *Journal of the Chemical Society-Faraday Transactions I*, 70:1807–1818, 1974.

[41] T. W. Healy, T. W. and L. R. White. Ionizable surface group models of aqueous interfaces. *Advances In Colloid and Interface Science*, 9(4): 303–345, 1978.

[42] L. Bousse, N. F. Derooij, and P. Bergveld. Operation of chemically sensitive field-effect sensors as a function of the insulator-electrolyte interface. *IEEE Transactions On Electron Devices*, 30(10):1263–1270, 1983.

[43] R. E. G. VanHal, J. C. T. Eijkel, and P. Bergveld, P. A novel description of ISFET sensitivity with the buffer capacity and double-layer capacitance as key parameters. *Sensors and Actuators B-chemical*, 24(1-3): 201–205, March 1995.

[44] Margaret Robson Wright. *An Introduction to Aqueous Eletrolyte Solutions*. John Wiley & Sons, 2007.

[45] P. Bergveld. ISFET, theroy and practice. *IEEE Sensor Conference Toronto*, pages 1–26, October 2003.

[46] Oren Knopfmacher, Alexey Tarasov, Mathias Wipf, Wangyang Fu, Michel Calame, and Christian Schönenberger. Silicon-based ion-sensitive field-effect transistor shows negligible dependence on salt concentration at constant pH. *Chemphyschem*, 13(5):1157–1160, April 2012.

[47] Xuan P. A. Gao, Gengfeng Zheng, and Charles M. Lieber. Subthreshold regime has the optimal sensitivity for nanowire FET biosensors. *Nano Letters*, 10(2):547–552, February 2010.

[48] A. L. McWorther. *Semiconductor Surface Physics*. University of Pennsylvania, Philadelphia, 1957.

[49] F. N. Hooge, T. G. M. Kleinpenning, and L. K. J. Vandamme. Experimental studies on 1/f noise. *Reports On Progress In Physics*, 44(5): 479–532, 1981.

[50] G. Ghibaudo. On the theory of carrier number fluctuations in MOS devices. *Solid-state Electronics*, 32(7):563–565, July 1989.

[51] N. Clement, K. Nishiguchi, J. F. Dufreche, D. Guerin, A. Fujiwara, and D. Vuillaume. A silicon nanowire ion-sensitive field-effect transistor with elementary charge sensitivity. *Applied Physics Letters*, 98(1): 014104, January 2011.

[52] F. N. Hooge. 1/f noise is no surface effect. *Physics Letters A*, A 29(3): 139–140, 1969.

[53] G. Ghibaudo, O. Roux, C. Nguyen-Duc, F. Balestra, and J. Brini. Improved analysis of low-frequency noise in field-effect MOS-transistors. *Physica Status Solidi A-applied Research*, 124(2):571–581, April 1991.

[54] J. D. Holmes, K. P. Johnston, R. C. Doty, and B. A. Korgel. Control of thickness and orientation of solution-grown silicon nanowires. *Science*, 287(5457):1471–1473, February 2000.

[55] http://www.soitec.com/en/in, February 2013.

[56] Marc J. Madou. *Fundamentals of Microfabrication*. CRC Press, 1997.

[57] Michael Köhler. *Etching with Microsystem Technology*. WILEY-VCH, 1999.

[58] Nitin K. Rajan, David A. Routenberg, Jin Chen, and Mark A. Reed. 1/f noise of silicon nanowire bioFETs. *IEEE Electron Device Letters*, 31(6):615–617, June 2010.

[59] http://www.srim.org/, February 2013.

[60] J. F. Ziegler. *Ion Implantation Science and Technology*. Edgewater, USA, 1996.

[61] S.M. Sze G.S. May. *Fundamentals of Semiconductor Fabrication*. John Wiley & Sons, 2007.

[62] K. E. Moselund, H. Ghoneim, H. Schmid, M. T. Bjoerk, E. Loertscher, S. Karg, G. Signorello, D. Webb, M. Tschudy, R. Beyeler, and H. Riel. Solid-state diffusion as an efficient doping method for silicon nanowires and nanowire field effect transistors. *Nanotechnology*, 21(43):435202, October 2010.

[63] Rajesh Katamreddy, Ronald Inman, Gregory Jursich, Axel Soulet, and Christos Takoudis. ALD and characterization of aluminum oxide deposited on Si (100) using tris(diethylamino) aluminum and water vapor. *Journal of the Electrochemical Society*, 153(10):C701–C706, 2006.

[64] W. Kern and D. A. Puotinen. Cleaning solutions based on hydrogen peroxide for use in silicon semiconductor technology. *RCA Review*, 31 (2):187, 1970.

[65] W. Kern. Citation classic - cleaning solutions based on hydrogen-peroxide for use in silicon semiconductor technology. *Current Contents/engineering Technology & Applied Sciences*, (11):18–18, 1983.

[66] H. Kim, P. C. McIntyre, and K. C. Saraswat. Effects of crystallization on the electrical properties of ultrathin HfO2 dielectrics grown by atomic layer deposition. *Applied Physics Letters*, 82(1):106–108, January 2003.

[67] L. Zhang, H. C. Jiang, C. Liu, J. W. Dong, and P. Chow. Annealing of Al2O3 thin films prepared by atomic layer deposition. *Journal of Physics D-applied Physics*, 40(12):3707–3713, June 2007.

[68] K. Bedner, V. A. Guzenko, A. Tarasov, M. Wipf, R. L. Stoop, D. Just, S. Rigante, W. Fu, R. A. Minamisawa, C. David, M. Calame, J. Gobrecht, and C. Schönenberger. pH response of silicon nanowire sensors: Impact of nanowire width and gate oxide. *accepted by Sensors and Materials*, 2013.

[69] K. Bedner, V. A. Guzenko, A. Tarasov, M. Wipf, R. L. Stoop, S. Rigante, J. Brunner, W. Fu, C. David, M. Calame, J. Gobrecht, and C. Schönenberger. Investigation of the dominant 1/f noise source in silicon nanowire sensors. *submitted to Sensors and Acutators B: Chemical*, 2013.

[70] S. M. Koo, Q. L. Li, M. D. Edelstein, C. A. Richter, and E. M. Vogel. Enhanced channel modulation in dual-gated silicon nanowire transistors. *Nano Letters*, 5(12):2519–2523, December 2005.

[71] Josh Goldberger, Allon I. Hochbaum, Rong Fan, and Peidong Yang. Silicon vertically integrated nanowire field effect transistors. *Nano Letters*, 6(5):973–977, May 2006.

[72] J. F. Conley, Y. Ono, R. Solanki, G. Stecker, and W. Zhuang. Electrical properties of HfO2 deposited via atomic layer deposition using Hf(NO3)(4) and H2O. *Applied Physics Letters*, 82(20):3508–3510, May 2003.

[73] Niklas Elfström, Robert Juhasz, Ilya Sychugov, Torun Engfeldt, Amelie Eriksson Karlstrom, and Jan Linnros. Surface charge sensitivity of silicon nanowires: Size dependence. *Nano Letters*, 7(9):2608–2612, September 2007.

[74] Jae-Hyuk Ahn, Sung-Jin Choi, Jin-Woo Han, Tae Jung Park, Sang Yup Lee, and Yang-Kyu Choi. Investigation of size dependence on sensitivity for nanowire FET biosensors. *IEEE Transactions On Nanotechnology*, 10(6):1405–1411, November 2011.

[75] Niklas Elfström and Jan Linnros. Sensitivity of silicon nanowires in biosensor applications. *Proceedings of the 17th International Vacuum Congress/13th International Conference On Surface Science/international Conference On Nanoscience and Technology*, 100: Swedish Vacuum Soc, 2008.

[76] Niklas Elfström, Amelie Eriksson Karlström, and Jan Linnrost. Silicon nanoribbons for electrical detection of biomolecules. *Nano Letters*, 8 (3):945–949, March 2008.

[77] L. A. Currie, L. A. and G. Svehla. Nomenclature for the presentation of results of chemical-analysis. *Pure and Applied Chemistry*, 66(3), March 1994.

[78] C. G. Jakobson and Y. Nemirovsky. 1/f noise in ion sensitive field effect transistors from subthreshold to saturation. *IEEE Transactions On Electron Devices*, 46(1):259–261, January 1999.

[79] Chengqing Wei, Yu Jiang, Yong-Zhong Xiong, Xing Zhou, Navab Singh, Subhash C. Rustagi, Guo Qiang Lo, and Dim-Lee Kwong. Impact of gate electrodes on 1/f noise of gate-all-around silicon nanowire transistors. *IEEE Electron Device Letters*, 30(10):1081–1083, October 2009.

[80] Nitin K. Rajan, David A. Routenberg, Jin Chen, and Mark A. Reed. Temperature dependence of 1/f noise mechanisms in silicon nanowire biochemical field effect transistors. *Applied Physics Letters*, 97(24): 243501, December 2010.

[81] Nitin K. Rajan, David A. Routenberg, and Mark A. Reed. Optimal signal-to-noise ratio for silicon nanowire biochemical sensors. *Applied Physics Letters*, 98(26):264107, June 2011.

[82] Chengqing Wei, Yong-Zhong Xiong, Xing Zhou, Navab Singh, Subhash C. Rustagi, Guo Qiang Lo, and Dim-Lee Kwong. Investigation of low-frequency noise in silicon nanowire MOSFETs in the subthreshold region. *IEEE Electron Device Letters*, 30(6):668–671, June 2009.

[83] A. Tarasov, W. Fu, O. Knopfmacher, J. Brunner, M. Calame, and C. Schönenberger. Signal-to-noise ratio in dual-gated silicon nanoribbon field-effect sensors. *Applied Physics Letters*, 98(1):012114, January 2011.

[84] Alexey Tarasov, Mathias Wipf, Ralph L. Stoop, Kristine Bedner, Wangyang Fu, Vitaliy A. Guzenko, Oren Knopfmacher, Michel Calame,

and Christian Schönenberger. Understanding the electrolyte background for biochemical sensing with ion-sensitive field-effect transistors. *ACS Nano*, 6(10):9291–9298, October 2012.

[85] Mathias Wipf, Ralph L. Stoop, Alexey Tarasov, Kristine Bedner, Wangyang Fu, Iain A. Wright, Colin J. Martin, Edwin C. Constable, Michel Calame, and Christian Schönenberger. Selective sodium sensing with gold-coated silicon nanowire field-effect transistors in a differential setup. *ACS nano*, 7(7):5978–83, July 2013.

[86] Alexey Tarasov. *Silicon Nanowire Field Effect Transistor for Sensing Applications*. PhD thesis, University of Basel, Department of Physics, 2012.

[87] Keithley. *Fundamentals of Semiconductor C-V Measurements*, February 2009.

[88] Yi Wei Chen, Maozi Liu, T. Kaneko, and P. C. McIntyre. Atomic layer deposited hafnium oxide gate dielectrics for charge-based biosensors. *Electrochemical and Solid-State Letters*, 13(3):G29–G32, 2010.

Publication List

Peer-reviewed Publications

- K. Bedner, V. A. Guzenko, A. Tarasov, M. Wipf, R. L. Stoop, D. Just, S. Rigante, W. Fu, R. A. Minamisawa, C. David, M. Calame, J. Gobrecht, C. Schönenberger. pH-Response of Silicon Nanowire Sensors: Impact of Nanowire Width and Gate Oxide, *(accepted by Sensors and Materials* (2013))

- K. Bedner, V. A. Guzenko, A. Tarasov, M. Wipf, R. L. Stoop, Sara Rigante, J. Brunner, W. Fu, C. David, M. Calame, J. Gobrecht, C. Schönenberger. Investigation of the dominant 1/f Noise Source in Silicon Nanowire Sensors, *(submitted to Sensors and Actuators B: Chemical* (2013))

- M. Wipf, R. L. Stoop, A. Tarasov, K. Bedner, W. Fu, I. A. Wright, C. J. Martin, E. C. Constable, M. Calame, C. Schönenberger. Selective sodium sensing with gold-coated silicon nanowire field-effect transistors in a differential setup, *ACS Nano* **7**, 5978-5983 (2013)

- P. Livi, K. Bedner A. Tarasov, M. Wipf, Y. Chen, C. Schönenberger and A. Hierlemann. A Verilog-A model for silicon nanowire biosensors: from theory to verification, *Sensors and Actuators B: Chemical* **179**, 293-300 (2013)

- A. Tarasov, M. Wipf, K. Bedner, J. Kurz, W. Fu, V. A. Guzenko, O. Knopfmacher, R. L. Stoop, M. Calame and C. Schönenberger. True Reference Electrode Realized with Silicon Nanowires, *Langmuir* **28**, 9899-9905 (2012)

- A. Tarasov, M. Wipf, R. L. Stoop, K. Bedner, W. Fu, V. A. Guzenko, O. Knopfmacher, M. Calame and C. Schönenberger. Understanding the Electrolyte Background for Biochemical Sensing with Ion-Sensitive Field-Effect Transistors, *ACS Nano* **6**, 9291-9298 (2012)

International Conferences

- K. Bedner, V. A. Guzenko, O. Knopfmacher, A. Tarasov, M. Wipf, D. Just, W. Fu, M. Calame, C. David, J. Gobrecht and C. Schönenberger. SOI-based Nanowire Field Effect Transistor Arrays for Sensing Applications. *37th International Conference on Micro and Nano Engineering* in Berlin, Germany, 19-23 September 2011, talk

- K. Bedner, V. A. Guzenko, M. Wipf, A. Tarasov, R. L. Stoop, R. Minamisawa, W. Fu, J. Brunner, C. David, M. Calame, J. Gobrecht and C. Schönenberger. Sensing with a Silicon Nanowire Ion Sensitive Field Effect Transistor: Effect of the Nanowire Width. *26th European Conference on Solid-State Transducers, Eurosensors 2012* in Krakow, Poland, 9-12 September 2012, talk

Acknowledgements

Many people contributed to this thesis and I am grateful to all of them. Fist and foremost, I would like to express my gratitude to my PhD supervisor Christian Schönenberger. He provided guidance at key moments in my work and helped with his immense knowledge to solve problems.
Besides my supervisor, I would like to thank the rest of the thesis committee: Christofer Hierold, Matthias Streiff, Michel Calame and Vitaliy Guzenko.
I also have to thank Jens Gobrecht and Christian David for their support to make this work possible.
I am especially grateful to Vitaliy Guzenko, who was always available to advise me and support me.
I thank Mathias Wipf, Alexey Tarasov, Ralph Stoop, Wangyang Fu and Oren Knopfmacher for their help to run my measurements in Basel, for all discussions and the fun we had in the mountains.
I wish to thank all technicians Arnold Lücke, Stefan Stutz, Thomas Neiger, Konrad Vogelsang, Anja Weber, Bianca Haas and Jana Lehmann for their technical help in the labs.
The SiNW project was funded by the Swiss funding agency Nano Tera and it was a consortium of several project partners. Thereby I had the pleasure to work with many people in Switzerland. I would like to thank Sara Rigante for the deposition and characterization of the ALD oxides.
Special thanks to my office mates, Simon Rutishauser, Christian Spreu and Jonathan Perron. It was a great time to share the office with them.
I am grateful to the secretaries at LMN, Edith Meisel and the Uni Basel, Department of Physics, Barbara Kammermann and Astrid Kalt for the administrative support.
My thanks also go to Dominik Zumbühl for everything I learned from him.
Lastly, and most importantly, I wish to thank my parents. They always supported me and loved me!