

**Reference Spurs in an Integer- $N$   
Phase-Locked Loop: Analysis,  
Modelling and Design**

by

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# Contents

Heading	Page
Contents	iii
Abstract	ix
Statement of Originality	xi
Acknowledgments	xiii
Thesis Conventions	xv
Publications	xvii
List of Figures	xix
List of Tables	xxv
<b>Chapter 1. Introduction</b>	<b>1</b>
1.1 Introduction . . . . .	2
1.2 GLIMMR . . . . .	2
1.2.1 60 GHz Band . . . . .	3
1.3 Frequency Synthesiser . . . . .	5
1.4 Motivation . . . . .	6
1.5 Major Contributions . . . . .	7
1.6 Thesis Outline . . . . .	8
<b>Chapter 2. Phase-Locked Loop Fundamentals</b>	<b>11</b>
2.1 Introduction . . . . .	12
2.2 Phase-Locked Loop Types . . . . .	14
2.2.1 Linear PLL . . . . .	14

2.2.2	All-digital PLL . . . . .	16
2.2.3	Digital PLL . . . . .	17
2.3	Phase-Locked Loop Architectures . . . . .	18
2.3.1	Integer- $N$ . . . . .	19
2.3.2	Fractional- $N$ . . . . .	20
2.4	Charge Pump PLL Component . . . . .	21
2.4.1	Reference clock . . . . .	21
2.4.2	Phase/frequency detector . . . . .	22
2.4.3	Charge pump . . . . .	23
2.4.4	Loop filter . . . . .	25
2.4.5	Voltage-Controlled Oscillator . . . . .	26
2.4.6	Frequency divider . . . . .	31
2.5	PLL for 60 GHz RF Transceiver . . . . .	32
2.5.1	PLL planning . . . . .	34
2.5.2	PLL simulation challenge . . . . .	35
2.5.3	PLL design challenge . . . . .	36
2.5.4	Reference spur issue . . . . .	39
2.6	Chapter Summary . . . . .	39
<b>Chapter 3. Phase-Locked Loop Noise</b>		<b>41</b>
3.1	Introduction . . . . .	42
3.2	Phase Noise . . . . .	43
3.3	Phase Noise Effect on RF Communication Systems . . . . .	44
3.4	Phase Noise in PLL . . . . .	45
3.4.1	PLL phase noise spectrum . . . . .	48
3.5	PLL Reference Spurs . . . . .	53
3.5.1	PFD delay . . . . .	54
3.5.2	Charge pump current mismatch . . . . .	55
3.5.3	Charge pump current leakage . . . . .	55
3.5.4	Switching delay . . . . .	56
3.5.5	Charge pump current rise and fall time characteristics . . . . .	57
3.5.6	Charge injection and charge sharing . . . . .	57
3.6	Chapter Summary . . . . .	58

<b>Chapter 4. Reference Spur Analysis</b>	<b>59</b>
4.1 Introduction . . . . .	60
4.2 Spur Magnitude . . . . .	61
4.3 VCO Tuning Voltage . . . . .	64
4.3.1 Charge pump current mismatch and PFD delay effect . . . . .	65
4.3.2 Charge pump switching delay effect . . . . .	67
4.3.3 Charge pump current rise and fall time characteristics . . . . .	68
4.3.4 Charge pump current leakage . . . . .	68
4.3.5 Loop filter order effect . . . . .	69
4.3.6 Tuning voltage ripple magnitude . . . . .	71
4.4 Analysis Verification . . . . .	72
4.5 Effect of Charge Pump Non-idealities . . . . .	75
4.6 Chapter Summary . . . . .	75
<b>Chapter 5. Reference Spur Behavioural Modelling</b>	<b>79</b>
5.1 Introduction . . . . .	80
5.2 PLL Behavioural Model Characterisation . . . . .	81
5.2.1 PFD characterisation . . . . .	81
5.2.2 Charge pump characterisation . . . . .	82
5.2.3 VCO characterisation . . . . .	84
5.3 Simulink Behavioural Modelling . . . . .	85
5.3.1 PFD Simulink . . . . .	86
5.3.2 Charge pump Simulink . . . . .	86
5.3.3 Loop filter Simulink . . . . .	91
5.3.4 VCO Simulink . . . . .	91
5.3.5 Frequency divider Simulink . . . . .	93
5.4 PLL Behavioural Modelling Result . . . . .	93
5.4.1 Reference spur . . . . .	94
5.4.2 PLL settling time . . . . .	94
5.5 Chapter Summary . . . . .	94

<b>Chapter 6. Spur Suppression Design Technique</b>	<b>97</b>
6.1 Introduction . . . . .	98
6.2 Reference Spur Suppression Technique Reviews . . . . .	98
6.2.1 Low VCO gain . . . . .	99
6.2.2 Improved charge pump circuit . . . . .	100
6.2.3 Other methods . . . . .	102
6.2.4 Spur suppression technique comparisons . . . . .	103
6.3 Ratioed Current Charge Pump . . . . .	103
6.4 Reference Spur Suppression Performance Estimation . . . . .	108
6.5 Chapter Summary . . . . .	113
<b>Chapter 7. PLL Circuit Design</b>	<b>115</b>
7.1 Introduction . . . . .	116
7.2 PLL Component Design . . . . .	116
7.2.1 Charge pump . . . . .	116
7.2.2 VCO . . . . .	119
7.2.3 Frequency divider . . . . .	123
7.2.4 Prescaler . . . . .	124
7.2.5 PFD . . . . .	130
7.2.6 Loop filter . . . . .	134
7.3 PLL Performance . . . . .	139
7.3.1 PLL phase noise . . . . .	140
7.3.2 PLL reference spur . . . . .	140
7.4 Chapter Summary . . . . .	141
<b>Chapter 8. Thesis Summary</b>	<b>145</b>
8.1 Analysis . . . . .	146
8.2 Modelling . . . . .	147
8.3 Design . . . . .	148
<b>Appendix A. Matlab codes</b>	<b>149</b>
A.1 Ripple voltage amplitude calculation . . . . .	150
A.2 Charge pump current generation . . . . .	152
A.3 Third order filter equations . . . . .	153

<b>Appendix B. Test chips</b>	<b>155</b>
B.1 GLIMMR Test Chips . . . . .	156
<b>Bibliography</b>	<b>159</b>
<b>List of Acronyms</b>	<b>169</b>
<b>Index</b>	<b>171</b>
<b>Biography</b>	<b>173</b>

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# Abstract

The Phase-Locked Loop (PLL) is commonly used for frequency synthesis in RF transceivers. It can be implemented in two architectures, namely, fractional- $N$  and integer- $N$ . In this thesis, the integer- $N$  architecture is chosen due to its suitability for frequency planning.

Here, a PLL with a low noise output is important to ensure signal purity. There are two dominant noise sources in a PLL, namely, phase noise and periodic noise. In the integer- $N$  PLL, periodic noise is also referred to as a reference spur, where the noise gives rise to multiple reference frequency offsets at the PLL output. Of these two noise sources, this thesis is focused on the analysis and suppression of reference spurs. It is because less work has been carried in the literature regarding spurs, and phase noise is better studied. The main factors underlying reference spurs are discussed. These factors are mainly from the charge pump and phase/frequency detector (PFD) circuit non-idealities, namely, PFD delay, charge pump current leakage, charge pump current mismatch, and rise and fall times characteristic of the charge pump current.

Reference spur magnitude can be predicted via a transient analysis. The simulation is time consuming, as the reference spur magnitude can only be captured after the PLL in its locked state. Therefore, the simulation period has to be set long enough to ensure enough data can be obtained to read that state. In this thesis, a reference spur mathematical analysis is presented to accurately estimate the reference spur magnitude. In the analysis, all the circuit non-idealities that contribute to the reference spur are considered. Circuit parameters required in the mathematical analysis can be obtained from transistor level simulation for each circuit. As the simulation for each circuit can be carried out separately, a large amount of simulation time can be saved. The proposed mathematical analysis also can be used to determine the major contributing factor to the problem of reference spurs.

The reference spur also can be estimated via behavioural modelling simulation. Behavioural modelling of the PLL using Simulink is presented in this thesis. Each PLL component is modelled separately, and circuit non-idealities contributing to the reference spur are included in the behavioural model. In addition to reference spur estimation,

the PLL behavioural model also can be used to visualise the dynamic behaviour of the system.

Results from the spur analysis show that a slight mismatch current in the charge pump helps to improve the reference spur performance. This thesis presents an analysis to determine an optimum charge pump current ratio for reference spur suppression, which is caused by the charge pump current mismatch and the switching delay. Further, a ratioed current charge pump circuit is proposed to replace the conventional charge pump circuit for a reference spur performance improvement. This spur suppression technique is implemented using a 180 nm SiGe BiCMOS technology for performance evaluation.

# Statement of Originality

This work contains no material that has been accepted for the award of any other degree or diploma in any university or other tertiary institution and, to the best of my knowledge and belief, contains no material previously published written by another person, except where due reference has been made in the text.

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11<sup>th</sup> January 2013

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Date

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**Noorfazila Kamal**

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# Thesis Conventions

The following conventions have been adopted in this Thesis:

1. **Notation.** The acronyms used in this thesis are defined in the List of Acronyms on page 169.
2. **Spelling.** Australian English spelling conventions have been used, as defined in the Macquarie English Dictionary (A. Delbridge (Ed.), Macquarie Library, North Ryde, NSW, Australia, 2001). Where two alternative spellings are allowed such as *biassing* or *biasing*, the shorter option is chosen. Also the word *analogue* is written *analog* due to its widespread usage in the engineering literature, even though it is not an Australian spelling.
3. **Typesetting.** This document was compiled using L<sup>A</sup>T<sub>E</sub>X2e. TeXnicCenter was used as text editor interfaced to L<sup>A</sup>T<sub>E</sub>X2e. TGIF was used to produce schematic diagrams and other drawings.
4. **Mathematics.** MATLAB code was written using MATLAB Version R2009a.
5. **Referencing.** The Harvard style has been adopted for referencing.
5. **Punctuation.** The Oxford convention for commas has been used for punctuation.

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# Publications

- KAMAL-N., AL-SARAWI S. F., AND ABBOTT-.D.** (2012). An accurate analytical spur model for an integer- $N$  phase-locked loop, *Proceedings of 4th International Conference on Intelligent and Advanced Systems, (ICIAS 2012)*, Vol. 2, pp. 659-664
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- KAMAL-N., AL-SARAWI S. F., WESTE-N. H. E., AND ABBOTT-.D.** (2010). A phase-locked loop reference spur modelling using Simulink, *Proceedings of International Conference on Electronic Devices, Systems and Applications, (ICEDSA 2010)*, pp. 279-283.
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# List of Figures

Figure		Page
1.1	A double conversion receiver proposed by GLIMMR . . . . .	3
1.2	International band allocation in the 60 GHz region . . . . .	4
1.3	Roles of a frequency synthesiser in RF transceivers . . . . .	5
<hr/>		
2.1	Phase-Locked Loop . . . . .	13
2.2	Low pass filter for linear PLL . . . . .	15
2.3	A tri-state PFD in a digital PLL . . . . .	18
2.4	Prescaler in an integer- $N$ architecture . . . . .	19
2.5	A charge pump PLL . . . . .	21
2.6	Phase/frequency detector (PFD) . . . . .	22
2.7	PFD timing diagram . . . . .	23
2.8	PFD input output characteristic . . . . .	23
2.9	A basic charge pump schematic . . . . .	24
2.10	Charge pump topology . . . . .	24
2.11	Second order low pass filter . . . . .	26
2.12	Differential cross-coupled LC oscillator . . . . .	27
2.13	An RLC parallel circuit . . . . .	27
2.14	A $-g_m$ oscillator . . . . .	28
2.15	Accumulation MOS varactor . . . . .	29
2.16	A Miller theorem based varactor . . . . .	30
2.17	A VIC connected to an LC cross-coupled VCO . . . . .	31
2.18	A master-slave frequency divider . . . . .	32
2.19	A regenerative frequency divider . . . . .	33
2.20	A double-conversion super-heterodyne architecture . . . . .	34
2.21	A switched capacitor VCO . . . . .	37

## List of Figures

---

2.22	Coarse and fine tuning VCO . . . . .	38
2.23	Differential tuning VCO . . . . .	39
<hr/>		
3.1	Power Spectral Density (PSD) of a synthesiser output . . . . .	42
3.2	Reciprocal mixing . . . . .	45
3.3	Effect of poor phase noise on a transmitter . . . . .	45
3.4	Effect of a strong reference spur in the receiver . . . . .	46
3.5	Charge pump PLL linear phase model . . . . .	46
3.6	VCO noise spectrum . . . . .	49
3.7	Frequency divider noise spectrum . . . . .	50
3.8	Charge pump current noise spectrum . . . . .	51
3.9	Loop filter noise spectrum . . . . .	52
3.10	PLL noise spectrum . . . . .	53
3.11	PFD and charge pump circuits . . . . .	54
3.12	Charge pump circuit with a switching delay . . . . .	56
3.13	Charge pump current rise and fall times . . . . .	57
<hr/>		
4.1	VCO tuning voltage . . . . .	61
4.2	A source-switched charge pump circuit . . . . .	65
4.3	Effect of a current mismatch to the PFD delay ( $t_{\text{PFD}}$ ) . . . . .	66
4.4	Effect of the UP signal switching delay on the VCO tuning voltage . . . . .	67
4.5	Second order low pass filter . . . . .	70
4.6	Third order low pass filter . . . . .	70
4.7	Reference spur model verification for a third and fourth order PLL . . . . .	73
4.8	Ripple magnitude ( $\Delta V$ ) model verification for a third and fourth order PLL . . . . .	74
4.9	Effect of VCO gain and charge pump non-idealities on the reference spur magnitude . . . . .	76
<hr/>		
5.1	PFD simulation setup . . . . .	82

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5.2	PFD timing diagram . . . . .	82
5.3	Charge pump current leakage simulation setup for a fourth order PLL .	83
5.4	A VCO tuning port current leakage simulation setup . . . . .	83
5.5	Charge pump mismatch current . . . . .	84
5.6	Rise and fall time characteristics of $I_{up}$ current . . . . .	85
5.7	VCO output frequency ( $f_o$ ) as a function of tuning voltage ( $V_{tune}$ ) . . . .	86
5.8	PLL Simulink model for a third and fourth order PLL . . . . .	87
5.9	PFD Simulink model . . . . .	88
5.10	Charge pump current: a comparison between interpolation and curve fitting methods . . . . .	89
5.11	Charge pump Simulink model . . . . .	89
5.12	Rise and fall time characteristics sub-system . . . . .	90
5.13	VCO frequency: a comparison between the interpolation and curve fitting method . . . . .	92
5.14	VCO Simulink model . . . . .	92
5.15	Frequency divider Simulink model . . . . .	93
5.16	Reference spur magnitude comparison between transistor level simulation and Simulink model for a third and fourth order PLL . . . . .	95
5.17	VCO tuning voltage comparison between a transistor level simulation and Simulink model for a third and fourth order PLL . . . . .	96
<hr/>		
6.1	Charge pump with bias generator circuit . . . . .	100
6.2	Charge pump error amplifier compensation circuit . . . . .	101
6.3	Randomised ripple on the tuning voltage . . . . .	103
6.4	Timing diagram for charge pump current when $I_{dn} > I_{up}$ . . . . .	105
6.5	Charge pump circuit . . . . .	106
6.6	Four different charge pump circuits . . . . .	109
6.7	Charge pump current, $I_{up}$ and $I_{dn}$ , for four charge pump topologies . . .	110
6.8	Reference spur magnitude comparison . . . . .	111
6.9	VCO tuning voltage comparison . . . . .	112

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## List of Figures

---

7.1	Rail-to-rail amplifier . . . . .	117
7.2	Charge pump current, $I_{up}$ and $I_{dn}$ , for three different charge pump topologies . . . . .	118
7.3	Ratioed current charge pump layout . . . . .	118
7.4	Open and closed-loop charge pump current noise for the conventional, ratioed current, and ratioed with matched current charge pumps . . . . .	119
7.5	LC cross-coupled differential VCO schematic . . . . .	120
7.6	VCO layout . . . . .	121
7.7	VCO output frequency as a function of tuning voltage . . . . .	121
7.8	The VCO open loop and closed-loop noise . . . . .	122
7.9	Master-slave frequency divider schematic . . . . .	124
7.10	Master-slave frequency divider layout . . . . .	124
7.11	Master-slave frequency divider micrograph . . . . .	125
7.12	Master-slave frequency divider measurement result . . . . .	125
7.13	Prescaler . . . . .	126
7.14	Dual modulus divider . . . . .	126
7.15	OR and AND gates implementation in an ECL topology . . . . .	127
7.16	$P$ counter . . . . .	127
7.17	$S$ counter . . . . .	128
7.18	ECL-to-CMOS converter . . . . .	129
7.19	Prescaler layout . . . . .	129
7.20	Dual modulus divider simulation result . . . . .	130
7.21	Prescaler simulation results for four different digital inputs . . . . .	131
7.22	Prescaler measurement results . . . . .	132
7.23	Frequency divider and prescaler phase noise . . . . .	133
7.24	PFD circuit . . . . .	133
7.25	D flip-flop circuit . . . . .	134
7.26	PFD layout . . . . .	134
7.27	Third order low pass filter . . . . .	138

7.28	Third order loop filter noise spectrum . . . . .	139
7.29	PLL layout . . . . .	140
7.30	PLL phase noise . . . . .	141
7.31	Reference spur magnitude comparison . . . . .	142
<hr/>		
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B.1	GLIMMR test chip 1 (GTC1) . . . . .	156
B.2	GLIMMR test chip 2 (GTC2) . . . . .	157
B.3	PLL in the GLIMMR test chip 3 (GTC3) . . . . .	158

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# List of Tables

Table	Page
2.1 Frequency planning . . . . .	35
6.1 Spur suppression technique comparison . . . . .	104
7.1 VCO performance comparison . . . . .	123
7.2 Performance summary of the ratioed with matched current charge pump PLL . . . . .	143