Enhancement of Antimonide-based P-Channel Quantum-Well Field Effect Transistors Using Process-Induced Strain

by

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B.S. Electrical Engineering, California Institute of Technology (2011)

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of

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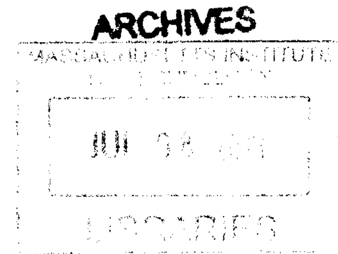

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ABSTRACT

For decades, the scaling of silicon CMOS has brought impressive growth to the semiconductor industry, as well as a wealth of technological innovations. However, the continued scaling of CMOS devices to the nanometer regime is now threatened by intrinsic limitations to the use of silicon as the channel material. Hence, there is a strong interest in III-V semiconductor materials to replace silicon as the channel material as a result of their outstanding electron transport properties.

While III-V materials have demonstrated impressive n-channel field-effect transistors (FETs), the same success has not yet been translated to the development of a high-performance III-V p-channel FET. This is because while many III-V's have high electron mobilities, they generally have very poor hole mobilities. The development of a high-performance III-V p-channel FET is critical to the realization of a future-generation III-V CMOS architecture.

Among the III-Vs, the antimonides have the highest hole mobilities. This makes them attractive for developing a III-V p-channel FET. This thesis examines the use of process-induced uniaxial strain combined with biaxial strain introduced during growth of the heterostructure as an approach to enhance antimonide-based FETs. Using a compressively stressed silicon nitride layer to induce uniaxial strain in the device, stressed devices with an InGaSb channel were fabricated and compared with unstressed devices processed in parallel. Enhancements of >50% in the intrinsic transconductance were observed as well as reductions of >30% in the source-drain resistance. This work illustrates the effectiveness of uniaxial strain in improving the performance of antimonide FETs.

Thesis Supervisor: Jesús A. del Alamo
Title: Professor of Electrical Engineering

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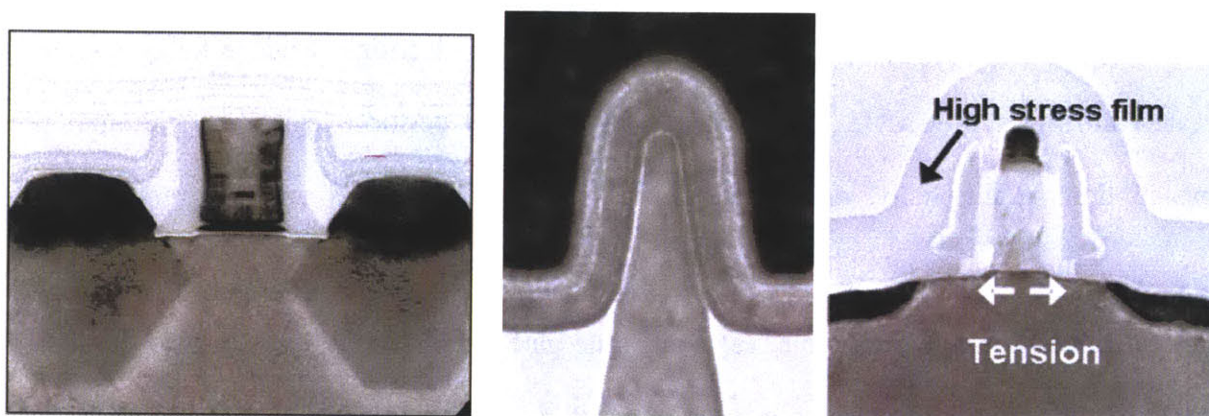
Chapter 1: INTRODUCTION

1.1 Silicon CMOS

For decades, innovation and advancements in electronics technology has been fueled by growth of the semiconductor industry. Integrated complementary metal-oxide semiconductor (CMOS) circuits have found their way into virtually all consumer electronic devices today. One of the greatest attributes of CMOS technology is its ability to perform logic with minimal power consumption. Additionally, at the heart of the growth of CMOS and the microelectronics industry is the concept of scaling. Device engineers realized very early on that decreasing the physical dimensions of transistors, especially the gate length, offered two great benefits: 1) a decrease in the cost-per-transistor, as more transistors can be fabricated on a single wafer, and 2) an increase in device performance, such as switching frequency and on-current. The concept of scaling has been so critical to growth in the semiconductor industry that industry-wide standards and benchmarks, known collectively as the International Technology Roadmap for Semiconductors (ITRS), have been created [1].

However, as devices were scaled more and more aggressively, a number of challenges had to be overcome. For instance, as the gate length is scaled, electrostatic modulation of the channel by the gate becomes more difficult, making it more challenging to turn the device on and off. As the footprint of the transistor is made smaller, making low-resistance contacts to the devices also becomes a problem. Another issue that had plagued CMOS for many years was the problem associated with PMOS transistors. It would be advantageous for CMOS to have both the NMOS

and PMOS devices behave similarly in terms of device performance. Some of these issues have been solved or mitigated using a variety of interesting techniques that have been successfully incorporated into mainstream silicon manufacturing, including the use of metal gate and high-k (high permittivity) dielectrics to replace polysilicon gates and silicon dioxide [2], multiple-gate device structures as opposed to strictly planar devices [3, 4], and strain [5, 6]. Figure 1 shows images of these key Si CMOS technologies.



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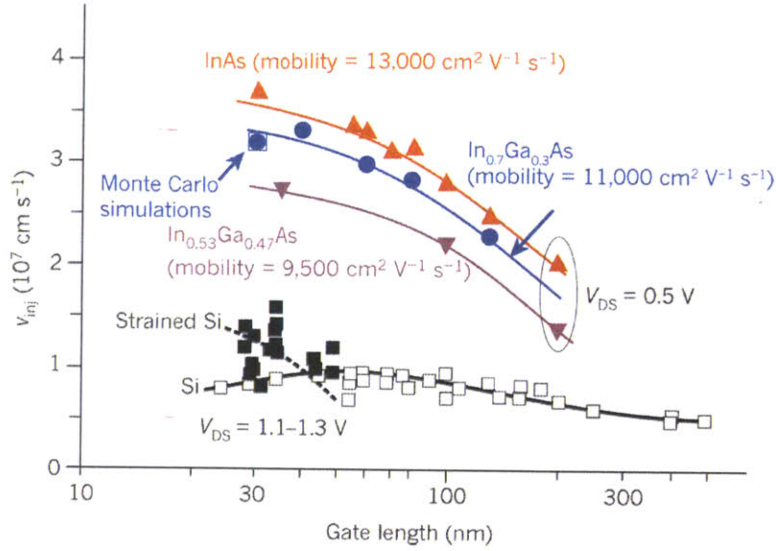
1.2 III-V CMOS

In today's regime of deeply-scaled CMOS, it has become evident that the continued use of silicon as the channel material presents a great challenge due to some intrinsic limitations of silicon. A major disadvantage of silicon is its limited source injection velocity, which is important in determining the switching speed and on-current of a transistor [7]. Additionally, as the density of transistors on a chip increases, a major limitation to further scaling is heat dissipation and cooling, giving rise to an era of "power-constrained scaling." To overcome this, one would like to reduce the operating voltage of the transistors and hence reduce the power consumption. While the operating voltage of silicon CMOS has declined over the years to roughly ~1 V today, there is great skepticism as to whether it can be reduced further without significantly compromising other aspects of device performance.

With these growing concerns over the continued scaling of silicon devices to the nanometer regime, other materials are being actively explored for use as alternative channel materials to replace silicon. III-V compound semiconductors have been particularly attractive as an alternative channel material because of their outstanding electron transport properties [8]. Fabricated III-V n-channel FETs have demonstrated source injection velocities twice as high as that of state-of-the-art silicon devices despite operating at a lower voltage [9]. Many of the techniques that previously found success with silicon devices, such as high-k dielectrics and non-planar device structures, are now being actively studied and developed for III-V devices [10, 11]. The importance of III-V materials is now broadly recognized, and they have been incorporated into the ITRS roadmap [1].



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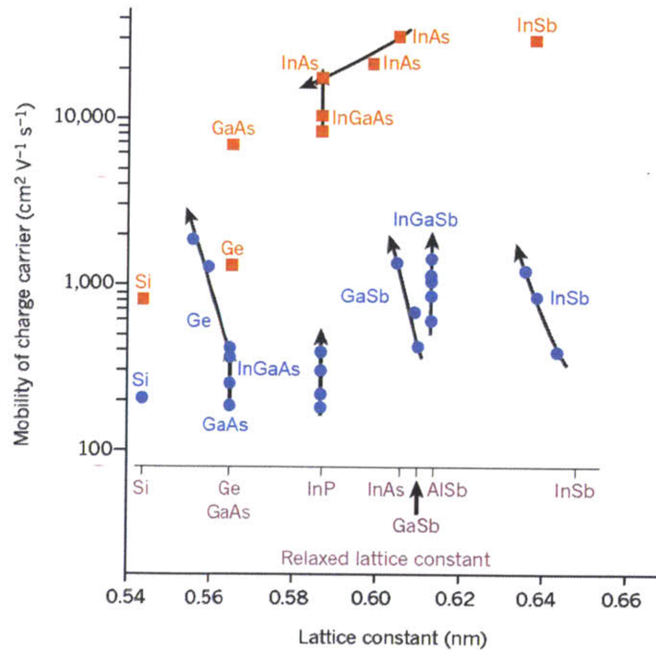


Figure 3: A plot of electron and hole mobilities for different semiconductor materials. Note that while many III-V's have outstanding electron mobilities, they can have low hole mobilities comparable to that of silicon. Image adapted from [8].

1.3 Motivation for Antimonides and Strain

However, while III-V materials have found great success in developing high-performance n-channel devices, development of a III-V p-channel device has been lacking. This is primarily due to the fact that while III-V materials such as InGaAs have impressive electron mobilities, the hole mobilities of most III-V materials are very poor, as illustrated in Figure 3. This huge disparity between n-channel and p-channel performance for III-V is a major hindrance to the integration of III-V materials with future-generation CMOS technologies.

A notable exception to this is the antimonide material system, which has the largest hole mobility among all III-V materials. This makes the use of antimonides an excellent starting point for developing a high-performance p-channel device. To further enhance the performance of antimonide devices, compressive strain can be used to increase the hole mobility. The use of strain has already found success in mainstream silicon CMOS manufacturing and was introduced at the 90 nm node in 2003 [5]. Through the use of strain, the performance disparity between Si NMOS and PMOS transistors was reduced significantly. Naturally, it would be advantageous to introduce the technique of strain to enhance antimonide devices.

One approach to achieve compressive strain is to introduce the strain during molecular beam epitaxy (MBE) growth of the antimonide heterostructure. By growing an antimonide channel layer on a relaxed buffer with a smaller lattice constant, the lattice constant of the channel layer would have to be reduced (compressed) in order to be lattice-matched to the epitaxial layers underneath. For sufficiently thin channel layers below a critical thickness, the strain can be incorporated into the heterostructure without relaxation and significant defects. Using this

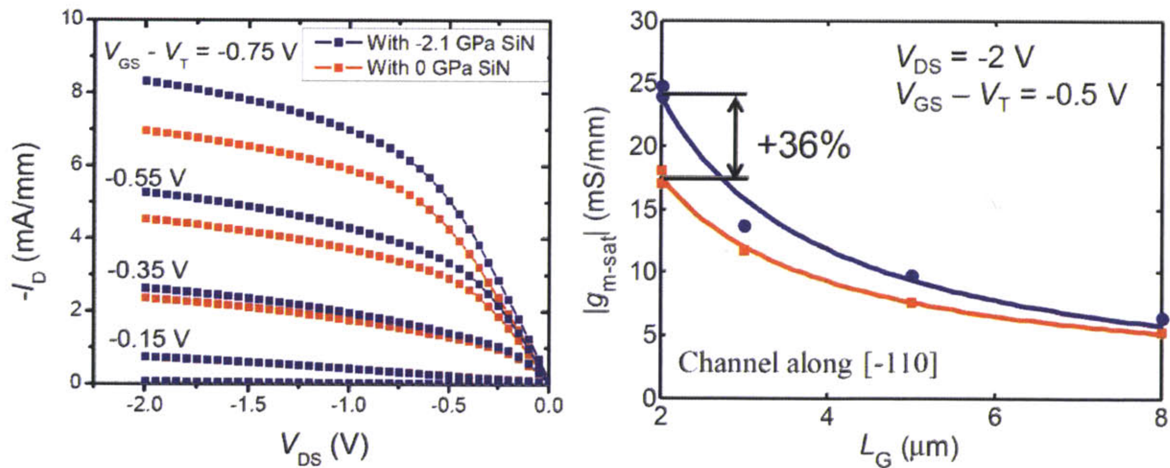
approach to incorporate the strain results in biaxial strain, meaning the strain is in all directions along the plane of the wafer, as opposed to just one direction (uniaxial strain).

In 2007, *Bennett et al.* demonstrated $In_xGa_{1-x}Sb$ quantum well heterostructures with 2% compressive biaxial strain and room temperature hole mobilities as high as 1500 cm^2/Vs [12]. Some of these strained heterostructures were then used to successfully fabricate 0.25 μm gate length p-channel devices with a maximum DC transconductance of 133 mS/mm [13]. In 2008, *Radosavljevic et al.* from Intel demonstrated p-channel FETs using a 1.9% compressively stressed InSb channel with a gate length of 40 nm and a maximum DC transconductance of 510 mS/mm, the largest ever reported for a III-V p-channel device [14]. Antimonide devices with a high-k dielectric incorporating biaxial strain have also been fabricated. *Nainani et al.* demonstrated long-channel devices with an Al_2O_3 dielectric and a 1.7% compressively strained InGaSb channel [15].

Another approach is to introduce the strain uniaxially via processing. In fact, it has been found in some materials that uniaxial strain can be used in combination with biaxial strain to enhance p-channel device performance even further. This has been observed in both SiGe and InGaAs. In 2010, *Gomez et al.* showed that with $Si_{1-x}Ge_x$ the additive mobility enhancement from a combination of biaxial and uniaxial strain was larger than what one would expect from adding the enhancements from biaxial and uniaxial strain individually [16]. The uniaxial strain was applied mechanically via bending experiments. In 2011, *Xia et al.* described a device structure incorporating process-induced strain using a stressed dielectric layer to enhance InGaAs p-channel devices [17]. A stressed nitride layer was deposited via plasma-enhanced chemical vapor deposition (PECVD). Using this process-induced approach to apply the strain, much higher levels of stress were obtained compared to the stress levels induced from just chip bending

experiments [18]. While a 36% improvement in the transconductance was observed with 2 μm gate length devices, as shown in Figure 4, the devices were still limited by the intrinsically low hole mobilities of InGaAs.

In 2011, *Xia et al.* also performed a study on the effect of uniaxial strain on biaxially strained InGaSb p-channel FETs [19]. The studies showed that the antimonides respond favorably to uniaxial strain. However, the study consisted of chip-bending experiments and hence the induced strain was limited to compressive stresses less than 100 MPa in magnitude. Given that the starting hole mobilities of InGaSb are much higher than that of InGaAs, it is possible that the enhancements seen by InGaSb from stress could be much higher than that of InGaAs.



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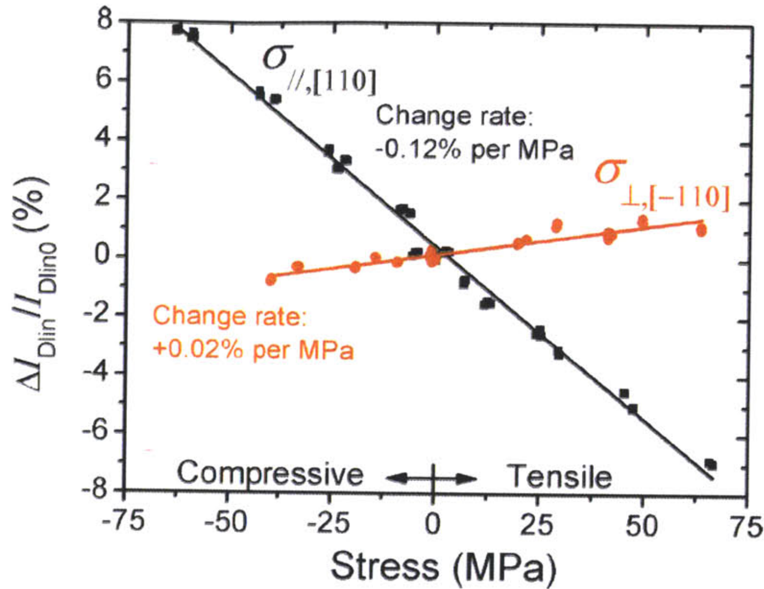

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With p-channel research actively being pursued with $In_xGa_{1-x}As$, Ge, and $In_xGa_{1-x}Sb$, what are the trade-offs between these materials? The advantage of $In_xGa_{1-x}As$ is its demonstrated superior electron transport properties and n-channel performance. Unfortunately, the hole mobility of $In_xGa_{1-x}As$ is significantly worse than that of Ge and $In_xGa_{1-x}Sb$, as can be seen from Figure 3. While strained Ge has demonstrated high hole mobilities, its relatively poor electron mobility limits its potential use as a channel material for high-performance n-channel devices. This suggests that perhaps the best solution would be to have an architecture that integrates together the n-channel $In_xGa_{1-x}As$ and p-channel Ge. While attractive, this approach presents a plethora of integration challenges because of their different lattice constants. Additionally, it has been found that increasing the indium composition of $In_xGa_{1-x}As$ generally increases the electron mobility,

and InAs, in fact, has a lattice constant closer to that of InGaSb than Ge. Finally, unlike InGaAs and Ge, InGaSb has electron and hole mobilities that are more comparable, suggesting the possibility of future III-V CMOS design with the same channel material [20].

1.4 Thesis Goals and Outline

Given the favorable response of antimonide devices to uniaxial strain from chip-bending experiments in the study of *Xia et al.* [19], straining antimonides using both uniaxial and biaxial strain appears to be a promising approach to developing a high-performance III-V p-channel FET. Additionally, antimonides are a desirable class of materials to work with because of their superior hole transport properties over arsenides and other III-V materials. For these reasons, it is the goal of this thesis is to fabricate a process-induced high uniaxially stressed device architecture to test the feasibility of uniaxial stress in enhancing antimonide-based FETs.

In order to achieve the high levels of stress needed to see significant device enhancement, a process-induced approach to incorporate the uniaxial stress was chosen over chip-bending experiments. Chapter 2 describes in detail the device architecture and fabrication steps used to implement the uniaxial stress. The chapter will also discuss some mechanical stress simulations and illustrate how the effect of scaling the architecture increases the magnitude of the stress in the channel. Chapter 3 then goes on to discuss the device characterization and results, comparing the results between stressed and unstressed devices. Finally, Chapter 4 summarizes some of the conclusions and presents some ideas on further work to be done.

Chapter 2: DEVICE ARCHITECTURE AND FABRICATION

2.1 Introduction to HEMT and Device Heterostructure

In order to study the impact of strain on enhancing antimonide-based p-channel FETs, a device architecture that allows for high compressive stress in the channel is needed. It would also be advantageous for the device structure to have scalability, so that the effect of stress on device performance can be studied as a function of the scaling. In addition, the architecture should allow for both biaxial and uniaxial strain to study the effect of superimposing these two types of stresses.

To study the effect of strain, a device structure similar to that of a high electron mobility transistor (HEMT) was adopted. The HEMT, also sometimes referred to as a heterojunction field-effect transistor (HFET), is a type of compound semiconductor field-effect transistor where the channel is created through the growth of epitaxial layers of materials with different band gaps [21]. With appropriate conduction (valence) band offsets, a two dimensional electron (hole) gas can be created from quantum confinement, creating a low-resistance conducting channel. This type of device structure is different from that of a conventional Si MOSFET which normally has a doped channel. Because in a HEMT there is no doping in the channel, higher carrier mobilities can be achieved as a result of the absence of impurity scattering (there are, however, sometimes delta doping layers implemented near but outside the channel layer to set the carrier concentration in the channel).

Additionally, another fundamental difference between a Si MOSFET and a HEMT is that while a MOSFET uses an oxide as the insulating layer between the gate and channel layer, a HEMT uses a wide band gap semiconductor as a barrier. For this reason, the barrier of a HEMT can be incorporated into the device structure during growth of the heterostructure rather than in subsequent processing steps. However, despite the convenience of this approach, there are some drawbacks. Firstly, because the barrier layer must be incorporated during the epitaxial growth of the heterostructure, the growth can become more complicated as a result of lattice-matching requirements and the need for sufficiently large enough conduction or valence band offsets. This significantly reduces the number of materials that can be grown and used effectively as a barrier. Secondly, because barriers normally have band gaps and offsets smaller than those of oxides used in MOSFETs, the gate leakage can be much larger. This problem can sometimes be mitigated by increasing the thickness of the barrier in HEMTs. However, doing so also reduces the ability of the gate to electrostatically modulate the channel, decreasing the transconductance and limiting the I_{on}/I_{off} ratio. Thirdly, the use of a barrier can present a challenge to achieving low series resistance. Because of the barrier's intended purpose as an insulator between the gate and channel, there can also be a tunneling resistance between the cap and channel that adds to the total series resistance.

Eventually, for antimonides, and III-V's in general, to be a viable technology in future CMOS applications, a MOSFET-like structure will have to be adopted to control the leakage and power consumption as well as address the other issues described above. However, because of its elegance and simplicity, some aspects of device physics can be more easily studied in isolation with a HEMT without the need for developing a high-k dielectric or using ion implantation. For this reason, a HEMT-like structure was used in this thesis work to study the stress effect on

antimonides. (Some of the other technologies needed to develop antimonide p-channel MOSFETs will be discussed and pursued in the "Ongoing and Suggestions for Further Work" section of Chapter 4.) Furthermore, it is worth noting that the term "HEMT" (high *electron* mobility transistor) is sometimes used informally to refer to both n-channel and p-channel transistors and is often used more to describe the device heterostructure and concept, rather than the particular carrier type. However, to reduce confusion and improve technical clarity, the rest of this thesis will use terms such as "p-channel FET" or "QW-FET" (quantum-well FET) to refer to the antimonide p-type transistor fabricated and characterized in this study.

Figure 6 shows a diagram of the heterostructure that was used in this study. The heterostructure was grown on a 3-inch semi-insulating GaAs substrate by Brian Bennett at Naval Research Laboratory. First, a GaAs regrowth layer was grown, followed by the growth of a metamorphic, relaxed $Al_{0.7}Ga_{0.3}Sb$ buffer 1.5 μm thick, setting the lattice constant of subsequent epitaxial layers. Then, a 5 nm layer of $Al_{0.7}Ga_{0.3}Sb$ is grown doped p-type with beryllium, followed by another 21 nm of undoped $Al_{0.7}Ga_{0.3}Sb$. Subsequently, the 7.5 nm $In_{0.4}Ga_{0.6}Sb$ channel is grown lattice matched to the $Al_{0.7}Ga_{0.3}Sb$ buffer layer underneath. Because the natural lattice constant of $In_{0.4}Ga_{0.6}Sb$ is larger than that of the $Al_{0.7}Ga_{0.3}Sb$ buffer layer, the channel of this device is biaxially compressed with ~2% strain. Following this, another 3 nm of $Al_{0.7}Ga_{0.3}Sb$ and 4 nm of $In_{0.2}Al_{0.8}Sb$ are grown. These two layers collectively form a 7 nm barrier to isolate the channel and the gate. The $In_{0.2}Al_{0.8}Sb$ also serves as an etch stop layer during the recessing of the cap (which is discussed in the process flow later). Finally, a heavily doped p^+-cap comprised of 30 nm InAsSb and 5 nm of InAs was grown to allow for low access resistance to the intrinsic device.

Layer
p+InAs 5 nm (Be ~ 1e19)
p+InAsSb 30 nm (Be ~ 1e19)
$In_{0.20}Al_{0.80}Sb$ 4 nm
$Al_{0.70}Ga_{0.30}Sb$ 3 nm
$In_{0.40}Ga_{0.60}Sb$ 7.5 nm
$Al_{0.70}Ga_{0.30}Sb$ 21 nm
p-$Al_{0.70}Ga_{0.30}Sb$ 5 nm (Be ~ 2e18)
$Al_{0.70}Ga_{0.30}Sb$ 1.5 μm
GaAs regrowth
S.I. GaAs

Figure 6: Cross section detailing the primary heterostructure used for device fabrication in this thesis work. The 7.5 nm $In_{0.4}Ga_{0.6}Sb$ channel is lattice-matched to the relaxed $Al_{0.7}Ga_{0.3}Sb$ buffer, resulting in 2% compressive biaxial strain.

The composite InAsSb/InAs cap was chosen over a pure InAs cap because of concerns of surface defects observed in an earlier heterostructures using a pure InAs cap. Figure 7 shows SEM images comparing the surface of the heterostructure in Figure 6 with that of another similar heterostructure but terminated with a 20 nm pure InAs cap. Line markings were visible on the surface with a pure InAs cap, suggesting the possibility of defects associated with strain in the cap. Because of this observation, the final devices presented in this study were fabricated using the composite cap structure, although much of the process development and device prototyping were done on samples with a pure InAs cap. The origin of these surface defects was not a major focus of the study presented in this thesis, so further study would be needed to achieve a better understanding, although the observed line defects bear a strong resemblance to the defects seen in [22], which described the defects as a result of threading dislocation stemming from the

AlGaSb/GaAs substrate interface. In our samples, it was found that removing the defected InAs cap revealed a smooth surface underneath, suggesting that these defects are caused or magnified by the tensile strain in the cap.

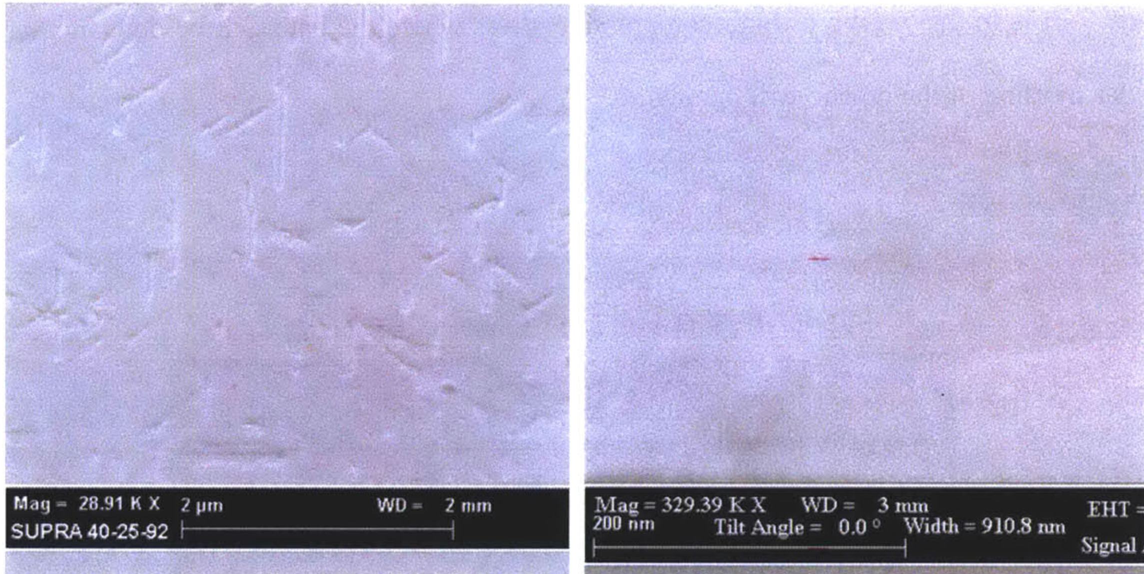


Figure 7: Left image shows the virgin surface of a structure terminated with a 20 nm InAs cap, while the right image shows the virgin surface of the heterostructure of Figure 6 which is terminated with an 30 nm InAsSb/5 nm InAs composite cap. Surface line defects were observed on the pure InAs sample but the composite cap showed a smooth surface.

2.2 Overview of Device Architecture

Using a biaxially strained quantum-well heterostructure for our antimonide p-channel FET study, a mechanism to incorporate the uniaxial stress is needed. For this study, the use of a high-stress

silicon nitride dielectric was used, similar to the film used in [17]. In order to induce stress in the intrinsic region of the FET, a compressively stressed silicon nitride film was deposited via PECVD. When a narrow opening is made in the nitride film, a region of high stress occurs at its edge. With both edges of the nitride acting on the substrate towards the other, this creates a compressively stressed region of the substrate under uniaxial strain. This effect is illustrated in Figure 9. It is in this region of high compressive stress where the gate will be deposited and the intrinsic portion of the device will operate.

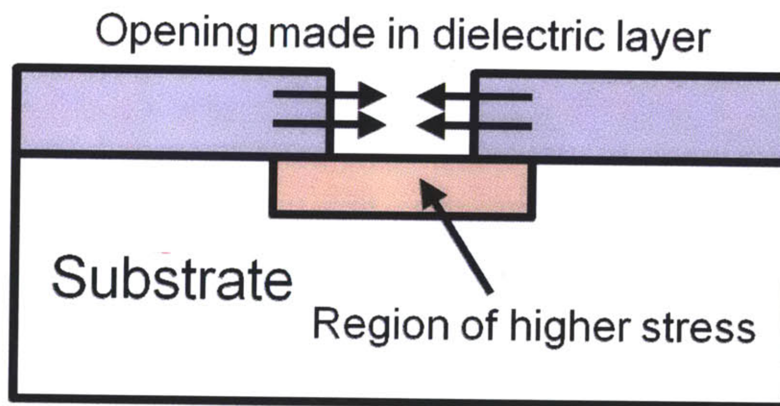


Figure 8: After deposition of a compressively stressed nitride film, an opening in the film creates a region of compressive stress in the semiconductor.

Figure 9 shows how the compressively stressed nitride film can be incorporated into the quantum-well FET design to create a stressed antimonide p-channel device. This cross-sectional diagram also illustrates the devices fabricated and characterized in this study to analyze the influence of stress on enhancing device performance.

A great advantage to this device architecture is that as the gate length of the device is scaled to smaller dimensions, the dimension of the opening in the nitride film is also being scaled. Because the amount of stress experienced by the substrate is largest at the edge of the film, reducing the dimension of the opening in the film increases the amount of stress experienced by the intrinsic portion of the FET.

In order to study how the stress from the nitride film induces stress in the substrate, mechanical simulations were done using the COMSOL Multiphysics® simulation software [23]. Figure 10 shows a mechanical stress simulation for a 1 μm gap in the nitride film. Figure 11 shows the same simulation for a 300 nm opening. From these simulations, shrinking the opening from 1 μm to 300 nm increased the magnitude of the surface stress at the center of the gap from -200 MPa to -400 MPa, due to the fact that the largest stress levels occur near the edge of the nitride film.

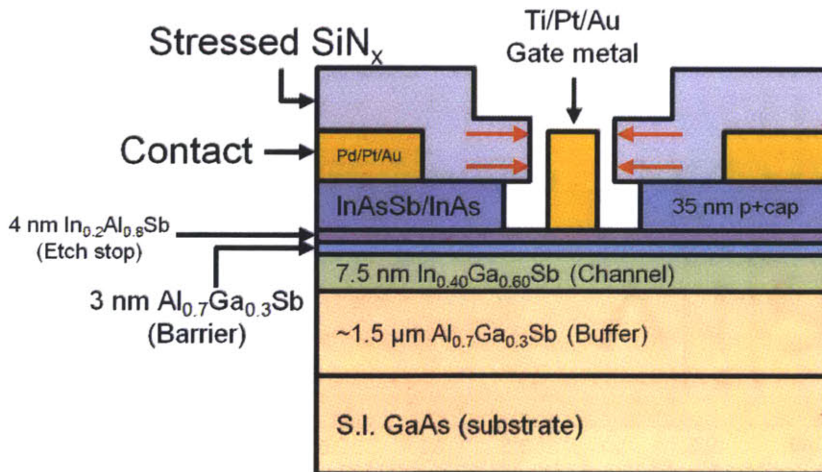


Figure 9: Cross-sectional diagram detailing the target device structure. The quantum-well InGaSb layer serves as a conducting channel and is grown with 2% compressive biaxial strain. The stressed SiN_x layer is used to induce uniaxial strain along the direction of carrier transport.

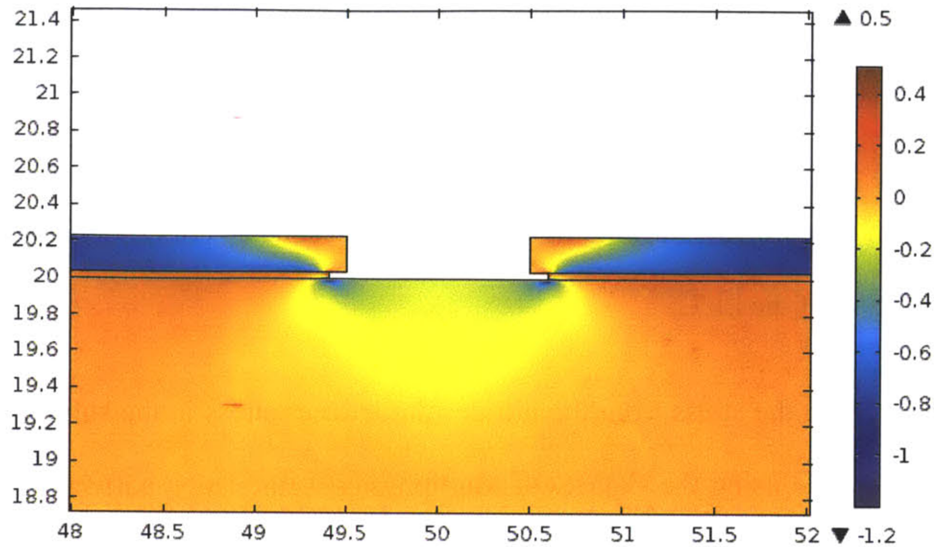


Figure 10: Mechanical simulation illustrating the stress experienced by a GaAs substrate from a 200 nm thick silicon nitride film with -1.5 GPa of intrinsic stress for a 1 μm opening. The simulation also includes a 100 nm cap recess. The center of the opening has -200 MPa of stress.

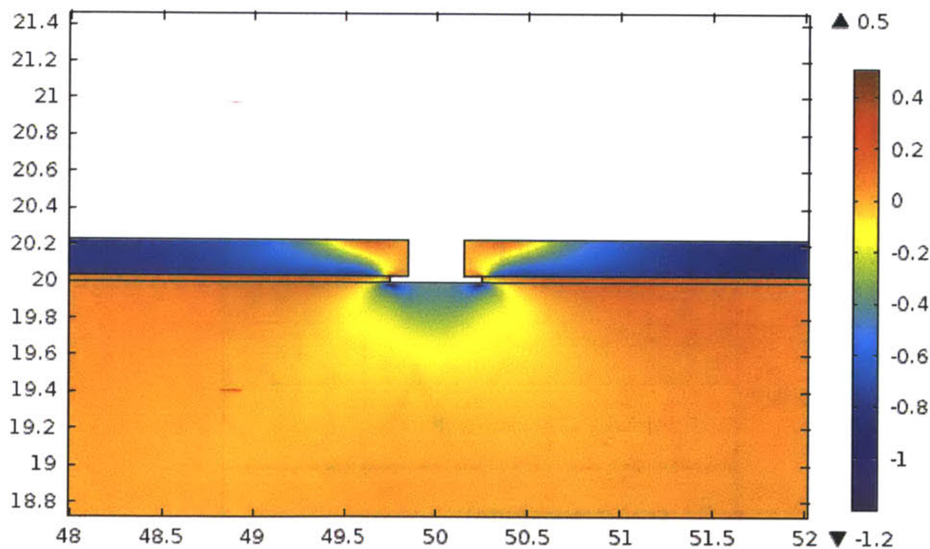


Figure 11: The same mechanical simulation with a 300 nm opening. The center of the opening has -400 MPa of stress. Decreasing the gap dimension increases the amount of stress in the substrate since most of the high stress is located near the edge of the nitride film.

2.3 Process Flow

To achieve the structure shown in Figure 9, a process flow was developed for device fabrication. This section details the processing steps, illustrated in Figure 12, used to fabricate the stressed antimonide p-channel devices.

Step 1: The sample is cleaned thoroughly with water and organic solvents and dried using a nitrogen gun. In this particular diagram and in subsequent illustrations, the thin etch stop layer and the barrier are drawn as a single layer for simplicity. Also, in the subsequent cross sections, the heterostructure layers are not labeled but are the same as that of the Step 1 diagram.

Step 2: A negative-tone AZ5214 photolithography step is used to pattern the Pd/Pt/Au ohmic contacts using a lift-off procedure. Pd/Pt/Au metal stacks are commonly used in literature for making p-type contacts to highly doped InAs layers [24]. Before deposition of the contact metal via electron beam evaporation, the sample is exposed briefly to O_2 plasma to remove resist residue and dipped in BOE to remove the InAs native oxide. After deposition of the contact metal and lift-off patterning, the Pd/Pt/Au contacts were annealed in an oxygen-free environment for > 1 hour at 200°C.

Step 3: A compressively stressed silicon nitride film is deposited using PECVD at 250°C. Another sample was deposited with a stress-free nitride film and subsequently processed in parallel to serve as a reference sample to compare the effects of the stress on enhancing device performance. The stress of the nitride film can be adjusted by varying the composition of high frequency (13.56 MHz) and low frequency (380 KHz) for the deposition [25]. On top of both the stressed and stress-free nitride film, a ~50 nm SiO_x layer was deposited to serve as a protective layer for the delicate nitride film (SiO_x not shown in the figures to maintain simplicity).

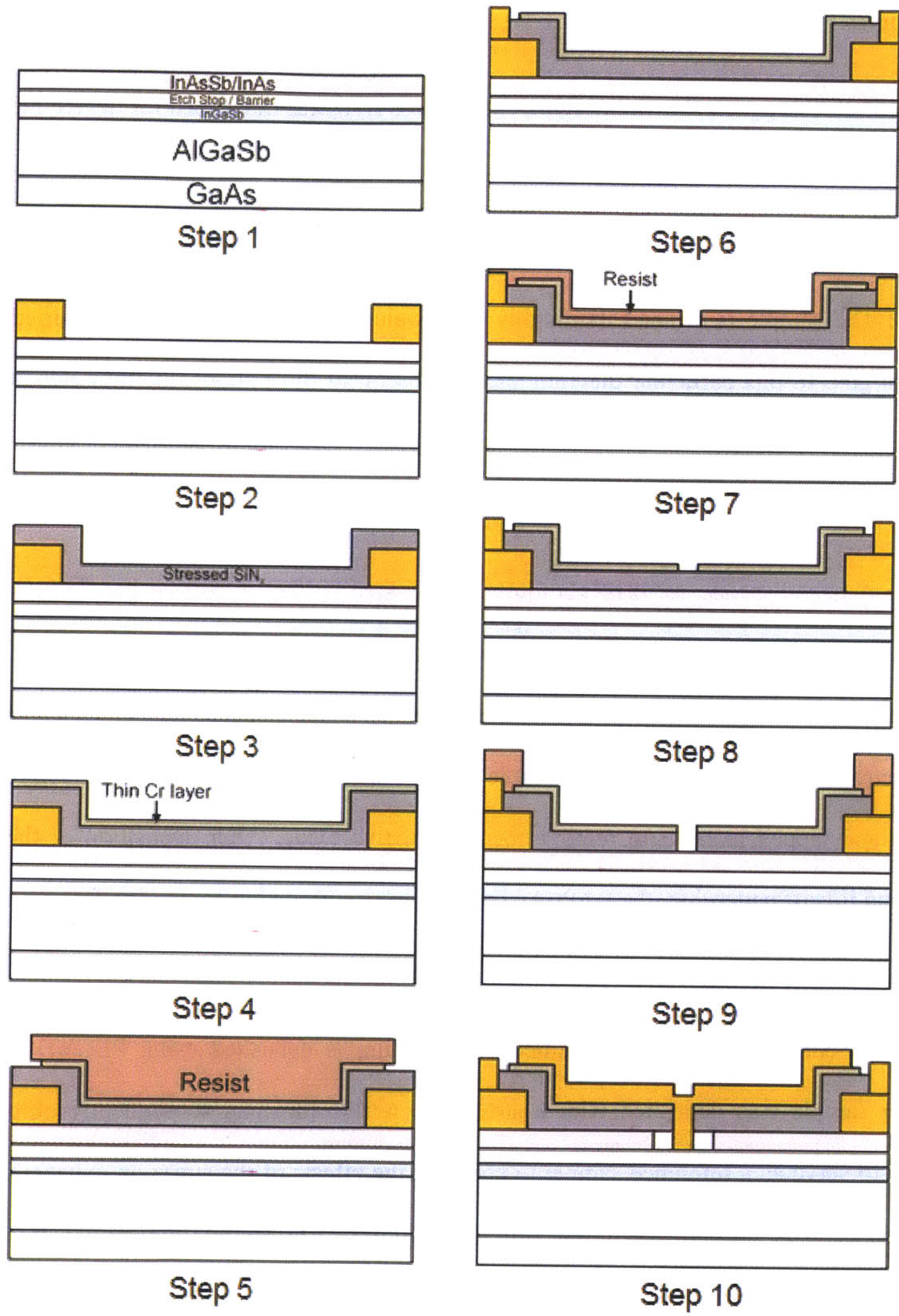


Figure 12: Process flow used to fabricate the stressed and unstressed InGaSb p-channel FETs.

Step 4: A thin layer of chrome (< 5 nm) is deposited via electron beam evaporation on top of the nitride film to be used as a hard mask later.

Step 5: A photolithography step to define the pad metal is patterned. The thin Cr layer is etched away using CR-7, a chrome chemical etchant from Cyantek Corporation [26]. A wet chemical etchant is used as opposed to dry etching in order to produce an undercut underneath the resist. This is to ensure that when the pad metal is deposited, it is not shorted to the Cr layer (and consequently to the gate, which follows later in the processing steps).

Step 6: With the photoresist as the mask, the silicon nitride layer is etched away using SF_6/O_2 plasma etching. Then, the pad metal is deposited via electron beam evaporation and the sample is soaked in acetone for lift-off to pattern the pad metal.

Step 7: The sample is coated with electron beam resist (PMMA A4) and a narrow pattern is made using a 125 keV ELS-125F electron beam lithography tool for the gate. Different gate lengths are drawn on the same sample, and gate lengths of the same dimension are drawn on the stress-free sample. The PMMA resist then serves as a mask for patterning the Cr layer, which is dry etched using Cl_2/O_2 plasma. The PMMA resist is etched away quickly in the process but given the small thickness of the Cr layer, only a brief etching is necessary to remove the Cr. This small pattern eventually will form the gate finger. The dimension of this opening determines the gate length of the device, which also affects the amount of stress induced in the channel.

Step 8: The sample is then soaked in acetone to remove any remaining PMMA resist.

Step 9: The SiO_x/SiN_x layer is etched using SF_6/O_2 plasma. Because of the Cr layer's high resistivity to the plasma, it serves as an excellent hard mask for dry patterning of the nitride. The

Cr layer is used as a mask for the nitride etch instead of the PMMA resist directly because of the inadequacy of PMMA resist as an etch mask against prolonged SF_6/O_2 plasma. Etch tests were done in order to verify the resistance of Cr to SF_6 etching. Figure 13 shows that Cr is highly resistant to SF_6 etching but can be patterned using Cl_2.

The SF_6 etching of the nitride layer is fairly anisotropic to ensure that the opening in the nitride is kept small to allow for large stress inducement. Figure 14 shows an SEM image of the nitride film patterned with the Cr mask. Following the dry etching of the nitride, another photolithography step is used define the pattern of the gate metal.

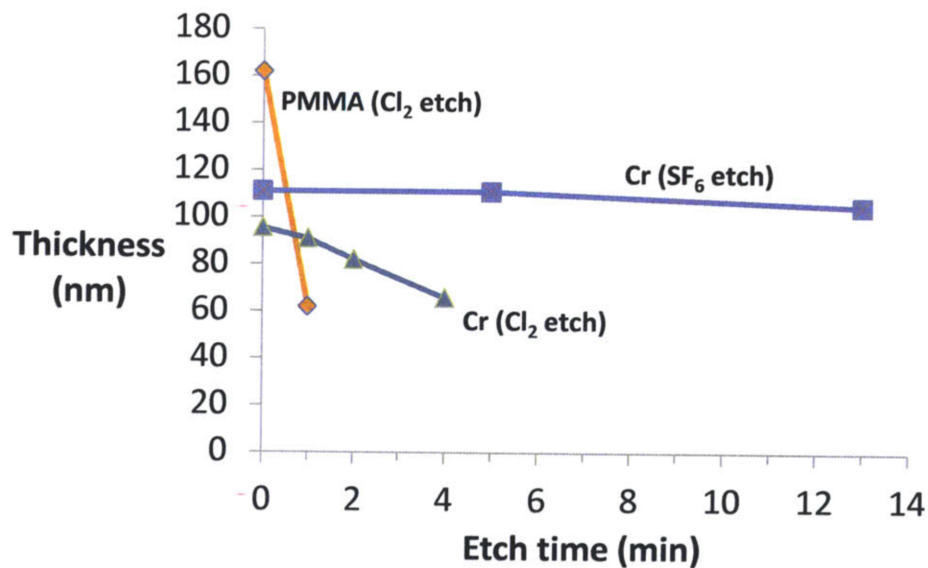


Figure 13: Etch rate of Cr for SF_6 plasma and Cl_2 plasma. In the process flow, the Cr layer is first patterned with Cl_2 using a PMMA mask. The Cr layer then serves as a hard mask for the nitride etching by SF_6.

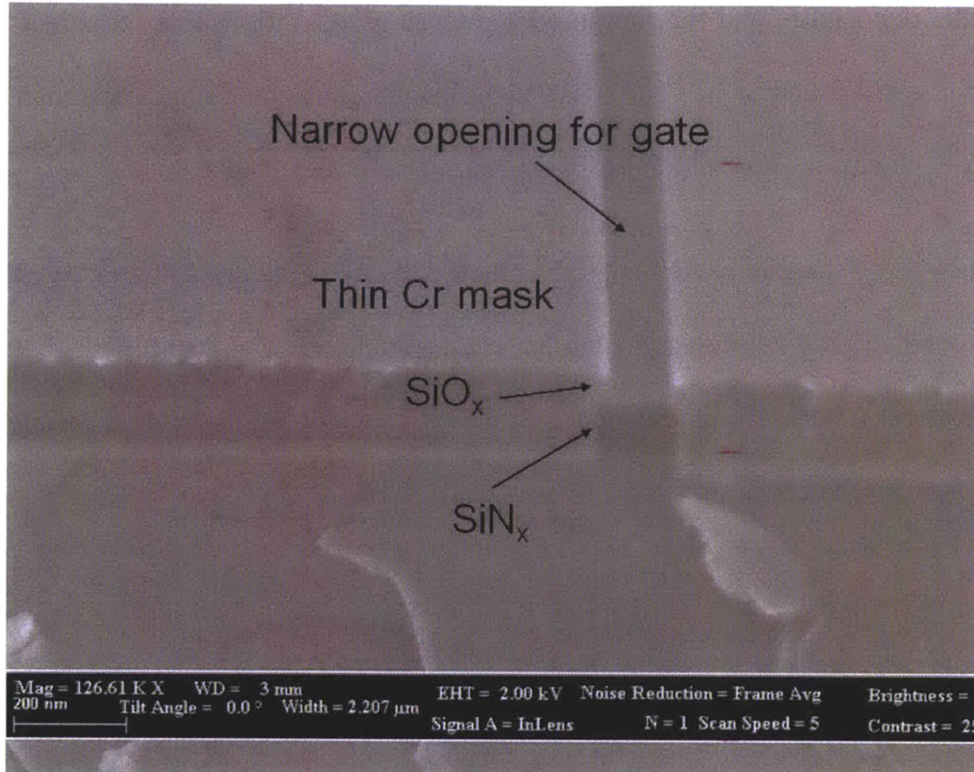


Figure 14: Cross-sectional SEM image detailing the use of the thin (several nanometers) Cr layer as a hard mask for the dry etching of the nitride film. Using the Cr hard mask allows for small pattern definition that is not easily accomplishable using PMMA resist because of its poor selectivity against the SF_6/O_2 plasma.

Step 10: The InAsSb/InAs p+-cap is then recessed using 3:1 citric acid and H_2O_2. Over-etching is done to ensure that the cap is fully removed, but not too long to avoid large undercut, which would increase the series resistance and also reduce the amount of induced stress. After the cap recess, the Ti/Pt/Au gate metal is deposited via electron beam evaporation and the sample is soaked in acetone for lift-off. Stress measurements were done to ensure that the gate metal did not contribute any stress to the device. Figure 15 shows the surface height profile of a 6-inch Si wafer deposited with the gate metal stack. The surface of the 6-inch wafer was measured before

and after the deposition, and the measured bow was used to determine the stress of the metal film, which would found to be < 30 MPa, significantly smaller in magnitude than the stress of the compressive nitride film, which had an intrinsic stress of -1.5 GPa.

Finally, one more lithography step is used to define the mesa pattern and a lactic acid-based wet etchant is used to perform device isolation. Figure 16 shows a cross section of the mesa etch using a photoresist mask. The mesa etch is designed to etch through the cap, channel, and buffer layers and stop on the GaAs substrate.

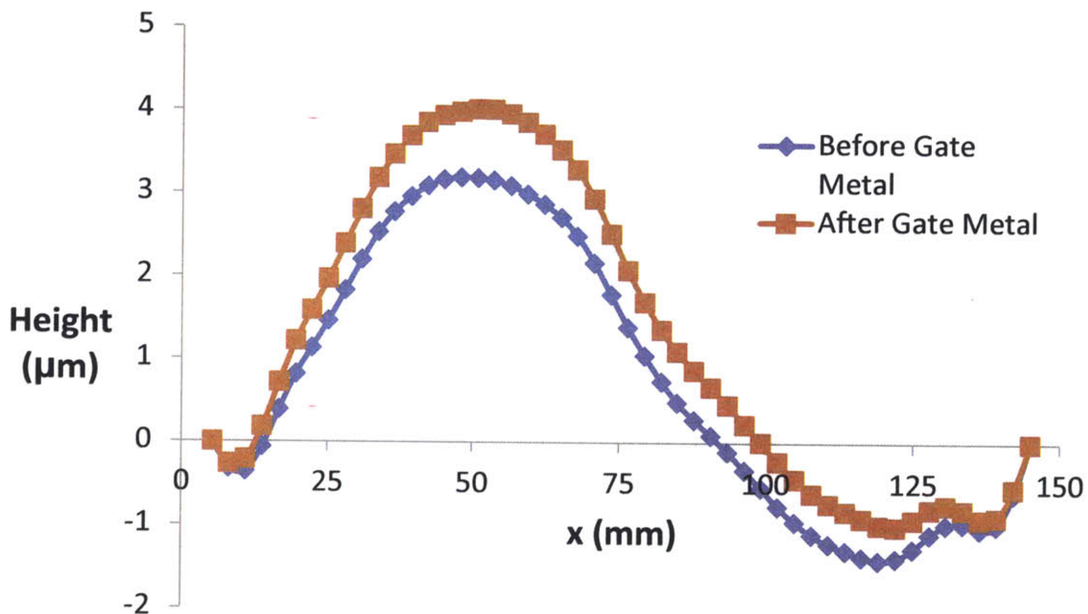


Figure 15: Surface profile of a 6-inch Si wafer before and after the deposition of the gate metal film. The data was used to determine the intrinsic stress of the metal film, which was measured to be < 30 MPa, much smaller than that of the -1.5 GPa compressively stressed nitride.

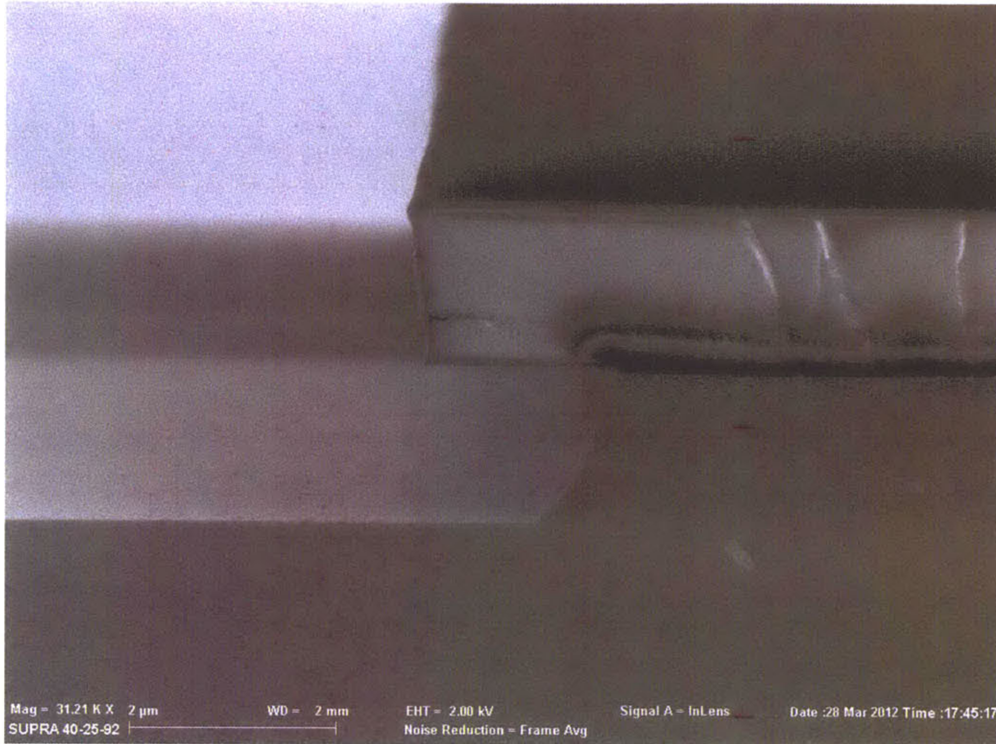


Figure 16: SEM image of the mesa etch with a photoresist mask. The mesa etch stops at the GaAs substrate.

2.4 Summary

In this chapter, a device architecture for incorporating uniaxial stress via a compressively stressed nitride was described along with a fabrication process flow. The device architecture takes advantage of increasing stress with scaling of the gate length. Using the process flow, devices of various gate lengths and transport orientations were characterized, and the results are discussed in the next chapter.

Chapter 3: DEVICE RESULTS

3.1 Introduction

Following the process flow described in Chapter 2, stressed InGaSb p-channel FETs were fabricated and compared with reference unstressed samples processed in parallel. In this chapter, we discuss the reduction in source-drain resistance and enhancement in transconductance resulting from the uniaxial strain, as well as some other device characteristics such as contact resistance and gate leakage.

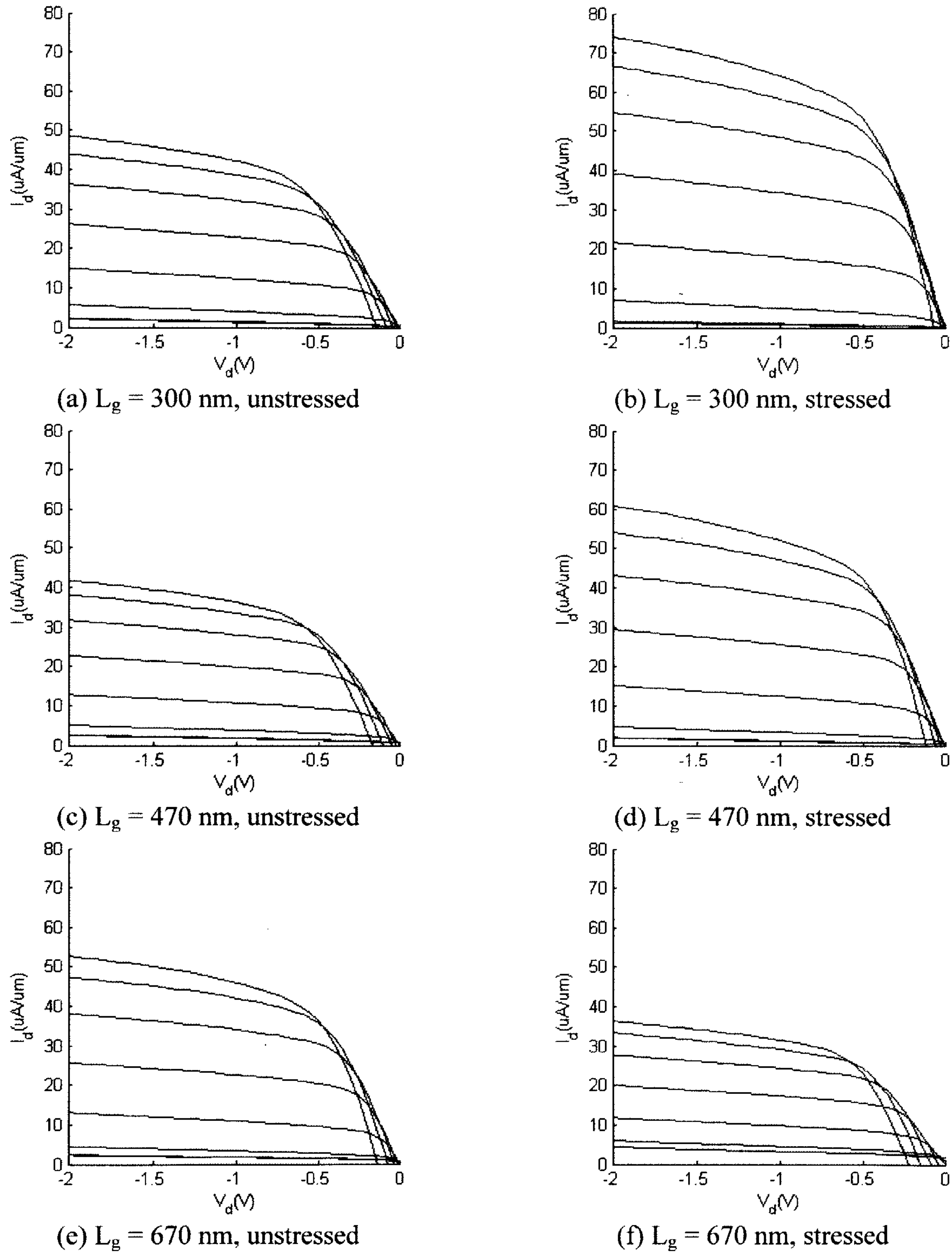
3.2 Output Characteristics

For both the stressed and unstressed devices, the thickness of both nitride films was made to be ~180 nm and the stressed nitride was deposited with an intrinsic stress of -1.5 GPa. The intrinsic stress of the unstressed nitride film was measured to be < 50 MPa. A larger thickness and greater intrinsic compressive stress result in higher uniaxial strain applied to the device, so it is desirable to make both of these as large as possible. In the devices fabricated, these were limited by the strength of the adhesion of the nitride film to the metal contacts and to the top surface (InAs) of the heterostructure. Devices of gate lengths 300 nm, 470 nm, and 670 nm were fabricated on both the stressed and unstressed samples with transport orientations of [110], [100], and [010]. Figure 17 compares output characteristics of typical stressed and unstressed devices for the various gate lengths. For the stressed devices, the observed on-current was found to be significantly higher than that of the unstressed devices. Also evident from the graphs is the large

gate leakage at low V_{DS} for high gate overdrive, believed to be caused by the thin (7 nm) barrier and is discussed in more detail later in this chapter. Figure 18 shows the transfer and subthreshold characteristics for the devices shown in Figure 17. The left column shows the drain current and extrinsic transconductance while the right column shows the subthreshold characteristics and gate leakage. The solid and dashed lines represent the stressed and unstressed devices, respectively. All stressed devices showed a significantly enhanced transconductance. Some stressed devices showed a reduction in I_g in reverse gate bias and an increase in forward gate bias while in all devices, gate leakage contributed substantially to the subthreshold characteristics. No substantial change in the threshold voltage was observed due to the stress.

3.3 Source/Drain Resistance

One of the primary causes of device enhancement from the stress can be attributed to a reduction in R_S/R_D, the source-drain resistance, measured using the gate current injection method [27] for both the stressed and unstressed devices. Figure 19 shows the percent reduction in the source-drain resistance for different gate lengths and transport orientations. All of the stressed devices exhibited a significant reduction in the source-drain resistance, with some devices showing more than a 30% reduction. Of particular interest is the observation that the reduction in R_{SD} does not appear to be scaling with the gate length as expected from the mechanical simulations. In theory, scaling the gate length decreases the opening in the nitride, which increases the magnitude of the stress transferred to the substrate, as discussed in Chapter 2. This expected increase in stress should result in a larger R_{SD} reduction. Furthermore, one would expect some type of dependence of the reduction on crystal orientation, but Figure 19 does not seem to reveal such behavior.



(a) L_g = 300 nm, unstressed

(b) L_g = 300 nm, stressed

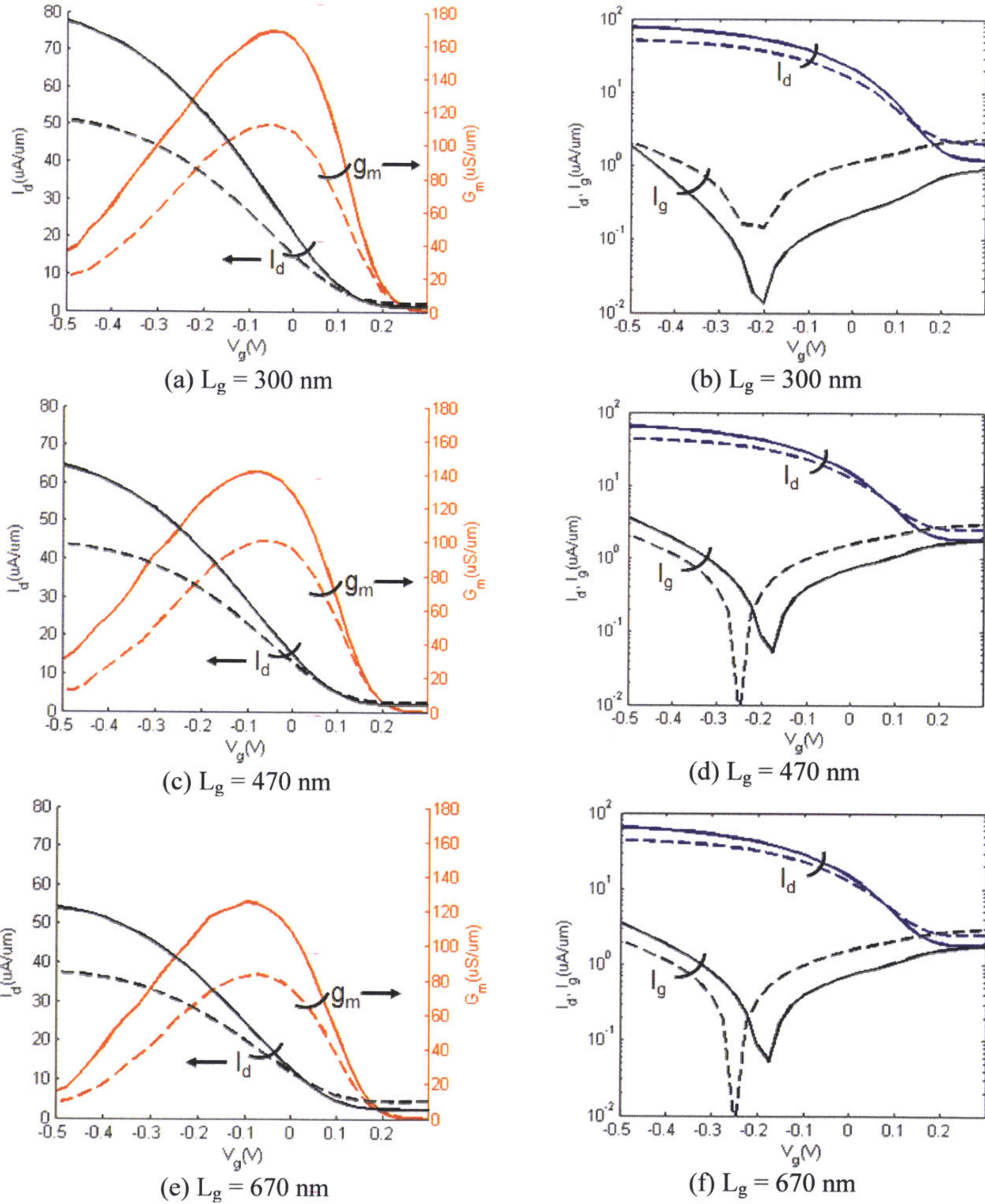
(c) L_g = 470 nm, unstressed

(d) L_g = 470 nm, stressed

(e) L_g = 670 nm, unstressed

(f) L_g = 670 nm, stressed

Figure 17: Output characteristics of unstressed and stressed devices for various gate lengths. All plots are for V_{GS} from -0.4 V to 0.3 V in 0.1 V steps.



(a) L_g = 300 nm (b) L_g = 300 nm

(c) L_g = 470 nm (d) L_g = 470 nm

(e) L_g = 670 nm (f) L_g = 670 nm

Figure 18: Transfer characteristics (left column) and subthreshold characteristics (right column) for stressed (solid lines) and unstressed (dashed lines) of different gate lengths for V_{DS} = -2.0 V.

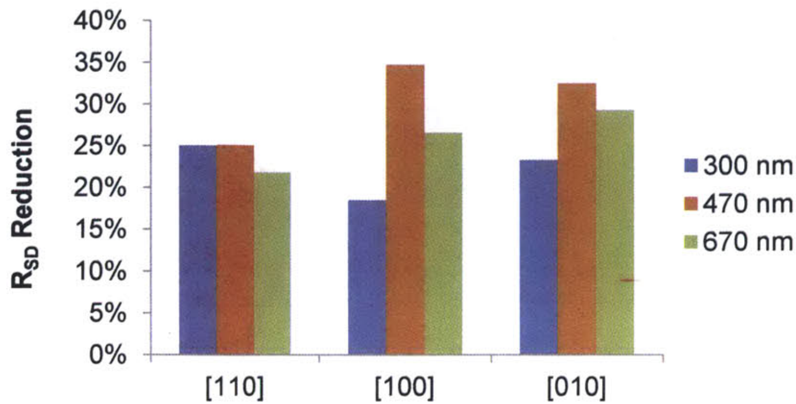


Figure 19: Graph describing the reduction in the source-drain resistance for various gate lengths and transport orientations. Stressed devices exhibited a large reduction in R_{SD}.

This is believed to be due to the poor adhesion between the stressed nitride and substrate/contact. When the nitride is under large compressive stress, the film is very delicate and agitations such as sudden changes in temperature or soaking the sample in solution can cause the nitride film to delaminate. For this reason, it can be a challenge to ensure that the stressed film is kept intact throughout the entire fabrication process. Consequently, complete or even partial delamination of the nitride film can result in relaxation along all or part of the device, taking away the would-be-seen enhancements had the film stayed adhered to the substrate. This delamination can sometimes been manifested in the form of a bubble or strange discoloring visible via optical microscope, as shown Figure 20. In order to overcome this adhesion problem, the stress or thickness of the nitride film can be reduced. However, this would erase some of the gains in device performance. An alternative is to explore adhesion promotion techniques such as pre-deposition NH_3 plasma treatment [28] or the use of an interfacial TiO_2 adhesion layer [29].

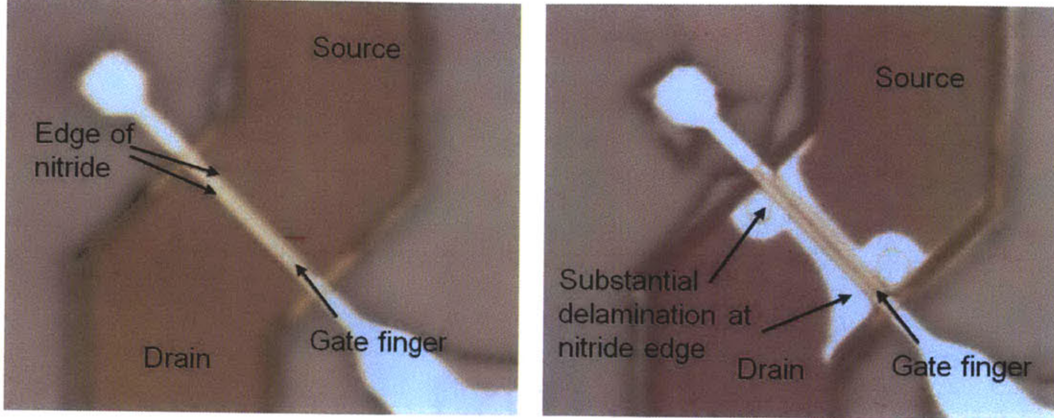


Figure 20: Examinations by an optical microscope reveal that delamination of the nitride film can occur at the nitride edge, relaxing the stress and removing the would-be-seen device enhancements.

3.4 Transconductance

Extrinsic transconductances were also measured and used to determine the intrinsic transconductance g_{mi} using the derivation from [30]:

$$g_{mi} = \frac{g'_{mi}}{1 - (R_S + R_D)g_d(1 + R_S g'_{mi})} \quad (1)$$

with

$$g'_{mi} = \frac{g_m}{1 - R_S g_m} \quad (2)$$

where g_m is the extrinsic transconductance and g_d is the output conductance.

Figure 21 shows the extrinsic and intrinsic transconductances for various gate lengths for both the stressed and unstressed devices along the [110] direction of transport. The peak extrinsic transconductances were determined for V_{DS} = -2.0 V. The stressed devices exhibited higher extrinsic and intrinsic transconductances compared with the unstressed devices, with the 300 nm

devices showing a 40% gain in extrinsic transconductance and 60% gain in intrinsic transconductance for the [110] orientation. Figure 22 shows the percent enhancement in intrinsic transconductance for all the different gate lengths and transport orientations. Many of the stressed devices exhibited enhancements in the intrinsic transconductance of more than 50%. Similar to the reduction in R_{SD} shown in Figure 19, there does not appear to be a clear dependence of the g_{mi} enhancement on crystal orientation or even the device gate length. Again, this is believed to be the result of adhesion issues associated with the stressed nitride. A closer examination of the various device transconductances revealed that while many of the unstressed devices had transconductances similar to one another, there were much larger variations in the transconductances for the stressed devices.

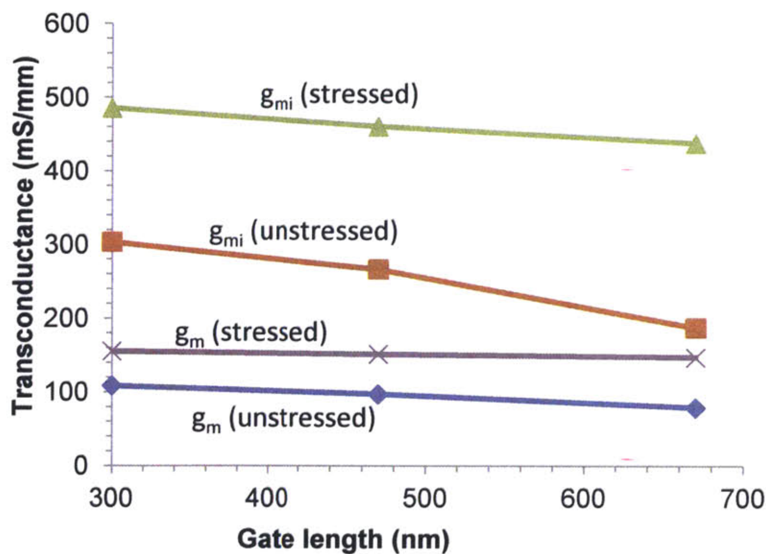


Figure 21: Plot illustrating the extrinsic and intrinsic transconductances for both the stressed and unstressed devices. Each data point is the average of transconductances measured from 3 to 5 different devices. All devices in this figure had transport directions along the [110] orientation.

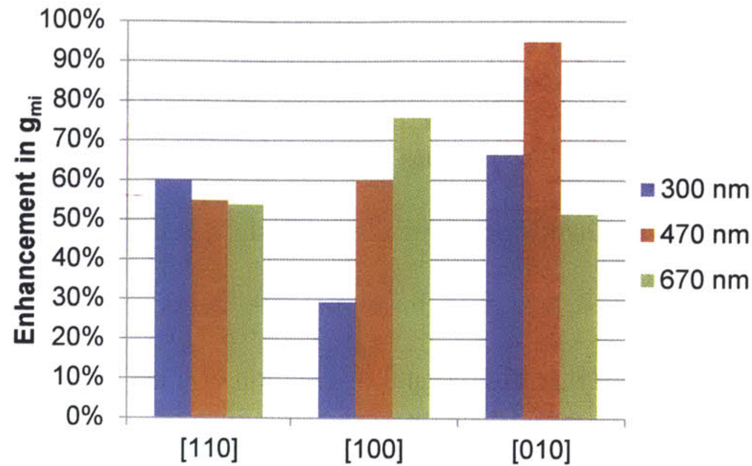


Figure 22: Percent enhancement in intrinsic transconductance for different gate lengths and transport orientations.

3.5 Contact Resistance

With the InAsSb/InAs (30 nm/5 nm) composite cap, an excellent contact resistance of 0.56 Ω·mm was achieved. Figure 23 shows measurements made from a transmission line measurement (TLM) structure. The structure consisted of mesas with metal contact pads with varying distances in between. The cap between the two pads was unrecessed, so the measured sheet resistance of 1320 Ω/sq is a mixture of both the cap resistance and channel resistance in parallel. This composite cap structure gives a notable improvement over a 20 nm pure InAs cap, the same structure discussed in Chapter 2. Figure 24 shows the TLM for a 20 nm InAs cap, which gave a contact resistance of 2.23 Ω·mm. Hence, the thicker composite cap structure resulted in a ~4x improvement in the contact resistance.

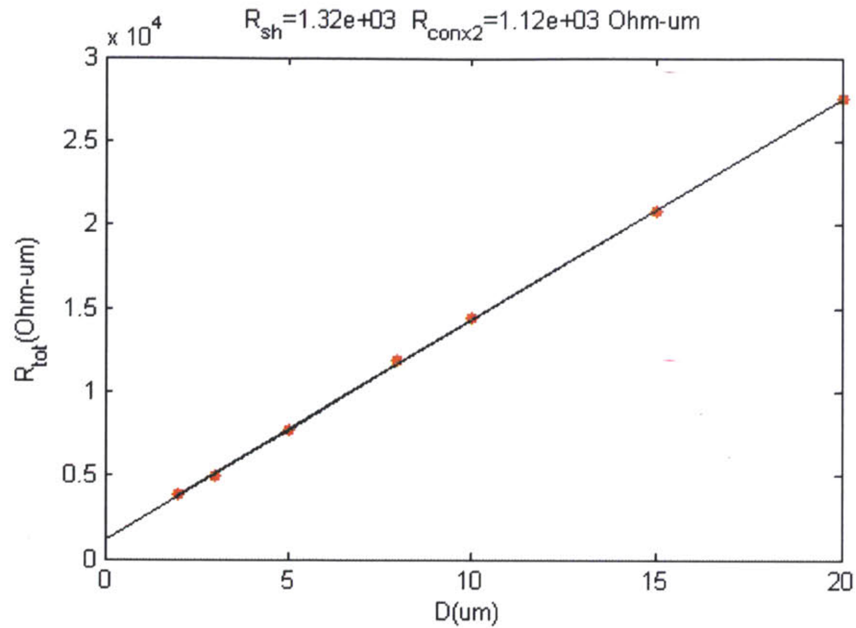


Figure 23: Using the InAsSb/InAs composite cap structure doped 10^{19} cm^{-3} with beryllium, a contact resistance of 0.56 Ω·mm and a sheet resistance of 1320 Ω/sq were extracted from TLM.

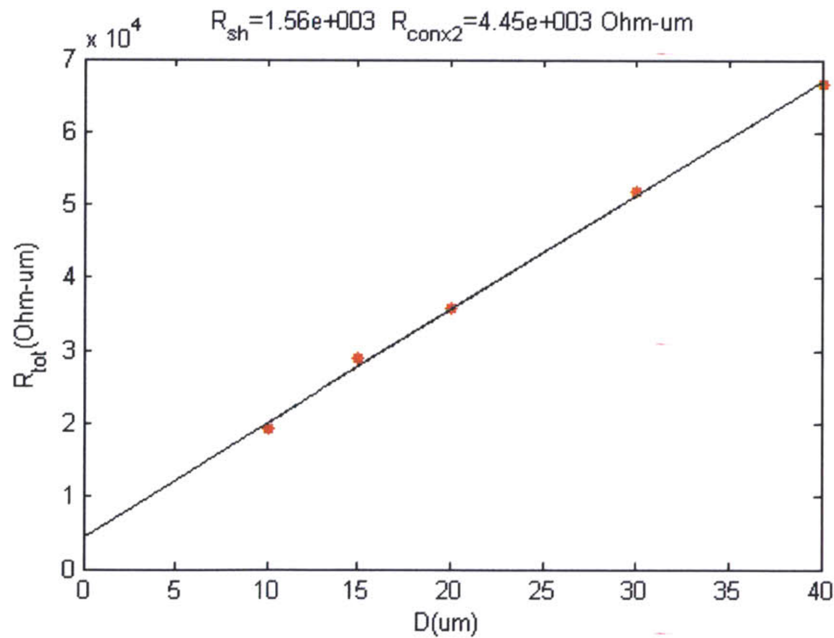


Figure 24: A 20 nm InAs cap structure doped 10^{19} cm^{-3} with beryllium gave a contact resistance of 2.23 Ω·mm and a sheet resistance of 1560 Ω/sq, extracted from TLM.

3.6 Gate leakage

As can be seen from Figure 17, all of the fabricated devices exhibited large amounts of gate leakage. For both the stressed and unstressed devices, the magnitude of the gate leakage becomes progressively worse as the gate length, and consequently the area of the gate, increases. The cause of this large gate leakage is under investigation and is likely due to the thin barrier, resulting in tunneling or thermionic emission.

An unstressed test device was fabricated with a thicker barrier of 14 nm (4 nm $In_{0.2}Al_{0.8}Sb$ / 10 nm $Al_{0.7}Ga_{0.3}Sb$) as opposed to the 7 nm barrier (4 nm $In_{0.2}Al_{0.8}Sb$ / 3 nm $Al_{0.7}Ga_{0.3}Sb$) used for the stressed devices in this study. Figure 25 shows the output characteristics of the test device with a thicker barrier, which had a gate length of 200 nm and exhibited significantly improved gate leakage. Figure 27 shows the transfer and subthreshold characteristics for the same device. A more than one order of magnitude reduction in the gate leakage was observed for the entire range of V_{GS}. This suggests that with a thicker barrier, the gate leakage can be reduced in a very significant manner, although at the expense of other device characteristics, as a thicker barrier would result in poorer electrostatics, greater impact of short-channel effects, and increased series resistance. The ideal approach would be to use high-k dielectrics to reduce the gate leakage without sacrificing other aspects of device performance. This is discussed in the further work section of Chapter 4.

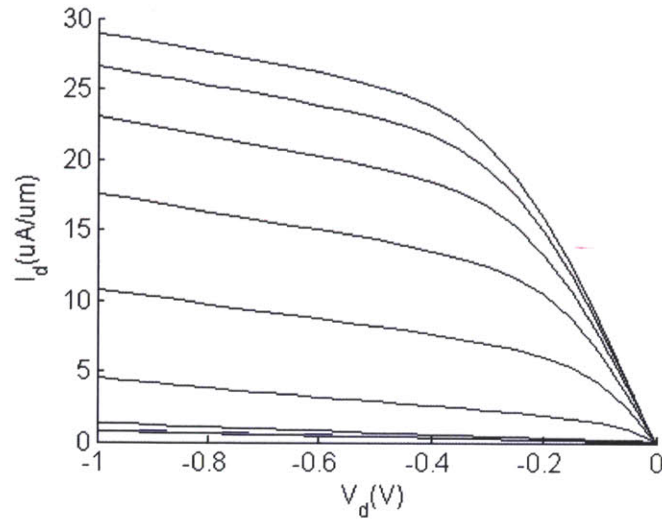


Figure 25: Output characteristics of a L_g = 200 nm device fabricated on a heterostructure with a thicker (14 nm) barrier without a stressed nitride. The curves are for V_{GS} = -0.5 V to 0.3 V in steps of 0.1 V.

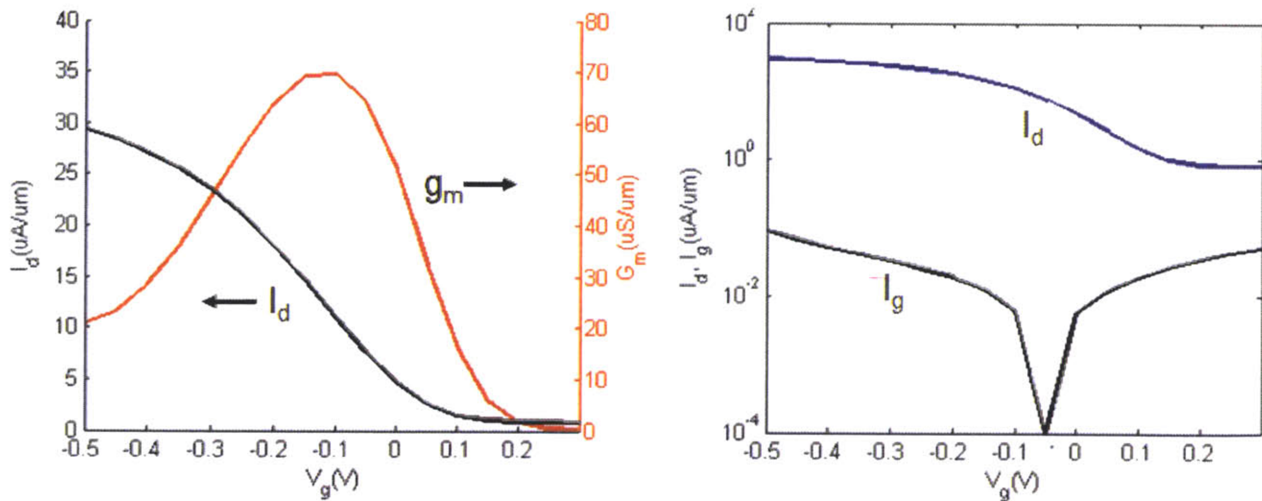


Figure 26: Transfer and subthreshold characteristics of the same (thicker barrier) device. A significant improvement in gate leakage was observed compared with the thin barrier devices of Figure 17. A more than one order of magnitude improvement in the gate leakage was seen for the entire range of V_{GS}. All curves are for V_{DS} = -1.0 V.

3.7 Summary

In this chapter, we showed that stressed InGaSb p-channel FETs showed considerable enhancement in device characteristics over the unstressed devices. Reductions of more than 30% in the source-drain resistance were observed. In addition, many of the stressed devices exhibited enhancements of more than 50% in the intrinsic transconductance. A novel composite InAsSb/InAs cap structure was also measured to have a contact resistance much smaller than a pure InAs cap. A high gate leakage was observed for both the stressed and unstressed devices and is believed to be solvable with a thicker barrier or use of a high-k dielectric.

Chapter 4: CONCLUSIONS AND FURTHER WORK

4.1 Conclusions

In this thesis work, enhanced InGaSb p-channel QW-FETs were fabricated using a stressed silicon nitride film with -1.5 GPa compressive stress. Reference samples were processed in parallel with an unstressed nitride film and compared to the stressed devices. Both films were deposited with a thickness of ~180 nm and all other processing details were identical. The stressed samples showed significant reduction in R_{SD}, with some devices showing a reduction of more than 30%. In addition, the stressed FETs exhibited significant enhancement in transconductance, with many devices showing gains of more than 50% in the intrinsic transconductance compared with the unstressed devices.

Scaling improved overall device performance, although the percent enhancements in transconductance and percent reduction in R_{SD} did not scale as expected with the gate length. There was also no observed dependence on orientation of carrier transport. This is believed to be due to adhesion issues associated with the stressed nitride film, resulting in partial or complete delamination of the film. This delamination would result in relaxation, removing the gains one would expect to see from the stress enhancement, resulting in a large variation of performance among the stressed devices. This hypothesis also suggests that greater gains in performance might be possible.

Despite some of these adhesion issues, which can be solved with appropriate adhesion promotion techniques, the stressed nitride device architecture demonstrates the effectiveness of stress in

enhancing antimonide devices and holds promise to the development of a high-performance antimonide p-channel FET.

4.2 Ongoing and Suggestions for Further Work

Current efforts are still underway to perform a more thorough characterization of the stressed and unstressed devices. This includes an investigation of causes for the large gate leakage, which is attributed to either tunneling or non-optimized work functions, resulting in large thermionic emission. Low temperature measurements could potentially help in determining which of these is the primary cause of the leakage. Aside from using a thicker barrier, the gate leakage problem can also be solved with the help of a high-k dielectric such as Al_2O_3 or HfO_2. The use of a high-k oxide is imperative to the development of a viable antimonide MOSFET for use in logic applications to reduce leakage and power consumption, given today's "power-constrained scaling." In addition, before strained antimonide devices can be used in logic, short-channel effects must be tightly controlled. This can be done with non-planar structures such as FinFETs or gate-all-around nanowires. Such device structures would require well-optimized dry etching techniques. Figure 27 shows an SEM image of some preliminary work on the plasma etching of antimonides.

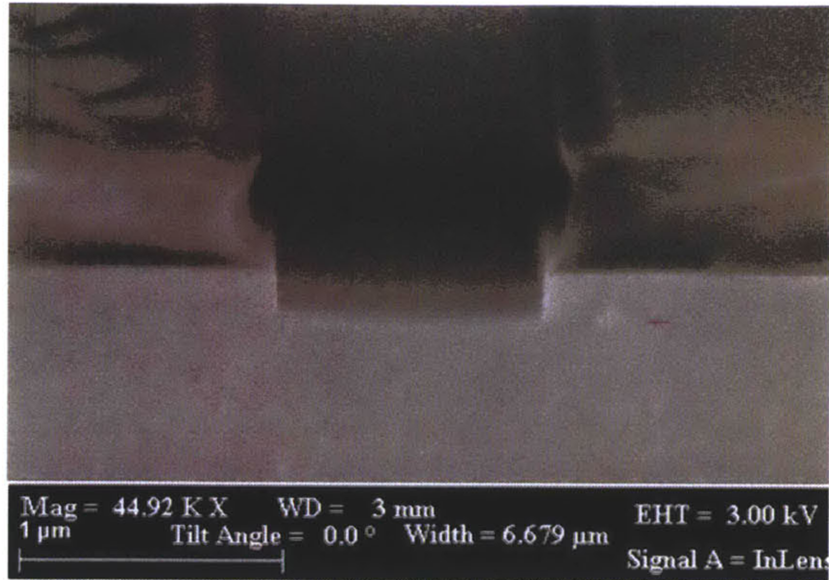


Figure 27: A trench etched in an antimonide heterostructure to a depth of roughly 200 nm using chlorine plasma chemistry.

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