Investigating Thermal Dependence on Monolithically-Integrated Photonic Interconnects

by

Yu-Hsin Chen

B.S. in Electrical Engineering,
National Taiwan University, Taiwan (2009)

Submitted to the Department of
Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2013

Author .....
Department of
Electrical Engineering and Computer Science
May 22, 2013

Certified by .....
Vladimir Stojanović
Associate Professor
Thesis Supervisor

Accepted by .....
Leslie A. Kolodziejski
Chair, Department Committee on Graduate Students

Investigating Thermal Dependence on Monolithically-Integrated Photonic Interconnects

by

Yu-Hsin Chen

Submitted to the Department of
Electrical Engineering and Computer Science
on May 22, 2013, in partial fulfillment of the
requirements for the degree of
Master of Science in Electrical Engineering and Computer Science

Abstract

Monolithically-integrated optical link is a disruptive technology which has the promising potential to remove memory bandwidth bottleneck in the deep multi-core regime. Although with the advantages of high bandwidth-density and energy-efficiency, it comes with design challenges from device, architecture and system perspectives. High thermal sensitivity of the essential optical ring resonator imposes constraints on the applicability of optical links in the electro-optical systems. To investigate the thermal dynamics as well as to develop advanced ring thermal-tuning mechanisms, real-time thermal monitoring at design stage is required.

In this work we propose a thermal simulation platform which integrates system modeling aspects including the high-level architectural performance model, the physical device evaluation model, and the thermal analysis model. By introducing the compact thermal model with linear transient thermal analysis solver, system thermal dynamics can be monitored at high efficiency. We demonstrate the temperature profile of a multi-core microprocessor system running real workloads. The evaluation results show the system thermal dependence on the manufacturing process, circuit thermal crosstalk and integrated ring heater efficiency.

Thesis Supervisor: Vladimir Stojanović
Title: Associate Professor

Acknowledgments

First of all, I would like to acknowledge my research advisor, Professor Vladimir Stojanović, for his support and mentorship. His inspiration always guides me toward the right path when I lost my direction. I have learned a lot from his insight into problems, which motivates me on my researches over the past two years.

I am grateful to work with so many brilliant and great people in the project and the group. I want to profoundly thank Chen Sun for being both a knowledgeable mentor and a good friend. I wouldn't be able to complete so much without his help. I thank Michael Georgas, Jonathan Leu and Benjamin Moss for the collaboration. I acknowledge Amr Suleiman for his companion when we were both in the lab. I also thank all the ISG members for helpful discussions.

Studying abroad can be tough, but luckily I've met many good friends. I gratefully acknowledge Yu-Wei Hu, Chun-Teh Chen, Tony Wu, Hao-Wei Su, Chia-Hsin Owen Chen and Hsin-Jung Yang for all the help they provided and all the joy we had. I also want to greatly thank Ting-Yun Sasha Huang for sharing every moment that we will never forget.

Finally, I would like to thank my parents and family for all the great support and unconditional love. This dream comes true all because of you.

Support

The work in this thesis is funded in part by DARPA.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

As the architecture of modern microprocessors is clearly moving into deep multicore regimes (Figure 1-1), paramount design issues shift from core performance to system scalability in order to support the projected gain from parallelism [22]. Bandwidth of DRAM interface is unlikely to scale up with the ever-increasing core demands [5], and will eventually constrain the achievable system performance. For desktop products, the next generation memory interface standard, DDR4 SDRAM, will have to achieve more than 266Gb/s data transfer rate [1]. On commercial server platform, custom-designed memory interface already reaches 2560Gb/s [4]. Even on mobile devices, a trend of boost in memory bandwidth is observed (Figure 1-2). To meet these demands, improved electrical signaling rates are possible, but not within reasonable power budget and packaging cost. Per-channel memory capacity is also limited since signal integrity becomes an issue under increased electrical bus speed. As in DDR4 standard, it already moves to single-DIMM point-to-point topology [1]. In addition, higher degree of multithreading in multicore reduces data locality. This results in further lowered energy-efficiency since more random access of memory suggests higher dynamic energy consumed in memory cell activation [8]. To overcome these challenges in future deeply parallel microprocessor systems, a disruptive technology is required to overcome the constraints imposed by current electrical solutions.

Recent works have proposed using monolithically-integrated silicon-photonics technology [19] for the processor-to-memory interface. Photonic link based on dense

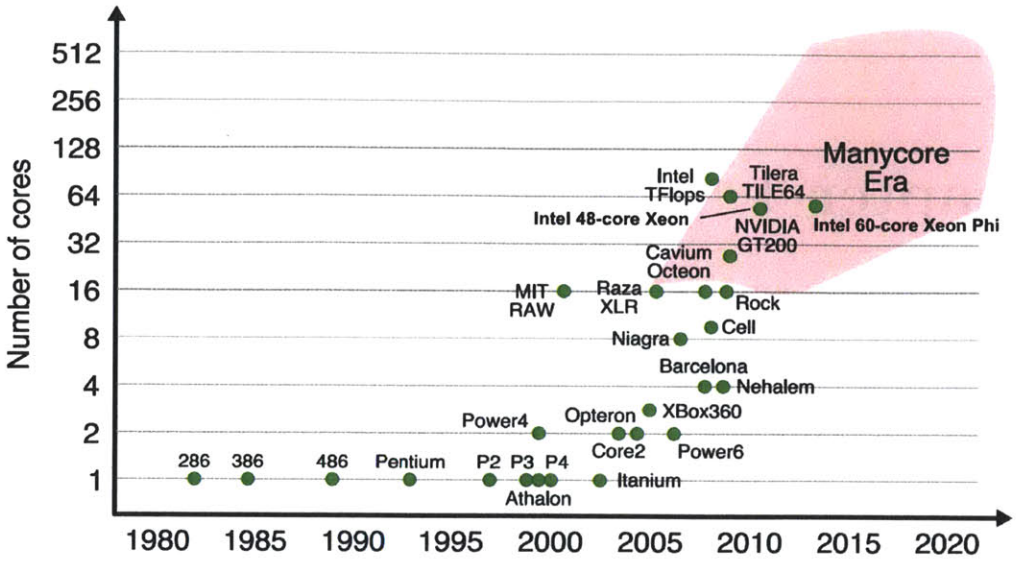


Figure 1-1: Scaling of core count in manycore architecture [7]

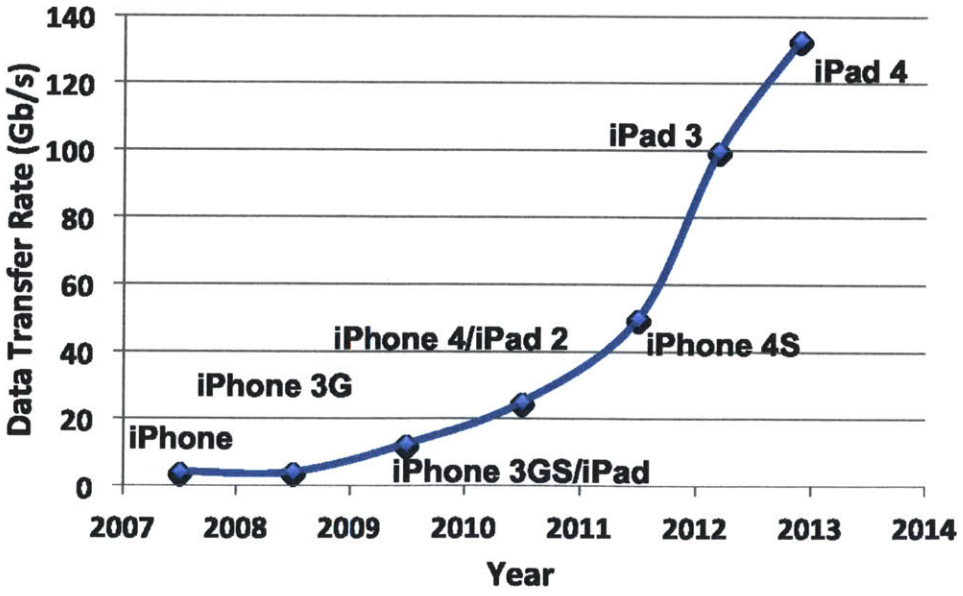


Figure 1-2: Scaling of memory bandwidth on mobile platform [3]

wavelength-division multiplexing (WDM) is expected to remove the bandwidth bottleneck with its superior bandwidth density and energy-efficiency [8]. Despite the promise, this new technology requires system, circuit and device designers to explore the tradeoffs between different components. In particular, high thermal sensitivity of optical ring resonators, the essential building block of on-chip WDM optical links, introduces vulnerability to temperature variations [9]. Chip local temperature changes due to electronics power dissipation and ring self-heating will lead to broken link function. This problem is made worse by the fact that chip power density increases drastically as technology scales, which creates an even more hostile environment for photonics. Precise characterization of cross-die thermal dynamics and corresponding photonics responses, along with the intervention of active ring thermal-tuning mechanisms, become crucial for integrated electro-optical systems.

For this thesis, we demonstrate the simulation platform that can track the thermal dynamics across the electronic circuits and photonic devices as the target architecture runs benchmarks or applications in an architectural simulator. It presents a means to capture the thermal interaction between the electrical and optical interface at scalable spatial and temporal granularities. Evaluation of the optical link performance can then be provided based on our physical models for optical devices. In addition, the computational overhead of solving the transient thermal analysis is greatly reduced by introducing the compact thermal model with linear, difference-equation based transient thermal solver. This makes the integration of electro-optical thermal modeling with architectural simulators possible, enabling real-time monitoring of system performance and exploration of thermal-inspired ring thermal-tuning mechanisms.

The rest of this thesis is organized as follows. In Chapter 2, we provide an overview of the photonics technology and discuss in detail about the impact of thermal effects on the system. In Chapter 3, we introduce the proposed thermal simulation platform. The most salient features of its framework architecture, especially the thermal modeling technique, are revealed. In Chapter 4, we perform evaluation on electro-optical systems and show the simulation results with in-depth observations.

Chapter 2

Background

2.1 Photonic Technology

Optical fiber interconnects have been used in large-scale long-distance communications to replace electrical signaling for decades thanks to its high channel capacities and low channel loss. As the computation capabilities of microchip systems boost with technology advances, photonic interconnects again become an attractive alternative over electrical links in chip-scale communication interfaces. Two paths of integrated electro-optical platforms have been proposed. Heterogeneous design [14, 23, 31] utilizes custom process development to get optimized photonics performance, but penalizes energy efficiency due to large parasitic and packaging capacitance, and costs more for 3D integration or microbump packaging. Monolithic integration, which is our assumed technology, may not yield optical devices with comparable performance to that of the heterogeneous design, but allows circuits and photonics to be built on the same silicon substrate and has been demonstrated on commercial CMOS processes [19, 21].

2.1.1 Photonic Building Blocks

Just as electrical circuit is developed on the basis of transistors and logic gates, WDM photonic link is composed by a set of fundamental building blocks, including both active and passive devices. In order to deliver monolithic integration, these

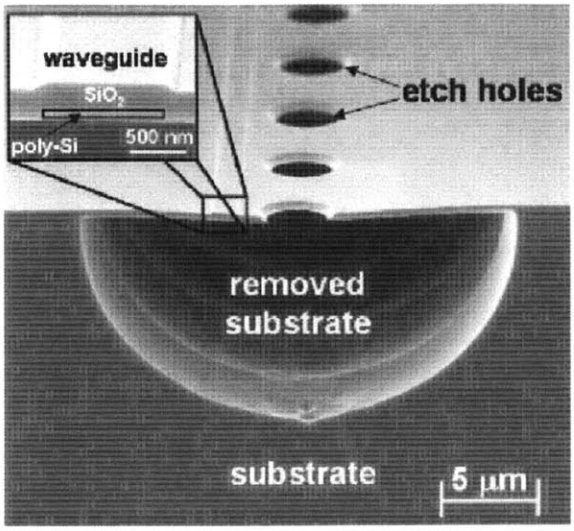


Figure 2-1: The SEM micrograph shows the undercut air-gap in bulk-CMOS process to reduce optical loss [21].

components must be compatible with the CMOS process manufacturing flow. Past works have already demonstrated successful integration of optical devices onto a single wafer of silicon with electrical circuits. The most important building blocks are reviewed in this section.

Optical Waveguides

Optical waveguides utilize the difference in refractive index between the core and surrounding materials to achieve light confinement. Usually, the core material, which is silicon in silicon photonics, has a higher refractive index than its surrounding cladding material. In various processes, waveguides are created in different ways. For example, in CMOS silicon-on-insulator (SOI) process, the waveguide core is made by the body layer sitting on top of the buried-oxide (BOX) layer [19]. In high-performance SOI process, the BOX layer is much thinner, which increases optical loss into the silicon substrate. In order to mitigate this effect, substrate undercut or substrate transfer with low refractive index materials, such as silicon carbide or silicon dioxide, becomes necessary as a post-processing step. In bulk-CMOS process, poly-

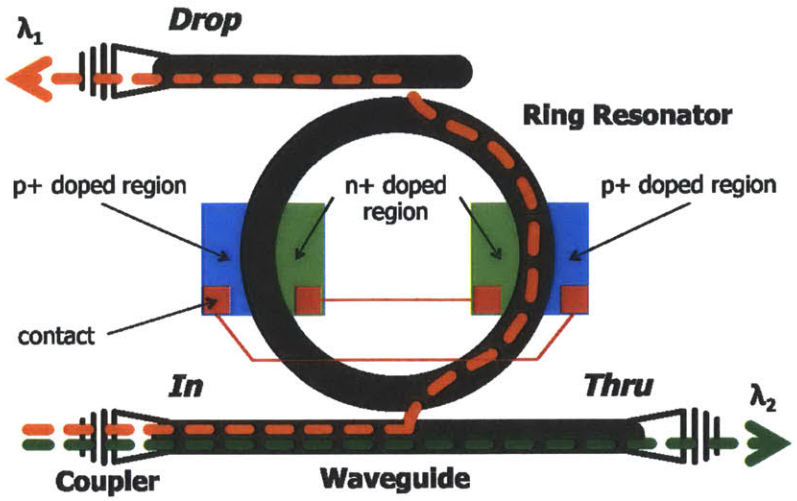


Figure 2-2: Optical ring resonator structure as a carrier injection modulator. The resonance of the ring is at λ_1, so wavelength λ_1 is trapped in the ring but wavelength λ_2 passes unaffected.

silicon layer forms the waveguide core, located on top of the deep-trench isolation [27] or even air gap as shown in Figure 2-1.

Optical Ring Resonators

Being the primary component of the optical link, the optical ring resonator acts as a notch filter on the optical spectrum when coupled to a waveguide. It is used as the basic structure to create optical modulators, switches and detectors on the WDM optical link. Figure 2-2 illustrates the cartoon of an integrated modulator based on the ring resonator structure. Thanks to the high refractive index contrast, the ring radii are typically less than 10μm, allowing hundreds of thousands of ring resonators to fit on the same die with electrical circuits.

The resonant wavelengths of the ring depend on both the ring geometry and the refraction index of the ring. Only the resonant wavelengths are trapped in the ring while other wavelengths pass unaffected. As the example shown in Figure 2-2, two wavelengths of light, λ_1 and λ_2, are coupled onto the same waveguide at the In port coupler with a ring resonator sitting next to the waveguide. The resonant wavelength of the ring is at λ_1, so λ_1 is trapped in the ring and then being dropped again at the

Drop port while λ_2 passing to the *Thru* port unaffected. By placing multiple ring resonators with different resonances on the same waveguide, each ring can perform certain actions on a specific set of wavelengths. This property forms the basics of WDM link functionalities.

Electrical Modulator Drivers and Optical Modulators

The transmitting side of the optical link is responsible for converting electrical signals into optical signals. It consists of electrical modulator drivers and optical modulators. The driver, which is essentially a chain of buffers, imprints data onto light through the optical modulator. The optical modulator is built on the structure of the ring resonator. The resonance of the ring resonator is determined by the following equation:

$$\theta = \frac{\omega L}{c} = \frac{kc_0 L}{c} = k \cdot n_{eff} \cdot 2\pi r = 4\pi^2 n_{eff} \frac{r}{\lambda}, \tag{2.1}$$

where θ is the phase shift as light travels through the ring, c is the phase velocity of the ring mode, c_0 is the speed of light in vacuum, $L = 2\pi r$ is the circumference of the ring, k is the wavenumber, ω is the angular frequency, λ is the wavelength of the light and n_{eff} is the effective index of refraction. When $\theta = 2\pi m$, m being an arbitrary positive integer, λ is the resonance wavelength. Equation (2.1) shows the relation between the refractive index and the ring resonance. Thus, by changing the refractive index dynamically, the ring resonator becomes an optical modulator device.

Fast modulation is achieved by changing the refractive index electrically through the free carrier plasma dispersion (FCD) effect [18, 20, 30]. The change in refractive index by FCD is described as

$$\Delta n = n_{fe} \Delta N_e + n_{fh} (\Delta N_h)^{0.8}, \tag{2.2}$$

where Δn is the change in refractive index, ΔN_e and ΔN_h are the changes in electron density and hole density, respectively. Experimental data in [25] shows empirically

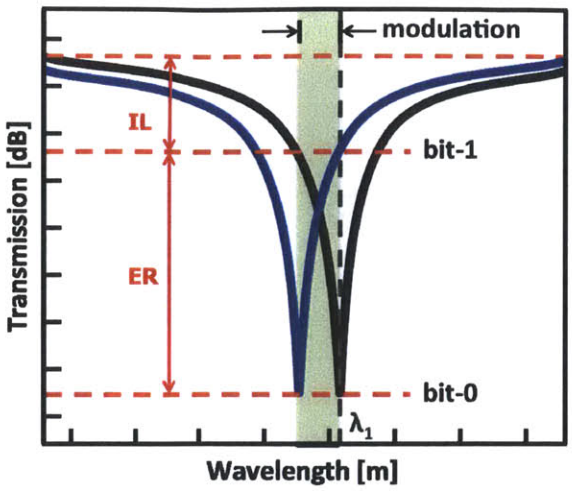


Figure 2-3: The frequency response of the ring follows a Lorentzian distribution. The resonance before modulation is at λ_1. By injecting free carrier electrically, the resonance blueshifts. The changes in optical power at λ_1 can be used to represent optical binary bits. Extinction ratio (ER) and insertion loss (IL) are two factors describing modulation characteristics.

determined characteristics for the coefficients n_{fe} and n_{fh}. At $\lambda = 1300$nm, The coefficient values are

$$n_{fe} = 6.0 \times 10^{-22} cm^{-3}, \qquad n_{fh} = 5.6 \times 10^{-18} cm^{-3}. \tag{2.3}$$

Both carrier-injection [17] and carrier-depletion [24] mechanisms were demonstrated to create ring modulators in CMOS processes. Figure 2-2 illustrates augmenting p+ and n+ doped regions on the ring to form PIN diodes. Electrical modulator drivers change the voltage of these diodes through the contact ports. Free carriers are then injected into the I-region, which is the ring waveguide, inducing FCD effect. The frequency response of the modulator at the *Thru* port is shown in Figure 2-3. It follows a Lorentzian distribution, and the resonance before modulation is at λ_1. By applying forward-biasing voltages at the PIN diodes, injected free carriers blueshifts the resonance. The optical power measured at λ_1 thus increases. The difference in the power level can be used to represent binary bits. The electrical modulator driver determines the biasing voltages based on this ring characteristics

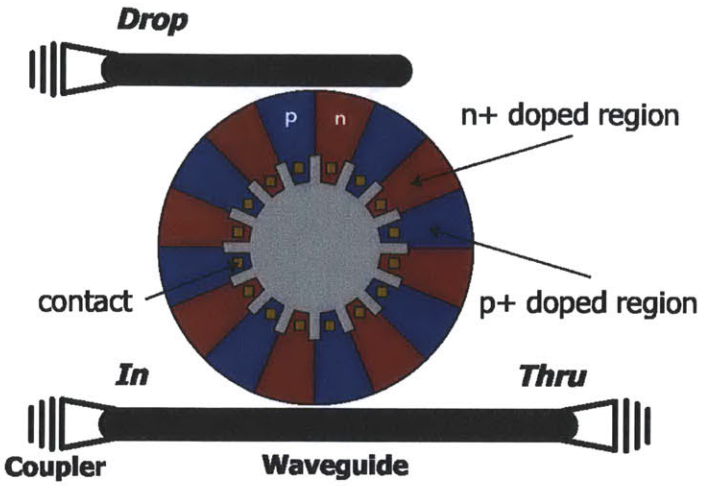


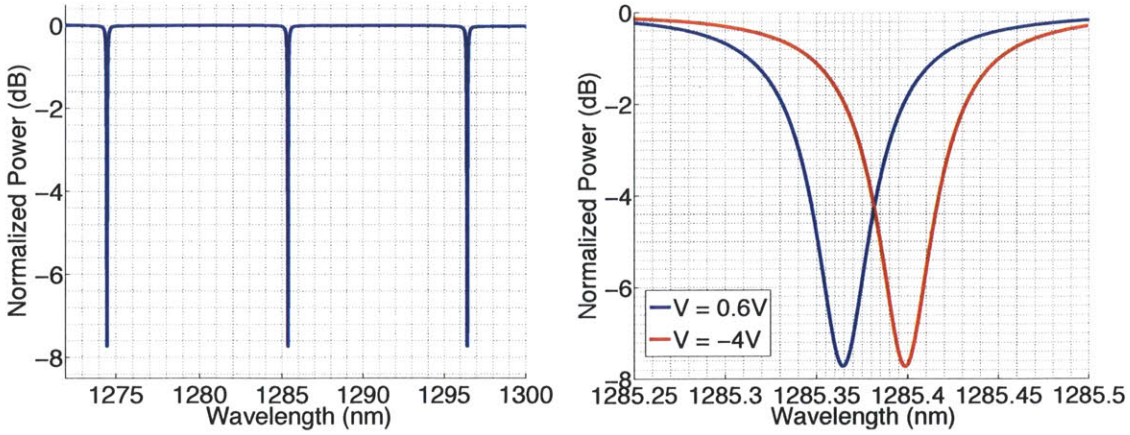
Figure 2-4: Implementation of a carrier-depletion ring modulator [24].

and also system tradeoffs. Key tradeoffs exist between the insertion loss (IL) and extinction ratio (ER). ER determines the on-to-off light intensity, which affects the receiver sensitivity design, and IL determines the total energy cost. Carrier-depletion ring modulators, on the other hand, work in a similar way. They integrate p-n junctions into the ring resonator waveguide. When applying reverse-biasing voltages, free carriers are depleted and the resonance redshifts. An example of implementation is shown in the cartoon of Figure 2-4, which has distributed lateral p-n junctions within the ring waveguide.

Table 2.1: Simulated Carrier-Depletion Ring Modulator Parameters

Parameter	**Value**
Ring Radius	7 µm
Ring Q Factor	26200
Ring Waveguide Width	1.2 µm
Ring Waveguide Height	80 nm
Ring Waveguide Confinement Factor	0.47
p-Type Doping Concentration	$5\times10^{23}\,\mathrm{m}^{-3}$
n-Type Doping Concentration	$5\times10^{23}\,\mathrm{m}^{-3}$
Number of p-n Junctions	84

Using ring/modulator models described in equation (2.1) (2.2) and (2.3), we simulate the behavior of the same type of carrier-depletion ring modulator as in Figure 2-4.



(a) Resonance FSR

(b) Modulation resonance shift

Figure 2-5: Simulation results of a carrier-depletion modulator

Table 2.1 lists the parameters of the simulated modulator. The resonance of the ring around $\lambda = 1300$nm is shown in Figure 2-5a. The free spectral range (FSR) is around 11.1 nm, or equivalently 2 THz, around 1300nm. Figure 2-5b shows the resonance shift when applying biasing voltage to modulate the ring. With a 4.6V difference in voltage, the resonance is shifted by around 0.035nm (6.4GHz).

Optical Detectors and Electrical Receivers

The receiving side of the optical link converts optical data back to the electrical domain. This process involves generating photocurrents based on the optical signal by using photodetectors, and then the data is sensed from the current by the electrical receivers. The material of the photodetector has to be CMOS flow compatible. Germanium and silicon germanium are demonstrated as good options for manufacturing photodetectors [12, 21]. However, the absorption spectra of these materials are wideband, so ring resonators are used to filter unwanted wavelengths before reaching the photodetector. The electrical receiver mainly has two types: trans-impedance amplifiers (TIA) and the current-integrating circuits. TIA is commonly used for standalone receivers, while current-integrating receiver is expected to perform better in monolithic integration environment.

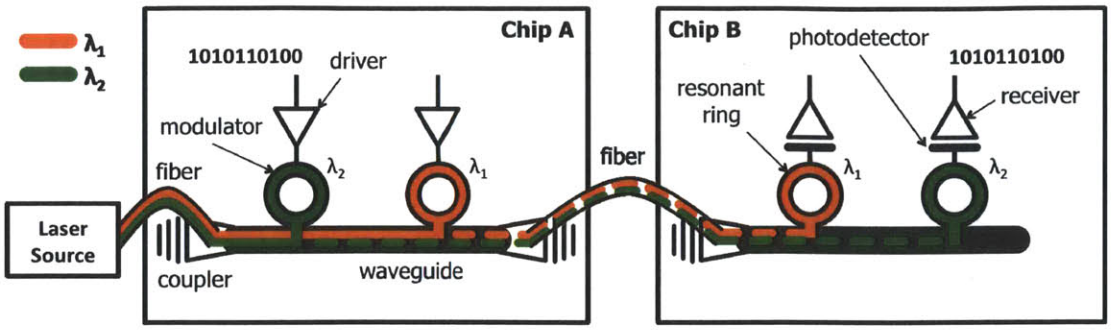


Figure 2-6: wavelength-division multiplexed (WDM) chip-to-chip photonic link

2.1.2 Photonic Link

Figure 2-6 illustrates an example of chip-to-chip wavelength-division-multiplexed (WDM) photonic link. One of the chips can be the microprocessor and the other one is the DRAM chip. Two pairs of transmitters and receivers are able to transmit two independent bitstreams simultaneously using only a single on-chip waveguide within each chip and one cross-chip single-mode fiber. Two wavelengths, λ_1 and λ_2, are provided by an external laser source and guided through the fiber to the surface of *Chip A*. The on-chip vertical grating coupler steers the light into the *Chip A* waveguide. The first ring modulator, which is tuned in to λ_2, encodes its bitstream on λ_2, leaving λ_1 untouched. Similarly, the second ring modulator only modulates data onto λ_1. When the modulated light reaches *Chip B*, λ_1 is caught by the first resonant ring filter and dumped onto the photodetector and receiver circuit. Likewise, λ_2 passes through the λ_1 ring filter and is caught by the last ring.

Since the loss of light in the waveguide is very low, usually around 3–4 dB/cm [19], there is no need to put buffers along the path of the link. Therefore, optical signals can be transmitted with high energy-efficiency. High bandwidth-density is achieved through WDM. The number of wavelengths that can be transmitted on a single waveguide is determined by the FSR of the rings. Smaller ring radius gives higher FSR, and more wavelengths can be used in a single channel. We expect to build WDM links with 32 to 64 wavelengths. However, this also implies that the operation of the link heavily relies on the functionality of the ring devices, which is the primary design challenge in building integrated photonics systems.

2.2 Thermal Dependence in Integrated Photonics System

As power density of microchip system scales rapidly, thermal-driven design is becoming as important as other design objectives such as performance and power. Uncontrolled temperature variations can reduce system efficiency or even break its functionality. System designers start to tackle this problem not only from physical mechanics perspective, but also from architectural and algorithmic point of views. Some common thermal management techniques are dynamic voltage and frequency scaling, clock gating and process throttling. These thermal-aware designs, though, are usually tradeoffs with performance.

In photonics-integrated systems, optical devices introduce another dimension of design considerations, especially constraints imposed by their thermal properties. From Section 2.1, we see the important role the ring resonator plays in an optical link, and the techniques we have to operate it for desired functionality. One major issue of the ring resonators, however, is the thermal dependence of the refractive index [6, 15]. This suggests that temperature variations will affect the ring resonance and hence fail the WDM link.

2.2.1 Ring Resonator Thermal Response

Based on the optical properties of silicon, its empirical relation between temperature and the refractive index is

$$n_{eff} = 3.38 + 13.182 \times 10^{-5} \cdot T, \tag{2.4}$$

where T is temperature in Kelvin. Equation (2.4) is applicable within the temperature range from 77K to 400K. We simulate the optical response of the ring resonators under temperature variations. As shown in Figure 2-7, the shift in resonance of the ring is linear with temperature changes. The resonance redshifts as temperature rises, and vice versa. From the simulation result, the thermal response of the ring is ap-

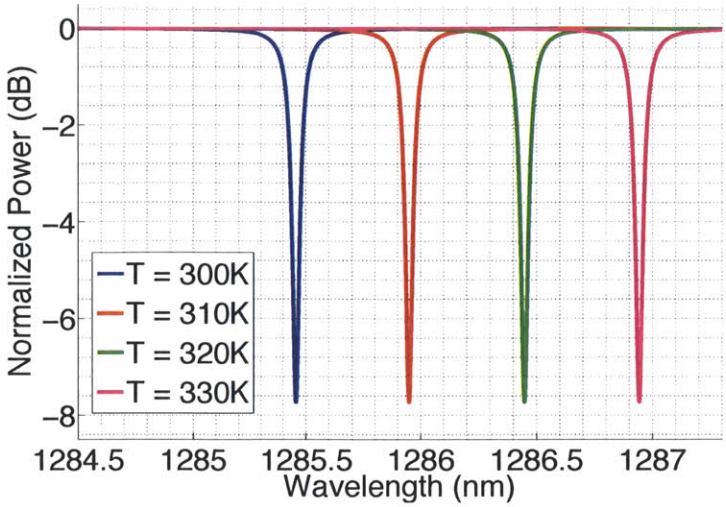


Figure 2-7: The shift in ring resonance due to temperature variations.

proximately 0.05nm/K, or equivalently 9GHz/K, around $\lambda = 1300$nm. Compared to the resonance shift caused by electrical FCD modulation, It is easier to move the resonance thermally. This also means that even one degree difference in temperature can move the ring out of its designed modulation resonances and destroy the functionality of the ring as well as the WDM link.

2.2.2 System Thermal Crosstalk

Two mechanisms contribute to the change in temperature of the ring: ring self-heating and environment heat transfer (Fig 2-8). The former depends on the input optical power on the ring. In general, at high powers, the trapped light in the ring is absorbed via two photon absorption (TPA) and generates free carriers. Due to FCD, this will result in blueshift of the ring resonance. The generated carriers are then absorbed via free carrier absorption (FCA). TPA and FCA, along with the surface etching absorption of carriers, create the self-heating effect and cause redshift of the resonance. Mostly the overall shift of resonance due to this process is redshift. On the other hand, the environment temperature variations will also change the thermal dynamics of the ring through heat transfer. In particular, within the monolithically-integrated system, optical devices usually sit beside electrical circuits to benefit from

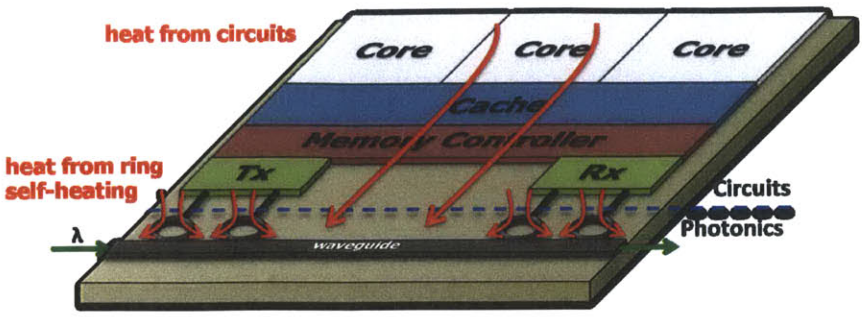


Figure 2-8: Thermal crosstalk in integrated photonics system. Both heat transfer from circuit and from ring self-heating change the thermal dynamics of the system.

low parasitic capacitance. This scenario creates a huge concern on the optical ring due to possible high power dissipation of the electrical circuits. Significant redshift of the ring resonance is expected.

2.2.3 Toward Thermal Control

Thermal effects of the ring resonator, nevertheless, can be beneficial to the system as well. Process variations cause mismatch between designed and manufactured ring properties, such as ring geometry or doping concentration. With appropriate thermal controls, the ring characteristics can be tuned back to desired performance. Therefore, in order to fight with system thermal crosstalk and process variations, heaters are integrated with the ring resonators to heat up the ring by purpose. Figure 2-9 shows the SEM micrograph of an implementation of a ring resonator with integrated heaters in bulk-CMOS process. The heater is the doped (yellow) sections of ring waveguide, which is made with poly-silicon, to reduce resistance for higher power delivery. To control the heater, ring thermal-tuning algorithm becomes an indispensable part for the integrated photonics system. It fills the gap between temperature dynamics and system performance, ensuring the functionality of the optical links.

Figure 2-9: The SEM micrograph shows a ring resonator with integrated heater [28, 29]. The heater is the doped (yellow) section of the ring waveguide with reduced resistance.

Chapter 3

Thermal Simulation Platform

This chapter focuses on the development of a simulation platform for the evaluation of monolithically-integrated photonic links under temperature variations. The simulator enables real-time thermal monitoring and feedbacks by introducing the compact thermal model with linear transient thermal solver. Along with the integration of architectural and photonic device models, it serves as a complete description of the system dynamics from high-level instructions to low-level physical operations.

3.1 Motivation

Thermal impacts on integrated photonics links, as described in Section 2.2, emerge to be the key for the future of electro-optical system. In particular, monolithic integration imposes higher limit in the design space and requires detailed inspection on the components within the system. Corresponding closed-loop thermal control logic is expected to be the last piece in building a high performance integrated photonics system, and the need to model and simulate system-wide thermal behaviors at design stage urges the creation of tools for thermal simulation.

HotSpot, a verified thermal modeling tool, is renowned for architectural studies such as dynamic thermal management and system thermal hotspot characterization [10]. *HotSpot* uses the compact thermal model as opposed to the finite element method commonly used in commercial thermal-modeling tools to facilitate the ther-

mal analysis process. While being suitable for modeling systems at functional block level above dozens to hundreds of micrometers, it is still inefficient at tracking system-wide thermal dynamics at device scale with high temporal granularity. In addition, it lacks the flexibility to configure for different manufacturing processes, making it difficult to customize for high accuracy designs.

To address these shortcomings, we developed the thermal simulation platform as a tool bridging architecture performance profiling and device physical properties based on system thermal behaviors. The simulator considers multicore or manycore microprocessor architectures with on-chip photonic links, and models the real-time thermal dynamics of the processor running applications or benchmarks. It is capable of capturing the thermal interaction between the electrical circuits and the optical devices as well as the ring self-heating effects, and measures the performance of the optical links throughout the simulation. Scalable granularities at both spatial and temporal domains are achieved through the platform framework design and the thermal modeling techniques.

3.2 Framework Overview

The thermal simulator framework, as shown in Figure 3-1, consists of three components: the performance model, the physical model, and the thermal model. The functionality of each model and the interaction between models in the simulator architecture are described as follows.

3.2.1 Performance Model

The performance model integrates tools such as Graphite [16] to serve as the scalable application-level architectural simulator. Users can develop and swap in various multicore or manycore architectures, including analytical optical link models, and simulate the execution of any compiled benchmarks or applications. Performance statistics such as electrical circuit activity factors and optical link usage patterns are generated and updated at each sampling period.

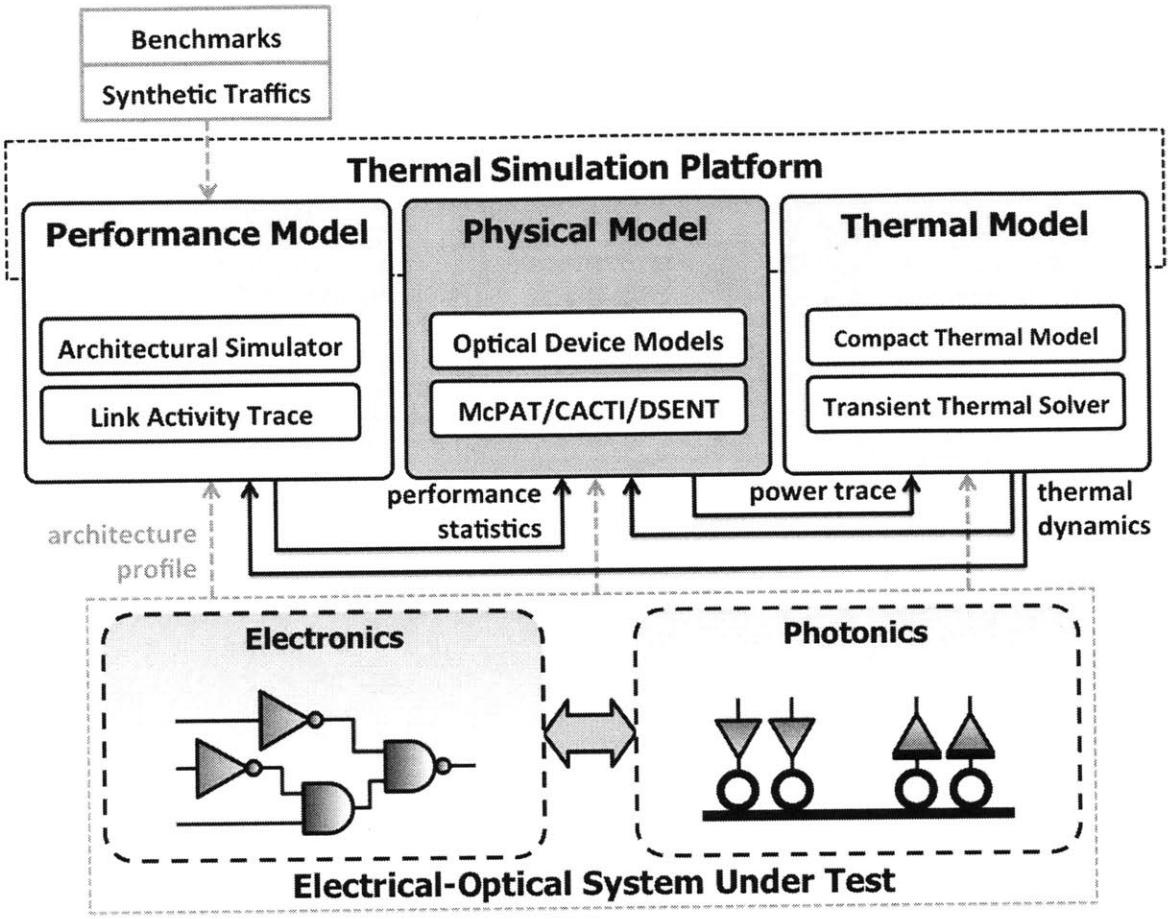


Figure 3-1: The framework of the thermal simulator. It consists of three components: the performance model, the physical model and the thermal model. Three models exchange information based on simulation states.

3.2.2 Physical Model

The physical model consists of optical device models, ring thermal-tuning algorithms and design exploration tools such as DSENT [26], McPAT [13], and CACTI [2]. It first parses the system architecture and technology parameters to construct the related physical properties of the system. Performance statistics are then read from the performance model for estimation of physical properties of both circuits and photonics. Power consumption traces for all building blocks, in particular, are created for thermal dynamics calculation.

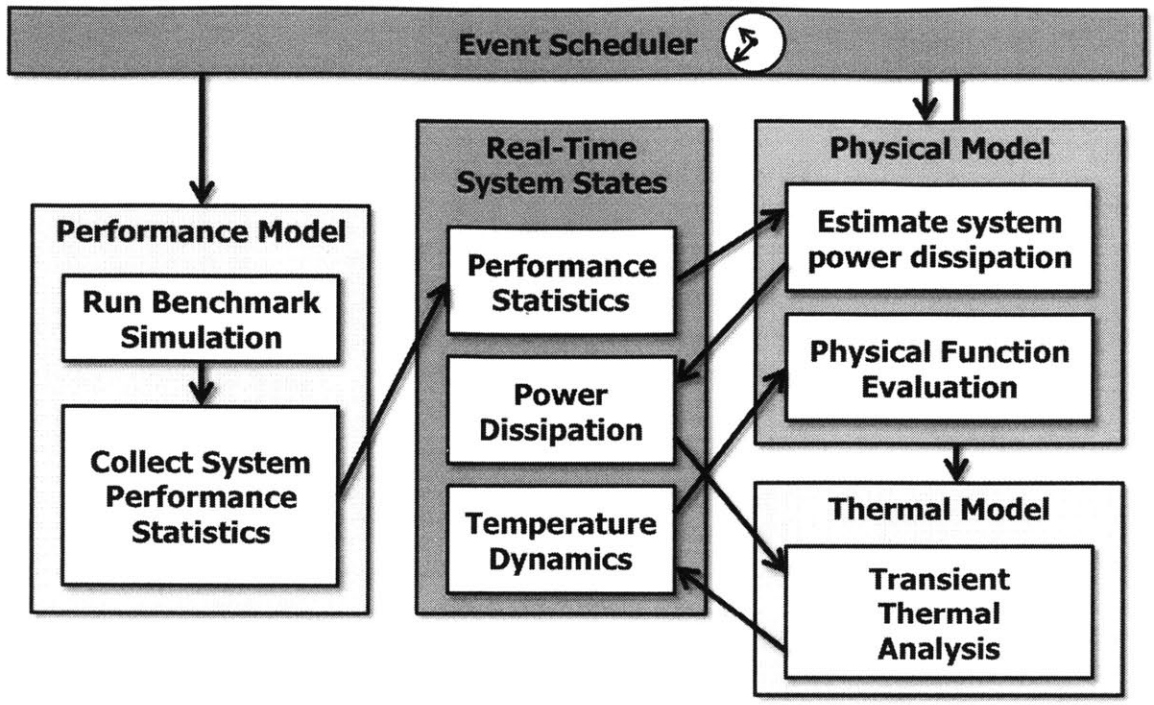


Figure 3-2: The system architecture of the thermal simulator. The event scheduler controls the operation of the three models. The models interact with each other through the centralized system state management structure.

3.2.3 Thermal Model

The thermal model first creates the system thermal representation structure based on the architectural floorplan and system process definition. It then performs transient thermal analysis by using the power traces generated in the physical model to evaluate the temperature at various points in the system. Temperature information is fed back to the physical models and performance model. The physical model updates the state of the link through its device models and activates ring thermal-tuning logic to form closed-loop control functions. The performance model can also simulate thermal management protocols for the design exploration at the architectural level.

3.2.4 Simulator Architecture

The simulator system architecture is shown in Figure 3-2. A system event scheduler arbitrates the three models. It advances system time and issues commands to

each model. By centralizing the management of system state information, the hazard that one model locks the operation of others is minimized. Different models can thus run at independent and runtime-adjustable sampling frequencies as illustrated in Figure 3-3 for accuracy and efficiency tradeoffs, making the system granularities flexible. The physical model can switch between two operation modes: the sub-bit time mode and the statistical mode. To characterize signal transition and inspect eye-diagram of the optical links, sub-bit time granularity is required. The simulator switches to sub-bit time mode for high accuracy simulation results. In this mode, exact transient quantification of each component within the system is calculated. On the other hand, when the link is idle or link detail information is not needed, the simulator can switch to statistical mode. Instead of obtaining device transient information, statistical estimation on device properties is provided at lower sampling frequency, and the simulator can run at relatively high efficiency.

3.3 Thermal Modeling Techniques

System-wide thermal dynamics modeling fills the gap between high-level architecture profiling and low-level device property evaluation. However, it is also the most critical part in the whole simulation platform since high granularity thermal characterization implies high computational overhead. In order to achieve efficient yet scalable thermal analysis, we introduce the compact thermal model with linear transient thermal solver.

3.3.1 Compact Thermal Model

Heat transfer within the integrated photonics system chip is mainly due to thermal conduction. Heat conduction is governed by the Fourier's Law of heat transfer. The one dimensional form of the equation is:

$$q = -k\frac{dT}{dx}, \tag{3.1}$$

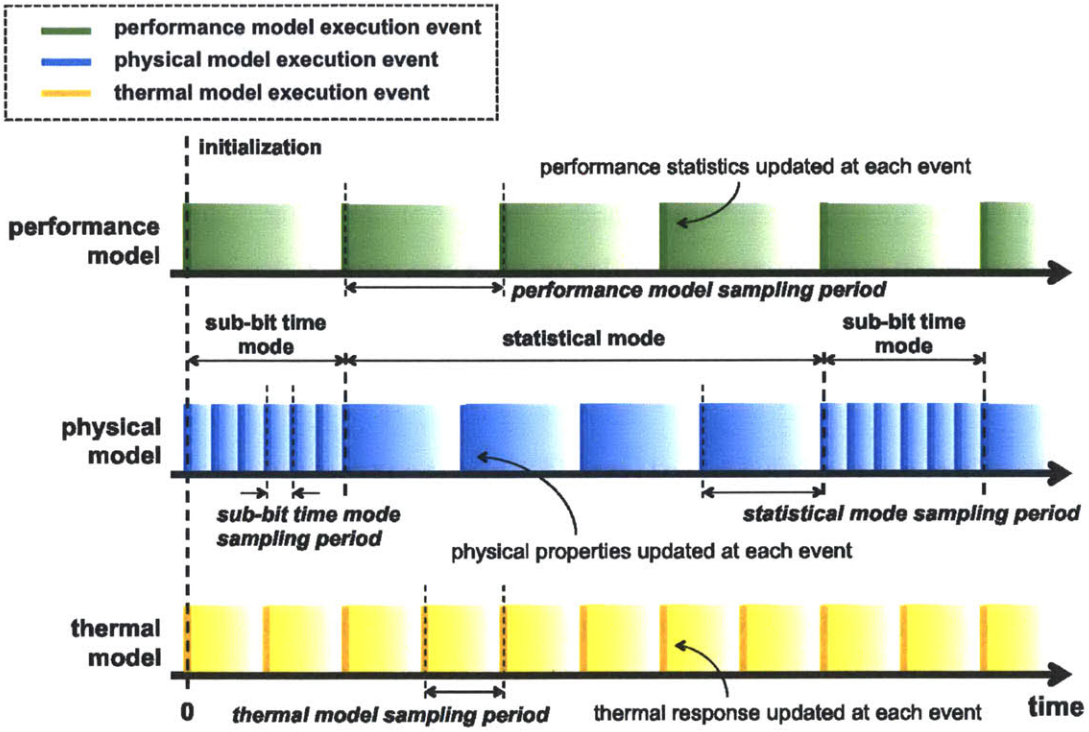


Figure 3-3: An example of the model event timing diagram. Different models run at independent sampling periods. According to the current state of the simulator, the physical model can switch between sub-bit time mode and statistical mode to balance accuracy and simulation efficiency.

where q is the heat transfer rate per unit area, k is the thermal conductivity, and dT/dx is the temperature gradient at position x. If we assume $q = Q/A$, where Q is the heat transfer rate and A is the heat conducting area, we can rewrite equation (3.1) as

$$\frac{T_2 - T_1}{Q} = \frac{1}{k}\frac{L}{A}, \tag{3.2}$$

where $T_2 - T_1$ is the temperature difference between two points at distance L. This equation has exactly the same form as the Ohm's Law, with T being voltage, Q being electrical current and k being electrical conductivity. Therefore, we can use the thermal-electrical duality listed in Table 3.1 to construct the thermal model as a equivalent electrical circuit. This form of thermal modeling is called compact thermal model. The same modeling technique is also used in *HotSpot* for thermal analysis, and is verified to have high accuracy as compared to commercial tools using finite element methods.

Thermal Property	**Dual Electrical Property**
Thermal Conductance $(1/R_T)$	Electrical Conductance $(1/R_E)$
Thermal Capacitance (C_T)	Electrical Capacitance (C_E)
Heat Transfer Rate (Q), or Power (P)	Electrical Current (I)
Temperature (T)	Voltage (V)

Table 3.1: Thermal-Electrical Duality

To construct the compact thermal model, the system floorplan and manufacturing process definition are analyzed. Figure 3-4 illustrates converting system floorplan to its compact thermal RC equivalent. It is essentially a three-dimensional T-model representation of the floorplan units. The dimension of each floorplan unit and its corresponding material determine the thermal resistances $R_{T,x}$, $R_{T,y}$ and $R_{T,z}$ of that unit as shown in equation (3.2). The thermal capacitance C_T is calculated similarly. By connecting the thermal resistance between neighboring floorplan units, a thermal RC network is formed as the compact thermal equivalent of the system. The energy generated in each unit induces heat transfer to neighboring units. From the thermal-electrical duality, we can use the power consumption as the current source input to the system. The temperature variations at the node in the middle of each unit represent

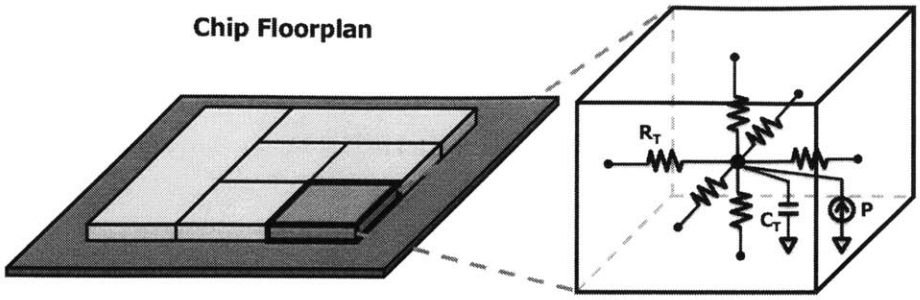


Figure 3-4: The system floorplan is analyzed and converted to the compact thermal model. The dimension and material determine the thermal conductance and capacitance of each floorplan unit. The power consumption represents the heat transfer rate and affects the thermal dynamics.

the thermal response for the whole unit. Therefore, more fine-scale floorplan implies more accurate thermal dynamics at specific location of the system.

Besides system floorplan, the manufacturing process as well as packaging layers also greatly affect the thermal behaviors. Different layer materials and layer thickness have distinct impact on both lateral and vertical heat transfer time constants, and need to be taken into account seriously. The simulator supports the definition of 3D system layer structure as shown in Figure 3-5. This example demonstrates the mapping from a CMOS SOI process, which is commonly used in integrated photonics systems, to the simulation layer definition. Each physical layer in the process can be mapped to multiple simulation layers by dividing down the thickness of that physical layer in order to achieve higher thermal response granularity. By defining the thermal conductance and heat capacity of the materials, the same floorplan can be used for every simulation layer to create the thermal RC compact model for that layer, and a full system RC network is formed by connecting models from all layers.

3.3.2 Linear Transient Thermal Solver

By introducing the compact thermal model, we convert the system under test into a thermal RC network. Therefore, solving the transient thermal dynamics is the same as doing the transient analysis on the equivalent RC circuit. This enables the application of many well-developed techniques and models to tackle this problem.

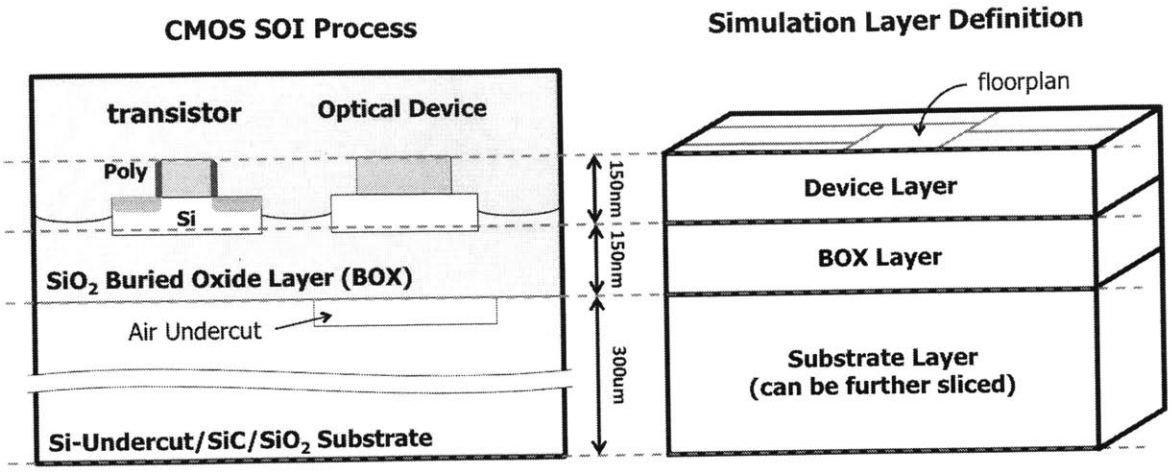


Figure 3-5: Converting a CMOS SOI process into the corresponding simulation layer definition. By defining the materials and thickness of each layer, heat transfer among vertical layers can be precisely modeled.

RC network is a very basic and common type of circuit which can be analyzed by relating to the I-V characteristics of the elements. However, it is very inefficient by directly solving the differential form of the capacitance I-V equation:

$$I = C\frac{dV}{dt}, \tag{3.3}$$

where C is the capacitance of the capacitor. Instead of looking for numerical methods on solving ordinary differential equations, such as the Runge-Kutta methods, we further transform the capacitor into its companion model, which is a commonly used technique adopted in simulation tools such as SPICE [11], and the simulator can take advantage of solving pure linear equations.

The concept of companion model is based on numerical integration for the capacitor I-V characteristics. Based on the backward-Euler integration formula, we can write the voltage across a capacitor at time point $n+1$ as a function of voltage at time point n by

$$V_{n+1} = V_n + \Delta t \cdot \frac{dV_{n+1}}{dt}, \tag{3.4}$$

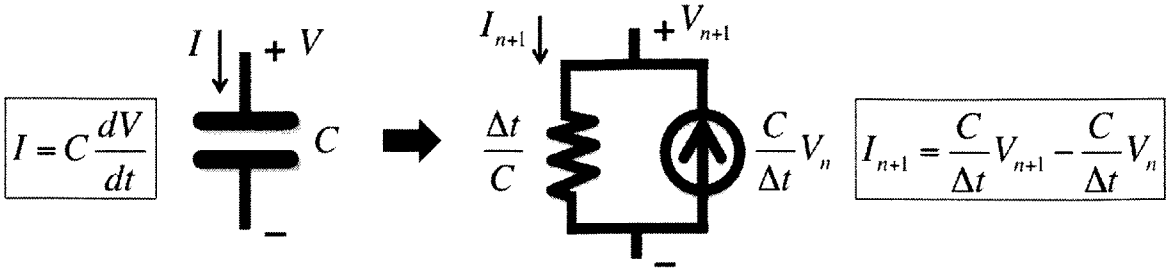


Figure 3-6: The companion model for the capacitor. Based on numerical integration, the voltage across the capacitor at the next time step can be related to the voltage at current time step linearly, which transform the capacitor into the model with only resistance and current source.

where $\Delta t = t_{n+1} - t_n$. according to equation (3.3), we get

$$V_{n+1} = V_n + \frac{\Delta t}{C} \cdot I_{n+1}, \tag{3.5}$$

and we can rewrite it as

$$I_{n+1} = \frac{C}{\Delta t} \cdot V_{n+1} - \frac{C}{\Delta t} \cdot V_n. \tag{3.6}$$

This I-V characteristics illustrates the model as shown in Figure 3-6. It transforms the ODE in equation (3.3) into a pure difference equation. The new model can be viewed as a resistor with resistance $\Delta t/C$ in parallel with a current source with current $(C/\Delta t) \cdot V_n$. By choosing appropriate time steps, the whole RC network becomes a pure resistor circuit, which can be solved at very high efficiency even at relatively large scale. To compare the efficiency, we simulate RC networks with different problem sizes on both our difference-equation solver and the traditional fourth-order Runge-Kutta method. The result is shown in Table 3.2. With no accuracy loss, the speedup is significant, and the advantage is more pronounced for larger problem size.

# of Nodes in the RC Network	**Speedup**
1600	13.7×
3200	300×

Table 3.2: Linear Solver Speedup over fourth-order Runge-Kutta method

Chapter 4

Thermal Behavior Evaluation in Integrated Photonics System

With the thermal simulator introduced in Chapter 3, we study various system configurations to get insights into the thermal behavior within integrated photonics systems. First, we perform simulation on a two-core microprocessor running a benchmark program. It gives us a flavor of thermal dynamics induced by real workloads. Second, we explore the heat transfer characteristics among common system processes. Finally, the thermal behavior of the ring resonator in integrated photonics systems is investigated, which demonstrates the capability of the thermal simulator capturing real-time optical response. These observations can be used as design guidelines to customize system architecture design, floorplan strategies and ring thermal-tuning algorithms.

4.1 System Thermal Dynamics in Architectural Simulation

The multicore architecture under test features cores communicating through on-chip optical WDM links. The floorplan of a single building tile is shown in Figure 4-1. It consists of a single 1GHz in-order single-issue core, private 32KB L1,

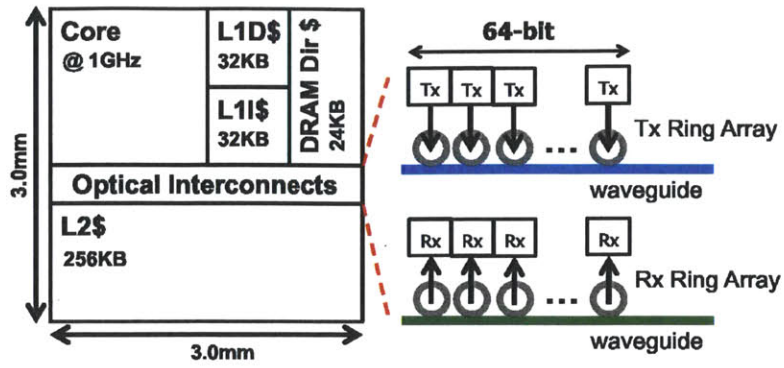


Figure 4-1: The floorplan of a single tile microprocessor with optical links.

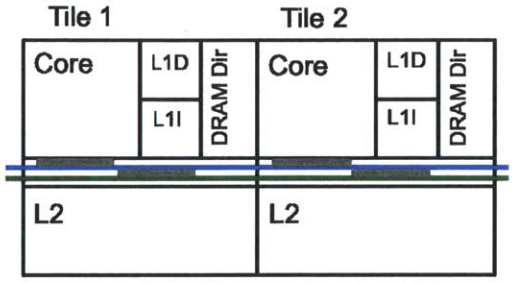


Figure 4-2: The 2-core architecture featuring on-chip WDM optical link network.

private 256KB L2 and 24KB DRAM directory caches. Network components include routers, transceivers, optical resonant ring array of modulators and detecting filters, and waveguides. The simulated flit size is 64 bits. A simple multicore based on this structure is a two-tile processor as shown in Figure 4-2. It has two optical WDM links. Each link consists of 64 data wavelengths multiplexed onto a single waveguide and sends one flit per cycle. The resonant ring array has 64 separate devices on both the transmit (Tx) and receive (Rx) sides, each with its own electrical modulator driver or receiver. The optical links run on a 1GHz clock.

The temperature evolution of the rings during application runtime is the most interesting part of the system. Per-ring spatial granularity is desired to capture the temperature profile of individual devices. On the other hand, since electronics are not as sensitive to temperature, coarser per-block granularity is adequate (Figure 4-2).

Figure 4-3 shows the temperature traces of blocks in Tile 1 of the two-core system

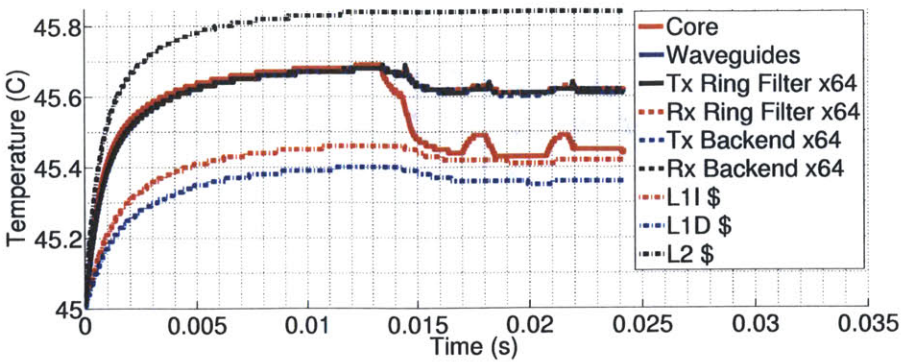


Figure 4-3: Temperature trace of Tile 1 blocks in the 2-core architecture

while running a two-thread radix sort benchmark with scaled workloads. Due to location, footprint size and benchmark activity, all blocks exhibit distinct thermal dynamics. The initial temperature of the system is the ambient temperature, which is assumed to be 45 degrees Celsius. For the first 13ms, each block in the system is in the heat-up phase. The temperatures of the caches and optical devices then stay at a relatively stable point, while the temperature of the core shifts a greater amount. The 64 individual devices in the ring array and transceivers show nearly identical thermal response throughout the simulation, which suggests that the heat transfer is quite smooth and even due to the random data pattern. Thermal crosstalk from electrical circuits, however, does affect optical device temperatures as shown around the last 10ms of the simulation.

This simulation, while only runs for a relatively simple benchmark, gives some hints on the thermal control strategies. First, the thermal control logic must be able to compensate the performance gap due to the temperature difference between the initial temperature, or ambient temperature, and the runtime stable temperature. Second, the floorplan of the integrated photonics system should avoid placing thermal sensitive optical devices beside blocks with high thermal variations, such as cores. Third, due to a relatively random of data transmission pattern among all Tx and Rx devices, an universal thermal-tuning mechanism is expected to cover the control of ring resonator performance.

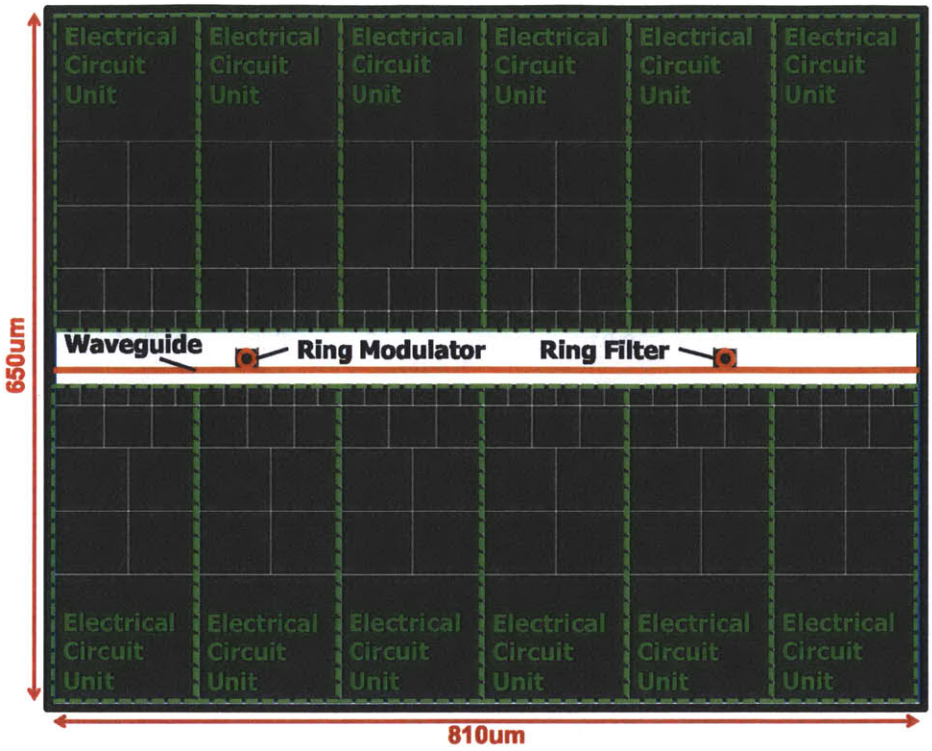


Figure 4-4: The floorplan of a test integrated photonics system. The top and bottom side are circuit blocks. In the middle, there are two ring resonator devices, one modulator and one filter, coupled to a waveguide.

4.2 Process Heat Transfer Characteristics

In Section 3.3.1 we discussed about the techniques for building the thermal model. It depends not only on the floorplan but also on the manufacturing process. The process layer definition mapping is provided for more accurate thermal simulation. In silicon photonics, CMOS SOI is the most commonly used process, since the BOX layer is naturally a good cladding material for waveguides. However, in order to deliver high performance circuitries, commercial SOI usually uses a very thin BOX layer. For monolithic integration, the silicon substrate has to be fully or partially replaced by low index materials such as air, silicon carbide or silicon dioxide to reduce mode loss. These materials, though, all have very different thermal properties. In this section, we will study the heat transfer characteristics of these materials used for integrated photonics systems and its impacts on the optical devices.

Figure 4-4 shows the floorplan of an integrated photonics system for test. The structure has electrical circuits at the top and bottom sides, each with 6 identical circuit units. Each circuit unit is further divided into several smaller floorplan blocks in order to see thermal dynamics at a finer granularity. The photonics devices sit in the middle with one ring modulator and one ring filter coupled to a single waveguide. Both ring device have integrated heater for thermal tuning.

The process simulation layers is listed in Table 4.1. The device layer includes both electrical circuits and optical devices. The substrate is divided into 6 more layers so the vertical heat transfer can be modeled in a greater detail. We use 4 different substrates: silicon, silicon with air undercut beneath optical devices, silicon carbide and silicon dioxide, Their thermal properties are shown in Table 4.2. Note that we assume the heat transfer within the undercut air cavity is by conduction rather than convection since the air flow is negligible.

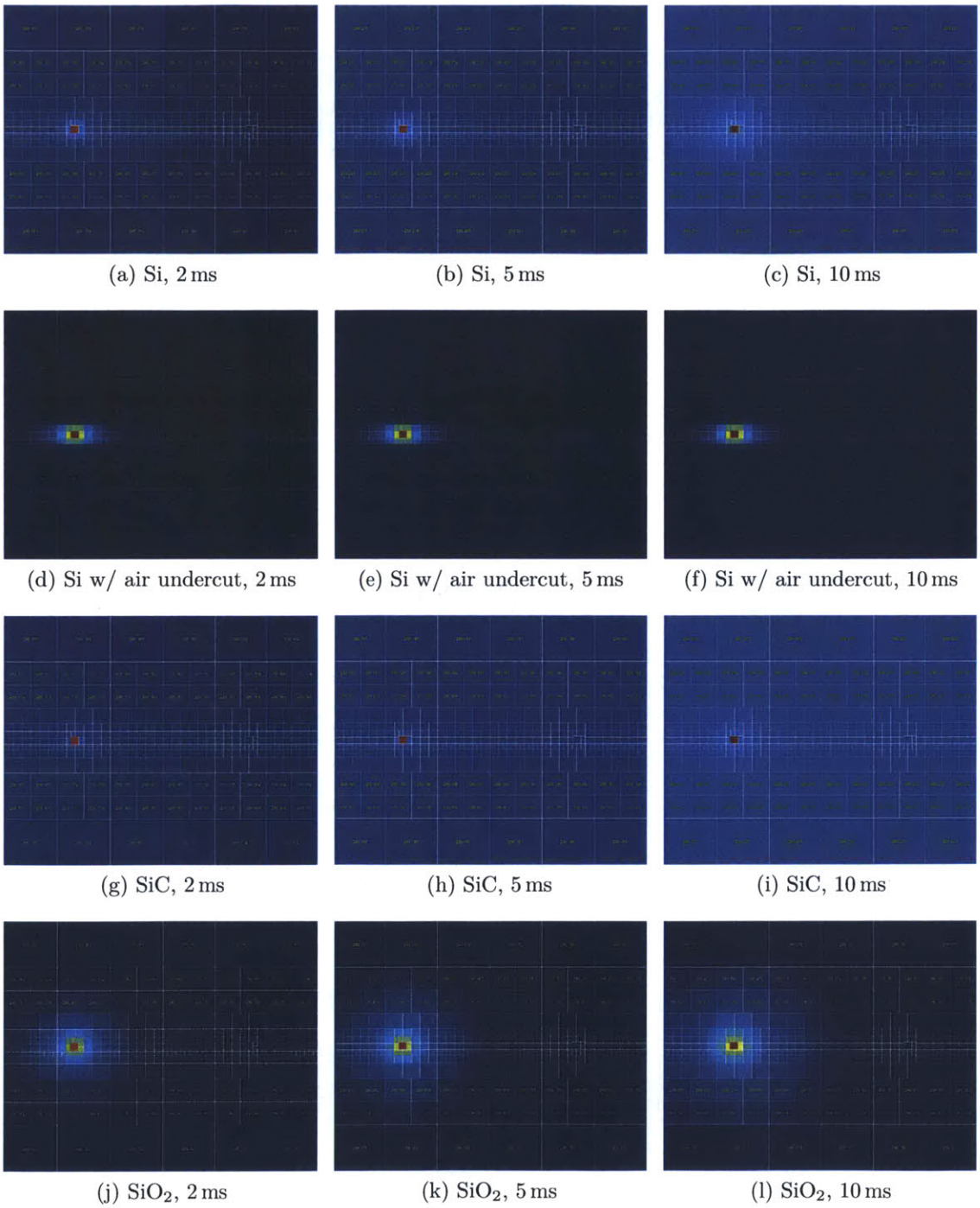
Layer	**Material**	**Thickness**
Device	Si	150 nm
BOX	SiO_2	150 nm
Substrate(1)	Si/Si with air undercut/6H-SiC/SiO_2	1 µm
Substrate(2)	Si/Si with air undercut/6H-SiC/SiO_2	2 µm
Substrate(3)	Si/6H-SiC/SiO_2	5 µm
Substrate(4)	Si/6H-SiC/SiO_2	32 µm
Substrate(5)	Si/6H-SiC/SiO_2	64 µm
Substrate(6)	Si/6H-SiC/SiO_2	192 µm

Table 4.1: Layer definition of the CMOS SOI process for simulation

Material	**Thermal Conductivity** [W/(m·K)]	**Specific Heat** [J/(m^3·K)]
Si	149.00	1.65×10^6
Air (conduction)	0.0257	1189.8
6H-SiC	490.00	2.25×10^6
SiO_2	1.38	2.27×10^6

Table 4.2: Thermal properties of process substrate materials

In this experiment, we use the ring modulator heater as the only heat source. The heater keeps heating at a constant delivered power of 3 mW during the simulation,



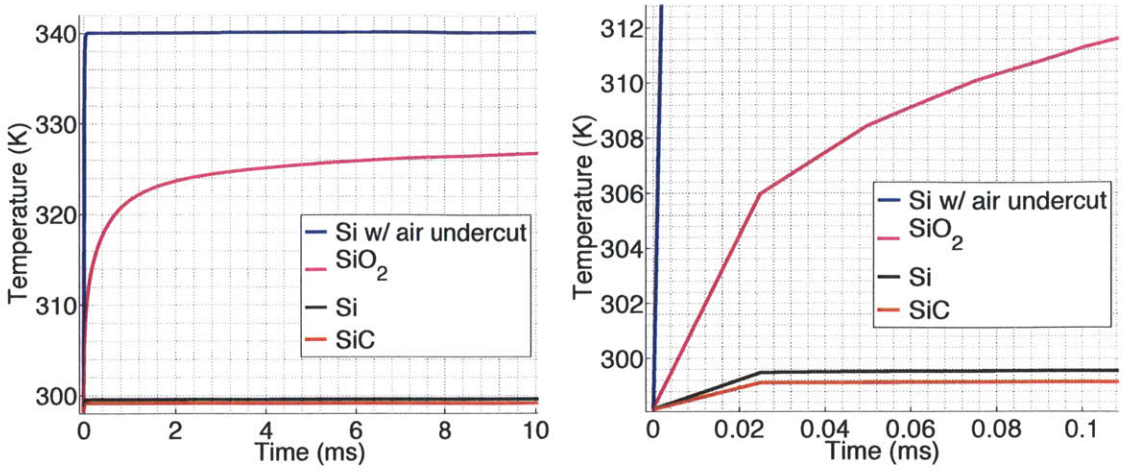
(a) Si, 2 ms (b) Si, 5 ms (c) Si, 10 ms

(d) Si w/ air undercut, 2 ms (e) Si w/ air undercut, 5 ms (f) Si w/ air undercut, 10 ms

(g) SiC, 2 ms (h) SiC, 5 ms (i) SiC, 10 ms

(j) SiO_2, 2 ms (k) SiO_2, 5 ms (l) SiO_2, 10 ms

Figure 4-5: The temperature color map of the device layer with different substrate materials at different simulation time points. (a)–(c): silicon, (d)–(f): silicon with air undercut beneath optical devices, (g)–(i): silicon carbide, (j)–(l): silicon dioxide.



(a) The entire simulation: 0–10ms

(b) Zoom-in: 0–0.1ms

Figure 4-6: The temperature of the modulator with different substrate materials.

and the total simulation time is 10 ms. Figure 4-5 shows the device layer temperature color map for four different substrates at 2ms, 5ms and 10ms of the simulation. Note that, for each simulation with one substrate material, the temperature color range is scaled to the highest and lowest temperatures of the whole simulation, so the same color might not represent the same temperature value across four simulations. Figure 4-6 compares the temperature variations of the modulator among four substrate materials. It is clear that the modulators in both silicon substrate with air undercut and silicon dioxide substrate, which have the lowest thermal conductivities, have relatively large temperature changes at long time constants since the heat cannot easily spread out. We can see a local hotspot at the modulator, while the temperature at the right-hand side of the chip doesn't even change. In the case of air undercut, the heat is mostly constrained within the air cavity so the circuit area has negligible temperature variations within 10 ms. On the other hand, the modulators with the other two substrates, which have much higher thermal conductivities, only change around one to two degrees, but their time constants are quite small. The temperature color maps show that almost the entire chip is heating up though the modulator temperature is still higher. Since the substrate is thermally conductive, most of the

heat quickly goes down into the substrate and spreads out, and then the substrate is heating up the entire chip slowly.

From the optical device point of view, the thermal behaviors shown in different substrate materials present challenges from different aspects for the design of thermal-tuning algorithms. For low thermal conductivity materials, the thermal control mechanism has to compensate for large temperature changes, but for high thermal conductivity materials, it has to be able to track the temperature change very quickly. Also, floorplan has to be reconsidered since the creation of local hotspot might have a negative effect for nearby devices.

4.3 Integrated Ring Resonator Thermal Properties

In this section we investigate the thermal properties of the ring resonator based on our thermal model and optical device models. Through this section the simulations all assume the same test system as in Figure 4-4. First, we will inspect the DC behavior of the ring resonator by heating up the modulator directly. Second, we send random data sequence through the optical link and examine the impact of circuit thermal crosstalk on the ring modulator performance.

4.3.1 Heater Efficiency and Ring Self-Heating

As demonstrated in Section 4.3, with silicon dioxide substrate, a noticeable local hotspot around the heater as well as the modulator is created in the system. This experiment focuses on the DC behavior of the ring resonator under the thermal influence of the integrated heater in silicon dioxide substrate, which is an indicator of how efficient the heater is being able to tune the ring resonator. We use the same carrier-depletion ring modulator as in Table 2.1, except that the Q factor is tuned to 4000. All the circuits are put into sleep mode with zero power consumption. The heater is still the only heat source with 3 mW delivered power, and it is toggled be-

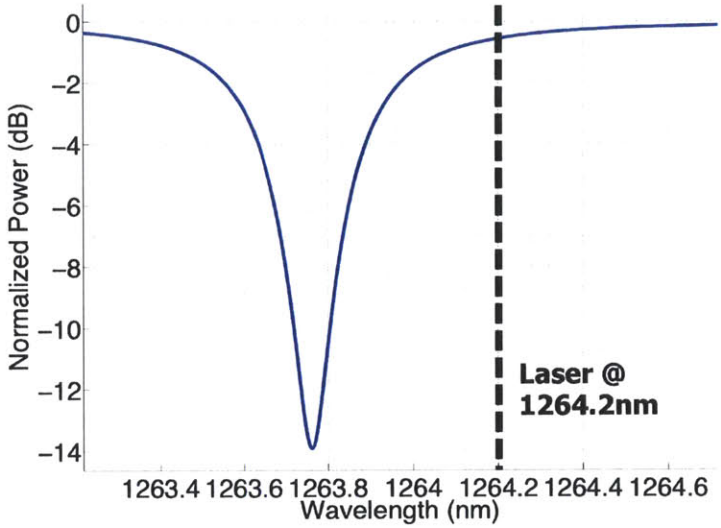
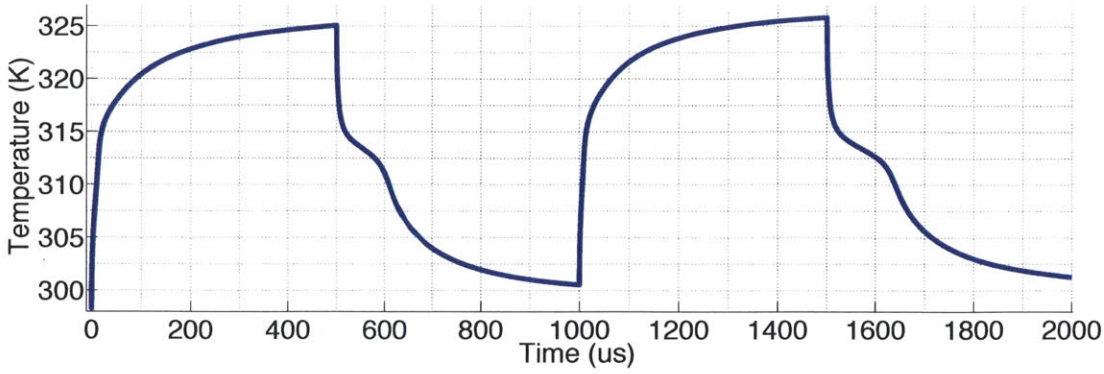


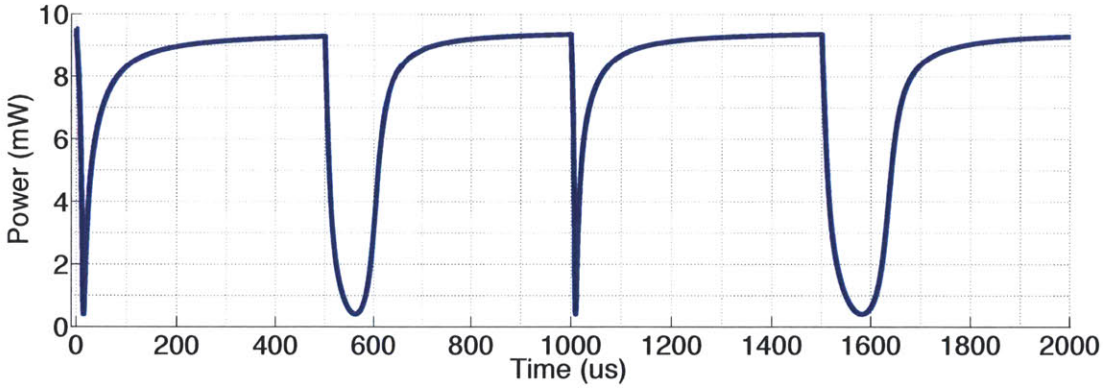
Figure 4-7: The frequency response of the ring modulator at ambient temperature, 298.15K, and the laser wavelength.

tween on and off every 500 µs. The ring modulator temperature initially is at the ambient temperature, which is 298.15 K, and the corresponding resonance is shown in Figure 4-7. The resonance center wavelength is around 1263.8 nm, and we tune the laser source to a fixed wavelength of 1264.2 nm. The laser power is 10 dBm, and is coupled into the *In* port of the ring modulator directly as shown in Figure 2-4. It is expected that, as the heater raises the temperature of the ring modulator, the resonance will redshift toward the laser wavelength, and vice versa.

The temperature trace and the *Thru* port power of the ring modulator are demonstrated in Figure 4-8. The thermal time constant is the key factor since it determines the resonance variation dynamics. Figure 4-8a shows that the thermal time constants of the heater on the modulator are not equal for the heating and cooling processes. The heating time constant is around 50 µs, and the cooling time constant is around 80 to 100 µs. This is because the heater is integrated with the ring modulator so the heat is directly transferred to the device, while the heat accumulated in the device can only be slowly dissipated through all the process layers into the environment during the cooling process. With the 3 mW delivered heater power, the ring modulator can be heated up by around 30 K. With the 0.05 nm/K ring resonator thermal response



(a) Temperature trace



(b) *Thru* port power trace

Figure 4-8: Ring modulator properties when toggling the ring modulator heater on and off every 500µs.

as revealed in Section 2.2.1, the heater efficiency is 0.5 nm/mW around 1300 nm. Previous work in [19] has demonstrated a ring heater efficiency of 0.38 nm/mW in similar manufacturing substrate transfer process.

Figure 4-8b shows the dynamics of resonance shift due to temperature variations. Since we place the laser wavelength out of resonance initially, we can observe the resonance oscillates around the laser wavelength as the *Thru* port power varies. Since the temperature changes more abruptly before one time constant, the resonance shifts toward the laser wavelength more quickly than it moves away from the laser wavelength, which explains the asymmetrical power variation rate at the two side of each lowest power point. Note that, since the laser power is high, ring self-heating plays an important role at the cooling stage as more laser power is going into the ring

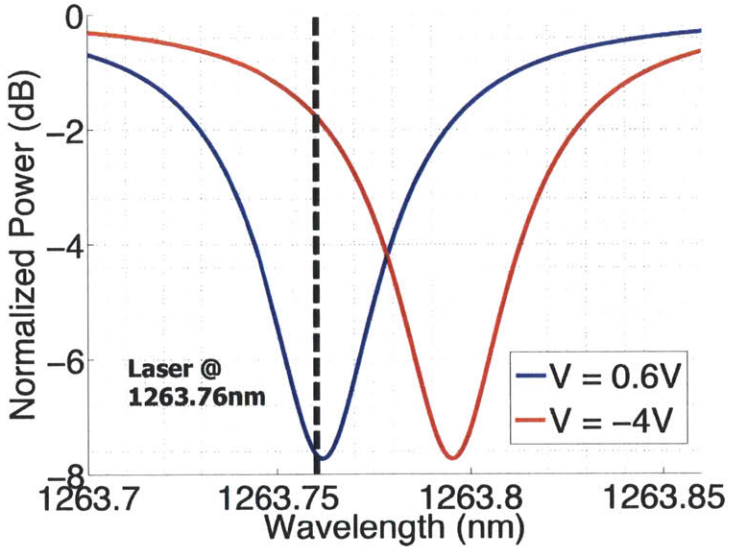


Figure 4-9: The frequency response of the ring modulator at 0.6 V (bit-0) and -4 V (bit-1) driving voltages. The laser wavelength is tuned approximately at the center frequency of the bit-0 resonance.

when resonance shifts. It can be seen that when the *Thru* port power decreases, the temperature cooling process actually slows down around 550 µs and 1600 µs of the simulation.

4.3.2 Optical Modulation with Circuit Thermal Crosstalk

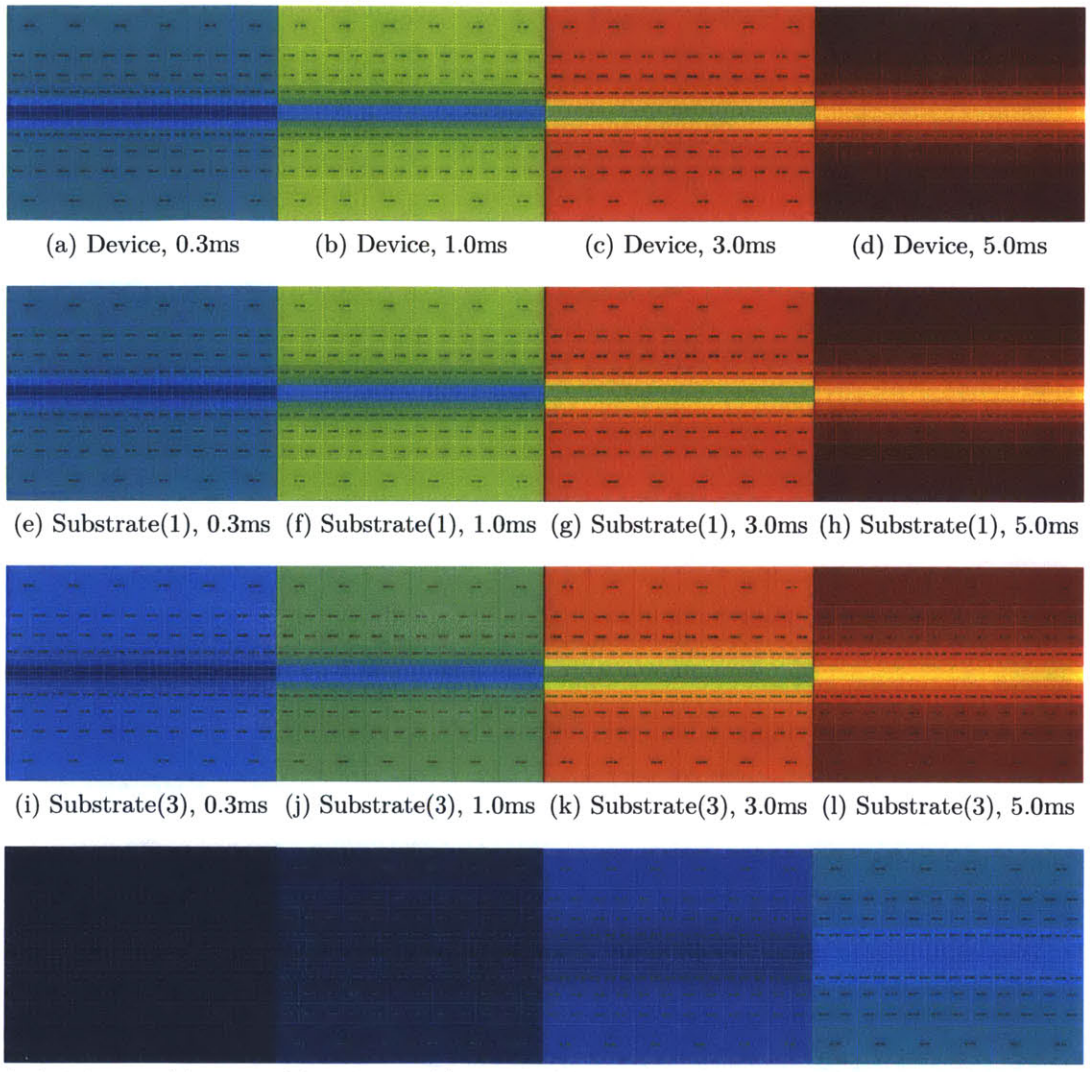
Temperature variations not only affect the DC performance of the ring resonator, but also change the dynamic response when modulating data onto wavelengths. In this section, we will demonstrate the modulation performance of the ring modulator under thermal crosstalk from nearby electrical circuits. With the heater efficiency revealed in Section 4.3.1, we can get an idea of the required bandwidth for the ring thermal-tuning mechanisms.

In this experiment, the heat source is the electrical circuitry, so the heater is turned off throughout the simulation. Each circuit unit in Figure 4-4 is assumed to consume a constant power at 25 mW. We use the same carrier-depletion ring modulator as in Table 2.1, which has a relatively high loaded Q factor to show the modulation response. The driving voltages of the modulator driver for bit zero and

bit one are 0.6 V and -4 V, respectively. The corresponding ring resonances are shown in Fig 4-9. The laser wavelength is tuned approximately at the center frequency of the bit-0 resonance, and the laser power is -10 dBm. Random data sequence is sent to the modulator driver, which controls the ring modulator to imprint data onto the wavelength. The data rate is set to 1 Gb/s.

Figure 4-10 and Figure 4-11 show the temperature color map at different times and layers of the simulation with silicon dioxide substrate and silicon substrate with air undercut, respectively. In the case of silicon dioxide substrate, the optical device section in the middle is always much cooler than the top and bottom sides since only the electrical circuitries are generating heat and silicon dioxide cannot tranfer heat fast. But in the case of silicon substrate with air undercut, there is no clear difference in temperature between electronics and photonics. Since silicon is very conductive thermally, the heat will spread out to the substrate quickly once generated and the whole substrate then is heating up everything above, including the air cavity. Also it can be seen that the heat is gradually spreading down to bottom substrate layers in silicon dioxide substrate, but the temperature is almost the same across vertical layers in silicon substrate. In both cases, the bottom layers have more even temperature distributions than upper layers since the heat spreads out more.

Figure 4-12 shows only the circuit (at the border of the chip) and the ring modulator temperature traces, which describes the relation of the temperature difference due to thermal crosstalk. At the first 1 ms of the simulation with silicon dioxide substrate as shown in Figure 4-12a, most of the heat is still spreading out to the substrate layers, so the circuit temperature rises much faster than the ring modulator temperature. Then, the substrate is heating up both the circuit and optical devices at around the same rate. For silicon substrate with air under as shown in Figure 4-12b, both circuits and ring modulator are heated by the silicon substrate evenly so the temperature rising rates are almost the same. In general, the thermal crosstalk from circuits has a relatively low bandwidth when compared to the heater efficiency and response time constant. Therefore, according to the settings in our simulation,



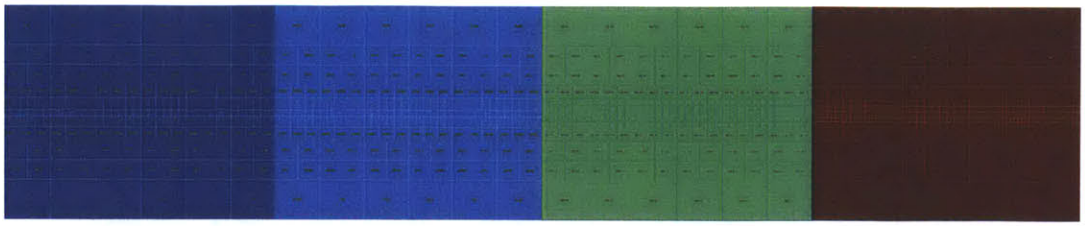
(a) Device, 0.3ms (b) Device, 1.0ms (c) Device, 3.0ms (d) Device, 5.0ms

(e) Substrate(1), 0.3ms (f) Substrate(1), 1.0ms (g) Substrate(1), 3.0ms (h) Substrate(1), 5.0ms

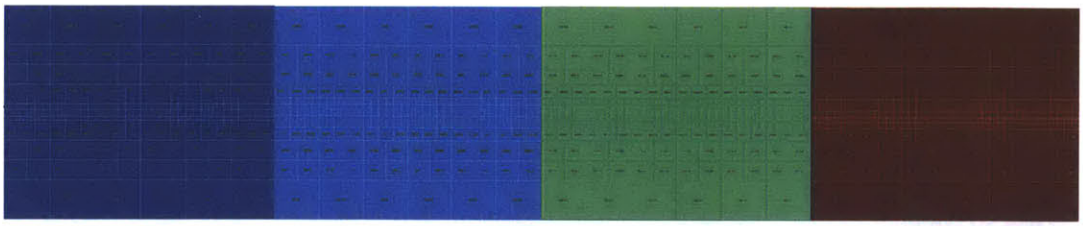
(i) Substrate(3), 0.3ms (j) Substrate(3), 1.0ms (k) Substrate(3), 3.0ms (l) Substrate(3), 5.0ms

(m) Substrate(5), 0.3ms (n) Substrate(5), 1.0ms (o) Substrate(5), 3.0ms (p) Substrate(5), 5.0ms

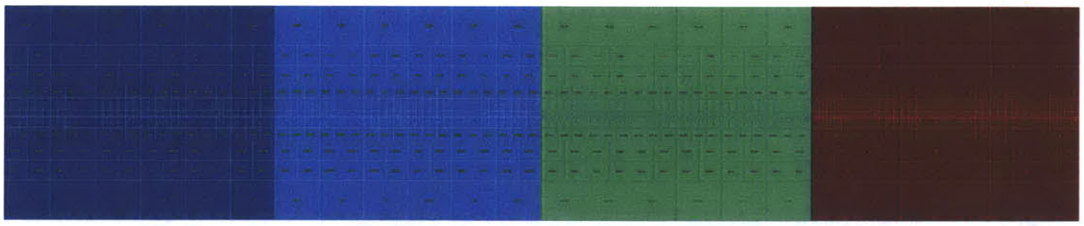
Figure 4-10: The temperature color map of the circuit thermal crosstalk simulation at different times and layers with silicon dioxide substrate.



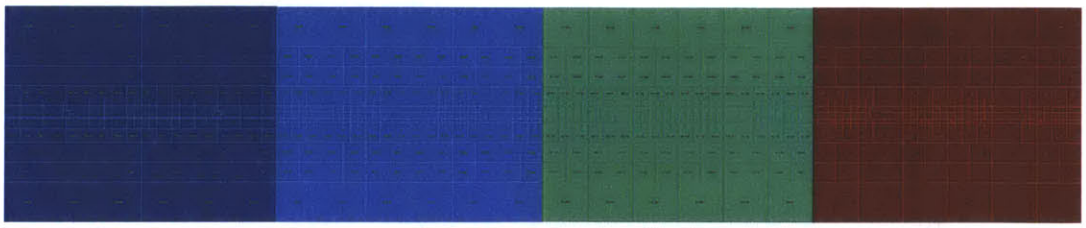
(a) Device, 0.3ms (b) Device, 1.0ms (c) Device, 3.0ms (d) Device, 5.0ms



(e) Substrate(1), 0.3ms (f) Substrate(1), 1.0ms (g) Substrate(1), 3.0ms (h) Substrate(1), 5.0ms

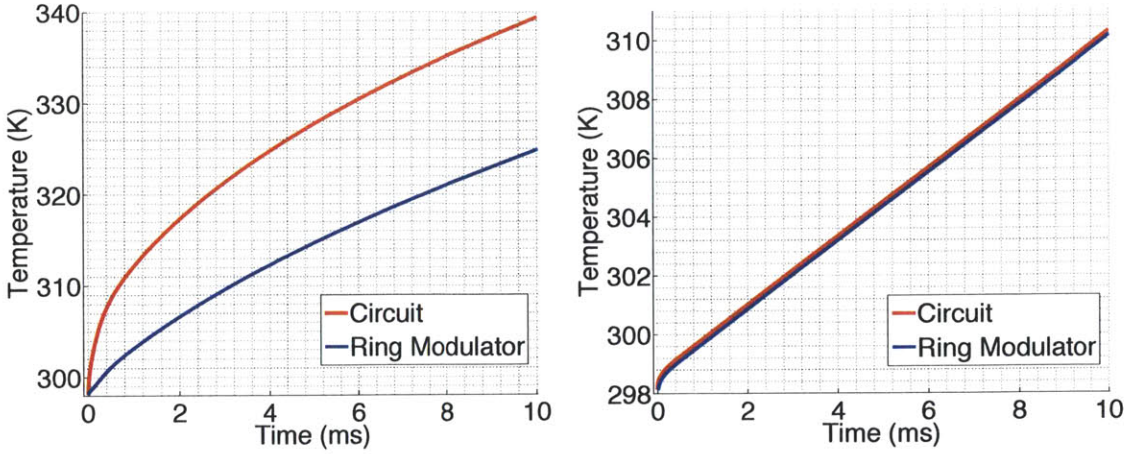


(i) Substrate(3), 0.3ms (j) Substrate(3), 1.0ms (k) Substrate(3), 3.0ms (l) Substrate(3), 5.0ms



(m) Substrate(5), 0.3ms (n) Substrate(5), 1.0ms (o) Substrate(5), 3.0ms (p) Substrate(5), 5.0ms

Figure 4-11: The temperature color map of the circuit thermal crosstalk simulation at different times and layers with silicon substrate with air undercut beneath optical devices.



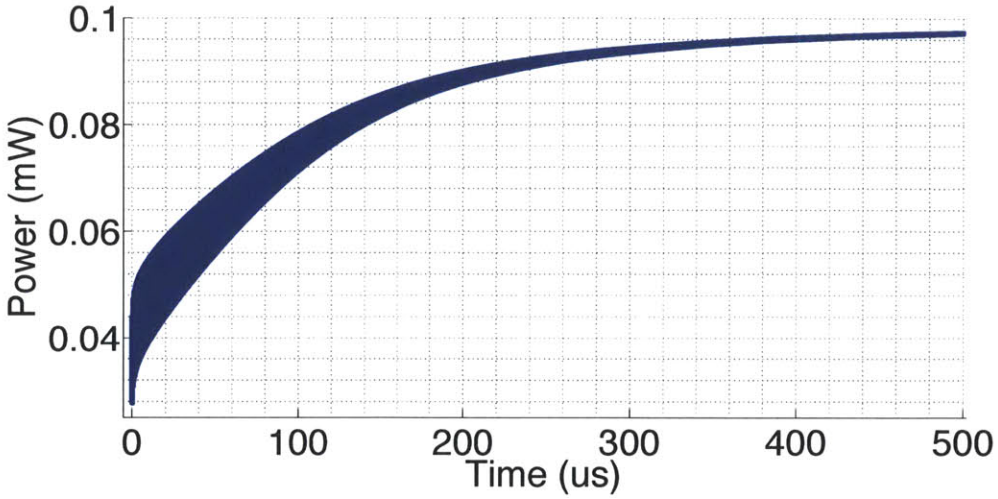
(a) SiO_2 substrate

(b) Si substrate with air undercut

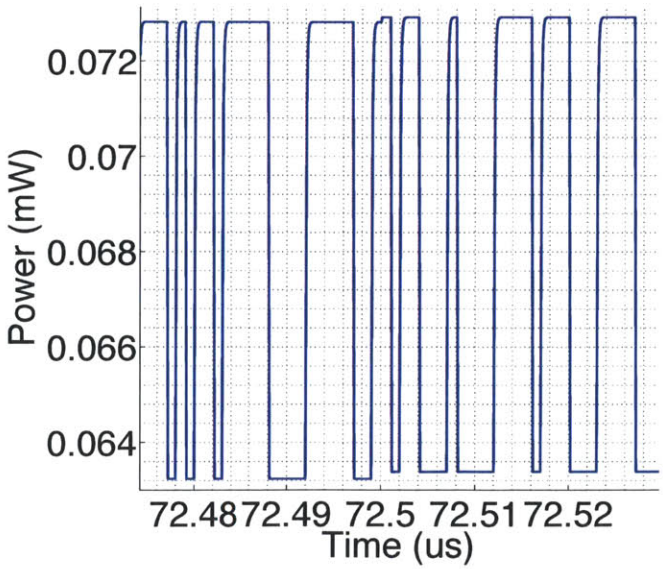
Figure 4-12: Temperature of circuit and ring modulator with circuit thermal crosstalk.

the thermal tuning mechanism should be able to stabilize the ring resonance at high accuracy.

Figure 4-13a shows the modulated wavelength at the *Thru* port of the ring modulator with silicon dioxide substrate, and Figure 4-13b zooms in to see the bit sequence. The extinction ratio of the modulated signal decreases from around 5 dB at the beginning to only 0.03 dB at 500 µs. This is because the bit-0 and bit-1 resonances are both redshifted thermally, so the power levels representing both bits increase but the difference is reduced, as implied by Figure 4-9.



(a) The *Thru* port modulated wavelength



(b) Zoom-in: the modulated random bit sequence

Figure 4-13: The modulated wavelength in thermal crosstalk with SiO_2 substrate. The wavelength is modulated with random bit sequence. Due to circuit thermal crosstalk, the extinction ratio of the modulated wavelength decreases.

Chapter 5

Conclusion

As a disruptive technology, monolithically-integrated optical links have the promising potential to remove the memory bandwidth bottleneck in the deep multi-core regime. This emerging opportunity comes with design challenges from device, architecture and system domains. We demonstrated the important role thermal effects play in the integrated photonics system. In particular, the ring resonator performance has a strong dependence on temperature variations, which requires ring thermal-tuning mechanisms to close of the loop of thermal control. The design of thermal-tuning algorithms relies on the understanding of thermal dynamics within the integrated photonics system, and it creates the need for a thermal analysis platform which can simulate the architectural operation of microprocessor systems, track the real-time system thermal behavior, and relate the temperature information back to the performance of the optical link performance.

In this thesis we present such a thermal simulation platform. It consists of all the three system modeling aspects as described above, including performance model for architectural simulation, physical model for device evaluation, and thermal model for system thermal dynamics analysis. We introduce the compact thermal model to convert the physical chip into a equivalent thermal structure based on system floorplan and manufacturing process, and apply the technique of linear difference-equation based thermal analysis to solve the transient thermal dynamics at scalable temporal and spatial granularities. In addition, with decoupled operating frequencies

for the three models, the simulation can be tuned to run at high efficiency according to the problem scale, which makes system-wide simulation feasible.

We evaluate the thermal dependence of the integrated photonics system from high level architectural operation to physical level device performance. Architectural simulation with real benchmark workloads provides insights into the influences of system functional blocks on the temperature variations of optical devices. The impact of circuit thermal crosstalk on the signal modulation of the optical link is demonstrated. The extinction ratio diminishes very quickly within a few degrees of temperature change, which confirms the need of accurate control on temperature stability of the ring resonators. The manufacturing process should also be considered when designing thermal control logics since the material thermal properties determine the overall heat transfer characteristics of the system. We also show that the integrated ring heater has a higher bandwidth than the crosstalk dynamics due to different heating path. Therefore, the feedback control loop of thermal-tuning will be able to lock the ring resonance with high accuracy, and this will be the future work on the development of a monolithically-integrated electro-optical system.

Appendix A

Source Code

The source code of the thermal simulator can be downloaded from the following link: http://www.mit.edu/~yhchen/ThermalSimulator.zip

Bibliography

[1] JEDEC DDR4 SDRAM interface standard.
`http://www.itrs.net/Links/2012ITRS/2012Tables/Assembly Pkg_2012Tables.xlsx`.

[2] CACTI6.5. Online Website,
`http://www.hpl.hp.com/research/cacti`.

[3] Apple iDevice Memory Bandwidth. Online Website,
`http://www.anandtech.com/show/6472/ipad-4-late-2012-review/3`.

[4] Intel Xeon Phi Coprocessor 5110P. Online Website,
`http://ark.intel.com/products/71992/`
`Intel-Xeon-Phi-Coprocessor-5110P-8GB-1_053-GHz-60-core`.

[5] ITRS assembly & packaging 2012 tables.
`http://www.jedec.org/sites/default/files/docs/JESD79-4.pdf`.

[6] Reja Amatya et al. Low power thermal tuning of second-order microring resonators. *Conf. on Lasers and Electro-Optics*, May 2007.

[7] Chris Batten et al. Building manycore processor-to-dram networks with monolithic silicon photonics. *Int'l Symp. on High-Performance Interconnects*, Aug 2008.

[8] S. Beamer et al. Re-architecting DRAM memory systems with monolithically integrated silicon photonics. *ISCA*, June 2010.

[9] M. Georgas et al. Addressing link-level design tradeoffs for integrated photonic interconnects. *IEEE Custom Integrated Circuits Conference*, pages 1–8, Sep 2011.

[10] W. Huang et al. Hotspot: A compact thermal modeling methodology for early-stage VLSI design. *IEEE Transactions on VLSI Systems*, 14(5):501–513, May 2006.

[11] Ron Keilkowski. *Inside SPICE*. McGraw Hill, 1994.

[12] Lionel Kimerling. Silicon microphotonics. *Applied Surface Science*, 159:8–13, June 2000.

[13] S. Li et al. Mcpat: An integrated power, area, and timing modeling framework for multicore and manycore architectures. *IEEE MICRO*, pages 469–480, Dec 2009.

[14] F. Liu et al. 10gbps, 530fj/b optical transceiver circuits in 40nm CMOS. *Symp. on VLSI Circuits*, pages 290–291, June 2011.

[15] L.-W. Luo et al. Power insensitive silicon microring resonators. *Optics Letters*, 37(4):590–592, Feb 2012.

[16] J. Miller et al. Graphite: A distributed parallel simulator for multicores. *IEEE Int'l Symp. on High Performance Computer Architecture*, pages 1–12, Jan 2010.

[17] B. Moss et al. A 1.23pj/b 2.5gb/s monolithically integrated optical carrier-injection ring modulator and all-digital driver circuit in commercial 45nm SOI. *Int'l Solid-State Circuits Conf.*, pages 126–127, Feb 2013.

[18] Ben R. Moss. High-speed modulation of resonant CMOS photonic modulators in deep-submicron bulk-CMOS. *M.S. Thesis*, Sep 2009.

[19] J. S. Orcutt et al. Open foundry platform for high-performance electronic-photonic integration. *Optics Express*, 20(11):12222–12232, May 2012.

[20] Jason Orcutt et al. Demonstration of an electronic photonic integrated circuit in a commercial scaled bulk CMOS process. *Conf. on Lasers and Electro-Optics*, May 2008.

[21] Jason S. Orcutt et al. Nanophotonic integration in state-of-the-art CMOS foundries. *Optics Express*, 19(3):2335–2346, Jan 2011.

[22] Dac C. Pham et al. Overview of the architecture, circuit design, and physical implementation of a first-generation cell processor. *IEEE Journal of Solid-State Circuits*, 41(1):179–196, Jan 2006.

[23] A. Rylyakov et al. A 3.9ns 8.9mw 4x4 silicon photonic switch hybrid integrated with CMOS driver. *Int'l Solid-State Circuits Conf.*, pages 222–224, Feb 2011.

[24] Jeffrey M. Shainline et al. Depletion-mode carrier plasma optical modulator in zero-change advanced CMOS. *Optics Letters*, 2013.

[25] R. Soref et al. *IEEE Journal of Quantum Electronics*, 23(1):123–129, Jan 1987.

[26] C. Sun et al. DSENT - a tool connecting emerging photonics with electronics for opto-electronic networks-on-chip modeling. *IEEE Int'l Symp. on Networks on Chip*, pages 201–210, May 2012.

[27] C. Sun et al. Integrated microring tuning in deep-trench bulk CMOS. In *IEEE Optical Interconnect Conference*, May 2013.

[28] E. Timurdogan et al. Automated wavelength recovery for microring resonators. *Conf. on Lasers and Electro-Optics*, 2012.

[29] M. R. Watts et al. Adiabatic resonant microrings (ARMs) with directly integrated thermal microphotonics. *Conf. on Lasers and Electro-Optics*, 2012.

[30] Qianfan Xu et al. 12.5 Gbit/s carrier-injection-based silicon micro-ring silicon modulators. *Optical Society of America*, 15(2), Jan 2007.

[31] I. Young et al. Optical I/O technology for tera-scale computing. *Int'l Solid-State Circuits Conf.*, pages 468–469, Feb 2009.