Energy Efficient Control for Power Management Circuits operating from nano-watts to watts

by

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Abstract

Energy efficiency and form factor are the key driving forces in today's power electronics. All power delivery circuits, irrespective of the magnitude of power, basically consists of power trains, gate drivers and control circuits. Although the control circuits are primarily required for regulation, these circuits can play a crucial role in achieving high efficiency and/or minimizing overall system form-factor. In this thesis, power converter circuits, spanning a wide operating range- from nano-watts to watts, are presented while highlighting techniques for using digital control circuits not just for regulation but also to achieve high system efficiency and smaller system form-factor.

The first part of the thesis presents a power management unit of an autonomous wireless sensor that sustains itself by harvesting energy from the endo-cochlear potential (EP), the 70-100mV electrochemical potential inside the mammalian inner ear. Due to the anatomical constraints, the total extractable power from the EP is limited to 1.1-6.3nW. A low switching frequency boost converter is employed to increase the input voltage to a higher voltage usable by CMOS circuits in the sensor. Ultra-low power digital control circuits with timers help keep the quiescent power of the power management unit down to 544pW. Further, a charge-pump is used to implement leakage reduction techniques in the sensor. This work demonstrates how digital low power control circuit design can help improve converter efficiency and ensure system sustainability. All circuits have been implemented on a 0.18μm CMOS process.

The second part of the thesis discusses an energy harvesting architecture that combines energy from multiple energy harvesting sources- photovoltaic, thermoelectric and piezoelectric sources. Digital control circuits that configure the power trains to new efficient system architectures with maximum power point tracking are presented, while using a single inductor to combine energy from the aforementioned energy sources all at the same time. A dual-path architecture for energy harvesting systems is proposed. This provides a peak efficiency improvement of 11-13% over the

traditional two stage approach. The system can handle input voltages from 20mV to 5V and is also capable of extracting maximum power from individual harvesters all at the same time utilizing a single inductor. A proposed completely digital time-based power monitor is used for achieving maximum power point tracking for the photovoltaic harvester. This has a peak tracking efficiency of 96%. The peak efficiencies achieved with inductor sharing are 83%, 58% and 79% for photovoltaic boost, thermoelectric boost and piezoelectric buck-boost converters respectively. The switch matrix and the control circuits are implemented on a 0.35μm CMOS process. This part of the thesis highlights how digital control circuits can help reconfigure power converter architectures for improving efficiency and reducing form-factors.

The last part of the thesis deals with a power management system for an offline 22W LED driver. In order to reduce the system form factor, Gallium Nitride (GaN) transistors capable of high frequency switching have been utilized with a Quasi-Resonant Inverted Buck architecture. A burst mode digital controller has been used to perform dimming control and power factor correction (PFC) for the LED driver. The custom controller and driver IC was implemented in a 0.35μm CMOS process. The LED driver achieves a peak efficiency of 90.6% and a 0.96 power factor. Due to the high power level of the driver, the digital controller is primarily used for regulation purposes in this system, although the digital nature of the controller helps remove the passives that would be normally present in analog controllers.

In this thesis, apart from regulation, control circuit enabled techniques have been used to improve efficiency and reduce system form factor. Low power design and control for reconfigurable power train architectures help improve the overall power converter efficiency. Digital control circuits have been used to reduce the form factor by enabling inductor sharing in a system with multiple power converters or by removing the compensator passives.

Thesis Supervisor: Anantha P. Chandrakasan
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Chapter 1

Introduction

With the ever growing energy demands, the focus towards efficient energy conversion systems has been increasing. Whether it is for wireless sensor nodes, hand-held battery operated portable devices, consumer electronics, the lighting industry or high performance computing and mission critical applications, high efficiency and small form factor power converters are required by all conceivable electronics around us. High efficiency translates to lower cost, better reliability and increased lifetime.

Low power electronics has enabled us to design wireless sensors and low power implantable electronics that work off minuscule amounts of energy harvested from the ambient energy (light, heat differentials, vibrations, RF, etc). These systems can be used in applications that require sensing (or actuation) along with communication with a central base station that may not be energy constrained. For these devices, the cost of replacing the battery may be too high thus, making energy harvesting a viable solution. The main challenge in such converters is maintaining high efficiencies even for low power levels since the harvested power is in the nW to 100's of μW range [1].

In the portable devices regime, recent advances in battery technology [2, 3] have led to higher battery capacities. However, with the mobile revolution, higher integration and increasing functionalities have made it necessary for designers to adopt low power design techniques like dynamic voltage-frequency scaling, parallelism, clock

and power gating [4–6]. It must be noted that the efficacy of dynamic voltage scaling relies heavily on the DC-DC converters that have to provide power to the load circuits with a fast loop response [7]. Further, the DC-DC converters powered by batteries for portable applications need to handle a wide load range efficiently [8] thereby, making the power management circuit and control design extremely critical.

The consumer electronics space has seen a significant increase in power consumption in the last decade. In 2010, the consumer electronics in the US used an estimated 193TWh, 5.1% of the overall annual US energy consumption [9]. A total of 700TWh has been used for lighting by the US in 2010. This accounts for close to 19% of the US annual energy usage [10]. Further, data centers consume significant energy (estimated to be close to 230TWh worldwide in 2010 [11]), 30-40% of which is typically lost in the infrastructure (cooling, power distribution, transformer losses, etc.) required for the computing equipment [12, 13]. These losses would be reduced if power is delivered efficiently to the data center electronics. Therefore, there is a growing need for efficient power conversion circuits. Often, depending on the specific application, these power converters may have volume/weight constraints limiting the size of the passives that can be used. This requires high switching frequencies which adversely effects the converter efficiency. Emerging technologies like Gallium Nitride (GaN) and Silicon Carbide (SiC) [14] made it possible to have high efficiency converters with small form factors. However power converter topologies and associated control schemes still need to be selected appropriately to meet the requirements and recommendations (efficiency, volume, power factor, EMI, etc.) laid out by regulatory bodies like Energy Star [15], CEA [16], FCC [17], etc.

1.1 Generalized Power Converter Architecture

Figure 1-1 shows a general power converter architecture consisting of a power train with rectifiers, switches, filter passives and sensors along with control circuits that are required for regulation purposes. Today, significant research is directed towards

making the power trains more efficient at high switching frequencies. GaN and SiC switches have provided efficiency improvements over conventional Silicon transistors for high voltage (>40V) power converters. For voltages below 40V, Gallium Arsenide (GaAs) FETs [18] have proven effective although not always cost effective. For low voltage designs, CMOS scaling [19] has made Silicon transistors better, faster and cost effective for voltage conversion in this design space. SiC diodes [20] have also helped the cause for high frequency converters with practically no recovery losses. Significant developments have also taken place in low loss, high frequency inductors [21, 22].

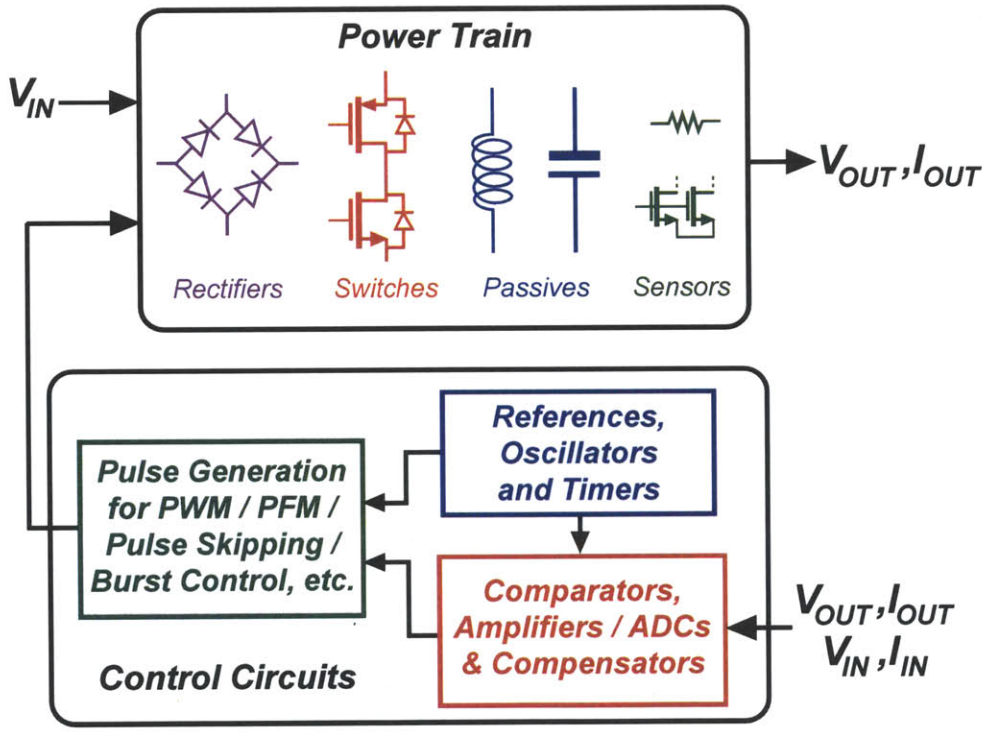


Figure 1-1: Generalized Power Converter Architecture

The primary function of the control circuits is regulation. Depending on the application, this may be for voltages or currents, input or output [23]. Most controllers consist of basic circuits like comparators, amplifiers, compensators, references, oscillators/timers and pulse generation circuits. The comparator (digital comparators along with ADCs for multi-bit digital controller implementations) compares the sensed electrical parameter that needs to be regulated with a reference. In certain

systems, the regulation may incorporate the load demands into the feedback loop [24] thereby varying the reference depending on the load. The comparator generates an error (or difference) signal which, depending on the control strategy, might need further processing by compensation circuits to meet the application's transient and loop bandwidth requirements. Pulse generation circuits utilize the output of the comparators or compensators (depending on the control scheme) to create appropriate pulses that are required by the power train for power conversion. The nature of the pulses depends on the control scheme used. Popularly used control schemes include Pulse Width Modulation (PWM), Pulse Frequency Modulation (PFM), Pulse Skipping and Burst Control.

1.2 Thesis Motivation

Due to the ubiquitous power processing by all conceivable electronics around us as described earlier, power converters need to be designed as efficient and miniaturized as possible. Traditionally, high efficiency and small form factors have been achieved by optimizing the power train with superior semiconductor components and magnetics [14, 18, 20–22]. However, the role of control circuits in achieving high efficiency and small form factors still needs to be studied while considering power converters covering a wide power range. In this thesis, control circuits for improving system efficiency and reduction of system form factor while providing the desired regulation have been discussed. For low power converters, the power overhead of the control circuits can become a significant fraction of the overall power budget limiting the system efficiency. By using low power design techniques in control circuits, it is possible to maximize the system efficiency. Further, it is also possible to use control circuits to re-architect the power train into efficient architectures thereby maximizing the system efficiency. Additionally, control circuits can also reduce the system form factor by sharing inductors between different converters in a multi-input, multi-output power conversion scenario. By using digital control it is possible to completely remove the

compensator passives that are otherwise present in analog controllers.

1.3 Thesis Organization

This thesis explores these aspects over a wide range of power levels- from nano-watts to watts. The thesis is organized as follows:-

Chapter- 2

Previous works showing the importance of control circuits for increasing system efficiency, reducing system form factor or providing improved regulation have been reviewed. Techniques for adaptive FET sizing, inductor sharing, inductor biasing and integrated digital controllers have been discussed.

Chapter- 3

An energy harvesting system for ultra-low power implants has been demonstrated. The system uses the endo-cochlear potential (EP), a 70-100mV biologically stabilized potential that exists in the inner ear of all mammals. Due to the anatomical constraints, a maximum of 1.1 to 6.3nW can be extracted from this *biological battery*. The power budget of this system is orders of magnitude less that conventional energy harvesting systems. In order to successfully extract energy from this bio-potential to sustain the sensor, the control overhead must be lower that the total energy extracted by the power converter. Ultra-low power digital control circuits operating in pico-watts along with leakage reduction circuits, ultra-low power timers and power gating circuits that are commonly used in digital circuits have been used for this purpose. The entire control consumes 544pW. This work demonstrates how low power control circuits are critical for the overall power converter efficiency (ratio of usable power to harvested power) and hence system sustainability in this case.

Chapter- 4

An energy harvesting system has been discussed that combines energy from

multiple energy harvesting sources- photovoltaic, thermoelectric and piezoelectric sources to increase overall system reliability. Digital control circuits that configure the power trains to a new efficient energy harvesting system architecture (peak improvement of 13%) with a digital time-based maximum power point tracking scheme are presented. This is done while using a single inductor to combine energy from the multiple energy sources all at the same time. An implementation without inductor sharing with the same functionalities would use at least 3 additional inductors. In this work, we demonstrate how control circuits can be used to increase system efficiency and reduce system form-factor by sharing inductors between multiple converters.

Chapter- 5

The power conversion circuits for an offline LED driver are presented. In order to reduce the system form factor, Gallium Nitride (GaN) transistors capable of high frequency switching has been utilized for a Quasi-Resonant inverted buck LED driver with 90.6% peak efficiency. A burst mode controller has been used to perform dimming control and power factor correction (PFC). This work demonstrates how control circuits have been used for controlling the LED light intensity and providing PFC. A peak PFC of 0.96 is obtained. Further, since the controller is digital in nature, it does not require any additional passives that are usually required by analog controllers.

Chapter 2

Previous work in control circuits for maximizing efficiency, minimizing form factor and improving regulation

Efficiency and form factor are of key concern in designing power converters. Moreover, to ensure reliable power delivery, the converter needs to meet the system's regulation requirements. In this chapter, previously reported techniques used in control circuits have been presented for maximizing efficiency, reducing form factor and improving regulation. The discussion is divided into three sections, each section highlighting the aspect that needs to be improved and how the control circuits have been used to do so.

2.1 Maximizing System Efficiency

In order to maximize the overall system efficiency, the power trains (FETs and passives), gate drivers and control circuits need to be appropriately designed. In most

cases, the system efficiency is dictated by the power FETs and the passives. However, in low power converters, the control circuit power consumption also needs to be looked at for optimizing the overall efficiency. This section will be discussing techniques that use control circuits to minimize both the power dissipation in both the power train and the control circuits thereby maximizing system efficiency.

2.1.1 Adaptive FET Size

For power converters delivering 100's of mW and higher, the system efficiency is usually dictated by power trains as the control power overhead is much smaller as compared to the delivered power. The optimization strategy involves designing or selecting FETs and passives to maximize the efficiency for a given load condition. However, this often leads to the converter being optimal for a set of load conditions and being sub-optimal for other conditions. Previous works [25–27] propose adaptive power train architectures with integrated FETs that re-size themselves depending on the loading conditions. In order to understand the benefit of this scheme, lets consider a simplified DC-DC Buck converter in the PWM mode as shown in Figure 2-1.

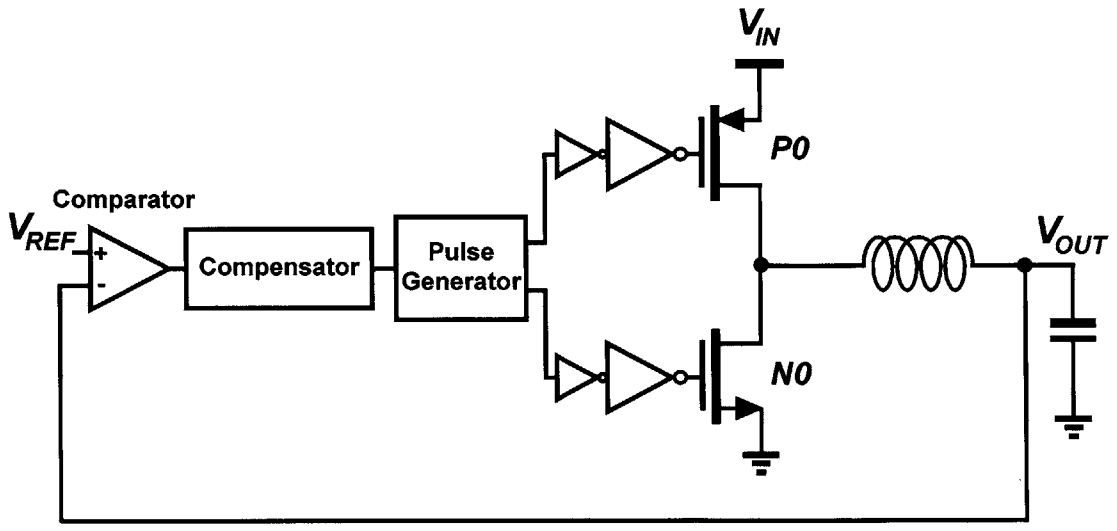


Figure 2-1: DC-DC Converter in the PWM mode

The power FETs *P0* and *N0* are sized depending on the output load. First, lets consider the power losses due to *N0*. Eq. 2.1 gives the general expression for the loss due to *N0* where $E_{G,N0}$ is the energy required to turn on the gate of *N0*, E_{G0} is the energy per unit width of *N0*, f_s is the switching frequency of the buck converter, $I_{N0,rms}$ is the rms current through *N0*, R_{N0} is the *N0* on-resistance and R_0 is the resistance per unit width of *N0*. Further, Figure 2-2(a) shows typical plots of conduction and switching losses for different FET sizes given the load.

$$\begin{aligned} \textit{Power Loss} &= \textit{Switching Loss} + \textit{Conduction Loss} \\ &= E_{G,N0} \cdot f_s + I_{N0,rms}^2 \cdot R_{N0} \\ &= E_{G0} \cdot W_{N0} \cdot f_s + I_{N0,rms}^2 \cdot \frac{R_0}{W_{N0}} \end{aligned} \tag{2.1}$$

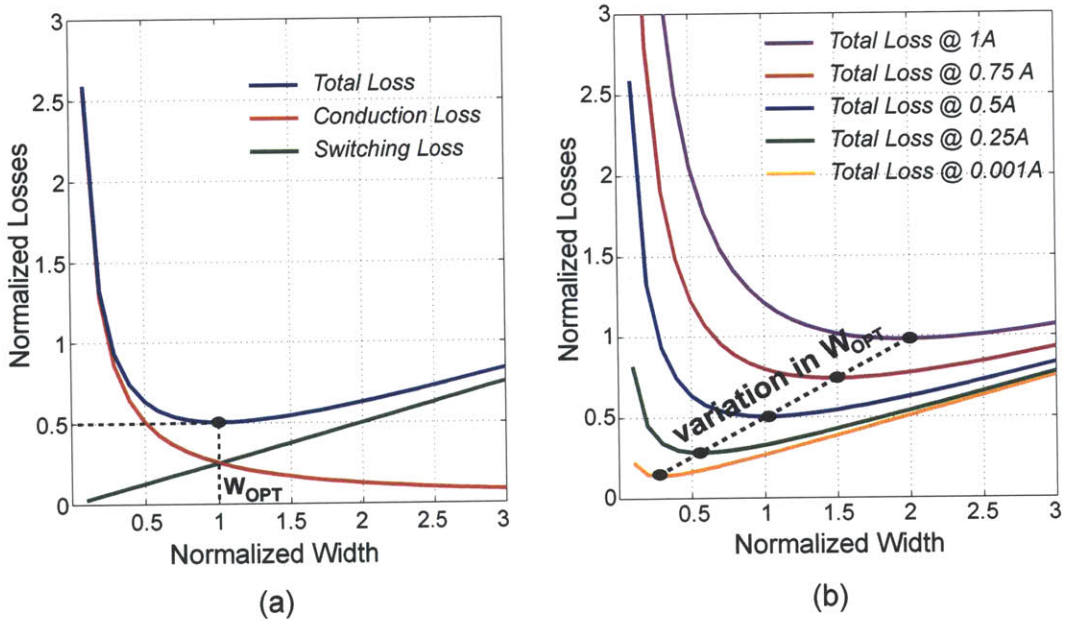


Figure 2-2: Optimizing FET size to minimize Losses

The optimal width of *N0* is obtained by minimizing Eq. 2.1 and is given by Eq. 2.2. The corresponding minimum loss is expressed by Eq. 2.3. It must be noted that Eq. 2.2 and Eq. 2.3 depend on the rms current ($I_{N0,rms}$), switching frequency (f_s), FET resistance per unit width (R_0) and FET capacitance per unit width as

the energy required to turn on the FET (E_{G0}) is directly proportional to the gate capacitance, including the capacitance due to miller effect. Figure 2-2(b) graphically shows the total losses for different load currents (therefore different rms current). A similar analysis can be done for *P0*.

$$W_{N0,opt} = I_{N0,rms} \cdot \sqrt{\frac{R_0}{E_{G0} \cdot f_s}} \tag{2.2}$$

$$Minimum\ Power\ Loss = 2 \cdot I_{N0,rms} \cdot \sqrt{R_0 \cdot E_{G0} \cdot f_s} \tag{2.3}$$

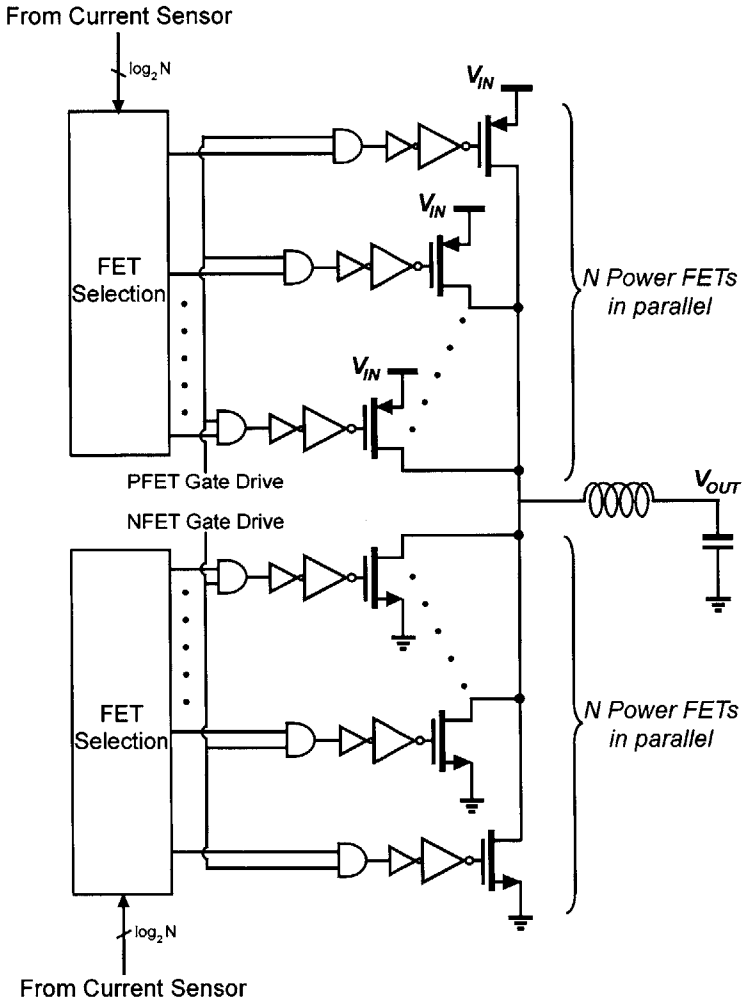


Figure 2-3: Power Train with Adaptive FET Width [25–27]

Keeping the switching frequency and technology constant, we can see that the optimal FET width varies with the load (and the rms current). Figure 2-3 shows the power train implementation with adaptive FET widths. By using control circuits, it is possible to implement current mirrors that sense the current and digitize the estimate to optimize the width of the power FETs [26, 27] dynamically. This ensures that the FET size is always close to the optimal width even for variable loads. Therefore, control circuits can help achieve efficiencies that are relatively constant with loading conditions.

2.1.2 Low Power Digital Controller Design

In low power converters (delivering μW to 10's of mW), the control circuit power overhead may become a significant fraction of the overall power budget. This causes a degradation in the overall system efficiency. Developments in IC processing have enabled the integration of all the control circuits into a single IC making it possible to implement complex digital compensators and pulse generators operating at low voltages with low power consumption [8, 23, 28–31]. Design philosophies like power gating that are usually used in digital design are also used in some of these controllers [8] thereby making the controllers capable of operating with low quiescent power. These design techniques helps maximize the overall system efficiency by lowering the control power overhead.

2.2 Minimizing Form Factor

A power converter's volume is often as important as its efficiency when it comes to deciding between different converter designs. The volume is dictated by the passives and the semiconductor devices. By switching at high frequencies, it is possible to reduce the size of passive components in the power train. However, increased switching frequencies are accompanied by increased losses (core and ac winding) in the

inductors and increased losses due to the power FETs. Both these losses are limited by the technology (properties of the magnetic material used and the FET's figure of merit- $Q_G.R_{ds,on}$) thereby, limiting the switching frequency of the converter. Further, for load circuits with high dI/dt, the output capacitor needs to be sized more for the instantaneous droops during load transients instead of the steady state current ripple [32]. Moreover, for analog controllers, the number of passive components in the compensator further increases the form factor. In this section, a few techniques using control circuits will be highlighted that can lead to reduction in the size of passives both in the power train and in the controller.

2.2.1 Inductor Sharing

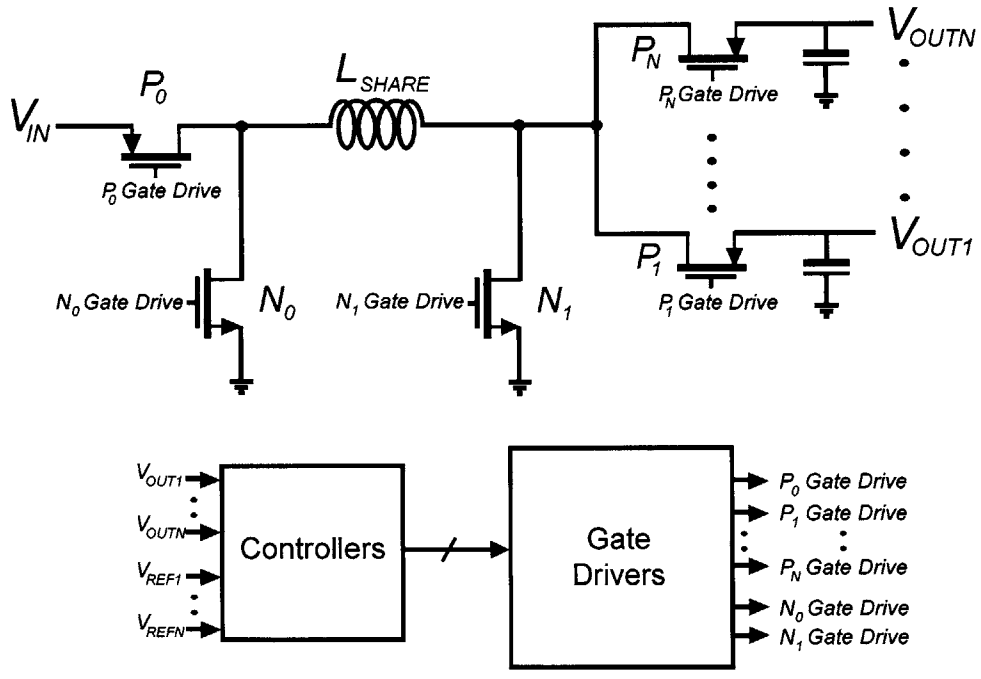


Figure 2-4: Switch Matrix with Single Inductor [33–37, 87]

In systems with multiple power converters (multi-core processors, PMIC units for mobiles and tablets, sensor nodes with energy harvesting, etc.), there is significant interest now in sharing a single inductor between different converters [33–37, 87]. This

reduces the overall system form factor and cost. For such systems, the power trains are implemented as switch matrices with a single inductor as shown in Figure 2-4. The control circuits enable the appropriate switches to configure the power train to the desired converter utilizing a single inductor. This scheme, although reduces the system form factor, comes at the cost of increased losses (due to the additional switches in the power train) and cross-regulation.

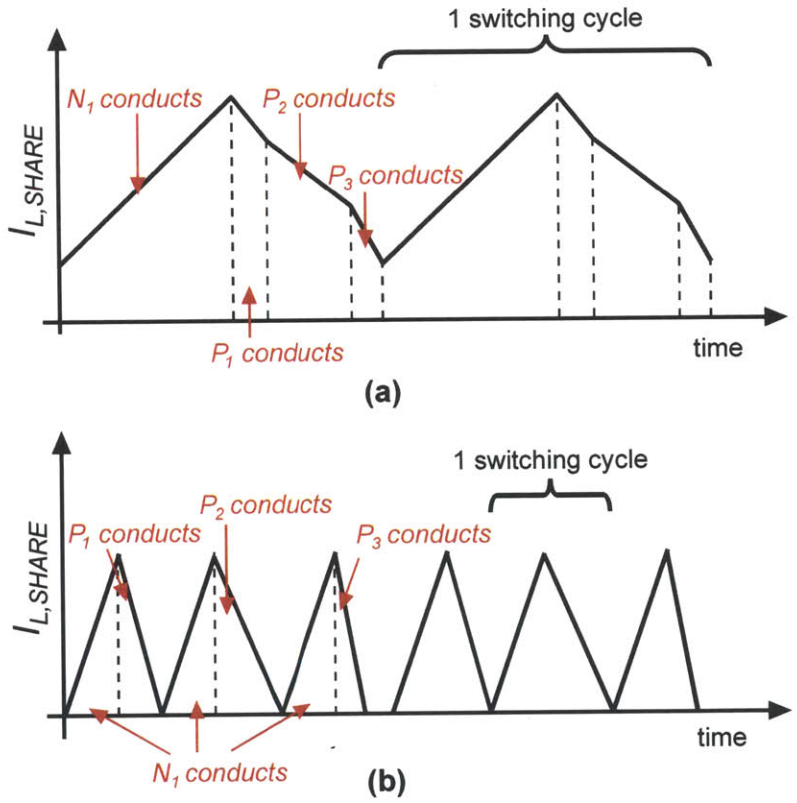


Figure 2-5: Inductor Current during Inductor Sharing:- (a) Current flows to all outputs during a single switching cycle [33–36], (b) Current flows to only one output during a single switching cycle [37, 87]

The main challenge in inductor sharing lies in controlling the multiple outputs of the converters. Since different outputs can have different requirements, the control circuits need to provide adequate power to all the outputs based on their individual load demands. There are two types of control techniques that have been reported in literature for multi-output converters. For the first type, the controller is capable

of enabling the power train such that multiple outputs can get powered during the same switching cycle [33–36] (Figure 2-5(a)). On the other hand, for the second type, power is transferred to only one output during a switching cycle [37, 87] (Figure 2-5(b)). In order to understand these two schemes, lets assume for now the switch matrix shown in Figure 2-4 is always configured in the boost mode. Therefore, P_0 is always enabled and N_0 is always disabled. Let's assume that we have three outputs- V_{OUT1}, V_{OUT2} and V_{OUT3}. For the first type of controller where all the outputs can be powered in a single switching cycle, the converters can work in both CCM and DCM. During a single switching cycle, first N_1 is turned on energizing the shared inductor, L_{SHARE}. Therefore, the slope of the inductor current is proportional to V_{IN}/L. While de-energizing it, the outputs (V_{OUT1} through V_{OUT3}) are turned on one by one. The inductor current slopes are therefore, $(V_{IN} - V_{OUT1})/L$, $(V_{IN} - V_{OUT2})/L$ and $(V_{IN} - V_{OUT3})/L$ during the de-energizing phase as can be seen from Figure 2-5(a). The individual duty cycles (or pulse widths) for switches N_1, P_1, P_2 and P_3 can be either determined by using a bang-bang voltage feedback for all but one output on which current mode feedback is performed [33]. Another method has been proposed for a buck converter in [34] where by using a set of independent control loops constructed from independent error equations, the duty cycles to the individual switches can be estimated. The work in [35] uses a similar bang-bang feedback technique as in [33] however, with a PLL to make the switching frequency constant.

For the second type of multi-output controllers, as shown in Figure 2-5(b), multiple switching cycles are required by converters to deliver power to all the outputs. For the boost converter example considered before, the corresponding strategy for this type of control scheme is to energize and de-energize the inductor for powering each output. Therefore, complete cycles are used by the individual outputs. The order in which the outputs receive power is either selected based on a time-multiplexed assignment [37] or on an arbiter with pre-assigned priorities [87]. The frequency and the individual pulse widths (or duty cycles) must be selected such that all the outputs can be adequately powered. This technique has shown to have better cross regulation performance since the currents to the outputs are independent of each other (when

the converter is operated within the specifications of the design). However, it suffers from slow response time and high losses due to increased switching and higher rms currents.

2.2.2 Inductor Core Bias

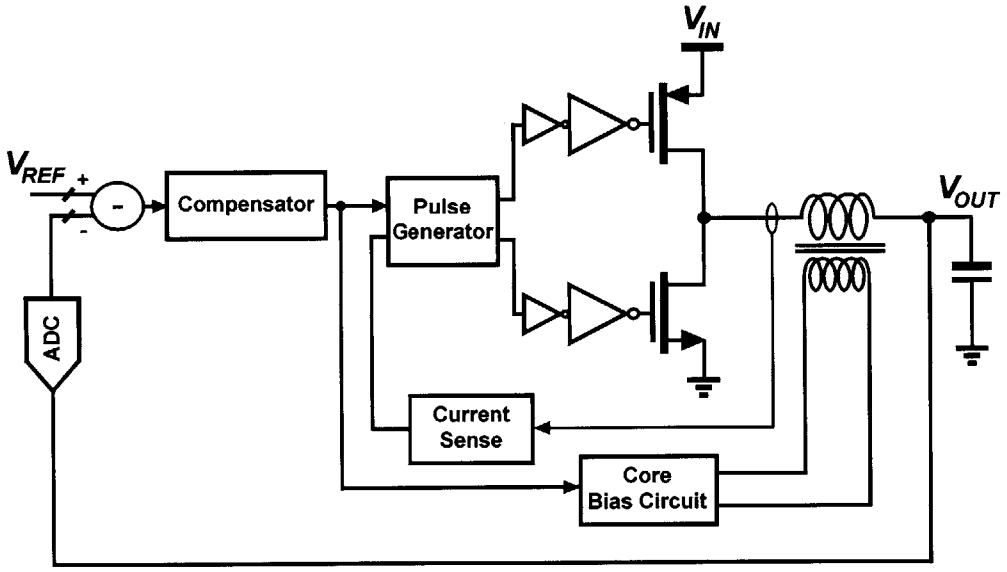


Figure 2-6: Current Mode Buck Converter with Core Biasing

By biasing the inductor core appropriately, it is possible to reduce the size of the converter's passives components [38]. In order to understand this technique, lets look at a buck converter having current-mode feedback. During a load transient, the time taken for the output voltage to settle depends on the dynamics of the feedback loop. However, a smaller inductance causes fast response time causing the converter's current to match the load quicker as compared to a larger inductor. Since the loop is required to control the inductor current in a current-mode controller, in [38] a Core Bias Circuit (Figure 2-6) has been employed that helps to change the inductance dynamically depending on the load. For this purpose, an additional winding is added to the core with more turns that the buck converter inductor. This makes it possible to bias the core with a small current from the Core Bias Circuit. The effectiveness of

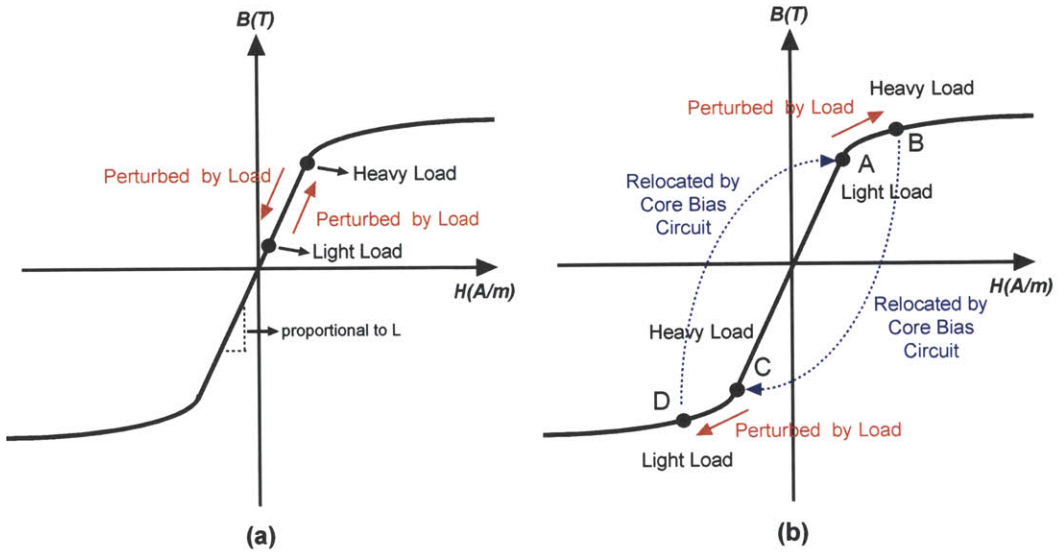


Figure 2-7: B-H Curves: (a) without Core Bias (traditional approach), (b) with Core Biasing Scheme [38]

the technique can be understood from Figure 2-7. In buck converter designs, while deciding the inductor size, the maximum current needs to be considered to prevent core saturation. Therefore, the inductor is primarily sized (core size) to support the maximum load of the converter. Figure 2-7(a) shows a typical B-H curve with its bias point varying depending on the load condition. However, the work in [38] proposes to bias the core at point A (Figure 2-7(b)) during light loads. A light to heavy transient is going to push the inductor to saturation causing the inductance to decrease (point B in Figure 2-7(b)). This causes the control loop to recover quickly. After the transient, the Core Bias Circuit biases the inductor at point C, a high inductance regime in the B-H curve to minimize the current ripple. However, the other specifically of this bias point is its proximity to the core saturation region. During a heavy to light transient, the load pushes the inductor in saturation to point D again saturating the core and decreasing the inductance. After the transient, the Core Bias Circuit again biases the core to point A. In order to see the advantages of this technique in terms of volume reduction, first we must note that the core biasing scheme requires a lower output capacitor to handle the load transients due to the fast transient response. The second

benefit comes from the fact that the inductor now needs to be sized to handle light loads as opposed to the traditional approach where the inductor is sized to handle the converter's peak current. For the implementation described in [38], a 40% reduction is obtained in inductor volume.

2.2.3 Fully Integrated Digital Compensators

Traditionally, due to the analog nature of the controllers used, passives were extensively used in the converters' compensators [40]. However, with digital controllers gaining popularity, there is a shift towards integration. Therefore, by implementing digital controllers it is possible to reduce the number of passive components and hence minimize the overall system form factor. However, digital controllers do more than minimize the form factor- the regulation aspect will be discussed in detail in the next section.

2.3 Improving Regulation

Power converters are required to supply power to the output efficiently along with some form of regulation. Depending on the system, the converter may be required to regulate the output voltage (e.g. in Point-of-Load converters for microprocessors [23, 39], etc.), output current (LED drivers [106]), input voltage or input current (maximum power point tracking systems [89–91]) or a combination (output voltage with control over the input current for grid connected systems employing PFC [45,97] or in battery chargers where depending on the state of charge, output current or the output voltage need to be controlled [41]). The control mechanism in all these converters may be voltage mode or current mode with compensators (Type-I, Type-II or Type-III) [40].

With advances in IC processing, digital controllers [23, 28–31] have gained in popularity. As discussed before, low power consumption, better integration and im-

Figure 2-8: Block Diagram of a Digital Controller with ADC, Compensator and Digital Pulse Modulator [23]

munity to noise and variations have made ideal candidates for high performance converters. Further, digital controllers designed using FPGAs or micro-controllers offer us the flexibility to easily change the design during prototyping. The basic block diagram of a typical digital controller regulating (in voltage mode) a converter's output voltage has been shown in Figure 2-8. The current mode counterpart requires another current ADC as discussed in [42]. For the controller in Figure 2-8, in order to function without limit cycles, the resolution of the Digital Pulse Width Modulator must be finner than the resolution of the ADC sensing the output voltage [30]. A compensator can be implemented as a digital filter although, a digital look-up table based fast compensator has also been proposed in [31]. Extensions to these techniques have been proposed with more complicated functions like predictive fats compensators [43] and time-optimal compensators [44] that ensure fast recovery after a transient. Further, digital control schemes that require additional informations from sensors in the system [26] can be implemented. These digital controllers are now being used extensively in Point-of-Load (POL) converters [23], PFC converters [45], isolated power supplies [23] and converters for maximum power point tracking in PV systems [91].

2.4 Conclusions

In this chapter, previously reported techniques to improve a power converter design using control circuits have been discussed. Table 2.1 summarizes these techniques.

Table 2.1: Summary of control circuit techniques for improving efficiency, form factor and regulation

References	Contributions	Impact
[25–27]	Adaptable FET sizing depending on the loading condition. Systems may perform load sensing or may depend on the load to convey the load current information	Improves efficiency over wide load range. Typically used in applications delivering 10's of mW to a few watts, although can be used for higher power levels
[33–37, 87]	Sharing inductors in a multi-input, multi-output power conversion system	Reduction in form factor, can be widely used for low power (Below 10's of mW) or POL applications
[38]	Adaptive inductor core biasing	Reduction in form factor, can be widely used for POL applications
[8, 23, 28–31, 42–45]	Integrated digital controllers	Below 10's of mW- improvement in efficiency. Above 10's of mW- improved regulation due to advanced digital control and reduction in form factor due to absence of compensators' passives

This thesis builds up on some of the techniques presented in this chapter. The role of control circuits in converters operating over a wide power range- from nano-watts to watts has been discussed. In chapter 3, a power converter with nano-watt power budget has been discussed. In addition to the digital low power design techniques discussed in this chapter, leakage reduction techniques have been highlighted to show how control circuits can help increase system efficiency. The power converter operates with quiescent power in pico-watts which is enabled by low power digital control techniques. As seen in this chapter, control circuits can help improve the efficiency by adaptively reconfiguring the power FET widths depending on the load. A similar technique of reconfiguring the power train dynamically depending in the load has

been proposed in chapter 4. A digital control scheme enabling reconfigurable power train architectures in energy harvesting systems has been presented that reduces the effective number of power stages between the harvester and the load depending on the load and energy harvester condition. This improves the overall system efficiency. Additionally, digital control enabling form factor reduction by inductor sharing has been discussed. Chapter 5 presents a digital controller for an LED driver which is primarily used for regulation purposes (PFC and dimming) due to the higher power budget of the power converter as compared to the converters presented in chapters 3 and 4. However, the digital nature of the control circuits makes it possible to remove the compensator passives that are otherwise present in analog controllers.

Chapter 3

Energy Harvesting from a Bio-Potential for Next Generation Implants

Biomedical implantable electronics have been in existence for sometime now. Pacemakers and cochlear implants [46] are a few examples of implantable electronics that are being extensively used today. Further, implantable electronic devices like retinal implants and intracranial pressure sensors are in the development phase [46]. Moreover, a wide range of implants are now being envisioned for sensing and *in-vivo* drug delivery [47]. Typically, most of these implants are powered by batteries that either need periodic replacement or need to be charged by wireless means [48]. However, there are stringent restrictions on the battery electrolytes' containments and on tissue heating [48] in these implants. Therefore, energy autonomy is a key concern in such systems.

Traditional energy harvesting sources like photovoltaic cells, thermoelectric generators and piezoelectric harvesters as described in [1] are not ideal for implants since these sources require conditions that do not exists inside a mammalian body. The human body by itself is a storehouse of energy [49]. Although not in the right form for

electronics, in principle if the body could be used to power the implantable devices, the desired energy autonomy would be achieved in these systems. Bio-fuel cells have been proposed in literature that convert glucose to electrical energy [50–52] which are promising for implantable applications. However, these techniques either require additional chemical agents that may not be available inside a human body normally or have issues with long term stability. Additionally, previous works, by using some very specific bio-potentials, demonstrate energy extraction from snails [53], insects [54] and trees [55]. However, these bio-potentials do not exist in mammals. Therefore, the search for usable and reliable harvest-able bio-potentials inside mammals is still an active research area.

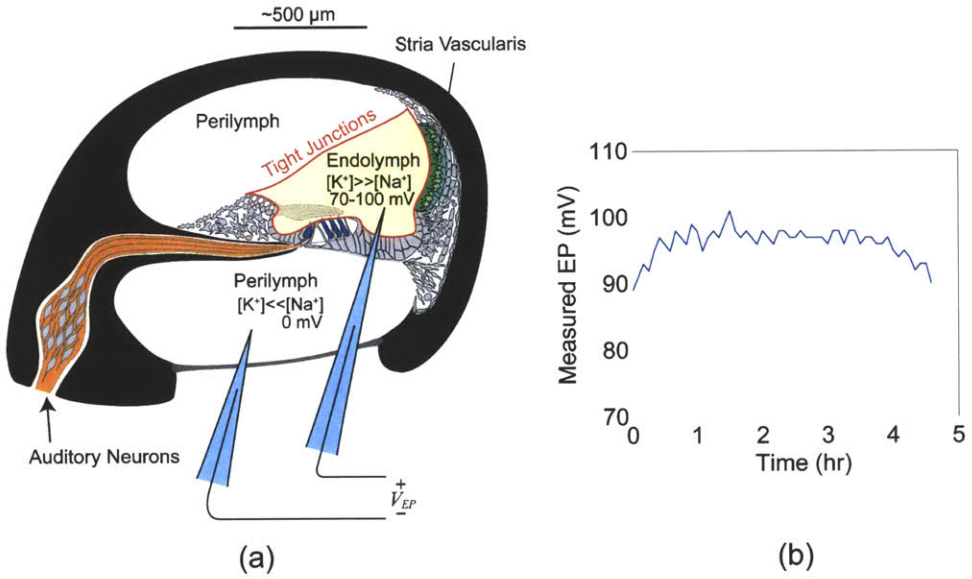


Figure 3-1: Endo-cochlear Potential in a Guinea Pig- (a) Cochlear Cross Section, (b) Measured Endo-cochlear Potential showing long term stability, courtesy Andrew Lysaght and Dr. Konstantina Stankovic, MEEI

3.1 Endo-Cochlear Potential

The Endo-Cochlear Potential (EP) is a 70 to 100mV dc bio-potential [56, 57] that exists between two fluids- the endolymph and the perilymph in a mammalian cochlea. This potential exists due to the higher concentration of K^+ ions in the endolymph as

compared to the perilymph. Figure 3-1(a) shows the anatomy of a guinea pig's inner ear with the location of the endolymph and the perilymph and the EP. Figure 3-1(b) shows a long term measurement of the EP in a guinea pig during an experiment (courtesy Andrew Lysaght and Dr. Konstantina Stankovic, MEEI). The EP is the largest dc bio-potential found in a mammal.

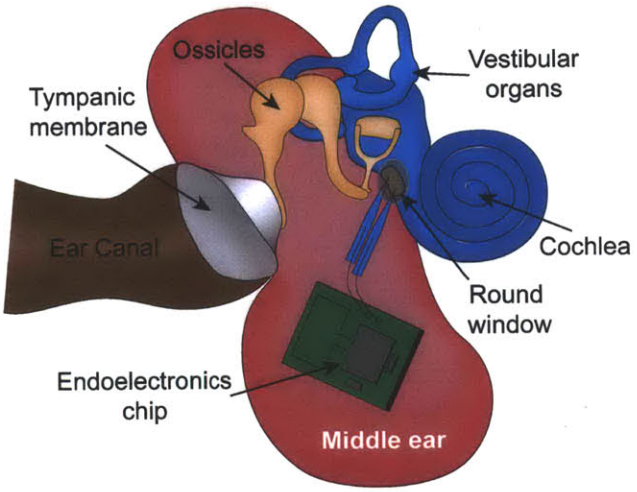


Figure 3-2: Proposed sensor being powered by the Endo-cochlear potential, courtesy Andrew Lysaght and Dr. Konstantina Stankovic, MEEI

The EP is actively stabilized by the inner ear making it a potential candidate for a *biologic battery* that can be used to power implant. The EP is well modeled [58] and is estimated to provide 14 to 28 μA of electrical current to inner ear. We focus on extracting a small fraction of this current to power an electronic implant. This proposed idea of extracting power from the EP has been demonstrated in [59]. The sensor, shown in Fig. 3-3, comprises of a PMU consisting of a boost converter with the associated control used to power the entire wireless sensor solely from the EP, and a low duty-cycled Radio Transmitter (RF-Tx) [60] that conveys the sensed information to the external world. Two $Ag^{+}/AgCl$ electrodes connected to the sensor are used to tap the EP. This chapter focuses on the power management unit (PMU) that powered the proposed sensor[1].

[1]The author of this thesis has designed the the power management circuits for the sensor, the RF-Tx was designed by Prof. Patrick Mercier (currently UCSD) and the surgeries for experimental testing with a guinea pig was performed by Andrew Lysaght (MEEI)

3.2 Sensor Architecture

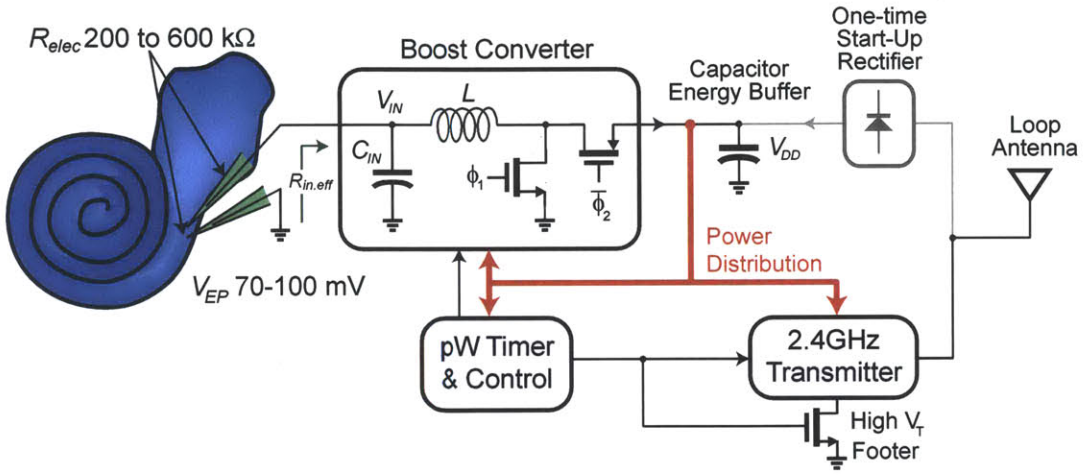


Figure 3-3: Sensor System Architecture [59]

The system comprises of a Power Management Unit (PMU) consisting of a boost converter with the associated control and timer circuits used to power the entire wireless sensor solely from the EP, and a low duty-cycled Radio Transmitter (RF Tx) that conveys the sensed information to the external world. The system architecture has been shown in Figure 3-3. As described before, the EP has a range of 70-100mV. Two $Ag^+/AgCl$ electrodes connected to the sensor are inserted into the endolymph and the perilymph to tap the EP. Due to the size and anatomical constraints in the inner ear, these electrodes need to have tip diameters close to 2μm. This causes the impedance of each electrode to be around 200kΩ to 600kΩ depending on the electrolyte concentration. With an overall electrode impedance of 400kΩ to 1.2MΩ, the maximum extracted power from the EP by the sensor is given by Eq. 3.1 where V_{EP} is the Endo-cochlear Potential (range of 70-100mV) and R_{elec} is the total electrode resistance (sum of endolymph and perilymph electrode).

$$P_{IN} = \frac{V_{EP}^2}{4.R_{elec}} \tag{3.1}$$

Therefore, designing circuits that extract energy from the EP has a some key chal-

lenges summarized as follows:-

1. Due to the low V_{EP} and high R_{elec}, the maximum extractable power from the EP by the sensor (P_{IN}) is in the range of 1.1-6.3nW. Although this ensures that a small fraction of the current generated by the cochlea is used by the sensor (0.1% to 0.8%), thereby potentially not impacting hearing, this makes the design of sensor electronics extremely challenging as the aforementioned extractable power range is significantly lower than the power budget of previously published low power wireless sensors [61, 62]. This means that the always-active circuits need to be designed such that their quiescent current is in the 10's to 100's of pA range. Further, circuits that can be power-gated also need to have leakage significantly lower that the overall system power budget.

2. To ensure maximum power extraction (as given by Eq. 3.1), the input voltage to the power converter in the sensor has to be close to half of V_{EP}. Therefore, we require a boost converter to convert a low input voltage (close to 35-50mV) to a higher voltage usable by CMOS circuits (0.8-1.1V here). Low power and high voltage conversion ratios make the task of designing an efficient boost converter extremely challenging. Along with switching and conduction losses, the leakage in the power train needs to be taken into consideration.

3. Starting up the sensor for the low EP voltage is extremely challenging. To address this challenge, a one-time wireless charging scheme is used to kick start the sensor. The same antenna used for the RF transmitter and ESD diodes have been re-used for the one-time start-up rectifier [60]. It is envisioned that after implantation, a burst of wireless power would be able to provide an initial voltage at the system power supply capacitor. Following this, the system would be able to sustain itself by extracting energy from the EP.

In this chapter, the first two challenges will be addressed while focusing on a PMU consisting of a boost converter with ultra-low power digital control circuits operating in pico-watts along with low power timers and power gating circuits that are commonly used in low power digital circuits. Additionally an auxiliary converter

(voltage doubler) has also been used to generate a higher supply voltage that is used implement leakage reduction techniques in the system. This system presents a classic example of where low power design of the control circuits can help increase the overall PMU efficiency and also sustainability in this case.

3.3 Power Management Unit for Energy Extraction from the Endo-cochlear Potential

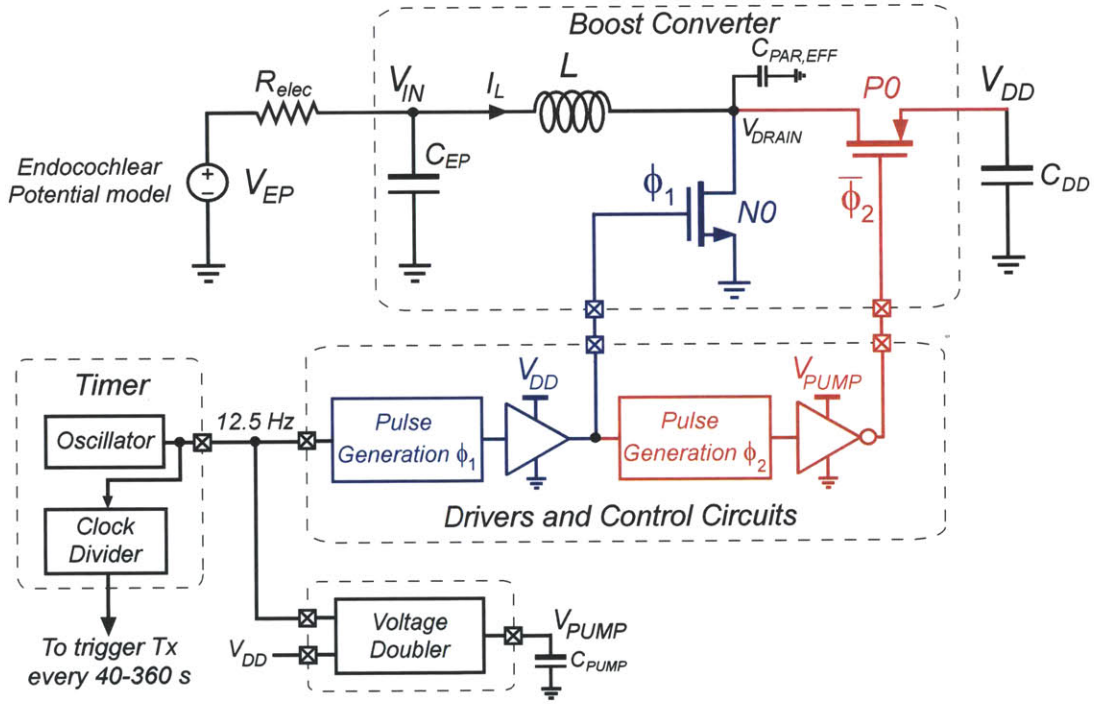


Figure 3-4: Power Management Unit for the sensor powered by the Endo-cochlear Potential

3.3.1 Ultra-Low Power Boost Converter Operation

The boost converter used in this work operates in the discontinuous conduction mode (DCM) due to the low power budget of 1.1 to 6.3nW. As discussed before, the converter is used to boost up an input voltage (V_{IN}) of 30-55mV up to 0.8-1.1V (V_{DD}).

The converter powers all the sensor circuits- boost converter control and timer circuits, a voltage doubler and a RF-Tx (Figure 3-4). The boost converter control circuits, timer and voltage doubler need to be powered continuously whereas the RF-Tx in the sensor is heavily duty-cycled (active for less than 0.0016% of the time) and is enabled only once in 40-360 seconds by turning on the high V_T footer shown in Figure 3-3. This ensures that the converter is able to accumulate enough energy from the EP to be able to turn on the RF-Tx for a short burst. Figure 3-5(a) shows this trickle charging operation of the boost converter. The system power supply slowly ramps up when the RF-TX is power-gated. When the RF-Tx is enabled, the V_{DD} droops instantaneously. After a short burst, the RF-Tx is again power-gated and the system power supply starts to increase again as shown in Figure 3-5(a). The converter input impedance (ratio of average V_{IN}, to average input current- I_{IN}) is approximately set equal to R_{elec} ensuring maximum power transfer. Therefore, V_{IN} is approximately half of the EP.

It must be noted that in traditional energy harvesting systems [63, 64], there are usually two power converters in series between the energy source and the load circuits where the first power converter regulates the input voltage (or adjusts the input impedance for maximum power transfer) storing the harvested energy on to a buffer (supercapacitor or battery) and the second converter regulates the output voltage to the load circuits. In this sensor however, due to the stringent power budget, a single boost converter has been used. The converter has an input impedance close to the electrode impedance thereby ensuring close to maximum power transfer from the EP. The output regulation, although coarse, is provided implicitly by the load circuits themselves. When the system has accumulated more energy, the RF-Tx is enabled more often.

Figure 3-5(b) shows the boost converter's operation on a cycle basis. During the Φ_1 phase, the NMOS power FET (*N0* in Figure 3-4) is on and the current through the inductor L ramps up storing energy in the inductor. After a fixed time t_1 (1.8 to 3μs in this work), *N0* is turned off and the PMOS power FET (*P0* in Figure 3-4) is turned

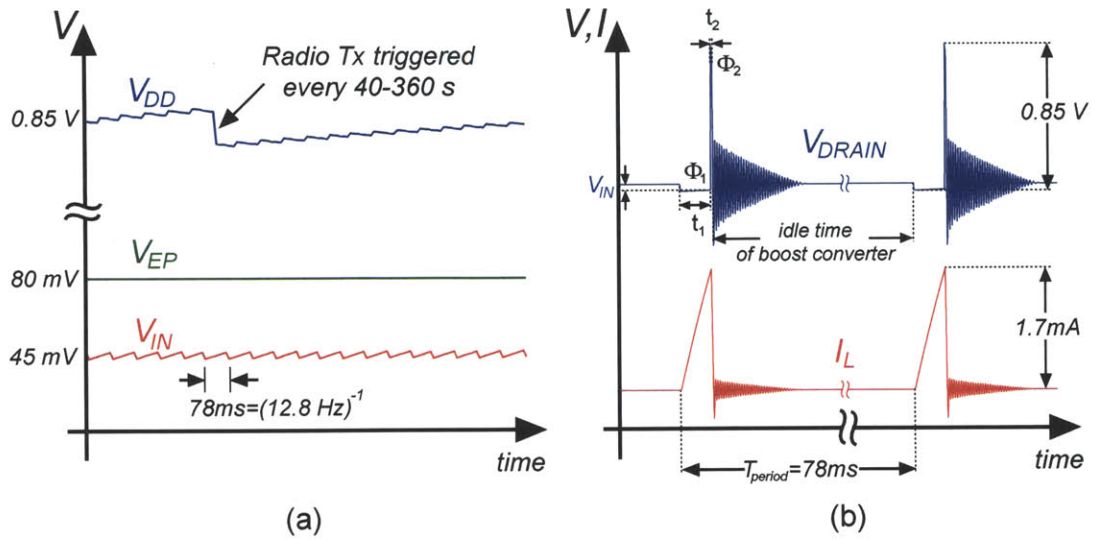


Figure 3-5: Boost Converter Operation, (a) Boost converter trickle charging system power supply, (b) Boost Converter Operation on a cycle basis

on for time t_2 causing the energy stored in the inductor to be transferred to the system power supply capacitor, C_{DD}. Since the converter is operates in DCM, following the Φ_2 phase, the converter stays idle until the Φ_1 phase of the next switching cycle. This idle phase (T_{period}-t_1-t_2) is much longer than phases Φ_1 and Φ_2 primarily due to the low input current to the converter. The major sources of losses in the converter are switching loss due to *N0* & *P0*, conduction loss in *N0* & *P0*, loss due to leakage in power train, loss due to $C_{PAR,EFF}$ (combined switching parasitic capacitance at the drain terminals of the power FETs) and conduction loss due to inductor ESR. It must be noted that $C_{PAR,EFF}$ accounts for the parasitic board capacitance, pad capacitance and the effective capacitance in parallel with the boost converter inductor which can be estimated from the inductor's self resonant frequency.

Further, in order to extract maximum power, the boost converter has to present an input impedance equal to the combined electrode impedances. It is possible to achieve this by a boost converter in DCM by fixing the *N0* on time (t_1), switching frequency (f_s) and the value of the inductor (L) [65]. The expression for the input impedance (Z_{IN}) is given by Eq. 3.2. In order to optimize the converter efficiency and ensure maximum power extraction, the converter losses need to be minimized

while satisfying Eq. 3.2.

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} \approx \frac{2 \cdot L}{t_1^2 \cdot f_s} \tag{3.2}$$

3.3.2 Unique Features of the Ultra-Low Power Boost Converter

Although the operation of the power converter is similar to that of a conventional boost converter in DCM, some specific considerations must be made while designing a power converter at such low power levels. There are two key aspects that make this converter's efficiency optimization different from previously published low power switching converters [64,66]. Before optimizing the converter, these aspects have been first discussed below.

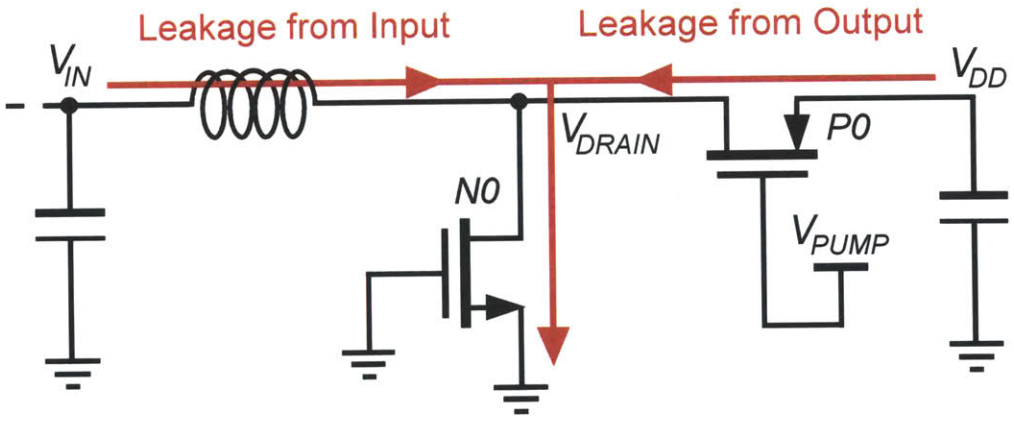


Figure 3-6: Leakage Paths in Boost Converter

Leakage in Power Train

While handling ultra-low power levels, the losses arising from the sub-threshold leakage currents through *N0* and *P0* can become comparable to the conduction and

switching losses due to the power FETs in the boost converter. In order to reduce the losses due to leakage currents, lets first see the leakage paths involved. During the converter's idle phase in DCM, both *N0* and *P0* are off as shown in Figure 3-6 (assume for now V_{PUMP} is equal to V_{DD}) and the V_{DRAIN} node voltage settles to V_{IN} as shown in Figure 3-5(b). For typical boost converters with high voltage conversion ratios, there are two leakage paths, one from the input and the other from the output as shown in Figure 3-6. The leakage current from the input flows through *N0* whereas the leakage current from the output flows through both *P0* and *N0*. Eq. 3.3 gives the expression for the sub-threshold leakage current in a NMOS transistor [67] where μ_o is the carrier mobility, C_{ox} is the gate oxide capacitance, m is equal to $1+\frac{C_{dm}}{C_{ox}}$, C_{dm} is the depletion layer capacitance, v_{th} is the thermal voltage, V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage and V_T is the threshold voltage. The expression for PMOS can be attained by simply using absolute values of V_{GS}, V_{DS} and V_T.

$$I_{DS,LEAK} = \mu_o C_{ox} \frac{W}{L}(m-1)v_{th}^2 \cdot e^{\frac{(V_{GS}-V_T)}{m \cdot V_{th}}} \cdot (1 - e^{-\frac{V_{DS}}{V_T}}) \tag{3.3}$$

In boost converters with high voltage conversion ratios, the loss due to the output leakage path tends to be much higher than the loss due to input leakage- 12.5 times higher in this implementation. This is mainly due to the fact that the output voltage, V_{DD}, is much higher than the input voltage, V_{IN}. Further, this leakage current is governed by the sub-threshold leakage through *P0*. In this work, an auxiliary converter (voltage doubler) has been implemented to reduce the leakage in *P0* which will reduce the power loss due to the output leakage path in the boost converter. In order to reduce this leakage, a gate signal with a supply voltage higher than V_{DD} is used. When off, *P0* sees a negative source to gate voltage (V_{SG}) which helps reduces sub-threshold leakage current in the transistor. A charge pump is used to generate the higher supply voltage (V_{PUMP}) required. This leakage reduction of course comes at a small cost of generating the V_{PUMP} supply. This will be discussed in detail later in this chapter.

Effect of Parasitic Capacitor in Power Train

In converters handling higher current levels, $C_{PAR,EFF}$ is usually smaller than the power FET intrinsic capacitances. However, due to the low current levels in this converter, the power transistors *N0* and *P0* are sized such that $C_{PAR,EFF}$ is greater than the intrinsic FET capacitances. Following the Φ_2 phase of the boost converter, the common drain terminal of *N0* and *P0* rings due to the resonant circuit formed by L, $C_{PAR,EFF}$ and C_{EP} as shown in Figure 3-5(b). Due to this ringing, the stored energy in $C_{PAR,EFF}$ is partly dissipated in the body diode of *N0* (V_{DRAIN} rings and goes a diode voltage below ground turning on the *N0* body diode) and in the inductor during the idle time of the boost converter. To get a quantitative idea, let's consider a typical value of 5pF for $C_{PAR,EFF}$. At a typical switching frequency of 1kHz and 1V V_{DD}, this would cause 2.5nW loss which is over the lower limit of the power budget of the system by 2.27 times and is 40% of the power budget upper limit. Further, it must be noted that depending on the board layout and the type of inductor, it might be difficult to control this parasitic capacitance. Therefore, the switching frequency of the converter needs to be appropriately selected. Therefore, keeping the leakage currents in the power train and the parasitic capacitances in mind, the boost converter is optimized.

3.3.3 Loss Optimization

In order to optimize the boost converter for efficiency at such low power levels, the converter losses need to be looked at in more detail. Equation 3.4 gives the analytical details of the converter's losses. In this analysis, $C_{N,0}$ and $C_{P,0}$ are the capacitances per unit width for *N0* and *P0*, W_N and W_P are the transistor widths, η is the efficiency of the voltage doubler, I_p is the peak inductor current, $R_{N,0}$ and $R_{P,0}$ are the resistance per unit width for *N0* and *P0*, $I_{LEAK0,N}$ and $I_{LEAK0,P}$ are the leakage currents per unit width of *N0* and *P0* and $R_{L,ESR}$ is the effective series resistance of the inductor.

$$
\begin{aligned}
Loss \approx\ & C_{N,0} \cdot W_N \cdot V_{DD}^2 \cdot f_s + \frac{1}{\eta} \cdot C_{P,0} \cdot W_P \cdot V_{PUMP}^2 \cdot f_s \\
& + \frac{I_p^2}{3} \cdot t_1 \cdot f_s \cdot \frac{R_{N,0}}{W_N} + \frac{I_p^2}{3} \cdot t_2 \cdot f_s \cdot \frac{R_{P,0}}{W_P} \\
& + V_{IN} \cdot I_{LEAK0,N} \cdot W_N + (V_{DD} - V_{IN}) \cdot I_{LEAK0,P} \cdot W_P \\
& + \frac{1}{2} \cdot C_{PAR,EFF} \cdot V_{DD}^2 \cdot f_s + \frac{I_p^2}{3} \cdot (t_1 + t_2) \cdot f_s \cdot R_{L,ESR}
\end{aligned} \tag{3.4}
$$

Further, since a boost converter with high voltage conversion ratios is being optimized, on approximating its inductor volt-second rule, we get Eq. 3.5. We also know that I_p is related to V_{IN}, L and t_1 as given by Eq. 3.6.

$$
V_{IN} \cdot t_1 \approx V_{DD} \cdot t_2 \tag{3.5}
$$

$$
I_p = \frac{V_{IN} \cdot t_1}{L} \tag{3.6}
$$

By imposing the impedance condition (Eq. 3.2) along with Eq. 3.5 and Eq. 3.6 on Eq. 3.4, we can simplify the conduction loss terms (for *N0*, *P0* and inductor *ESR*) and make the approximation V_{DD} is much greater than V_{IN}. Rewriting Eq. 3.4 with the aforementioned modifications, we get Eq. 3.7.

$$
\begin{aligned}
Loss \approx\ & C_{N,0} \cdot W_N \cdot V_{DD}^2 \cdot f_s + \frac{1}{\eta} \cdot C_{P,0} \cdot W_P \cdot V_{PUMP}^2 \cdot f_s \\
& + \frac{2^{3/2}}{3} \cdot \frac{V_{IN}^2}{L^{1/2}} \cdot \frac{1}{Z_{IN}^{3/2}} \cdot \frac{1}{f_s^{1/2}} \cdot \left[\frac{R_{N,0}}{W_N} + \frac{R_{P,0}}{W_P} \cdot \frac{V_{IN}}{V_{DD}} + R_{L,ESR} \right] \\
& + V_{IN} \cdot I_{LEAK0,N} \cdot W_N + V_{DD} \cdot I_{LEAK0,P} \cdot W_P \\
& + \frac{1}{2} \cdot C_{PAR,EFF} \cdot V_{DD}^2 \cdot f_s
\end{aligned} \tag{3.7}
$$

In order to minimize losses in the converter for fixed values of Z_{IN}, V_{IN} and L, the optimal values of f_s, W_N and W_P need to be obtained. Since this is a three variable optimization, minimizing Eq. 3.7 completely analytically is involved. It is worth

looking at approximations that can be made to simplify the optimization. First, among the switching frequency dependent loss terms, as mentioned before, C_{PAR} is much greater than the intrinsic device capacitances- $C_{N,0} \cdot W_N$ and $C_{P,0} \cdot W_P$ for such low power converters. Second, $R_{N,0}/W_N + [R_{P,0} \cdot V_{IN}]/[W_P \cdot V_{DD}]$ is much greater than the inductor *ESR* in this converter. With the aforementioned approximations, Eq. 3.7 can be optimized analytically by equating the partial derivatives of the with respect to f_s, W_N and W_P to zero. Eq. 3.8, 3.9 and 3.10 are obtained that give approximate optimal values of f_s, W_N and W_P.

$$f_{s,opt} \approx \left[\frac{\sqrt{k_1}}{2 \cdot k_4} \cdot \left\{\sqrt{\alpha \cdot k_2} + \sqrt{\beta \cdot k_3}\right\}\right]^{4/5} \tag{3.8}$$

$$W_{N,opt} \approx \left[\frac{k_1 \cdot \alpha}{k_2 \cdot \sqrt{f_{s,opt}}}\right]^{1/2} \tag{3.9}$$

$$W_{P,opt} \approx \left[\frac{k_1 \cdot \beta}{k_3 \cdot \sqrt{f_{s,opt}}}\right]^{1/2} \tag{3.10}$$

where α equals $R_{N,0}$, β equals $[R_{P,0} \cdot V_{IN}]/V_{DD}$, k_1 is $[2^{3/2} \cdot V_{IN}^2]/[3 \cdot L^{1/2} \cdot Z_{IN}^{3/2}]$, k_2 is $V_{IN} \cdot I_{LEAK0,N}$, k_3 is $V_{DD} \cdot I_{LEAK0,P}$ and k_4 is $\frac{1}{2} \cdot C_{PAR,EFF} \cdot V_{DD}^2$. For further refining the optimal values of $f_{s,opt}$, $W_{N,opt}$ and $W_{P,opt}$, a MATLAB routine is written which also takes into account the losses due to intrinsic device capacitances and the inductor *ESR*- the terms that were ignored in the analytical optimization before. The MATLAB code gives optimal values (Figure 3-7, assuming V_{IN} of 40mV and V_{DD} of 1V) that differ by about 10% from the expressions obtained analytically (Eq. 3.8, 3.9 and 3.10). During this optimization, $I_{LEAK0,N}$, $I_{LEAK0,P}$ and $C_{PAR,EFF}$ have been intentionally over-estimated. This design margin has been introduced to account for variability or any additional parasitic capacitance that may affect the efficiency of the actual implementation.

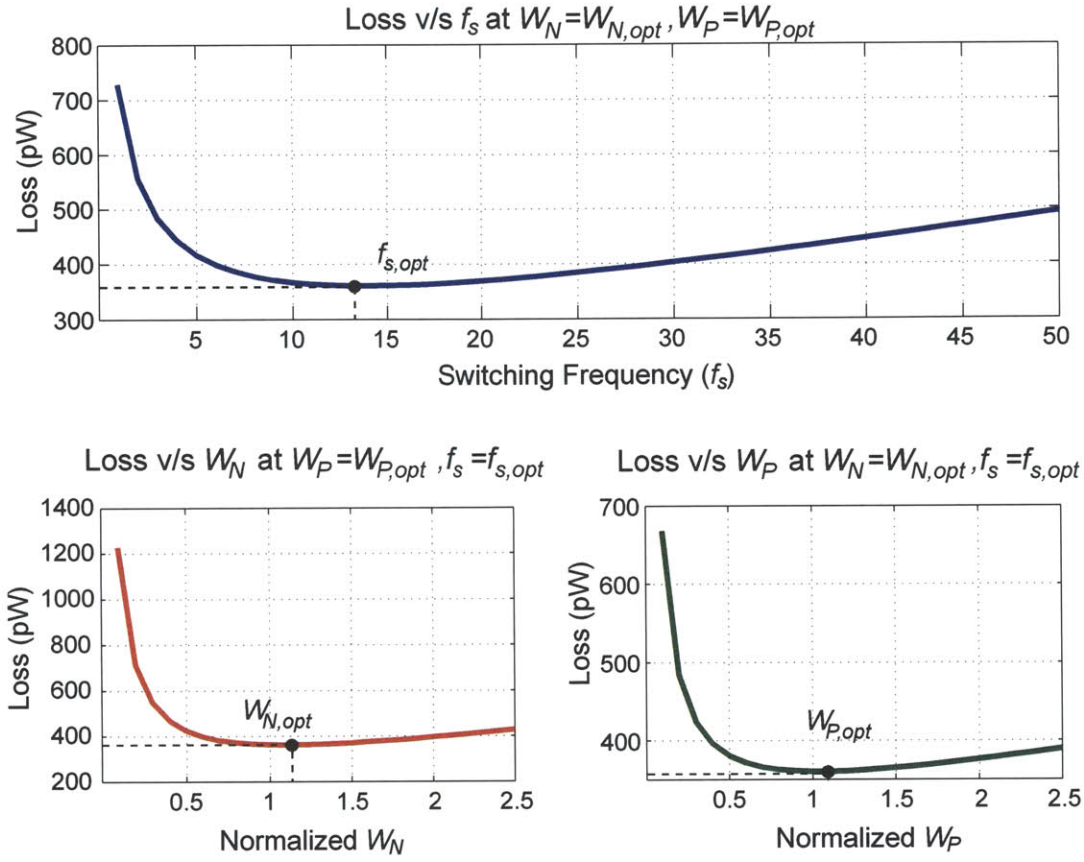


Figure 3-7: Loss Optimization with respect to f_s, W_N and W_P

3.3.4 Boost Converter Passives

As we can see from Eq. 3.7, higher inductance gives lower losses for fixed input impedance. However, due to the small form-factor requirement of the implant, the inductor (L) is limited to values in the range of 22μH to 47μH. A supply capacitor (C_{DD}) of 100nF to 220nF (ceramic) is used at the output of the boost converter. It must be noted that the maximum value of C_{DD} is limited by the insulation resistance of the capacitor since at these power levels, even the leakage of the off-chip C_{DD} capacitor needs to be considered. However, the minimum C_{DD} depends on the maximum instantaneous droop that can be sustained by the system power supply when the RF-Tx is enabled.

3.4 Control and Auxiliary Converter Circuits

In order for the wireless sensor to sustain itself, all the control and auxiliary circuits (shown in bottom half of Figure 3-4) have been designed to consume less than the energy harvested by the boost converter. The power consumed by these blocks account for the control power over-head which is extremely critical in ultra-low power converters. The control circuits ensuring maximum power extraction, power FET gate drivers, oscillator, current reference, and voltage doubler. In this section, the details of these circuits will be discussed.

3.4.1 Φ_1 Pulse Generation

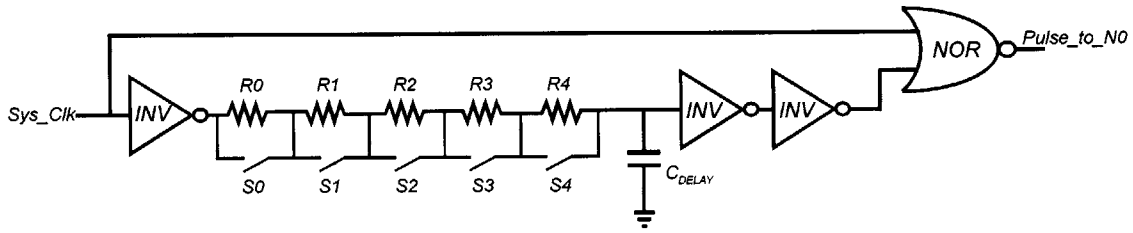


Figure 3-8: Pulse Generator for Φ_1 phase of Boost Converter

As discussed before in Subsection 3.3.1, the boost converter is configured to present an input impedance (Eq. 3.2) close to the electrode impedance to ensure maximum power extraction from the EP. This is done by configuring the converter to the desired input impedance before powering up the sensor. A tunable pulse generator (shown in Figure 3-8) is used to create the t_1 pulse with the desired width required during the Φ_1 phase of the boost converter. The pulse generator requires the system clock (*Sys_Clk*) as an input. A tunable resistor (implemented using *R0* through *R4* and switches *S0* through *S4*) along with a capacitor (C_{DELAY}) are used to introduce a delay in the clock. Subsequent logic circuits generate the pulses having the widths equal to the delays as shown in Figure 3-8. The pulse generator has been

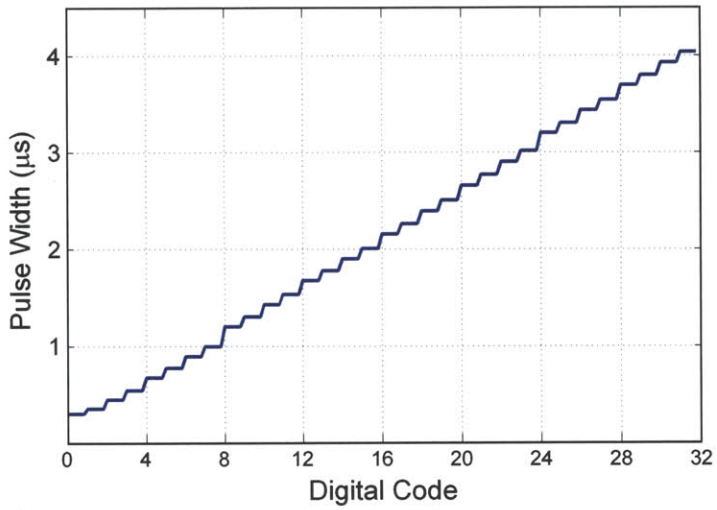


Figure 3-9: Pulse Width t_1 v/s Digital Code to switches *S0* through *S4*

designed for widths ranging from 0.25μs to about 4μs (in th typical corner at 0.9V) with 5 external tuning bits (to switches *S0* through *S4*) as shown in Figure 3-9 to cater for a wide range of electrode impedances (Eq. 3.2). Further, increased number of bits enable us to externally tune the resistor for process variations. Temperature variations do not need to be considered for this application as the implant ideally is in an environment having a stable temperature. It must be noted that inverters in the circuit have been designed to not contribute substantially to the overall pulse width. Since the transistors in these inverters operate above threshold (V_{DD} of 0.8-1.1V), the pulse generator can be designed such that the delays due to the tunable resistor and the capacitor C_{DELAY} contribute to the required pulse width. This makes the pulse widths and hence the converter's input impedance less sensitive to V_{DD}. Moreover, in practice, small variations in converter's input impedance caused by V_{DD} variations during the sensor's operation can be tolerated if the power transfer inefficiency due to mismatch between the electrode (source) impedances and the (load) converter's input impedance is negligible. For this design, the input impedance of the converter varies by close to 30% in the worst case for impedances values in the range of 400kΩ to 1.2MΩ with V_{DD} variation of 0.8-1.1V. This translates to a worst case power transfer inefficiency of only 3%.

3.4.2 Φ_2 Pulse Generation

As discussed before, during the Φ_2 phase, the boost converter's power transistor *P0* is enabled and the stored energy in the inductor is transferred to the output capacitor C_{DD}. Since the boost converter operates in DCM with synchronous rectification, it is necessary to ensure that *P0* turns off when the inductor current is close to zero. In case *P0* is turned off before the inductor current goes to zero, the parasitic body diode of *P0* gets enabled causing the residual inductor current to flow through the body diode instead of the transistor. This causes power higher power dissipation since the forward voltage of the diode (0.5-0.6V) is higher than the voltage drop across *P0* when on (less than 50mV). Considering the other case, when *P0* is turned off after the inductor current goes to zero, current flows back to the input from the output capacitor C_{DD}. This reduces the output power and reduces system efficiency. Therefore a Zero Current Switching (ZCS) scheme similar to [64, 68, 69] has been implemented.

Figure 3-10 shows the details of the circuits performing ZCS. A pulse generator similar to the circuit shown in Figure 3-8 but with smaller resistors and capacitor is used for Φ_2 pulse generation. The width of t_2 is required to be smaller than t_1 (Eq. 3.5) for the boost converter implemented. This pulse generator creates pulse widths varying from 9ns to 96ns to account for variability and wide range of t_1 values. A feedback loop is implemented to adjust the t_2 pulse width appropriately. Since the pulses created by the pulse generator blocks are discrete in nature, in the steady state, the t_2 pulse width toggles between two pulse width settings- one where the t_2 pulse width is slightly less than the ideal value (given by Eq. 3.5) and the other where the t_2 pulse width is slightly greater than the ideal value. When the t_2 pulse width is less than the ideal value, after *P0* is turned off, the parasitic body diode gets enabled and the voltage at the V_{DRAIN} node goes one diode drop over V_{DD}. However, when the t_2 width is greater than the ideal value, the V_{DRAIN} node voltage goes below V_{DD} after *P0* is turned off. By using a clocked comparator (StrongARM register [70]) that compares the V_{DRAIN} voltage with V_{DD} after *P0* is turned off, the feedback loop

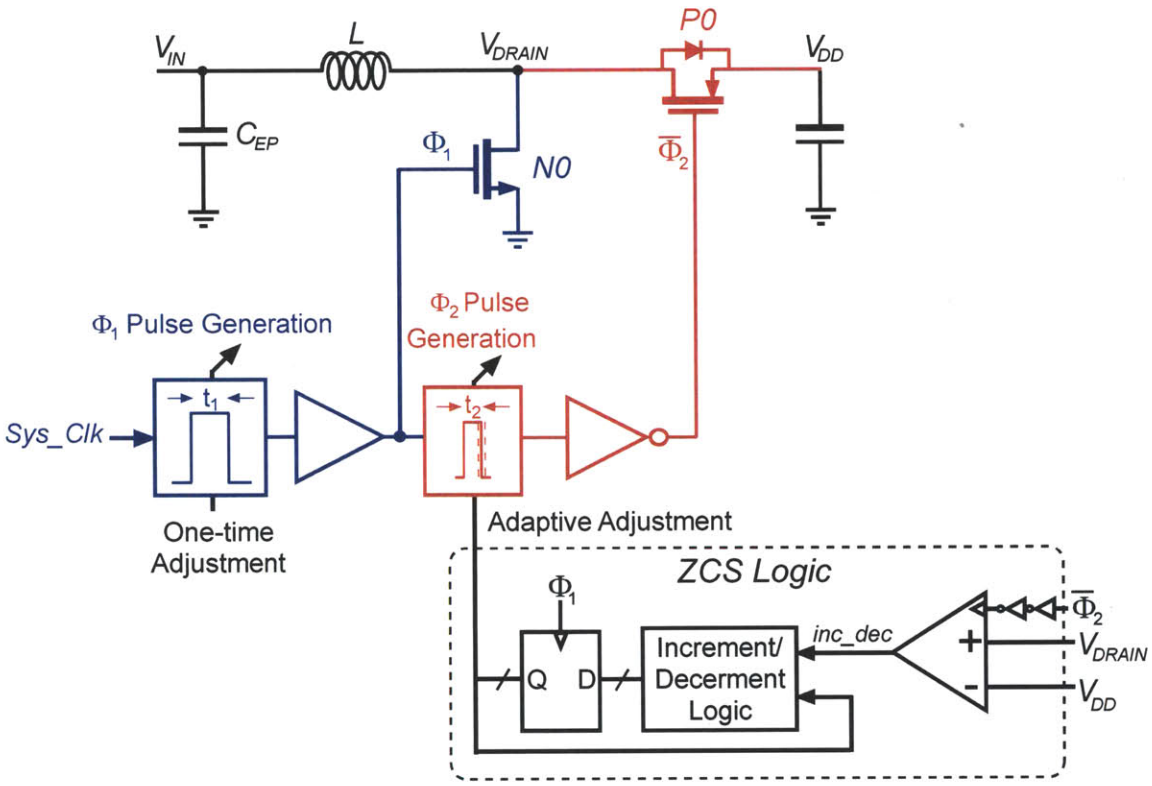


Figure 3-10: Zero Current Switching Circuit Details with Boost Converter, based on [64, 68, 69]

detects if the t_2 is greater than or smaller than the ideal value. The comparator output is used by an Increment/Decrement Logic block that either increases or decreases the t_2 width depending on the comparator decision. Therefore, as mentioned before, in steady state, the delay settings toggle between two states. Finally, an inverter chain is used to drive the gate of *P0* with the signal generated by the ZCS circuits.

3.4.3 Timer and Reference Circuits

All wireless sensors require Timers and References. Since these circuits need to be always active, their power consumption is critical for system sustainability. In this design, a pW Relaxation Oscillator similar to [71] and a clock divider have been implemented as Timer circuits (Figure 3-11). The oscillator is designed to generate

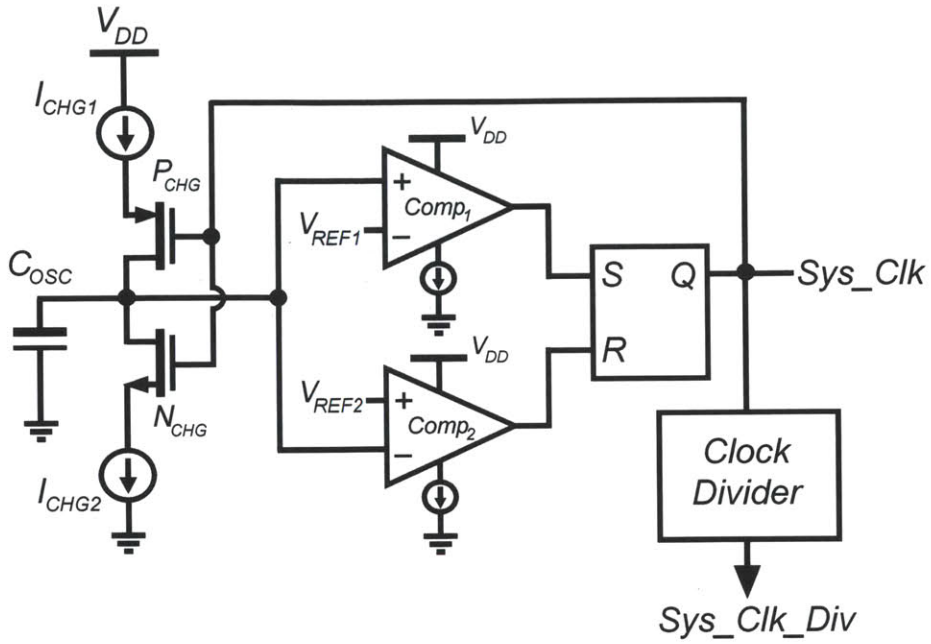


Figure 3-11: pW Relaxation Oscillator, similar to [71]

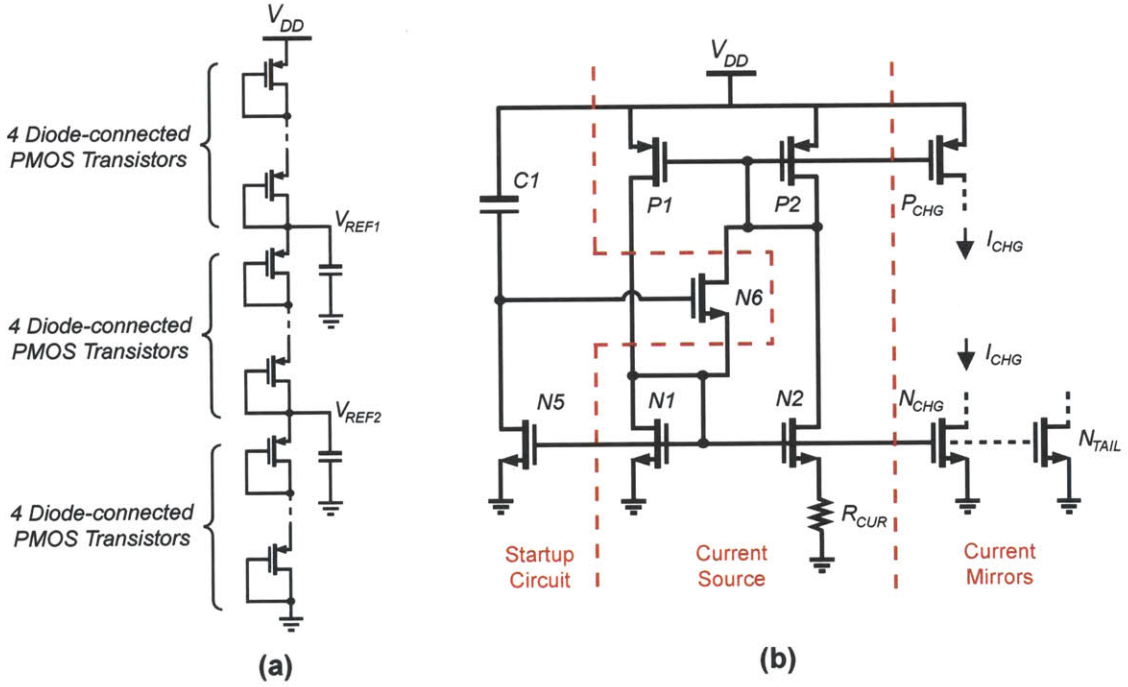


Figure 3-12: Auxiliary Circuits for Relaxation Oscillator: (a) Voltage Divider for Relaxation Oscillator, (b) Current Reference based on [72, 73]

a 12.82 Hz clock (*Sys_Clk*), with frequency close to the optimal f_s for the boost converter (discussed in Subsection 3.3.3). The clock divider creates a lower frequency clock (*Sys_Clk_Div*) from *Sys_Clk* which is used to enable the RF-Tx once in 40 to 360 seconds. Circuits for generating reference voltages (Figure 3-12(a)) and reference currents (Figure 3-12(b)) required by the oscillator have also been implemented.

In this implementation, two analog comparators, $Comp_1$ and $Comp_2$ (differential amplifier stage followed by common source stage), are used to compare the voltage across C_{OSC} with two reference voltages, V_{REF1} and V_{REF2}. Depending on which comparator triggers, either P_{CHG} or N_{CHG} is enabled causing current sources I_{CHG1} and I_{CHG2} to charge or discharge C_{OSC}. To the first order, the time period (T_{period}) of the oscillator is governed by I_{CHG1}, I_{CHG2}, C_{OSC} and the difference between V_{REF1} and V_{REF2}. However, in practice T_{period} also depends on the comparator delay ($t_{d,comp}$) and SR-latch delay ($t_{d,latch}$). Eq. 3.11 shows the approximate expression for the oscillator time period.

$$T_{period} \approx C_{OSC} \cdot (V_{REF1} - V_{REF2}) \cdot \left[\frac{1}{I_{CHG1}} + \frac{1}{I_{CHG2}}\right] + t_{d,comp} + t_{d,latch} \qquad (3.11)$$

For this design, the references V_{REF1} and V_{REF2} are set to $2V_{DD}/3$ and $V_{DD}/3$ respectively by a voltage divider formed by cascading twelve PMOS transistors in the subthreshold regime (Figure 3-12(a)). Currents I_{CHG1}, I_{CHG2} and the analog comparator bias currents are generated from the a supply independent current reference [72, 73] as shown in Figure 3-12(b). A R_{CUR} of 470MΩ is used to generate a current reference of value 60pA.

3.4.4 Voltage Doubler

As discussed before in Subsection 3.3.2, a voltage doubler circuit [74] is used to create an auxiliary power supply, V_{PUMP} ($\geq$1.5V), to power the gate drive circuit for the power FET *P0*. This results in a negative V_{SG} for *P0* when the device is off thereby,

reducing the sub-threshold leakage from the output in the boost converter. Further, the voltage doubler is also used to power the footer transistors of the RF-Tx helping in reducing leakage in the RF-Tx. In this subsection, the details of the ultra-low power voltage doubler circuit, efficiency analysis and its benefits will be discussed in detail.

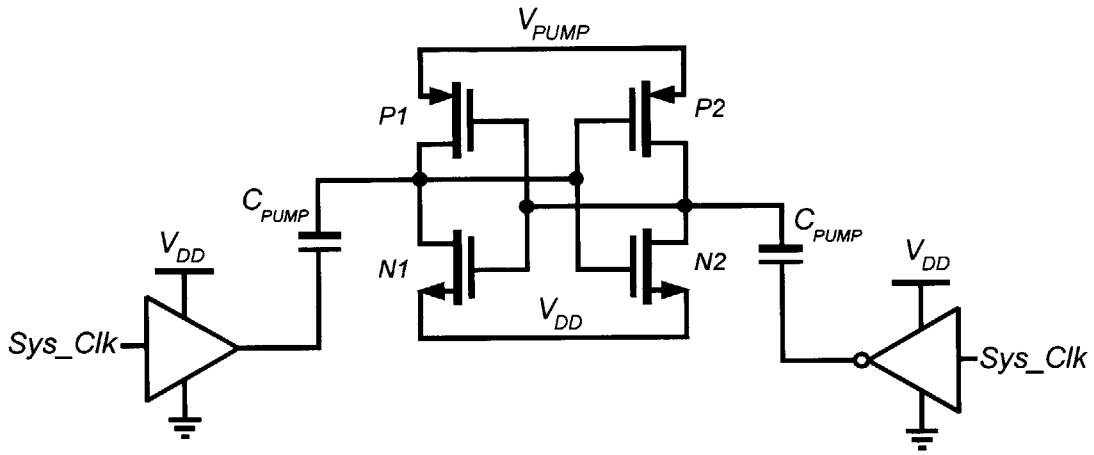


Figure 3-13: Voltage Doubler for Leakage Reduction

Figure 3-13 shows the implementation of the voltage doubler circuit. The doubler utilizes 2fF/μm^2 MiM capacitors for C_{PUMP} capacitors in Figure 3-13. The voltage doubler has been designed to deliver 30 to 40pW to the *P0* gate driver circuit. The circuit is switched at the same 12.8 Hz *Sys_Clk* frequency generated by the pW Oscillator discussed earlier. A total of 34.8pF is used as the charge transfer capacitors (2XC_{PUMP}). A 350pF output decoupling capacitor for the V_{PUMP} supply is also integrated with the charge pump. In order to operate effectively, the doubler power FETs *N1* and *N2* in Figure 3-13 use deep n-wells to avoid any threshold voltage increase due to body effect.

It must be noted that while optimizing the voltage doubler efficiency, the sub-threshold leakage currents through transistors *P1*, *P2*, *N1*, *N2* and through the buffer and inverter driving the bottom plate of C_{PUMP} need to be taken into account. Figure 3-14 shows the current paths in the doubler circuit during the two clock phases,

direction of switching currents (I_{SW1} and I_{SW2}) has been shown in blue and the leakage currents (I_{LEAK1} through I_{LEAK4}) in red. The total output current from the V_{PUMP} supply is given by Eq. 3.12 and the total input current from V_{DD} is given by Eq. 3.13 where α is the ratio of bottom plate parasitic capacitance to the actual capacitance and C_{Tran} is the switching effective gate capacitance due to the switches in the doubler circuit.

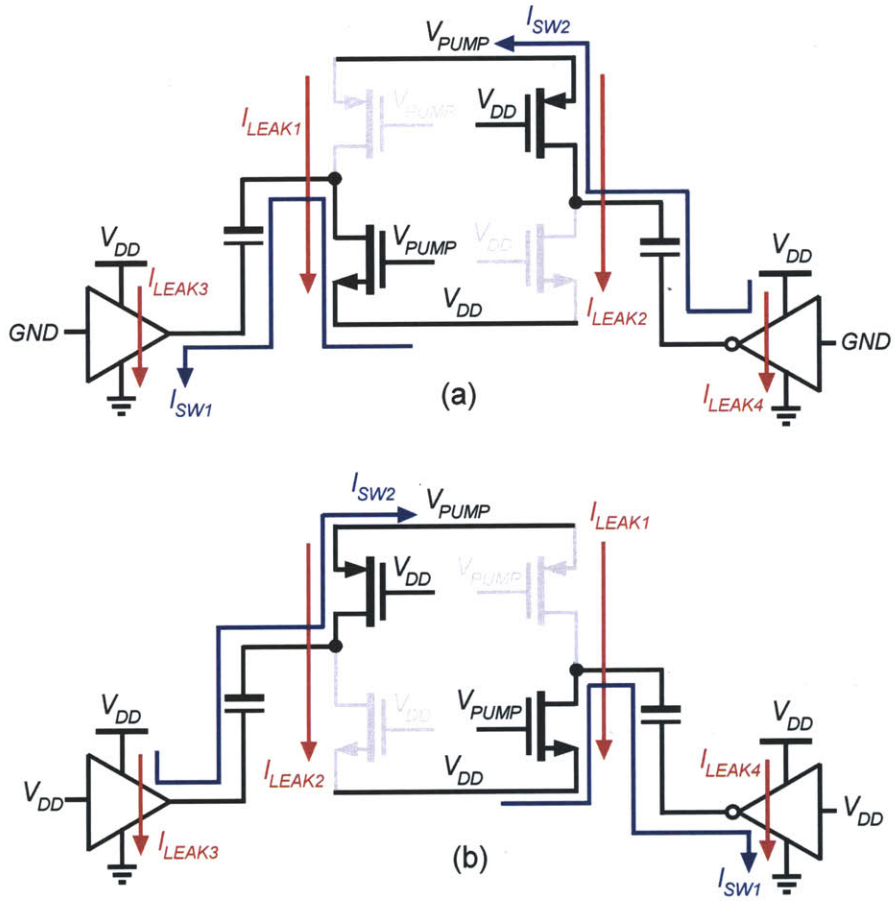


Figure 3-14: Current Paths Charge Pump in: (a) $Sys\_Clk{=}GND$, (b) $Sys\_Clk{=}V_{DD}$

$$I_{OUT,doubler} \approx 2C_{PUMP}[2V_{DD} - V_{PUMP}]f_s - C_{Tran}[V_{PUMP} - V_{DD}]f_s - I_{LEAK1} - I_{LEAK2} \tag{3.12}$$

$$I_{IN,doubler} \approx 4C_{PUMP}[2V_{DD} - V_{PUMP}]f_s + 2\alpha C_{PUMP}V_{DD}f_s - C_{Tran}[V_{PUMP} - V_{DD}]f_s - I_{LEAK1} - I_{LEAK2} + I_{LEAK3} + I_{LEAK4} \tag{3.13}$$

Therefore, the efficiency of the converter can be expressed as in Eq. 3.14 with terms k_1 and k_2 which have been defined in Eq. 3.15 and Eq. 3.16 respectively.

$$\eta_{doubler} \approx \frac{\left[1 - k_1\right]}{\left[2 + k_2\right]} \cdot \frac{V_{PUMP}}{V_{DD}} \tag{3.14}$$

$$k_1 = \frac{C_{Tran}[V_{PUMP} - V_{DD}]f_s + I_{LEAK1} + I_{LEAK2}}{2C_{PUMP}(2V_{DD} - V_{PUMP})f_s} \tag{3.15}$$

$$k_2 = \frac{2\alpha C_{PUMP}V_{DD}f_s - C_{Tran}[V_{PUMP} - V_{DD}]f_s + I_{LEAK3} + I_{LEAK4} - I_{LEAK1} - I_{LEAK2}}{2C_{PUMP}(2V_{DD} - V_{PUMP})f_s} \tag{3.16}$$

We must note that Eq. 3.14 is similar to the efficiency expression for the conventional *1:2* voltage conversion charge pump except for the fact that terms accounting for leakage along with usual switching losses and losses due to charge sharing have been included here. The voltage doubler efficiency has been optimized to around 77% in this implementation. Due to the ultra-low power requirement, the C_{PUMP} capacitors has been intentionally over-sized to account variations in leakage current through the doubler circuit transistors or in the *P0* gate drive circuit which is the load circuit for the doubler. Higher C_{PUMP} would enable us to suppress the efficiency degradation due to leakage in the doubler circuit (Eq. 3.15 and Eq. 3.16) and would also help in supplying more current to the *P0* gate drive circuit (Eq. 3.12).

The benefit of the voltage doubler in reducing the boost converter leakage can be quantified now. For this implementation, because of the voltage doubler, the leakage power due to sub-threshold leakage in *P0* is reduced from 224pW (simulated without doubler) to as low as 0.75pW (simulated with doubler) at the typical corner. This comes at the cost of increased switching loss and leakage in the *P0* gate drive circuit due to higher supply voltage. This overhead is estimated to be 30-40pW. On factoring in the efficiency of the doubler, this overhead becomes 39 to 52pW. Without the doubler, the gate drive circuit would have consumed 4pW. Therefore, an

overall benefit of 175 to 188pW (simulated) is obtained. Although may seem a small amount, this power reduction is close to 17% of the minimum system power budget. Moreover, in the fast corner, a benefit of about 950pW is obtained. Therefore, the doubler also enables us to make the PMU robust to process variations. Since we have the V_{PUMP} supply in the system, one may consider using an NMOS high side device with a floating driver instead of *P0*. However, the high side NMOS would have the same leakage as *P0* for the same on-resistance in the process used. Therefore, for reducing the power train leakage, a negative supply would be needed along with the V_{PUMP} supply. This would have an additional overhead without significant benefit. Hence this has not been pursued here.

Apart from the leakage reduction in the power train, the voltage doubler also helps in reducing leakage current in the RF-Tx. Having an elevated supply voltage (V_{PUMP}) in the system allows us to use a 3V NMOS transistor as the high V_T footer device for the RF-Tx. As the 3V transistors have higher I_{ON} to I_{OFF} ratios compared to the nominal 2V devices provided by the process, when off, the RF-Tx has more than 375X lower leakage with a 3V footer than with a nominal 2V device for the same on-resistance. This enables us to use smaller and therefore faster transistors in the RF-Tx resulting in lower power consumption [60].

Apart from the control circuits described, for this implementation, efforts have been made to reduce the sub-threshold leakage in logic circuits. The transistors in the logic circuits have been judiciously sized to reduce transistor leakage currents. Further, for logic circuits where the frequency is not a key concern, like the clock divider, 3V transistors provided by the process have been used.

3.5 Experimental Results

The PMU switches, control circuits, voltage doubler and the RF-Tx have been implemented on a 0.18μm CMOS process with 2V and 3V transistors. Figure 3-15 shows the die micro-photograph with the PMU details. As can be seen, most of the area

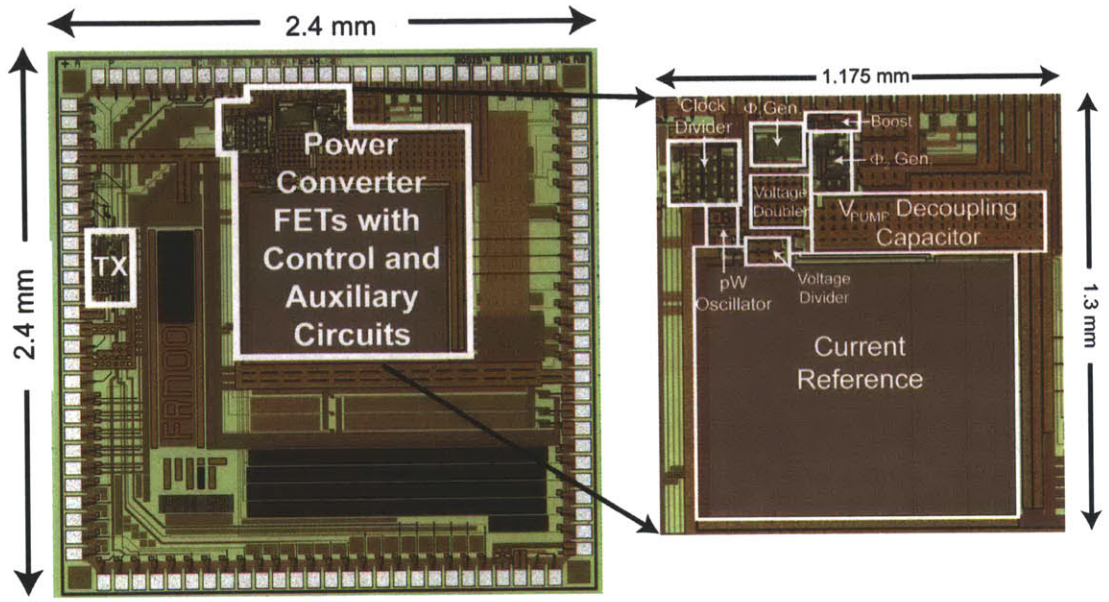


Figure 3-15: Die Micro-photograph with the PMU details

is occupied by the Current Reference resistor (R_{CUR} of 470MΩ) and the decoupling capacitor for the V_{PUMP} supply (350pF). The large R_{CUR} is due to the low quiescent requirements of the sensor circuits. The large decoupling capacitor is to minimize the droop in the V_{PUMP} supply during a RF-Tx transmission as the V_{PUMP} supply does not use any off-chip capacitors. Figure 3-16 shows the implantable sensor board. The only off-chip components are the boost converter inductor L (47μH, 4.8mm x 4.8mm), system supply capacitor C_{DD} (200nF), input capacitor C_{IN} (1μF) and an antenna (3mm x 4.3mm)for the RF-Tx.

3.5.1 Boost Converter Output Power and Efficiency

The output power (Figure 3-17(a)) and efficiency (Figure 3-17(b)) have been measured for an electrode impedance of 1MΩ (emulated by a 1MΩ resistor for this measurement) for two different values of the EP (80mV and 100mV, emulated using a voltage source for this measurement) with a V_{DD} of 0.9V and boost converter inductance of 47μH. The input voltage to the boost converter is varied by changing the input impedance of the boost converter. It can be observed from Figure 3-17(a), maximum power is

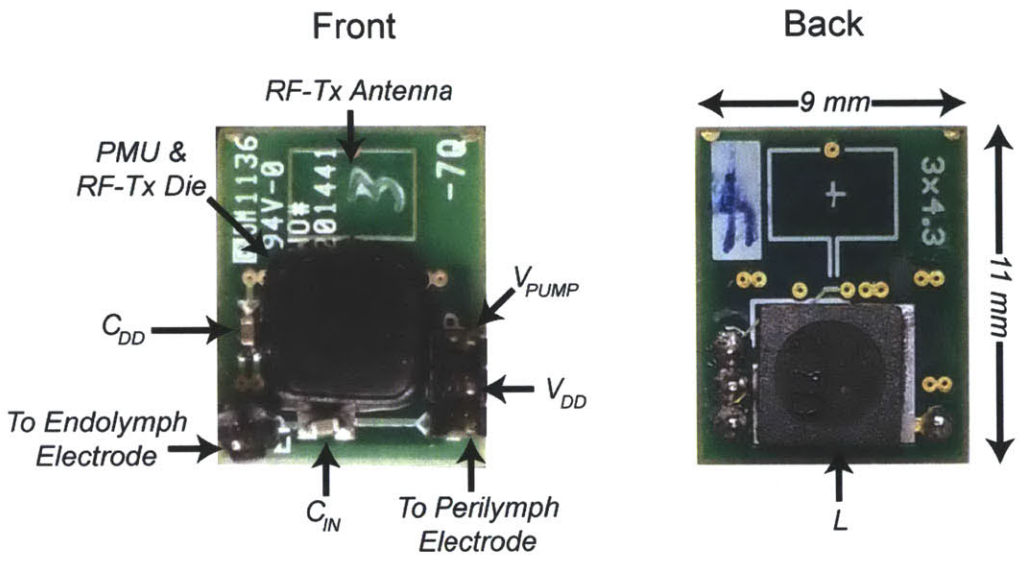


Figure 3-16: Implantable Senor Board Front and Back

extracted by the boost converter for voltages close to half of the EP. This is when the converter's input impedance equals the electrode impedance. For the boost converter efficiency in Figure 3-17(b), it is observed that the efficiency tends to be higher for higher input voltages. This is due to smaller inductor peak currents and therefore, smaller conduction losses for higher input voltages. However, for input voltages higher than a certain level (60mV for EP of 80mV, 70mV for EP of 100mV), the efficiency reduces due to lower power output from the boost converter. The converter is also characterized for different inductors. Figure 3-18(a) shows the output power from the boost converter for EP of 80mV, electrode impedance of 750kΩ, V_{DD} of 0.9V for different values of boost converter inductor. Figure 3-18(b) shows the corresponding efficiency plot.

3.5.2 Power Consumption of Individual Blocks

The quiescent power consumption of the individual blocks has been measured. For an input power of close to 1.2nW (with emulated EP of 80mV and electrode resistance of 1.28MΩ), the boost converter efficiency is observed to be close to 53% with V_{DD} around 0.9V. This translates to a total output power of 637pW from the boost con-

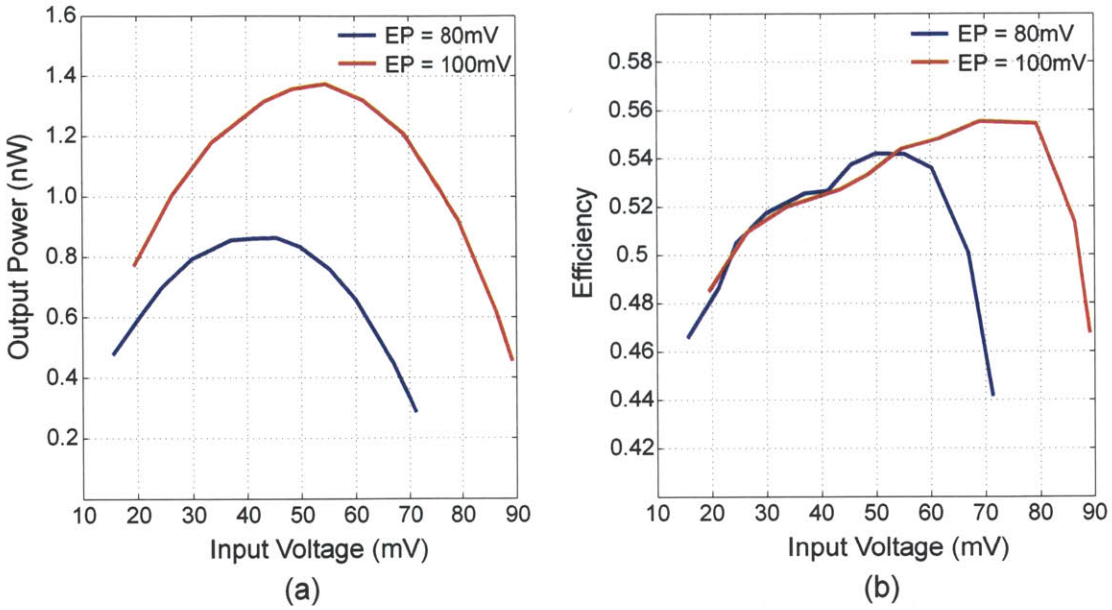


Figure 3-17: Boost Converter Results for different EP voltages: (a) Measured Power v/s Input Voltage, (b) Measured Efficiency v/s Input Voltage

verter. Figure 3-19 shows the power breakup of the individual circuits utilizing this power. Overall, 544pW is consumed in the converter's control circuits (Boost converter Impedance adjustment block, timer, reference, drivers and voltage doubler).

Careful design of the boost converter with the supporting control and auxiliary circuits ensure that the output power from the converter is not only enough to sustain the converter but a small fraction can also be used to power duty cycled load circuits like the RF-Tx in this work.

3.5.3 Supply Voltage Measurements during Surgical Experiments

Measurements have been made with the wireless sensor connected to electrodes tapping the EP of a anesthetized guinea pig. The sensor is kick-started by using a one-time wireless startup scheme [60], following which the system sustains itself by drawing power solely from the EP. The measured system power supply (V_{DD}) and

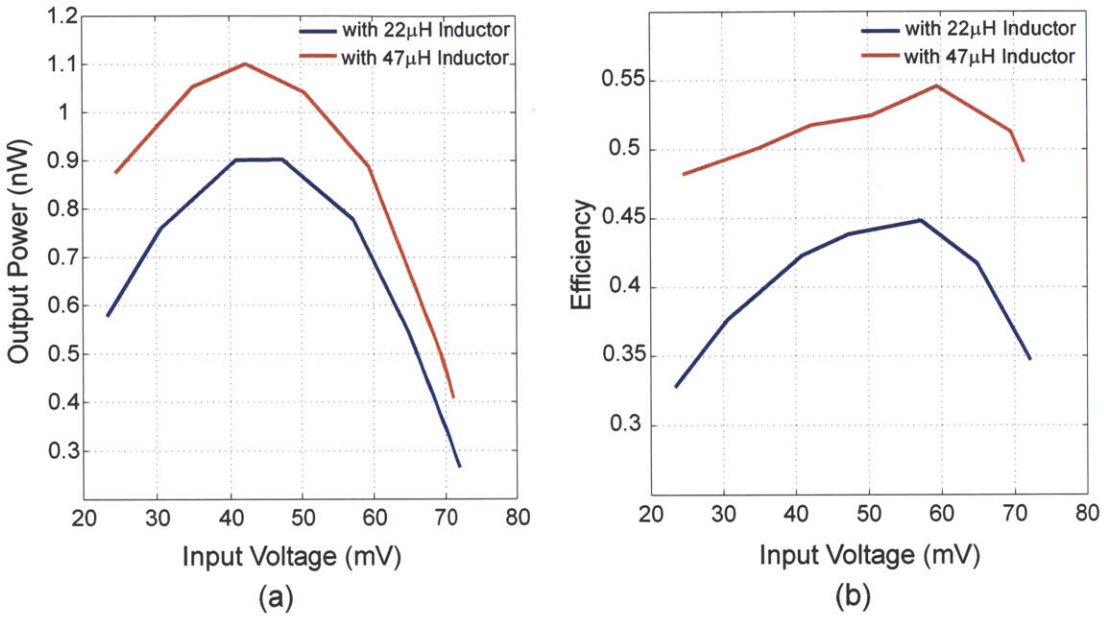


Figure 3-18: Boost Converter Results for different inductors: (a) Measured Power v/s Input Voltage, (b) Measured Efficiency v/s Input Voltage

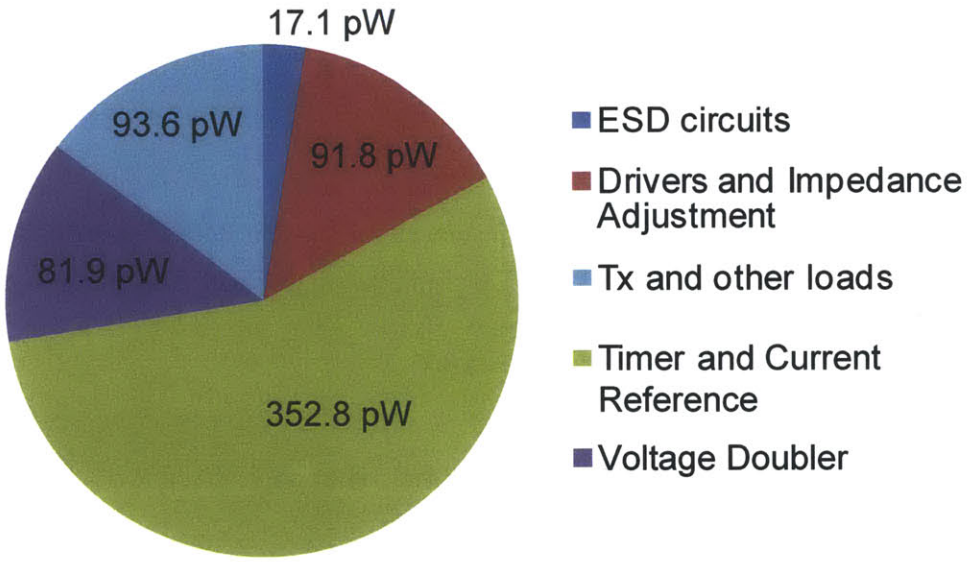


Figure 3-19: Power Consumption of Individual Circuit Blocks

doubler (V_{PUMP}) voltages have been shown in Figure 3-20 over a 3 hour period functioning absolutely autonomously. This shows the stability of the EP and the fact that

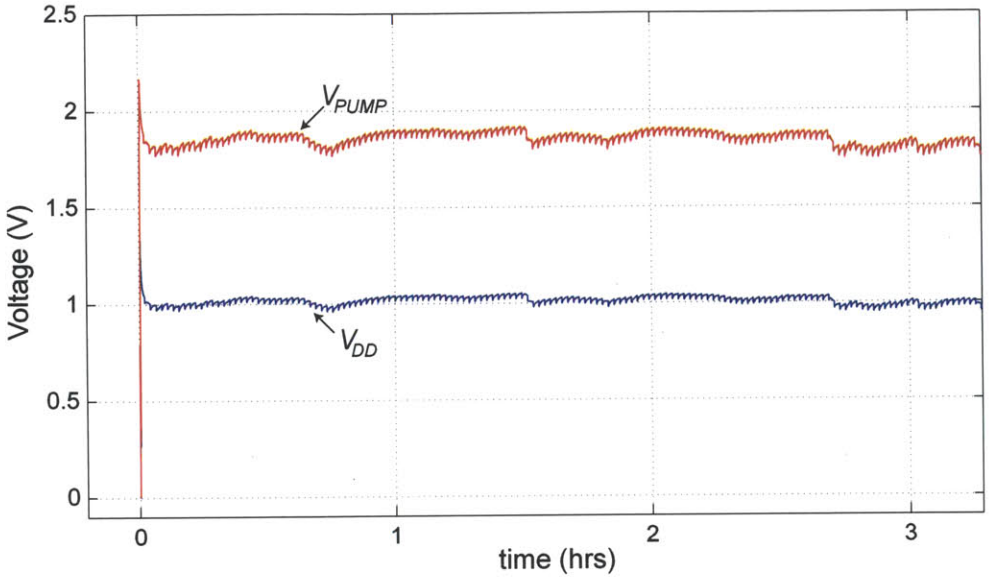


Figure 3-20: Long Term Transient Measurements

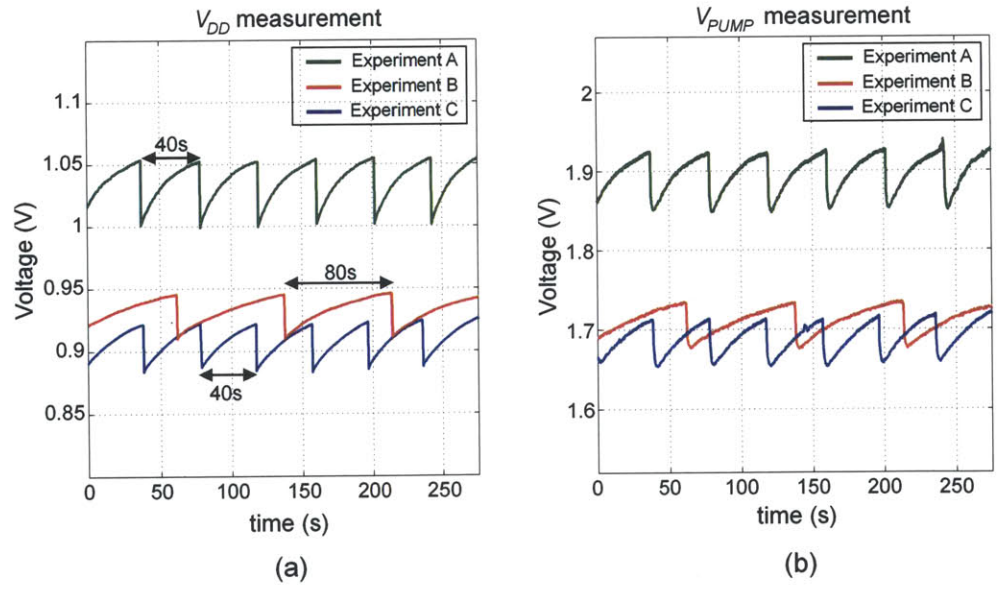


Figure 3-21: Short Term Transient Measurements: (a)V_{DD} measurement, (b)V_{PUMP} measurement

an implantable electronics can be powered by a bio-potential existing within mammals. Figure 3-21(a) shows the short term V_{DD} measurements made during three separate surgical experiments for EP values of 80-100mV and electrode impedances

in the range of 400kΩ to 1MΩ. Figure 3-21(b) shows the corresponding V_{PUMP} measurements. The supply voltages droop when the RF-Tx is enabled. For the measurements made, the RF-Tx is enabled either once in 40 to 80 seconds as can be seen in Figure 3-21. This is a one time setting that is done prior to the surgical experiment. Further, after the surgical experiment. hearing tests have been conducted that show that this power draw does not significantly affect the guinea pig's hearing [59].

3.5.4 Comparison of Boost Converter for EP Harvesting with State-of-Art Ultra-Low Power DC-DC Converters

Table 3.1 compares this work with State-of-Art ultra-low power converters [64, 75, 76]. As can be seen, the converter implemented is the lowest power boost converter reported. The converter has been optimized for low power levels of up to 4nW and has a quiescent power consumption of 544pW including all the timer, references and control circuits.

Table 3.1: Comparison with State-of-Art Ultra-Low Power DC-DC Converters

	[76]	[64]	[75]	This Work
Topology	Buck	Boost	Boost	Boost with Voltage Doubler
Voltage Conversion	2-5.5V step down to 1.3-5V	25-100mV boosted to 1.8-5V	80mV to 2.5V boosted to 3-5V	Inductive Boost:- 20-70mV boosted to 0.8-1.1V Voltage Doubler:- 0.8-1.1V boosted to 1.5-1.9V
Output Power	2.5μW-125mW	10-300μW	1μW-30mW	544pW-4nW
Efficiency at ultra-low power	55% at 2.5μW	32% at 10μW	20% at 1μW	54% at 1nW
Quiescent Power	760nW	NR	9.9nW	544pW

3.6 Conclusion

In this work, an ultra-low power PMU has been described that powers an implantable wireless sensor. The PMU works solely off the EP, a 70 to 100mV bio-potential existing in the mammalian ear. The power budget of the entire system is 1.1-6.3nW. Low power digital design techniques have been used to ensure that control circuits do not consume more than the power that can be extracted from the EP by the boost converter. First, digital implementations of of all control circuits operating at low voltage and low frequency (12.8Hz) help keep the quiescent power of all the control circuits down to 544pW. Moreover, the boost converter is also operated at the same switching frequency as the control circuits to reduce the loss due to the parasitic drain capacitance, $C_{PAR,EFF}$. Second, using leakage reduction techniques normally used in low power digital designs using a voltage doubler, the efficiency of the boost converter is increased. This work discusses how by using low power digital design techniques, sensor's sustainability is achieved.

Chapter 4

Energy Combining from Photovoltaic, Thermoelectric and Piezoelectric Harvesters with MPPT and Single-Inductor

Advancements in integrated circuit design have enabled the development of ultra-low power sensor nodes for health monitoring, industrial automation, smart buildings and for the automotive industry [77–80]. These low power circuits are required to sense signals, digitize, process and then transmit low data-rate information to a base-station. These sensors may be located in large numbers or in remote locations [79], making battery replacement extremely challenging. By using energy harvesting, it is possible to achieve battery-less, near-perpetual operation of these sensors. Further, attempts are also being made towards increasing the battery life of hand-held portable devices using energy harvesting [81].

Energy harvesting, by nature, is sporadic, making it unreliable for practical systems. By combining energy from multiple sources, it is possible to increase the overall system reliability. Also, there is a need to have a reconfigurable, universal

energy harvesting system that can interface with any harvester. In this work one such system will be discussed that combines energy from solar, thermal and vibration sources.

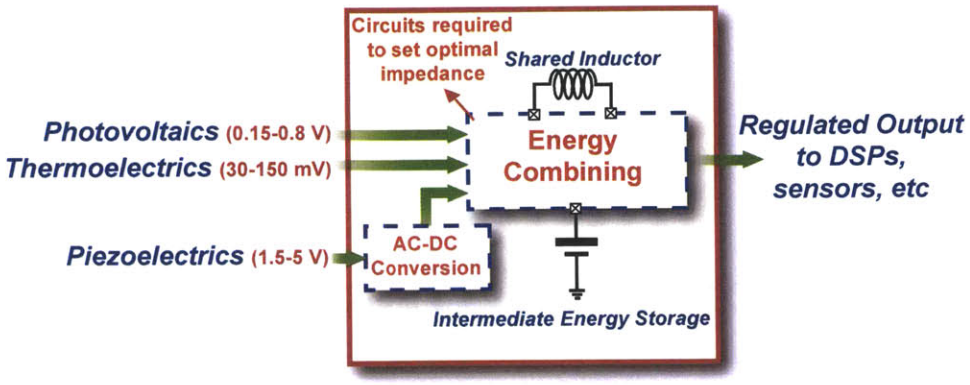


Figure 4-1: The multi-input energy harvesting system with solar, thermal and vibration energy inputs, intermediate storage, shared inductor and regulated output

Previous approaches in multi-input energy harvesting have involved either adding output voltages from individual harvesters by stacking individual storage capacitors [63], or selecting the harvester with maximum instantaneous power and directing its power to the output [82]. However, there is a need for a more efficient architecture for multi-input energy harvesting systems. Figure 4-1 shows a high level block diagram of the multi-input harvesting system that has been implemented in this work. Since the system has to cater for a variety of different energy sources, the design of such a power management unit will have some key challenges. Firstly, the power converters have to deal with a wide range of input voltages, from 20mV to 5V, for different harvesters [83–85]. Secondly, the system has to cater for a wide range of harvester impedances, from Ωs to kΩs [83–86]. Table 4.1 summarizes the requirements of different harvesters. Thirdly, high end-to-end efficiency is extremely important for these ultra-low power systems. Lastly, the component count needs to be kept low even with multiple power converters in the system.

In this chapter, the details of a multi-input energy harvesting system [65] are discussed. Section 4.1 of this chapter highlights the system architecture. It proposes a dual-path architecture for a single energy harvesting source and then extends the

Table 4.1: Comparison of different harvester voltages, optimal impedances and tracking requirements

Parameters \ Harvester Type	Thermal	Solar	Vibration
Material, Size, Conditions	BiTe, 50cm^2 ΔT~2-5K	Si (1-2 series) 500-2000lux	PZT (1-2 parallel) >1g
Harvester Voltage (open ckt)*	50-300mV	200-900mV	3-10V
Impedance to be presented for optimal power transfer	5-10Ω	0.05-2kΩ	10-150kΩ
Maximum Power Extraction	one time setting	tracking	one time setting

* Note the voltage to the energy harvesting circuit is lower (closed ckt voltage) during circuit operation

architecture to multiple harvesting sources. Section 4.2 deals with the maximum power extraction schemes for energy harvesters and presents a new Maximum Power Point Tracking (MPPT) scheme for photovoltaic harvesters. Section 4.3 focuses on inductor sharing for the energy combining architecture. Section 4.4 presents the measurement results and finally Section 4.5 concludes the chapter.

4.1 System Architecture

Traditional energy harvesting architectures consists of two stages of DC-DC converters [63, 64], as shown in Figure 4-2. This is assuming the harvester is a dc source (e.g. thermoelectric or photovoltaic harvesters). For an ac source (e.g. a piezoelectric harvester), a rectifier is used before interfacing with the DC-DC converters. The first converter is the Maximum Power Extraction stage. This stage is required to present the optimal input impedance [64] necessary for maximum power transfer from the harvester to the energy harvesting circuits. For switched-mode power converters, the input impedance can be viewed as the ratio of the input voltage to the average input current calculated over a number of switching periods [64]. The impedance can

be adjusted by setting the pulse width parameters or the switching frequency of the converter. This will be discussed in detail later in Section 4.2 of this chapter. Other techniques of regulating the harvester closed circuit voltage are also used [87] in the Maximum Power Extraction stage. These designs, may differ in implementation, but are implicitly the same as configuring the power converter input impedance.

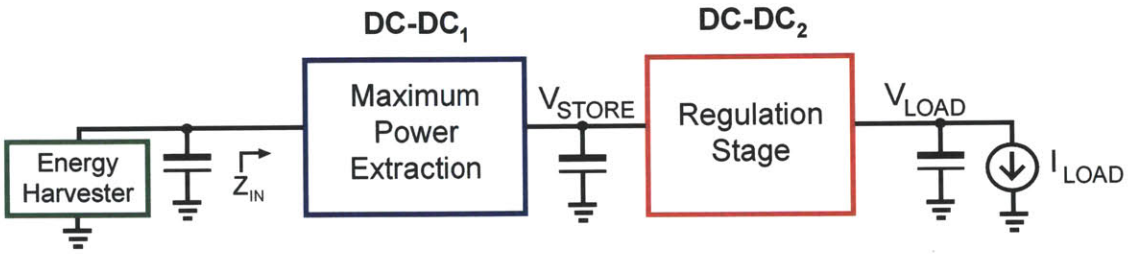


Figure 4-2: Traditional architecture with two stage power conversion

The energy extracted from the harvester needs to be stored to power loads when the ambient energy is not enough to meet the instantaneous load requirement. A battery or super-capacitor is used as the intermediate energy storage element at V_{STORE}. The second stage, shown in Figure 4-2, is the Regulation Block that provides the load circuits (e.g. DSP, μ-Controller and sensor circuits) with a stable regulated supply V_{LOAD} (say 1.8V), from the intermediate storage node, V_{STORE}. Therefore, both the input and output voltages of the energy harvesting circuits are set based on system requirements- the input is set by the impedance of the maximum power extraction block and the output, by the regulation stage. However, due to the two DC-DC converters in series, the energy from the harvester is processed twice before reaching the load circuits, thereby limiting the overall efficiency.

Figure 4-3 shows the dual-path architecture [65] that achieves higher efficiency than the traditional architecture. Here, the Maximum Power Extraction stage is split into two parallel converters- primary and secondary converters. When the ambient energy is available, the primary converter directly powers V_{LOAD} (at 1.8V in this implementation). Therefore, energy is transferred from the harvester to the load using a single power converter stage. However, as the load requires regulation, the primary converter is enabled only when the voltage V_{LOAD_DIV} (from a tunable

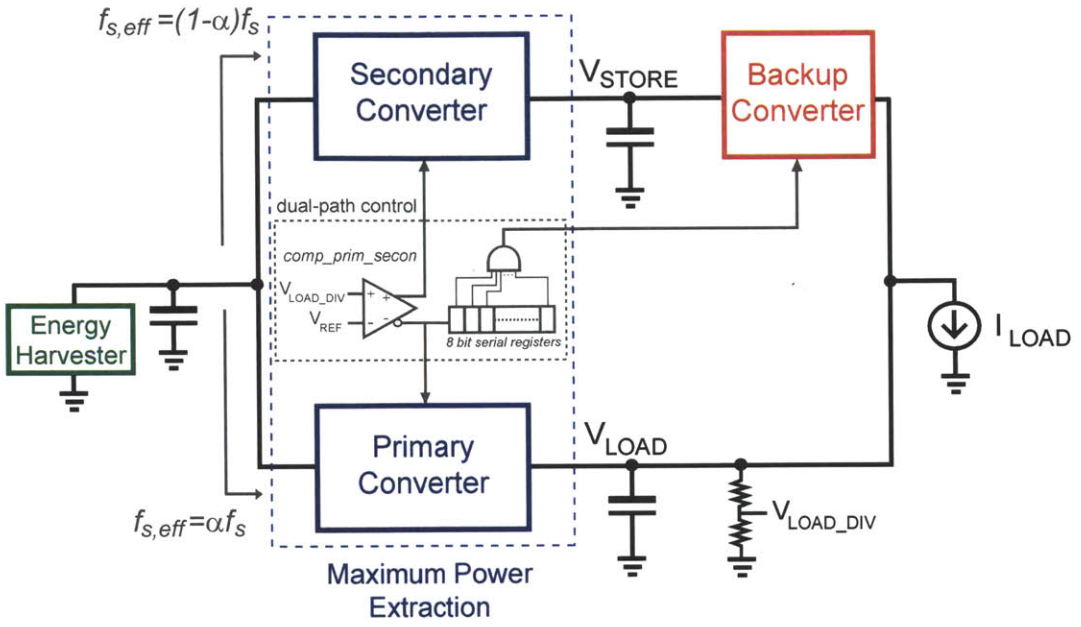


Figure 4-3: Dual-Path architecture with control

resistive division of V_{LOAD}), is below an internal reference V_{REF} (0.6V generated from a diode reference similar to [88]). When V_{LOAD_DIV} is higher than V_{REF}, the secondary converter is enabled, storing the excess energy from the harvester on to V_{STORE} (1.8-3.3V in this implementation). The control circuit for enabling these converters consists of a clocked comparator (a StrongARM latch [70] is used for this purpose), comp_prim_secon. This comparator enables the gate drive signals either to the primary converter or to the secondary converter power stages, depending upon whether V_{LOAD_DIV} is lower or higher than V_{REF}. Therefore, due to the complementary switching of the primary and secondary converters, V_{LOAD} is regulated and V_{STORE} is charged at the same time. Assuming the switching frequency of the Maximum Power Extraction stage in traditional architectures is f_s, for the dual-path architecture the effective frequencies (over a period of time) for the primary and secondary converters become $\alpha.f_s$ and $(1-\alpha).f_s$, where α is approximately the fraction of the input power being transferred to V_{LOAD}. Therefore, the system can be viewed as a pulse frequency modulated (PFM) power converter system where the individual frequencies of the primary and secondary converters are modulated depending on the

load requirement keeping the overall frequency of the Maximum Power Extraction stage the same as in traditional architectures.

In the dual-path scheme, the primary converter adequately delivers power to the load when the harvester is able to meet the load requirement. When the ambient energy is not enough for the load, the primary converter alone is not able to regulate the output. Therefore, backup converter is activated, transferring the previously stored energy from V_{STORE} to V_{LOAD}. Conceptually, this can be done by detecting when V_{LOAD_DIV} falls below V_{REF}-ΔV, another reference slightly lower than V_{REF}. The ΔV offset is required to ensure that the backup converter is active only when the primary converter alone is not able to regulate the load. However, in practice the comparator offsets might cause the primary and backup converters to falsely trigger with respect to each other when comparing V_{LOAD_DIV} with two voltages V_{REF} and V_{REF}-ΔV which are very close to each other. Here, the backup converter is activated only when the output of comparator comp_prim_secon enables the primary converter continuously for a fixed number of system clock cycles, the number being 8 in this implementation. Continuously enabling the primary converter indicates that the system needs more power hence, the backup converter gets activated. The number 8 is selected based on a trade off. If the number selected is larger, then the offset in the backup converter control circuit will increase thereby increasing the difference between the regulated voltage during light and heavy loads. However, if this number is smaller, then chance of triggering the backup converter when the primary converter is able to meet the load requirement increases. It was observed that the number 8 was adequate for this implementation in terms of regulation (shown in the Section 4.4), and also to ensure that the backup converter was not enabled at light to medium loads (with respect to the harvested power).

The dual-path architecture provides an efficiency improvement over the traditional architecture. It bypasses the second stage of the traditional two stage architecture (Regulation Block in Figure 4-2) when the input energy is able to meet the load requirement. Therefore, the system reduces to a single power converter supplying

energy directly to the load. When the load is much higher than the input power, the dual-path architecture functions exactly like the traditional architecture transferring the previously stored energy from V_{STORE} to V_{LOAD}. Therefore, we can see that by arranging the DC-DC converters appropriately, it is possible to have one converter between the harvester and the load in the best case and two converters (similar to traditional architectures) in the worst case. As will be shown in Section 4.4, the dual-path architecture provides a peak efficiency improvement of 11-13%.

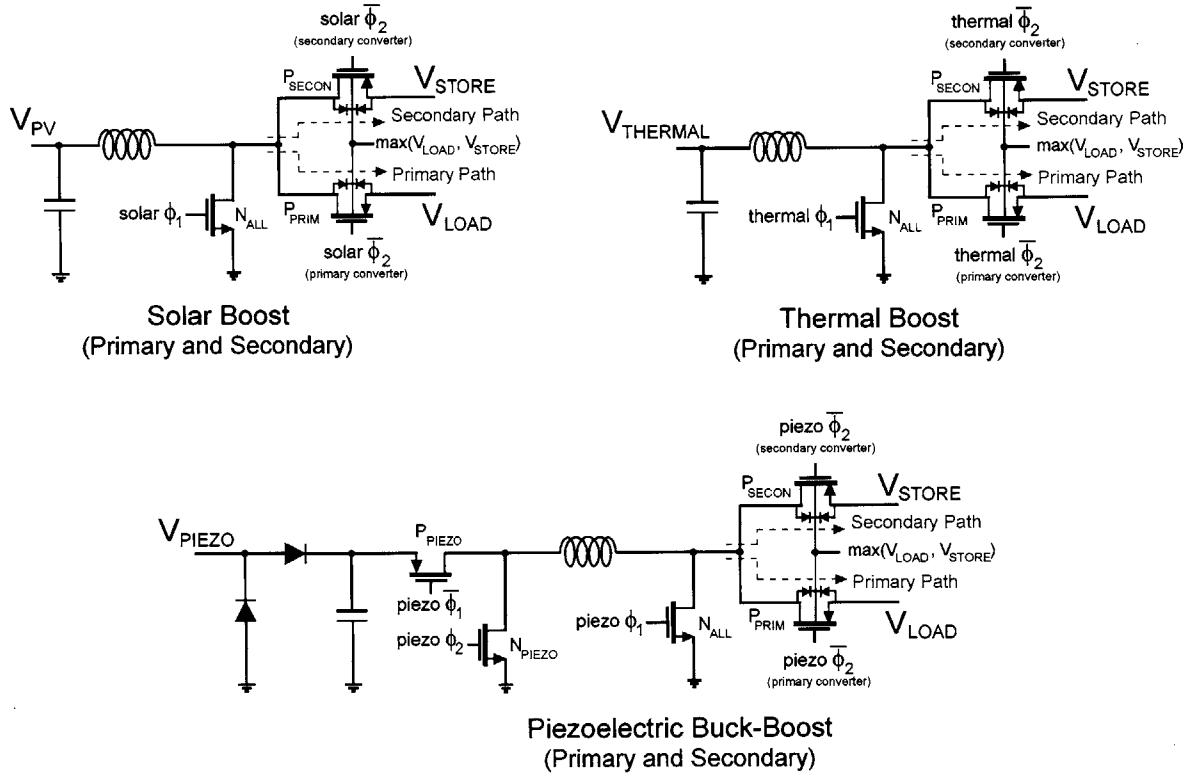


Figure 4-4: Conceptually the individual power converters in the dual-path scheme (inductor sharing between converters for different harvesters not shown for clarity)

In this work, in order to combine energy from multiple harvesting sources, multiple power converters are used in parallel for the Maximum Power Extraction stage. These converters either store energy to V_{STORE} or supply power to V_{LOAD} in parallel. For thermal and photovoltaic inputs, boost converters have been implemented and for the piezoelectric input, a rectifier followed by a buck-boost converter is employed. For each of these harvesters, the dual-path architecture, with both primary and secondary

converters, is implemented. Figure 4-4 shows the conceptually individual power converter topologies for the different harvesters in the dual-path mode. The inductor and ϕ_1 switches in the power stage of the primary and secondary converters for each harvesting source can be shared. Therefore, the efficiency improvement due to the dual-path architecture can be obtained without the addition of an extra inductor. In the actual implementation, a switch matrix with a single inductor is used that can be configured to the converter topologies shown in Figure 4-4. This will be discussed in detail later in Section 4.3. The bulk terminals of P_{PRIM} and P_{SECON} have to be biased here to the greater of V_{LOAD} and V_{STORE} to prevent activation of body diodes. This is done using an analog multiplexer and a comparator for comparing V_{LOAD} and V_{STORE}. It must be noted that the only overheads in the dual-path architecture are from the extra control circuits (occupying 0.0696mm^2 for each harvester, that can be significantly reduced by removing the test circuits), extra switch in the power train (P_{PRIM}, occupying 0.0315mm^2) which adds an additional capacitance (estimated to be 4.9pF which is less that 7% of the C_{gd}+C_{db} due to N_{ALL}) and higher $R_{ds,on}$ (higher by 25% in the worst case) of P_{PRIM} and P_{SECON} due to body biasing. For the boost topology with high voltage conversion ratios, in case of thermoelectric and photovoltaic harvesters, an increased $R_{ds,on}$ for P_{PRIM}/P_{SECON} does not affect the efficiency significantly since the converters spend more time energizing the inductor than de-energizing it. Therefore, even with these overheads, the benefit of the dual-path architecture is obtained.

4.2 Maximum Power Extraction

4.2.1 Harvester Electrical Models

Most energy harvesters can be modeled as either a voltage or current source (the main energy source) and a circuit element limiting the maximum extractable power from the harvester. Figure 4-5 shows the electrical models along with the plot of

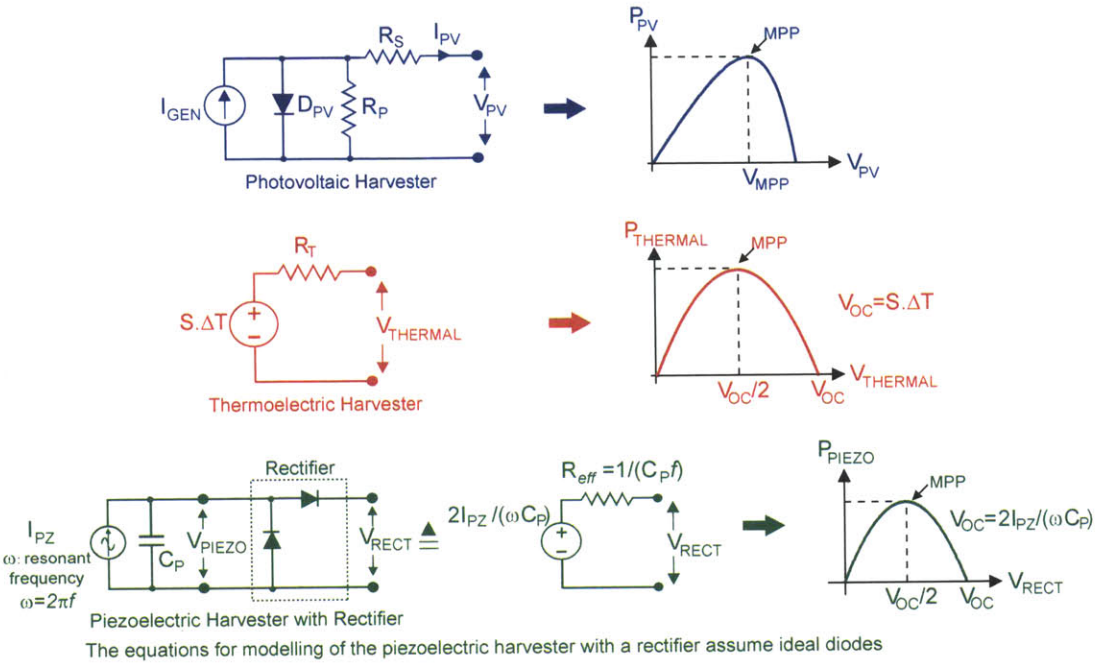


Figure 4-5: Energy harvester electrical models with corresponding power versus closed circuit voltage

power versus closed circuit voltage for individual harvesters. For photovoltaic cells, the current source I_{GEN} represents the light activated energy source. For a given light intensity, the amount of extractable power depends on the cell voltage (V_{PV}). For low cell voltages (say <0.2V for single cell), the current supplied by the photovoltaic cell (I_{PV}) is close to I_{GEN}, but the output power is low because of low V_{PV}. For higher cell voltages (say >0.4V for single cell), the diode parallel to I_{GEN} gets activated and shunts part of I_{GEN} to ground, thereby reducing I_{PV}. Therefore, there is an optimum voltage for power extraction from the photovoltaic cells. This is the maximum power point voltage (V_{MPP}) [89–93]. Depending on the type of cell, the series and shunt resistors (R_s and R_p in Figure 4-5) may also affect the V_{MPP}. It must be noted that this point varies with the light intensity. In case of thermoelectric harvesters [84], as shown in Figure 4-5, the voltage being generated is given by $S.\Delta T$, where S is the Seebeck coefficient of the thermoelectric material and ΔT is the temperature differential applied across the thermoelectric material. In this case, the internal resistance (R_T) in series with the voltage source limits the maximum extractable power. For

piezoelectric harvesters, by an analysis similar to the one in [86], it can be shown that the ac model of the piezoelectric harvester at resonance, along with the rectifier, is equivalent to a dc voltage source in series with a resistor as shown in Figure 4-5 Maximum power extraction from an energy harvester that is modeled using linear elements is achieved if the input impedance of the power converter interfacing with the harvester is configured to be equal to the harvester's internal impedance. For piezoelectric (along with a rectifier) and thermoelectric harvesters, this requirement can be met since the internal impedance can be modeled as a resistor that is approximately constant over the harvester's operating range. Therefore, power converters for thermoelectric and piezoelectric harvesters require one-time impedance tuning during installation. However, for photovoltaic cells, the main power limiting element, diode D_{PV}, is non-linear. Therefore, the maximum power transfer theory for linear circuits is not applicable. The analysis in [93] presents an expression for the optimal current-versus-voltage (I-V) response of a circuit element necessary for extracting maximum power from a photovoltaic cell. However, realizing a circuit element having an arbitrary I-V response based on the non-linearity in the energy source is extremely difficult. Instead, a feedback (or tracking) loop is usually employed to regulate the photovoltaic cell voltage (V_{PV}) close to the maximum power point voltage (V_{MPP}) for different light intensities. In this work, a unified approach to maximum power extraction by impedance adjustment is extended for all harvesters. This is explained in the next sub-section.

4.2.2 Realization of Impedance for Optimal Power Extraction

In order to facilitate low power operation, all the power converters have been made to operate in the discontinuous conduction mode (DCM) in this work. Considering a boost converter in the Maximum Power Stage in traditional architectures, as shown in Figure 4-6, during the first switching phase ϕ_1, the inductor current ramps up to $V_{HAR}.t_1/L$ and ramps down to a value close to zero by the end of the second switching

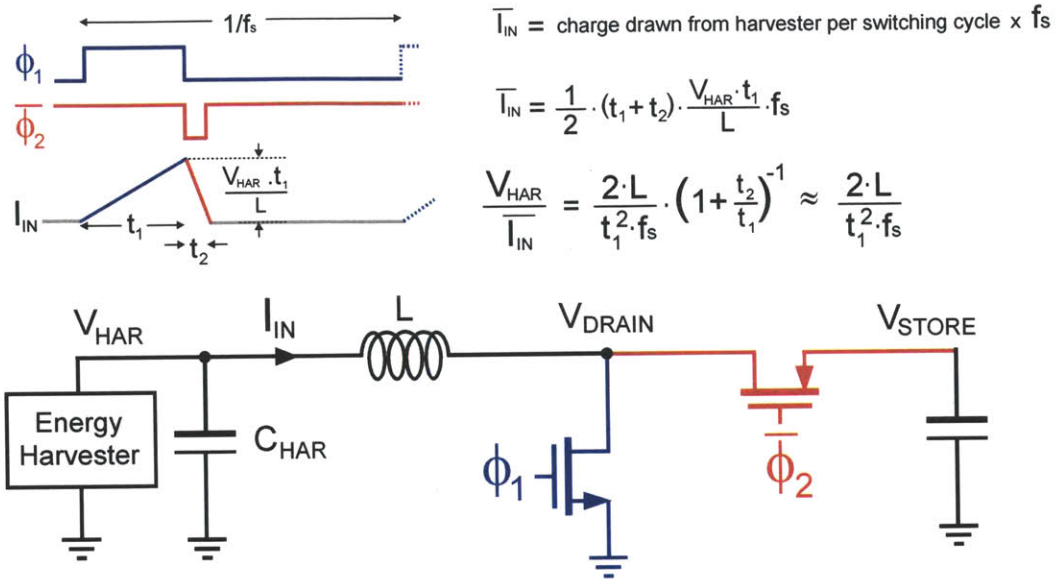


Figure 4-6: Impedance adjustment in boost converters as the Maximum Power Extraction stage for traditional architecture

phase ϕ_2. The average input current (I_{IN}) is given by Eq 4.1.

$$I_{IN} = \frac{V_{HAR}.t_1.(t_1+t_2).f_s}{2.L} \tag{4.1}$$

where L is the value of the inductor, V_{HAR} is the energy harvester output voltage, t_1 is the time duration of ϕ_1, t_2 is the time duration of ϕ_2 and f_s is the switching frequency of the boost converter as shown in Figure 4-6. As mentioned before, the power converter input impedance can be viewed as the ratio of the input voltage (V_{HAR}) to the average input current (I_{IN}). Therefore, the input impedance can be expressed by Eq 4.2

$$\frac{V_{HAR}}{I_{IN}} = \frac{2.L}{{t_1}^2.f_s}.\left(1+\frac{t_2}{t_1}\right)^{-1} \tag{4.2}$$

Also for the boost converter in Figure 4-6, the inductor volt-second rule gives the relationship between ϕ_2 and ϕ_1 time durations, t_2 and t_1 as shown in Eq 4.3

$$t_2 = \frac{V_{HAR}.t_1}{V_{STORE} - V_{HAR}} \tag{4.3}$$

For boost converters with high conversion ratios (>3 in case of converters used for thermoelectric and photovoltaic harvesters with V_{HAR} around 20mV-0.6V and V_{STORE} of 1.8 to 3.3V for this implementation), Eq 4.2 is approximated to Eq 4.4 as $t_2 << t_1$.

$$\frac{V_{HAR}}{I_{IN}} \approx \frac{2.L}{{t_1}^2.f_s} \tag{4.4}$$

This approximation does not affect the power transfer for high thermoelectric harvester voltages as the maximum voltage is about 200mV and t_2 is still much less than t_1 as can be seen from Eq 4.3. However, in case of high photovoltaic harvester voltages (0.6V for 2 photovoltaic harvesters in series under extremely bright light) and for V_{STORE} equal to 1.8V (an extreme case for this approximation), the converter impedance from Eq 4.2 differs from the approximate converter impedance given by Eq 4.4 by 33%. In this cases, as will be seen in the next sub-section, the internal power monitor and tracking loop automatically adjusts the converter impedance close to the appropriate optimal impedance for maximum power transfer. The approximation in Eq 4.4 basically amounts to ignoring the charge drawn from the harvester during ϕ_2 as it is significantly smaller than the charge drawn during ϕ_1 for boost converters with high conversion ratios. It must be noted that even for the buck-boost topology, which is used for the piezoelectric harvester, Eq 4.4 holds as charge is drawn from the harvester only during one phase, that is during ϕ_1 (when the inductor is charged) and not during ϕ_2 (when the inductor is discharged). The work in [64,88] derives a similar expression to (4), however under the assumption that t1 is equal to $1/(2f_s)$. Keeping t_1 independent of f_s gives us an extra flexibility to vary the impedance as will be seen later in Section 4.3. Eqs 4.1- 4.4 have been derived for traditional energy harvesting architectures. This expression can be extended to the dual-path architecture, where the primary and secondary converters individually present impedances given by Eq 4.5 and Eq 4.6 respectively.

$$\frac{V_{HAR}}{I_{IN,PRIM}} \approx \frac{2.L}{t_1{}^2.\alpha.f_s} \tag{4.5}$$

$$\frac{V_{HAR}}{I_{IN,SECON}} \approx \frac{2.L}{t_1{}^2.(1-\alpha).f_s} \tag{4.6}$$

where, α is the fraction of the power going into the primary converter and t_1 is kept the same for both the primary and secondary converters. The effective switching frequencies of the primary converter and secondary converter are $\alpha.f_s$ and (1-α).f_s respectively. As both these converters are in parallel, the total effective impedance that the harvester sees is still as in Eq 4.4. Therefore, by tuning the values of t_1 and f_s for a given L, the input impedance of the converter can be configured to the optimal setting and maximum power transfer can be obtained. In this implementation, for thermoelectric and piezoelectric harvesters, the power converter input impedances are configured to the desired values before power up as the impedance is known to be constant. However, for photovoltaic harvesters, an internal tracking loop adjusts the impedance such that it is close to its optimal setting at all times. It must be noted that the input capacitor, C_{HAR} as shown in Figure 4-6, is essential for setting the impedance. C_{HAR} acts as a temporary storage and supplies the large switching currents required during the power converter operation. Typically, the harvesters alone cannot supply the high switching current without causing droops in voltage.

4.2.3 Time-Based Power Monitor

The input power information is necessary for energy harvesting systems that require a feedback/tracking loop for optimal power transfer (e.g. from photovoltaic cells). In most cases, these systems employ ADCs and/or power inefficient current sensors to estimate the input power. In this sub-section, a time-based power monitor for a boost converter is proposed that utilizes the timing information present in the system to estimate input power. As seen before, by adjusting t_1 (time duration of ϕ_1 of a power converter), for a fixed frequency, it is possible to set the impedance of the

power converter to a desired value. However, for the proper operation of a power converter in DCM, it is also important to estimate the time duration of ϕ_2, which is t_2. Eq 4.3 in the previous section gives the t_2 pulse width necessary for the inductor current to be exactly equal to zero at the end of ϕ_2 for a boost converter in the Maximum Power Extraction stage for the traditional architecture. It must be noted that t_2 needs to be adjusted dynamically, as over the course of circuit operation, V_{HAR} or V_{STORE} might change. Direct computation of t_2 from Eq 4.3 is a power intensive process. A Zero Current Switching (ZCS) scheme has been proposed before [64,68,69] that estimates t_2 in a power efficient manner from the zero crossing of the inductor current for power converters in DCM. In this sub-section, it will be shown that the input power information can be extracted from the pulse width of t_2.

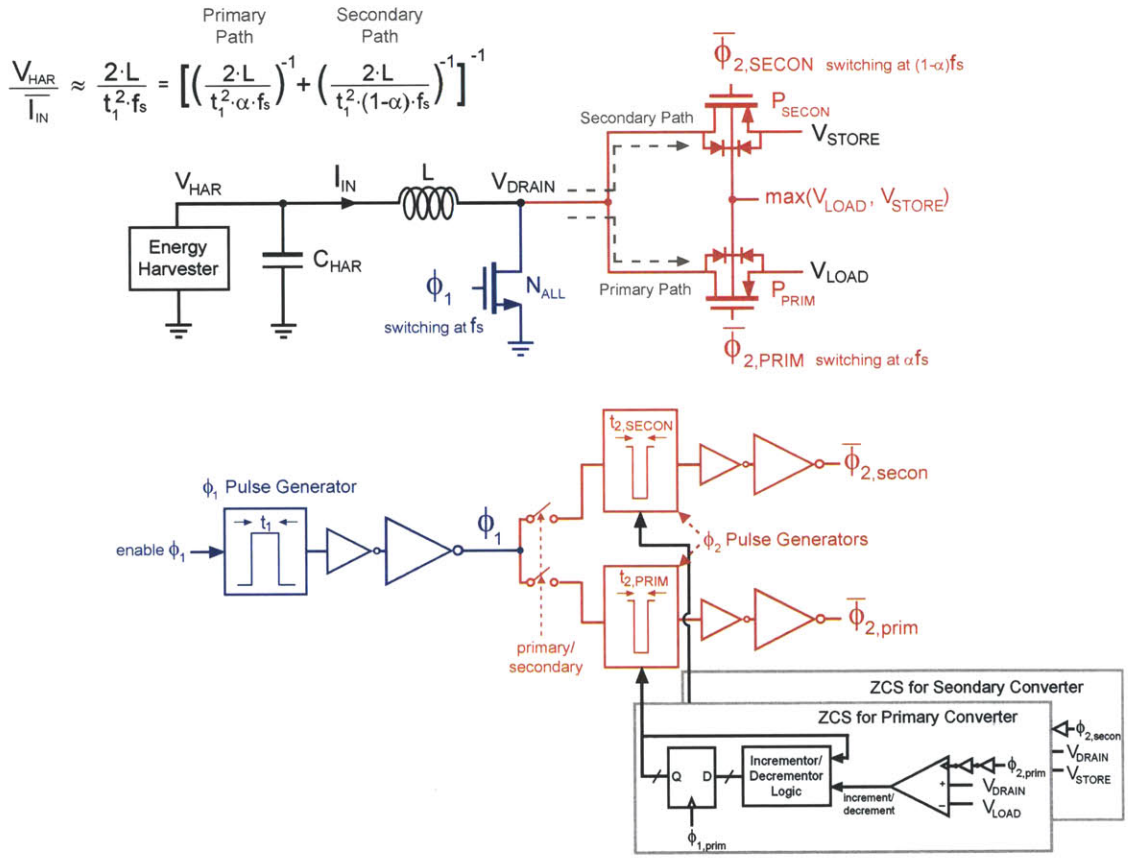


Figure 4-7: Impedance adjustment and ZCS in boost converters for dual-path architecture

In this work, the ZCS scheme has been extended to the dual-path architecture. Figure 4-7 shows two ZCS feedback loops used for primary and secondary converters in the context of the boost topology. During phase ϕ_1, transistor N_{ALL} is on and the inductor is energized. Depending on whether the primary or the secondary converter is enabled, either P_{PRIM} or P_{SECON} is turned on during ϕ_2, and energy is transferred to either V_{LOAD} or V_{STORE}. The ZCS circuits need to estimate the pulse widths of the gate drive signals, $t_{2,PRIM}$ and $t_{2,SECON}$, that are required by P_{PRIM} and P_{SECON}. The appropriate pulse widths are set by digitally tuning the ϕ_2 pulse generator blocks as shown in Figure 4-7. By comparing V_{DRAIN} with V_{LOAD} (and V_{STORE}), a one-bit feedback control signal is used that either increments or decrements the pulse width of $t_{2,PRIM}$ (and $t_{2,SECON}$). Therefore, the circuits converge to the pulse widths required for zero current switching. The following analysis shows that for boost converters with high conversion ratios, the $t_{2,PRIM}$ and $t_{2,SECON}$ pulse widths convey the input power information. Considering the input power to the energy harvesting system, we have Eq 4.7 as shown.

$$P_{IN} = V_{HAR}.I_{IN} \tag{4.7}$$

Also, by extending Eq 4.3 to the dual-path scenario, we get Eq 4.8 for the primary converter.

$$t_{2,PRIM} = \frac{V_{HAR}.t_1}{V_{LOAD} - V_{HAR}} \tag{4.8}$$

By using equations Eq 4.1,Eq 4.7 and Eq 4.8, we arrive at Eq 4.9.

$$P_{IN} \approx \frac{(V_{LOAD} - V_{HAR}).t_{2,PRIM}.V_{LOAD}.t_{2,PRIM}.f_s}{2.L} \tag{4.9}$$

By rearranging Eq 4.9, we get Eq 4.10

$$t_{2,PRIM} \approx \sqrt{\frac{2.L.P_{IN}}{V_{LOAD}.(V_{LOAD} - V_{HAR}).f_s}} \tag{4.10}$$

For a boost converter with high conversion ratios (where V_{LOAD} is 1.8V and

$V_{HAR,OPTIMAL}$ varies from 0.2V to 0.5V, in case of 1-2 photovoltaic cells in series), this expression can be approximated to Eq 4.11

$$t_{2,PRIM} \approx \frac{1}{V_{LOAD}} \cdot \sqrt{\frac{2.L.P_{IN}}{f_s}} \tag{4.11}$$

As can be seen from Eq 4.11, $t_{2,PRIM}$ can be used to estimate the power supplied by the harvester if f_s and V_{LOAD} are kept constant. A similar expression can be obtained for $t_{2,SECON}$. By extending Eq 4.11 to $t_{2,SECON}$, it can be observed that $t_{2,SECON}$ will be inversely proportional to V_{STORE} which is higher than V_{LOAD} in this implementation. Therefore, for better resolution of input power, $t_{2,PRIM}$ has been used. In this design, a time resolution of 25-30ns is used for $t_{2,PRIM}$. It must be noted that even though the analysis here has been done for a boost converter with high conversion ratio, Eq 4.11 holds even for the buck-boost topology.

4.2.4 Using Power Monitor Output in MPPT for Photovoltaic Cells

The approach of monitoring the input power by observing $t_{2,PRIM}$ is utilized for the MPPT loop implemented in power converters for photovoltaic cells as shown in Figure 4-8. In order to accurately estimate the input power, a block averaging operation is performed on $t_{2,PRIM}$ before using it as a input power monitor. This is done to remove the variations in $t_{2,PRIM}$ due to the ripple on V_{LOAD} and V_{PV}. Usually, after estimating the power, the MPPT loops are required to vary a control-circuit parameter [89–92] (e.g. duty cycle, frequency, pulse widths, etc) so that the system can be configured to extract power optimally from the photovoltaic cell irrespective of the light intensity. In this work, the effective impedance of the boost converters (primary and secondary) is dynamically adjusted so that $t_{2,PRIM}$, the estimator of input power, is maximized. This is done by tuning t_1 (time duration of ϕ_1 of the boost converter). Since the MPPT is inherently a slow tracking loop, a tunable divided down version of primary converter clock (α.fs) is used as the sub-hertz MPPT clock

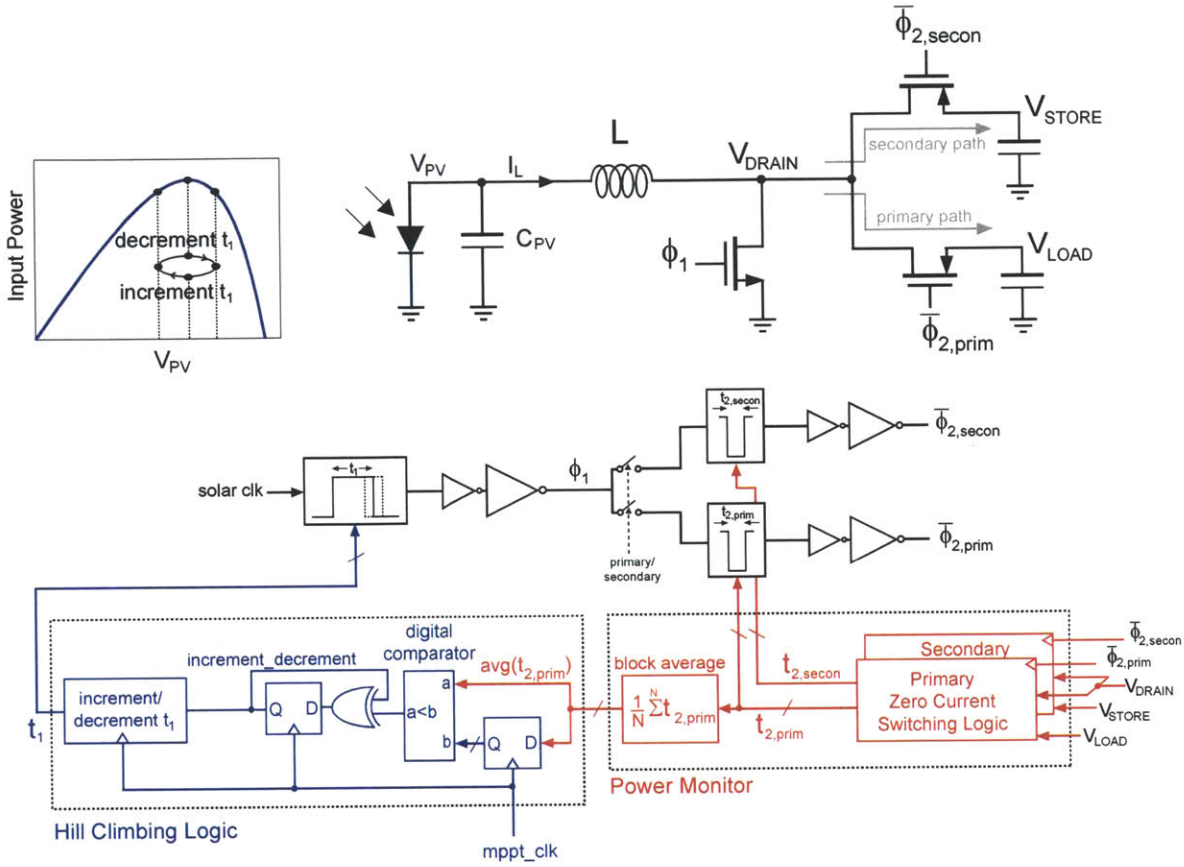


Figure 4-8: MPPT loop for solar boost converters with Hill Climbing Logic (or Perturb and Observe) and Power Monitor, inductor sharing switches and body bias circuits not shown for clarity

(mppt_clk). The logic for Hill-Climbing (or Perturb and Observe) involves comparing the output of the power monitor in the current mppt_clk cycle with the previous cycle output. An increment_decrement signal is used to perturb t_1. If the current cycle power monitor output is greater than the previous cycle output, t_1 is perturbed (incremented or decremented) in the same direction as before, else the direction of perturbation is changed using an EX-OR gate acting as a controlled inverter. By employing this scheme, the MPPT loop converges to impedances (or t_1) that are closest to optimum impedance (or t_1) required for maximum power extraction. At steady state, the system continuously monitors the input power and oscillates between three states, the center one being closest to the maximum power point. Figure 4-9 shows

the corresponding flow diagram used to implement MPPT. It must be noted that all the control circuits in this design are powered off V_{LOAD}. Hence, even at no load, the primary converter has to be active to supply the control circuit power, although at a much lower frequency (effective switching frequency of αf_s having low α). This will reduce the how frequently of power monitor output is compared but will not affect the average power extracted from the photovoltaic cell. Therefore, even at no load, the power monitor is active tracking the maximum power point. As can be seen, this method does not depend on empirical relations for the maximum power point voltage as in the fractional open circuit MPPT scheme [89,91] or on current sensors [90,91,94] that maybe power inefficient or may not be very accurate.

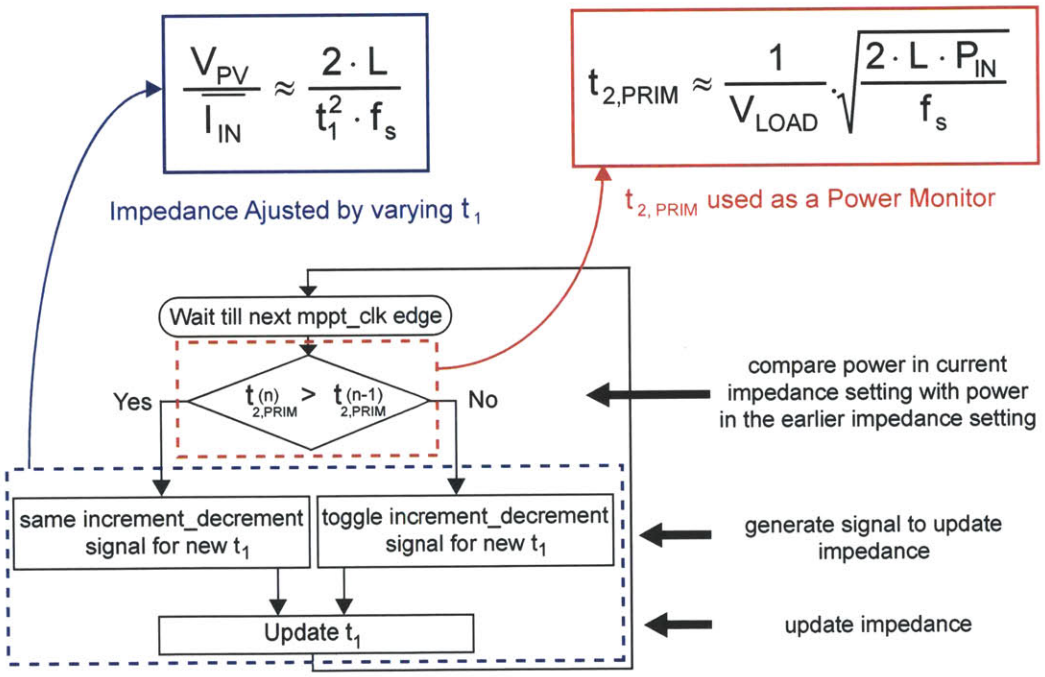


Figure 4-9: Flow-diagram for MPPT loop

It must be noted that the proposed power monitor can also be used to shut down the power converters when the input power from the harvester is too low. Although this feature has not been implemented in this design, it is envisioned that in a wireless sensor node, the μ-Controller in the system would be used to disable all the pulses (ϕ_1 and ϕ_2) to the power converters when it detects that the corresponding power

monitor output is lower than a threshold. It can then periodically wake up the power converters to check if the harvester power is back up again.

4.3 Inductor Sharing

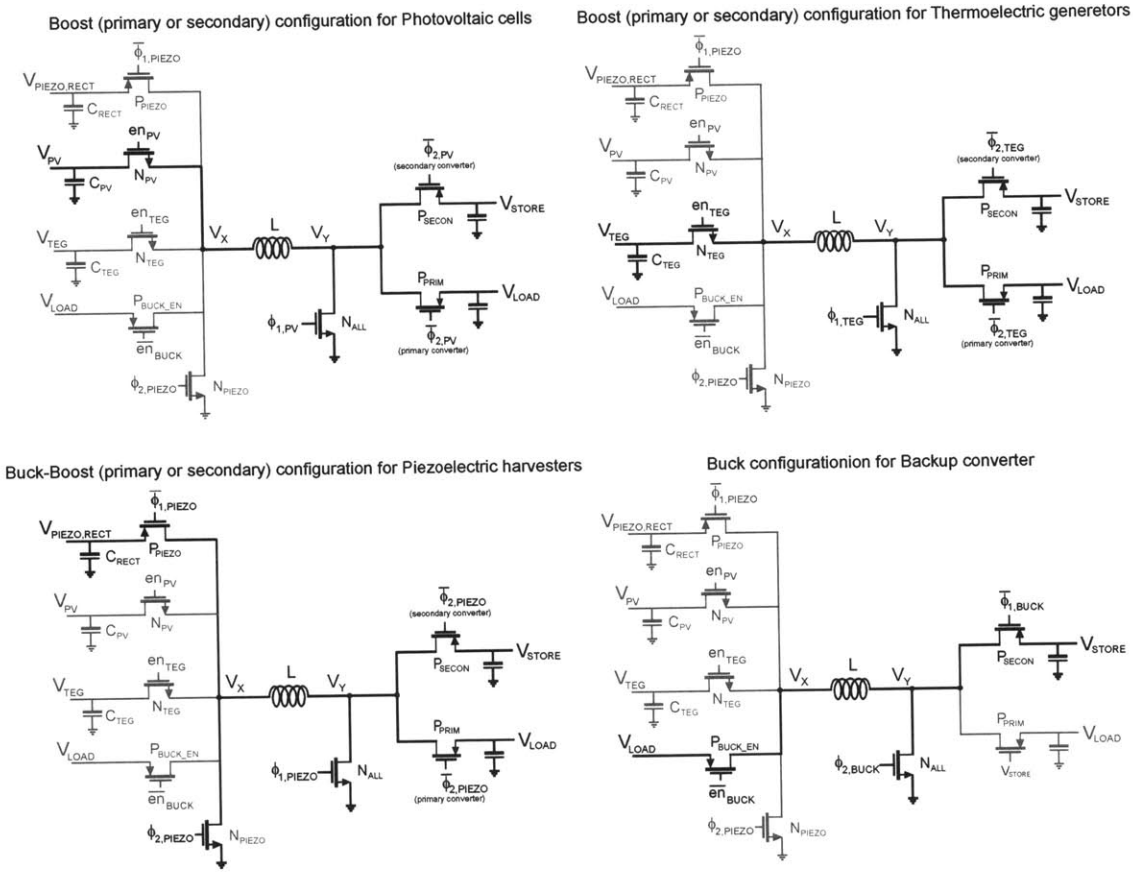


Figure 4-10: Reconfigurable switch matrix, body bias circuits for P_{PRIM}, P_{SECON} and P_{BUCK} not shown for clarity. For P_{PRIM} and P_{SECON}, analog multiplexers and comparators are used select the higher of V_{LOAD} and V_{STORE} and for P_{BUCK}, the higher of V_{LOAD} and V_X is dynamically selected

In order to reduce the number of external off-chip components, a previous energy harvesting system [87] has looked into an inductor sharing scheme. In this work too, a single inductor has been time shared among all the dc-dc converters implemented. Until this section, all the transistor level schematics in this chapter have ignored the

inductor sharing details for simplicity. In this section, the circuit details of inductor sharing will be highlighted. In this design, a switch matrix has been used that can be reconfigured into all the power converters required in this system. This is shown in Figure 4-10. The number of inductors has been reduced to one from four (one of each harvester, another for the backup stage buck converter). Since all the converters have been designed to work in DCM, these circuits are switched such that the idle time between switching phases (time between ϕ_2 of nth switching cycle and ϕ_1 of n+1th switching cycle) for a given converter is utilized for the ϕ_1 and ϕ_2 switching phases of other converters. This has been conceptually illustrated by the timing diagram shown in Figure 4-11.

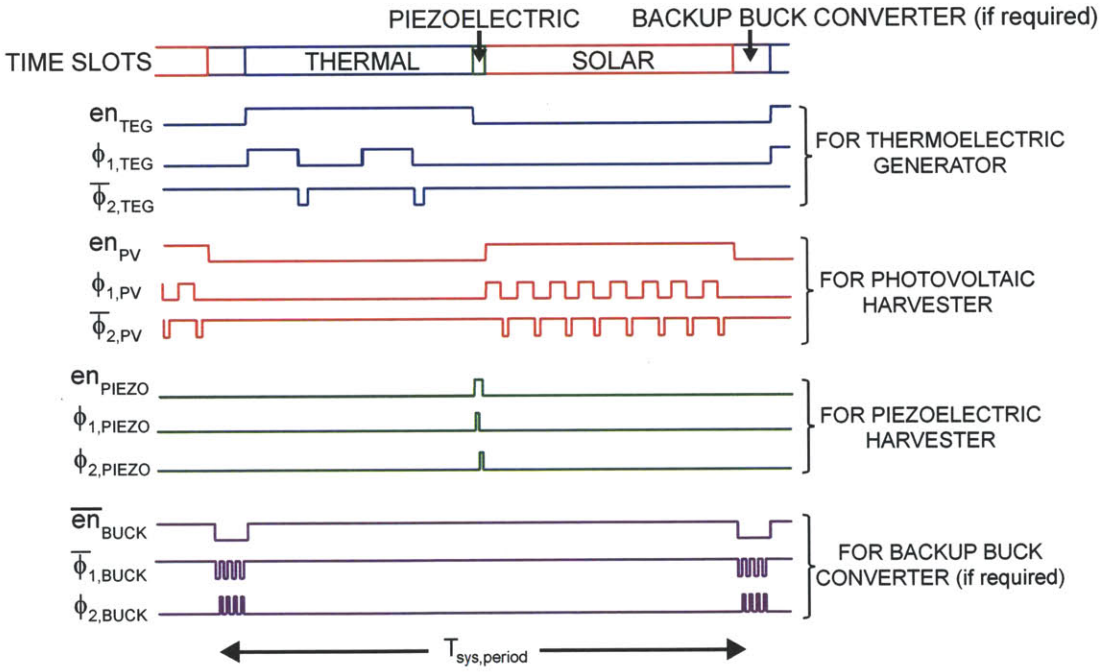


Figure 4-11: Timing diagram for inductor utilization

When the switch matrix is configured as a boost converter for photovoltaic cells, the switches of the power converters used for thermoelectric and piezoelectric harvesters are off and these converters are in their idle modes. It must be noted that this idle time is necessary for converters in DCM and should not be viewed as inefficiency in power transfer. The impedance the converters present to the harvesters,

as given by Eq 4.4 in the previous section, is over a complete switching cycle. During the converters switching phases, ϕ_1 and ϕ_2, power is instantaneously extracted from the capacitors (C_{PV}, C_{TEG}, C_{RECT} shown in Figure 4-10) parallel to the harvesters. During the converter idle time, these capacitors get charged by the harvester. In this way, on average the converter maintains the impedance necessary for maximum power transfer. Therefore, even with time multiplexing the inductor, the system can provide the optimal impedances necessary for maximum power transfer from individual harvesters all at the same time. The only overhead in power transfer in this scheme comes from the additional conduction and switching losses due to the inductor sharing switches in series with the inductor.

Effective harvester impedances vary from a few Ωs to 100s of kΩs as shown in Table 4.1. In order to meet the impedance requirements, it is possible to fix the switching frequency (f_s in Eqs 4.1- 4.6 and Eqs 4.9 to 4.11 of all the energy harvesting converters (to say $1/T_{sys,period}$), decide on the time-slots for inductor access by different converters and tune t_1 according to Eq 4.4 in previous section. However, this methodology is not desirable since the power converters operating at different voltage and input impedances would have the same switching frequency, hence resulting in individual sub-optimal efficiencies. It is preferred to have a design where each converter has a different switching frequency depending on corresponding voltage levels and impedance requirement for optimal efficiency. Here, the effective frequencies for different converters have been made different by having multiple ϕ_1 and ϕ_2 pulses during a single time-slot as shown in Figure 4-11. Therefore, the effective switching frequency for a converter is the system clock frequency divided by the number of switching pulses within the created time-slots. In this implementation, an internal pattern generator circuit is used to create these time-slots within a $T_{sys,period}$ of 256μs (corresponding to the system clock f_s in Section 4.1). The power converters used for the thermoelectric harvester have an effective switching frequency of 7.8kHz as it has 2 switching cycles within $T_{sys,period}$. The power converters for photovoltaic harvesters have an effective frequency of 31.25kHz with 8 switching cycles within $T_{sys,period}$. The overhead due to inductor sharing in these cases comes from the additional switches

N_{TEG} and N_{PV}. In order to minimize these losses, the en_{TEG} and en_{PV} signals are kept high for the entire duration for which these converters are active thereby reducing the switching losses in N_{TEG} and N_{PV} as shown in Figure 4-11. This allows us to increase the widths of these switches. Since piezoelectric harvesters have the highest effective source impedance, the power converter of these harvesters require a single switching cycle within $T_{sys,period}$ resulting in an effective switching frequency of 3.9kHz. As the inductor is switched in and switched out every cycle, this converter effectively works in the buck-boost mode. The backup converter (a buck converter here) has 4 switching cycles during its time-slot within the $T_{sys,period}$, resulting in an effective frequency of 15.6KHz. When enabled, the backup converter occupies its time-slot and delivers power to the load along with the primary converters (of all the harvesters). When the primary converters are able to meet the load requirement, the backup converter remains idle and does not occupy its time-slot.

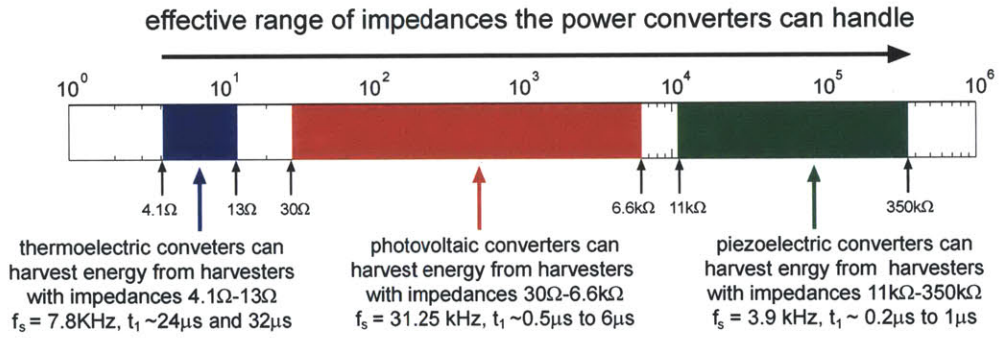


Figure 4-12: Range of impedance covered by the internal pattern generator for $T_{sys,period}$ of 256μs

With the effective switching frequency and the ϕ_1 on time of each individual harvester, the system can cater for a wide range of impedances simultaneously as shown in Figure 4-12. In this implementation, the time-slots for accessing the inductor are hard-coded in the internal pattern generator logic. This implementation also allows us to reconfigure the time-slots by external sources. In a sensor node, it is envisioned that the μ-Controller in the system can be used to set the time-slots if

required.

4.4 Experimental Results

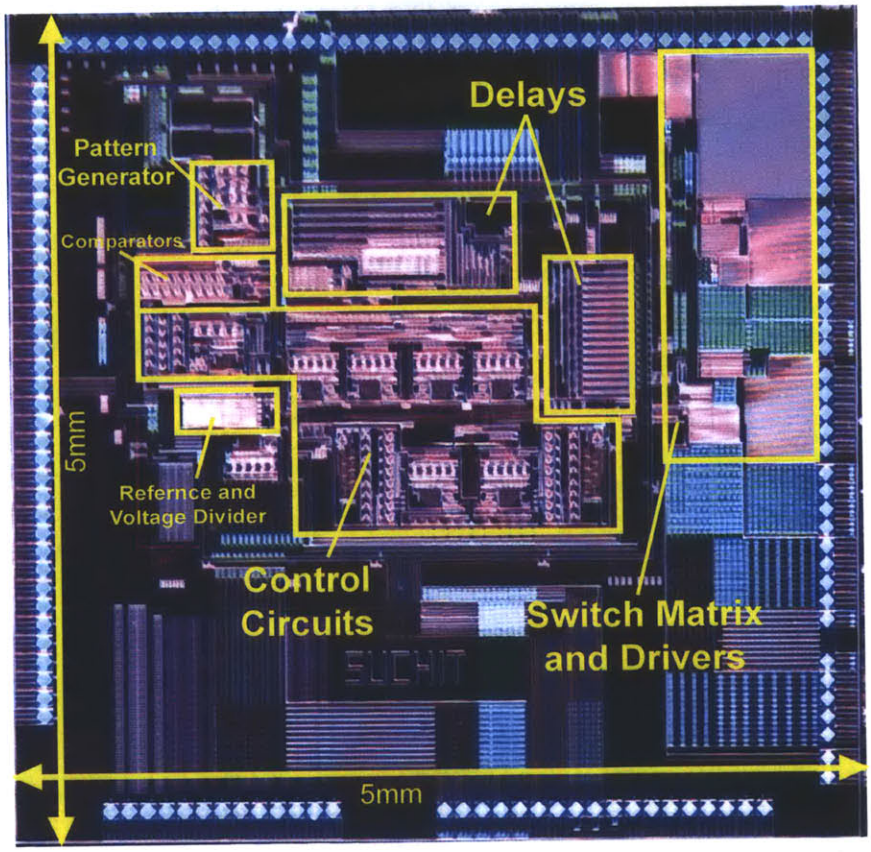


Figure 4-13: Die Microphotograph of Multi-Input Energy Harvesting IC

The power switches and control circuits were implemented in a 0.35μm CMOS process. The die micro-photograph is shown in Figure 4-13. The test board has been shown in Figure 4-14. The system has been tested with photovoltaic cells [83], thermoelectric harvesters [84] and piezoelectric harvesters [85] as input sources along with super-capacitors and/or 3.3V Lithium batteries as the intermediate storage elements (for V_{STORE}). However, for input and output power measurements, Keithley 2400 source meters have been used. A 22μH inductor along with an output capacitor of 15μF (at V_{LOAD}) was used. In order to suppress the 3.9KHz ripple on the harvester

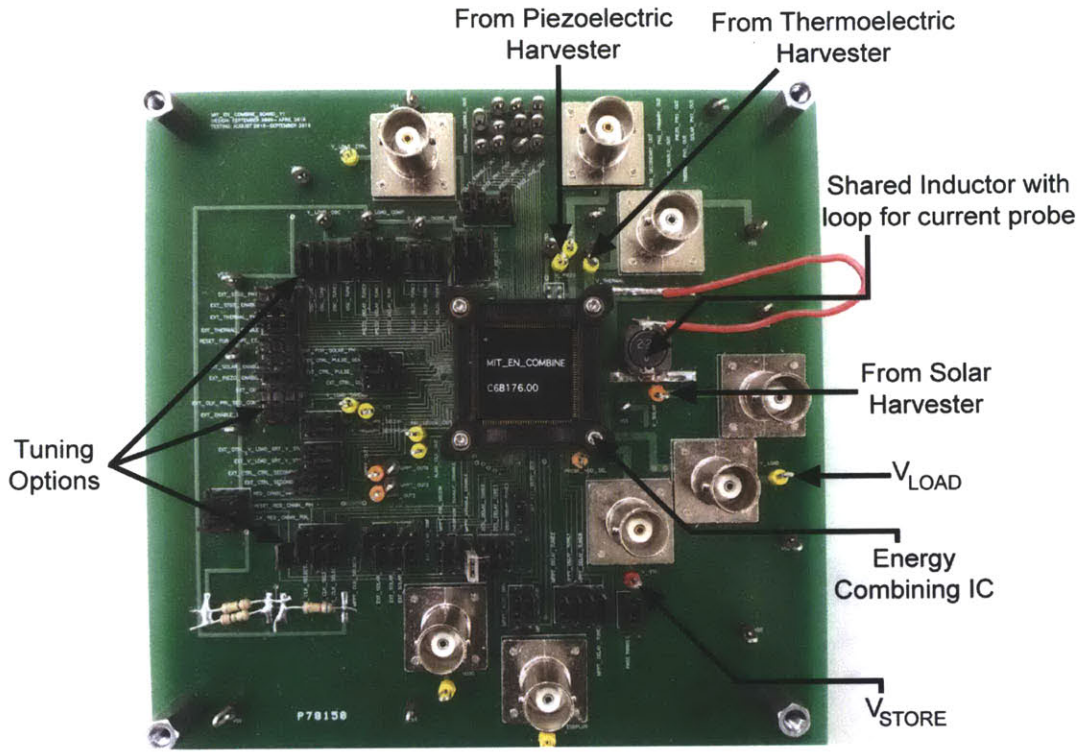


Figure 4-14: Picture of the Test Board used to test the Multi-Input Energy Combining System

voltages, input capacitors- 47μF for photovoltaic, 94μF for thermoelectric and 1μF for piezoelectric (at the output of the rectifier) were used. The measured input ripple was less than 10mV for the photovoltaic cell, less than 13mV for thermoelectric generator and less than 20mV for the piezoelectric harvester.

4.4.1 Measured Efficiencies

Figure 4-15 shows the measured efficiencies for all the power converters implemented with and without inductor sharing. All the measurements have been made with the control circuits running off the 1.8V V_{LOAD} and with the time-slots for inductor access as shown in Figure 4-11. For these efficiency measurements, V_{STORE} is set to 1.8V. The total output power is measured as the sum of the power to V_{LOAD} and V_{STORE}. The photovoltaic primary/secondary boost converter achieves a peak

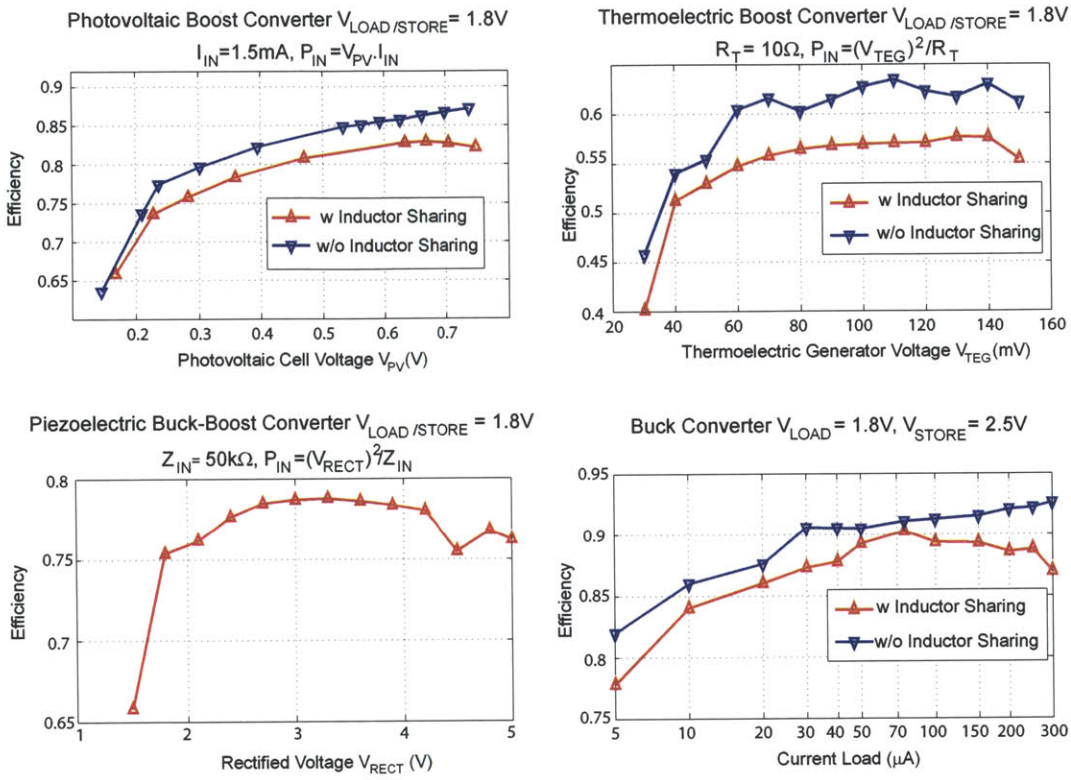


Figure 4-15: Measured efficiencies of photovoltaic boost, thermoelectric boost, piezoelectric buck-boost primary/secondary converters and backup buck converter

efficiency of 83% with inductor sharing and 87% without sharing. The thermoelectric primary/secondary boost achieves a peak efficiency of 58% with inductor sharing and about 64% without sharing. The piezoelectric buck-boost primary/secondary converter has a peak efficiency of 79%. The backup buck converter has an efficiency varying from 78% to 90% throughout the load range with inductor sharing and 82% to 92% without sharing. The dual-path scheme essentially bypasses this converter when the primary converters are able to meet the load requirement depending on the ambient conditions. Therefore, this provides a peak efficiency improvement of 11-13% with inductor sharing and 11-12% without sharing. If we consider an average case where the energy harvesters are able to meet the load requirement for half of the time, the dual-path scheme provides an average improvement of approximately 5-7%. Therefore, as a system solution, this design is able to compensate for the losses

due to inductor sharing by using the dual-path architecture. Most of the efficiency overhead from inductor sharing arises form the additional power FETs introduced. In this implementation, 60-70% of the estimated conduction losses are due to the FETs, the rest are from the inductor's resistance.

4.4.2 Dual-Path Control Transients

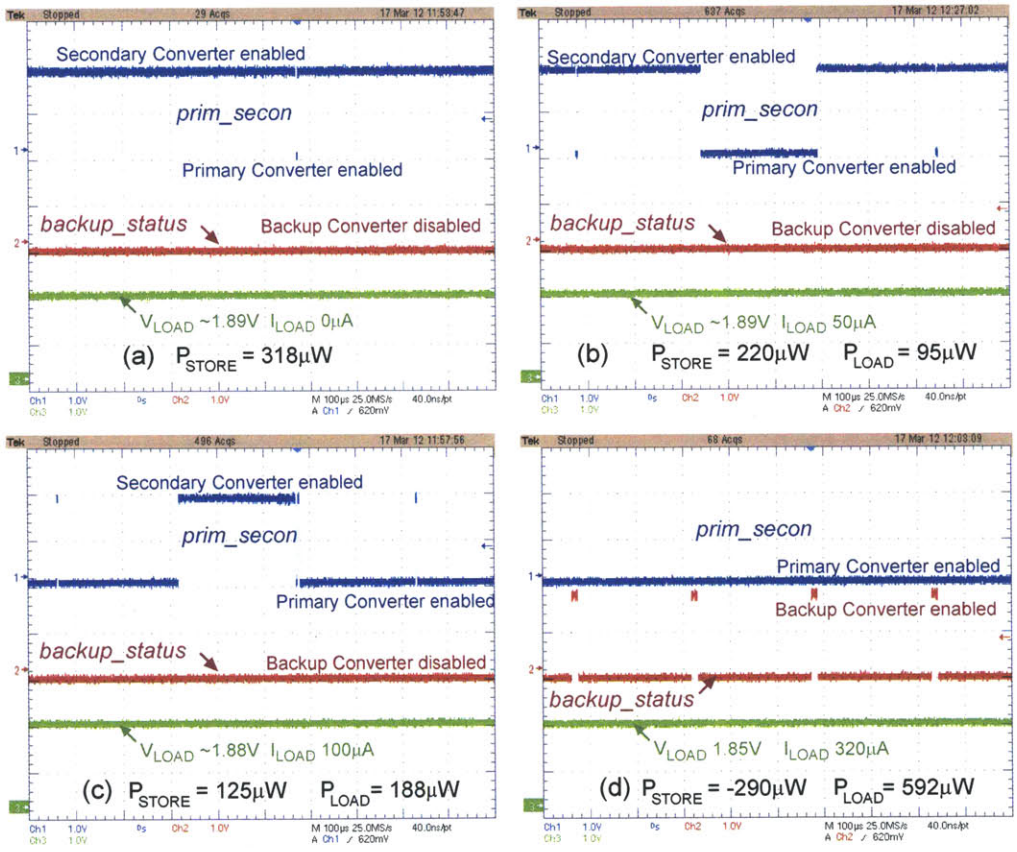


Figure 4-16: Transients of the dual-path architecture showing- (a) secondary converter active most of the time for I_{LOAD} $0\mu A$, (b) secondary converter active more frequently than primary converter for I_{LOAD} $50\mu A$, (c) primary converter active more frequently than secondary converter for I_{LOAD} $100\mu A$, (d) primary and backup converters active for I_{LOAD} $320\mu A$

Figure 4-16 shows the measured transient waveforms for the dual-path control in the context of photovoltaic harvesters. These measurements were made with 2 photovoltaic cells in series under about 590lux light intensity having a voltage of about

0.4V. Figure 4-16 shows the control signals prim_secon (low- primary converter enabled, high- secondary converter enabled) and backup_status (high- backup converter enabled). Figure 4-16(a) shows the condition when the I_{LOAD} is 0μA. During this condition, the system spends most of the time operating the Secondary converter and thus, charging the V_{STORE} node. The primary converter is enabled only to supply power to the control circuits and the gate drivers internal to the circuit that run off V_{LOAD}. Figure 4-16(b) and Figure 4-16(c) show the conditions when the input power is able to meet the load requirements of 50μA and 100μA. However, in the former case, the secondary converter is active for most of the time and in the later case, it is the primary converter that is active more often. Figure 4-16(d) shows the condition when the load is much higher that the power from the harvester. During this time, the backup converter is enabled along with the primary converter. It can be seen that the difference between the regulated output V_{LOAD} from Figure 4-16(a) and Figure 4-16(d) is only 40mV.

4.4.3 MPPT Transients

Figure 4-17 shows the MPPT functionality. As mentioned before in Section 4.2, the MPPT circuit oscillates about three states, the state at the center being closest to the optimal power point of the photovoltaic cell. Figure 4-17(a) shows the long term photovoltaic harvester voltage under normal in-door lighting of 600lux having a V_{MPP} of 0.205V (2 cells in parallel each 4x5.15cm^2). Under this condition the circuit was delivering 300μW of harvested power. Figure 4-17(b) shows the dynamic performance under intentional shading. As seen, the photovoltaic harvester voltage comes back to the steady state after being disturbed. Figure 4-17(c) shows the performance when two photovoltaic cells (each 3x2.5cm^2) are placed in series under 1500lux while delivering 260μW of harvested power. For the system designed, a peak tracking efficiency (closeness to peak power point, as defined in [92]) of 96% was obtained. The entire control circuits including the MPPT logic consume about 5μW.

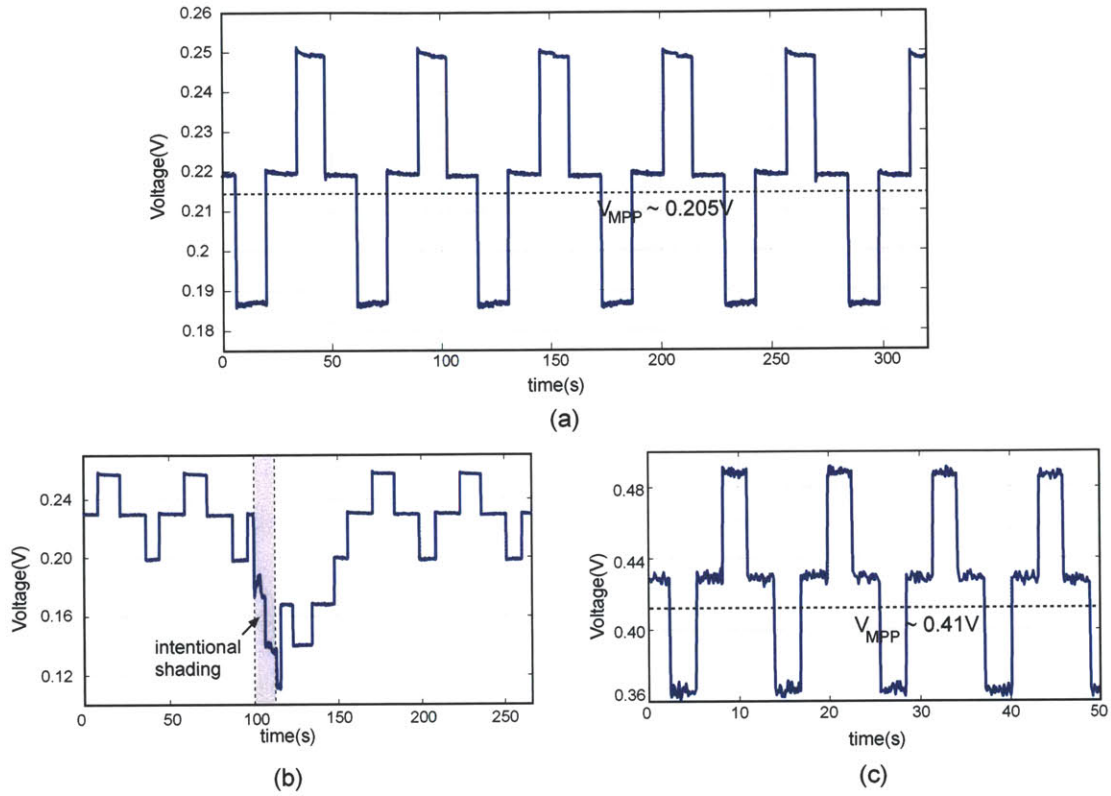


Figure 4-17: Photovoltaic harvester voltages with MPPT enabled- (a) Tracked voltage for 2 cells (4x5.15cm^2) in parallel, (b) Dynamic response of the MPPT circuit after intentional shading, (c) Tracked voltage for 2 cells (3x2.5cm^2) in series. Note that since these results have been obtained for long term voltage measurement, the voltage ripple has not been captured in these plots. The ripple on the oscilloscope was measured to be <10mV for these states

4.4.4 Inductor Sharing Transients

Figure 4-18 shows the switching transient waveforms of all the converters implemented utilizing the same inductor. The time-slots assigned to each power converter are according to Figure 4-11. As mentioned before, by setting the ϕ_1 duration and the effective switching f_s of the individual power converters, the wide range of impedances is realized. In Figure 4-18, the power converters for thermoelectric harvesters are tuned for about 6Ω input impedance. For photovoltaic, the converter impedance is set to around 1.4 kΩ and for piezoelectric converters, it is tuned to around 50 kΩ.

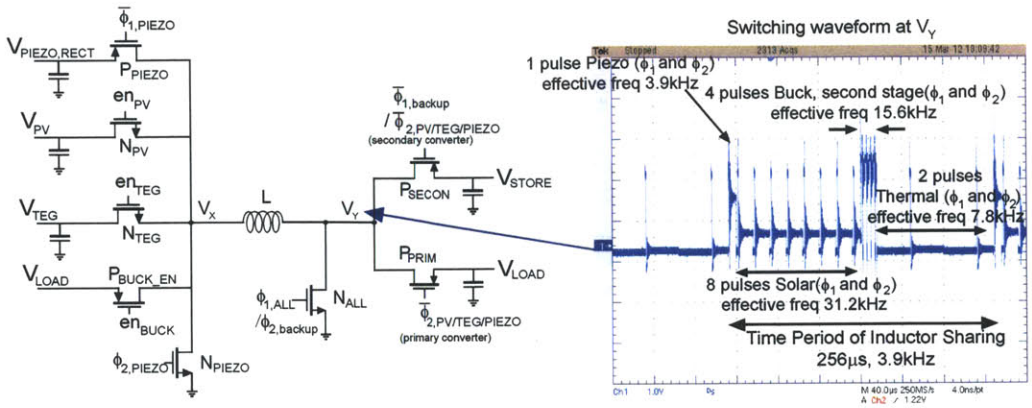


Figure 4-18: Inductor sharing transient showing all the power converters utilizing the single inductor

This figure also shows the backup buck converter enabled switching at effectively 15.6kHz. The measured input voltages are 60mV, 400mV and 2.5V from thermoelectric, photovoltaic and piezoelectric harvesters (after the rectifier) respectively. The output voltage was regulated to 1.88V and the V_{STORE} was at 2.3V. The measured t_1 and t_2 pulse widths in the primary converter for thermoelectric harvester are 32μs and 800ns. For the photovoltaic harvester, the t_1 and t_2 pulse widths are 1.86μs and 470ns. For the piezoelectric harvester, the measured t_1 and t_2 pulse widths are 504ns and 590ns. Finally, for the buck converter, the measured t_1 and t_2 pulse widths are 1μs and 170ns.

4.4.5 Zero Current Switching Waveforms

Figure 4-19 shows the Zero Current Switching waveforms for converters used to harvest energy from photovoltaic cells. Since the pulse widths of $t_{2,PRIM}$ and $t_{2,SECON}$ are digitally controlled, the Zero Current Switching circuit creates pulse widths that are either just more (for Current Ramp 1) than or just less (for Current Ramp 2) than the ideal pulse width required for inductor current to be exactly zero at the end of the switching phase $\phi 2$ as described in [64, 68, 88]. Figure 4-19(a) shows these two states. It must be noted that since, for MPPT, the $t_{2,PRIM}$ is time averaged,

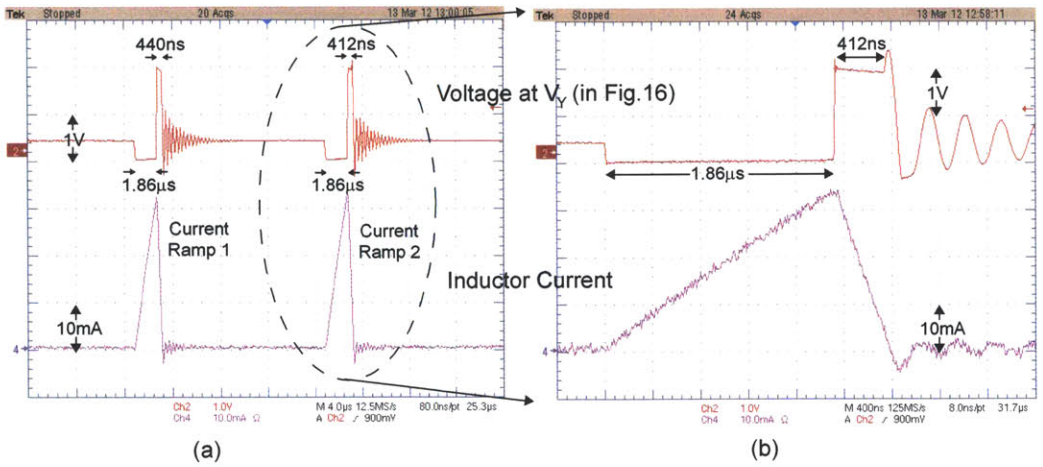


Figure 4-19: Zero Current Switching Waveforms, (a) two states-when t_2 is just more than and just less than the ideal pulse width required for exact ZCS, (b) zoomed in waveforms for when t_2 is just less than ideal pulse width required for exact ZCS

this does not affect the tracking loop. Figure 4-19(b) zooms in on the second state when the pulse width of $t_{2,PRIM}$ is slightly less than the ideal pulse width required for Zero Current Switching. As the inductor current has to go to zero, the parasitic diode across the PMOS (P_{PRIM} in this case) gets activated discharging the residual inductor current to V_{STORE} (actually higher of V_{LOAD} and V_{STORE} as shown in Figure 4-7, here $V_{STORE}>V_{LOAD}$). This causes the voltage at V_Y (Refer to Figure 4-18) to instantaneously rise up by a forward diode voltage.

4.4.6 Load Transient Response and Output Voltage Ripple

Figure 4-20(a) and 4-20(b) show the response of the system when a load step of 300μA was applied to the V_{LOAD} (being regulated to 1.88V). A ripple of 25mV is obtained when the load is 300μA and ¡15mV for the no load condition. For this measurement, the input voltages from each of the harvesters were 50mV, 400mV and 2V from thermoelectric, photovoltaic and piezoelectric harvesters respectively. As can be seen from Figure 4-20, the regulated voltage is slightly higher during no load condition. This is when the primary converter is regulating the output. During a load transient, the primary converter alone is not able to regulate V_{LOAD}. This backup converter to

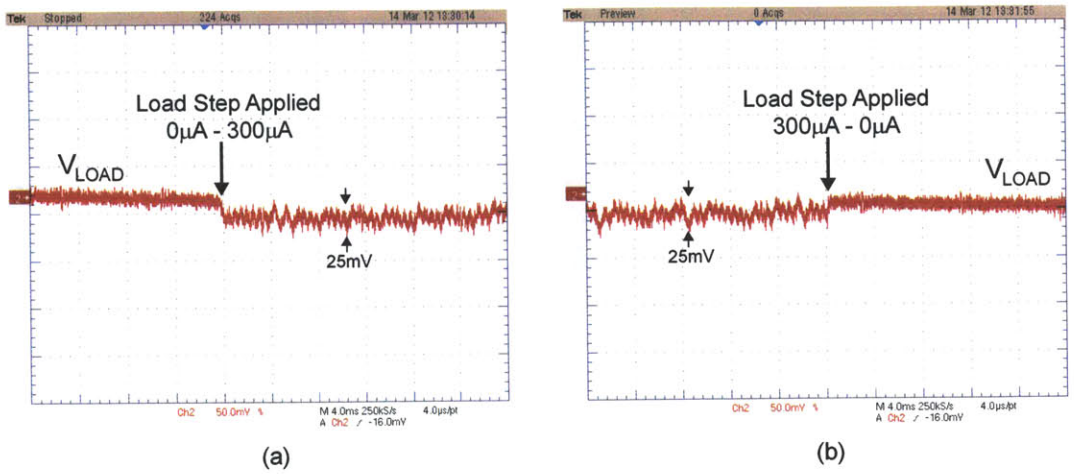


Figure 4-20: Load Transient on V_{LOAD}, (a) Load Step of 0-300μA, (b) Load Step of 300-0μA

get triggered which along with the primary converter now regulates V_{LOAD}.

4.4.7 Comparison with State-of-Art Energy Harvesting Systems

Table 4.2 shows a comparison of the energy combining system with previously published energy harvesting designs. It can be seen that the performance is similar to the individual state of art energy harvesting systems. However, this system provides diversity in energy source and hence reliability with no extra off-chip components. It must be noted that the efficiency comparison has been made for the individual maximum power extraction stages (boost for photovoltaic and thermoelectric and buck-boost for piezoelectric) to be consistent with all the previously published designs. The dual-path advantage is obtained after this stage. Therefore, while considering overall end to end efficiency, as discussed earlier, the system presented here has 11-13% higher peak efficiency and 5-7% higher average efficiency.

Table 4.2: Comparison with State-of-Art Energy Harvesting Systems

Parameters	JSSC 2011	JSSC 2010	JSSC 2010	ISSCC 2011	This work
Energy Source	Thermoelectric	Vibration	Thermoelectric	Photovoltaic	Photovoltaic, Thermoelectric and Vibration
Input dc voltage to power converters (after rectification if required)	25mV - 0.100V with thermoelectric generator resistance	2-5V	20mV - 0.240V	0.5-2V	20mV - 0.16V Thermal 0.15 - 0.75V Solar 1.5 - 5V Piezoelectric
Architecture	Two-Stage from harvester to charger and load	charger	charger	charger	*Dual-Path* from harvester to charger and load
In-built Maximum Power Extraction	Yes	Externally Tunable	No	Yes	Yes
Peak Tracking Efficiency for Photovoltaic	NA	NA	NA	80%	96%
Maximum Output Power	300μW	70μW	200μW	10mW	1.3mW Thermal Boost, 2.5mW Photovoltaic (5-10mW with increased switching freq), 200μW Piezoelectric
Peak Efficiency of power converters	58% for Thermal Boost	87% for Vibration Buck	~65% for Thermal Boost for comparable conversion ratios (20-30)	87% for Solar Boost	64% Thermal Boost, 87% Photovoltaic Boost, (without inductor sharing) 58% Thermal Boost, 83% Photovoltaic Boost, 79% Piezoelectric Buck-Boost (with inductor sharing)

4.5 Conclusions

This chapter highlights the role of digital control in increasing system efficiency and reducing form factor. First, a dual-path architecture, enabled by digital control, is proposed. This technique reconfigures the power train such that depending on the load conditions, the number of converters between the energy harvester and the load can be reduced. This helps improve the peak efficiency by 11-13% as compared to traditional power converter architectures used in energy harvesting systems. Second, digital control circuits have also been used to time share a single inductor for combining energy from multiple harvesting sources. The number of inductors has been reduced to one from four (one of each harvester, another for the backup stage buck converter). Inductor sharing has efficiency overhead (3-6%) but is preferred over having multiple inductors in such a system as it provides a cost effective solution.

Chapter 5

LED Driver with Gallium Nitride FET and Burst Mode Controller

With the advent of high brightness LEDs [95], the lighting industry is expected to see a significant growth in the near future. Higher reliability with superior efficacies in terms of lumen/Watt (Figure 5-1 [95]) have made LEDs potentially more cost effective than CFLs and ideal candidates for next generation lighting systems. Future milestones set by the DOE [95], EnergyStar [96] and other regulatory bodies indicate that increased efficacies and better power conditioning can lead to substantial decrease in overall energy consumption and reduction in greenhouse gas emissions.

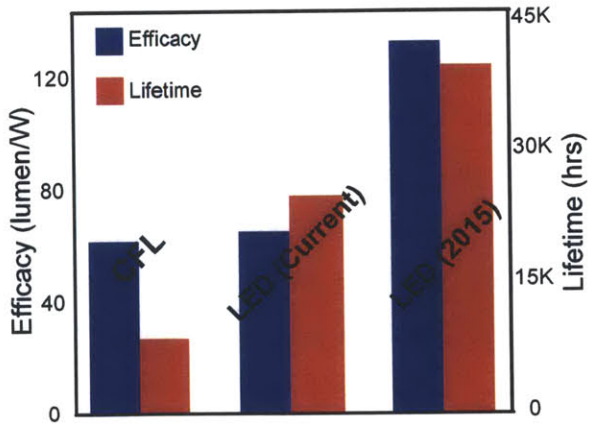
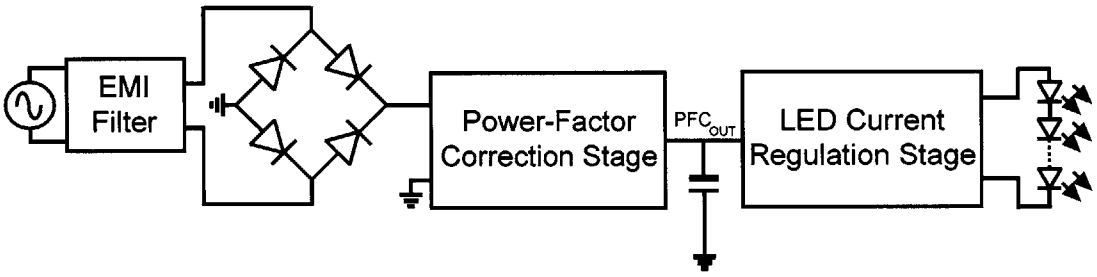
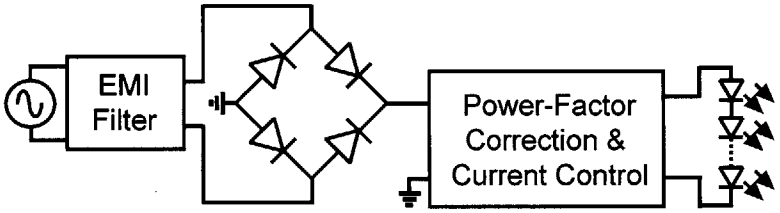


Figure 5-1: Comparison of LEDs with CFL in terms of lumen/Watt and Lifetime [95]

However, for LEDs to get the expected acceptance and for them to completely replace CFL bulbs, the power conversion circuits within the LED drivers need to be miniaturized so that the entire driver electronics can be fit inside the traditional bulb socket. This can be achieved by operating the power converters at high switching frequencies so that the passive components in these converters can be miniaturized. Moreover, this needs to be done while preserving the power converter efficiency.



(a) Two Stage LED driver architecture



(b) Single Stage LED driver architecture

Figure 5-2: LED Driver Architectures: Two stage [97, 98, 105] and Single stage architectures [100, 107]

The power converters in offline LED drivers, along with efficient power conversion, need to perform two additional functions- control the LED current and perform power factor correction (PFC). A class of two-stage LED drivers is [97, 98, 105] is usually used to perform these functions separately. The first stage interfacing with the AC input, along with the EMI filter and rectifier, performs PFC. The PFC stage output capacitor provides an intermediate storage. The second stage transfers energy stored in the PFC stage output capacitor to the LEDs and tightly regulates the current as shown in Figure 5-2(a). These converters, although have a very small output

current ripple, suffer with degraded efficiency due to two power conversion stages. Another class of LED drivers [100, 107] use a single power conversion stage that performs PFC as shown in Figure 5-2(b). These perform better in terms of efficiency as compared to the two stage architecture. Some circuitry is generally included to adjust the average LED current thereby incorporating dimming into the PFC. Due to the absence of the intermediate storage, these converters have a 120Hz (twice the ac line frequency) current and voltage ripple at the output. Table 5.1 summarizes the LED driver design approaches. Some studies [99] carried out show that the 120Hz flicker in single stage LED drivers is inconsequential and falls in the range that is unobservable to most humans. For these reasons, the single stage architecture has been focused on in this work.

Table 5.1: Summary of LED driver design approaches

	Two-Stage Architecture	Single-Stage Architecture
References	[97, 98, 105]	[100, 107]
Efficiency	Limited due to two stages of power converters	Tends to be higher than two-stage drivers due to single power converter
Output Ripple	Low current ripple as second stage tightly regulates the output current whereas the first stage performs PFC	Tends to have high current ripple at 120Hz as the first stage performs only PFC. The ripple is not suppressed by the converter.

Among single stage LED drivers, the inverted buck converter [106, 107] shown in Figure 5-3 is a popular topology used in commercial offline LED drivers. Ease in driving a ground referenced FET and the fact that the LEDs need not be ground referenced make this a frequently used topology. The low side FET does not require high voltage level shifters that would otherwise be required for a buck converter. The converter operation is very similar to that of the traditional buck converter. Figure 5-3 shows the converter operation in two phases- Φ_1 and Φ_2. During Φ_1, the FET is turned on allowing current to flow from the V_{RECT} node, through the LED, filter

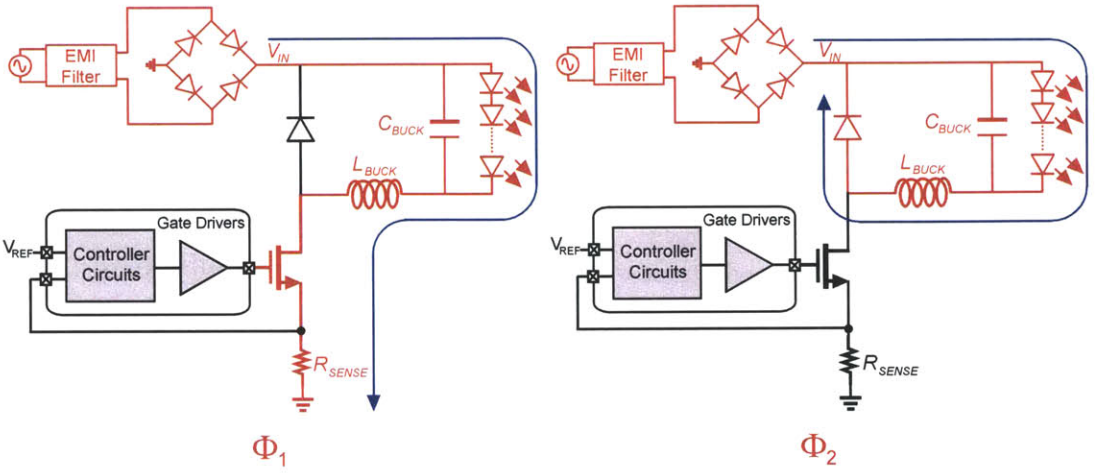


Figure 5-3: Traditional Inverted Buck LED Driver [106, 107]

inductor and the FET to ground. During Φ_2, the FET is turned off causing the diode to carry the inductor current back to the V_{RECT} node as shown in Figure 5-3. This may be followed by an idle time if the converter is in the DCM. For this topology, the average inductor current is equal to the LED current. Previous works [100, 103] have also operated the inverted buck converter in the Critical Conduction Mode (CRM) which is at the boundary of CCM and DCM. It must be noted that LED drivers regulate the output current instead of the output voltage. The current is usually estimated by using a sense resistor (R_{SENSE}). By comparing this with a reference voltage, the FET current, and hence the LED current, can be controlled [107].

It is desired to operate the LED driver at high frequencies to scale down the size of the passives. However, for such power converters, the maximum switching frequency is limited by switching losses due to the output capacitance of the FET along with the ac winding and core losses in the inductors [121]. Without careful design and implementation, high frequency operation may cause the aforementioned losses to be prohibitively high. Further, the sense resistor introduces additional conduction losses. In this work, efforts have been made to minimize the these losses while still operating the power converter at high switching frequency.

5.1 Power FETs offered by Wide Bandgap Semiconductors

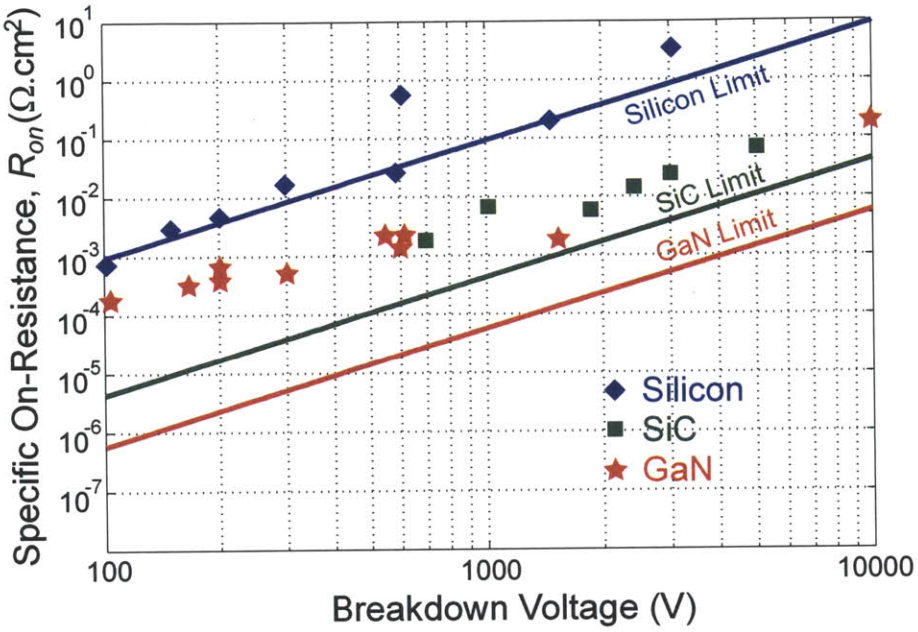


Figure 5-4: Comparison of Specific On-Resistance between Si, SiC and GaN (adopted from [110–113])

Emerging technologies like Silicon Carbide (SiC) [109] and Gallium Nitride (GaN) [102, 103, 109] have enabled power FETs with superior capabilities compared to Silicon (Si) FETs. Due to the wide bandgaps of these materials, the devices can sustain a higher electric field (critical electric field E_{crit}) making it possible to operate them at much higher voltages than Silicon devices. Thus, for the same breakdown voltage, V_{BR}, the wide bandgap semiconductor FETs have much lower on-resistances. Before quantifying the advantages of these superior devices, we should look at the metrics that can be used to compare these technologies. Figure 5-4 (adopted from [109–113]) shows the specific-on-resistances of Si, SiC and GaN FETs as a function of the breakdown voltage (maximum drain-source voltage). The parallel lines represent the limits set by the material properties and the data-points represent some state-of-art devices reported in literature (adopted from [110–113]). The

technology limit depends on device properties like carrier mobilities, critical electric fields, etc and is given by Eq 5.1 [109] as shown.

$$R_{ds,onspecific} = \frac{4.{V_{BR}}^2}{\epsilon_o.\epsilon_r.\mu.{E_{crit}}^3} \tag{5.1}$$

Here, μ represents the mobility, ϵ_o is the permittivity of free space and ϵ_r is the relative permittivity of the material. Table 5.2 shows the material properties of Si, SiC and AlGaN-GaN (state of art GaN devices are usually formed by a AlGaN-GaN heterostructure, this provides the high carrier mobility) that are used to evaluate Eq 5.1. We can see from Figure 5-4 that the reported GaN devices are still one to two orders of magnitude off from the GaN limit. This difference can be attributed to the contact resistance between metal and AlGaN [103]. Particularly at low breakdown voltages, the contact resistances form a larger fraction of the overall on-resistance of the device. However, it is expected that with further advancements, future GaN devices will be closer to the GaN limit [104].

Table 5.2: Comparison of Si, SiC and AlGaN-GaN Material Parameters [109]

	Silicon	Silicon Carbide	Gallium Nitride
Mobility (cm^2/V.s)	1450	900	2000
Critical Field (MV/cm)	0.25	2.2	3.5
Permittivity	11.8	9.7	9.0

Based on Eq. 5.1, a figure-of-merit- Baliga Figure-of-Merit (BFoM) has been proposed in literature [114]. It is defined as $\epsilon_r.\mu.{E_{crit}}^3$ (proportional to the denominator of Eq. 5.1). However, BFoM does not provide a fair comparison for high switching frequency power converters as it does not account for device capacitances. Another figure-of-merit (FoM) that accounts for the device capacitances has been proposed- the Huang New Material Figure-of-Merit (HMFoM) [115]. This metric is defined as $\sqrt{R_{ds,ON}.Q_G}$ where Q_G is the gate charge of the device. Since the gate

capacitance of a power transistor is non-linear and depends on the device's operating condition, the most accurate technique of accounting for the switching loss due to the gate capacitance is to take the gate charge into consideration [116]. Further, due to the square root operation, the HMFoM gives the estimate of the minimum losses due to the device. Table 5.3 compares the FoMs of Silicon, Silicon Carbide and Gallium Nitride technologies. It can be observed that Gallium Nitride and Silicon Carbide technologies have superior FoMs. This makes it possible to design power converters with smaller form-factors, higher efficiency and reliability with these wide bandgap devices.

Table 5.3: Comparison of Si, SiC and AlGaN-GaN normalized FoMs (material properties from [109], FoM definitions from [114, 115]

	Silicon	Silicon Carbide	Gallium Nitride
BFoM [114]	1	500	2400
HMFoM [115]	1	7.75	16.9

5.2 LED Driver Architecture

The GaN FET in the power train can potentially enable high frequency operation with high efficiency. However, in order to operate the power converter at frequencies in the range of 10MHz and higher, the power converter topologies that absorb the parasitic capacitors and inductors into the power train need to be used. In this work (details of [117]), the Quasi-Resonant topology [118, 119] is adopted for a near-Zero Voltage Switching (ZVS) Inverted Buck Converter as shown in Figure 5-5. The resonant circuits, formed by L_R, C_{OUT} and C_D, help achieve near-ZVS. Inductor- L_{BUCK} and capacitor- C_{BUCK} form the LC filter of the inverted buck converter. The power train is switched at 11MHz. The detailed operation of the Quasi-Resonant Inverted Buck will be discussed in Section 5.3 of this chapter. In this work, low permeability, low loss magnetic cores described in [121] have been used to make custom high frequency

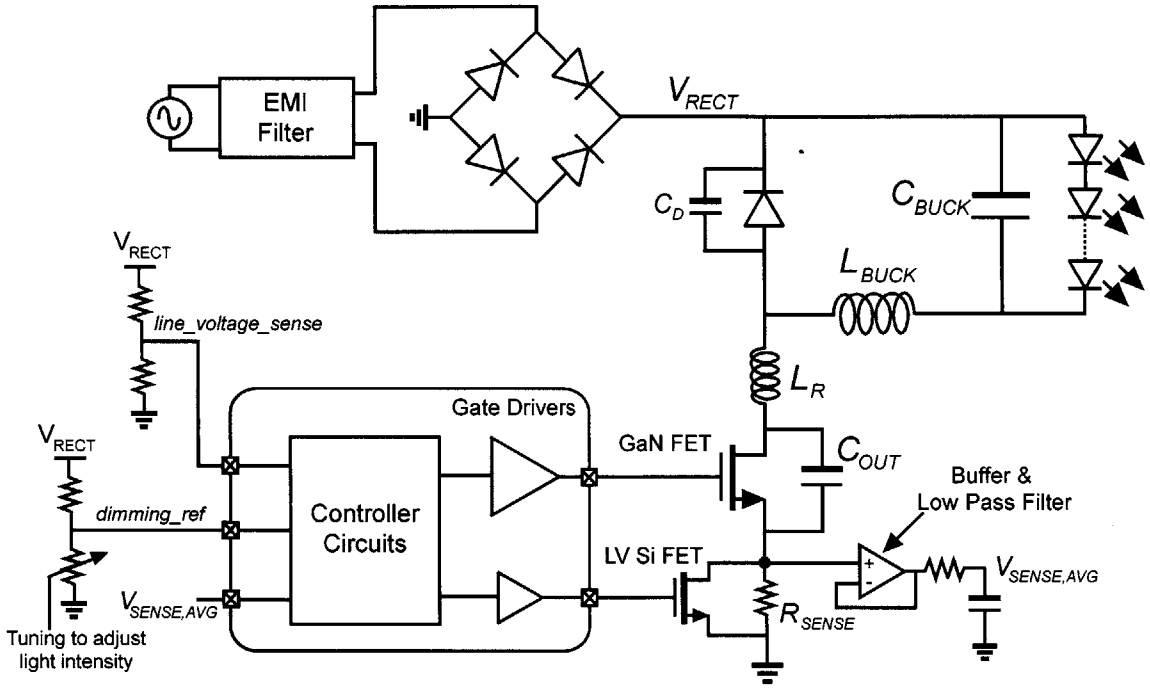


Figure 5-5: Architecture of the LED Driver

inductors L_R (850nH at 11MHz) and L_{BUCK} (12μH at 11MHz). Efforts have been made to minimize inter-winding capacitance and high frequency resistance due to skin effect. The details of the custom inductors will be discussed in Section 5.5 of this chapter. This power train is used a drive a string of 20 LEDs in series. On the input side, a full bridge rectifier and an EMI filter (4th order- two cascaded LC stages, similar to [105]) are used to interface with the ac input voltage.

The LED current (light intensity) is controlled by using a Burst-Mode controller with a 68KHz burst frequency. Two prototypes have been designed, one with a FPGA control and discrete drivers and another with a custom IC consisting of the controller logic and drivers designed using a 0.35μm CMOS process with 3.3V/15V voltage handling capability. The FET current (also the input current to the power train) is sensed using a sense resistor R_{SENSE}. Here, in order to reduce the conduction loss in R_{SENSE}, the sensing operation is duty-cycled, that is only for one in 16 system (or burst) cycles is the current allowed to flow through R_{SENSE}. For the remaining cycles, the resistor is bypassed by using a low voltage Silicon FET (LV Si FET, hence

a low $R_{ds,on}$ switch). By averaging the voltage across R_{SENSE}, the FET current can be estimated and controlled. The detailed operation of the controller will be discussed in Section 5.4 of this chapter.

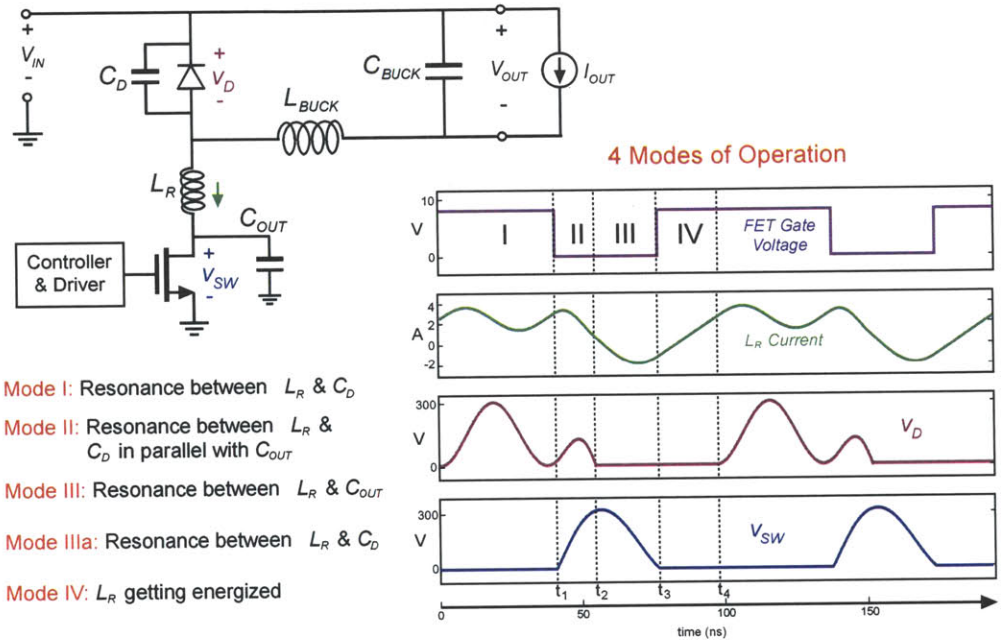


Figure 5-6: Quasi-Resonant Inverted Buck based on [118, 119] for near-Zero Voltage Switching (LV Si FET not shown for simplicity)

5.3 Quasi-Resonant Inverted Buck Converter Operation

In Quasi-Resonant inverted-buck converters, resonant circuits formed by L_R, C_{OUT} and C_D are made to resonate such that just prior to turning on the FET, the voltage at the drain terminal comes close to ground as shown in Figure 5-6. This minimizes the switching loss due to C_{OUT} and enables operation at frequencies in the range of 10MHz and higher. It must be noted that this comes at the cost of increased rms currents along with higher $R_{ds,ON}$ of the FET it has to handle a higher voltage stress in this topology as compared to a non-resonant topology. Nevertheless, quasi-resonant

operation enables high frequency operation [118] which is the main objective of this work. The detailed analysis of Quasi-Resonant buck-converters has been done in [119]. The same analysis and equations can be applied for an inverted-buck converter since the inverted-buck converter follows the same principles as the traditional buck converter. The converter's resonant operation can be broken down to 4 modes. Since the L_{BUCK} is chosen much greater than L_R, for the analysis, L_{BUCK} can be replaced by a current source, I_{OUT}. The following explanation will walk through each of the modes. It must be noted that in this analysis, all capacitors have been assumed to be linear. In practice, both C_{OUT} and C_D are non linear and the measured waveforms would deviate from the analytical equations. However, these equations give the basic understanding behind the Quasi-Resonant converter operation.

5.3.1 Mode I: Resonance between resonant inductor and diode capacitor

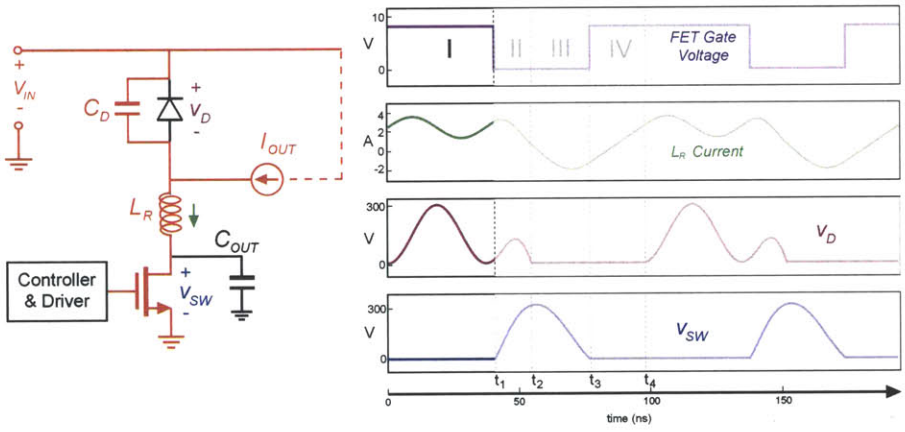


Figure 5-7: Mode I of Quasi-Resonant operation, based on [118, 119]

Figure 5-7 shows the Mode I of operation. This mode begins by considering a particular time instant when the FET is on and the entire I_{OUT} current flows through L_R and the FET. The diode is just turned off as the current through it just goes to zero. This sets an initial condition of v_D equal to 0V. Figure 5-7 shows the paths of current flow in red. The resonant circuit formed by C_D and L_R resonates. The

diode voltage, v_D and current through L_R can be solved by using Eqs 5.2 and 5.3 in conjunction with the initial conditions:- $v_D(0)$=0V and i_L=I_{OUT}.

$$i_L = C_D \frac{dv_D}{dt} + I_{OUT} \tag{5.2}$$

$$V_{IN} = v_D + L_R \frac{di_L}{dt} \tag{5.3}$$

By solving these, we obtain Eqs 5.4 and 5.5 where $\omega_D = \frac{1}{\sqrt{L_R.C_D}}$ and $Z_D = \sqrt{\frac{L_R}{C_D}}$.

$$v_D(t) = V_{IN}.[1 - cos(\omega_D t)] \tag{5.4}$$

$$i_L(t) = I_{OUT} + \frac{V_{IN}}{Z_D}.sin(\omega_D t) \tag{5.5}$$

5.3.2 Mode II: Resonance between resonant inductor with FET and diode capacitors

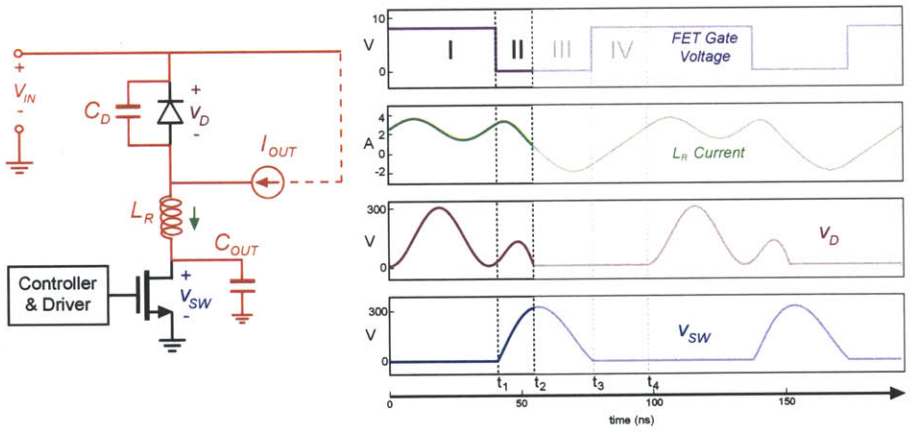


Figure 5-8: Mode II of Quasi-Resonant operation, based on [118, 119]

Mode I is terminated when the FET is turned off. This results in a resonant circuit consisting of C_D, C_{OUT} and L_R. The following differential equations (Eqs 5.6 and 5.7) can be used to solve for the diode voltage (v_D), FET drain voltage (v_{SW}) and inductor current (i_L).

$$i_L = C_D \frac{dv_D}{dt} + I_{OUT} = C_{OUT} \frac{dv_{SW}}{dt} \tag{5.6}$$

$$V_{IN} = v_D + L_R \frac{di_L}{dt} + v_{SW} \tag{5.7}$$

Assuming that the time duration of Mode I was t_1, the initial conditions for v_D and i_L can be obtained from Eqs 5.4 and 5.5 respectively. Let these be $v_D(t_1)$ and $i_L(t_1)$. Since the FET is just turned off, the initial condition for v_{SW} is 0V. By solving Eqs 5.6 and 5.7 along with the initial conditions, we obtain Eqs 5.8, 5.9 and 5.10 where $C_{eff} = \frac{C_{OUT}.C_D}{C_{OUT}+C_D}$, $\omega_{SD}=\frac{1}{\sqrt{L_R.C_{eff}}}$ and $Z_{SD}=\sqrt{\frac{L_R}{C_{eff}}}$.

$$\begin{aligned} v_D(t) &= v_D(t_1) + [V_{IN} - v_D(t_1)].[1 - cos\{\omega_{SD}.(t-t_1)\}].\left[\frac{C_{OUT}}{C_{OUT}+C_D}\right] \\ &+\frac{1}{\omega_{SD}.C_D}.\left[i_L(t_1) - \frac{I_{OUT}.C_{OUT}}{C_{OUT}+C_D}\right].sin\{\omega_{SD}.(t-t_1)\} \\ &-\frac{I_{OUT}.(t-t_1)}{C_{OUT}+C_D} \end{aligned} \tag{5.8}$$

$$\begin{aligned} i_L(t) &= \frac{V_{IN} - v_D(t_1)}{Z_{SD}}.sin[\omega_{SD}(t-t_1)] + \frac{I_{OUT}.C_{OUT}}{C_{OUT}+C_D} \\ &+\left[i_L(t_1) - \frac{I_{OUT}.C_{OUT}}{C_{OUT}+C_D}\right].cos[\omega_{SD}(t-t_1)] \end{aligned} \tag{5.9}$$

$$\begin{aligned} v_{SW}(t) &= \frac{C_D.[V_{IN} - v_D(t_1)]}{C_D + C_{OUT}}.[1 - cos\{\omega_{SD}(t-t_1)\}] + \frac{I_{OUT}.(t-t_1)}{C_{OUT}+C_D} \\ &+\frac{1}{C_{OUT}.\omega_{SD}}.\left[i_L(t_1) - \frac{I_{OUT}.C_{OUT}}{C_{OUT}+C_D}\right].sin[\omega_{SD}(t-t_1)] \end{aligned} \tag{5.10}$$

Mode II gets terminated when either v_{SW} or v_D reaches 0V. If v_{SW} does not get to 0V, v_D eventually goes to 0V due to the presence of a negative linear term in Eq 5.8. Depending on whether v_D or v_{SW} reaches 0V first, the converter enters either Mode III or Mode IIIa. Lets assume for now that v_D reaches 0V and the converter

enters Mode III at time t_2. The alternative mode Mode IIIa will be discussed later in the section.

5.3.3 Mode III: Resonance between resonant inductor and FET capacitor

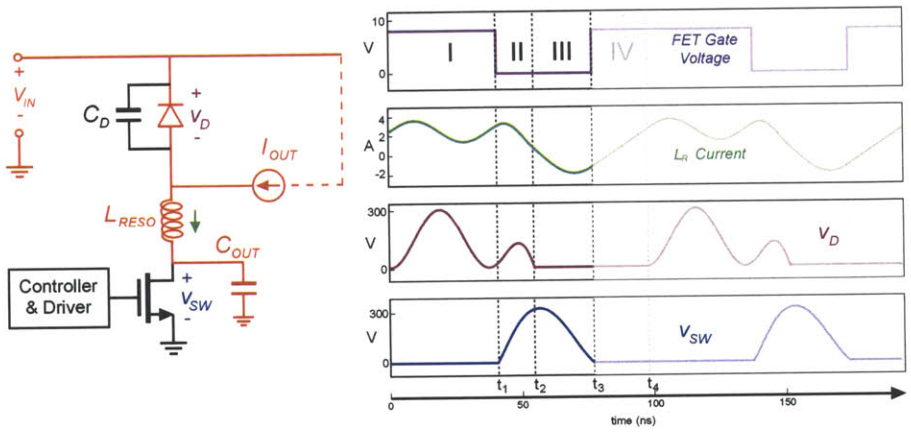


Figure 5-9: Mode III of Quasi-Resonant operation, based on [118, 119]

When the converter enters Mode III, the diode is turned on but the switch remains off. Figure 5-9 shows the corresponding circuit in red along with the relevant current and voltage waveforms. The resonant circuit formed by C_{OUT} and L_R resonates till the drain voltage, v_{SW}, comes close to 0V after which the FET is turned on again. Eqs 5.11 and 5.12 can be used to solve for the i_L and v_{SW}. The initial conditions for solving can be determined from the Mode II equations derived before. Let these be $i_L(t_2)$ and $v_{SW}(t_2)$.

$$V_{IN} = L_R \frac{di_L}{dt} + v_{SW} \tag{5.11}$$

$$i_L = C_{OUT} \frac{dv_{SW}}{dt} \tag{5.12}$$

By using these equations and the initial conditions, Eqs 5.13 and 5.14 can be obtained for i_L and v_{SW} where $\omega_S = \frac{1}{\sqrt{L_R \cdot C_{OUT}}}$ and $Z_S = \sqrt{\frac{L_R}{C_{OUT}}}$

$$i_L(t) = i_L(t_2).cos\left\{\omega_S.(t-t_2)\right\} - \frac{v_{SW}(t_2) - V_{IN}}{Z_S}.sin\left\{\omega_S.(t-t_2)\right\} \tag{5.13}$$

$$\begin{aligned} v_{SW}(t) &= V_{IN} + i_L(t_2).Z_S.sin\left\{\omega_S.(t-t_2)\right\} \\ &\quad + [v_{SW}(t_2) - V_{IN}].cos\left\{\omega_S.(t-t_2)\right\} \end{aligned} \tag{5.14}$$

5.3.4 Mode IV: Energizing resonant inductor

Mode III ends when the FET drain voltage, v_{SW}, reaches close to 0V. This is the time when the FET is turned on again. The work in [119] considers only ZVS cases, i.e. when v_{SW} actually reaches 0V. In this work, however, cases where exact ZVS is not achieved and v_{SW} goes to values close to 0V (near-ZVS) are also permitted. Exact ZVS often results in higher circulating currents. By allowing the converter to function in near-ZVS, the efficiency of the converter may not get substantially affected since the rms currents are lowered at the small cost of switching loss due to the imperfect ZVS. For this reason, the near-ZVS cases are also permitted in this design.

During this mode, both the FET and diode are on resulting in V_{IN} being across L_R. Therefore, i_L can be described by Eq 5.15, assuming i_L is equal to $i_L(t_3)$ at the beginning of this mode. This goes till i_L equals I_{OUT} after which Mode IV terminates and Mode I begins.

$$i_L(t) = i_L(t_3) + \frac{V_{IN}.(t-t_3)}{L} \tag{5.15}$$

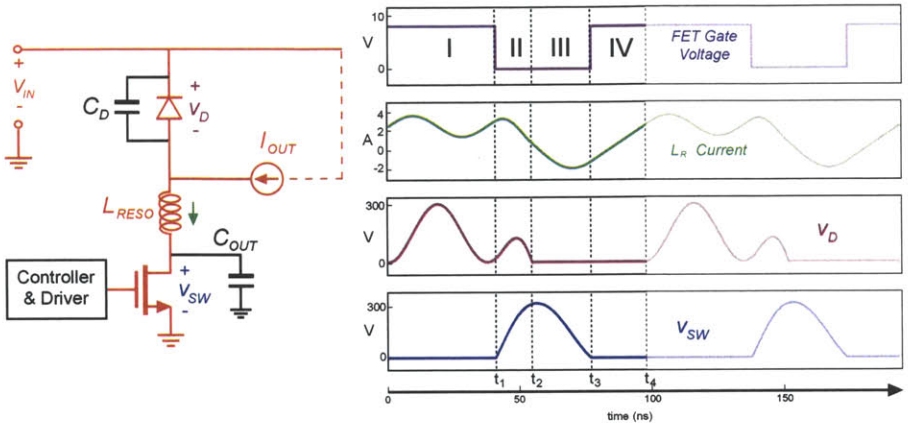


Figure 5-10: Mode IV of Quasi-Resonant operation, based on [118, 119]

5.3.5 Analysis with Mode IIIa: Resonance between resonant inductor and diode capacitor

Until now, we have assumed that for ZVS (or near-ZVS), the v_D reaches 0V before v_{SW} at the end of Mode II. However, depending on the relative values of C_D (parasitic or intentional [119]) and C_{OUT}, the converter may resonate such that v_{SW} reaches 0V before v_D. At this time instant, the switch is turned on and the converter enters an alternative mode-Mode IIIa. During this mode, C_D and L_R resonate with till v_D reaches 0V. Eqs 5.3 and 5.2 described before dictate the dynamics of the circuit in this mode. These equations along with initial conditions $i_L(t_3)$ and $v_D(t_3)$ give is us Eqs 5.16 and 5.17, where $\omega_D = \frac{1}{\sqrt{L_R.C_D}}$ and $Z_D = \sqrt{\frac{L_R}{C_D}}$.

$$\begin{aligned} v_D(t) &= [i_L(t_3) - I_{OUT}].Z_D.sin\{\omega_D.(t-t_3)\} \\ &\quad +[v_D(t_3) - V_{IN}].cos\{\omega_D.(t-t_3)\} + V_{IN} \end{aligned} \tag{5.16}$$

$$\begin{aligned} i_L(t) &= I_{OUT} + [i_L(t_3) - I_{OUT}].cos\{\omega_D.(t-t_3)\} \\ &\quad -\frac{v_D(t_3) - V_{IN}}{Z_D}.sin\{\omega_D.(t-t_3)\} \end{aligned} \tag{5.17}$$

After v_D reaches 0V, Mode IIIa gets terminated and Mode IV (as described before) begins. Figure 5-11 shows the 4 modes of operation that are associated with the converter when Mode IIIa is enabled instead of Mode III.

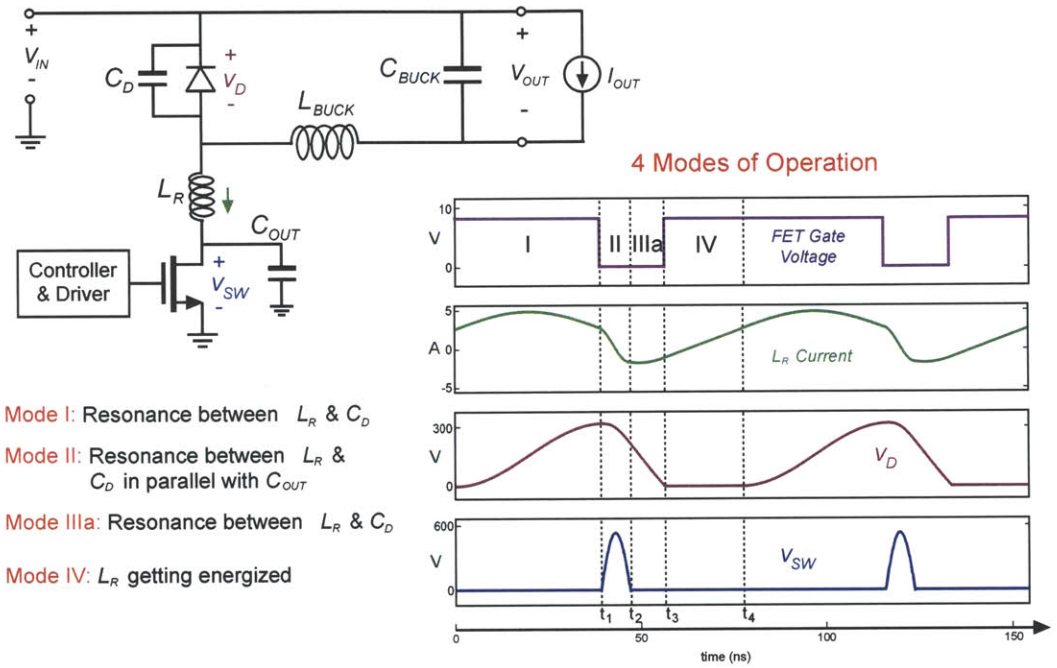


Figure 5-11: Quasi-Resonant Inverted Buck for near-Zero Voltage Switching with Mode IIIa, based on [118, 119]

5.3.6 Control Parameter for Regulation with Quasi-Resonant Inverted Buck

In every practical systems having a power converter, the output voltage or the current will need to be regulated. In case of an LED Driver, the LED current needs to be controlled as the light intensity depends on the current. The control strategy and the circuit details of the controller will be discussed later in Section 5.4. However, in this section, the control parameter which is used to vary the current is introduced. For the Quasi-Resonant Inverted Buck converter described in this section, due to the resonant nature of the converter, it is often difficult to achieve all conversion ratios and guarantee near-ZVS at the same time by just varying the duty cycle of the FET's gate

signal [119]. However, by employing a burst mode adjustment strategy, the converter output can be regulated by driving the gate of the FET with signals having a fixed duty cycle (required for near-ZVS), but in bursts as shown in Figure 5-12. An output capacitor (C_{BUCK}) is used to filter the bursts at the output whereas the EMI filter is used to filter the current bursts at the converter input. Therefore, by controlling the width of the burst, the LED current can be regulated.

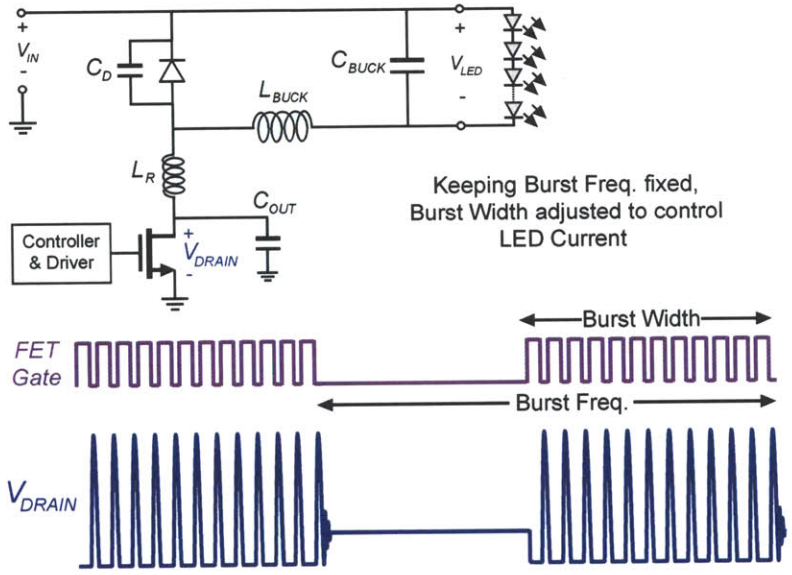


Figure 5-12: Burst control to vary currents

5.4 Controller and Driver with Dimming and Power Factor Correction

5.4.1 PFC and Dimming Control Strategy

In order to incorporate the dimming (LED light intensity control) and PFC features into the LED driver, two prototypes, one with FPGA and another with a custom digital controller and driver IC have been designed. Both the controller versions perform the same functions. The controller uses a burst mode technique discussed in

the previous section to adjust the converter input current, I_{IN} and hence, the LED current, I_{LED} . As in any converter, the control loop requires a reference voltage. By using a rectified sinusoidal reference- *dimming_ref* (which generated from the rectified input voltage- V_{RECT}), I_{IN} can be made to follow V_{RECT} thereby achieving PFC. The input current I_{IN} is estimated by sensing and averaging the voltage across R_{SENSE} as shown in Figure 5-13. By varying the amplitude of *dimming_ref*, the amplitude of the I_{IN} into the converter can be controlled. Therefore the LED current can be varied and PFC can be achieved at the same time. The digital nature of the controller allows us to remove the need for passives in the analog compensator [120] thereby potentially reducing the controller form factor. These compensator passives are typically large resistors and capacitors that need to be off-chip components.

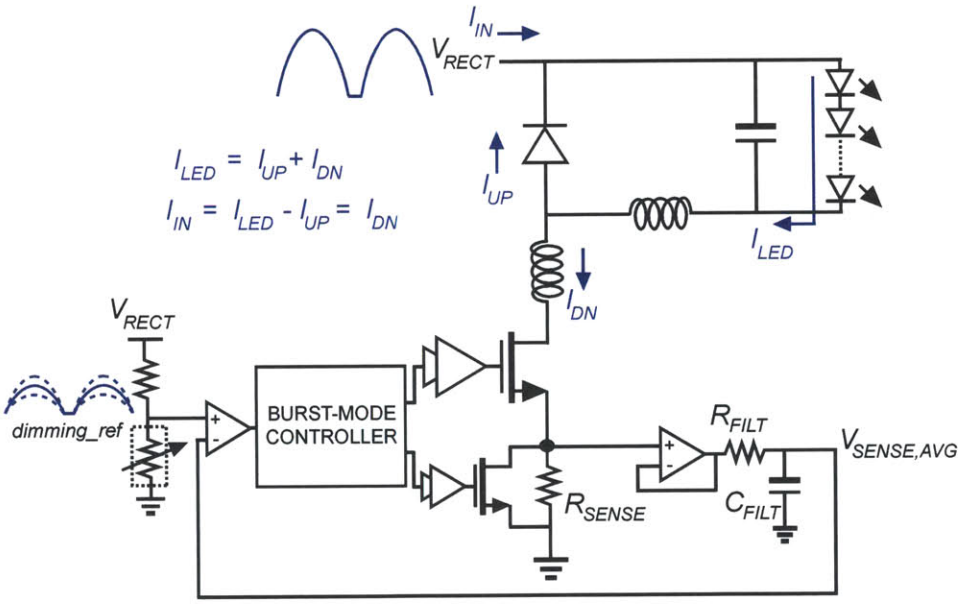


Figure 5-13: Concept of PFC and Dimming Control by sensing Input Current

In this work, the R_{SENSE} has been periodically bypassed to decrease the conduction loss caused by the sense resistor. The current is sensed once in 16 burst cycles. Therefore, for 15 out of 16 burst cycles, a LV Si FET is enabled bypassing the R_{SENSE}. For the burst cycles when R_{SENSE} is enabled, a low pass filter consisting of an Operational Amplifier (in the buffer configuration) and a R-C stage (R_{FILT} and C_{FILT}) are used to create $V_{SENSE,AVG}$. The low pass filter is required for aver-

aging the 11MHz current pulses. A comparator is used to compare the $V_{SENSE,AVG}$ with the *dimming_ref*. If the low pass filter is designed such that $R_{FILT}.C_{FILT}$ is larger than the duration of the burst, the $V_{SENSE,AVG}$ at the end of the burst can be approximated as Eq. 5.18. The time period of the burst is represented by T_{burst}.

$$V_{SENSE,AVG} \approx I_{IN}.R_{SENSE}.T_{burst}/(R_{FILT}.C_{FILT}) \tag{5.18}$$

To detect input currents with 4mA precision (a design decision based on minimum input current step sensed during the AC cycle for PFC as seen from Figure 5-27 shown later) with a 5mV differential input to a comparator, a R_{SENSE} of greater than 0.9Ω is required with R_{FILT} of 50Ω and C_{FILT} of 200nF capacitor. In order to accommodate margin for switching noise during comparison, a sense resistor of 1 to 1.5Ω has been used. For the range of R_{SENSE} used, an efficiency improvement of about 2 to 3% is observed by bypassing this resistor for 15 out of 16 cycles. It must be noted that a smaller resistor (about 1/16th of value of R_{SENSE} used) would give the same efficiency we would obtain with bypassing R_{SENSE} for 15 out of 16 burst cycles. However, for small R_{SENSE} values, the sense resistor voltages would be too low making the comparison with the reference voltage difficult. Moreover, with switching noises riding on top of the desired current estimator voltage, it would be difficult to estimate the current accurately for low values of R_{SENSE}. In order to reduce the R_{SENSE} losses further, a reduction in R_{SENSE} duty cycle from once in 16 cycles to once in 32 or more cycles may be selected. However, this would reduce the number of comparisons in the PFC loop by half since the clock used for duty cycling the R_{SENSE} is the same clock used in the feedback loop. Therefore, a lower R_{SENSE} duty cycle would make the feedback loop slow affecting the PFC.

5.4.2 Controller Operation

The block diagram of the burst mode controller [122] has been shown in Figure 5-14. Two frequencies- *hf_clk* (11MHz) and *lf_clk* (68KHz) are used for generating the

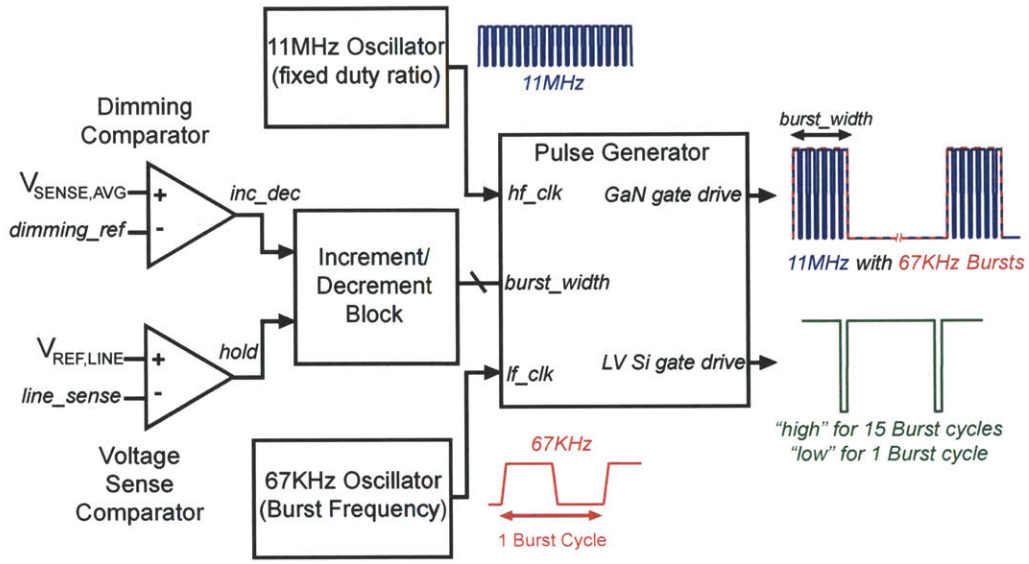


Figure 5-14: Block diagram of circuits for PFC and dimming control

required gate drive signals. The *hf_clk* is created with the appropriate duty ratio required for near-ZVS as shown in Figures 5-6 to 5-11. This ratio is set to 0.65 and is kept constant throughout the converter operation in this implementation (dictated by the resonance and the load current). In order to reliably control the LED current, a Pulse Generator utilizes *lf_clk*, a lower frequency clock, to create burst pulses of the desired widths. The final pulse to the GaN FET is basically *hf_clk* with an envelope riding on top of it at a frequency of *lf_clk* as shown in Figure 5-13. The burst width dictates the output power level. In order to ensure that the feedback loop is stable, the burst width has been made monotonic with the Pulse Generator digital input. Figure 5-13 also shows the signal to the LV Si FET, the FET used to periodically bypass R_{SENSE} as described before. This signal is created by a 4-bit counter with logic circuits that give a "low" only once in 16 system (or burst) cycles. For the other 15 cycles, the LV Si FET gate is "high" thereby keeping the FET on and bypassing R_{SENSE}. A one-bit feedback loop is implemented consisting of a Dimming Comparator, Increment/Decrement Logic and the Pulse Generator. The Dimming Comparator is used to compare $V_{SENSE,AVG}$ (averaged voltage across R_{SENSE} in

Figure 5-13) with *dimming_ref*. The Dimming comparator sends an *inc_dec* signal to an Increment/Decrement Logic Block to generate a 5-bit digital code representing the desired pulse width for the Pulse Generator. A Line Voltage Sense Comparator is also used to shut off the loop when the line voltage has gone too low (say 60V in case of 20 LEDs in series) during the ac cycle. Since for a buck LED driver, below this threshold practically no power is supplied to the LEDs, the Line Voltage Sense Comparator sends a hold signal to the Increment/Decrement logic. The Increment/Decrement operation is then disabled. This ensures that the feedback loop does not increase the burst width unnecessarily when no power is supplied to the LEDs.

5.4.3 Controller and Driver IC Implementation

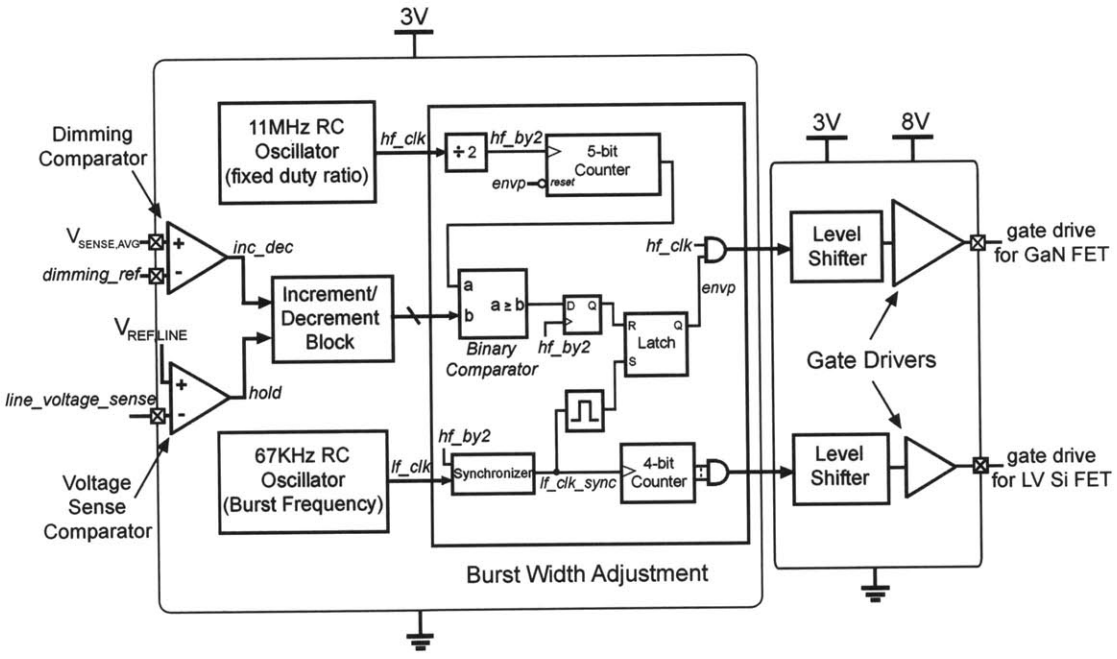


Figure 5-15: Detailed Controller and Driver Implementation for the custom IC

The block diagram of the burst mode controller and gate driver IC is shown in Figure 5-16. The IC version of controller performs the PFC and Dimming control operation with the basic circuitry described earlier. All the control circuits operate off a 3V supply. The Pulse Generator is designed with digital logic and counters

that ensure that the burst widths are monotonic with the burst width digital code (Figure 5-16) that is given to it by the Increment/Decrement Logic preceding this block.

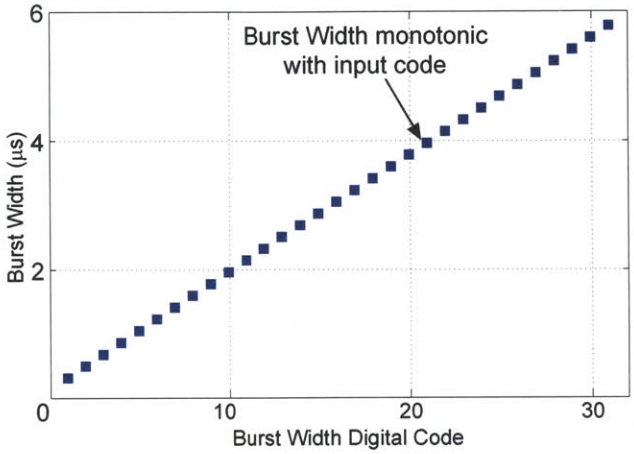


Figure 5-16: Pulse Generator Static Characteristics implemented in test-chip

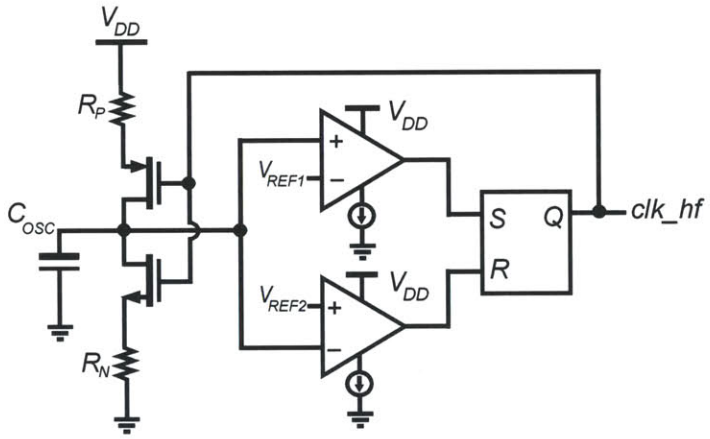


Figure 5-17: RC Oscillator used in custom controller IC

Two RC relaxation oscillators generate the required 11MHz and 68KHz pulses (*hf_clk* and *lf_clk*). Figure 5-17 shows the type of RC oscillator circuit used for both *hf_clk* and *lf_clk*. The duty ratios and the frequencies are set by adjusting the resistors R_P and R_N and the capacitor C_{OSC} appropriately. Level shifters and Gate Drivers operating at 8V have been implemented to drive the gates of both the GaN and LV Si FET. It must be noted that in this work, the power for the on-chip control circuits

and the gate drivers has been supplied externally from 3V and 8V supplies. Prior works [105–107] report auxiliary power converters that supply power to these circuits from the AC input to the system.

5.5 Custom High Frequency Magnetics

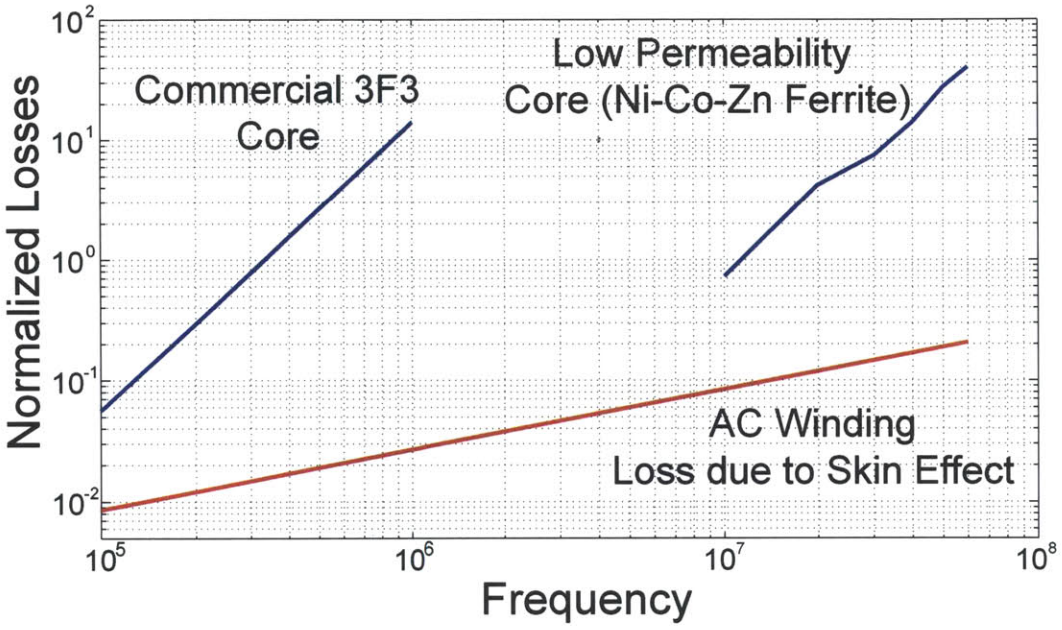


Figure 5-18: Normalized Losses in a Resonant Inductor

At high frequencies, inductor design becomes a critical part of the converter design. Commercial magnetic cores like 3F3 are not suitable for applications having switching frequencies beyond 1MHz. Previous core characterization work based on Steinmetz loss parameters [121,123–125] show that low permeability Ni-Co-Zn ferrite cores can be used at high frequencies without significantly affecting the converter efficiency. In this work, the two inductors, L_{RESO} and L_{BUCK}, have been made both using these Ni-Co-Zn ferrite cores. Figure 5-18 compares this material with 3F3 in terms of core loss in a resonant inductor estimated from their respective Steinmetz parameters [121, 123]. By designing two inductors-one with a 3F3 core and another made using a Ni-Co-Zn ferrite [124, 125], having the same inductance and same peak

current handling capability, it can be seen that at high frequencies, the 3F3 core inductor has core losses much higher than the inductor with Ni-Co-Zn ferrite core. Figure 5-18 also shows the estimated AC winding loss as a function of frequency for the inductor with the Ni-Co-Zn core. Figure 5-19 shows the two inductors L_{BUCK} and L_{RESO} that have been made using low loss, low permeability magnetic cores [124,125] along with *litz* and flat wires. A single layer of winding has been used to minimize inter-winding capacitance.

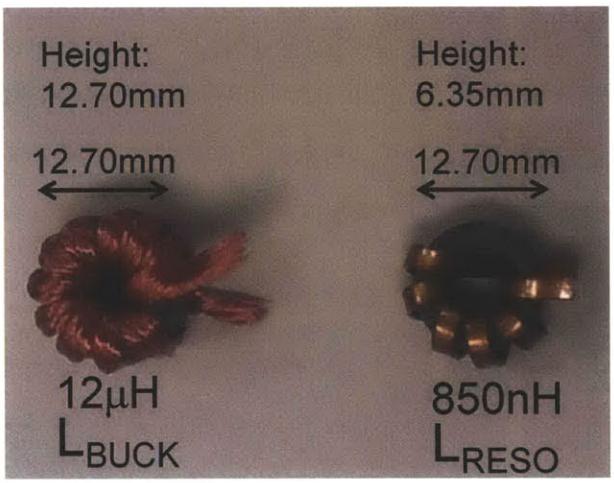


Figure 5-19: Customized L_{BUCK} and L_{RESO} inductors

5.6 Experimental Results

Two prototype test boards that perform power conversion for driving LEDs, PFC and dimming control have been designed and tested. The first prototype has a FPGA based controller with discrete drivers along with the GaN FET, LV Si FET, a diode and required the passives as shown in Figure 5-20(a). The second prototype uses a custom CMOS IC for driving the LED driver FETs, for PFC and dimming control as shown in Figure 5-20(b). This board uses an FPGA only for the IC programmability and testing purposes. It does not perform any PFC or dimming function. Both the boards were tested with 20 LEDs (3.2V each) in series.

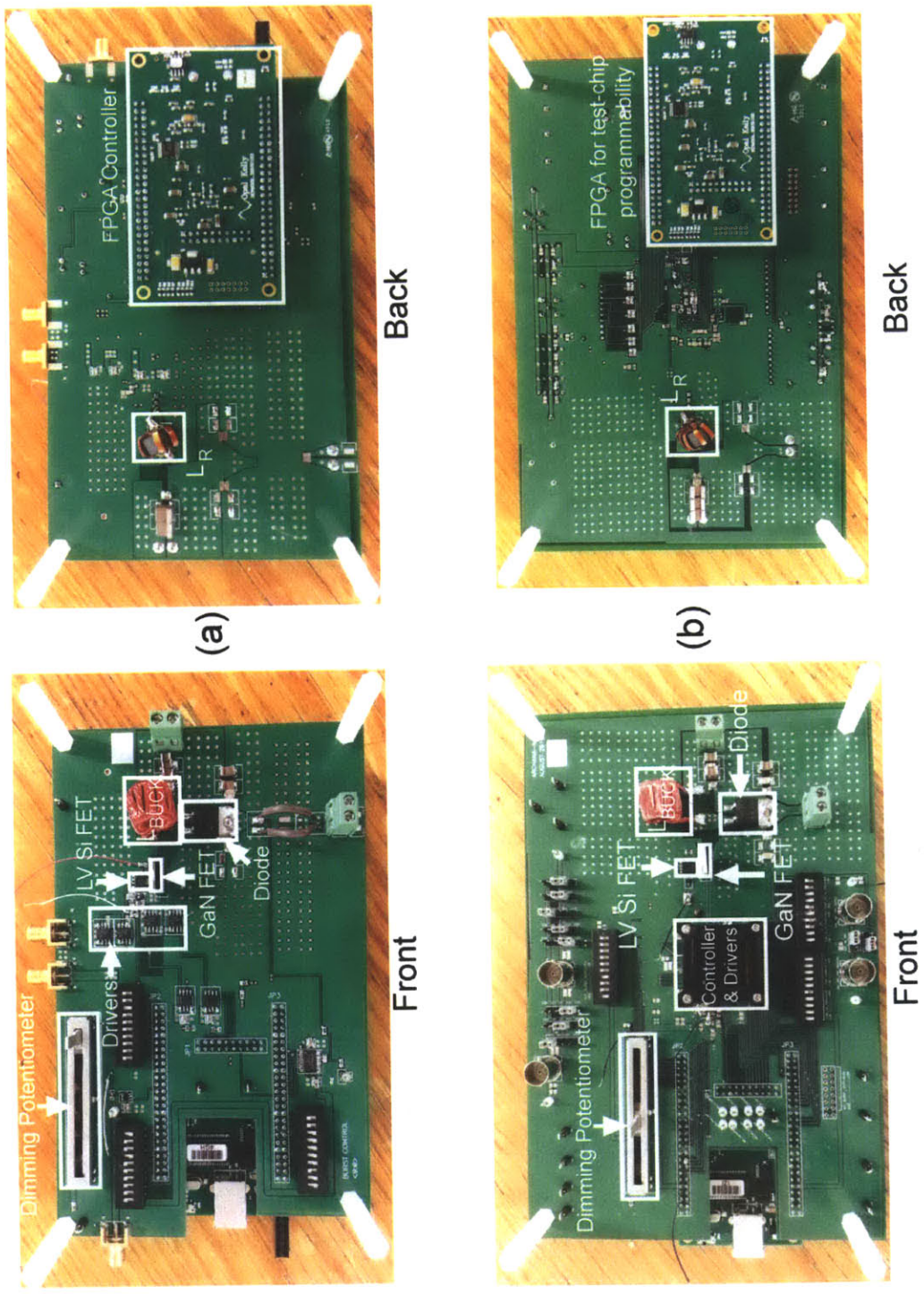


Figure 5-20: Photographs of - (a) Test Board with FPGA based controller, (b) Test Board with Custom IC Controller and Driver

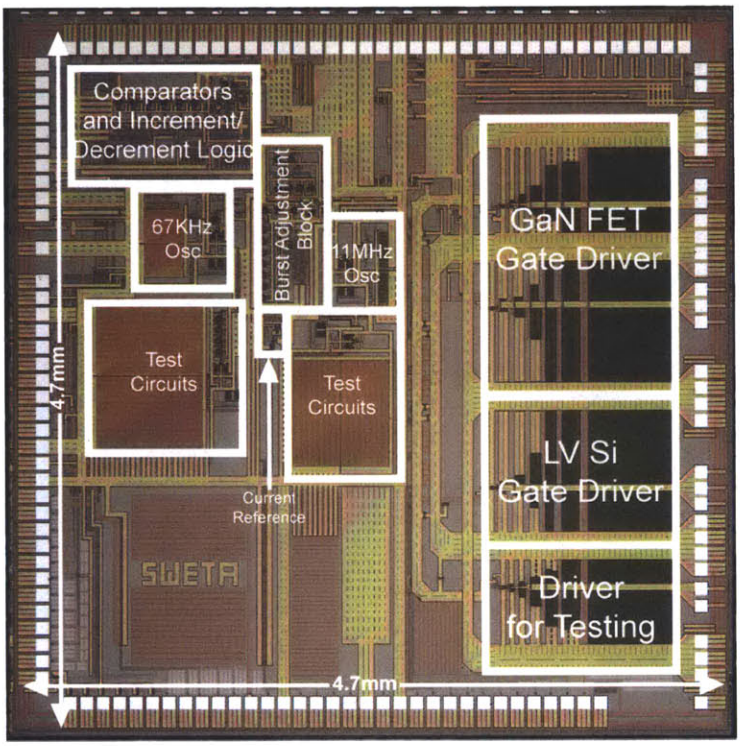


Figure 5-21: Die Micrograph of the controller and gate driver IC for LED Driver

The custom IC has been designed on a 0.35μm digital CMOS process with a 3.3V and 15V handling capability. Figure 5-21 shows the micro-photograph of the custom controller and driver IC. The test-chip occupies a total of 4.7mmx4.7mm. The 3.3V control circuits (without test circuits) occupy 2.4mm^2 and the drivers (without the test driver) occupy 4.5mm^2.

Figure 5-22 shows the experimental setup used for the LED Driver. The test board with the Power Train and the custom IC with controller and driver is connected with a separate EMI Filter (4th order LC filter- two LC stages cascaded) and Rectifier Board (for ease of testing with both ac and dc input sources). The circuit is in operation driving a string of 20 LEDs in series. These are powered off a 110V$_{rms}$ AC input source. The Common Mode Chokes have been used to prevent any conductive EMI from the circuit into the multimeters measuring current. These chokes are required only to increase the accuracy of measurements.

Table 5.4 gives the box volume of the major LED driver components. In practice,

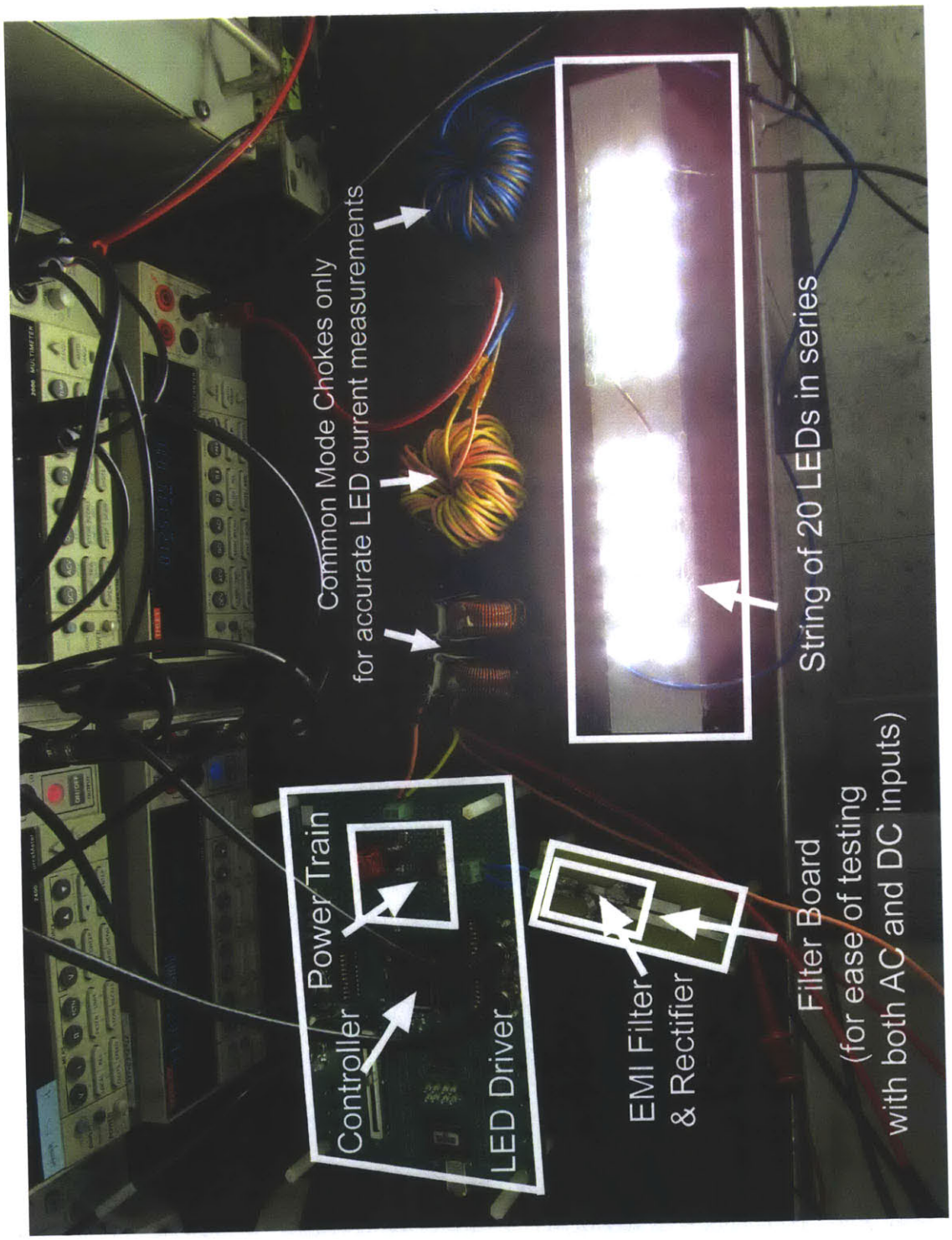


Figure 5-22: LED Driver Test Setup

Table 5.4: Size Breakdown of Converter

Component	Box Volume
Power Train Magnetics	$0.26in^3$
Power Train FETs and Diode	$0.11in^3$
Power Train Capacitors	$0.02in^3$
EMI filter	$0.06in^3$
Controller IC Prototype	die capable of being packaged in within $0.004in^3$ volume

the sum of the individual box volumes is not the total volume. Therefore, on adding 50% (a conservative estimate) of the sum of box volumes to get an estimate of the volume, we get a power density of $32\text{W}/in^3$ for 22W peak power.

5.6.1 Improvement in Efficiency with GaN over Si

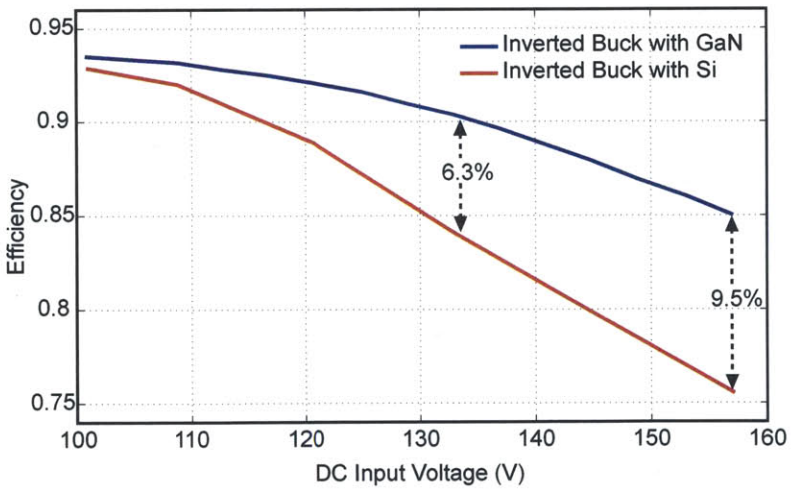


Figure 5-23: Efficiency of LED driver with DC input voltage for GaN and Silicon FETs

In order to quantify the efficiency advantage provided by the GaN FET for this converter, two versions of the Quasi-Resonant inverted buck converter were imple-

mented, one with a commercial high voltage Silicon FET (HV Si FET) and the other with the GaN FET with similar input and output capacitances. All other components have been kept the same. Figure 5-23 shows the measured efficiencies of the power trains of the two converters in open loop with DC inputs ranging from 100V to 157V. It is observed that for both the versions of the converter, the efficiency reduces at higher input voltages. This is due to higher conduction losses caused by higher rms current (more circulating currents) in the resonant circuits and the LED driver FET(GaN or HV Si FET, depending on the version of converter) at high voltages. However, we can see that with the GaN FET, the efficiency is significantly improved- for 133V and 157V, the efficiency improvements of 6.3% and 9.5% respectively are observed. These improvements can be attributed to the lower $R_{ds,ON}$ of the GaN FET as compared to the HV Si FET. The voltage of the LED string for these measurements varies from 61 to 65V and the output power (power to LEDs) ranges from about 7W to 21W for these measurements.

5.6.2 Efficiency of LED driver with AC input

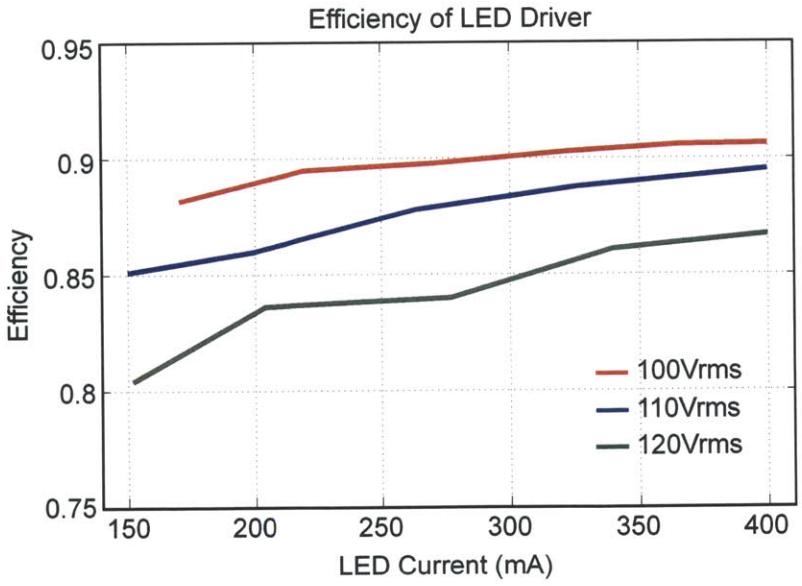


Figure 5-24: Efficiency of LED driver with AC inputs

The system has been tested with a string of 20 LEDs (each of 3.2V diode voltage) in parallel with a 15μF capacitor using the custom inductors described before of values 850nH and 12μH. Figure 5-24 shows the efficiency of the system for different LED current levels (in rms). The power converter has been tested for AC inputs varying from 100-120V_{rms}. A peak efficiency of 90.6% is obtained at 400mA LED current (without gate driver losses) for100V_{rms}. At 110V_{rms} and 120V_{rms}, the peak efficiencies are 89.5% and 86.7% for LED current of 400mA. The gate driver losses amount to 1-1.7% of the input power to the converter for these measurements. The reduction in efficiency at higher voltages is due to higher conduction losses caused by higher rms current in the resonant circuits and the GaN FET at high voltages.

5.6.3 Power Factor of LED driver with AC input

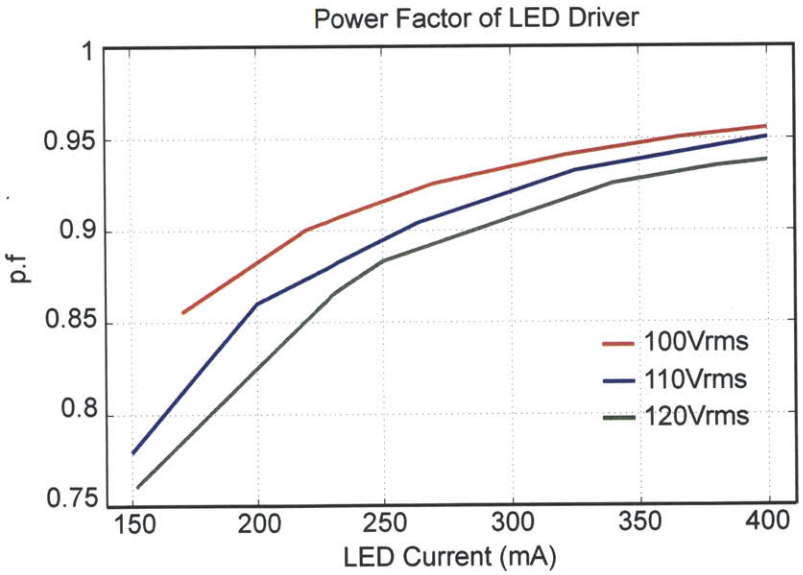


Figure 5-25: Power Factor of LED driver with AC inputs

Figure 5-25 shows the efficiency of the system for different current levels. The peak power factor of 0.96 is obtained for 400mA output current at 100V_{rms} input. It is observed that at lower dimming levels, the power factor of the system reduces. This is due to the phase shifts between the input voltage and current and the distortions

in input current (relative to the input current) that increase at lower dimming levels. Looking at the converter from the input side, we can simplify the system to be basically a simple LC filter (EMI filter) along with a variable load (Quasi-Resonant inverted buck converter) that varies depending upon the lighting intensity desired. At the line frequency (60Hz), the system looks essentially like a capacitor (from the EMI filter) with a variable resistor (converter viewed as variable resistor) in parallel, as the inductors (470μH) in the EMI filter present a low impedance that can be ignored at 60Hz. Therefore, at low light levels, at 60Hz the system behaves more capacitive than resistive. At high light levels, the system is more resistive. It is for this reason, the power factor is higher LED current levels than lower current levels.

5.6.4 Near-ZVS Transients with Burst-Mode Control

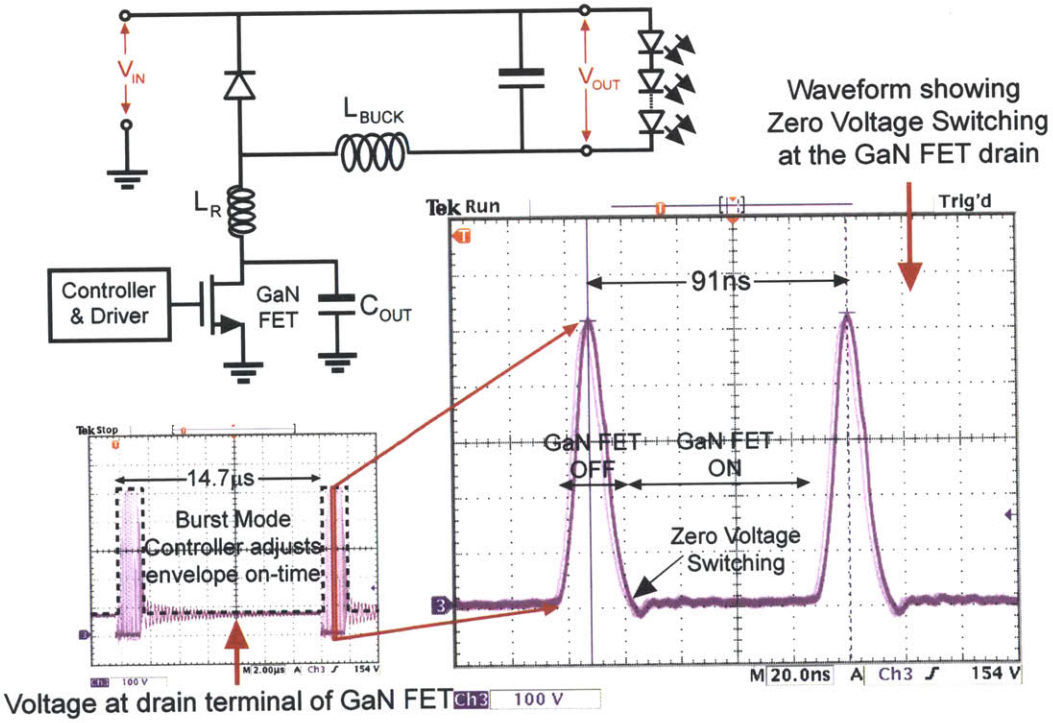


Figure 5-26: Transient showing near Zero Voltage Switching (LV Si FET not shown for simplicity)

As previously discussed in Section 5.4, the resonant nature of the power train

allows us to GaN FET is turned on only when the voltage at the drain is close to 0V which helps minimize switching losses due to the GaN FET output capacitance. In Figure 5-26, the near-ZVS operation is shown when a DC voltage of 130V was applied to the Quasi-Resonant inverted buck converter. The power train of the converter is switched at 11MHz (Time period of 91ns). The output current is controlled by adjusting the burst width of the envelope having a frequency of 68KHz (Time period of 14.7μs) as shown in the bottom left of Figure 5-26. Over a 110V_{rms} AC cycle, the maximum voltage stress of the FET is close to 600V.

5.6.5 Static Current-Voltage characteristics of PFC and Dimming Control loop

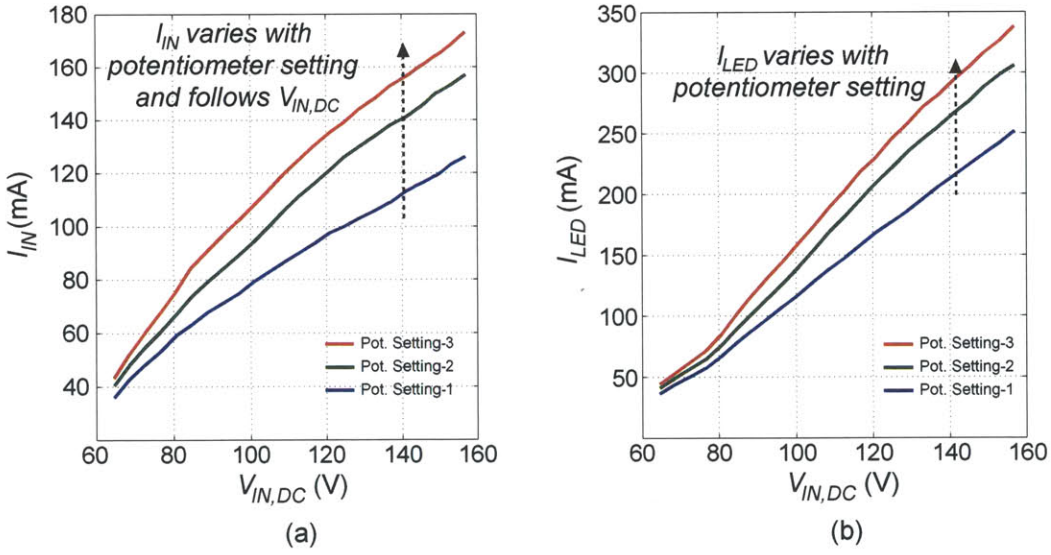


Figure 5-27: Controller Static Characteristics:- (a)I_{IN} versus $V_{DC,IN}$, (b)I_{LED} versus $V_{DC,IN}$

Figure 5-27 shows the static Current-Voltage characteristics of the PFC and Dimming Control loop implemented. As discussed previously in Section 5.4, the input current, I_{IN}, to the LED driver is made to linearly track the input voltage by the controller. In order to see the static characteristics of the controller, the Quasi-Resonant inverted buck converter along with the controller are tested with a DC input

voltage $V_{DC,IN}$. During the actual operation with an AC source, a rectified sinusoidal voltage would replace $V_{DC,IN}$ and would be tracing the X-axis of the plot in Figure 5-27(a). Under these conditions, I_{IN} will be tracing the curves plotted in this figure. Figure 5-27(b) shows the corresponding LED currents at three different potentiometer settings. Both I_{IN} and I_{LED} can be changed by changing the potentiometer resistance. When the resistance is increased, the amplitude of the reference, *dimming_ref*, to the control loop increases thereby increasing the amplitude of I_{IN} and I_{LED}. When decreased, it reduces the *dimming_ref* and hence, decreases the amplitude of the currents. In this fashion both PFC and Dimming features are included in the LED driver design.

5.6.6 Time-Domain Measurement of LED Driver input voltage and current

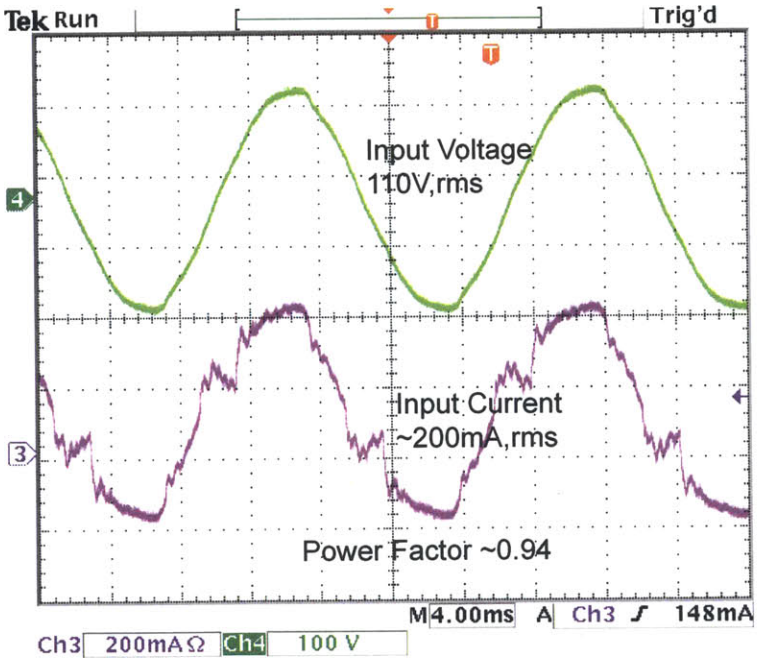


Figure 5-28: Transient waveforms showing input voltage and current to the LED Driver

Figure 5-28 shows the time-domain waveforms of the input current with an AC

input of 110V_{rms} at 60Hz. The power factor for this measurement is 0.94. By using the control strategy explained in Section 5.4, the input current is made to follow the sinusoidal nature of the input voltage.

5.6.7 Time-Domain Measurement of LED Driver output voltage and current

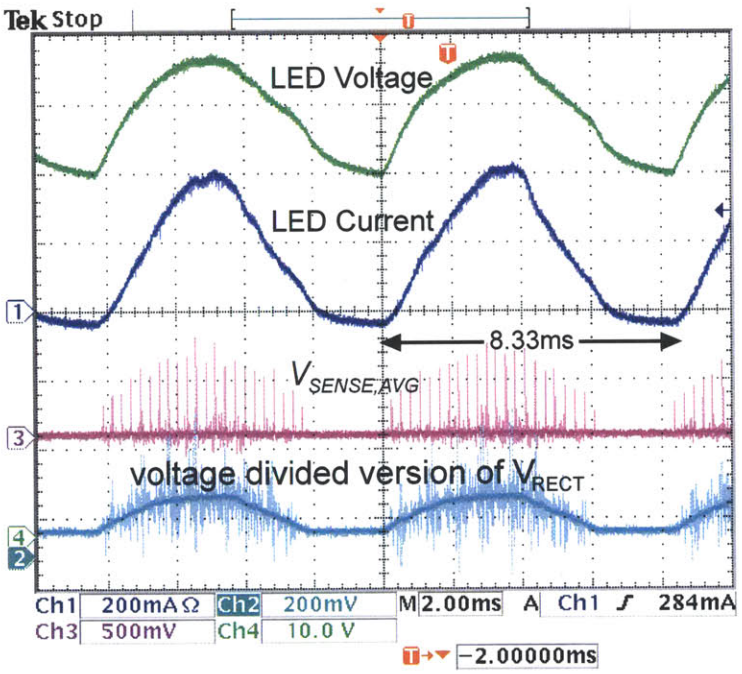


Figure 5-29: Transient waveforms showing LED voltage and current with $V_{SENSE,AVG}$ and voltage divided version of V_{RECT}

Figure 5-29 shows the time-domain waveforms of the output LED current along with the LED voltage, the input current estimator voltage -$V_{SENSE,AVG}$ and the voltage divided version of the rectified input voltage -V_{RECT}.

5.6.8 Comparison with State-of-Art Single Stage LED Drivers

Table 5.5 compares the LED Driver presented in this work with some previously published single stage LED drivers [106–108] for similar output power levels. As can be seen, this work demonstrates higher efficiency at higher switching frequencies while utilizing smaller magnetics with comparable power factors.

Table 5.5: Comparison with State-of-Art Single Stage LED Drivers

	TPS92001 EVM-628	ISSCC 2011	ISSCC 2012	This Work
Topology	Inverted Buck with Si FETs	Inverted Buck with Si FETs	Flyback with Si FETs	Quasi-Resonant Inverted Buck with GaN FETs
Controller	Current Controlled PWM	Current Controlled PWM	Critical Conduction Mode	Current Controlled Burst Mode
Switching Frequency	133KHz	43KHz	Not Reported	11MHz
Peak Efficiency	85%	88%	84.5%	90.6%
Inductors	470µH	5.5mH	1.8mH	L_{RESO} 850nH L_{BUCK} 12µH
Peak Power Factor	0.90	0.98	0.98	0.96
Output Power	Peak 20W	2.5-7W	6-12.5W	7-22W

5.7 Conclusion

Superior figure of merit of GaN FETs has made it possible for us to implement high frequency topologies that were not cost effective in the past due to low efficiencies with Silicon FETs. This work presents a high switching frequency, high efficiency LED Driver using GaN FETs with a digital burst mode controller for PFC and dimming features. Techniques to reduce the sense resistor conduction losses by using circuits that periodically bypasses the resistor have been used. Digital control circuits have

been used to perform PFC. In this work the role of digital control is to achieve the desired regulation (PFC). A peak power factor of 0.96 is achieved. Further, in this work, digital control also helps reduce the passives that are normally used in analog compensators. By using digital compensators, it is possible to completely do away with these passives that are normally off-chip. This helps reduce the pin count and the form factor of the controller.

Chapter 6

Summary and Conclusions

This thesis discusses the role of control circuits for improving efficiency, reducing form factors while providing the desired regulation. Three power converters covering a wide power range- from nano-watts to watts have been presented. Digital control circuits for these individual converters have been highlighted. This chapter first summarizes the key results of each power converter design. Further, ways in which this thesis advances the some of the previously published control techniques for improving efficiency and form factor (presented in Chapter 2) have been discussed. Some generalizable principles are also presented. Finally, some future research directions have been proposed.

6.1 Summary and Key Results

This thesis covers a wide gamut of power converter systems handling power levels from nano-watts to watts. Chapter 3 presents an ultra-low power boost converter harvesting power from the Endo-cochlear Potential. Since the power budget for the entire system is from 1.1 to 6.3nW, digital control circuits have been designed to consume less than the power harvested by the boost converter in the system. The converter presented in this chapter has the lowest power budget reported. The quiescent power

consumption of the control circuits is kept to 544pW. Due to the low power budget, along with conduction and switching losses, we also have leakage losses in the power train that limits the converter efficiency. Digital techniques to minimize this leakage have been used. The boost converter achieves efficiencies of $\geq$50% at the nano-watt level. Chapter 4 discusses a multi-input energy harvesting circuit combining energy from photovoltaic, thermoelectric and piezoelectric harvesters to increase the reliability of the system. A dual-path architecture is proposed that has 11-13% higher efficiency than traditional energy harvesting architectures. The number of inductors has been reduced to one from four (one of each harvester, another for the backup stage buck converter). Further, circuit techniques to perform maximum power extraction from all the harvesters have also been discussed. Chapter 5 presents a 11MHz, 90.6% peak efficiency LED driver with 0.96 peak power factor. A custom digital controller and driver IC has been implemented to perform PFC and dimming functionalities based on a digital burst mode control scheme.

6.2 Contributions to Digital Control and Conclusions

The common theme of this thesis has been investigating the role of control circuits in power converters in improving efficiency and reducing form factor while providing the desired regulation. Table 6.1 summarizes the key results discussed earlier along with the role of digital control circuits in achieving these results in the power converters presented in this thesis. By considering power converters operating over a wide range of power levels from nano-watts to watts, some generalizable conclusions can be made. First, reconfigurable power converter architectures enabled by digital control along with low power digital design principles can help maximize a power converter's efficiency. Here, we must note that the impact of low power design of digital control in converter's efficiency is limited to low power converters however, digital control enabling reconfigurable power architectures do not need to be limited to low power

applications. Second, digital control can help reduce the number of passives in both the power train (with some overhead) as well as the controller. In certain designs, depending on the design targets, the designer may not choose to incur the overhead associated with reduction of passives in the power train. However, even in such designs, the digital nature of the control can help reduce the compensator passives.

Table 6.1: Thesis Contributions

	Key Results	Role of Digital Control
Chapter 3	• Quiescent power of 544pW for a boost converter with the the lowest power budget reported • Boost converter efficiency $\geq$50% for nano-watt level while stepping up 30-55mV to 0.8-1.1V.	• Ultra-low quiescent power digital controller design improving overall system efficiency • Efficiency improvement due to leakage reduction by employing digital techniques in power converter
Chapter 4	• 11-13% higher efficiency with dual-path architecture over traditional energy harvesting architectures • Number of inductors reduced from 4 to 1 in a multi-input energy harvesting system	• Efficiency improvement from efficient architecture enabled by digital control circuits • Form factor reduction by inductor sharing enabled by digital control circuits
Chapter 5	• 0.96 peak power factor for 90.6% peak efficiency LED driver	• Regulation along with form factor reduction by using digital control (no compensator passives)

6.3 Future Directions

Based on the work in this thesis, the following two directions can be envisioned for next generation power converters.

1. Implantable electronics (pace-makers, cochlea implants, etc) rely on batteries or wireless power transfer. These systems can use similar low power converter design concepts presented in Chapters 3 and 4 of this thesis to attain better energy autonomy. Utilizing bio-fuel cells that can extract energy from the blood glucose in human body, the already existing energy source can be supplemented. Some recent advances have shown that bio-fuel cells might be able to supply enough energy to power some implants. The already existing source along with the bio-fuel cell would increase the long term reliability of the implant. For implants like pace-makers, this would ensure that the battery lifetime is extended which would potentially remove the need for battery replacement. Some efforts are being taken in this direction [126]. For implants similar to cochlear implants, this would enable the user to potentially remove the low cosmesis transmitter on the users scalp when the harvested energy from the bio-fuel cell is enough. Low power converters presented in this thesis can enable such systems.

2. High frequency power conversion has been limited to low voltage applications until now. With the lower specific on resistance of GaN FETs, it is now possible to design high voltage, high frequency (10MHz and above) converters that traditionally used much lower switching frequencies (100's of KHz) using smaller passive components. High frequency topologies that had prohibitively high losses with silicon devices can now be implemented using GaN enabling high efficiency converters with small form factors. However, high switching frequencies do not necessarily mean smaller passives. For grid connected applications requiring PFC, although the high switching frequency makes the converter's magnetics smaller however, the size of the output capacitor is still limited by the 120Hz

ripple. Typically a large capacitor is required to act as an energy buffer and minimize the voltage ripple. A smaller ripple means that all the DC-DC converters powered by this buffer capacitor can be designed for a narrow input voltage range at low switching frequencies. However, using high frequency power converters with GaN FETs would give an opportunity to design fast controllers so that the DC-DC converters can be powered off smaller buffer capacitor with increased ripple. With the fast controllers the DC-DC converters would be able to handle a wide input voltage range without sacrificing their regulation.

Appendix A

Generalized MPPT using Time-based Power Monitor

For boost conversion ratios close to 3 (ratio of V_{LOAD} to V_{HAR}), we must see how closely $t_{2,PRIM}$ predicts the optimal power point of a photovoltaic harvester. It must be noted that $t_{2,PRIM}$ is actually given by Eq. 4.10 which has a term (V_{LOAD}-V_{HAR}). This term has been approximated to V_{LOAD} in order to get a closed form expression for the power monitor as given by Eq. 4.11. Therefore the timing information in $t_{2,PRIM}$ is an approximate power monitor. In this appendix, it will be shown that the effect of this approximation reduces the accuracy to locate the maximum power point voltage but this reduces the amount of extractable power from the photovoltaic harvester by less than 3%. Let us define a *factor- closeness to maximum power*. This is the ratio of the power that can be extracted from the harvester at the voltage where $t_{2,PRIM}$ is maximum to the maximum power that can be extracted from at harvester at its true V_{MPP}. To analyze this, a photovoltaic harvester model same as in Figure 4-5 is used. Various values of the diode non-ideality factor and I_{GEN} have been considered to mimic different types of harvesters and different light intensities as shown in Figure A-1. The *closeness to maximum power* factor is observed to be greater than 0.97. The same analysis is done for different values of R_S and R_P and similar plots of closeness to maximum power is obtained.

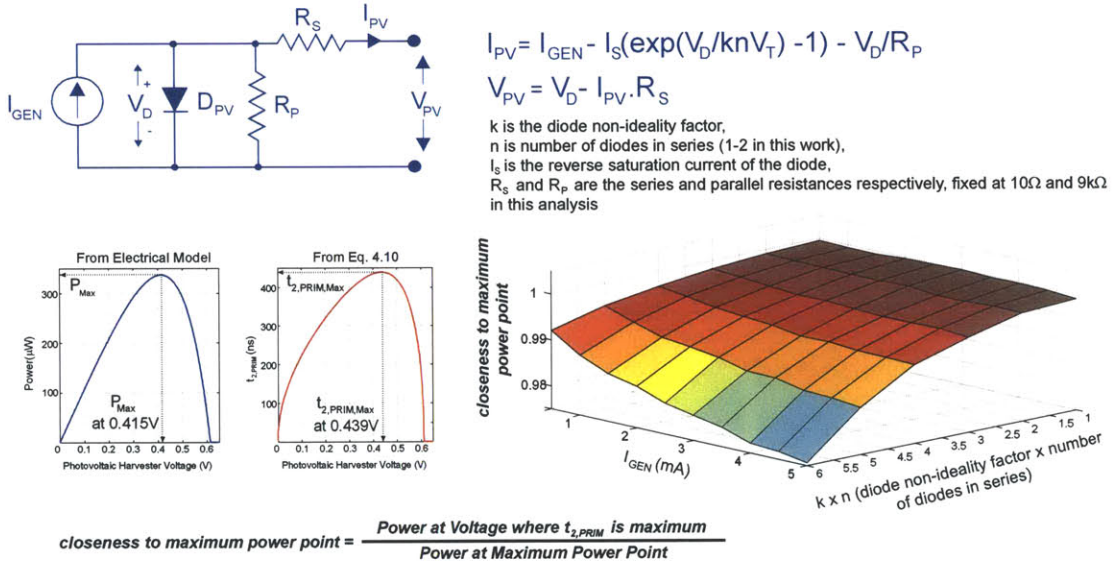


Figure A-1: Model of photovoltaic harvester with closeness to maximum power plotted for different diodes and different intensities

Appendix B

MATLAB and Verilog Codes for LED Driver

This appendix gives the MATLAB and Verilog codes that have been used in analyses and controller's FPGA implementation for the LED Driver.

B.1 MATLAB Code for Quasi-Resonant Converter Analysis

The Quasi-Resonant Inverted Buck converter is analyzed using the equations described in Section 5.3 of this thesis. The code assumes linear FET and diode capacitances. Although in practice, non-linearities in the capacitance would cause the measured response to be slightly different, this code helps us get an understanding of multi-resonant circuits in the Quasi-Resonant Converter.

The input parameters to the MATLAB routine are-LED current (load), duty (burst width*burst frequency), Lr (resonant inductor), Csw (FET capacitance), Cd (Diode Capacitance) and tx (time duration of Mode-I). With these inputs, the MATLAB code decides the modes that the Quasi-Resonant converter will go through.

It also generates plots of resonant inductor current (Il), Diode Voltage (Vd), Switch Voltage (Vsw) (as shown in Figures 5-7 to 5-11). It also outputs values of output voltage of converter (Vout), maximum voltage stress of FET (Maximum_Switch_Voltage) and RMS current in the resonant inductor (Il_rms).

Listing B.1: MATLAB Code for Quasi-Resonant Converter Analysis

```
clc;
clear;

load=0.45108;
duty=0.21;
Io=load/duty;
Vin=150;
Lr=850*10^-9;
Csw=80*10^-12;
Cd=40*10^-12;
wd=1/((Lr*Cd)^0.5);
ws=1/((Lr*Csw)^0.5);
Csd=Cd*Csw/(Cd+Csw);
wsd=1/((Lr*Csd)^0.5);
Zd=(Lr/Cd)^0.5;
Zsw=(Lr/Csw)^0.5;
Zsd=(Lr/Csd)^0.5;
tx=40*10^-9;
t=0:0.1*10^-9:1000*10^-9;
flag_no_zvs=0;

% Mode 1
mode1_limit_counter=int32(tx*10^10);
mode1_limit=tx;
for i=1:mode1_limit_counter
    Il(i)=Io+((Vin/Zd)*sin(wd*t(i)));
    Vd(i)=Vin*(1-cos(wd*t(i)));
    Vsw(i)=0;
```

```
29 end
30
31 % Mode 2
32 flag_mode3a=0;
33 flag_mode3b=0;
34 mode2_start_counter=mode1_limit_counter+1;
35 for i=mode2_start_counter:10000
36     if (flag_mode3a == 0 & flag_mode3b ==0)
37         Il(i)= Il(mode1_limit_counter)*cos(wsd*(t(i)-mode1_limit))...
                + ((Io*Csw/(Csw+Cd))*(1-cos(wsd*(t(i)-mode1_limit))))...
               +((Vin-Vd(mode1_limit_counter))/Zsd)*sin(wsd*(t(i)-...
               mode1_limit));
38         Vsw(i)= ((Il(mode1_limit_counter)/(wsd*Csw))*sin(wsd*(t(i)...
               -mode1_limit))) + (Io*(t(i)-mode1_limit)/(Csw+Cd)) - (...
               Io/((Csw+Cd)*wsd))*sin(wsd*(t(i)-mode1_limit)) + ((Vin-...
               Vd(mode1_limit_counter))*(Cd/(Csw+Cd))*(1-cos(wsd*(t(i)...
               -mode1_limit))));
39         Vd(i)= Vd(mode1_limit_counter) + Il(mode1_limit_counter)...
               *(1/(wsd*Cd))*sin(wsd*(t(i)-mode1_limit)) + (Vin-Vd(...
               mode1_limit_counter))*(Csw/(Csw+Cd))*(1-cos(wsd*(t(i)-...
               mode1_limit))) - Io*(t(i)-mode1_limit)/(Csw+Cd) - (Io/(...
               wsd*Cd))*(Csw/(Csw+Cd))*sin(wsd*(t(i)-mode1_limit));
40         mode2_limit=t(i);
41         mode2_limit_counter=i;
42     else
43         Il(i)=Il(i-1);
44         Vsw(i)=Vsw(i-1);
45         Vd(i)=Vd(i-1);
46     end
47
48     if(Vsw(i) ≥ 0 & Vd(i) ≥ 0)
49         flag_mode3a=0;
50         flag_mode3b=0;
51     elseif (Vsw(i) < 0)
52         flag_mode3a=0;
53         flag_mode3b=1;
```

```
54      else
55          flag_mode3a=1;
56          flag_mode3b=0;
57      end
58  end
59
60  %mode2_limit=double(mode2_limit_counter*0.1*10^-9);
61
62  % Mode 3
63  mode3_start_counter=mode2_limit_counter+1;
64  flag_end_of_mode3=0;
65  if (flag_mode3a == 1)
66      for i=mode3_start_counter:10000
67          if(flag_end_of_mode3 == 0)
68              Il(i)= (Vin-Vsw(mode2_limit_counter))*(1/Zsw)*sin(ws*(...
                    t(i)-mode2_limit)) + (Il(mode2_limit_counter)*cos(...
                    ws*(t(i)-mode2_limit)));
69              Vd(i)= 0;
70              Vsw(i)= Vsw(mode2_limit_counter)*cos(ws*(t(i)-...
                    mode2_limit)) + Zsw*Il(mode2_limit_counter)*sin(ws...
                    *(t(i)-mode2_limit)) + Vin*(1-cos(ws*(t(i)-...
                    mode2_limit)));
71              if(Vsw(i) <= 0)
72                  flag_end_of_mode3=1;
73                  mode3_limit_counter=i;
74                  mode3_limit=t(i);
75              end
76              if(i == 10000)
77                  flag_no_zvs=1;
78              end
79          end
80      end
81
82      if(flag_no_zvs == 1)
83          min_Vsw=ceil(Vsw(mode3_start_counter));
84          mode3_limit_counter=mode3_start_counter;
```

```
85          mode3_limit=t(mode3_start_counter);
86          for i=mode3_start_counter:10000
87              if(ceil(Vsw(i)) < min_Vsw)
88                  min_Vsw=Vsw(i);
89                  mode3_limit_counter=i;
90                  mode3_limit=t(i);
91              end
92          end
93      end
94
95  elseif (flag_mode3b == 1)
96      for i=mode3_start_counter:10000
97          if (flag_end_of_mode3 == 0)
98              Il(i)= (Vin-Vd(mode2_limit_counter)*(1/Zd)*sin(wd*(t(i...
                    )-mode2_limit))) + (Il(mode2_limit_counter)-Io)*cos...
                    (wd*(t(i)-mode2_limit)) + Io;
99              Vsw(i)= 0;
100             Vd(i)= Vin*(1-cos(wd*(t(i)-mode2_limit))) + Vd(...
                    mode2_limit_counter)*cos(wd*(t(i)-mode2_limit)) + ...
                    Zd*(Il(mode2_limit_counter)-Io)*sin(wd*(t(i)-...
                    mode2_limit));
101             if(Vd(i) ≤ 0)
102                 flag_end_of_mode3=1;
103                 mode3_limit_counter=i;
104                 mode3_limit=t(i);
105             end
106         end
107     end
108 end
109
110 % Mode 4
111 mode4_start_counter=mode3_limit_counter+1;
112 for i=mode4_start_counter:10000
113     Il(i)=(Vin*(t(i)-mode3_limit)/Lr) + Il(mode3_limit_counter);
114     Vsw(i)=0;
115     Vd(i)=0;
```

```
116     if (Il(i)≤Io)
117         mode4_limit=t(i);
118         mode4_limit_counter=i;
119     end
120 end
121
122
123 if(flag_mode3a == 1)
124     toff=mode3_limit-mode1_limit;
125 elseif(flag_mode3b == 1)
126     toff=mode2_limit-mode1_limit;
127 end
128
129 Flag_NO_ZVS=flag_no_zvs
130 Time_Period=mode4_limit
131 Freq=1/Time_Period
132 Toff=toff
133
134 %Ploting Waveforms
135 %inductor current
136 subplot(3,1,1);
137 plot(t(1:mode4_limit_counter),Il(1:mode4_limit_counter));
138 %diode voltage
139 subplot(3,1,2);
140 plot(t(1:mode4_limit_counter),Vd(1:mode4_limit_counter));
141 %switch voltage
142 subplot(3,1,3);
143 plot(t(1:mode4_limit_counter),Vsw(1:mode4_limit_counter));
144
145 %RMS Current
146 Il_sq_sum=0;
147 for i=1:mode4_limit_counter
148     Il_sq_sum=Il_sq_sum+(Il(i)*Il(i));
149 end
150 Il_rms=sqrt(Il_sq_sum/double(mode4_limit_counter))
151
```

```
%Output Voltage
Vd_sum=0;
for i=1:mode4_limit_counter
    Vd_sum=Vd_sum+Vd(i);
end
Vout=Vd_sum/double(mode4_limit_counter)

%Peak Switch Voltage
Maximum_Swich_Voltage= max(Vsw)
```

B.2 Verilog Codes for FPGA based Controller

An Opal Kelly 6001 FPGA board was used to implement a burst mode controller described in Section 5.4. The controller requires a Comparator, Operational Amplifier (for sensing and feedback control) and an ADC (for sensing the line voltage). The ADC has been used for experimental purposes. In the IC implementation, the ADC has been replaced by a comparator. Also, the pulse generation in this version of the controller has the ability to have a 6-bit pulse width input. In the IC implementation, this has been optimized to 5-bits. All the control logic is included in the code. It requires a 200MHz input clock that is generated by an on-board PLL on the Opal Kelly 6001.

Listing B.2: Verilog Code for FPGA based Controller

```
`timescale 1ns / 1ps
module pulse_gen_v1(
        input clk,
        input initialize,
        input [5:0] adc_data,
        input comparator_out,
        input [4:0] T,
        input [4:0] toff,
```

```
9           input [5:0] burst_control,
10          output [7:0] count,
11          output adc_clk,
12          output clk_to_ps,
13          output enable_adc,
14          output set_env_dash,
15          output dimming_sig,
16          output [5:0] test_out,
17          output clk_for_sense_comp,
18          output delayed_clk_for_sense_comp
19      );
20
21          reg [31:0] count_temp;
22          reg [4:0] temp1;
23          reg [5:0] temp2;
24          reg set;
25          reg set_dash;
26          reg enable_ps;
27          reg [12:0] temp_env1;
28          reg [13:0] temp_env2;
29          reg set_env;
30          reg set_env_dash;
31          reg [3:0] count_dimming;
32          reg dimming_sig;
33          reg [5:0] test_out;
34          reg clk_for_sense_comp;
35          reg [7:0] clk_div;
36          reg slow_clk;
37          reg delayed_clk_for_sense_comp;
38
39          wire enable_adc;
40          wire [5:0] concat_toff;
41          wire [13:0] concat_burst_control;
42
43          always @ (posedge clk)
44              begin
```

```
45              if (initialize == 0)
46                  begin
47                      count_temp <= 32'b0;
48                  end
49              else if (initialize == 1)
50                  begin
51                      count_temp <= count_temp + 1;
52                  end
53              end
54
55          always @ (posedge clk)
56              begin
57                  if (initialize == 0)
58                      begin
59                          temp1 <= 5'b0;
60                          temp2 <= 6'b0;
61                      end
62                  else if (initialize == 1)
63                      begin
64                          if (temp1 < T)
65                              begin
66                                  temp1 <= temp1 + 1;
67                                  set <= 1'b1;
68                                  if (temp2 < concat_toff)
69                                      begin
70                                          temp2 <= temp2 + 1;
71                                          set_dash <= 1'b1;
72                                      end
73                                  else
74                                      begin
75                                          set_dash <= 1'b0;
76                                      end
77                              end
78                          else
79                              begin
80                                  temp1 <= 5'b0;
```

```
81                              temp2 ≤ 6'b0;
82                              set ≤ 1'b0;
83                          end
84                  end
85          end
86
87      always @ (posedge clk)
88          begin
89              if (adc_data < 6'b010111)
90                  enable_ps ≤ 1'b0;                    //changed...
                        1'b0 to 1'b1
91              else
92                  enable_ps ≤ 1'b1;
93          end
94
95
96      always @ (posedge clk)
97          begin
98              if (initialize == 0)
99                  begin
100                     temp_env1 ≤ 13'b0;
101                     temp_env2 ≤ 14'b0;
102                 end
103             else if (initialize == 1)
104                 begin
105                     if (temp_env1 < 13'b0100100000000 ) ...
                                        //setting burst mode ...
                            frequency to ¬50KHz
106                         begin
107                             temp_env1 ≤ temp_env1 + 1;
108                             set_env ≤ 1'b1;
109                             if (temp_env2 < ...
                                concat_burst_control)        //...
                                setting duty ratio
110                                 begin
111                                     temp_env2 ≤ temp_env2 + 1;
```

```
112                                     set_env_dash <= 1'b1;
113                                 end
114                             else
115                                 begin
116                                     set_env_dash <= 1'b0;
117                                 end
118                         end
119                     else
120                         begin
121                             temp_env1 <= 13'b0;
122                             temp_env2 <= 14'b0;
123                             set_env <= 1'b0;
124                         end
125                 end
126             end
127
128
129         always @ (negedge clk)
130             begin
131                 delayed_clk_for_sense_comp <= clk_for_sense_comp;
132             end
133
134 /*      always @ (posedge clk)
135             begin
136                 clk_div <= clk_div + 1;
137                 if (clk_div == 11'b0)
138                     slow_clk <= 1'b1;
139                 else
140                     slow_clk <= 1'b0;
141             end
142 */
143
144
145
146         always @ (negedge set_env_dash)
147             begin
```

```
148                 count_dimming <= count_dimming + 1;
149                 if (count_dimming == 4'b0000)
150                     dimming_sig <= 1'b1;                          //...
                            change to 1'b0 for removing dimming
151                 else
152                     dimming_sig <= 1'b0;
153                 if (count_dimming == 4'b0001)
154                     clk_for_sense_comp <= 1'b1;
155                 else
156                     clk_for_sense_comp <=1'b0;
157             end
158
159         always @ (posedge delayed_clk_for_sense_comp)
160             begin
161                 if (initialize == 0)
162                     test_out <= 6'b0;
163                 else
164                     begin
165                         if (enable_ps == 1'b1)
166                             begin
167                                 if (comparator_out == 1'b1)
168                                     begin
169                                         if (test_out < 6'b111111)
170                                             test_out <= test_out + ...
                                                    1;
171                                         else if (test_out == 6'...
                                                b111111)
172                                             test_out <= test_out;
173                                     end
174                                 else if (comparator_out == 1'b0)
175                                     begin
176                                         if (test_out > 6'b000000)
177                                             test_out <= test_out - ...
                                                    1;
178                                         else if (test_out == 6'...
                                                b000000)
```

```
179                                                    test_out <= test_out;
180                                                end
181                                            end
182                                        end
183                                    end
184
185             assign concat_toff [5:0]= {{1'b0},{toff[4:0]}};
186             assign concat_burst_control [13:0]= {{3'b000},{test_out...
                    [5:0]},{5'b00111}};
187 //          assign concat_burst_control [13:0]= {{3'b000},{...
        burst_control[5:0]},{5'b00111}};
188             assign count [7:0] = count_temp [31:24];
189             assign adc_clk = count_temp[10];
190             assign clk_to_ps = ¬((¬set_dash)&&(1'b1)&&(set_env_dash)...
                    &&(enable_ps)) ;    // removed enable_ps bypassing adc1
191             assign enable_adc = 1'b0;
192
193 endmodule
```

Listing B.3: UCF Code for FPGA based Controller

```
1  NET "clk"    LOC="T8"   | IOSTANDARD="LVCMOS33";
2
3  NET "count<0>"     LOC="A4"   | IOSTANDARD="LVCMOS33";
4  NET "count<1>"     LOC="C5"   | IOSTANDARD="LVCMOS33";
5  NET "count<2>"     LOC="B5"   | IOSTANDARD="LVCMOS33";
6  NET "count<3>"     LOC="A5"   | IOSTANDARD="LVCMOS33";
7  NET "count<4>"     LOC="C6"   | IOSTANDARD="LVCMOS33";
8  NET "count<5>"     LOC="B6"   | IOSTANDARD="LVCMOS33";
9  NET "count<6>"     LOC="A6"   | IOSTANDARD="LVCMOS33";
10 NET "count<7>"     LOC="A7"   | IOSTANDARD="LVCMOS33";
11
12 NET "clk_to_ps"    LOC="C8"   | IOSTANDARD="LVCMOS33";
13 NET "set_env_dash"      LOC="C7"   | IOSTANDARD="LVCMOS33";
14 NET "dimming_sig" LOC="B8" | IOSTANDARD="LVCMOS33";
```

```
15
16 NET "comparator_out"    LOC="G3"    | IOSTANDARD="LVCMOS33";
17 NET "adc_clk"      LOC="A13" | IOSTANDARD="LVCMOS33";
18 NET "enable_adc"   LOC="B14" | IOSTANDARD="LVCMOS33";
19 NET "adc_data<5>" LOC="K16" | IOSTANDARD="LVCMOS33";
20 NET "adc_data<4>" LOC="K15" | IOSTANDARD="LVCMOS33";
21 NET "adc_data<3>" LOC="H16" | IOSTANDARD="LVCMOS33";
22 NET "adc_data<2>" LOC="H14" | IOSTANDARD="LVCMOS33";
23 NET "adc_data<1>" LOC="F16" | IOSTANDARD="LVCMOS33";
24 NET "adc_data<0>" LOC="G16" | IOSTANDARD="LVCMOS33";
25
26 NET "initialize"  LOC="D5"   | IOSTANDARD="LVCMOS33";
27
28 NET "T<4>"         LOC="M3" | IOSTANDARD="LVCMOS33";
29 NET "T<3>"         LOC="N3" | IOSTANDARD="LVCMOS33";
30 NET "T<2>"         LOC="L1" | IOSTANDARD="LVCMOS33";
31 NET "T<1>"         LOC="M1" | IOSTANDARD="LVCMOS33";
32 NET "T<0>"         LOC="M2" | IOSTANDARD="LVCMOS33";
33
34 NET "toff<4>"      LOC="A3" | IOSTANDARD="LVCMOS33";
35 NET "toff<3>"      LOC="A2" | IOSTANDARD="LVCMOS33";
36 NET "toff<2>"      LOC="B2" | IOSTANDARD="LVCMOS33";
37 NET "toff<1>"      LOC="B1" | IOSTANDARD="LVCMOS33";
38 NET "toff<0>"      LOC="C2" | IOSTANDARD="LVCMOS33";
39
40 #NET "burst_control<7>"     LOC="T13" | IOSTANDARD="LVCMOS33";
41 #NET "burst_control<6>"     LOC="R14" | IOSTANDARD="LVCMOS33";
42 NET "burst_control<5>"     LOC="T15" | IOSTANDARD="LVCMOS33";
43 NET "burst_control<4>"     LOC="R15" | IOSTANDARD="LVCMOS33";
44 NET "burst_control<3>"     LOC="R16" | IOSTANDARD="LVCMOS33";
45 NET "burst_control<2>"     LOC="P15" | IOSTANDARD="LVCMOS33";
46 NET "burst_control<1>"     LOC="P16" | IOSTANDARD="LVCMOS33";
47 NET "burst_control<0>"     LOC="N14" | IOSTANDARD="LVCMOS33";
48
49 #NET "test_out<7>"     LOC="G1"    |  IOSTANDARD="LVCMOS33";
50 #NET "test_out<6>"     LOC="H2"    |  IOSTANDARD="LVCMOS33";
```

```
51
52 NET "test_out<5>"     LOC="K1"     |  IOSTANDARD="LVCMOS33";
53 NET "test_out<4>"     LOC="J3"     |  IOSTANDARD="LVCMOS33";
54 NET "test_out<3>"     LOC="K2"     |  IOSTANDARD="LVCMOS33";
55 NET "test_out<2>"     LOC="L3"     |  IOSTANDARD="LVCMOS33";
56 NET "test_out<1>"     LOC="E1"     | IOSTANDARD="LVCMOS33";
57 NET "test_out<0>"     LOC="E2"       | IOSTANDARD="LVCMOS33";
58 NET "clk_for_sense_comp"     LOC="H1"      |   IOSTANDARD="LVCMOS33...
      ";
59 NET "delayed_clk_for_sense_comp"     LOC="J1"      |   IOSTANDARD="...
      LVCMOS33";
```

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