Resonant Transmission Line Drivers

by

Matthew E. Becker

B.S. Electrical Engineering, 1995
M.Eng. Electrical Engineering, 1996
Massachusetts Institute of Technology

Submitted to the Department of Electrical Engineering in Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy in Electrical Engineering

at the

Massachusetts Institute of Technology

February 2000

Signature of Author: _____
Department of Electrical Engineering
January 28, 2000

Certified by: _____
Thomas F. Knight, Jr.
Senior Research Scientist

Accepted by: _____
Arthur C. Smith
Chairman, Committee for Graduate Students

Resonant Transmission Line Drivers

Matthew E. Becker

Submitted to the Department of Electrical Engineering on Jan 28, 2000
in Partial Fulfillment of the Requirements for the
Degree of Doctor of Philosophy in Electrical Engineering

Abstract:

Resonant systems are pervasive in nature including such things as lasers, organ pipes and kindergarten swings. Such systems provide high amplitude, periodic output and because they recycle energy, use very little energy input. Often such systems must resonate multiple frequencies, as in an antenna. The shape of the antenna determines which frequencies will resonate. A large body of research has focused on **analyzing** systems to determine their frequency response in some narrow band.

Unfortunately, little work has explored how to **synthesize** a resonant system for a desired set of frequencies. This thesis presents a design procedure using impedance discontinuities (shape) to produce a resonator that supports the desired amplitude and phase relationships at each frequency of interest.

The basis for the tuning theory is the finding that a discontinuity at some location introduces a voltage and phase shift to the resonating waveform. The amount of shift is determined by the size of the impedance step and the current phase at the location of the discontinuity. Normally, this would present an intractable design problem because at a particular point each frequency has a different phase and so a different shift. However, another important conclusion is that at any point where the phase is a multiple of 90°, a discontinuity will introduce no phase shift. This effectively decouples different frequencies so that they can be tuned independently.

The space of applications for this tuning technique is quite broad. Some applications include acoustics, fluid dynamics, optics, electronics, RF antennas and power supplies. The thesis focuses on two applications: resonant clocks and resonant transformers.

The first application explores driving the clock of a microprocessor with a transmission line tuned to resonate the first few harmonics of a square wave. A 20MHz mockup demonstrated a factor of 10 power savings over an actively driven system. Further, Spice simulations showed a factor of 4 power savings at frequencies up to 1GHz. The other application is a resonator that can produce a trapezoidal waveform for an adiabatic system. A transmission line is tuned to shift the phase and voltage of an input square-wave, which is easy to produce, into a trapezoid by the far end of the line.

Thesis Supervisor: Dr. Thomas F. Knight, Jr.
Title: Senior Research Scientist

Acknowledgments

I would like to acknowledge the people who have made it possible for me to achieve my goals. Above all comes my family - my parents and my beautiful wife. Thank you, TK. (Dr. Thomas Knight) I'm glad you decided to take a chance on a young freshman 8 years ago. Your guidance has been wonderful. Lastly I would like to thank my thesis readers, Prof. Gill Pratt and Prof. Anantha Chandrakasan, who have challenged me to go that extra yard, with special thanks to Dr. Bob Sproull for taking time out to read these last few drafts.

Table of Contents

1. Introduction

Resonant systems are pervasive in nature. If you have ever watched the waves at the beach, listened to a trumpet play or pushed a child in a kindergarten swing, you have seen a resonant system in action. In the field of electrical engineering, resonant systems include antennas, AC power supplies and lasers, to name just a few examples.

Such systems provide high amplitude, periodic output and because they recycle energy, use very little energy input. For example, the kinetic energy at the bottom of a kindergarten swing is converted into potential energy as the swing rises, only to be "recovered" as the swing falls. A parent must add only enough energy to replace the energy lost to friction. Resonant systems recover energy in one form and redeliver it the next cycle. [Koller, Younis]

Often such systems must also resonate multiple frequencies, as in an antenna. The shape of the antenna determines which frequencies will resonate. This thesis presents a design procedure using impedance discontinuities (shape) to produce a resonator to support the desired amplitude and phase relationships at each frequency of interest.

1.1 Prior Related Work

The search of prior literature has ranged through a wide array of topics. The search began in acoustics, optics and mechanics. There is a tremendous body of research focused on analysis of distributed, resonant systems, but virtually none on synthesis. As a sampling, in the area of organ pipes, one of the oldest forms of resonant systems devised, the primary body of work describes organ construction as an art form rather than engineering. Some of the articles briefly delve into an analysis of how length relates to the harmonics or overtones present. The most interesting analysis work in the field of acoustics described the resonance of a few very common structures, such as the flare of a trumpet horn. [Benade]

A good portion of the literature involves time domain analysis and synthesis. In the area of transmission lines, some previous theoretical work focuses on analysis in the time domain. [Schutt, Dhaene] Their primary objective is to devise faster algorithms for calculating the reflections present when a quiescent line is disturbed by an impulse or step function. A few articles explore how to synthesize a transmission line to deliver a desired waveform in the time domain. [Burkhart, Hayden, Curtens] Often these experimenters are trying to devise a control system requiring a particular waveform. Again, they use a quiescent line that is disturbed by some impulse event.

From the application side, a number of recent inventions and papers have delved into using single frequency resonators to drive digital loads. [Tran, Reymond] Further inventions have used the resonant sine wave, not for power savings, but to synchronize physically distributed entities. [Chi]

Unfortunately, sine waves are not an optimal waveform to drive digital logic, because of their slow rise times. First, during the rise time inverters experience cross-over current which waste power: the longer the rise time, the more power.

Second, because certain digital devices have different thresholds, the lengthened rise time introduces additional skew. A more appropriate waveform would be a square wave with its fast rise times.

1.2 Overview of Synthesis Technique

In order to resonate a square wave, a single transmission line would have to resonate each of the harmonics that are present in that waveform. The following thesis explores a synthesis technique using impedance discontinuities (shape) to design a resonator that will support the desired amplitude and phase relationships at each frequency of interest. Further, this technique is applicable to any periodic waveform and can even be extended to other disciplines, like acoustics.

1.2.1 Basis of Tuning Theory

The basis for the tuning theory is the finding that a discontinuity in impedance at some location introduces a voltage and phase shift to the resonant standing waveform. The amount of shift is determined by the size of the impedance step and the phase of the standing wave at that location. Later chapters will explore this relationship in detail.

Please note that the tuning technique provides control through the standing waveforms, i.e. the waveform of voltage or current amplitude as a function of distance. In order to get instantaneous voltage or current, one simply needs to multiply this amplitude by the sinusoidal term related to time.

Let's follow through a basic example of tuning a transmission line for a single frequency, say 475MHz. Normally, this could be accomplished by increasing or decreasing the length of a uniform line until exactly one phase, or 180°, of the signal fits in the channel. At a velocity of $1x10^8$ m/s, a uniform line would need to be 10.5cm long in order for a 475MHz waveform to reach 180°. But for this example, let's assume that the length is too short, fixed at 8cm. The 475MHz signal would reach only 136.8° over the course of 8 cm.

Therefore, a discontinuity, such as the one shown in Figure 1.1, would have to make up the difference by adding a 43.2° phase shift (180° – 136.8°). The discontinuity appears at 2cm where the line transitions from an impedance of Z_a to an impedance of Z_b.

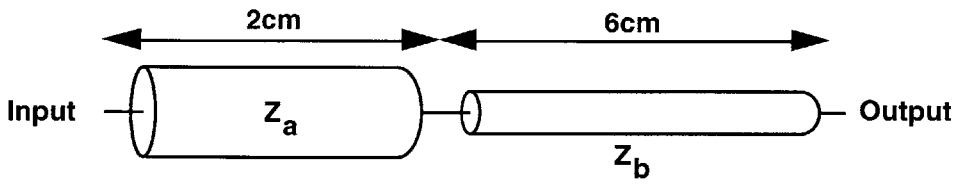

Figure 1.1. Tuning a Line for One Frequency

Figure 1.2 shows how the voltage standing wave undergoes a phase shift at the location of the discontinuity, 2cm. Signals on both sides of the discontinuity are of the same frequency, 475MHz, but the phase has been shifted by the desired

amount. Please note that the discontinuity has also introduced a voltage shift from the left side amplitude of 1 volt to a right side amplitude of almost 4 volts. This example will be revisited in more detail later.

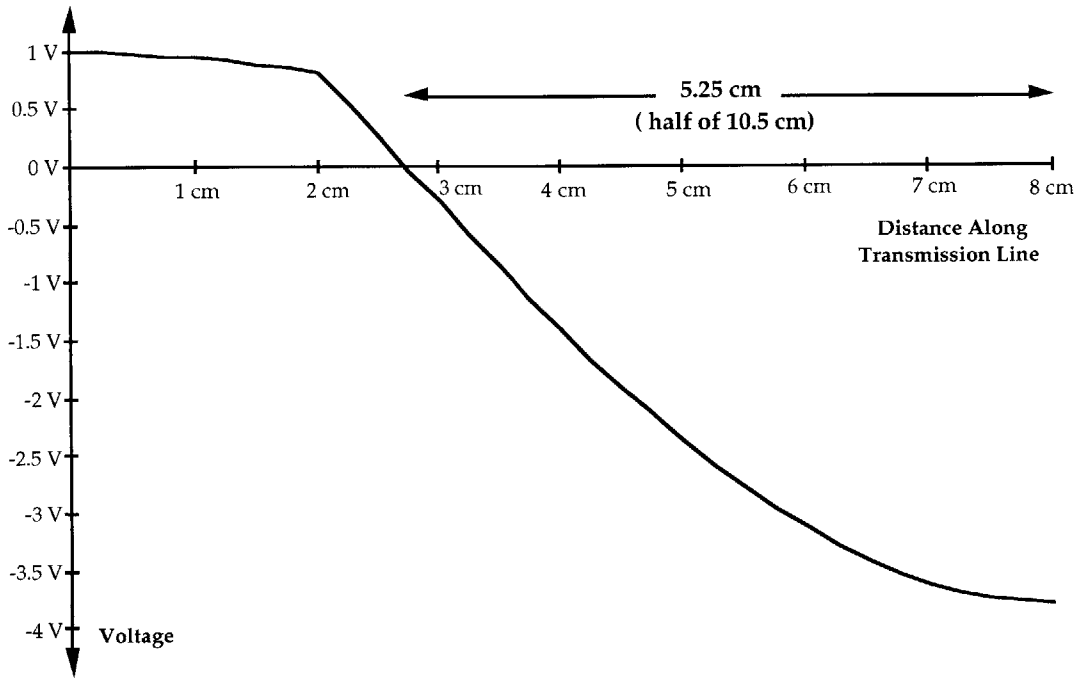

Figure 1.2. Voltage Amplitude on a Line Tuned for One Frequency

1.2.2 Multiple Frequency Tuning

The challenge for the synthesis technique is to apply tuning to multiple frequencies, simultaneously. Relating this back to the example above, we would have to tune the line to resonate 2 frequencies that aren't necessarily related. For larger numbers of frequencies, the design problem can become intractable because at a particular location each frequency has a different phase. The different phases translate into different required shifts in phase and voltage.

In order to overcome this challenge, another important conclusion is that any discontinuity located where the phase is a multiple of 90°, will introduce no phase shift. This effectively decouples different frequencies so that they can be tuned independently. These phase locations at multiple of 90° occur where either the voltage or current are equal to zero.

Figure 1.3 shows one of the more interesting applications explored in detail later. It shows a transmission line with 3 discontinuities placed at the voltage and current zeroes of a 3GHz waveform. Each section has a length of X and an impedance of Z_a, Z_b, Z_c or Z_d. The length is such that a full cycle, 360°, fits in the line. The standing waveform below the transmission line is plotted merely for reference. The amplitude of the standing wave may change from section to section depending on the discontinuities.

The discontinuity at 180° will not introduce either a phase or a voltage shift. The discontinuities at 90° and 270° will not introduce any phase shift but will alter the voltage by the ratio of the impedances.

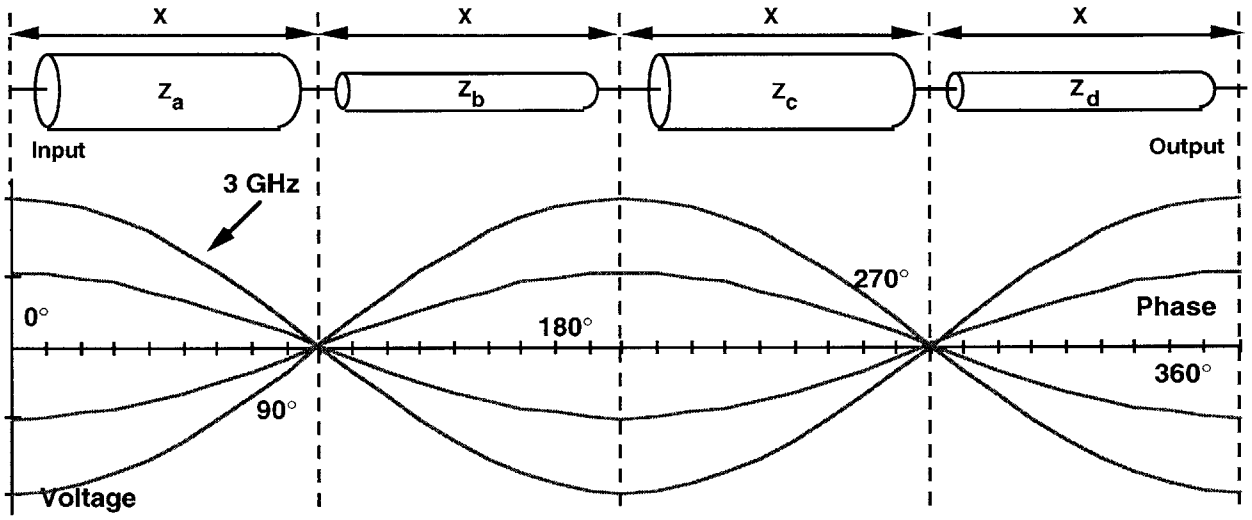

Figure 1.3. Discontinuities Located at Zeroes

Figure 1.4 shows the effect on a 1GHz signal in the same line. Since the left discontinuity occurs when the 1GHz signal is at 30°, a phase shift and a voltage shift are introduced. The same occurs at the right discontinuity. Note that the discontinuity at the center introduces just a voltage amplitude shift because the 1GHz frequency signal is also at a 90° phase point.

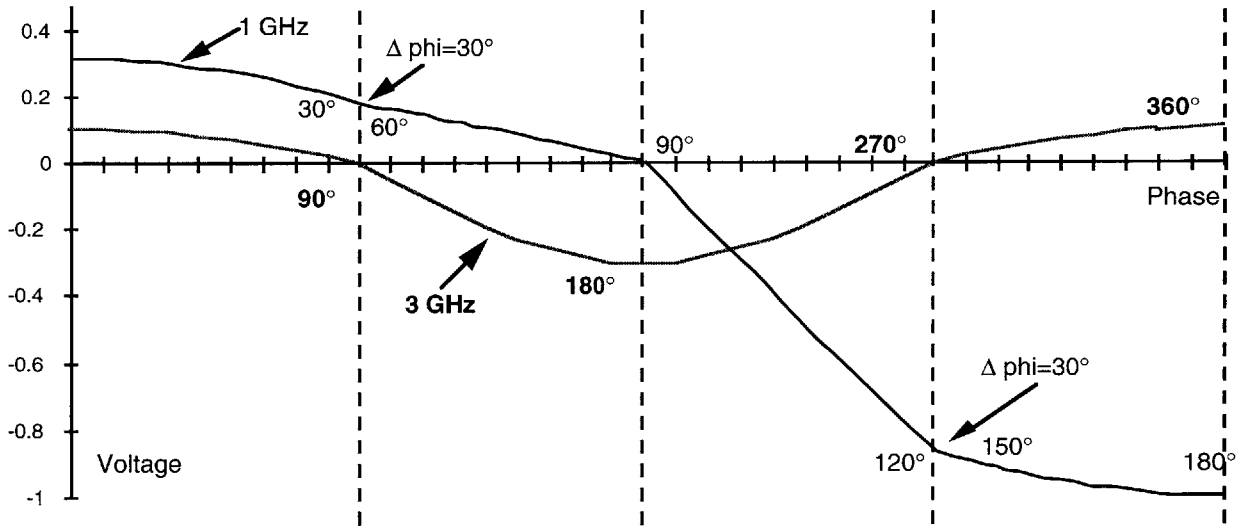

Figure 1.4. Affect on 1GHz Frequency Signal

Why is this interesting? Notice that the voltage amplitude at the left end of the line is 0.3 volts for the 1GHz signal and 0.1 volts for the 3GHz signal. The sum of

these two waveforms represents the first 2 harmonics of a 0.1 volt square wave. At the right end of the line, the 1GHz signal has an amplitude of -1 volt while the 3GHz signal has an amplitude of 0.11 volts. The sum of these two waveforms represents the first 2 harmonics of a 1 volt linear ramp waveform. The transmission line resonator has been tuned to not only fit two harmonics into a single line, but has also transformed the left signal from a square wave into a linear ramp by the far end of the line!

Note that at intermediate points along the line the voltage amplitudes will have varied according to their standing wave pattern. This means that the instantaneous voltage will be some random waveform associated with the sum of each of those frequency/amplitude components.

The thesis also explores using large impedance discontinuities to linearize the phase shift part of the problem. Finally, the theory section includes lumped elements into the tuning equations. These lumped elements can model existing loads that might cause phase and voltage shifts that must be accounted for. Or these elements can be used for tuning.

1.3 Applications

The space of applications for this tuning technique is quite broad. Some applications include acoustics, fluid dynamics, optics, electronics, RF antennas and power supplies. The thesis focuses on two applications: resonant clocks and resonant transformers.

1.3.1 Resonant Clocks

Over the years a number of trends have increased the power consumption of the clock drivers in standard digital systems. First, the clock capacitance has steadily increased as the die size and the gate capacitance have become larger. Second, the clock frequency is increasing. Clock drivers on today's micro-processor chips must drive a 4 nF load at 500 MHz. This burns a very significant 40% of the overall chip power. [Bowhill]

As mentioned before, the big benefit of using a tuned transmission line to drive a clock load is that most of the energy to drive the capacitance, comes from the line instead of the power supplies. Therefore, the clock power consumption falls to just the amount burnt in the parasitic resistance of the transmission line. In our micro-processor example this can amount to a factor of 10 in power savings. Another benefit explored later is that the instantaneous voltage transitions through $1/2\ V_{DD}$ simultaneously across the entire transmission line. This translates to virtually no skew across a single die.

The micro-processor example is nice and simple, because the driver and capacitive load are collocated, so that we only care about the signal at one location. This lets us ignore the voltage shifts at each discontinuity and just design the cavity for the phase. Further, just a few harmonics are necessary to produce a high quality square wave.

A large scale mockup has proven the viability of the transmission line clock driver technique. At 20 Mhz a transmission line clock driver with uniform

impedance reduces power consumption by a factor of 5.8 relative to a standard clock driver. Using a tuned transmission line saves a factor of 9.5 over the standard driver. The quality of waveforms is significantly better for the tuned transmission line. Further, Spice simulations showed a factor of 4 power savings at frequencies up to 1GHz.

1.3.2 Resonant Transformers

Another more challenging application lies in the area of signal conversion as briefly mentioned above. The end of the theory chapter explores an example application to convert a square wave input into a trapezoidal output for an adiabatic system. [Younis] The adiabatic system utilizes charge recovery from data values to reduce power consumption.

The value of using a square-wave input is that it is very simple to produce without consuming much power. Also the two waveforms share the same frequency components, but in varied amounts. Over the length of line, the voltage of each frequency component in the square wave must be altered to a new desired value. Further, the first and third harmonics of the square wave have the same sign, while the first and third harmonics of the trapezoid are of opposite sign. This means that either the first harmonic or the third harmonic must be phase shifted so that it is 180° out of phase.

One important item to note is that the resonate transformer can just as easily step up a voltage level, as step down a voltage level. The input waveform does not limit the scope of the output waveform. The primary limitation arises from the quality of the resonator, i.e. parasitics, and from the amount of power being actively consumed by the load versus the amount of power supplied by the driver.

1.4 Outline

Chapter 2 reviews basic transmission line theory. This includes inductance and capacitance of a simple parallel stripline. From these, impedance and velocity can be calculated. The chapter explores the basics of resonant cavities including terminations, reflections and sinusoidal resonance. The primary purpose is to set the stage for the next chapter.

Chapter 3 explores the core of the thesis, namely tuning resonant transmission lines. It begins by describing the pair of equations that govern the waveform in the presence of a discontinuity. The chapter then explains some of the characteristics of impedance variations. It next uses the resonant transformer application to illustrate how to linearize the problem and utilize zeroes. Finally, chapter 3 introduces lumped elements into the framework.

Chapter 4 presents the central application explored, resonant clock drivers for standard microprocessors. The chapter begins with the basics and then explains how to drive such a system using a resonant transmission line. The chapter describes a 20MHz mockup that demonstrates the viability of the technique. The chapter concludes by describing the 1GHz simulations.

Chapter 5 explores the practical issues encountered in building a transmission line resonator. The beginning focuses on how to build a transmission line with a

sufficiently low impedance to drive common loads. Then the chapter delves into the effects of parasitic resistance on velocity and voltage. Finally, the chapter tries to quantify the effect of system variability on resonance, including load, length and impedance variation.

Chapter 6 revisits the important ideas presented throughout this thesis. And it tries to fit this work into the space of what remains to be explored.

Finally, an appendix provides the schematics used in the 1GHz simulations.

2. Review of Transmission Line Theory

2.1 Introduction

The following chapter is meant to review basic transmission line theory with an eye towards Equation 2.8 relating voltage and current on a resonating line. The first section, 2.2, begins the review with the LC ladder model, impedance and velocity. Section 2.3 calculates the impedance and velocity of an example used later in the application chapter. Then, section 2.4 explores time domain reflections due to line terminations.

Building on the termination discussion, Section 2.5 focuses on the most important subset of waveforms, sinusoids. This leads to the important result showing that the voltage and current standing waves are related by a derivative embodied in Equation 2.8. This result will begin the next chapter and lead to the synthesis technique for resonant lines.

2.2 Basic Theory

Figure 2.1 shows the circuit model equivalent for an ideal transmission line. The line is sectioned into stages each with an inductor and capacitor. L represents the inductance per unit length and C is the capacitance per unit length. Each section of the LC ladder has a capacitance of C times the distance of the section, dx, and has an inductance of L times the distance. As dx approaches zero, the number of stages approaches infinity and the line begins to approximate a transmission line.

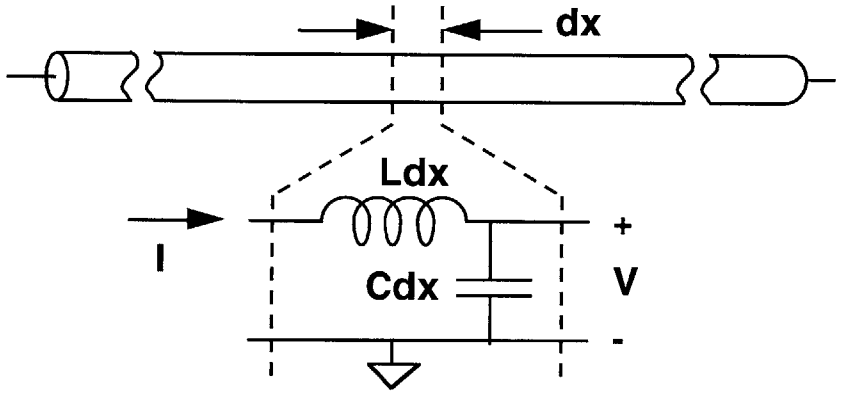

Figure 2.1. Circuit Model of Transmission Line

The inductor in Figure 2.1 introduces a voltage step based on the slope of the current.

$$V_{right} - V_{left} = \partial V = -(L_l \partial x)\frac{\partial I}{\partial t}$$

The equation can be re-written by pulling the dx expression into the denominator. Following the lead of field theory, let's take the partial derivative with respect to time.

$$\frac{\partial V}{\partial x} = - L_1 \frac{\partial I}{\partial t} \qquad \text{or} \qquad \frac{\partial^2 V}{\partial x^2} = - L_1 \frac{\partial^2 I}{\partial x \partial t}$$

Equation 2.1

At the right common node in Figure 2.1, the current encounters a step based on the slope of the voltage. This is caused by the capacitor drawing charge to support a new voltage level.

$$I_{right} - I_{left} = \partial I = -(C_1 \, dx)\frac{\partial V}{\partial t}$$

As before, the equation can be re-written by pulling the dx expression into the denominator and taking the partial derivative with respect to distance.

$$\frac{\partial I}{\partial x} = - C_1 \frac{\partial V}{\partial t} \qquad \text{or} \qquad \frac{\partial^2 I}{\partial t \partial x} = - C_1 \frac{\partial^2 V}{\partial t^2}$$

Equation 2.2

The wave equation relating time and distance for signals traveling down the transmission line can be computed from the above derivations, Equation 2.1 and Equation 2.2.

$$\frac{\partial^2 V}{\partial x^2} = L_1 C_1 \frac{\partial^2 V}{\partial t^2}$$

Equation 2.3

Canceling the $\partial^2 V$ terms on either side and simplifying leaves the definition of velocity. As will be shown later the velocity, v, is dependent only on the intrinsic characteristics of the transmission line.

$$\frac{1}{\partial x^2} = L_1 C_1 \frac{1}{\partial t^2} \Rightarrow \frac{\partial x^2}{\partial t^2} = \frac{1}{L_1 C_1} \Rightarrow v = \sqrt{\frac{1}{L_1 C_1}}$$

Equation 2.4

The general solution to the wave equation, Equation 2.3, is

$$V(x,t) = F\left(t + \frac{x}{v}\right) + G\left(t - \frac{x}{v}\right)$$

Let's substitute this into either Equation 2.1 or Equation 2.2, integrate and solve for the impedance, Z. Impedance is the effective resistance of the transmission line, Z=V/I.

$$Z_o = \text{impedance} = \sqrt{\frac{L_1}{C_1}}$$

Equation 2.5

2.3 Calculating Impedance and Velocity

Probably the simplest form of transmission line to analyze is the strip line as shown in Figure 2.2. This type of line is also easy to build in a ceramic package or PCB. The impedance of the line in Figure 2.2 is related to the dielectric constant of the insulator, the spacing and width. The velocity is solely dependent on the dielectric.

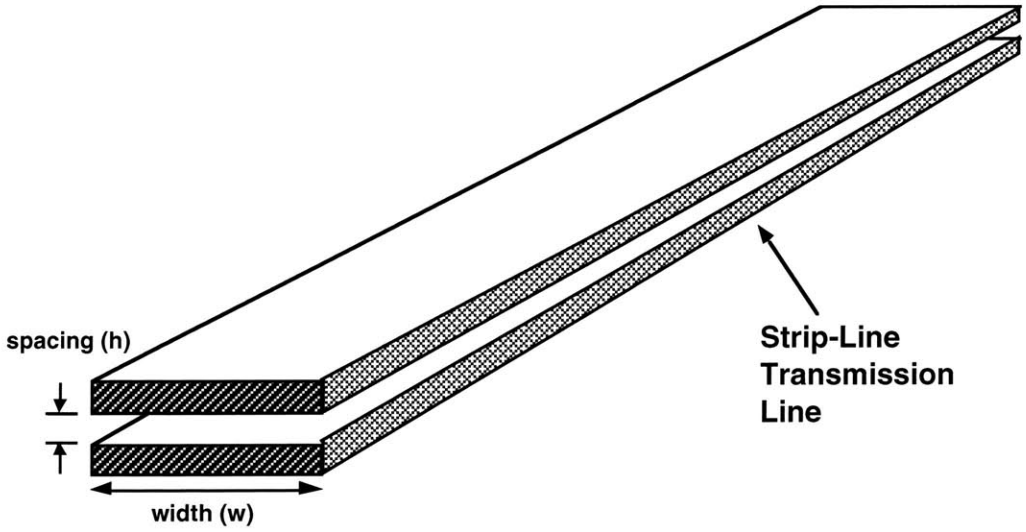

Figure 2.2. Strip Line Transmission Line

The capacitance per unit length and the inductance per unit length can be estimated from basic principles. In the equations below, w corresponds to the width of the conducting plates and h to the spacing between them. ε_o corresponds to the relative dielectric constant of the insulator. These equations neglect fringe fields at the edge of the conductors, which for smaller width lines can be quite significant. Chapter 5 will briefly explore the effect and use of fringing fields.

$$C_1 = \varepsilon_o \left(8.85 \times 10^{-12}\ \text{F/m}\right)\left(\frac{w}{h}\right)$$

$$L_1 = \left(4\pi \times 10^{-7}\ \text{H/m}\right)\left(\frac{h}{w}\right)$$

Let us work through some example numbers that will be used for the application explored in chapter 4. This application requires a low impedance line,

i.e. wide lines, closely spaced together. The width, w, is limited to 2 cm, so that the line can fit under a chip. Current industrial processes limit the spacing, h, to 50 μm. Finally, higher dielectric constant insulators can raise the capacitance and lower the impedance. However, we don't want to use any material that is too exotic or too difficult to work with. This limits the dielectric constant to about 9. Plugging in these numbers yields capacitance and inductance per unit length.

$$C_l = 9\left(8.85\times10^{-12}\text{F/m}\right)\left(\frac{2\text{cm}}{50\mu\text{m}}\right) = 3.19\times10^{-8}\text{F/m}$$

$$L_l = \left(4\pi\times10^{-7}\text{H/m}\right)\left(\frac{50\mu\text{m}}{2\text{cm}}\right) = 3.14\times10^{-9}\text{H/m}$$

These values can be used to calculate both impedance and velocity using Equation 2.4 and Equation 2.5.

$$Z_o = \sqrt{\frac{L_l}{C_l}} = \sqrt{\frac{3.14\times10^{-9}\text{H/m}}{3.19\times10^{-8}\text{F/m}}} = 0.314\Omega$$

$$v = \frac{1}{\sqrt{L_l C_l}} = \frac{1}{\sqrt{\left(3.14\times10^{-9}\text{H/m}\right)\left(3.14\times10^{-8}\text{F/m}\right)}} = 1\times10^{8}\text{m/s}$$

In the applications we shall discover that driving a voltage into a capacitive load requires a very low impedance line. The impedances must be a large factor smaller than that achieved with a single strip line. In chapter 5 we shall explore methods to reduce the impedance further by ganging lines stacked both vertically and horizontally.

2.4 Reflection Coefficient and Terminations

In a transmission line there can be both forward propagating and backward propagating waveforms as shown in Figure 2.3. These waveforms do not affect each other in a uniform line. Individually the voltage and current are related by the impedance to $V_+=I_+Z_o$ and $V_-=I_-Z_o$.

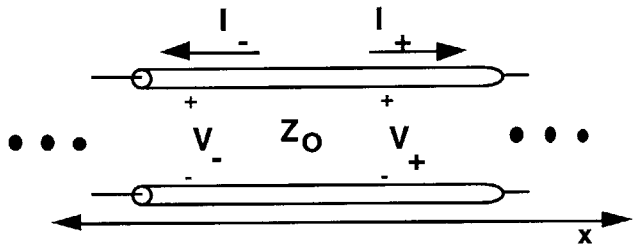

Figure 2.3 A Section of a Uniform Transmission Line

The voltage at any particular point would be the sum of the forward and reverse propagating waves. The instantaneous current would be the difference of the forward and reverse waves.

$$V(x,t) = V_+(x,t) + V_-(x,t)$$

Equation 2.6

$$I(x,t) = I_+(x,t) - I_-(x,t) = \frac{V_+(x,t)}{Z_0} - \frac{V_-(x,t)}{Z_0}$$

Equation 2.7

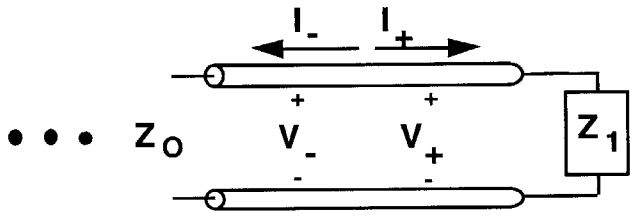

Figure 2.4 Transmission Line Terminated with Impedance Z_1

Figure 2.4 shows a terminated line where the impedance undergoes a step from Z_0 to Z_1. The termination constrains the reverse wave to be a function of the forward wave and the load impedance. First, the combined voltage and current at the termination are related by $V=Z_1I$. Substituting the voltage and current from Equation 2.6 and Equation 2.7 yields:

$$V_+ + V_- = Z_1\left(\frac{V_+}{Z_0} - \frac{V_-}{Z_0}\right)$$

Below we solve for V_-/V_+, which represents the reflection coefficient, R. This coefficient relates the outgoing voltage, V_-, to the incoming voltage, V_+.

$$R = \frac{V_-}{V_+} = \left(\frac{Z_1 - Z_0}{Z_1 + Z_0}\right)$$

Three special cases provide some useful insight. When $Z_1 = Z_0$ (infinite, uniform line), R = 0 and no reflection occurs. When $Z_1 = 0$ (short circuit), R = -1 and the reflected wave is equal and opposite. This means that the combined voltage must be zero, while the combined current is twice the forward current. Finally, when $Z_1 = \infty$ (open circuit), R = 1 and the reflected wave is equal. The combined voltage will be double the incoming voltage and the current will be zero.

2.5 Sinusoids on Transmission Lines

This section focuses on the transmission line shown in Figure 2.5 with an impedance of Z_O. As drawn this transmission line terminates at x = 0 in an open circuit and the line extends to infinity in the positive x direction.

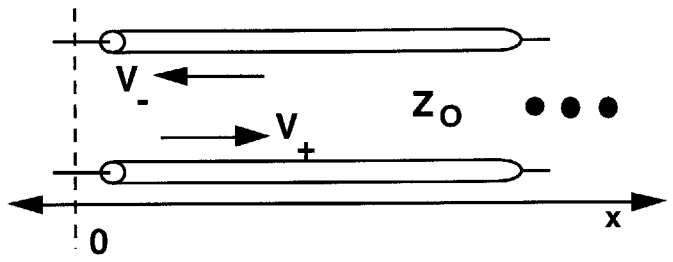

Figure 2.5 Transmission Line with Open Termination at x=0

One very important set of waveforms that can resonate within this line is sinusoidal. From the wave equation, Equation 2.3, we know that the most general solution would consist of a pair of waveforms traveling in opposite directions. These waveforms would take the form of F(t-x/v) and G(t+x/v). Because the line is terminated in an open circuit, the voltages for the reverse wave and forward wave must be equal, leading to the following two equations. As shown below these can be rewritten in exponential form for easy manipulation.

$$V_+(x,t) = \frac{V}{2}\sin\left(\omega t - \frac{\omega x}{v}\right) = \frac{V}{2}\frac{e^{j\omega t}e^{-j\frac{\omega x}{v}} - e^{-j\omega t}e^{j\frac{\omega x}{v}}}{2j}$$

$$V_-(x,t) = \frac{V}{2}\sin\left(\omega t + \frac{\omega x}{v}\right) = \frac{V}{2}\frac{e^{j\omega t}e^{j\frac{\omega x}{v}} - e^{-j\omega t}e^{-j\frac{\omega x}{v}}}{2j}$$

The voltage at any particular point would be the sum of these waveforms as shown below. Below we proceed with the sum and group like terms.

$$V(x,t) = V_+(x,t) + V_-(x,t)$$

$$V(x,t) = \frac{V}{2\times 2j}\left[e^{j\omega t}\left(e^{j\frac{\omega x}{v}} + e^{-j\frac{\omega x}{v}}\right) - e^{-j\omega t}\left(e^{j\frac{\omega x}{v}} + e^{-j\frac{\omega x}{v}}\right)\right]$$

Once the terms are fully separated, each can be divided by 2 and 2j and resolved back into sin's and cos's. Note that the equation for voltage along the line varies independently with time and distance. Essentially, the cos term sets the maximum amplitude, while the sin term sets the temporal behavior.

$$V(x,t) = V\left(\frac{e^{j\omega t} - e^{-j\omega t}}{2j}\right)\left(\frac{e^{j\frac{\omega x}{v}} + e^{-j\frac{\omega x}{v}}}{2}\right) = V\sin(\omega t)\cos\left(\frac{\omega x}{v}\right)$$

In the above equation ω/v is equivalent to $(2\pi/\text{wavelength})$ or $2\pi/\lambda$. Therefore, at intervals of $x=0$, $\lambda/2$, λ, etc., the voltage simplifies to a full sinusoid in time and the current is zero. Conceptually, this corresponds to points in which the forward and reverse voltage waves must be equal. Inserting an open circuit and removing the remainder of the line at any such point will have no effect on the above resonance.

At intervals of $x=\lambda/4$, $3\lambda/4$, etc., the current simplifies to a full sinusoid in time and the voltage is zero. Conceptually, this corresponds to points in which the forward and reverse current waves must be equal. Inserting an short circuit and removing the remainder of the line will have no effect on the resonance.

Figure 2.6 shows how the voltage varies over the length of the line. Multiple snapshots of time are shown. At distances from the origin that are multiples of $\lambda/2$ the voltage represents a maximum sinusoid. When shifted by $\lambda/4$ the voltage is a minimum with a voltage of zero for all time.

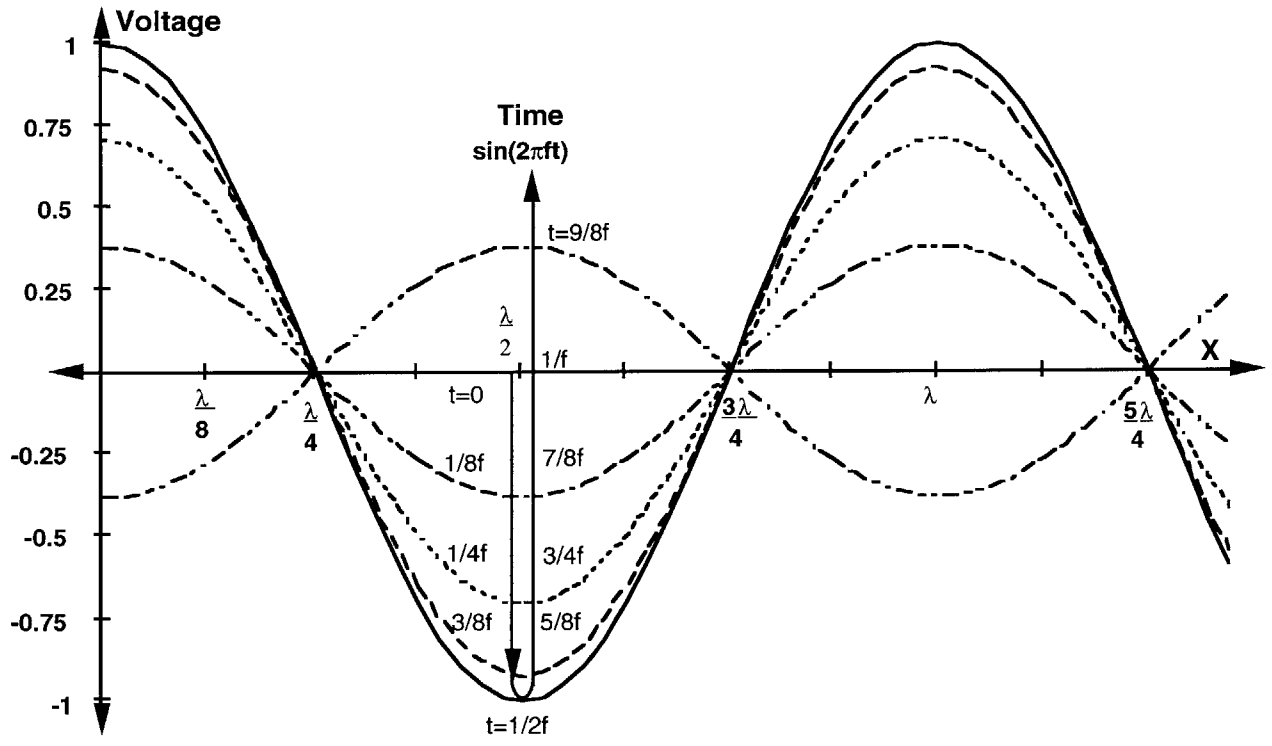

Figure 2.6 Voltage(x, t) on Open Terminated Line Resonating a Sinusoid

The same procedure can be used to solve for I(x, t) for the line in Figure 2.5 with the open termination at x=0. The current as a function of distance and time can be solved for in the same manner as with voltage.

$$I(x,t) = -\frac{V}{Z_o}\cos(\omega t)\sin\left(\frac{\omega x}{v}\right)$$

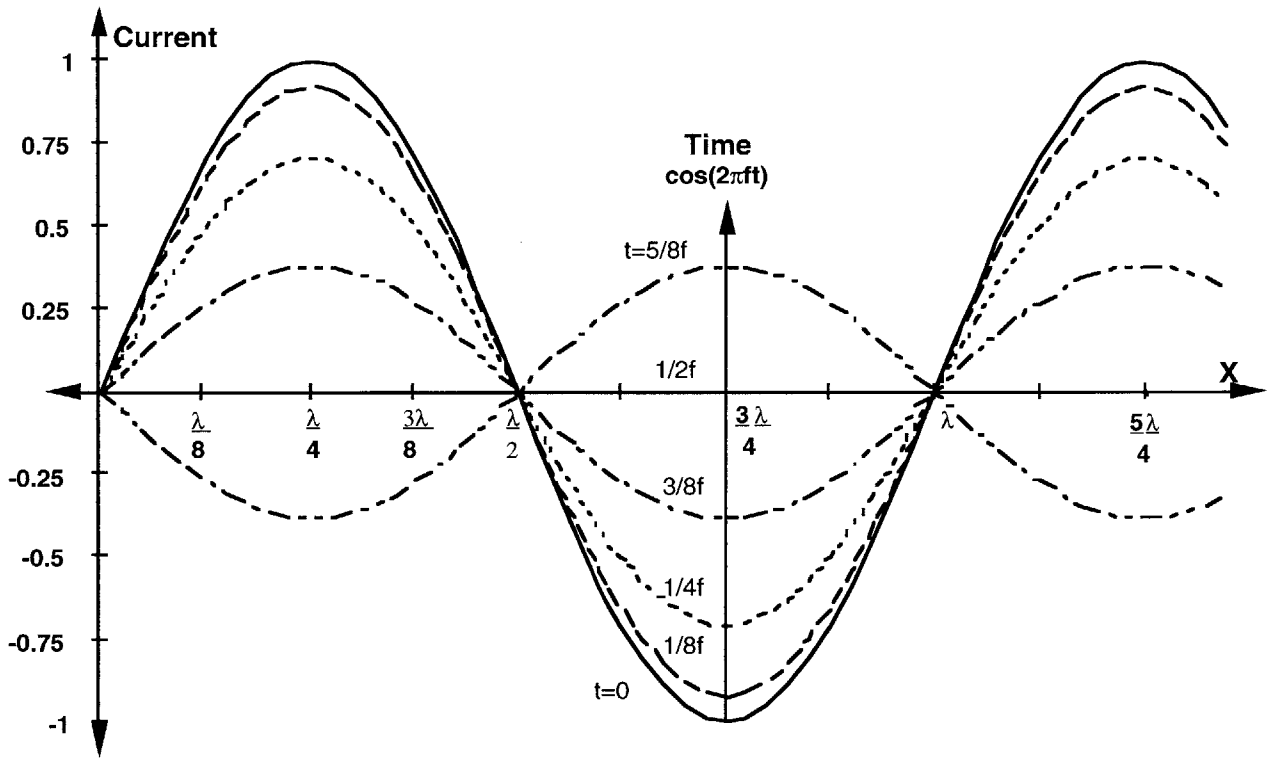

Figure 2.7 Current(x, t) on Open Terminated Line Resonating a Sinusoid

Figure 2.7 plots the current as function of distance for multiple snapshots of time. The current is sinusoidal in distance and time, but the time component is phase shifted by 90° relative to voltage. This is interesting because the current as a function of distance, I_x, represents the slope of the V_x. This relationship is captured in Equation 2.8. and will be used as the foundation for describing more complex transmission lines in the next chapter.

$$I_x = \frac{k}{Z_o}\frac{\partial V_x}{\partial x} \quad \text{where } k = \frac{\lambda}{2\pi}$$

Equation 2.8

3. Impedance Discontinuity Theory

3.1 Introduction

The following theory describes how to design a line that will resonate a desired waveform. Most transmission line theory focuses on the problem of analysis. By contrast this theory focuses on synthesis: specify the desired waveform and derive the line from the constraints implied by that waveform.

This chapter begins with the basic principles of a resonating transmission line. The next section illustrates the implications for synthesis in one simple example. Then, the chapter introduces phase boundaries and zeros. This is followed by another example. The final section describes a way to linearize the synthesis problem.

3.2 Basic Theory

The following theory is based on a few very simple facts. First, in a uniform line the voltage and current form a standing wave that is sinusoidal as a function of distance. Second, current and voltage are related by a derivative and the impedance, $I_x R = k dV_x/dx$. And finally, the voltage and current must be continuous along the line, even at an impedance discontinuity. This leads to the following equations for voltage across a discontinuity:

$$V_a \cos\left(\frac{2\pi f}{v}x\right) = V_b \cos\left(\frac{2\pi f}{v}x + \Delta\Phi\right)$$

Equation 3.1

and current across a discontinuity:

$$\frac{V_a}{Z_a}\sin\left(\frac{2\pi f}{v}x\right) = \frac{V_b}{Z_b}\sin\left(\frac{2\pi f}{v}x + \Delta\Phi\right)$$

Equation 3.2

V_a and Z_a represent the voltage amplitude and impedance to the left of the discontinuity. V_b and Z_b represent the voltage amplitude and impedance to the right of the discontinuity. The velocity in the line appears as "v" and "f" represents the frequency. The phase of the signal to the left of the discontinuity appears inside the left cos and sin terms. The phase to the right appears inside the right cos and sin terms. Note that this has been written in terms of the phase on the left shifted by some $\Delta\phi$.

As Equation 3.1 states, for a given waveform, the voltage will be continuous at all points in space. However, its slope, dV_x/dx, will not remain continuous. Since the voltage and current are related by a derivative, the slope changes by the impedance ratio across the boundary. So if going into the discontinuity the slope of the voltage standing wave is 3 and Z_b/Z_a is 2, then the slope in the next section

would be 6. This corresponds to a different phase and voltage amplitude, hence the use of V_b and $\Delta\phi$.

When dealing with multiple frequencies on a single line, at any given point along a line, they will have different phases. This means that a discontinuity at a particular point will introduce different voltage and phase shifts depending on the frequency. We can use this concept to tune a line.

3.3 A Simple Example of Tuning

Let's look at a simple example to drive the point home. Assume we want to make a given line resonate at a given frequency. Normally this can be achieved by changing the length of the line to match some multiple of half of the wavelength. However, in this example we are going to assume the length is fixed, fixed at a value we don't want. To resonate the desired frequency, we'll introduce an impedance variation to add phase to the signal so that it fits in the line.

Figure 3.1 shows the line involved, where X_a and X_b are fixed:

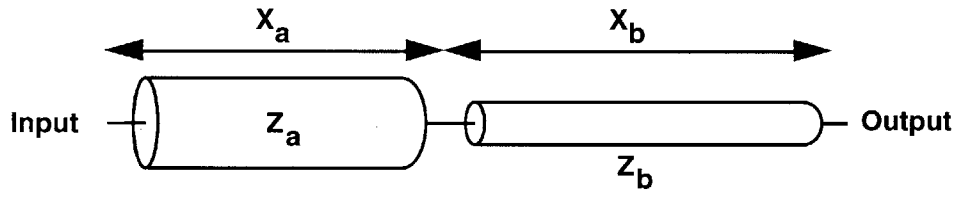

Figure 3.1. Example of Tuning a Line for One Frequency

The basic equations relating voltage and current at this discontinuity appear below. They assume that the entire transmission line will resonate a half wavelength. This condition appears as π - $F(X_b)$ in the right cos and sin terms. The idea is that the beginning of the line needs to have a phase of 0 and we have moved forward a distance, X_a, to get to the discontinuity. For the end of the line the phase needs to be π in order to reflect properly and we are moving back a distance, X_b, from the end of the line.

$$V_a \cos\left(\frac{2\pi f}{v} X_a\right) = V_b \cos\left(\pi - \frac{2\pi f}{v} X_b\right)$$

$$\frac{V_a}{Z_a} \sin\left(\frac{2\pi f}{v} X_a\right) = \frac{V_b}{Z_b} \sin\left(\pi - \frac{2\pi f}{v} X_b\right)$$

For this example, let's resonate a 475 MHz sinusoid in a 8 cm line with a velocity of $1x10^8$ m/s. For a uniform line to resonate at this frequency, it would have to be 10.5cm long. The 475 MHz signal would reach only 136.8° over the course of 8 cm. In order to reach half a wavelength it needs to be at 180° by the end of the line. Therefore, the discontinuity must make up the difference by adding a 43.2° phase shift (180° – 136.8°).

In this example, let's limit ourselves to one impedance variation located at, say, X_a = 2cm (X_b = 6cm). Finally, we will arbitrarily assume an initial impedance of Z_a = 5Ω and a V_a = 1 volt input amplitude. Let's plug in the numbers we know:

$$(1\text{Volt})\cos\left(\frac{2\pi\times 475\text{MHz}}{1\times 10^8\text{m/s}}\,0.02\text{m}\right) = V_b\cos\left(\pi-\frac{2\pi\times 475\text{MHz}}{1\times 10^8\text{m/s}}\,0.06\text{m}\right)$$

$$\frac{(1\text{Volt})}{5\Omega}\sin\left(\frac{2\pi\times 475\text{MHz}}{1\times 10^8\text{m/s}}\,0.02\text{m}\right) = \frac{V_b}{Z_b}\sin\left(\pi-\frac{2\pi\times 475\text{MHz}}{1\times 10^8\text{m/s}}\,0.06\text{m}\right)$$

Solving the first equation gives a value of 3.791V for V_b. Plugging this into the second equation yields 32.91Ω for the impedance of the b section. This tells us that a line composed of a 2 cm section at 5Ω and a 6 cm section at 32.91Ω will resonate a 475 MHz waveform. Also it will convert the input amplitude from 1V to an output amplitude of 3.791V. At the end of the 2 cm section the phase is 34.2° and the discontinuity adds the 43.2° phase shift.

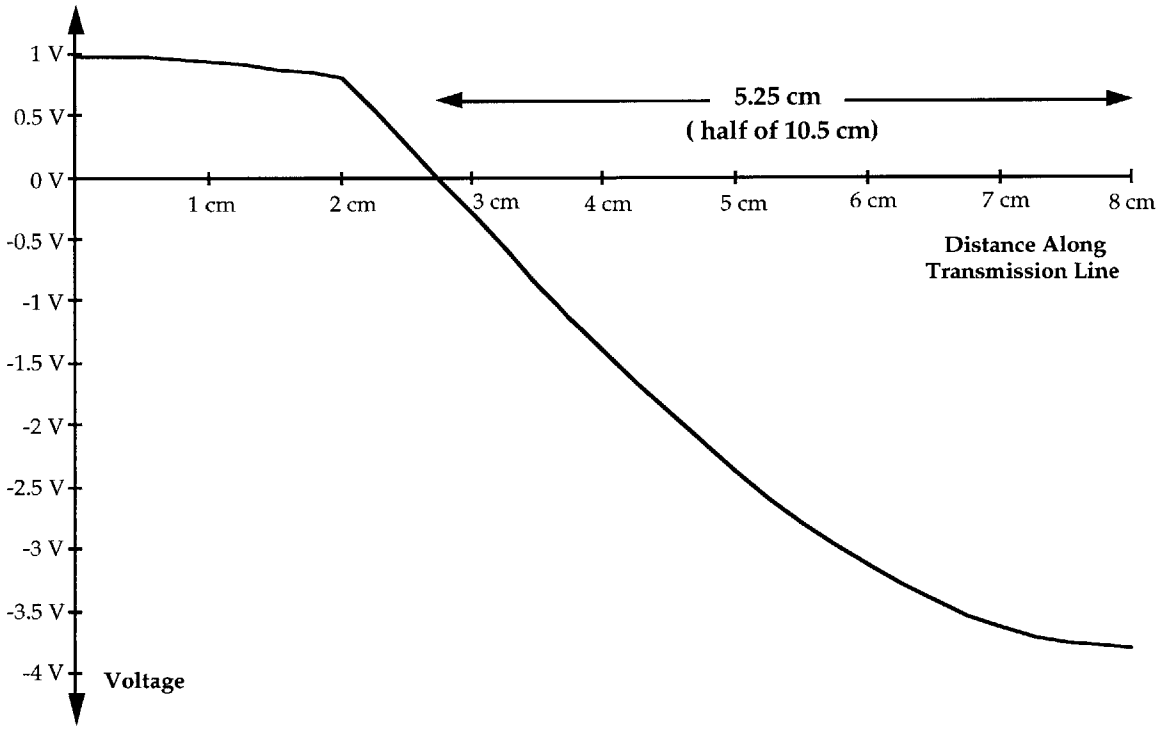

Figure 3.2. Voltage Amplitude on a Line Tuned for One Frequency

Figure 3.2 shows the voltage amplitude as a function of distance along the line. It is quite apparent that the discontinuity occurs at 2 cm. Both sides of the discontinuity have the same frequency component, but at the discontinuity a large phase shift has been introduced. The change in slope is directly related to the impedance ratio. Note that the distance from when the amplitude voltage V=0 to

V=–maximum, or 90° of phase, matches the 5.25cm for a quarter wavelength of a 475MHz waveform.

Figure 3.3 shows the current amplitude as a function of distance along the line. Just as with the voltage, it is quite apparent that the discontinuity occurs at 2cm.

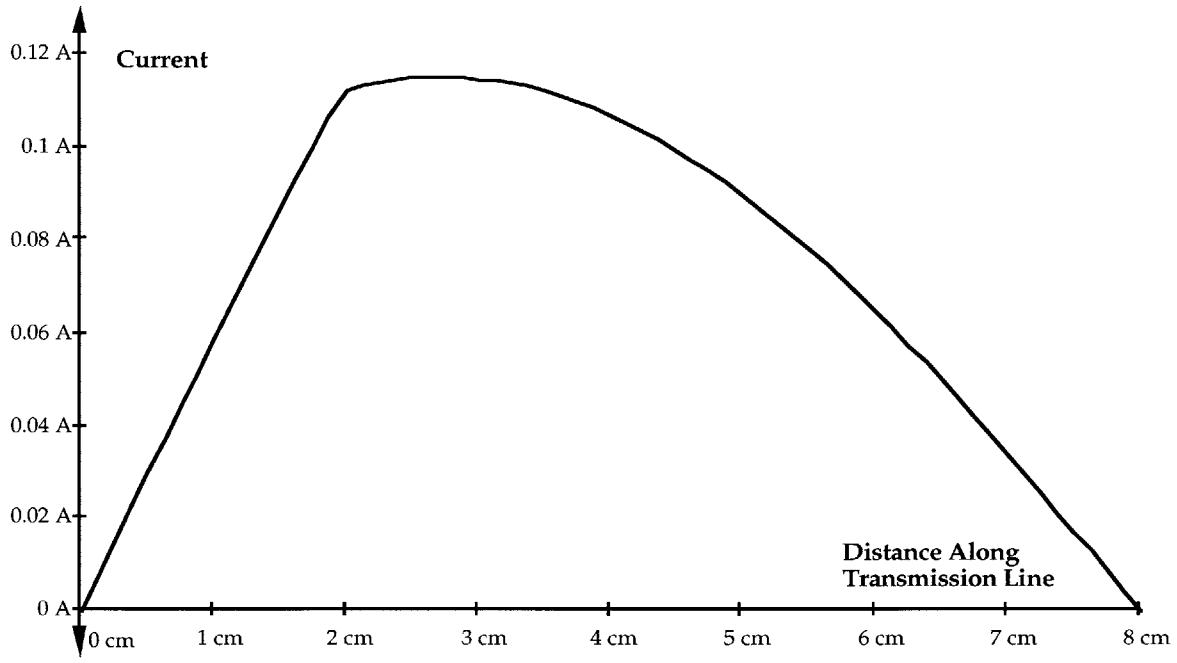

Figure 3.3. Current on a Line Tuned for One Frequency

3.4 Phase Boundaries

This section introduces the idea of phase boundaries. These appear at multiples of 90°. A phase boundary is a phase point that cannot be crossed by introducing a phase shift with an impedance change. After a brief description, this section illustrates the concept with an example.

There are two causes for phase boundaries, one related to voltage and the other related to current. Trying to cross 90° or 270°, the voltage phase boundary, requires that the cos term in Equation 3.1 changes sign. Since V_a and V_b are just amplitudes (no negatives), the left and right sides cannot be equal. Hence we cannot introduce a phase shift to cross this boundary.

Crossing 0° or 180°, the current phase boundary, means that the cos terms in Equation 3.1 will have the same sign. However in Equation 3.2, the sin terms will have different signs. In order to make the two sides equal, we would need a negative impedance. Since we cannot physically produce a negative impedance, we cannot introduce a phase shift to cross this boundary.

Said simply, an impedance discontinuity cannot introduce a sign reversal in the voltage standing wave or the current standing wave.

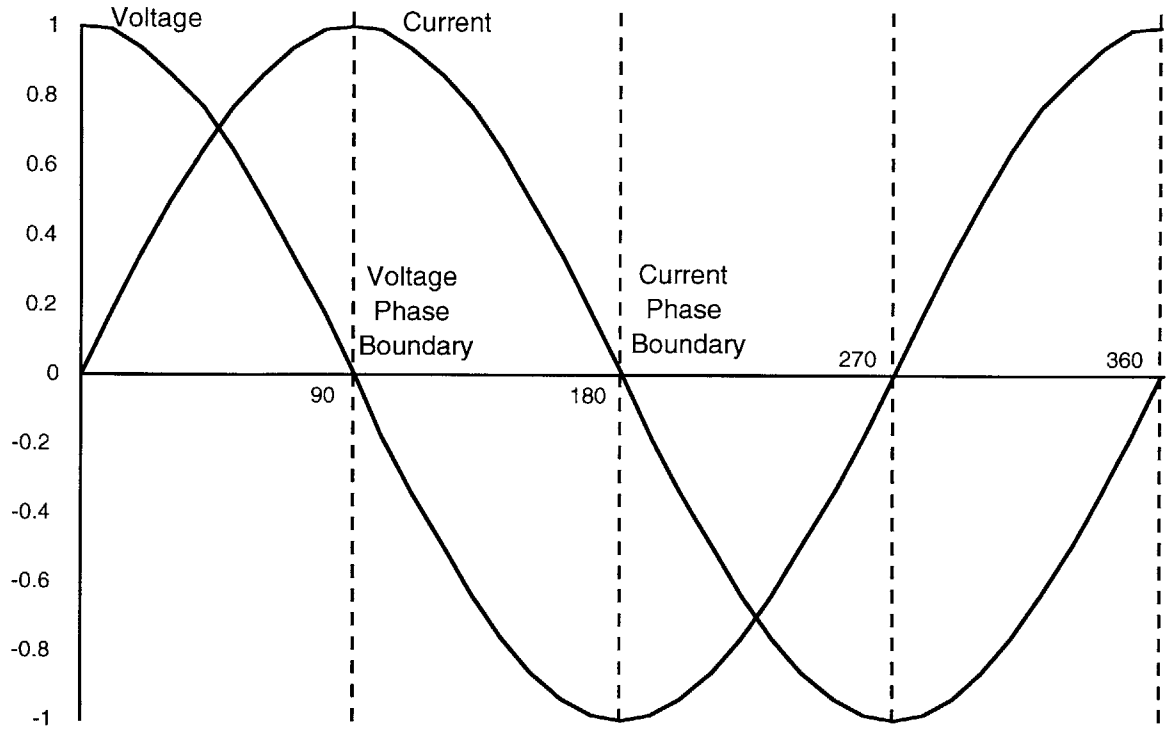

Figure 3.4. Voltage and Current Waveforms

3.4.1 Phase Boundary Example

The best way to illustrate phase boundaries is to break our previous example by trying to cross one. In this case, let's resonate a 475 MHz sinusoid in a **6 cm** line with a velocity of $1x10^8$ m/s. Again, let's limit ourselves to one impedance variation located at 2 cm, an initial impedance of 5Ω and a 1V input amplitude. The 475 MHz signal would reach only 102.6° over the course of 6 cm. In order to reach half a wavelength, the discontinuity must add 77.4°.

Note that we are not shifting more than 90°. However, at the location of the discontinuity the phase is already 34.2°. With the addition of 77.4° we would cross the 90° phase boundary to 111.6°. This would require a negative amplitude. Let's plug the numbers into Equation 3.1 and see it happen:

$$1\cos\left(\frac{2\pi\times 475\text{MHz}}{1\times 10^8\text{m/s}}\,0.02\text{m}\right) = V_b\cos\left(\pi-\frac{2\pi\times 475\text{MHz}}{1\times 10^8\text{m/s}}\,0.04\text{m}\right)$$

Solving the voltage equation yields a value of -2.247V for V_b. Since a negative amplitude can't happen, we can't get across this phase boundary. If we continue and plug these numbers into Equation 3.2, we get the following:

$$\frac{1}{5\Omega}\sin\left(\frac{2\pi\times 475\text{MHz}}{1\times 10^8\text{m/s}}\,0.02\text{m}\right) = \frac{V_b}{Z_b}\sin\left(\pi-\frac{2\pi\times 475\text{MHz}}{1\times 10^8\text{m/s}}\,0.04\text{m}\right)$$

The current equation yields an impedance of -18.58Ω for the right section. Since we can't create a negative impedance, we can't resonate a 475 MHz sinusoid in a 6 cm line with only one discontinuity at 2 cm. If we move the discontinuity back to 0.5 cm, the line can resonate, because the phase shift does not cross a boundary.

3.5 Discontinuities at Zeroes

The tuning method presented above scales badly for larger numbers of frequencies. One method of simplifying the problem involves properly locating the discontinuities.

One good place to locate an impedance discontinuity is at a phase of 90° or 270°. In the voltage equation, Equation 3.1, the left cosine equals zero, forcing the right cosine to be zero also. Hence, the phase shift is zero and the voltage equation drops out. The current equation, Equation 3.2, becomes a linear equation because both sin's will be equal to 1 or -1. Only a voltage shift occurs, not a phase shift. The voltage-current equations simplify to:

$$\frac{V_a}{Z_a} = \frac{V_b}{Z_b}$$

By locating the discontinuity at a voltage zero, we have simplified the overall equations by one order. Unfortunately, at the other frequencies, where the voltage is not zero, the discontinuity will still introduce both a voltage and a phase shift.

Another good place to locate an impedance discontinuity is at a phase of 0° or 180°. In the current equation, Equation 3.2, the left sin will equal zero, forcing the right sin to be zero also. Hence, the current equation drops out. The voltage equation, Equation 3.1, simplifies to equating the voltage on the left and right. In other words locating a discontinuity at a current zero has no effect on the waveforms. The other frequencies still experience both a voltage and phase shift.

3.5.1 Two Frequency Tuning Example Using Zeroes

Let me describe a slightly more complicated example using discontinuities located at zeroes to simplify the problem. For this example I will convert two frequencies of a square wave into two frequencies of a linear ramp.

If you remember Fourier series decomposition, a square wave is the sum of odd harmonics with amplitudes inversely related to frequency, while a linear ramp is the sum of odd harmonics with amplitudes inversely related to the square of frequency and every other harmonic is 180° out of phase. Here are the decompositions. For simplicity, I will focus on just the first two frequencies.

$$\text{Square Wave} = 1\text{V}\sin(2\pi 1\text{GHz t}) + \frac{1\text{V}}{3}\sin(2\pi 3\text{GHz t}) + \frac{1\text{V}}{5}\sin(2\pi 5\text{GHz t}) + \ldots$$

$$\text{Linear Ramp} = 1\text{V}\sin(2\pi 1\text{GHz t}) - \frac{1\text{V}}{9}\sin(2\pi 3\text{GHz t}) + \frac{1\text{V}}{25}\sin(2\pi 5\text{GHz t}) - \ldots$$

In a single line we need to resonate a 1 GHz sinusoid with an output voltage of, say, 1V. In the same line we need to resonate a 3 GHz sinusoid with an output voltage of 1/9V. In order to produce a ramp as the output, the two harmonics must also be 180° out of phase. The square wave input, chosen because it is easy to produce and drive, requires a 1:1/3 relationship between the voltage amplitudes of the 2 frequencies, 1GHz:3GHz.

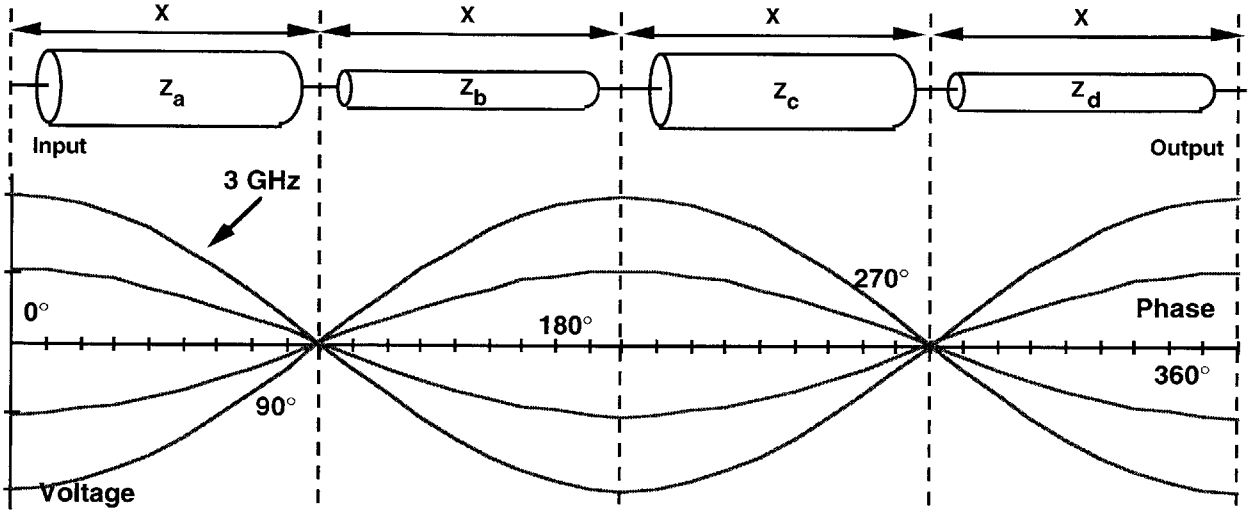

Figure 3.5. Discontinuities Relative to Third Harmonic

Realizing that discontinuities at zeroes do not affect phase, we can base the total line length and location of discontinuities on the third harmonic. As shown in Figure 3.5, we have chosen the line to resonate 2π of the third harmonic. The discontinuities are located at the zeroes: 90°, 180° and 270°. The discontinuity at 180° leaves V_{3b} equal to V_{3c}. V_{3b} refers to the voltage amplitude of the 3GHz waveform in the section of the line labeled b. However, the discontinuities at 90° and 270° introduce voltage shifts.

$$\text{discontinuity at } 90^\circ: \quad \frac{V_{3a}}{Z_a} = \frac{V_{3b}}{Z_b}$$

$$\text{discontinuity at } 180^\circ: \quad V_{3b} = V_{3c}$$

$$\text{discontinuity at } 270^\circ: \quad \frac{V_{3c}}{Z_c} = \frac{V_{3d}}{Z_d}$$

Based on the location of the discontinuities and line length, we can consider the structure of the first harmonic. If the 3GHz signal reaches a phase of 360° by the end of the line, the 1GHz signal will reach only 120°. The first harmonic will need to travel π over the length of the line, which requires a total phase shift of 60°, 180°–120°. As in Figure 3.6, this can distributed as two 30° shifts at the first and last

discontinuity. Since the center crossing will be at 90° the center discontinuity will not create a phase shift.

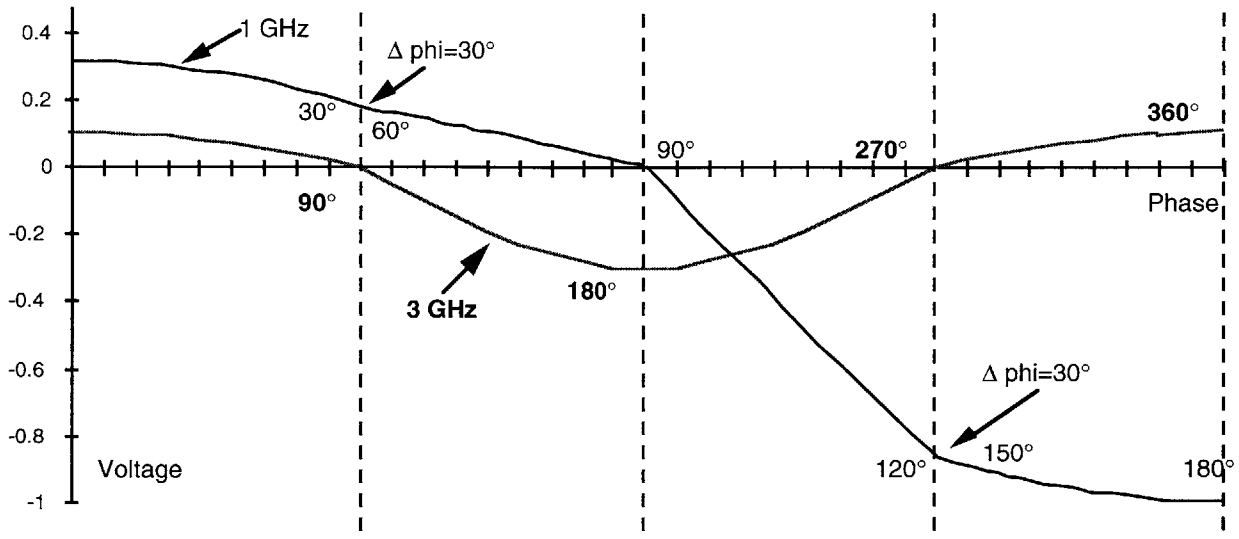

Figure 3.6. Desired Waveforms of Two Frequency Example

There are three sets of equations for the first harmonic, one for each discontinuity. The amplitude of the voltage amplitude of the 1GHz waveform for each section of the line appears below.

$$\text{discontinuity at } 90°: \; V_{1a}\cos\left(\frac{\pi}{6}\right) = V_{1b}\cos\left(\frac{\pi}{3}\right) \quad \text{or} \quad \sqrt{3}\,V_{1a} = V_{1b}$$

$$\text{discontinuity at } 90°: \; \frac{V_{1a}}{Z_a}\sin\left(\frac{\pi}{6}\right) = \frac{V_{1b}}{Z_b}\sin\left(\frac{\pi}{3}\right) \quad \text{or} \quad \frac{V_{1a}}{Z_a} = \sqrt{3}\,\frac{V_{1b}}{Z_b}$$

The second discontinuity produces just a voltage shift:

$$\text{discontinuity at } 180°: \; \frac{V_{1b}}{Z_{1b}} = \frac{V_{1c}}{Z_{1c}}$$

The third discontinuity also has an equation for voltage and current:

$$\text{discontinuity at } 270°: \; V_{1c}\cos\left(\frac{2\pi}{3}\right) = V_{1d}\cos\left(\frac{5\pi}{6}\right) \quad \text{or} \quad V_{1c} = \sqrt{3}\,V_{1d}$$

$$\text{discontinuity at } 270°: \; \frac{V_{1c}}{Z_c}\sin\left(\frac{2\pi}{3}\right) = \frac{V_{1d}}{Z_d}\sin\left(\frac{5\pi}{6}\right) \quad \text{or} \quad \sqrt{3}\,\frac{V_{1c}}{Z_c} = \frac{V_{1d}}{Z_d}$$

Together the 3 linear equations of the 3rd harmonic and the 5 linear equations of the 1st harmonic can be solved to quantify our internal waveforms and

impedance values. The result will be a line that resonates a square wave at the input of the line and a linear ramp at the output. Table 3.1 shows the voltages and impedances that solve the equations above. Note that the output was fully specified and the input voltage ratio was specified.

	Section A	Section B	Section C	Section D
Voltage of 1st	1/3 V	1/sqrt(3) V	sqrt(3) V	**1 V**
Voltage of 3rd	1/9 V	1/3 V	1/3 V	**1/9 V**
Impedance	5/3 Ω	5 Ω	15 Ω	**5 Ω**

Table 3.1 Voltages and Impedances of Internal Sections

3.6 Linearization

Each variation introduces a pair of non-linear equations involving sin and cos terms for each frequency of interest. Even locating discontinuities at zeroes only reduces the number of equations by one order. As the number of frequencies to be tuned scales the previous solution technique suffers.

One method to simplify the problem involves applying conditions that linearize the phase shift part of the problem. This process begins by solving for the phase and voltage shift across a discontinuity from Equation 3.1 and Equation 3.2:

$$\Delta\phi = \tan^{-1}\left[\sin\theta\cos\theta\frac{Z_b - Z_a}{Z_b\sin^2\theta + Z_a\cos^2\theta}\right]$$

$$\frac{V_b}{V_a} = \sqrt{\cos^2\theta + \left(\frac{Z_b}{Z_a}\right)^2\sin^2\theta}$$

When the $Z_b >> Z_a$ and $\theta \approx \pi/2$ or $\approx 3\pi/2$, the sin terms dominate and the relationships simplify to:

$$\Delta\phi = \frac{\pi}{2} - \theta \quad \text{and} \quad \Delta\phi = \frac{3\pi}{2} - \theta$$

$$\frac{V_b}{V_a} = \frac{Z_b}{Z_a}\sin\theta$$

Figure 3.7 plots the phase shift relationship for an impedance variation with a ratio of 50. The phase shift becomes highly linear in the specified region. Namely, the waveform shifts from its initial phase to $\pi/2$ or $3\pi/2$. Initial phases that are around 0 and π, introduce highly non-linear shifts. Figure 3.9 plots the ratio of the voltage shift to the current phase and the impedance change.

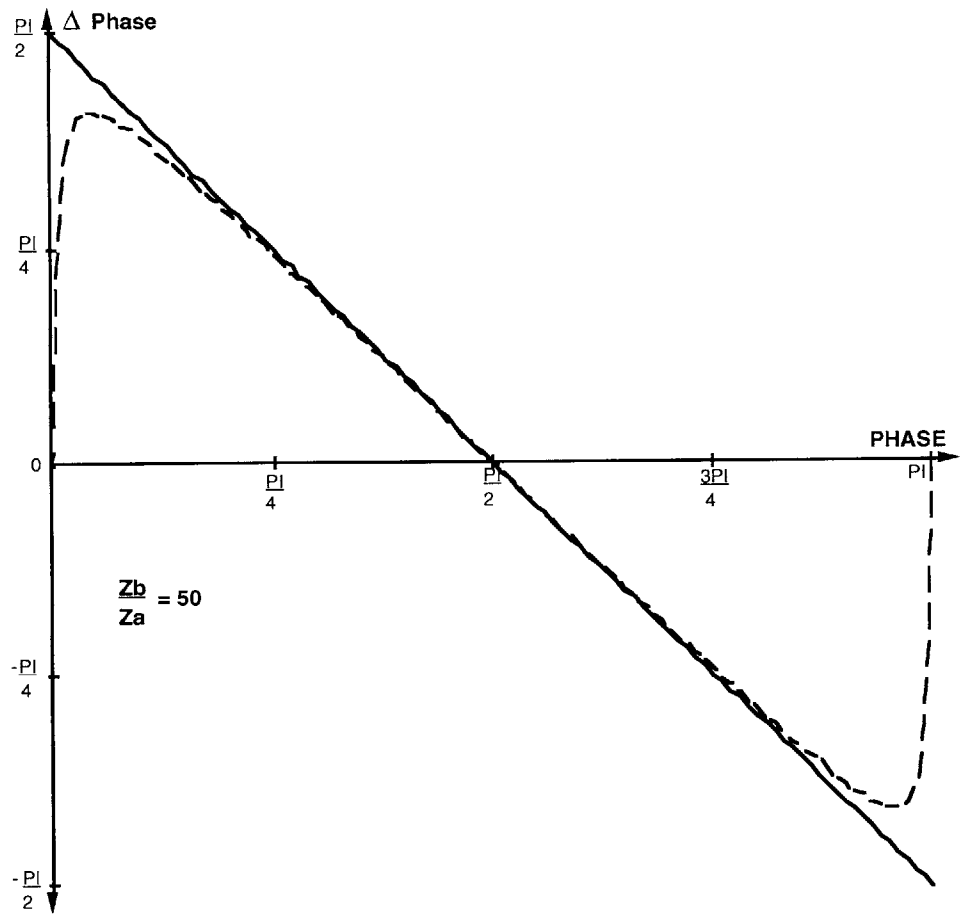

Figure 3.7. Phase Shift as a Function of Phase for Large Impedance Increase

When the $Z_a >> Z_b$ and $\theta \approx 0$ or $\approx \pi$, the cos terms dominate and the relationships simplify to:

$$\Delta\phi = -\theta \quad \text{or} \quad \Delta\phi = \pi - \theta$$

$$\frac{V_b}{V_a} = \cos\theta$$

Figure 3.8 shows the phase shift relationship for variations where the impedance decreases by a factor of 50. Namely, the phase shift becomes highly linear in the specified region in which the waveform shifts from its initial phase to 0 or π. Initial phases that are around $\pi/2$ and $3\pi/2$, introduce highly non-linear shifts. Figure 3.9 plots the ratio of the voltage shift to the current phase and the impedance change.

Because the voltage and phase shift relationships simplify for large impedance discontinuities, tuning a line can involve alternating high and low impedances. As long as each waveform has an initial phase in the linear region, the tuning equations remain simple.

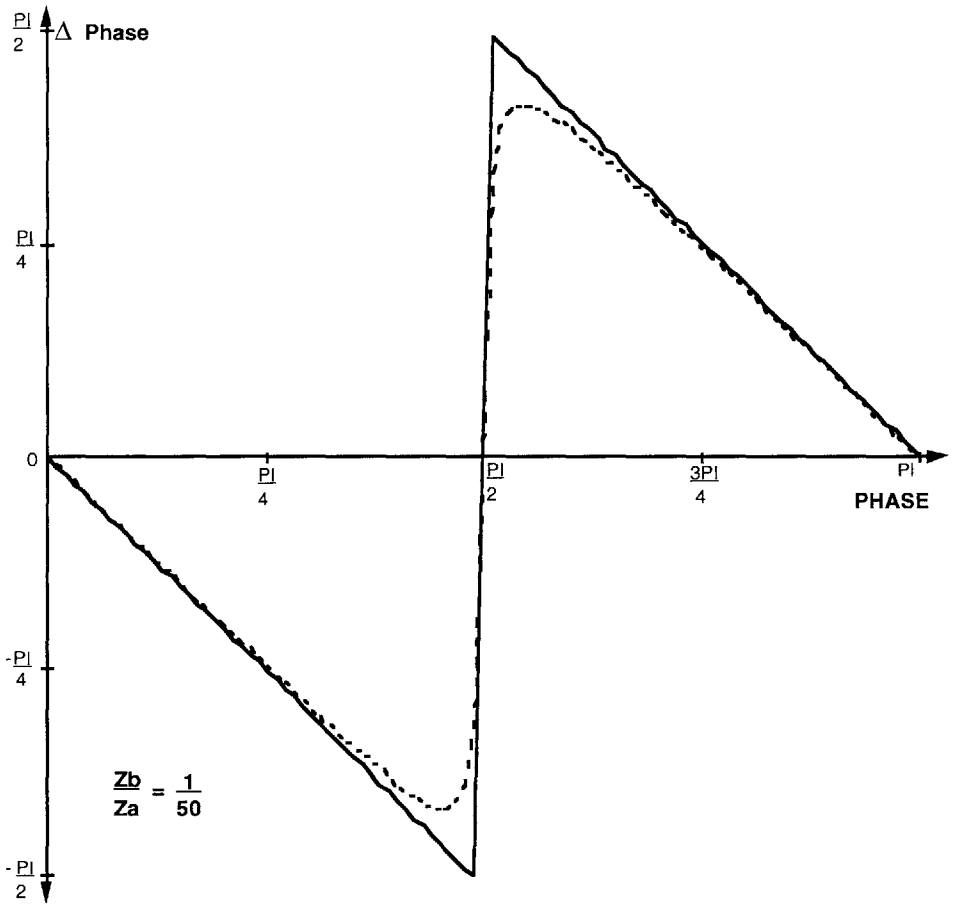

Figure 3.8. Phase Shift as a Function of Phase for Large Impedance Decrease

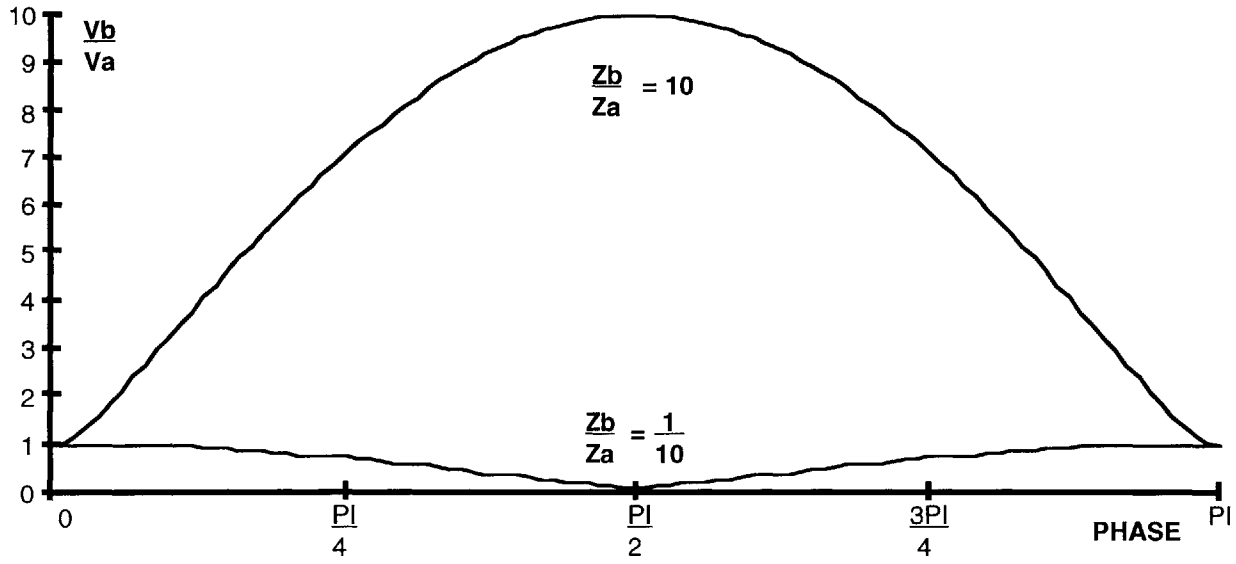

Figure 3.9. Voltage Change as a Function of Initial Phase

3.7 Lumped Elements

Lumped elements, like capacitors and inductors, must be included in this theoretical framework for three reasons. First, they affect the resonance of a transmission line. Second, the clock loads we wish to drive and sometimes unavoidable parasitics may be represented as lumped elements. Third, the use of varactors or variable capacitors along the line could be used to tune or fine tune the line.

Similar to an impedance variation, an element introduces phase and voltage shifts. The element acts as a frequency dependent impedance. The elements can be wired in parallel or in series. A parallel connection leaves the voltage continuous, but introduces a current step based on the voltage. A series connection leaves current continuous, but introduces a voltage step based on the current.

This leads to the following equation for voltage:

$$V_a \cos\left(\frac{2\pi f}{v}x\right) = V_b \cos\left(\frac{2\pi f}{v}x + \Delta\Phi\right) + \frac{V_a}{Z}\sin\left(\frac{2\pi f}{v}x\right)\left[L\omega - \frac{1}{C\omega}\right]_{Series}$$

Equation 3.3

and current:

$$\frac{V_a}{Z}\sin\left(\frac{2\pi f}{v}x\right) = \frac{V_b}{Z}\sin\left(\frac{2\pi f}{v}x + \Delta\Phi\right) + V_a \cos\left(\frac{2\pi f}{v}x\right)\left[\frac{1}{L\omega} - C\omega\right]_{Parallel}$$

Equation 3.4

As before V_a and V_b represent the voltage amplitude on each side of the element. The phase of the signal before the discontinuity appears inside the left cos and sin terms. Just as with impedance discontinuities, the phase after the element has been written in terms of the old phase shifted by some $\Delta\phi$. A new set of terms related to the lumped elements appears on the far right. In the voltage equation it multiplies the current before the element by the impedance to introduce a voltage step. In the current equation the term divides the voltage before the element by the impedance to introduce a current step.

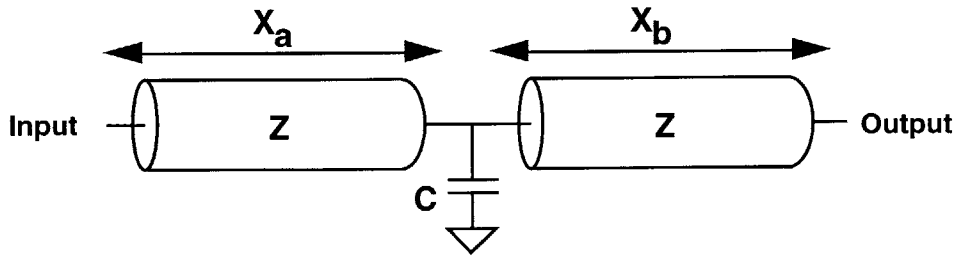

Figure 3.10. Transmission Line with a Lumped Capacitive Load

Figure 3.10 shows one of the four possible configurations, a capacitor wired in parallel with a uniform transmission line. The capacitor has an impedance of

$1/2\pi fC$. As expected, any phase and voltage shift depends on the current phase and voltage and by extension the frequency of the waveform.

The following equations describe the voltage and current across the element shown in Figure 3.10. Note the parallel connection introduces a current step.

$$V_a \cos\left(\frac{2\pi f}{v} X_a\right) = V_b \cos\left(\pi - \frac{2\pi f}{v} X_b\right)$$

$$\frac{V_a}{Z} \sin\left(\frac{2\pi f}{v} X_a\right) = \frac{V_b}{Z} \sin\left(\pi - \frac{2\pi f}{v} X_b\right) - \frac{V_a}{(1/2\pi f C)} \cos\left(\frac{2\pi f}{v} X_a\right)$$

3.7.1 Simple Example of Tuning with a Capacitor

This section revisits the first tuning example presented on tuning. However, this time instead of an impedance step at 2 cm we shall use a lumped capacitor at 2 cm. Figure 3.10 shows the setup involved.

As a reminder, the previous problem was to resonate a 1V, 475 MHz waveform in an 8 cm line that would normally resonate at 625 Mhz waveform. The velocity of the line is $1x10^8$ m/s and the impedance is 5Ω. So, let's plug in these numbers into Equation 3.3 and Equation 3.4:

$$1V \cos\left(\frac{2\pi \times 475MHz}{1\times 10^8 m/s} 2cm\right) = V_b \cos\left(\pi - \frac{2\pi \times 475MHz}{1\times 10^8 m/s} 6cm\right)$$

$$\frac{1V}{5\Omega} \sin\left(\frac{2\pi \times 475MHz}{1\times 10^8 m/s} 2cm\right) = \frac{V_b}{5\Omega} \sin\left(\pi - \frac{2\pi \times 475MHz}{1\times 10^8 m/s} 6cm\right) - \frac{1V}{(1/C2\pi \times 475MHz)} \cos\left(\frac{2\pi \times 475MHz}{1\times 10^8 m/s} 2cm\right)$$

Solving the voltage equation again yields a value of 3.791 V for V_b. Plugging this into the current equation produces 254.2pF as the capacitance. This tells us that a line composed of a 2 cm section of 5 Ω, a 254.2pF capacitor and then 6 cm of 5 Ω will resonate a 475 Mhz waveform.

As shown in Figure 3.11, the voltage waveform, though continuous, changes slope at the capacitor. The waveform exactly matches the waveform of Figure 3.2 in the previous example.

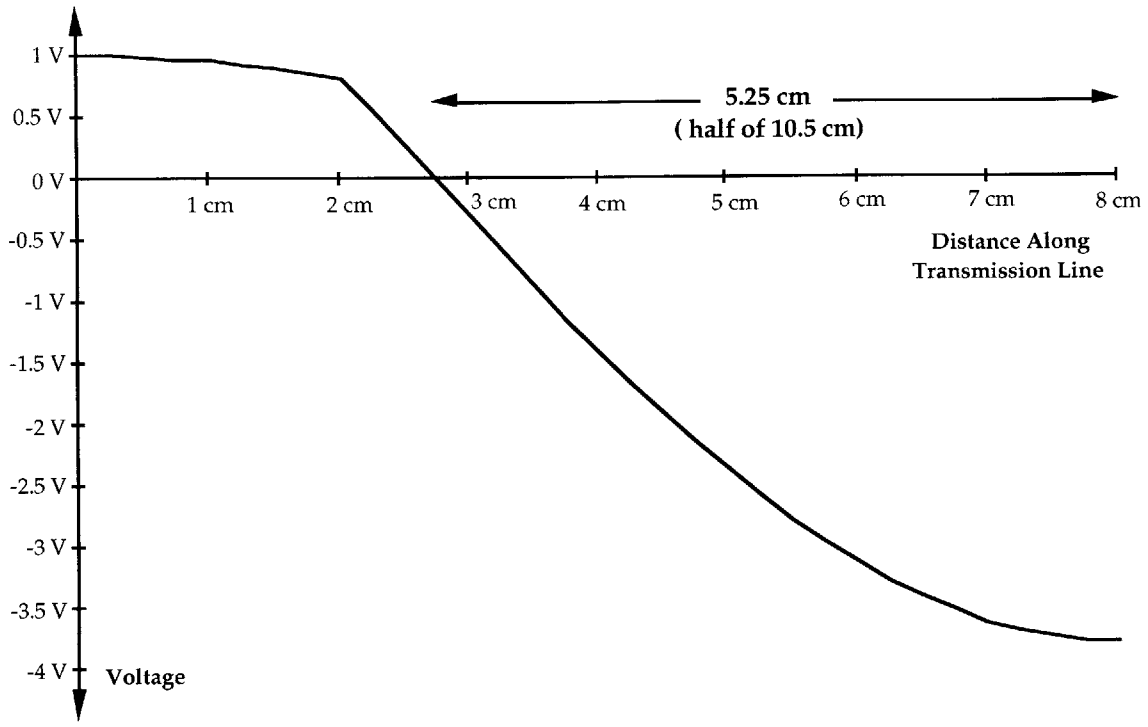

Figure 3.11. Voltage Along Transmission Line for Capacitor Tuning Example

However unlike the previous example the current waveform in Figure 3.12 is not continuous at the location of the capacitor. It experiences a step equivalent to the current drawn by the capacitor.

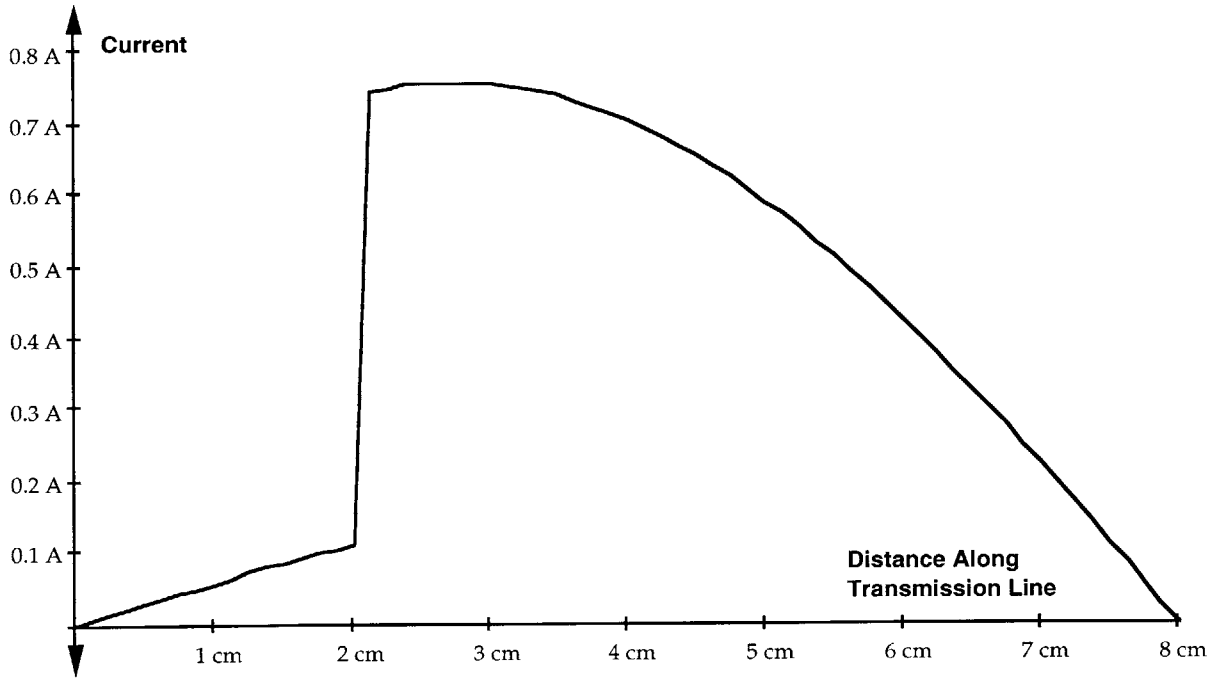

Figure 3.12. Current Along Transmission Line for Capacitor Tuning Example

3.7.2 Phase Boundaries and Zeroes

With the introduction of lumped elements into the theoretical model, phase boundaries take on a new characteristic. Because an element introduces a step in voltage or current, the waveform can step from positive to negative or vice versa. So for a series element which introduces a voltage step, the voltage phase boundary can be crossed. However, a current phase boundary will still exist. For an element connected in parallel, where a current step is introduced, the current phase boundary disappears. The voltage phase boundary still can not be crossed.

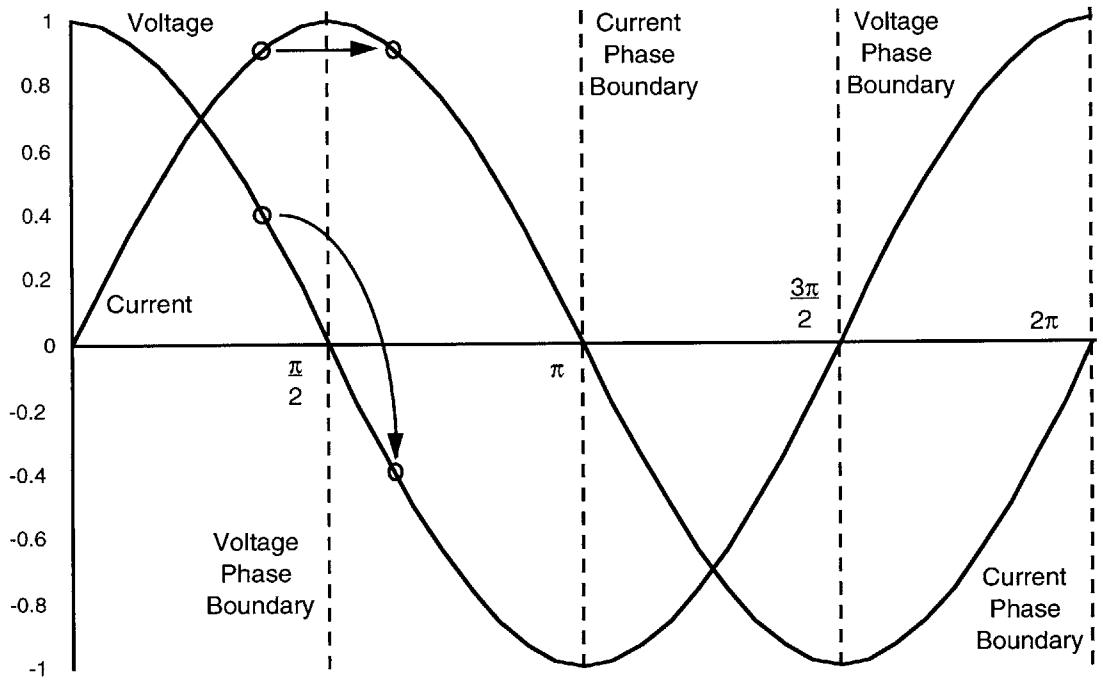

Figure 3.13. Crossing a Voltage Phase Boundary with a Series Element

Figure 3.13 shows an attempt to move across the voltage phase boundary at $\pi/2$ in which voltage changes from positive to negative. The current is positive on both sides of the element. In order to equalize the voltage on both sides of Equation 3.3, a series inductor can provide a positive voltage step: (+) = (-) + (+)(+).

$$V_a \cos\left(\frac{2\pi f}{vel}x\right) = V_b \cos\left(\frac{2\pi f}{vel}x + \Delta\Phi\right) + \frac{V_a}{Z}\sin\left(\frac{2\pi f}{vel}x\right)[L\omega]_{Series}$$

The other voltage phase boundary at 2π, in which current goes from negative to positive, can also be crossed with a series inductor. This results from the current being negative, making the inductor term negative: (-) = (+) + (-)(+)

Both the current boundaries can be crossed with a parallel capacitor. At π this results from the voltage being negative while the current is changing from positive to negative: (+) = (-) + (-)(-). At 2π, the voltage is positive while the current changes from negative to positive: (-) = (+) + (+)(-).

$$\frac{V_a}{Z}\sin\left(\frac{2\pi f}{vel}x\right)=\frac{V_b}{Z}\sin\left(\frac{2\pi f}{vel}x+\Delta\Phi\right)+V_a\cos\left(\frac{2\pi f}{vel}x\right)[-C\omega]_{Parallel}$$

Finally, just as impedance discontinuities can be placed at voltage or current zeroes, so can lumped elements. By matching the type of connection, series or parallel, with the type of zero, voltage or current, the same non-effect on phase can be achieved. This means that tuning for multiple frequencies can be simpler through decoupling.

3.8 Conclusions for Theory Chapter

This chapter explored two basic methods of tuning a transmission line for resonating a desired waveform. The first involves placing impedance discontinuities and sizing them to alter the phase of each frequency along the line. The basic equations we have learned are voltage in Equation 3.1 and current in Equation 3.2.

$$V_a\cos\left(\frac{2\pi f}{vel}x\right)=V_b\cos\left(\frac{2\pi f}{vel}x+\Delta\Phi\right)$$

$$\frac{V_a}{Z_a}\sin\left(\frac{2\pi f}{vel}x\right)=\frac{V_b}{Z_b}\sin\left(\frac{2\pi f}{vel}x+\Delta\Phi\right)$$

Two important realizations can make the tuning problem much simpler. First, large discontinuities cause a linear amount of phase shift based on the current phase. The second realization that properly locating a discontinuity decouples the problem of tuning multiple frequencies. A discontinuity located at a voltage zero introduces no phase shift and no voltage shift. And a discontinuity at a current zero, there is no phase shift, but the voltage shift is related to the ratio of the impedances.

The final set of equations explains how to tune using lumped elements that introduce steps into the voltage and phase. The equation for voltage and current must be modified to Equation 3.3 and Equation 3.4.

$$V_a\cos\left(\frac{2\pi f}{vel}x\right)=V_b\cos\left(\frac{2\pi f}{vel}x+\Delta\Phi\right)+\frac{V_a}{Z}\sin\left(\frac{2\pi f}{vel}x\right)\left[L\omega-\frac{1}{C\omega}\right]_{Series}$$

$$\frac{V_a}{Z}\sin\left(\frac{2\pi f}{vel}x\right)=\frac{V_b}{Z}\sin\left(\frac{2\pi f}{vel}x+\Delta\Phi\right)+V_a\cos\left(\frac{2\pi f}{vel}x\right)\left[\frac{1}{L\omega}-C\omega\right]_{Parallel}$$

4. Application for Microprocessor Clock Driver

This chapter describes one of the most obvious applications of the transmission line technique, using the technique to drive microprocessor-like loads. The technique reduces power consumption by at least a factor of four and leads to zero skew in the traditional sense. However, this technique does not eliminate second-order skew effects such as rise time differences across the chip.

The chapter is broken into three basic sections. The first describes traditional clock drivers and how the transmission line technique can be applied to them. The second section describes a low frequency mockup which tested the technique at 20 MHz and realized a factor of 10 improvement in power. The third section describes the Spice simulations of the technique at 1GHz, which led to power savings of a factor of 4.

4.1 Overview of Driver Application

4.1.1 Standard Clock Driver

A standard clock distribution structure appears in Figure 4.1. It includes a clock generator, a buffer and a distribution network. The clock lines are drawn as transmission lines to emphasize that they introduce delay. However, since the series resistance dominates over the inductance, it is more appropriate to model the clock lines as distributed RC lines.

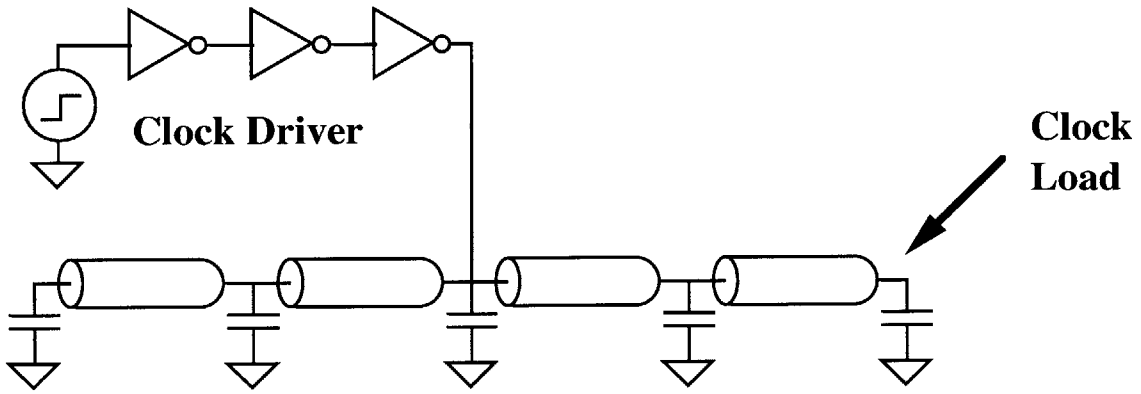

Figure 4.1 Standard Clock System for Large Chips

Figure 4.2 shows the crux of the problem with using the standard driver. Current to charge the clock capacitance passes from the power supply through the pmos device with its associated resistance. This energy is dumped into the ground supply when discharging the capacitance. Since the clock drives such a large fraction of the chip's transistors every cycle, the clock power represents 40% of the total power.

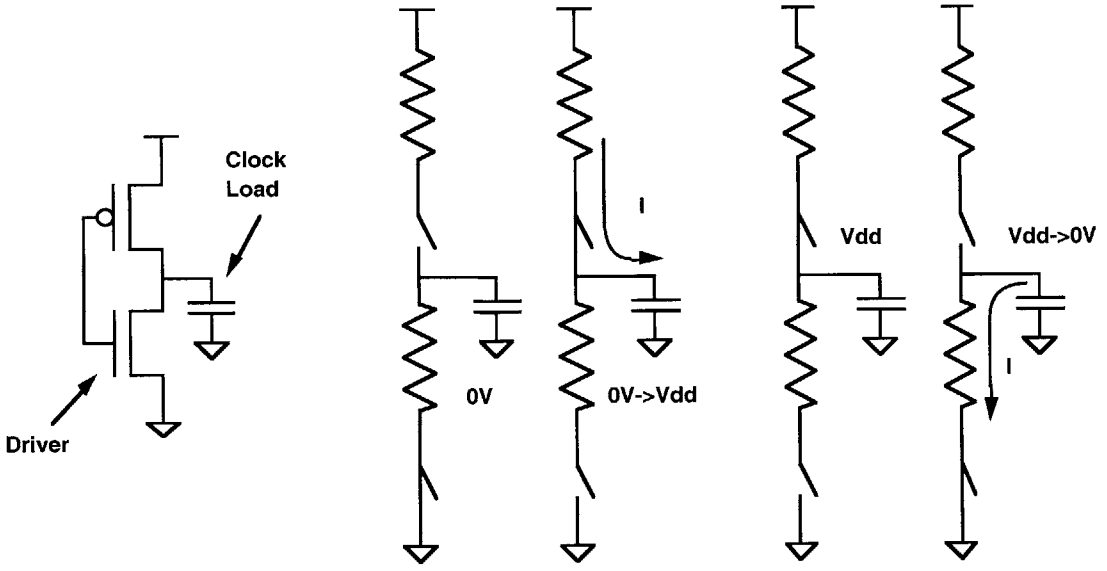

Figure 4.2 Power Consumption in Standard Clock System

4.1.2 Benchmark Clock Driver - Alpha 21164

The Alpha 21164 microprocessor represents a good benchmark of advanced micro-processors. First, the Alpha is at the forefront of design work with high clock rates and prolific use of the clock to improve bandwidth. Second, its clock structure consists of a fused clock plane that achieves reasonably low skew at the operating frequency.

Basic Reference Data	Clock Load	3.7 nF
	Die size	1.6 cm x 1.8 cm
	Vdd	3.3V
	Drive Transistor Size	58 cm x 0.5 um
	Frequency	300 MHz
Performance Parameters	Rise time	500 ps
	Clock Power	40% of 50 W
	Skew time	30-90 ps

Table 4.1 Alpha 21164 Benchmark Data

Table 4.1 lists the relevant published data for the Alpha 21164. [Bowhill] These basic system level characteristics have been adapted for the mockup (Section 4.2) and simulations (Section 4.3). The clock load, 3.75 nF, is comprised of 3 major elements: interconnect (1.95 nF), gate (1.2 nF) and driver self-loading (0.6 nF). Both the interconnect and self loading capacitances will not vary in a data dependent fashion. The large die size, 1.6 cm x 1.8 cm, causes a maximum skew time of 90 ps. The operating frequency is 300 MHz with transition times of 500 ps (15% of cycle time). A

pair of inverters with a combined width of 58 cm, drive the clock load at this transition rate. At 3.3V the clock consumes 20 W, which represents 40% of the total.

Within this framework, we seek to match the reference data and optimize for rise time, power and skew delay. The power consumption is a function of rise time based on the size of the driver. Namely, as the driver shrinks, it consumes less pre-driver power and self-loading power, but suffers from longer rise times. The mockup and simulations have been geared to match the rise time as a percentage of the clock period. Various skew reduction techniques are explored in the next chapter. Each section, mockup and simulation, describes its own version of the standard chip used to a make fair comparison.

4.1.3 Transmission Line Clock Driver

Our technique, shown in Figure 4.3, simply adds an external transmission line to the standard driver. Energy is recovered by charging and discharging the final clock load not through the clock driver, but through the transmission line as seen in Figure 4.4. This also means that the clock buffers can be smaller resulting in less pre-driver power.

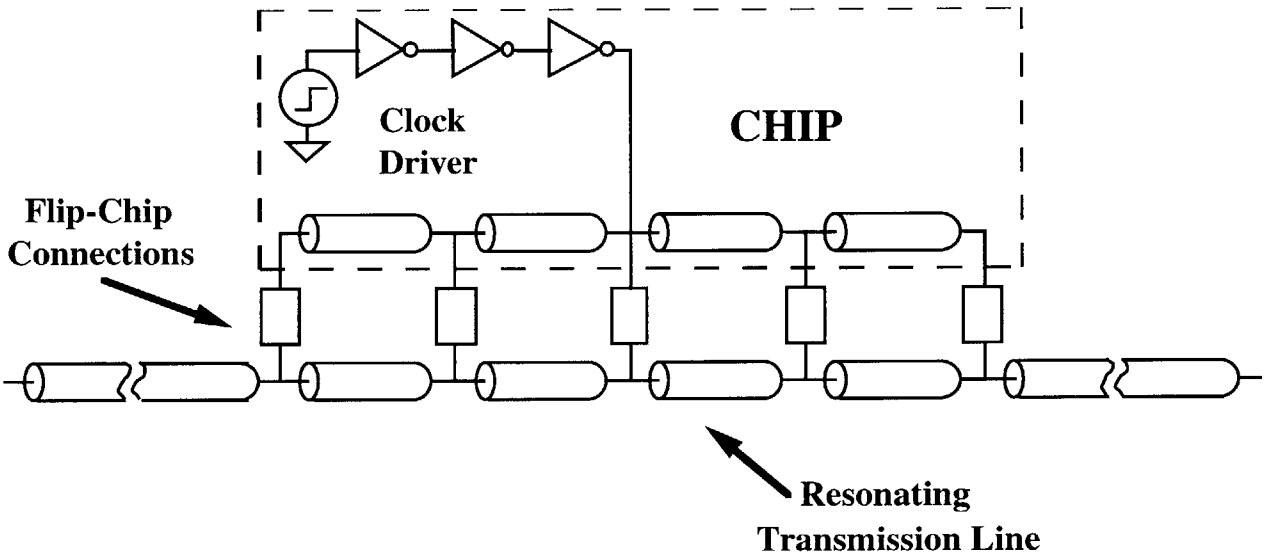

Figure 4.3 New Transmission Line Clock System

Let me walk through a simplified description of how the technique works. The central driver forces a square wave into the chip and the external transmission line. Because the driver is smaller, it cannot fully drive the system. However, a reduced height pulse flows down the length of the transmission line. The pulse travels to the open termination of the transmission line and reflects back towards the chip. The line length is such that the pulse in the transmission line will reach the driver exactly when it drives again. The result is an increase in the pulse height.

Eventually the transmission line will be resonating a full clock pulse at a given clock frequency. The transmission line frequency can be tuned by artificially loading or unloading the line or by using impedance discontinuities. Taps using

flip-chip technology strap the internal clock line to the external transmission line. A pin structure like flip-chip is useful because of its low inductance, short pin lengths and the even distribution of pins across the chip.

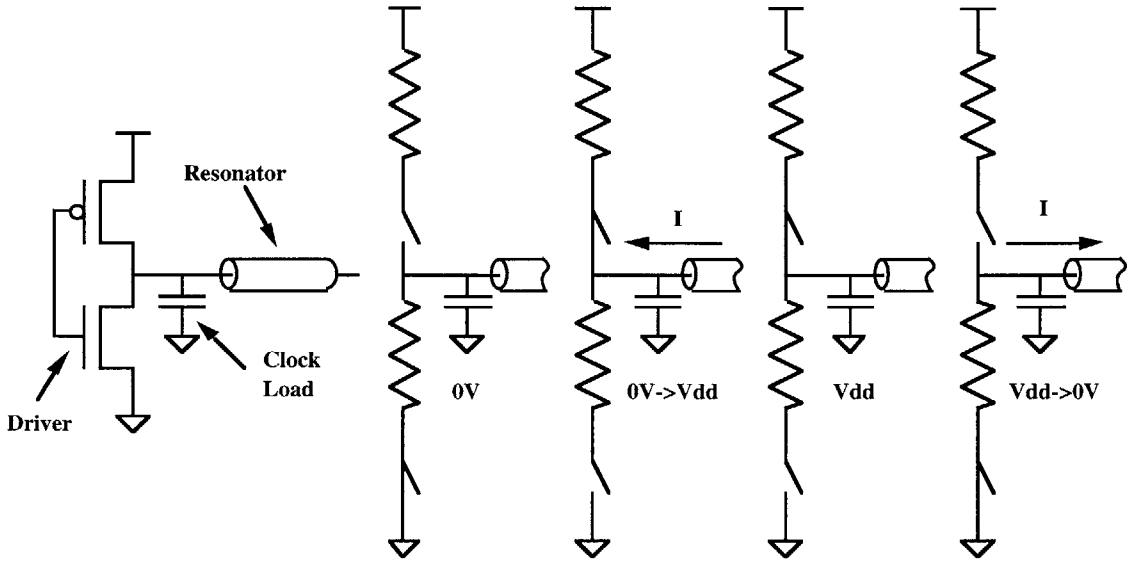

Figure 4.4 Power Consumption with Transmission Line Technique

Figure 4.5 shows a realistic implementation for the transmission line technique. The key features are the chip, connections and strip-line. In order to properly drive the large clock capacitance, the strip-line must have a low impedance. This will most likely require a stacked set of strip lines or a mesh as described in the next chapter.

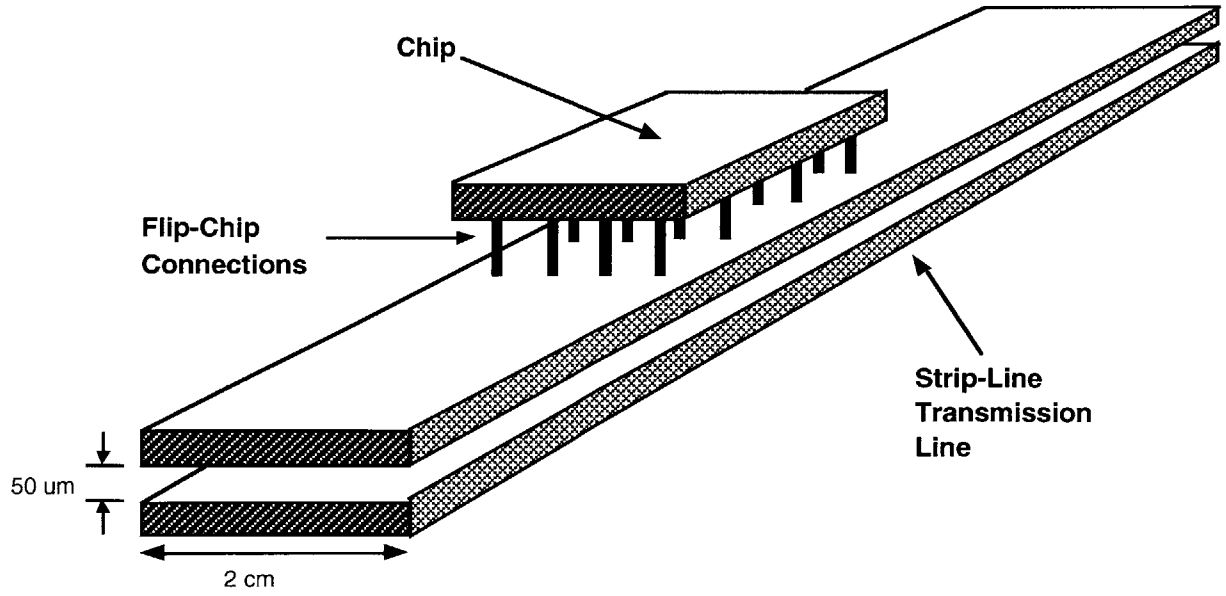

Figure 4.5 Possible Implementation of Transmission Line Technique

4.2 Large Scale Mockup

The large scale mockup provides experimental evidence that this technique is viable. It is a low frequency version of the 300 MHz clock driver described above. For the following experimental work, I have assumed a clock rate of 500 MHz which would be the next generation Alpha. At 20 MHz a transmission line clock driver with uniform impedance reduces power consumption by a factor of 5.8 relative to a standard clock driver. Using a tuned transmission line saves a factor of 9.5 over the standard driver. Further, the quality of waveforms is significantly better for the tuned version.

Section 4.2.1 lists many of the reasons for building the mockup. Section 4.2.2 describes the overall structure, scaling and comparison issues. In Section 4.2.3, I cover the testing method. Section 4.2.4 shows the results from the standard clock driver which provide a basis for comparison. The next section, 4.2.5, presents the results from the clock driver with a uniform transmission line. Finally, section 4.2.6 describes the success of the clock driver with a tuned transmission line.

4.2.1 Purpose

Why would anyone want to build a large scale version to test this clock driver technique? Even though the mockup runs at under 20 MHz with transmission line dimensions that span an entire room, the basic tenets remain the same. The power consumption is directly related to the total capacitance of the clock load, 2.2 nF. And the addition of a resonant structure significantly reduces power consumption.

There were three overwhelming reasons to build such a large, low frequency model:

- Fast construction time
- Ease of testing
- Fast redesign and alteration time

Building the system required just a few days instead of the months required to produce a Mosis chip and circuit board. This resulted from the use of standard components and lumped circuit elements that function reasonably well at 20 MHz, but not much above.

As for testing, a big win was the ability to tune the input frequency to match the transmission line instead of the other way around. This saved countless hours of needless work to find the system's "sweet" spot. A real system would need some type of variable capacitor to provide tuning to the desired frequency.

Because the system was easy to modify, results from one test could be used to quickly improve the design. For example the initial system, shown in Figure 4.6, simulated the on-chip clock wires with resistors, R_{LOAD}, instead of real 2 in. wires. In a compact amount of space the resistors were meant to provide the delay expected in traveling across a 24 inch chip. Unfortunately, the resistors shorted together separated points along the external transmission line. Because the voltage varied along the transmission line for a given moment in time, the resistors were causing excess power consumption. Once testing verified this, each resistor could be replaced with the more realistic structure, a 2 inch wire. The new configuration appears in

Figure 4.7. Determining the error and modifying the design required just a few days of work.

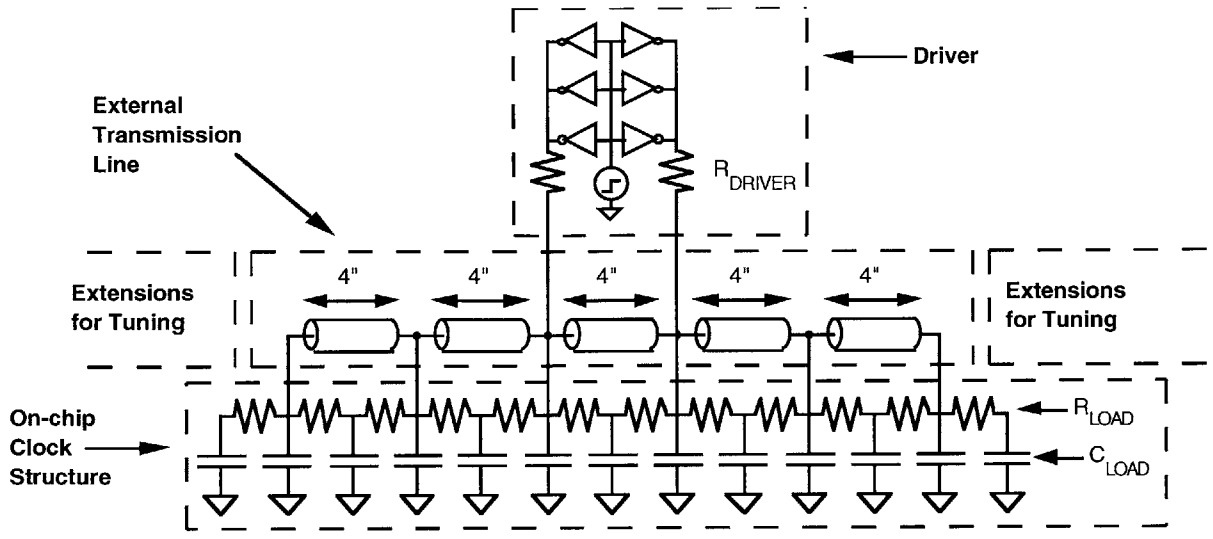

Figure 4.6 Original Structure of Standard Clock Driver

4.2.2 Overview

Figure 4.7, Figure 4.9 and Figure 4.11 show each configuration of the large scale mockup: a standard clock driver, a clock driver with a uniform transmission line and a clock driver with a tuned transmission line. All configurations can be broken into three distinct parts. From top to bottom there appears the driver, the external transmission line and finally the on-chip clock structure. The clock structure is shared between all the designs.

The **driver** is a pulse generator with variable frequency that drives a set of inverters with an output impedance of approximately 7Ω each. Further, the inverters drive the clock load in series with a pair of resistors. By altering the number of inverters wired through the resistor and the size of R_{DRIVER}, the driver can exhibit a higher output impedance without actually finding a new, smaller inverter part. In the normalizing equations this driver impedance is converted into an effective width, w. For the configurations with a transmission line, the basic length of the line is chosen to get approximately 20MHz. Then the exact frequency is changed to match the true resonant frequency of that particular line.

The central section of the **external transmission line** is shared between all the configurations. This includes the five 4 in segments that match the length of the entire chip, 20 in. This length is derived from the frequency scale up factor of 500 MHz : 20 MHz, and the width of a standard chip, 2 cm.

$$L_{CHIP}(20\,\text{MHz}) = L_{CHIP}(500\,\text{MHz})\left(\frac{500\,\text{MHz}}{20\,\text{MHz}}\right) = 0.787\,\text{in.}\left(\frac{500\,\text{MHz}}{20\,\text{MHz}}\right)$$

$$L_{CHIP}(20\,\text{MHz}) = 19.7\,\text{in.}$$

The extensions of the **external transmission line** changes extensively between configurations. As seen in Figure 4.7, the standard driver has no extensions at all. The next configuration in Figure 4.9 uses a uniform transmission line that is 15 ft. long. Figure 4.11 shows the tuned line.

In order to reduce the line impedance to 10Ω, 11 twisted pairs were ganged together. This is the impedance for most of the external transmission lines: the five central sections, the 15 ft. sections of the uniform line, the 8 in. section of the complex line and the 4ft. 8in. section of the complex line. For the 15 in. high impedance section of the complex transmission line, I use only 3 twisted pairs ganged together to produce an impedance of roughly 35Ω.

Lumped elements, C_{LOAD}, model the **on-chip clock** capacitance. The total load is 2.2 nF. The small, 2 in. wires represent the on-chip clock wires and connect the loads.

4.2.3 Testing Method

This section contains a list of the steps involved in testing and evaluating each transmission line driver. I then describe how to normalize power relative to frequency, the self-loading power and the pre-driver power. The last two components are dependent on the inverter width and frequency. As mentioned earlier, the inverter width, w, is varied by introducing a resistor to simulate a smaller driver.

The first three steps are performed on the standard driver:

1) Measure the rise time, T_{STD}, for a given inverter width, w_{STD}
2) Measure the power, P_{STD}, at w_{STD}
3) Normalize P_{STD}

Then the following steps are performed on each transmission line driver:

4) Measure the rise time, T, for a given inverter width, w
5) Change w until $T = T_{STD}$
6) Measure the power, P, at w
7) Normalize P
8) Compare the normalized powers

The first three steps involving the standard clock driver, provide a base line against which to compare the transmission line drivers. As one can see in the final 5 steps, the driver width acts as the independent variable. As the width increases the signal rise times improve, but the power increases. In step 5 I choose the driver width such that the transmissions line driver provides the same quality of signal, based on rise time, as the standard driver. At this size I can compare the normalized powers.

I calculate the power, P and P_{STD}, by measuring the current drawn from the power supply and multiplying it by the applied voltage, 5V. Then I normalize the power for three different effects as seen in Equation 4.1. First, in order to compare powers obtained at different frequencies, I normalize the power relative to a

frequency of 20 Mhz with the three frequency terms, (20 MHz/F), (20 MHz/F_{SELF}) and (20 MHz/F_{STD}). F, F_{SELF} and F_{STD} represents the frequency for the current configuration, for the self-loading test case and for the standard driver, respectively.

Second, in order to compare configurations fairly, I need to include the self-loading power. Self-loading power is the power required to fill the source and drain capacitance of the driver. Because all the designs used the same inverter part, they all have the same self-loading capacitance and all consume the same amount of self-loading power, even in the cases with a smaller, simulated inverter width, w. Therefore, I normalize the measured power to correct for the reduced self-loading capacitance when I simulate a smaller inverter. This correction appears in the second term of Equation 4.1. (1-w/w_{STD}) represents the fraction of the extra width to the total width. By multiplying this by the total self-loading power, I calculate the self-loading power related to the unused width. This can then be subtracted from the total power, leaving a normalized power which accounts for the reduced self-loading of a smaller, simulated inverter.

Finally, in order to compare configurations fairly, I need to include the pre-driver power. Pre-driver power represents the amount of power consumed in driving the input to the final inverter stage. Please note that in all of the configurations, this power comes from the pulse generator, not the power supply. Therefore, I estimate the pre-driver power by dividing the measured power in the standard case by an inverter scale up factor of 4. This correction is added to the total power by the third term of Equation 4.1. Further, in order to compare pre-driver powers with different inverter widths, the pre-driver power has to be normalized relative to the inverter width. Therefore, I multiply the standard pre-driver power by the by the new width, w/w_{STD}.

$$P_{NORM} = P_{TEST}\left(\frac{20\,MHz}{F_{TEST}}\right) - P_{SELF}\left(1-\frac{w}{w_{STD}}\right)\left(\frac{20\,MHz}{F_{SELF}}\right) + \frac{1}{4}P_{STD}\left(\frac{w}{w_{STD}}\right)\left(\frac{20\,MHz}{F_{STD}}\right)$$

Equation 4.1

4.2.4 Standard Clock Driver

This section will describe two important test cases that establish some metrics for evaluating later designs. The first is the self-loading case and the second is the standard driver. I begin with a schematic of the test structure. Then I show the measured results and plug them into our normalizing equation for both this case and for later cases. At the end of the section, I have included a printout of the waveforms produced by the standard driver.

Figure 4.7 shows the schematic for the standard clock driver. For all the test cases C_{LOAD} is fixed at 2.2 nF. However, the frequency and R_{DRIVER} vary quite extensively from case to case. Please note that I did not remove the external transmission line from the standard driver, even though I could have. I did this for two reasons. First, the standard driver performs better with the external transmission line and so makes a harder standard to beat. Second, for a real chip the clock impedance would probably be lower than the 2 in. segments by themselves, but definitely not lower than the impedance with the external transmission lines.

In order to calculate the self-loading for the entire part, I simply disconnect the clock load and measure the current flowing through the power supply.

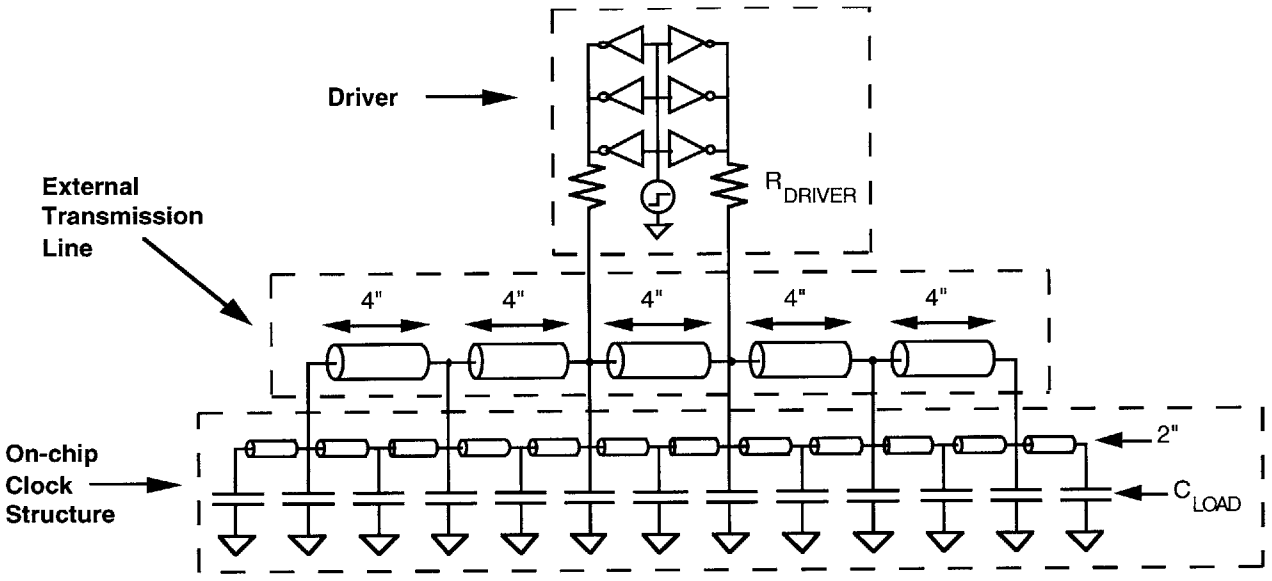

Figure 4.7 Standard Clock Driver

Table 4.2 shows the power consumption for a few important cases. The values fill in the variables of the normalization function, Equation 4.1. I have included the rise times at the edge and center of the chip.

	Center T	Edge T	P	w/w_{STD}	P_{NORM}
Self-Loading @ 16.4 MHz			0.12 W	1	
Standard @ 2 MHz	15.6 ns	11.6 ns	0.19 W	1	2.4 W
Standard @ 16.4 MHz	13.3 ns	10 ns	1.5 W	1	2.3 W
Standard @ 14 MHz	14.7 ns	11.4 ns	1.48 W	1	2.6 W

Table 4.2 Mock-up of Standard Clock Driver

Below, I have made the substitutions and simplified the previous relation down to Equation 4.2. First, I include the self-loading power and frequency: P_{SELF}=0.12 W and F_{SELF}=16.4 MHz. Next I substitute the pre-driver power and frequency: P_{SELF}=0.19 W and F_{SELF}=2 MHz. Finally, I use Equation 4.2 to calculate the normalized power for a few different frequencies close to my region of interest: 16.4 MHz and 14 MHz. These appear above in Table 4.2.

$$P_{NORM} = P_{TEST}\left(\frac{20\,MHz}{F_{TEST}}\right) - 0.12\,W\left(1-\frac{w}{w_{STD}}\right)\left(\frac{20\,MHz}{16.4\,MHz}\right) + \tfrac{1}{4}\,0.19\,W\left(\frac{w}{w_{STD}}\right)\left(\frac{20\,MHz}{2\,MHz}\right)$$

$$P_{NORM} = P_{TEST}\left(\frac{20\,MHz}{F_{TEST}}\right) - 0.15\,W + 0.62\,W\left(\frac{w}{w_{STD}}\right)$$

Equation 4.2

Below I have included a plot of the last test case of the standard driver. This was run at 14 MHz, a period of 71.5 ns. Channel 1, C1, corresponds to the center of the chip and Channel 2, C2, corresponds to the edge of the chip. Despite the seemingly reasonable rise times of the last row in Table 4.2 and shown on the right of Figure 4.8, note the poor quality of the waveform. Basically, the standard inverter part can't drive the given load because the high inductance at its pins. The next sections will describe how both transmission line drivers clean up the quality appreciably. The transmission lines do so by reducing the size of the current spike flowing through the inverter chip pins and the related voltage noise.

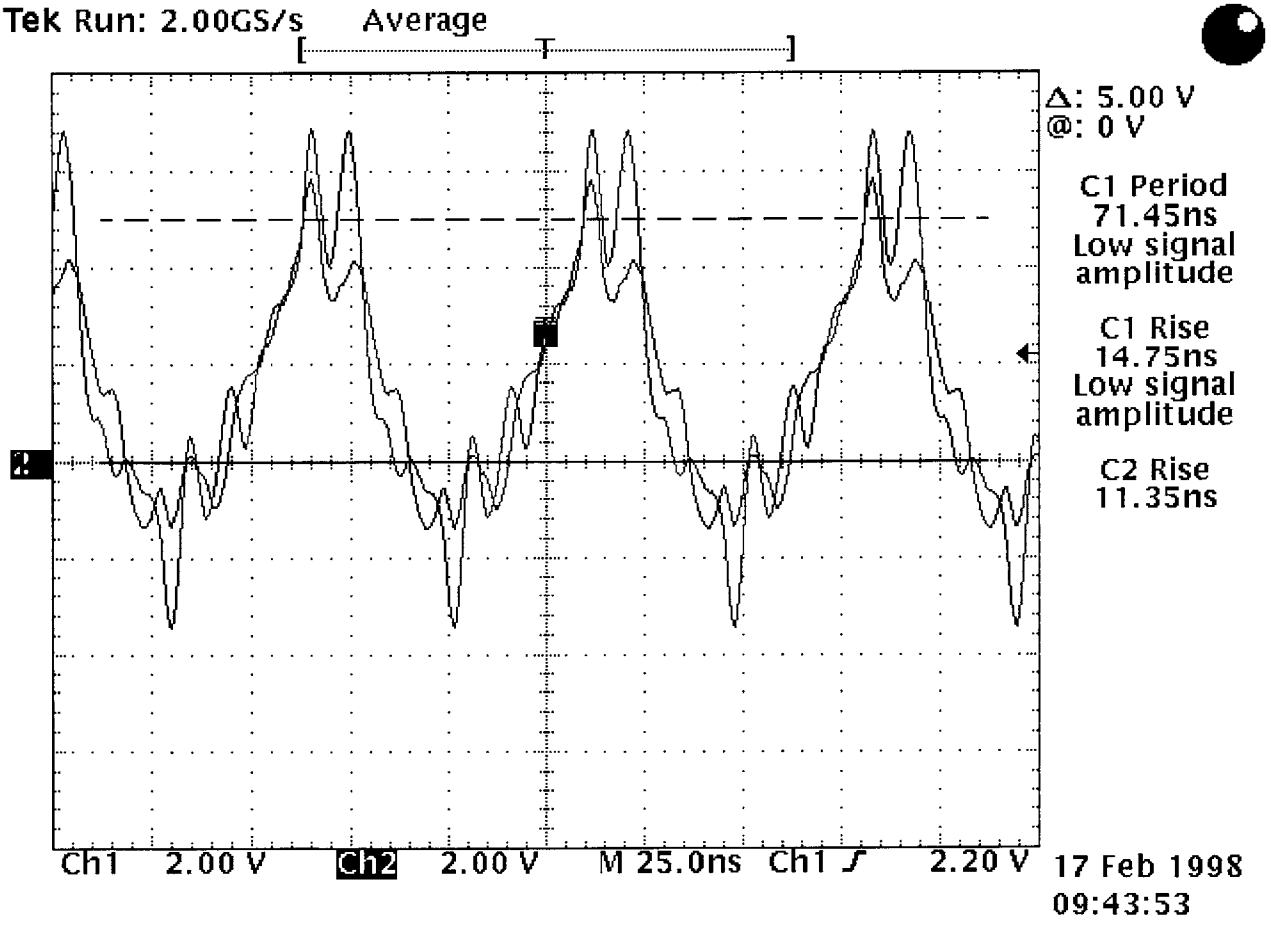

Figure 4.8 Clock Signal of the Standard Driver

4.2.5 Driver with Uniform Transmission Line

This section will describe the results from testing the clock driver with a uniform transmission line. I begin with a circuit schematic followed by a table of power and rise time results. At the end of the section, I have included a printout of the clock signals produced by the driver. Figure 4.9 shows the schematic for the uniform transmission line driver. Please notice that four of the inverters have been disconnected to provide a smaller driver. Further, the value of R_{DRIVER} is varied quite extensively from case to case. For all the test cases C_{LOAD} is fixed at 2.2 nF and the frequency at 14 MHz. The frequency was chosen by setting the initial length and then changing the frequency of the oscillator to the "sweet" spot of the transmission line. The impedance of the entire transmission line is fixed at approximately 10Ω.

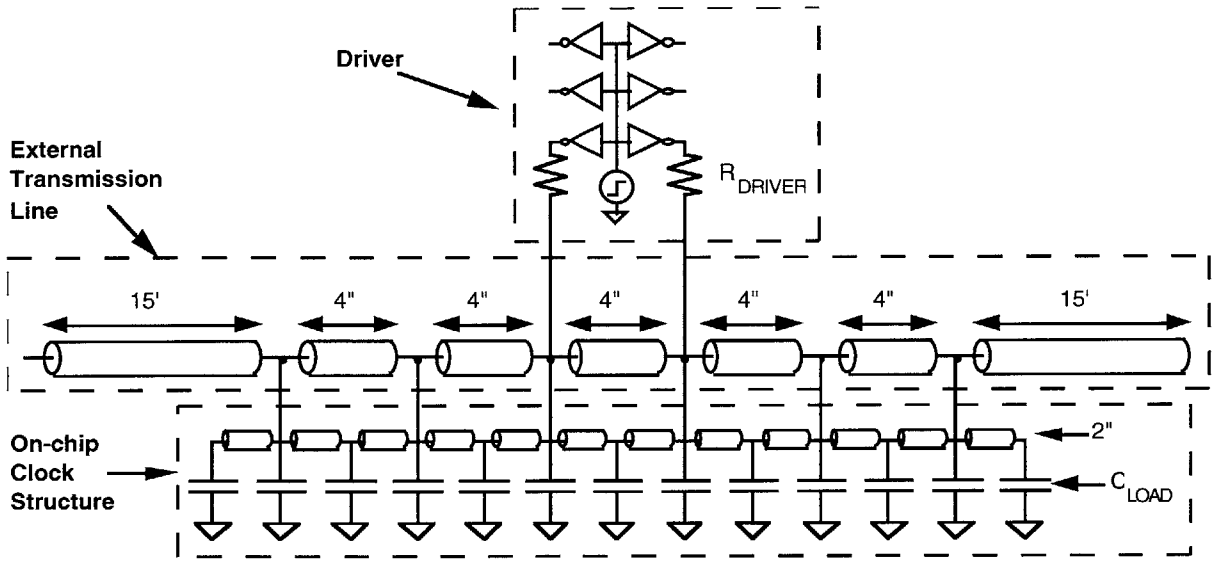

Figure 4.9 Clock Driver with Uniform Transmission Line

Table 4.3 shows the power for many different driver widths, w. In order to calculate the normalized power at 20 MHz, w/w_{STD} and P is substituted into Equation 4.2. Based on the rise time and overall quality of the waveform, the point where the transmission line driver matches the standard clock driver appears when $w/w_{STD}=0.07$. At this width, the transmission line clock driver consumed 0.42 W and saves a factor of **5.7** over the standard clock driver.

Below in Figure 4.10 I have included a plot of the uniform transmission line driver. This was run at 14 MHz, a period of 71.5 ns. The width of the driver, w, was set to 0.07 times the width of the standard driver, w_{STD}. This was done by introducing a resistor between the driver and the load. Channel 1, C1, corresponds to the center of the chip and Channel 2, C2, corresponds to the edge of the chip. The quality of this waveform is quite superior to that found with the standard driver in Figure 4.8, even though the driver width and power are significantly smaller.

	Center T	Edge T	P	w/w_{STD}	P_{NORM}
Extension w/1 drive & 47Ω	14.1 ns	20.5 ns	0.32 W	0.04	0.33 W
Extension w/1 drive & 27Ω	14 ns	19 ns	0.35 W	0.06	0.39 W
Extension w/1 drive & 22Ω	10 ns	19 ns	0.37 W	0.07	0.42 W
Extension w/1 drive & 6.7Ω	6.6 ns	18.8 ns	0.38 W	0.15	0.49 W
Extension w/1 drive	4.6 ns	19.3 ns	0.40 W	0.33	0.62 W

Table 4.3 Mock-up of Clock Driver with Uniform Transmission Line

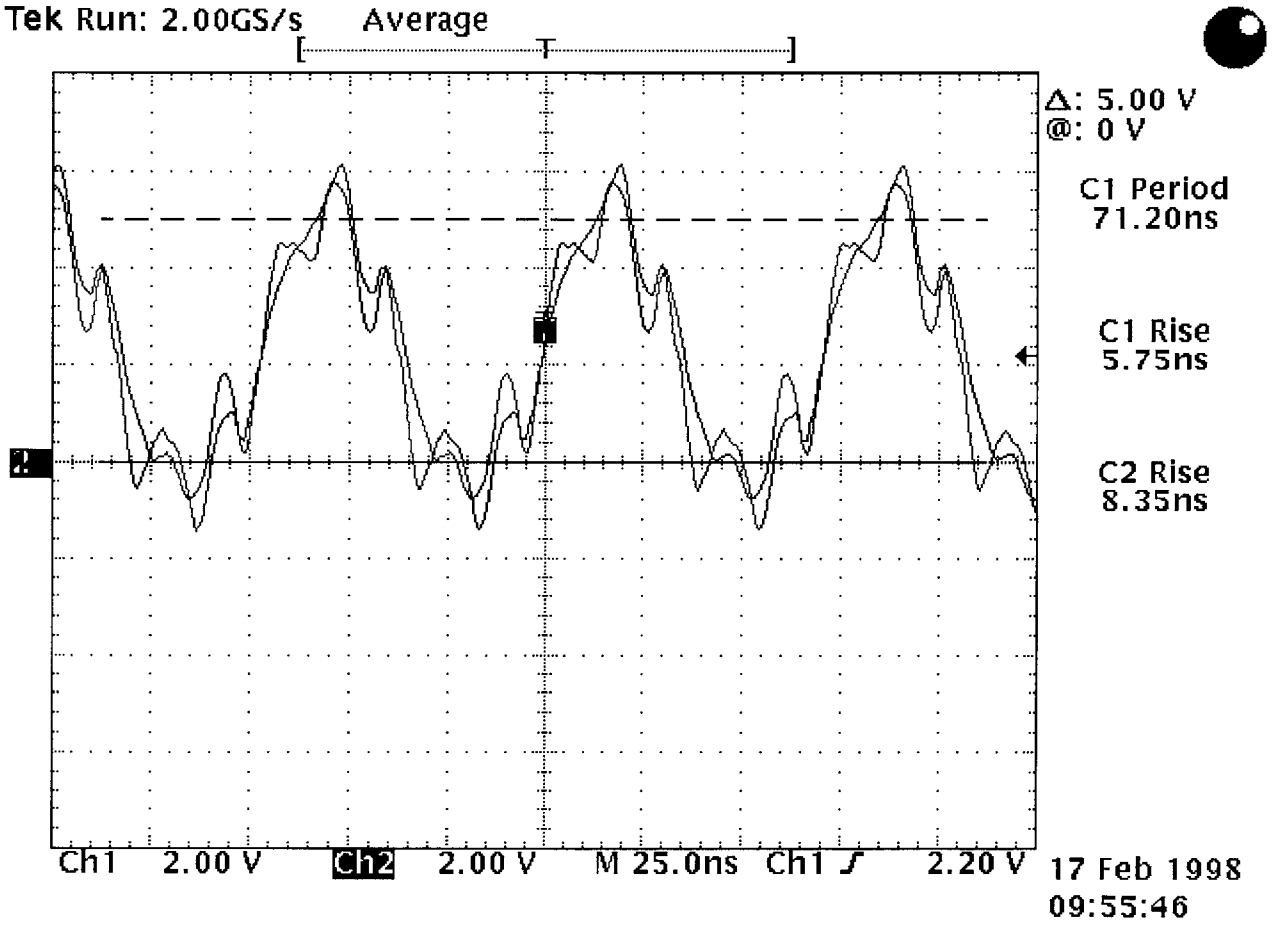

Figure 4.10 Clock Signal of the Driver with a Uniform Transmission Line

4.2.6 Driver with Tuned Transmission Line

This section will describe the results from testing the clock driver with a tuned transmission line. I begin with a circuit schematic followed by a table of power

and rise time results. At the end of the section, I have included a printout of the clock signals produced by the driver.

Figure 4.11 shows the schematic for the tuned transmission line driver. Please notice that four of the inverters were disconnected to provide a smaller driver. Further, the value of R_{DRIVER} is varied quite extensively from case to case. For all the test cases C_{LOAD} is fixed at 2.2 nF and the frequency at 16.4 Mhz. Again, the structure and lengths of the transmission line was chosen according to theory and then fine tuned by adjusting the frequency source. It would be difficult if not impossible to tune the line purely from the tuning equations because of unknown parasitics and load anomalies.

The tuned line reinforces the first and third harmonics of a 16.4 MHz square wave. I use a low impedance, 10Ω, for my central section: five 4 in. sections and a pair of 8 in. sections. Beyond this a 15 in. section of higher impedance, 35Ω, and a 4 ft. 8 in. of low impedance, 10Ω, tune for each harmonic.

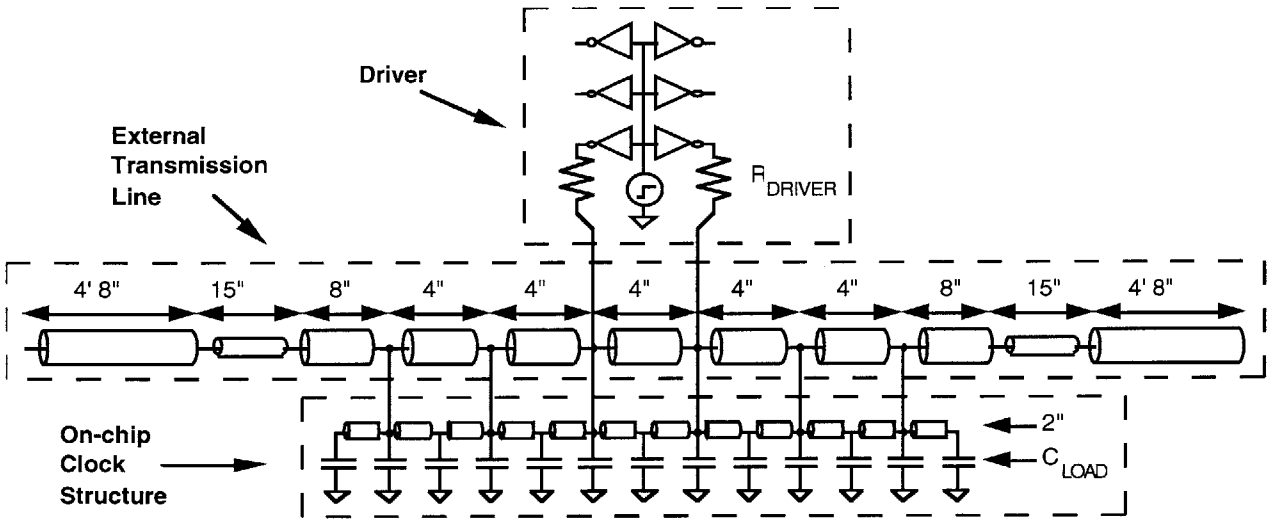

Figure 4.11 Clock Driver with Tuned Transmission Line

Table 4.4 shows the power consumption and rise times of the complex resonating transmission line for many different driver widths. Based on the rise time and overall quality of the waveform, the point where the complex transmission line driver matches the standard clock driver appear when w/w_{STD} = 0.06. At this width the transmission line clock driver consumes 0.24 W and saves a factor of **9.5** over the standard driver.

	Center T_R	Edge T_R	P_{MEAS}	w/w_{STD}	P_{NORM}
Extension w/1 drive & 47Ω	19.9 ns	21.0 ns	0.27 W	0.04	0.20 W
Extension w/1 drive & 27Ω	5.6 ns	14.5 ns	0.29 W	0.06	0.24 W
Extension w/1 drive & 22Ω	5.0 ns	14.2 ns	0.3 W	0.07	0.26 W
Extension w/1 drive & 6.7Ω	3.5 ns	12.1 ns	0.33 W	0.15	0.35 W
Extension w/1 drive	3.2 ns	12.1 ns	0.33 W	0.33	0.46 W

Table 4.4 Mock-up of Tuned Transmission Line Clock Driver

Below in Figure 4.12 I have included a plot of the complex transmission line driver. This is run at 16.4 MHz, a period of 61.1 ns. The width of the driver, w, was set to 0.06 times the width of the standard driver, w_{STD}. Channel 1, C1, corresponds to the center of the chip and Channel 2, C2, corresponds to the edge of the chip. The quality of this waveform is quite superior to that found with the previous drivers, even though the driver width and power are significantly smaller.

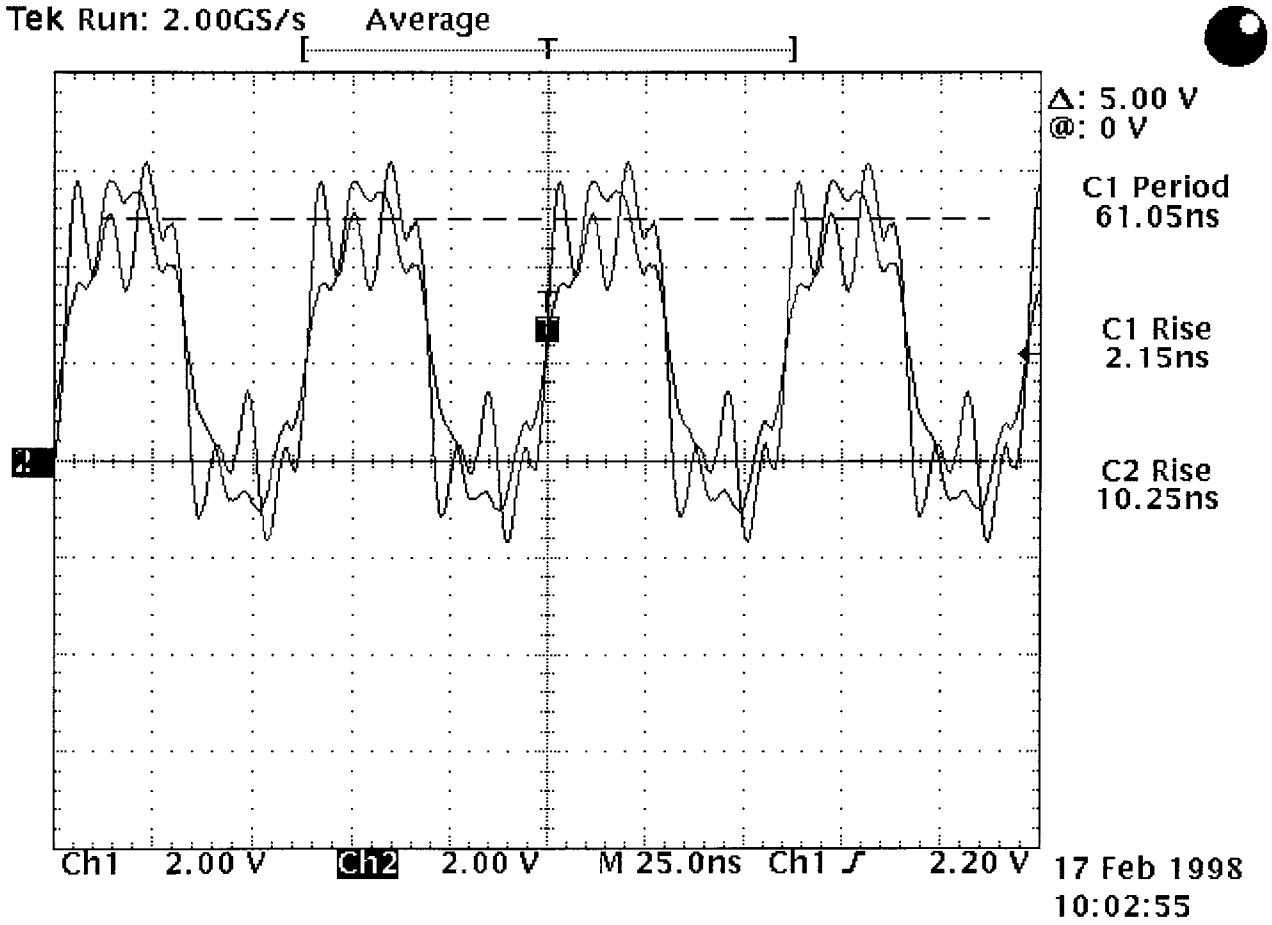

Figure 4.12 Clock Signal of the Driver with a Tuned Transmission Line

4.3 Hspice Simulations

The hspice simulations have proven the applicability of the transmission line clock driver technique to current and future process generations. The simulations focus on a 1 GHz driver. The power savings comes in at roughly **a factor of 4.** This is significantly lower than originally expected from the mockup results. The likely cause is the cutoff frequency of the flip-chip bumps.

The first section will list some of the assumptions and simplifications made for simulation purposes. The second section will describe how the standard clock driver performed with respect to power, transition times and skew. The third section delves into the transmission line driver simulations. The final section will explore the practical issues of how to tune for a given waveform.

4.3.1 Overview

The basic structure is a square chip, 1.6cm on a side. The 4nF load is evenly distributed and driven at a frequency of 1 GHz. Parasitic inductance and resistance are included relative to this frequency. The transistor length is 0.24 um which for a fanout of 4 produces transition times of 130 ps. Vdd is set at 1V.

In order to reduce simulation times, the actual schematics model only a 1/16th wide section of the chip. The RC skew of the clock net can be measured between the center and edge along the long dimension. The standard driver uses a split driver in which each part drives 2 mm off center. The transmission line driver uses a single center driver.

To compare the simulated power against a full chip like the Alpha 21164, one would need to multiply the simulation power by approximately 3.3. This would include a factor of 11 for the vdd differential from 3.3V to 1V. And it would include 0.3 for the lower frequency of the Alpha, 300 MHz. The power already includes the factor of 16 related to the reduced simulation width.

Please refer to the appendix for the schematics of all 1 GHz simulations.

4.3.2 Standard Clock Driver

Figure 4.13 shows the block digram used to simulate the standard driver. The size of the final driving stage totals 8 mm of width. Both the pre-driver power and the final driver power are measured separately. The pre-driver sizes increase by a fanout of four.

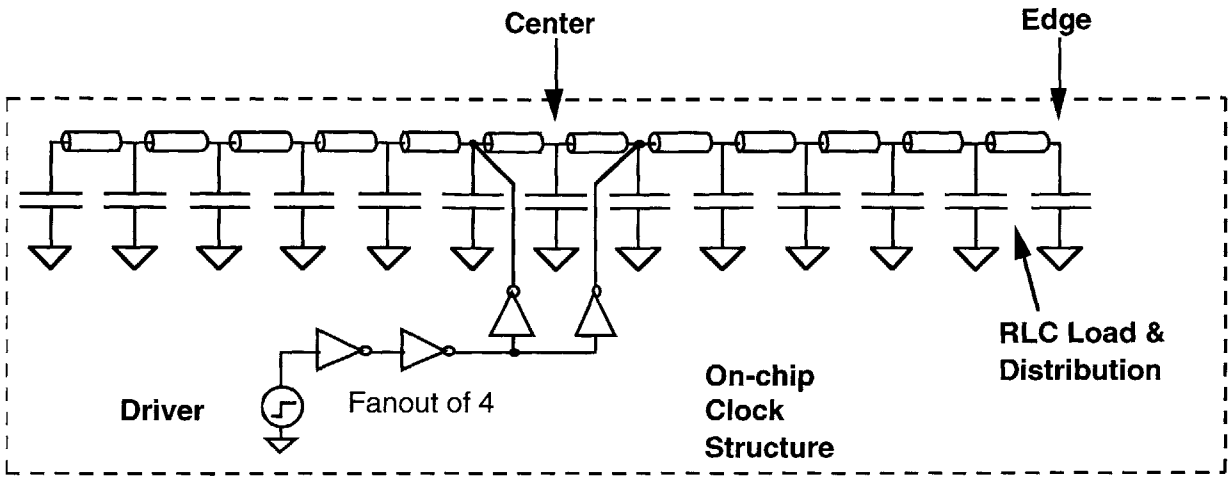

Figure 4.13 Schematic of Standard Driver

Figure 4.14 shows the waveforms at the center and edge of the chip. These should represent the extremes for the purposes of skew and transition times.

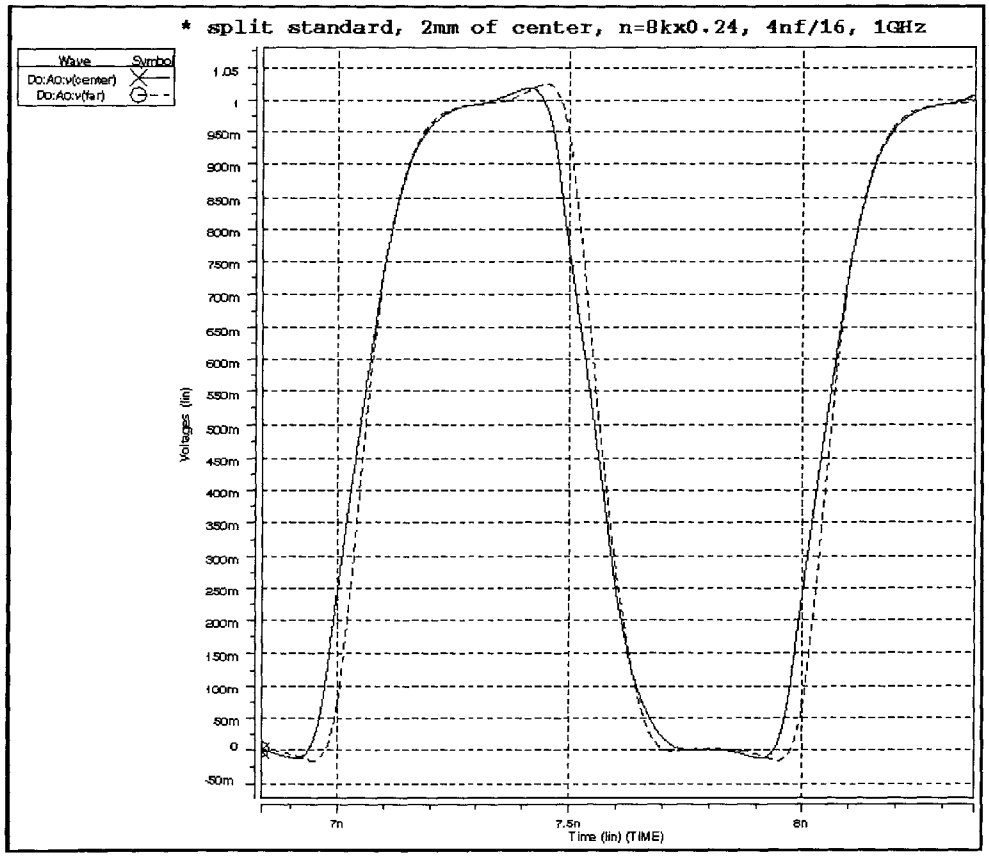

Figure 4.14 Waveforms at Center and Far Edge of Chip in Standard Driver

The important results from the simulations are that the transition times are a maximum of 130 ps. This represents 13% of the total cycle time, which roughly compares with the expectations from the numbers published for the Alpha 21164. The skew across the entire 16 mm chip is approximately 30 ps. Finally, the power consumed is 6.5W, where the pre-driver contributes approximately a third. Once scaled by 3.3, this power, 21.5W, which matches closely the 20W reported for the Alpha 21164.

4.3.3 Transmission Line Driver

Figure 4.15 shows the schematic used to simulate the transmission line driver. The size of the final driving stage totals only 2.8 mm of width. This is almost a factor of three smaller than the driver width in the standard case. Further, the driver is not split, but consolidated in the center. This should be easier to build and control.

The transmission line and load appears above. The first part with an impedance of 2Ω consists of the short sections connected to the chip through flip-chip bumps and the first extension. Combined the length is 42 mm long. The second wing has an impedance of 7.25Ω over its length of 25 mm. The flip-chip bumps shown as circles in the figure can be modeled as 100pH inductors.

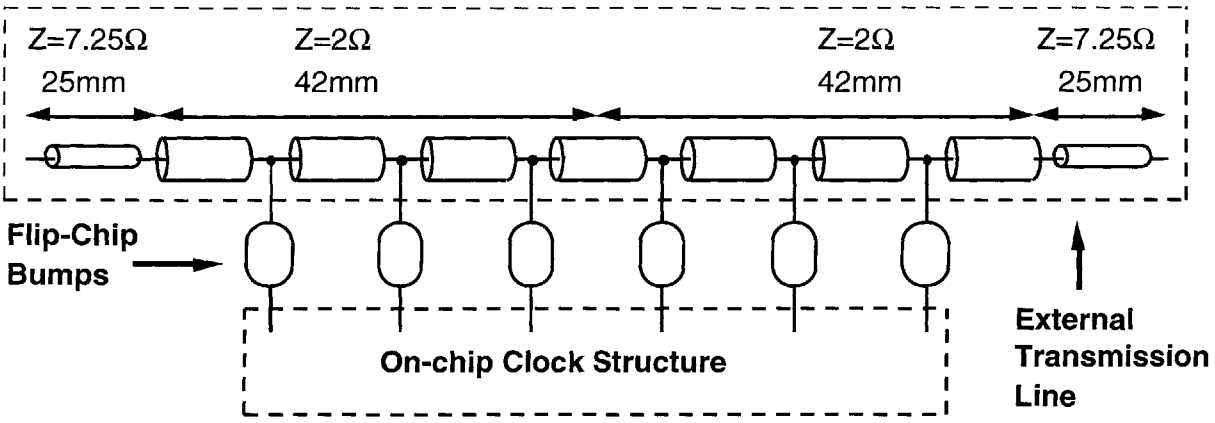

Figure 4.15 Schematic of Transmission Line Driver

Figure 4.16 shows the center and edge waveforms for the transmission line driver. The important results from the simulations are that the transitions times are slightly lower, about 125 ps. The skew is about 30% better across the entire 16 mm chip, only 20 ps. Finally, the power consumed is a factor of 4 better than the standard at only 1.6W. An interesting side point is that, because the final driver is helped by the transmission line, the pre-driver consumes a larger percentage of the total power, almost 40%.

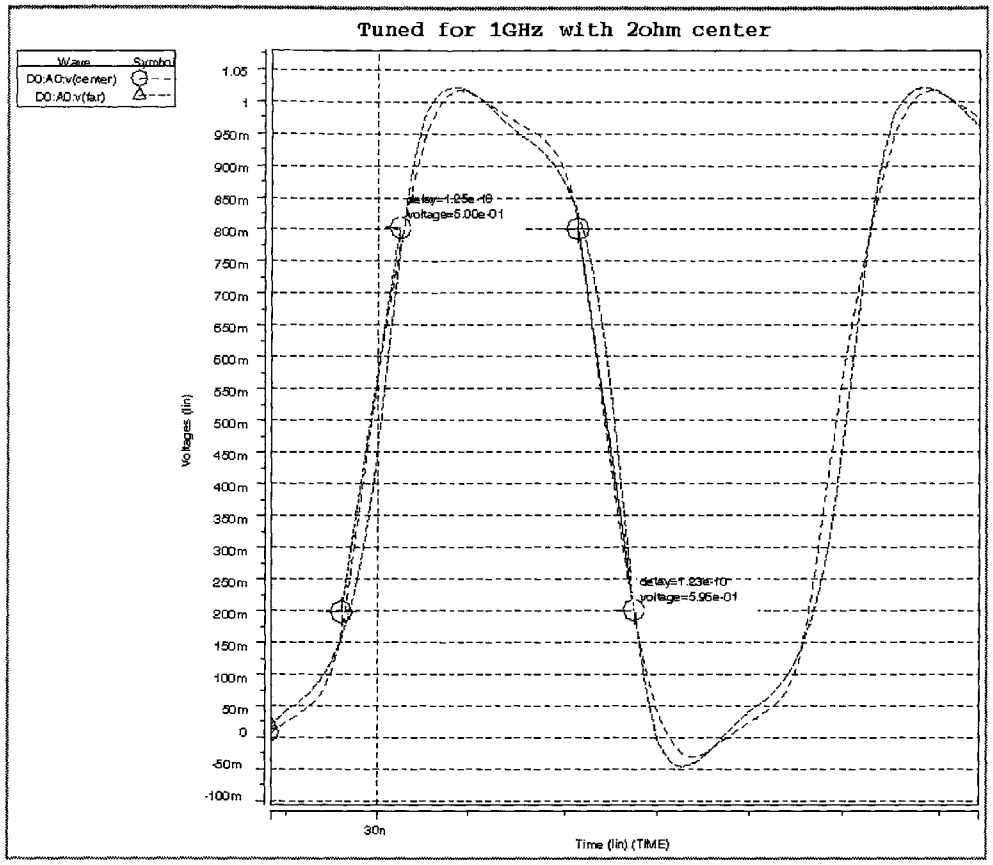

Figure 4.16 Waveforms of T-line Driver

4.3.4 How to Really Tune a Line

Determining the correct transmission line for a given load involves some amount of trial and error to find the sweet spot of the system, but a large portion relies on the tools developed in the first two chapters. Let me begin by listing the basic steps:

1) Determine cap/length of load and chose an impedance
2) Chose a tuning strategy
3) Set basic length for the desired frequency
4) Chose location and effect of discontinuities
5) Sweep discontinuity sizes until other harmonics are tuned
6) Repeat to get to the sweet spot...

Step one of the process begins by determining the capacitance per unit length of the load. This gives a rough idea of the level of impedance needed. Basically, the impedance level must be sufficiently low so that the line can drive the load. However, an impedance that is too low will burn extra power, because the current

in the line is related to the impedance, while the power is related to the parasitic resistance. As the impedance falls, the current rises, V/Z, which makes the parasitic power rise, $I^2R_{parasitic}$. A factor of 5 lower C_l in the transmission line versus the load/length is a good starting point.

Step two is to pick a basic impedance variation strategy. For this case, I chose to tune the base length for the third harmonic and use discontinuities to tune the 1st harmonic into place. By placing discontinuities at the voltage maximum of the 3rd harmonic, I can affect the first harmonic exclusively.

Because the flip-chip connections have such a high inductance, 100pH, they filter out much of the 5th harmonic. This removes any performance improvement that could have been obtained by tuning for the 5th harmonic. Figuring out this ugly fact involved some of that trial and error mentioned in the first paragraph. For better connections or lower frequencies, I might tune the base length for the 5th harmonic and then use two discontinuities to tune the 1st and third. Alternately, one could tune the fourth harmonic into location and then tune the other harmonics into place. The space of tuning ideas is quite large.

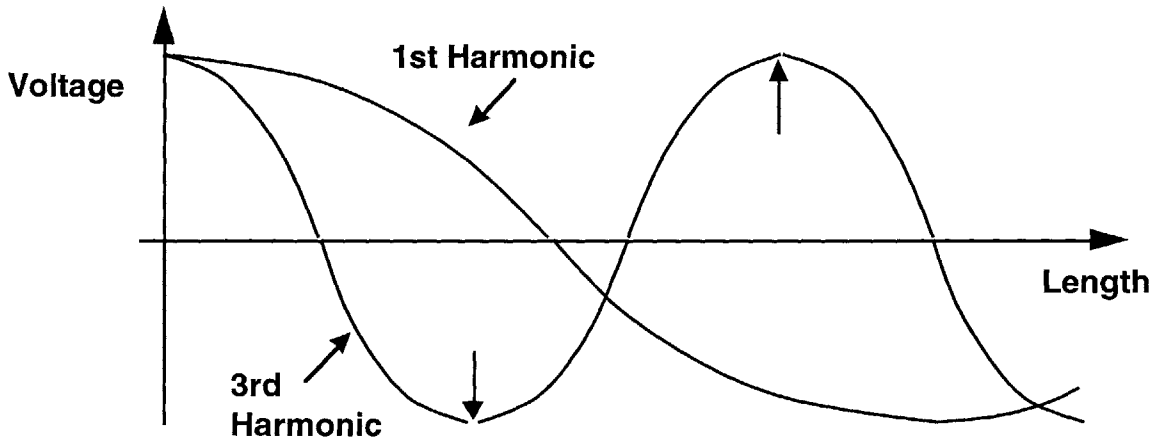

Figure 4.17 Line Voltages through Step 3

Step three involves running the first Hspice AC simulation to set the length of a uniform line to the desired frequency. The driver should be a sinusoidal driver that is swept through the frequencies of interest. Change the length until the voltage peaks at the given location. As shown in Figure 4.17, the third harmonic fits exactly in the channel, while the 1st harmonic still needs some tuning.

Once the length is correct, step four involves checking for the location where you want to place the discontinuities. As mentioned before I used the maxima for the third harmonic, which are marked with arrows in Figure 4.17. The end ones are not useful, because they are the open termination points. The two centrally located ones however are valuable. Now comes a little cheat sheet, Figure 4.18, to help decide how a discontinuity will affect a given waveform. If you recall from chapter 3, an impedance discontinuity will introduce a shift in phase based on the current phase. As shown in the diagram if the voltage is positive and rising then that location has a phase between 0° and 90°. A positive jump in impedance at this

location will add phase or lower the frequency. Each of the regions and the subsequent effect of increasing impedance is shown below in Figure 4.18.

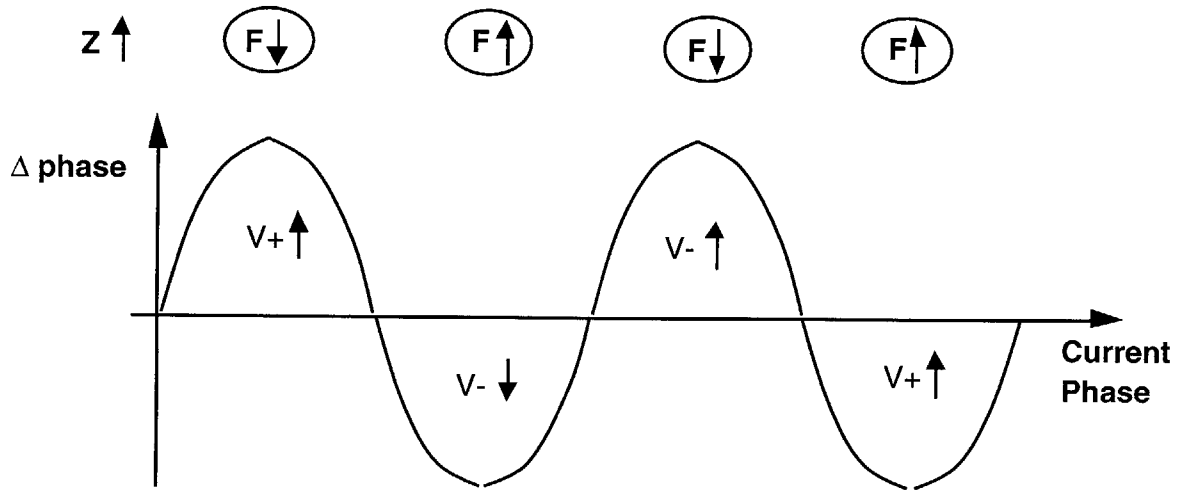

Figure 4.18 Cheat Sheet for Tuning a Line

Going back to our simulation, the line is tuned for too low a frequency. A positive phase shift is needed to shift the frequency higher and make the first harmonic fit. At the left maximum, the voltage is positive and falling, so a negative step in impedance will shift the frequency higher. At the right discontinuity, a positive step will shift the frequency higher, because the voltage is negative and falling. Since higher impedances are easier to build, that is typically the one to chose.

As step 5 suggests, one should sweep across multiple discontinuity sizes located at this right location until the first harmonic is aligned. Finally step 6 suggests that the process should be repeated for different tuning styles and initial impedances to find the most appropriate. The primary reason one would need to repeat is because the tuning equations do not incorporate nearly as much detail as Spice does. In this particular case the model neglects parasitics and much of the loading model. Until the synthesis technique can be updated with these important secondary issues, it can only provide a great starting place and a guide to expected effects. The repetition with Spice is still needed to find the sweet spot of each system.

4.4 Application Conclusions

Two sets of results have been presented in this chapter. One for the 20 MHz mockup and one for the 1 GHz simulations. In the large scale mockup a uniform impedance tuned to the correct length reduces power consumption by a factor of 5.8 relative to a standard clock driver. And using an impedance tuned transmission line saves a factor of 9.5 over the standard driver with the bonus of much cleaner waveforms. From the 1 GHz simulations, we found that the power falls by a factor of 4 and the skew improves by about 30%

5. Secondary Effects

5.1 Outline

This chapter focuses on a variety of secondary issues from impedance reduction to the effects of parasitic resistance. The next section describes how to use vertical and horizontal stacking to reduce impedance. The second section explores two skew reduction techniques, the removal of edge connections and usage of a "hairy" chip model. The third section derives skin depth and parasitic resistance for a strip line. The effect of the parasitics is included in the velocity and then in the voltage amplitude. The fourth section mentions the issues associated with choosing a dielctric. The last two sections explore the effect of variability in capacitance and physical dimensions.

5.2 Impedance of a Stacked Transmission Line

A few configurations, shown in Figure 5.1, can increase the capacitance of the transmission line. Arguably the simplest is to stack lines as shown on the left of Figure 5.1. The five conducting layers alternate between gnd and signal. The transmission line in the figure would have four times the capacitance of a single line with similar dimensions: spacing, width and length.

The right configuration, similar to fractal capacitors, involves interleaving the conducting layers in the horizontal dimension as well as the vertical. [Lee] For channels with equal horizontal space and vertical space, the interleaving increases the surface area and capacitance by roughly another factor of 2. Also as interconnect technology scales, the minimum height of the wires increases relative to the minimum width, which means that horizontal interleaving provides an even larger advantage.

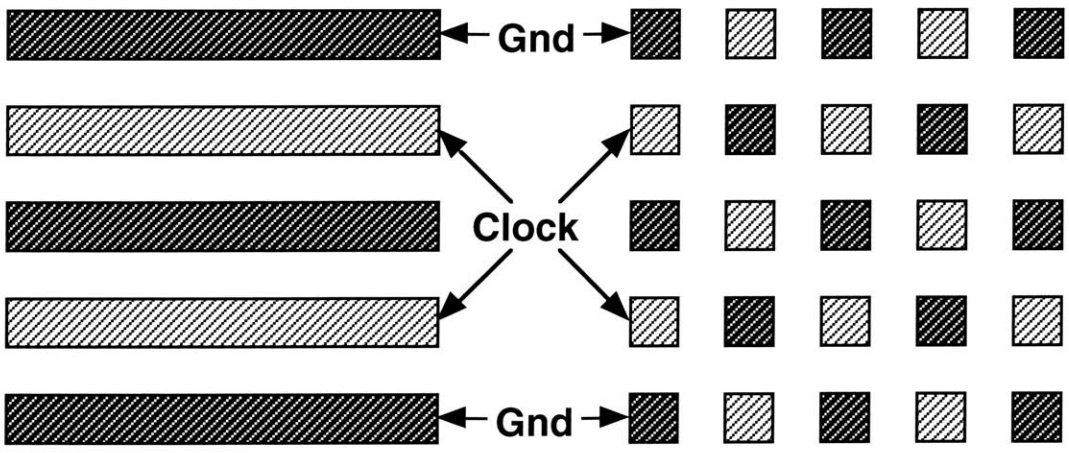

Figure 5.1. Cross-section of Low Impedance Transmission Lines

An approximation for the capacitance and inductance can be made by modifying the equations presented in Chapter 2. The final term includes horizontal

and vertical interleaving based on N, the number of conducting channels, which for the case on the left of Figure 5.1 would be 4.

$$C_l = \varepsilon_o \left(8.85\times10^{-12}\,\text{F/m}\right)\left(\frac{w}{h}\right)\left(2N_{\text{conducting channels}}\right)$$

$$L_l = \left(4\pi\times10^{-7}\,\text{H/m}\right)\left(\frac{h}{w}\right)\left(\frac{1}{2N_{\text{conducting channels}}}\right)$$

In the velocity equation rewritten below, the 2N term and the 1/2N term would simply cancel out. In other words the number of conductors has no effect on the propagation of a wave. Physics explains that velocity depends solely on the material properties of the dielectric. Based on the numbers presented in chapter 2, the velocity, v, would remain 1×10^8 m/s.

$$v = \frac{1}{\sqrt{L_l\left(1/2N\right)C_l(2N)}} = 1\times10^8\,\text{m/s}$$

In the impedance equation rewritten below, the 2N term and the 1/2N term multiply. In other words the number of conductors reduces the impedance by a factor of 2N. Based on the numbers presented in chapter 2, the impedance would fall to 0.314Ω/2N.

$$Z_o = \sqrt{\frac{L_l\left(1/2N\right)}{C_l(2N)}} = \sqrt{\frac{3.14\times10^{-9}\,\text{H/m}}{3.19\times10^{-8}\,\text{F/m}}}\sqrt{\frac{1}{4N^2}} = 0.314\Omega/2N$$

A microprocessor presents a load of 3.7nF spread across 2 cm of length. This can be massaged into an effective capacitance per unit length of 3.7nF/2cm or 1.9×10^{-7}F/m. In order for a resonator to drive such a capacitive load, it must have appreciably more capacitance. A stack of 11 conductors with 10 channels could be used in conjunction with horizontal interleaving to increase the capacitance per unit length of a single line by a factor of 20, making it significantly larger than the clock load. The height of the channel, 50um is an assumption of today's ceramic process parameters. The width is set by the width of the chip to be driven in our previous applications

$$C_l = 9\left(8.85\times10^{-12}\,\text{F/m}\right)\left(\frac{2\text{cm}}{50\mu\text{m}}\right)\left(2\times10\,\text{conductors}\right)$$

$$C_l = 6.38\times10^{-7}\,\text{F/m}$$

The inductance per unit length would consequently fall by a factor of 20.

$$L_1 = \left(4\pi \times 10^{-7}\,\mathrm{H/m}\right)\left(\frac{50\mu\mathrm{m}}{2\mathrm{cm}}\right)\frac{1}{(2 \times 10\,\mathrm{conductors})}$$

$$L_1 = 1.57 \times 10^{-10}\,\mathrm{H/m}$$

5.3 Clock Skew from Rise Time Differences

Beyond power, one of the very exciting prospects of this design regards clock skew. Ideally the **entire** resonating transmission line crosses through 1/2 Vdd at the **same** time. In real cases, the clock load, interconnect delay and dispersion within the transmission line introduce a minimal amount of skew, less than 10 ps. This performance figure is almost an order of magnitude better than what is achieved in the Alpha!!

Unfortunately, though the center crossing is relatively well controlled, the differences in rise and fall times across the chip can be serious. Consider the situation in the frequency domain as shown in Figure 5.2. In the frequency domain, our clock waveform decomposes into a sum of sinusoids. The primary components are the 1st, 3rd and 5th harmonics. As we move farther away from the center of the chip, the amplitudes of the third and the fifth harmonics fall off more quickly than the first, because of the structure of the standing wave. This degrades the rise and fall times at the edge of the chip.

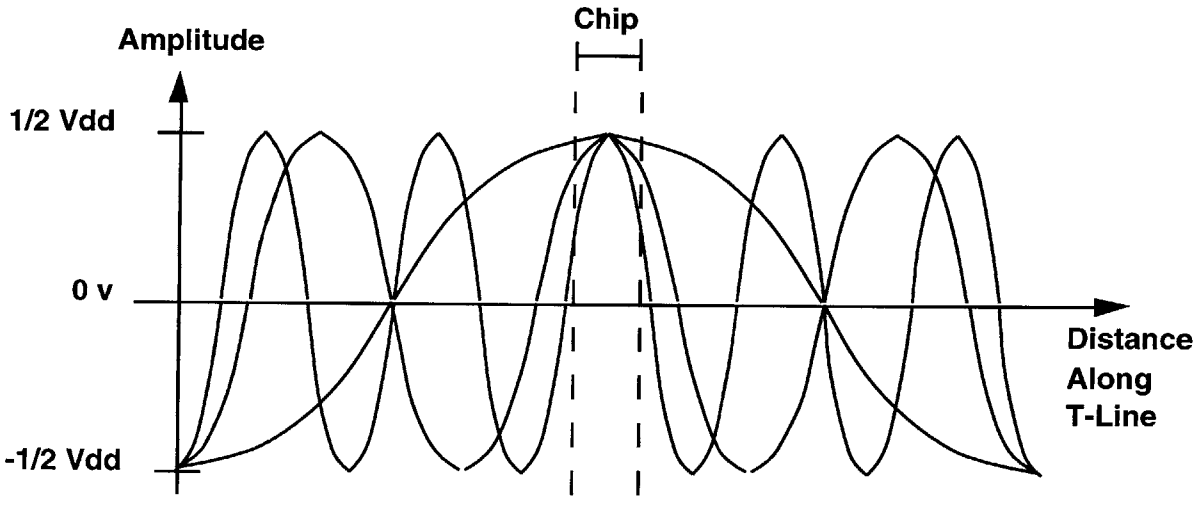

Figure 5.2 Frequency Domain View of Skew Problem

Figure 5.3 shows the situation for a rising edge of the clock waveform at various points across the chip. The center of the chip has a very nice rise time, while the edge of the chip has a much longer rise time.

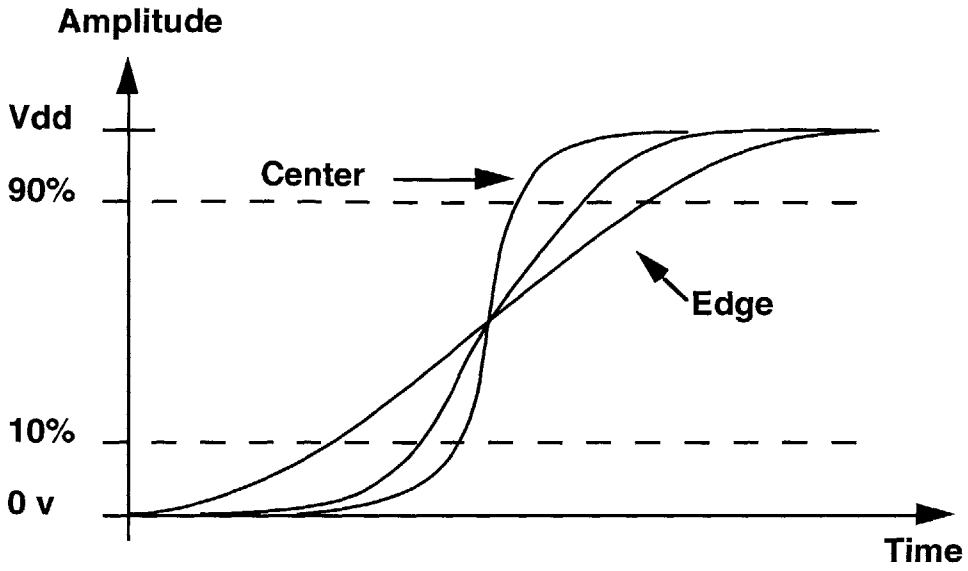

Figure 5.3 Rising Edge of Clock Waveform across the Chip

Because our clock waveform feeds pre-charge style circuitry as well as static circuitry, skew must be measured throughout a large range of voltages. With static logic, skew is measured at roughly 1/2 V_{dd}, the inverter threshold voltage. However, in pre-charge circuits, when the clock reaches an p- or an n-device threshold, pre-charged nodes can begin to discharge. Taking this into account, the maximum skew could occur not at 1/2 V_{dd}, but at a higher, or lower, voltage. Figure 5.3 shows skew measured from the center's 90% point to the edge's 90% point. This assumes that the device thresholds are approximately 10% of the power supply voltage.

5.3.1 Clock Skew Reduction - No Edge

Since the waveforms degrade quickly as one moves farther away from the center, we can reduce skew by disconnecting the edge of the chip. In this way an interior point with a better rise time propagates to the edge of the chip. Figure 5.4 shows this new configuration.

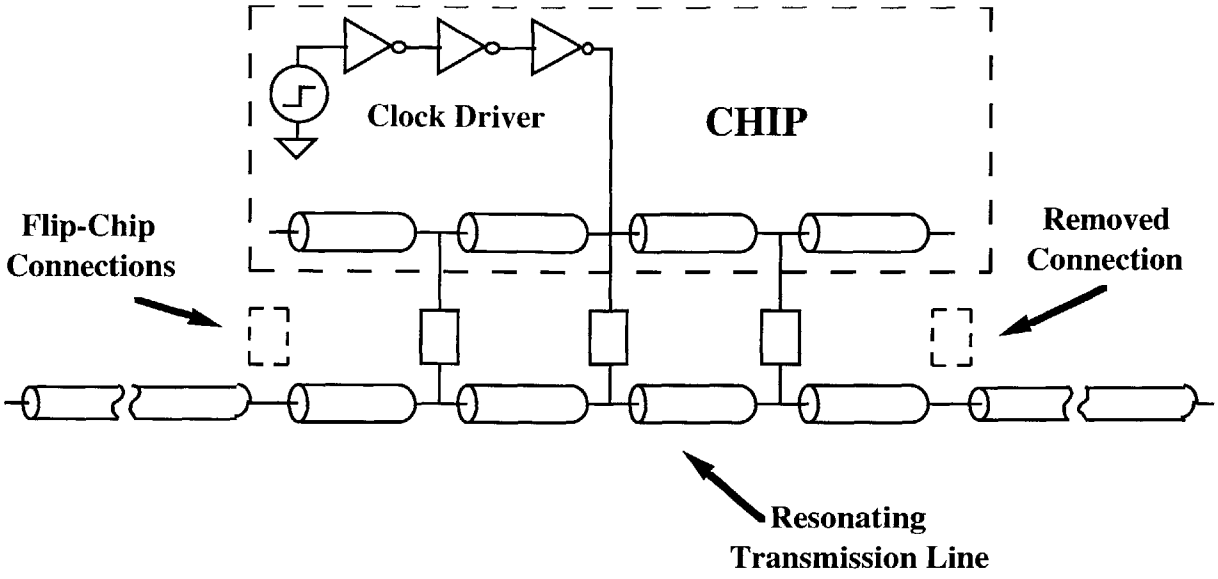

Figure 5.4 Clock Structure to Reduce Clock Skew

Figure 5.5 shows the rising clock waveform at various points across the chip. The center of the chip has a nice rise time. The edge of the chip receives a delayed version of the rising edge from an interior connection. The maximum skew again occurs at the 90% point. It can be measured from the center's 90% point to the edge's 90% point. This turns out to be half of the skew in the previous version.

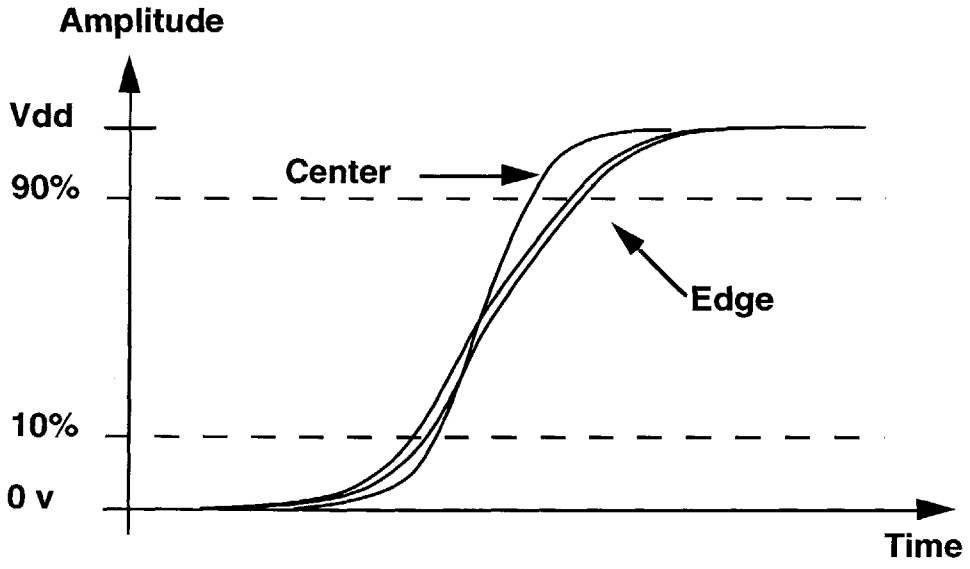

Figure 5.5 Rising Edge of Clock without Edge Connections

5.3.2 Clock Skew Reduction - Hairy Chip

As described in Section 5.3, signals farther from the center of the line have worse rise times than those at the center. And from Section 5.3.1, the situation can be improved by shifting the sampling point closer to the center of the line. Another option would be to give each sampling point its own transmission line, as shown in Figure 5.6. In this way each sampling point will receive the best signal possible.

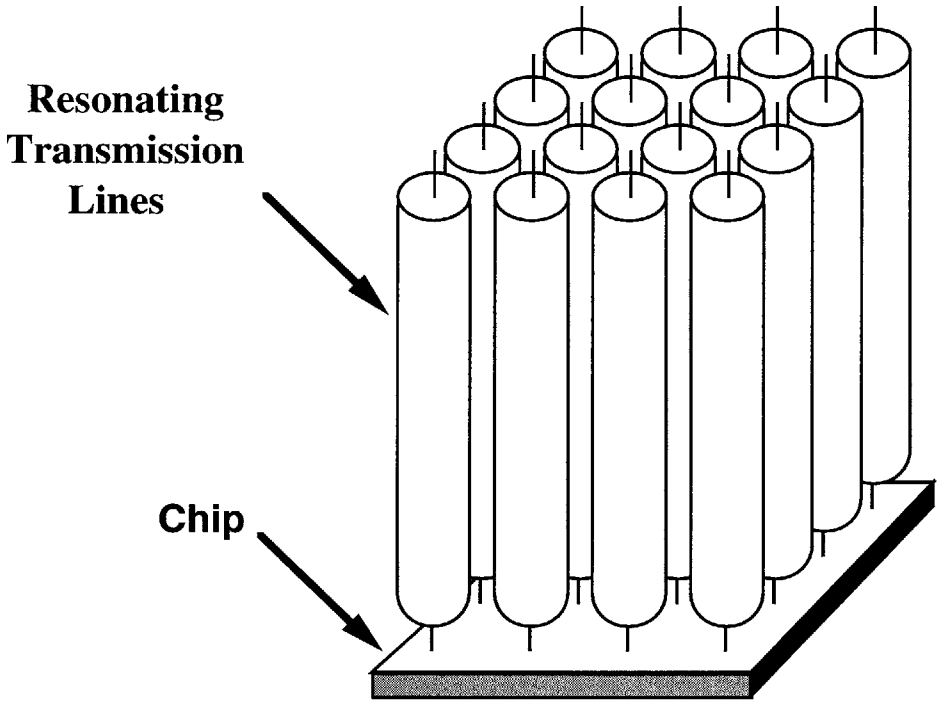

Figure 5.6 Concept of Hairy Chip

Figure 5.7 shows how the transmission lines can be folded into the substrate. For visual compactness the figure has been simplified to just 4 separate lines. Though this implementation is realizable, designing the layers may prove complex, especially with horizontal **and** vertical stacking. Secondly, it may not be reasonable for the separate lines to share a ground plane because of coupling.

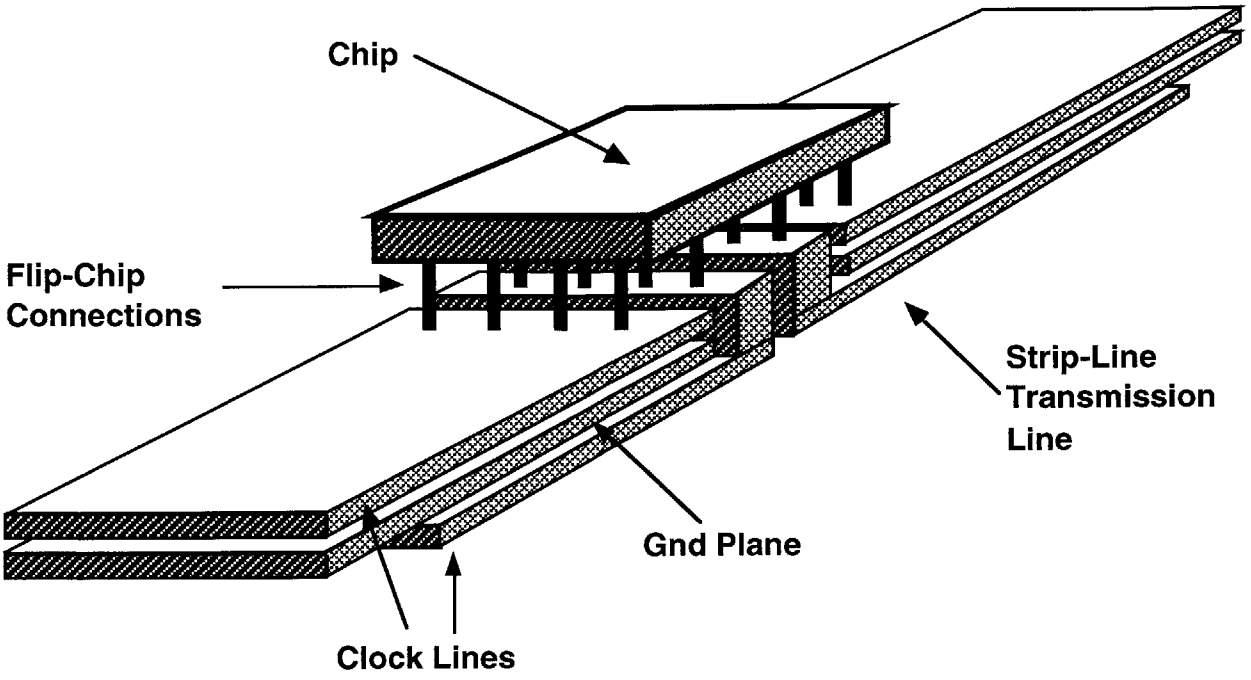

Figure 5.7 Possible Implementation of Hairy Chip

5.4 Skin Depth and Parasitic Resistance

The parasitic resistance will have a minimal effect on the velocity and a more significant effect on line losses. In order to calculate resistance, we must first calculate the skin depth at each harmonic, the frequencies of interest. We will be using copper with a resistivity, ρ, of 1.72×10^{-8} Ωm. To first order, the following equation for skin depth, δ, should hold:

$$\delta(f) = \sqrt{\frac{\rho}{\pi f \mu}}$$

Equation 5.1

$$\delta(f) = \sqrt{\frac{1.72\times10^{-8}\,\Omega\mathrm{m}}{\pi f\left(4\pi\times10^{-7}\,\mathrm{H/m}\right)}} = \frac{6.6\times10^{-2}\,\mathrm{m\cdot s^{-1/2}}}{\sqrt{f}}$$

Since 95% of the current flows within three skin depths of the surface, we must chose our metal thickness greater than this. For example, at a base frequency of 1 GHz, the thickness should be at least:

$$\text{Thickness} > 3\bullet\delta(1\mathrm{GHz}) \text{ or } 6.26\,\mu\mathrm{m}$$

If the wire thickness is large compared to the skin depth, the following calculations for resistance per unit length should hold. For the higher frequencies,

like the other harmonics of a square wave, the skin depth is even smaller so the approximation should only improve.

$$R_l(f) = \rho \frac{1}{\delta(f)} \frac{1}{w}$$

$$R_l(f) = 1.72\times10^{-8}\,\Omega m \frac{\sqrt{f}}{6.6\times10^{-2}\,m\,s^{-1/2}} \frac{1}{2cm} = \left(2.61\times10^{-7}\,\Omega/m\right)\sqrt{f}$$

$$R_l(1GHz) = 8.25\times10^{-3}\,\Omega/m$$

$$R_l(3GHz) = 0.0143\,\Omega/m$$

$$R_l(5GHz) = 0.0185\,\Omega/m$$

5.4.1 Effect on velocity

Because the frequencies of interest are so high, the inductance dominates the parasitic resistance. This means the frequency dependent parasitics won't impact the velocity significantly. An ideal transmission line has a velocity derived in Chapter 2, while a real line with parasitics would be more complex.

$$v = \frac{1}{\sqrt{L_l C_l}} = 1\times10^{8}\,m/s$$

$$v = \frac{1}{\sqrt{L_l C_l}\left[1 - \frac{R_l G_l}{4\omega^2 L_l C_l} + \frac{G_l^{\,2}}{8\omega^2 C_l^{\,2}} + \frac{R_l^{\,2}}{8\omega^2 L_l^{\,2}}\right]}$$

Where R is the parasitic resistance of the conducting plates and G is the parasitic conductance of the dielectric. Both parasitics are dominated by the impedance of the inductor and capacitor at the frequencies of interest. Looking at the last term with the numbers explored earlier, we find that the change in velocity due to parasitic resistance is insignificant relative to 1.

$$\frac{R_l^{\,2}}{8\omega^2 L_l^{\,2}} = \frac{\left(2.61\times10^{-7}\,\Omega/m\cdot\sqrt{500MHz}\right)^2}{8\cdot(2\pi\cdot500MHz)^2\cdot\left(1.57\times10^{-7}\,H/m\right)^2} = 1.75\times10^{-11}$$

5.4.2 Effect on voltage

Unfortunately the effect of parasitic resistance and dielectric losses on voltage cannot be neglected. The equation for voltage as described in the second chapter was a pair of waveforms, one forward propagating wave and one reverse. As shown below, each wave consists of 2 exponentials, a real component (α) and an imaginary component (β).

$$V = V_+ e^{-\alpha x} e^{-j\beta x} + V_- e^{\alpha x} e^{j\beta x}$$

The real component (α) is the combination of the dielectric losses and the conductor losses. The conductive losses which result from parasitic resistance are captured in the equation below.

$$\alpha = \frac{R}{2Z_o} = \frac{\left(2.61\times10^{-7}\,\Omega/\mathrm{ms}^{-1/2}\right)\sqrt{f}}{2(0.314\Omega)} = \left(4.15\times10^{-7}\,\mathrm{m}^{-1}\mathrm{s}^{-1/2}\right)\sqrt{f}$$

The dielectric losses are captured in the equation below.

$$\alpha = (\mathrm{loss\,tangent})\left[\pi f\sqrt{\mu\varepsilon}\right] = (0.001)\left[\pi f\sqrt{4\pi\times10^{-7}\,\mathrm{F/m}\cdot 9\cdot 8.85\times10^{-7}\,\mathrm{H/m}}\right]$$

$$\alpha = \left(3.14\times10^{-11}\,\mathrm{m}^{-1}\mathrm{s}^{-1}\right)f$$

For a 1GHz square wave the length of the transmission line would be 5cm, which a wave would need to traverse twice each cycle. The voltage lost for each of the harmonics over the course of this length is shown below. The first term in the exponential represents the conductor parasitics, while the second represents the dielectric losses.

$$\Delta V = e^{-\alpha(1\mathrm{GHz})x} = e^{-(0.0131+0.0314)0.1} = 0.996 \text{ or } 0.44\%$$

$$\Delta V = e^{-\alpha(3\mathrm{GHz})x} = e^{-(0.0227+0.0942)0.1} = 0.988 \text{ or } 1.2\%$$

$$\Delta V = e^{-\alpha(5\mathrm{GHz})x} = e^{-(0.0293+0.157)0.1} = 0.982 \text{ or } 1.8\%$$

The resonance of the transmission line cavity must be such that it retains the appropriate level at the source. The Q of the cavity is defined by the above losses. As the frequency increases, these losses stay relatively constant. The cavity length varies inversely with frequency which offsets the dielectric losses that vary directly with the frequency.

5.5 Choosing a Dielectric

A few issues arise in the choice of a dielectric material in the resonator. Of obvious importance is choosing a material with low losses. This will be explored more in the next sections. The other item which is not so obvious is the tradeoff between velocity and impedance. The dielectric constant sets the velocity of the line and sets the inherent size of the impedance for given dimensions.

A material with a high dielectric constant will have a lower velocity and a lower impedance for a given set of dimensions. On the positive side the low impedance translates into a better driver for the load and the low velocity means a

shorter line to resonate the desired frequency. The shorter line means lower losses related to parasitics, but parasitics will increase as a percentage of the impedance.

A material with a low dielectric constant will have a higher velocity and a higher impedance. On the positive side, the chip will represent a smaller section of the transmission line and so skew will be reduced. On the negative side, the length of the line increases and so the power burnt increases. Since the impedance is higher the parasitics represent a smaller portion of the total.

Generally, a low dielectric constant is desirable in the wings of the chip to reduce the length and therefore losses of the line. Directly under the chip a high dielectric material is needed to reduce skew and improve drive. If a single dielectric must be chosen, balancing these two desires is important.

5.6 Load Capacitance Variation

If the clock load were to vary wildly from cycle to cycle, the resonant circuit might function poorly. A drastically smaller clock load on a particular cycle could cause the voltage on the clock line to spike. For a number of reasons such an effect is not a concern. But first let's explore the primary reason for load variability.

5.6.1 Typical Load

Figure 5.8 shows a few examples of clock loading that can be found in synchronous circuits. On the left appears a domino style "and" gate in which the precharge and evaluate devices present load. At the upper right is a clocked nand gate that creates clock qualified data. Finally at the lower right appears a standard latch whose load is the nmos pass transistor and the inverter.

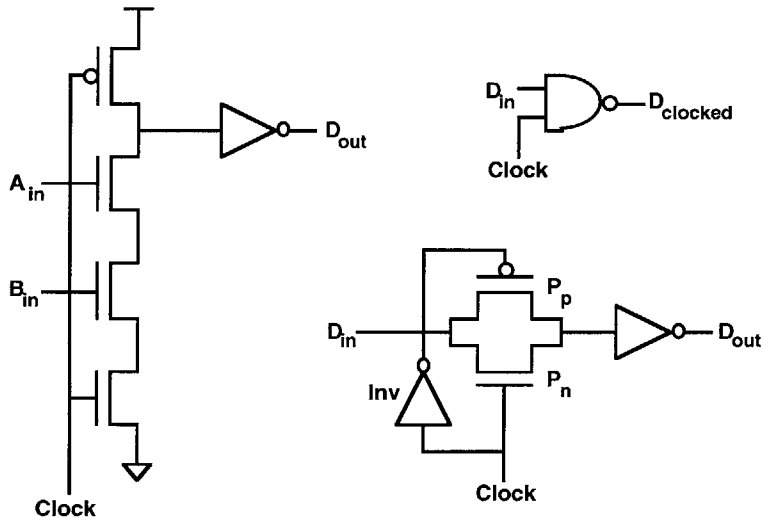

Figure 5.8. Typical Examples of Clock Loads

Let's take a look at the clocked nand gate, upper right. If the D input is low, the output node will not transition. Therefore, the clock capacitance will be dependent on just the gate oxide capacitance. However, if the D input is high, then

the output node will transition in the opposite direction from the clock. The subsequent clock capacitance will be a combination of the gate oxide **and** miller effect.

Note that gate oxide, a constant, will dominate the clock capacitance. The back gate coupling related to data dependence should introduce something on the order of a 17% variation in capacitance from best to worst case. The following table lists data-dependent variations for the common clocked gates based on Spice simulations.

Gate Type	% variation
nand	17%
nor	6%
pass	25 to 35%
dynamic	11%

Table 5.1. % Variation in Capacitance for Clocked Gates

5.6.2 Why data-dependent variability is not a concern

There are three reasons why one should not worry about load variability. First, the data would need to be correlated across the entire chip in order to seriously affect the overall capacitive load. Second, the transmission line capacitance is a significant factor larger than the total load capacitance. Relative to the transmission line capacitance, the data dependent variation of 20% would be reduced to 2 or 3% of the total capacitance. Finally, the drive transistors should ameliorate some of the spike and undershoot presented by the cycle to cycle variation.

Note that this discussion ignores clock gating, a technique that introduces a very large amount of variance in capacitance. Because clock power has been reduced by a large factor, I am assuming that clock gating loses its appeal. If clock gating was combined with a resonant driver, load variability could be a serious issue.

5.7 Physical Variations of Transmission Line

Another possible concern about variation centers on the characteristics of the transmission line. This would include variations in width, spacing, length and dielectric constant between parts of the transmission line and of the entire line from some expected, nominal value. Should the characteristics vary too much, the quality of the resonant waveform might be degraded. Variations in the width, spacing and dielectric constant boil down to variations in the impedance, while the length and dielectric constant variations look like velocity variations.

5.7.1 Impedance Variation

Information for common manufacturing tolerances is hard to come by, but one number bandied about is that, in a particular process, a 50Ω impedance can be expected to vary by no more than 5%. This variability is almost exclusively between a substrate and the expected, nominal value. Within a **particular** substrate the

impedance is more carefully controlled. This means that though the absolute value of an impedance will vary, the relative value between sections of the transmission line will remain constant. Since tuning relies exclusively on relative values, the 5% absolute variation will not affect how the transmission line resonates.

Further, the 5% number is quoted for chip to chip communication. Within a particular substrate, local to the microprocessor chip, the variability will be much lower. Finally, because we are interested in an impedance much lower than 50Ω, the importance of width variations falls significantly. For all these reasons impedance variation of transmission lines should be a secondary concern.

5.7.2 Velocity/Length Variation

On the other hand, variations that affect the velocity of a channel, but not its length, should be considered carefully. The effect of length variation can be safely ignored, because the lithographic tolerances are quite low. For a 2cm section of transmission line, variation of 1 to 2μm amounts to at most 0.01% (2μm/2cm). On the other hand, the dielectric constant accounts for a significant portion of the impedance variation, maybe half of the 5% mentioned earlier. The velocity in the line is dependent on the square root of the dielectric constant, so we can expect variations in velocity of 2.5%. Changes in velocity mean that the phase of a waveform at the location of a discontinuity could change from the expected value.

The best way to correct for any such variation is to use a feedback tuning technique, post-manufacturing trimming or lumped element selection. Fortunately, none of these variations will cause any cycle-to-cycle variation, unlike the data dependent capacitance explored earlier.

6. Conclusion

This chapter presents how this work fits into the wider space of what remains to be done. It begins with the major findings of the thesis, namely how to synthesize resonant cavities for very broad band, periodic signals. Finally, it will conclude by outlining the broad space of things left to be done.

6.1 This Work

Chapter 2 began with the basic of transmission line theory. And in chapter 3 we learned how to tune a transmission line for a desired periodic waveform using impedance discontinuities. This involved two basic equations relating voltage and current across a discontinuity.

$$V_a \cos\left(\frac{2\pi f}{v}x\right) = V_b \cos\left(\frac{2\pi f}{v}x + \Delta\Phi\right)$$

$$\frac{V_a}{Z_a}\sin\left(\frac{2\pi f}{v}x\right) = \frac{V_b}{Z_b}\sin\left(\frac{2\pi f}{v}x + \Delta\Phi\right)$$

We also learned that the tuning process can be simplified by linearizing the phase shift with large discontinuities or by removing it altogether by locating a discontinuity at a voltage or current zero. The end of that section looked at the first application of converting a square wave into a linear ramp waveform.

The end of the chapter laid out the basis for tuning using lumped elements that introduce steps into the voltage and phase. The basic equations describing the voltage and current were modified to handle series and parallel elements.

$$V_a \cos\left(\frac{2\pi f}{v}x\right) = V_b \cos\left(\frac{2\pi f}{v}x + \Delta\Phi\right) + \frac{V_a}{Z}\sin\left(\frac{2\pi f}{v}x\right)\left[L\omega - \frac{1}{C\omega}\right]_{\text{Series}}$$

$$\frac{V_a}{Z}\sin\left(\frac{2\pi f}{v}x\right) = \frac{V_b}{Z}\sin\left(\frac{2\pi f}{v}x + \Delta\Phi\right) + V_a \cos\left(\frac{2\pi f}{v}x\right)\left[\frac{1}{L\omega} - C\omega\right]_{\text{Parallel}}$$

Chapter 4 covered the central application pursued in this thesis: square-wave clock drivers for microprocessors. The choice was made because of the usefulness of the technique for power reduction and the ease with which to generate and resonate the waveforms.

A version of the clock-driver was built at two different frequencies. The 20 MHz mockup provided true verification of the basic principles with waveforms on an oscilloscope. We were able to use a resonant cavity to reduce power consumption and create much cleaner waveforms. But more importantly we showed that when the line was tuned for the desired frequencies, the improvement in waveform quality and power was much more significant. The line with a uniform impedance tuned to the correct length reduced power consumption by a factor of 5.8 relative to

a standard clock driver. And using the impedance tuned line saved a factor of 9.5 over the standard driver.

The other version of the clock driver was a set of Spice simulations at a frequency of 1 GHz. The purpose of these was to show the applicability of the tuning technique at technologically relevant frequencies. From the 1 GHz simulations, we found that a tuned transmission line reduced power by a factor of 4 and improved skew by 30% over the actively-driven clock.

6.2 Future Work

This work has focused on the problem of synthesizing a resonant line for a desired set of frequencies. It began as an attempt to answer the question of what was going on in a transmission line. In essence, figuring out the why's in the analysis problem. As the work progressed, a new idea began to take shape: that of phase and voltage shifts in the resonant standing waves.

Another, possibly more intuitive way to understand the problem is to focus on power instead of voltage and current standing waves. The idea is that the power must be conserved at every point along the system. At a discontinuity the power must be equal on either side. Certainly much of the same theory could be derived by following such a line of reasoning and this approach is worth exploring.

A deeper question that remains open is whether a transform exists to convert from the frequency space into the impedance space. The impedance space is just the impedance as a function of distance. A large portion of my work was oriented towards developing such a transform, and the synthesis technique presented here was as close as I could come. The biggest difficulty with a transform is the broad space of possible waveforms.

It would be rather simple to transform a waveform into an impedance shape, <u>if</u> one could specify a waveform at every point along the line. The problem lies in choosing the desired waveform. Typically a user is concerned only with the voltage and/or current at a few key locations and cares nothing about the waveform in the intervening space. Unfortunately, the user also cares about the simplicity of the line impedance: no impedance can be too large or too small or require fine grain control of impedance. Marrying these two sets of desires from both the impedance and frequency spaces represents the real difficulty in finding a useful transform.

Another area unexplored by this thesis, that may be partly related to finding a transform, is the idea of "continuous" impedance discontinuities. At first this might sound contradictory, but a simple example will illustrate the point. The flare of a trumpet horn is a fabulous method for matching a high impedance, the tube of the horn, to a low impedance, the outside world. Such a discontinuity in impedance does not change suddenly, but changes gradually over distance, hence use of the term "continuous." Incorporating such discontinuities into this theoretical framework, could open this technique up to an even wider range of applications.

Beyond the possible work in the theoretical aspect of impedance tuning, there remains much to be done on the application side. Probably the most interesting is applying the lumped element tuning equations to an active tuning technique. The idea would be to use varactors (variable capacitors) to fine tune a line to the exact

resonance desired. Some method of measuring the activity on the line would be needed, along with some intelligence in altering the line correctly.

Another very interesting application would be to marry this tuning technique to the idea of salphasic distribution of clock signals to distributed loads. [Chi] The power of very low skew distribution coupled with square wave distribution is quite exciting.

A few other secondary issues touched on in this thesis, but not explored in detail are the incorporation of parasitics directly into the model, the hairy chip method of skew reduction and the variability in the system parameters including load capacitance and velocity variability.

I have greatly enjoyed filling out this relatively untouched space of theory and applications and hope that future work in this area will be as fruitful.

Bibliography

Benade, Arthur H. Fundamentals of Musical Acoustics. New York: Dover Publications, 1990. 137, 406-410.

Bowhill and Gronowski. "Practical Implementation Methods and Circuit Examples used on the ALPHA 21164," Proceedings of VLSI Circuits Workshop . June 1996.

Burkhart, Scott and Russel Wilcox. "Arbitrary Pulse Shape Synthesis Via Nonuniform T-line," IEEE Transactions on Microwave Theory and Techniques, Volume 38, Number 10. October 1990. 1514-1518.

Chi, Vernon L. "Salphasic Distribution of Clock Signals for Synchronous Systems" IEEE Transactions on Computers. Version 43, Number 5, May 1994. 597-602.

Collin, Robert E. Foundations for Microwave Engineering. New York: McGraw-Hill, 1966.

Curtins, H. and A. V. Shah. "Step Response of Lossless Nonuniform Transmission Lines with Power-Law Characteristic Impedance Function" IEEE Transactions on Microwave Theory and Techniques, Number 11. November 1985. 1210-1212.

Dhaene, Tom, Luc Martens and Daniel De Zutter. "Transient Simulation of Arbitrary Nonuniform Interconnection Structures Characterized by Scattering Parameters" IEEE Transactions on Circuits and Systems I - Fundamentals Theory and Applications, Volume 39, Number 11. November 1992. 928-937.

Hayden, Leonard A. and Vijai K. Tripathi. "Nonuniformly Coupled Microstrip Transversal Filters for Analog Signal Processing" IEEE Transactions on Microwave Theory and Techniques, Volume 39, Number 1. January 1991. 47-53.

Horowitz, Mark. "Clocking for High Performance Processors," Proceedings of VLSI Circuits Workshop . June 1996.

Koller, J. and W. Athas. "Adiabatic Switching, Low Energy Computing, and the Physics of Storing and Erasing Information", Proceedings of Physics of Computation Workshop. October 1992.

Lee, Thomas, Hirad Samavati, Ali Hajimiri, Arvin Shahani and Gitty Nasserbakht. "Fractal Capacitors". IEEE Journal of Solid State Circuits, Volume 33, Number 12. December 1998. 2035-2041.

Ramo, Simon, John R. Whinnery and Theodore Van Duzer. Fields and Waves in Communication Electronics, Second Edition. New York: John Wiley & Sons, 1984. 210-312.

Reymond, Welles. Standing Sine Wave Clock Bus for Clock Distribution Systems. General DataComm, Inc. Middlebury, CT: US Patent #1993000143442. May 14, 1996.

Schutt-Aine, Jose E. "Transient Analysis of Nonuniform Transmission Lines" IEEE Transactions on Circuits and Systems I - Fundamentals Theory and Applications, Volume 39, Number 5. May 1992. 378-385.

Tran, Thanh T., Clarence Mar, Javier Izquierdo. Sine Wave Clock Distribution with High Voltage Output. Compaq Computer Corp. Houston, TX: US Patent #1992000855453. January 25, 1994.

Younis, Saed G., Thomas Knight. "Resonant Power Supply Techniques for Adiabatic Logic" Symposium on Integrated Systems. Chapel Hill, March 1995.

Younis, Saed G. Asymptotically Zero Energy Computing Using Split-Level Charge Recovery Logic (CMOS). Ph.D. Thesis Massachusetts Institute of Technology, 1994.

A1. Appendix of 1GHz Schematics

The following appendix includes all the schematics for the 1GHz simulations and a brief description. The first section covers the on-chip clock load used throughout the simulations. The next section describes the top level schematic of the standard driver. The third section includes the model of the flip-chip bumps and a model of the transmission line. And the appendix concludes by describing the top level schematic for the tuned transmission line driver.

A1.1 Model of Load

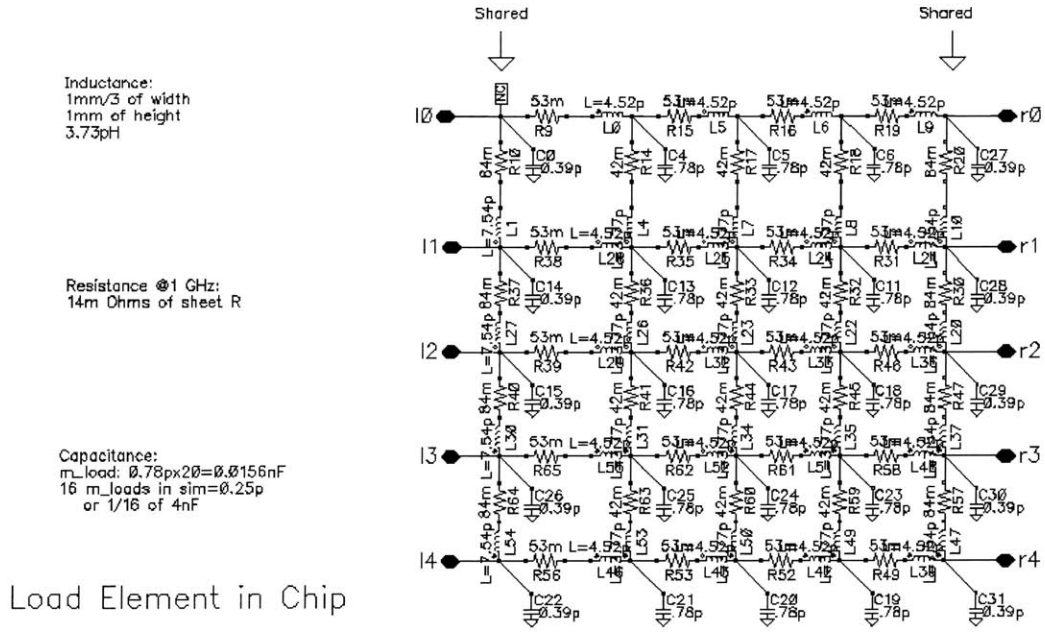

Figure 1.1. Schematic of m_load

The basic element of the clock load, called "m_load", consists of a 5 by 5 array of capacitors connected by a mesh of inductors and resistors. It is meant to represent a 1mm square section of clock load. 16 m_load modules are connected in series to represent one slice of the total chip, called "m_chip". 16 slices would need to be connected in order to create a full chip with a capacitance of 4nF. The simulations

stop at the level of one slice. Therefore, m_chip represents 1/16th of the total load and m_load represents 1/256th of the total load.

The parasitic resistance is calculated relative to a frequency of 1GHz and accounts for the expected width of internal metal that can be utilized to distribute clock, namely 1/3rd. Note that the side elements are shared with the side of the next m_load and so have half (or twice) the value of central elements. The slice allows connections every 1mm along most of the length of the load. The two dimensional nature of m_load does not really affect the simulations, but it begins to give the impression that the clock load is distributed in both dimensions.

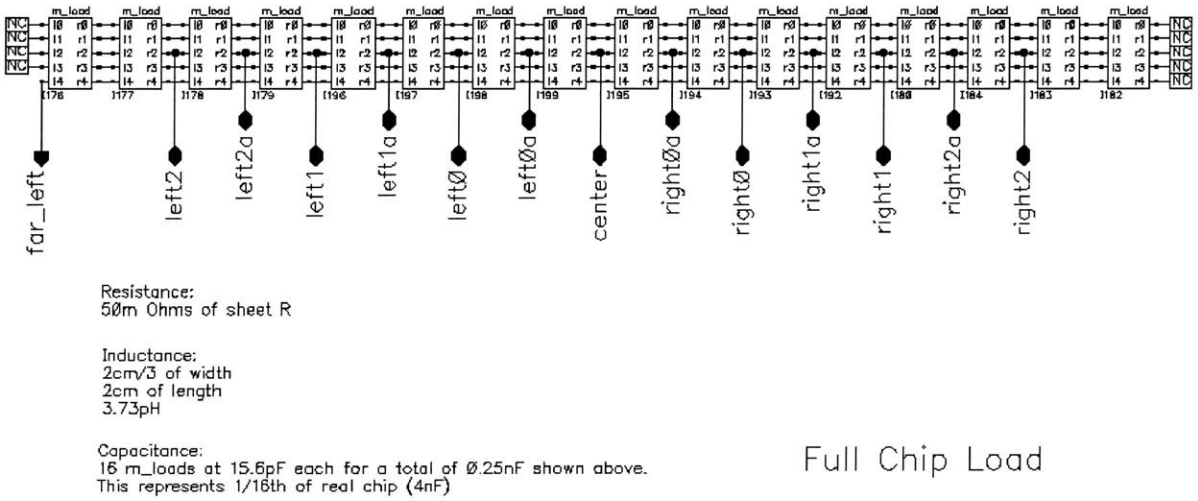

Figure 1.2 Schematic of m_chip

A1.2 Top Level of Standard Driver

The top level of the standard driver is called m_standard. The driver is split with each side connecting 2mm off the center point. Skew is measured between the center and the edge of the slice, "far". The n-device size of the final driver stage is 8mm by 0.24 microns. The beta ratio of the final inverter is 3 to 1 to give roughly equal rise and fall times. The power supplies of the final stage and two pre-driver stages are each connected to a very large capacitance. The power can be calculated from the amount of voltage droop on these nodes.

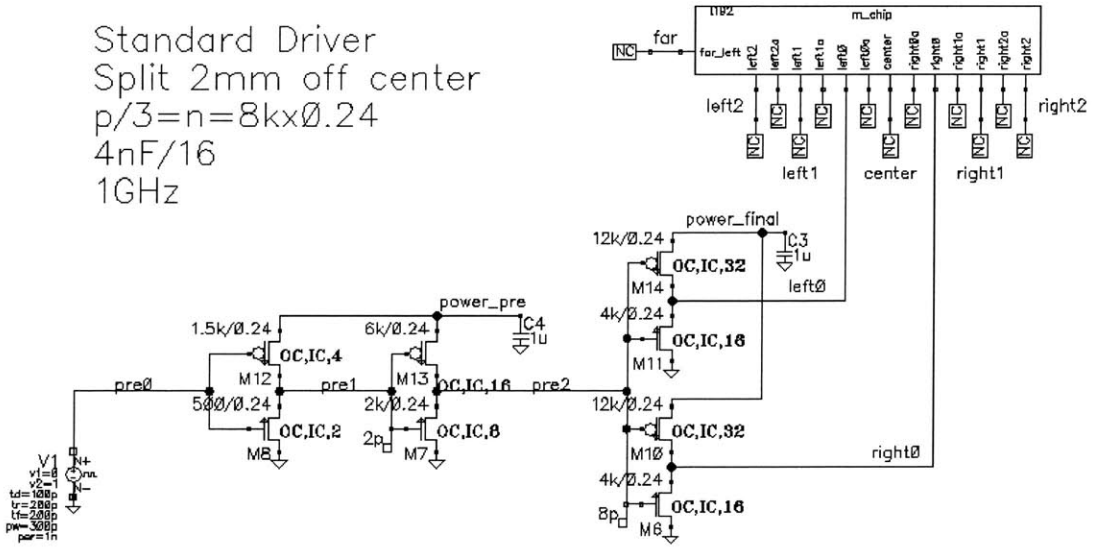

Figure 1.3 Schematic of m_standard

A1.3 Model of Transmission Line

This section includes the model used for the transmission line, m_t1mm. As the name suggests, m_t1mm models a 1mm long section of line with a two stage, RLC ladder. The length is tuned by adding or removing sections. The impedance of the line can be set by changing the parameter, "z". A copy of m_t1mm, m_t1mma, uses "za" instead of "z". Another copy named m_t1mmb uses "zb". These allows different impedances in different sections of the lines. The parasitic resistance is sized relative to an impedance of 8.42Ω which represents the impedance calculated for a line with 1mm of width, dielectric constant of 4 and spacing of 50um that uses horizontal stacking. The inductance and capacitance are directly dependent on the impedance and the velocity.

The second schematic shows the simple model of the flip-chip bumps. Basically they present an inductance of 100pH.

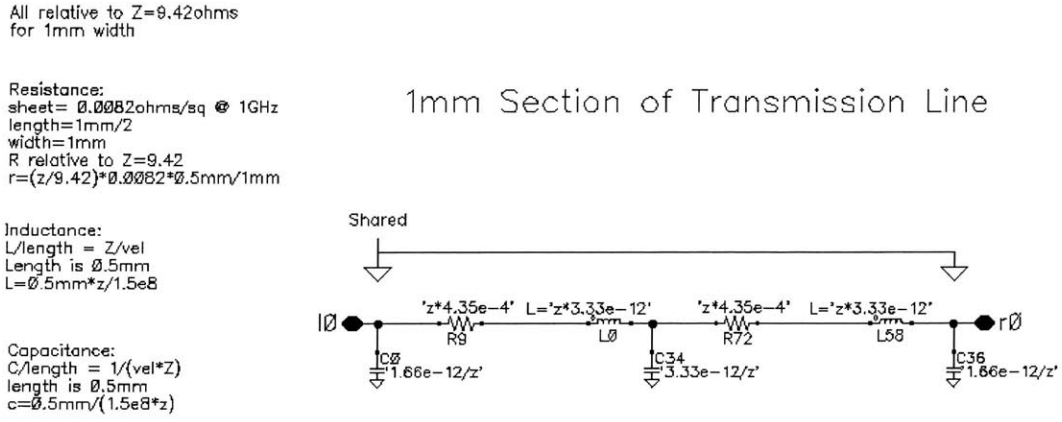

Figure 1.4. Schematic of m_t1mm

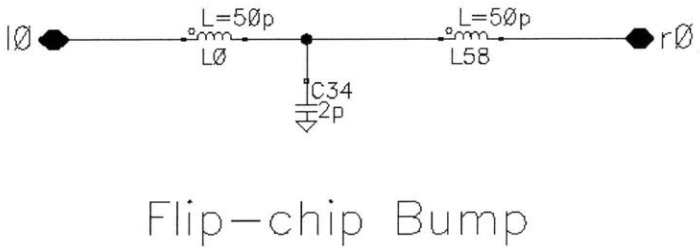

Figure 1.5 Schematic of m_flip

A1.4 Top Level of Tuned Transmission Line Driver

The top level of the tuned transmission line driver is called m_tuned. The driver feeds the center point. The n-device size of the final driver stage is 2.8mm by 0.24 microns. The beta ratio of the final inverter is 3 to 1 to give roughly equal rise and fall times. The power supplies of the final stage and two pre-driver stages are connected to a very large capacitance. The power can be calculated from the amount of voltage droop on these nodes. Skew is measured between the center and the edge of the slice, "far".

The flip-chip bumps connect the center of the chip to the transmission line every 1mm. At the edge of the chip, right2 and left2, the transmission line jumps to the extensions above the clock load, m_load. It flows from the outside in towards the middle. The impedance consists of 2Ω across the middle of the chip and the 36mm extension whose node names are "zn" for the right side and "yn" for the left side. At this point the impedance jumps to 7.25Ω for the remaining 25mm. This would be through the "za" and "ya" sections that are 23mm long and the "zb" and "yb" sections that are 2mm long.

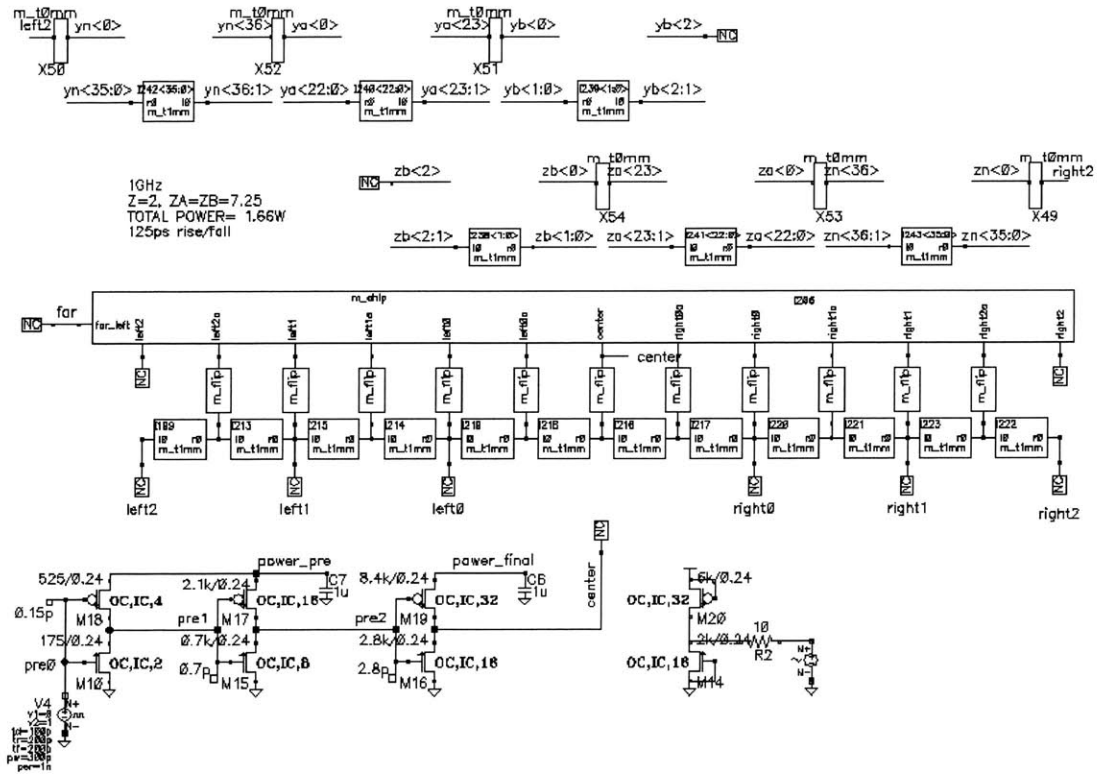

Figure 1.6 Schematic of m_tuned