X-RAY DIFFRACTION TECHNIQUES FOR FUTURE ADVANCED CMOS METROLOGY CHALLENGES

by

Chiu Soon Wong, M.Sc.

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Supervised by

Prof. Patrick J. McNally

Declaration

I hereby certify that this material, which I now submit for assessment on the programme of study leading to the award of Ph.D. is entirely my own work, that I have exercised reasonable care to ensure that the work is original, and does not to the best of my knowledge breach any law of copyright, and has not been taken from the work of others save and to the extent that such work has been cited and acknowledged within the text of my work.

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Abstract

Traditional Si CMOS scaling following Moore's Law is becoming increasingly difficult as physical limits are approached at sub-20 nm nodes and beyond. A significant issue is the limited charge carrier mobility in Si, and so new channel materials that carry relatively higher mobility carriers have been used, such as strained Si. Other materials such as III-V and germanium (Ge) are currently under consideration for replacing the conventional Si channel for future generations of low power and high speed electronics. However, challenges still remain with the realisation of high quality III-V material on Si for CMOS devices fabrication because the tolerance to dislocations is very low ($<10^5$ cm^{-2}). In order to overcome this problem, a non-destructive X-ray characterisation routine which can be used to effectively help III-V growers identify various issues associated with heteroepitaxial growth of III-V materials and which delivers useful experimental feedback to growers for material quality optimisation has been designed. The feasibility of this routine has been demonstrated through the characterisation of a series of deliberately fabricated "problematic" heteroepitaxial GaAs materials.

According to industry experts, the future of modern nanoelectronics may well also depend on a second trend, which is the implementation of diverse functionality within modern ICs. This "More than Moore" (MtM) approach will be realised through the manufacture of complex Systems on Chip (SoC) and Systems in Package (SiP), evolving towards fully three-dimensional ICs (3-D ICs). However, progress in this direction is hampered by the lack of a compelling metrology in order to measure non-destructively and *in situ* the process induced warpage, strain and other defects inside silicon die, a problem which has been highlighted by the International Technology Roadmap for Semiconductors (ITRS). Therefore, the second aim of this thesis has been the development of a novel laboratory-based technique called X-ray diffraction 3-dimensional surface modelling (XRD/3DSM) in order to address this major stumbling block in the development of MtM integrated circuit technology.

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List of Abbreviations

AFM	Atomic force microscopy
APB	Anitphase boundary
APD	Antiphase domain
CMOS	Complementary metal-oxide-semiconductor
CTE	Coefficient of thermal expansion
ELO	Epitaxial lateral overgrowth
FET	Field-effect transistor
FWHM	Full-widths-at-half-maximum
FCC	Face-centred-cubic
FEA	Finite element analysis
GaAs	Gallium arsenide
GaSb	Gallium antimonide
Ge	Germanium
GOF	Goodness-of-fit
HR-XRD	High-resolution X-ray diffraction
IC	Integrated circuit
ITRS	International technology roadmap for semiconductors
InSb	Indium antimonide
InAs	Indium arsenide
IP	Intellectual property
LABR	Large area back reflection topograph
LAT	Large area transmission topograph
LPE	Liquid phase epitaxy
MBE	Molecular beam epitaxy
MCE	Microchannel epitaxy
MM	More Moore

MOVPE	Metalorganic vapour phase epitaxy
MtM	More than Moore
PCB	Printed circuit board
PL	Photoluminescence
QFN	Quad flat no-lead package
QFP	Quad flat package
QW	Quantum-well
RADs	Rocking-curve analysis software
RC	Rocking curve
RF	Radio frequency
RSM	Reciprocal space mapping
Si	Silicon
SiP	System in package
SoC	System on chip
SXRT	Synchrotron X-ray topography
TEM	Transmission electron microscopy
UQFN	Ultra-thin quad flat no-lead package
μ-Raman	Micro-Raman
XRD	X-ray diffraction
XRD/3DSM	X-ray diffraction 3-dimensional surface modeling
2D	2-Dimensional
3D	3-Dimensional

Chapter 1

Introduction

1.1 Complementary metal-oxide-semiconductor (CMOS) field-effect transistor (FET) scaling

Since the early 1970s, the dimensions of CMOS transistors have been aggressively downscaled, successfully enhancing the performance of transistors by about 30-35% for each new generation of CMOS technology. This Si CMOS scaling is described by Moore's law [1-5], where transistor size shrunk at the rate of ~0.7x for each generation, down to the technology node of 130 nm. The traditional scaling process has apparently slowed down as it reached the 90 nm CMOS generation node [1-5], largely due to issues with the gate dielectric (silicon dioxide, SiO_2) becoming physically too thin. The restriction on the SiO_2 thickness approached the 1.2 nm limit as illustrated in Fig. 1.1. Reducing the oxide thickness more would mean a prohibitively large gate leakage current arises as a consequence of the direct tunnelling across the relatively thin gate oxide [4, 6].

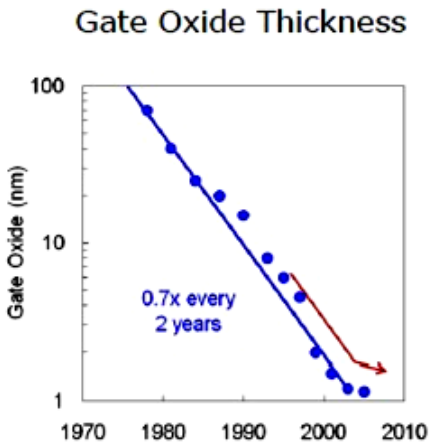


Figure 1.1 Gate oxide thickness scaling. Traditional scaling slackened at the 90 nm technology node [4].

In 2007, Intel announced the first 45nm generation of transistor technology by introducing a revolutionary high-k metal-gate transistor in cooperation with strained Si technology. This new technology improved the performance of the device by approximately 23 % compared to the 65 nm node [2, 4]. The significant improvement is due to the use of a high-k gate that enabled a >25x gate leakage reduction, in addition to mobility advantages offered by strained Si [4]. If Moore's law continues, it will need further new materials as substitutes for the existing solutions. Overall, the CMOS technology has been through a revolutionary change after the 130 nm node as more chemical elements have been introduced in order to drive the CMOS roadmap forward (see Fig. 1.2), and this is likely to continue in future CMOS technologies [7].

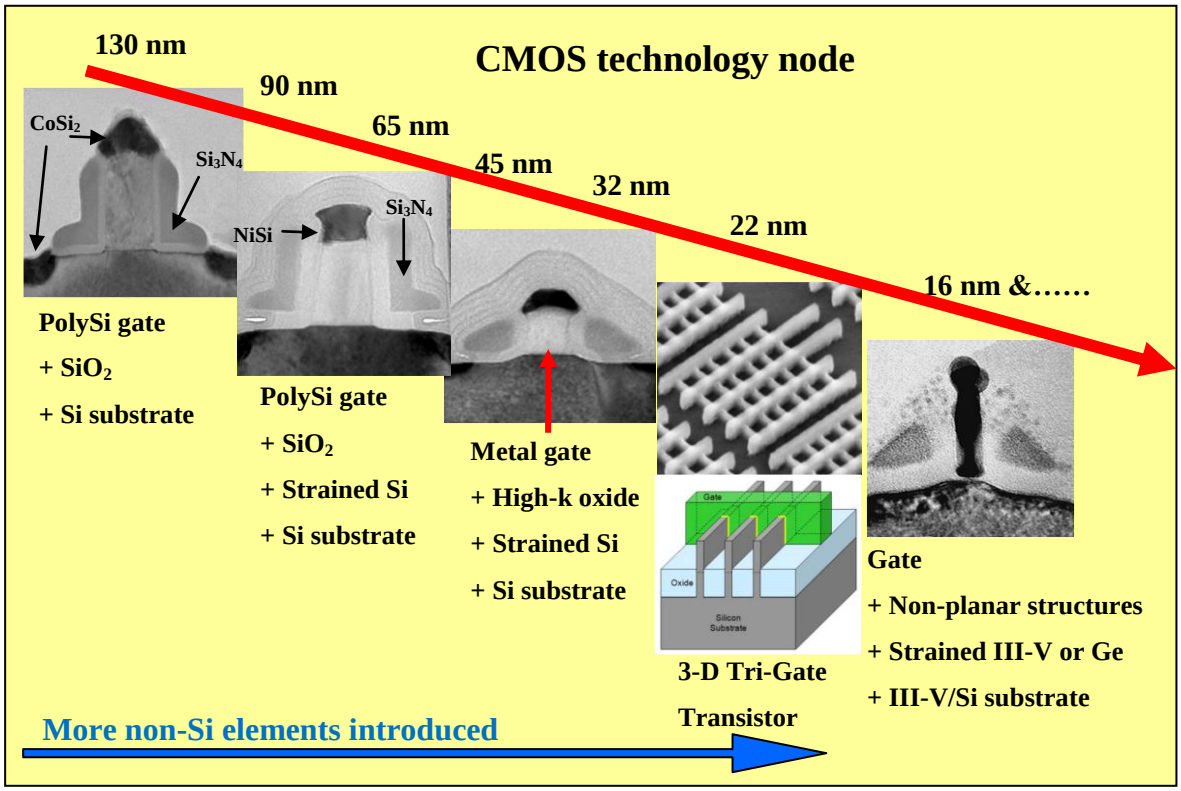


Figure 1.2 The evolution of CMOS technology after the 130 nm technology node [4, 7] (the options for future technologies are subject to change).

1.1.1 Moving towards "More Moore" and "More than Moore" technologies

"More Moore"

Looking towards future CMOS technology nodes such as the 16 nm node and beyond, the existing technology is insufficient to drive the CMOS roadmap due again to the limited channel mobility in Si MOS devices [8, 9] (see Fig. 1.2). One of the obvious remedies that has been consistently pointed out by the International Technology Roadmap for Semiconductors (ITRS) 2009-2011[8, 9], is to replace the conventional Si or strained Si CMOS channel with alternative materials offering a higher mobility than Si. Channel materials being proposed are Ge and III-V materials [8-11]. Considering the high electron mobility exhibited by III-V materials compared to Si, these materials are amongst the best alternative channel materials to bring about the mobility improvement for n-MOSFETs. In addition, III-V materials have remarkable optical properties: the III-V direct band gap allows a more efficient photon creation/conversion than in Si. Therefore, more functionality (optoelectronic devices) can be added to conventional logic functions on the same Si platform. Fig. 1.3 shows a plot of carrier mobility as a function of energy band gap for numerous semiconductor materials [8]. III-V compound semiconductors such as indium antimonide (InSb), indium arsenide (InAs), gallium antimonide (GaSb) and gallium arsenide (GaAs) possess comparatively higher electron mobility than that of Si. Although InSb and InAs possess the highest electron mobility, they are not the ideal choice of n-channel materials because of their narrow energy band gaps, as they are more susceptible to thermal generation of excess carriers, thus resulting in current leakage [8]. By forming the III-V ternary semiconductors (i.e. InGaAs, InAsSb and InGaSb), one can avail of a wide selection of composition and energy band gap for n-channel FET applications while simultaneously maintaining their superior electron mobility. In particular, a very high-speed InGaAs quantum-well (QW) transistor has been demonstrated at an operating voltage of only 0.5 V

[12, 13]. These have made III-V materials a promising material choice for future high-speed logic applications as they give rise to high transistor drive current in addition to ensuring low gate delay.

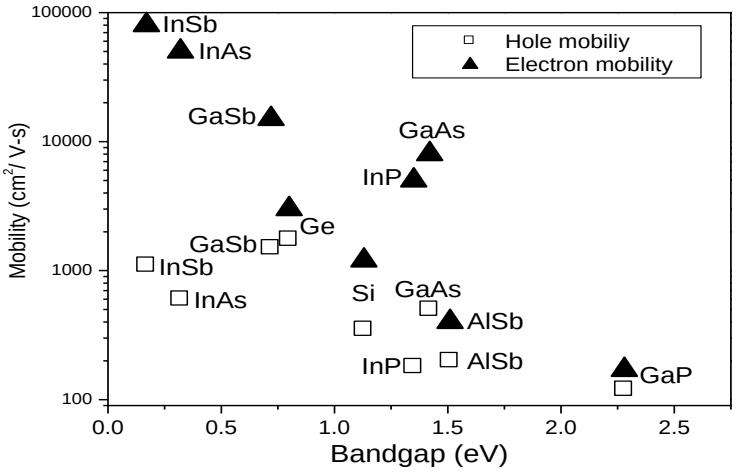


Figure 1.3 Carrier mobility as a function of minimum energy band gap for elemental and III-V compound semiconductors [8].

Considering the materials for the p-type channel, both III-Vs (such as InGaAs, InSb, InGaSb, GaAs) and Ge are the primary candidates as they offer significantly higher hole mobility than that of Si [8]. Although, most III-V materials are superior in electron mobility, they are not significantly better in terms of hole mobility. This has been one of the crucial obstacles to be encountered, when identifying a suitable high mobility III-V p-FET candidate in order to balance the mobility between p-and n-channel FETs [14]. Nevertheless, recent works have demonstrated one solution by incorporating strain as a mobility enhancer for both the Ge [15] and III-V materials such as InGaAs and GaSb [16, 17] for p-channel FET applications. That suggests it is possible to further improve the hole mobility of Ge and III-V materials by straining them, but it is yet to be thoroughly investigated.

A fundamental requirement for integrating the III-V materials into the channel of a silicon based MOSFET (i.e. onto a silicon substrate), is to produce a suitable platform. Hetero-integration of III-V materials presents several very difficult technological challenges. The key challenge lies in the significant lattice mismatch between the Si substrate and the III-V over-layers, since there is a 4.1% mismatch between Si and GaAs. Large numbers of defects (misfit and threading dislocations) are generated in the epitaxial layers due to the large lattice mismatch [18, 19].

Different growth strategies have been explored to overcome the materials issues associated with GaAs heteroepitaxy on Si. The use of strained or composition-graded buffer layers in combination with thermal annealing have been thoroughly investigated, but the high cost associated with the growth of thick GaAs epilayers and the propagation of dislocations into the active areas of the devices during annealing have hindered its implementation in production [20-22]. Low-temperature growth of GaAs on Si using atomic hydrogen as a surfactant has been shown to reduce significantly the average defect density (10^4 cm^{-2}) and enhance the electrical properties of the as-grown film by bending and pinning threading dislocations via modification of the surface energy and growth dynamics. While the relaxation of the lattice mismatch in the early stages of growth is very efficient using this method, it has as the main drawback of poor thermal stability of the resulting GaAs epilayers [23, 24]. One of the most promising alternatives is selective growth of GaAs on patterned Si substrates, also called epitaxial lateral overgrowth (ELO) or microchannel epitaxy (MCE) [25-28]. In this case the silicon substrate is masked with a thin dielectric film and subsequently patterned using lithographic techniques with micron or nanomet scale resolution. Selective nucleation of GaAs in the mask-free Si areas enables lattice mismatch dislocations to be trapped by the mask vertical sidewalls provided the aspect ratio of the opening is sufficiently large. Improvements in defectivity are required as there is an immense

challenge in using III-V material on Si to fabricate CMOS devices because the tolerance to dislocations is very low ($<10^5$ cm^{-2}).

The new materials and device architectures in development, such as hetero-integration of III-V on Si will ultimately provide a route that push CMOS technology scaling forward [4, 9-11]. The extension of CMOS scaling using non-Si materials channels for future high speed and low power logic transistor is labelled by the ITRS as the "More Moore" (MM) approach. However, the most critical issue still remains, i.e. the realisation of high quality III-V materials on Si substrates.

"More than Moore"

Recently, a second trend called "More than Moore" (MtM) is defined by industry experts, where added value to devices is provided by incorporating functionalities that do not necessarily scale according to Moore's Law [29, 30]. One MtM approach enables the migration of the non-digital components from the printed circuit board (PCB) into a single package containing the integrated circuit (IC). System on chip (SoC), System in Package (SiP) and 3-dimensional (3D) IC technologies provide such a route for the continued improvement in chip performance, with reduced power, cost and size at the system level while the new materials and architectures that can support Moore's Law scaling, are not yet ready [4, 30].

SoC refers to integrating all components of a computer or other electronic system on one silicon platform horizontally (chip), as shown in Fig. 1.4. It may consist of analogue, radio frequency (RF), power sensors as well as passives components to expand the functions/value of the semiconductor chips [29, 31]. This technology not only helps to satisfy the ever-increasing demands for high processing performance, but at the same time ensures a

slim form factor and lower overall power consumption. Nonetheless, the implementation of SoC technology is hampered by the long design times due to integration complexities, high wafer fabrication costs, test costs, and mixed-signal processing complexities requiring dozens of mask steps and intellectual property (IP) issues [31, 32].

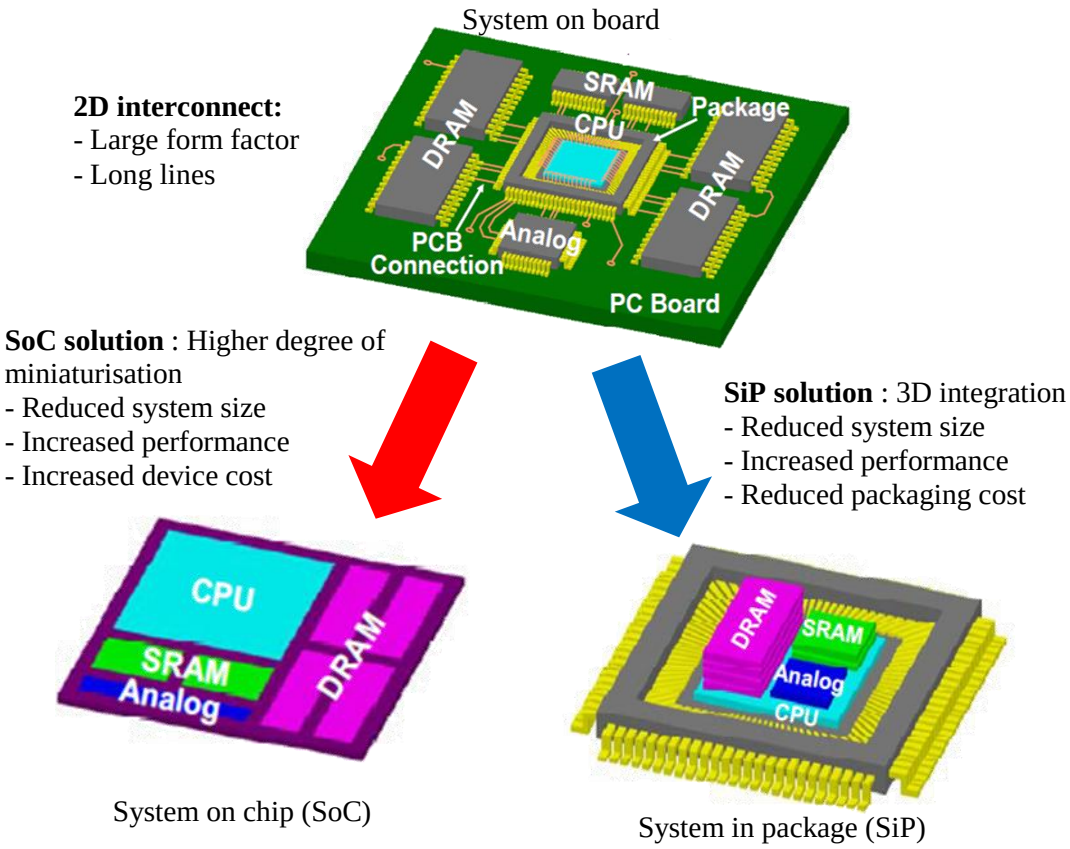


Figure 1.4 The concept of SoC and SiP: migration from the system board level onto the chip (SoC) or into the package (SiP) [9, 33].

Therefore, a new paradigm called system-in-package (SiP) is being innovated to overcome the shortcoming of the SoC approach. This is due mainly to the capabilities of SiP to integrate several either already existing, and/or dedicated dies, together to create a new function without having to pay for long product development times and very expensive mask

sets [31, 32]. These materials, technologies and functional components on different dies can be connected in 3-dimensions by vertically stacking each layer one on top of another in the same package (see Fig. 1.4), enabling the continued increase in functional density and decrease in cost per function required to maintain the progress in cost and performance for electronics, such as for mobile communications markets [9, 32].

The core innovation of SiP technology is not for the replacement of SoC technology, but it is in fact the heterogeneous integration of digital and non-digital functionalities into compact systems as illustrated in Fig. 1.5 [29]. This is particularly important for future multifunctional systems as they will require not only more signal and data processing power, but also require the interaction with the outside world via an appropriate transducer, such as sensors and actuators. This implies that future highly integrated systems (advanced SoC/SiP systems) will comprise of both SoC ("More Moore") and SiP ("More than Moore") components in which SoC components may be viewed as the brain of an intelligent compact system, whereas SiP components will be responsible for interaction with the outside world and users (see Fig. 1.6) [9, 29].

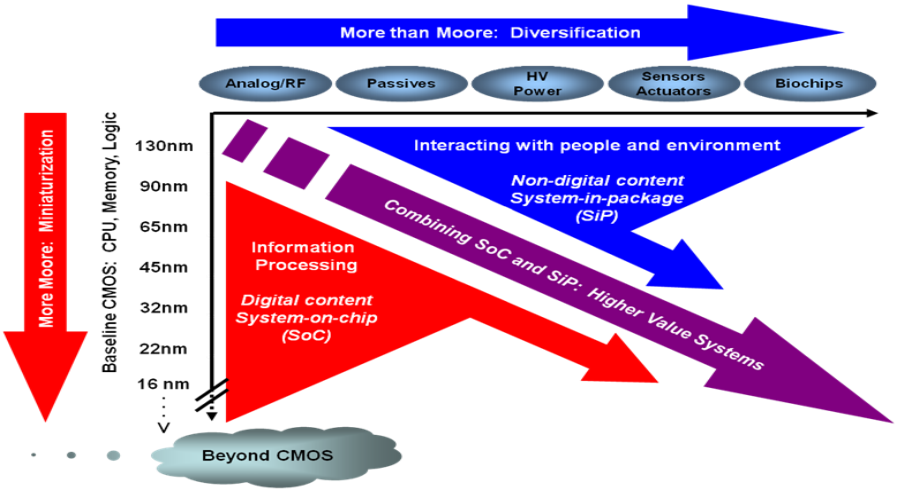


Figure 1.5 The combined need for digital and non-digital functionalities in an integrated system is translated as a dual trend in the ITRS: miniaturisation of the digital functions ("More Moore") and functional diversification ("More than Moore") [29].

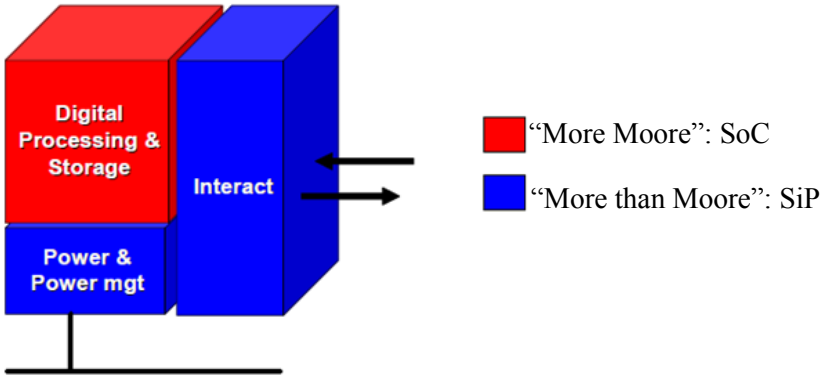


Figure 1.6 "More than Moore" technologies complement the digital processing and storage elements of an integrated system in allowing the interaction with the outside world and in powering the system [9, 29].

The existing SoC/SiP systems are however plagued by reliability problems as they are not as reliable as traditionally packaged integrated circuit systems. Issues such as electrical, thermal and mechanical stress management are the primary concerns in order to meet the future integration requirements of advanced SoC/SiP systems[32, 34]. Manufacturing-induced thermal stress, created during the fabrication of packaged integrated circuits, can be large enough to induce cracking or interfacial delamination in the package, which could potentially degrade the performance and reliability of the packaged chip, ultimately leading to device failure. However, there are no available laboratory based metrologies that can non-destructively measure or image stress/strain, warpage inside packaged chips or SoC/SiP packages. Therefore, the need to develop non-destructive metrologies that can be used to effectively measure stress/strain in packaged chips or SoC/SiP systems is identified by the ITRS, in both the 2011 and 2009 editions [35, 36]. These non-destructive measurement methodologies will be used to gain a better understanding of the sources and distribution of strain inside the packaged chips or SoC/SiP systems, created

during different packaging or manufacturing processes, and thereby helping to improve the manufacturing efficiency, performance and reliability of advanced packaging products.

1.2 Scope of this thesis

Concerning further miniaturisation by "MM" solutions, one of the obvious tasks is the replacement of the Si channel by III-V materials, where the most critical issue is the realisation of high quality hetero-integration of III-V materials lattice matched to Si substrates.

In order to circumvent these problems, it is important to understand and identify the sources of defect/strain generation. Through the selection of appropriate characterisation methodologies, I aim to achieve the following technological objective:

1) Design a non-destructive X-ray characterisation routine that can be used to effectively identify various issues associated with heteroepitaxial growth of III-V materials, and delivers useful experimental feedback to growers for material quality optimisation.

Although "MtM" technology provides an alternative route, which enables continued rapid progress in functional density during a period where traditional CMOS scaling cannot keep pace and new architectures are not ready, it is still plagued by reliability issues that need to be addressed in order in improve the efficiency of the existing packaging products. Therefore a second aim in this thesis is as follows:

2) Development and implementation of a novel technique for non-destructive analysis of manufacturing process-induced stress/warpage inside completely encapsulated packaged chip

1.3 Characterisation methodology

i) Characterisation of heteroepitaxial growth of III-V materials

The most common problems that have to be encountered during the hetero-integration of III-V materials lattice matched to Si substrates have been anti-phase domains, dislocations, strain and lattice tilts distributed within the III-V layers due to their crystal dissimilarities. These factors mean that abundant extended defect densities ($>10^8$ cm^{-2}) are generated in the III-V epitaxial layers when directly grown on Si substrates. The selection of appropriate characterisation techniques is an essential first step to identify significant effects of each growth step (i.e. growth and annealing temperatures, III/V flux ratios and layer thickness), towards the production of low defect density heteroepitaxial of III-V materials.

An X-ray characterisation routine that can be used to effectively help III-V growers in tackling the aforementioned problems was designed, as summarised in Fig. 1.7. This routine was planned using mainly X-ray diffraction techniques such as conventional X-ray diffraction (XRD) and high-resolution XRD (HR-XRD) performed at Dublin City University (DCU) by me and synchrotron X-ray topography (SXRT) performed at HASYLAB. It is to examine specimens using a range of essentially non-destructive methods; this is because often one characterisation technique alone cannot reveal all the desired characteristics of the specimens under test. Likewise, many preferred techniques are destructive in nature – either during the measurement itself or prior to the measurement, during sample preparation. When one uses non-destructive methods, it allows the same specimen to be measured a number of times in order to obtain comprehensive information. Apart from X-ray techniques, I have also employed optical techniques such as micro-Raman spectroscopy, and photoluminescence spectroscopy to characterise the surface quality of the specimen. Other measurements such as atomic force microscopy (AFM) and transmission electron microscopy (TEM) were provided by collaborators from Instituto de Ciencia de Materiales de Madrid (ICMM-CSIC) and

IMDEA Materials, Madrid, Spain, respectively. These measurements served the purpose of complementing the analysis of my own results.

In order to demonstrate the capability of this X-ray characterisation routine in identifying the existence/generation of different defects associated with heteroepitaxial growth as well as in identifying the significant effects of each growth process, I have implemented this routine to characterise a series of deliberately fabricated heteroepitaxial GaAs materials with different defects (antiphase domains, dislocations, strain/relation, lattice tilts). These 'problematic' GaAs materials were deposited on Ge and Si substrates by altering the growth parameters, which will be explained in more detail in Chapter 4. In this work all the materials were grown and provided by collaborators from Instituto de Ciencia de Materiales de Madrid (ICMM-CSIC), Spain.

ii) Lab-based X-ray diffraction 3-dimensional surface modelling (XRD/3DSM)

As the reader will subsequently see, XRD-3DSM is a novel technique for non-destructive analysis of strain/warpage inside completely encapsulated packaged chips. Originally developed by DCU Researchers using synchrotron sources [37, 38]. It was developed using XRD techniques, utilising a laboratory-based a triple-axis Jordan Valley D1 X-ray diffractometer at DCU. Maps are produced of the entire Si die inside a packaged chip, which reveal warpage via mapping of rocking curve full-widths-at-half-maximum (FWHM) as a function of position across encapsulated packages. SXRT is used to validate data obtained from XRD/3DSM. More details of the technique will be explained in Chapter 5.

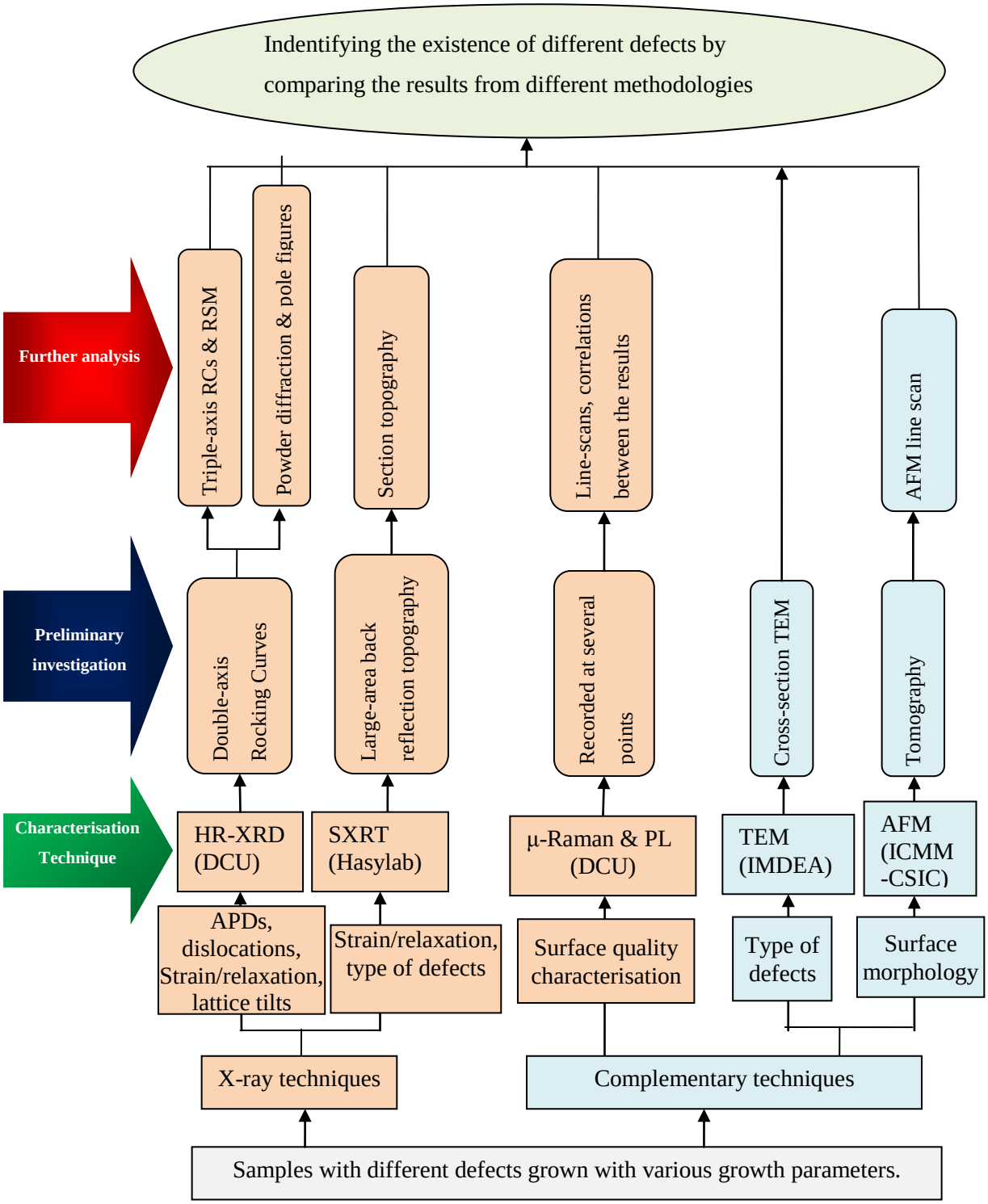


Figure 1.7 The work flow of the characterisation methodology used for analysing the quality of heteroepitaxially grown III-V materials. Acronyms are defined in the text.

1.4 Report Layout

This report is structured into a number of chapters, organised as described by the chart in Fig. 1.8. Chapter 2 describes the fundamentals of the characterisation methodology and the instrumental setup. Chapter 3 discusses the major barriers that hamper the heteroepitaxy of GaAs on non-polar substrates and the challenges encountered in growing high quality GaAs layers by ELO on nanostructured-oxide substrates. Chapter 4 gives a brief discussion regarding the growth of GaAs samples and reviews the charactersation of heteroepitaxial growth of GaAs samples using the X-ray charactersation routine shown in Fig. 1.7. More specifically, the implementation of distinct approaches in identifying various issues associated with heteroepitaxial growth will be discussed. Chapter 5 reviews briefly the evolution of IC packaging technology and the development and implementation of XRD/3DSM for non-destructive analysis of die stress inside packaged chips. Chapters 6 and 7 demonstrate the feasibility of the XRD/3DSM technique for chateracterisation of die stress inside fully encapsulated packaged chips. Finally, Chapter 8 covers the conclusions from this research and outlines future work.

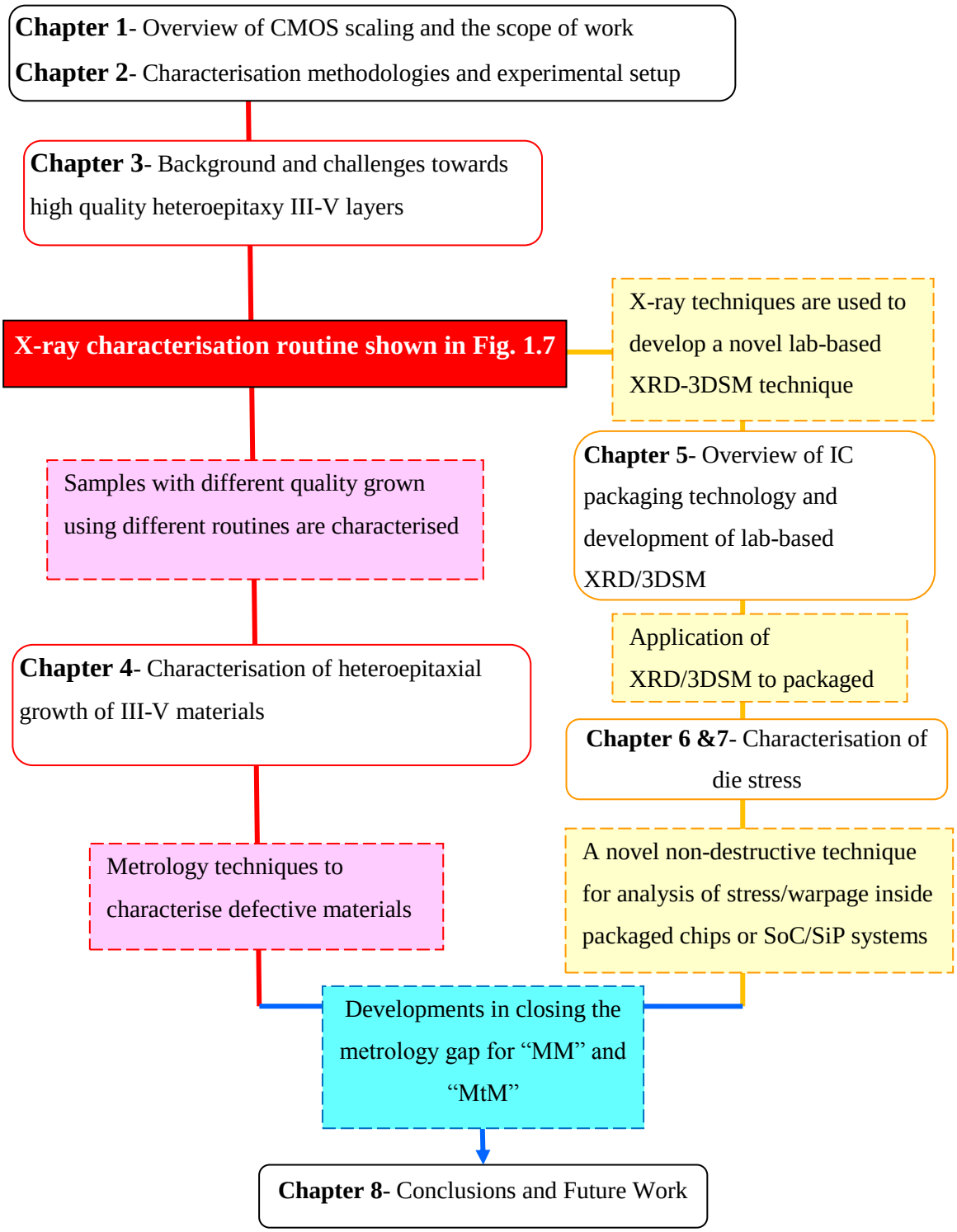


Figure 1.8. Chart showing the organisation of this thesis.

Chapter 2

Characterisation Methodology and Instrumental Setup

2.1 Introduction

The selection of appropriate characterisation methodologies is vital for analysing and comprehending the source of defects and strain generation and their influence on the properties of semiconductor materials. This chapter has the preliminary aim of introducing the fundamental and instrumental setup of numerous characterisation techniques that have been selected for this work.

2.2 X-Ray diffraction (XRD)

X-Ray diffraction is a non-destructive analytical methodology which can provide information about the chemical composition and crystallographic structure of natural and manufactured materials. It is used extensively for quality control of production, especially in research and development applications.

2.2.1 Fundamentals of X-ray diffraction

In 1911, the phenomenon of X-ray diffraction (XRD) in crystalline materials was discovered by von Laue, Friedrich and Knipping in rock salt [39]. In the following year, 1912, W. L. Bragg confirmed that crystal diffraction is associated with a set of evenly spaced sheets typically running through centres of the atoms of the crystal lattice, as depicted in Fig. 2.1. The scattered X-rays from adjacent planes will add up constructively and generate a strong diffraction. This, however, only occurs under specific circumstances, namely when [40]:

$$n\lambda = 2dsin\theta \qquad (2.1)$$

where n is an integer representing the order of diffraction, λ is the wavelength, d is the interplanar spacing of the diffracting planes and θ is the angle between the incident beam and the diffracted beam relative to the reflecting plane. That said, reflection occurs when the following criteria are satisfied [40]:

i) the angle of incidence is equivalent to the diffracted angle ,

ii) the path-length difference ($AO+AB$ or $dsin\theta + dsin\theta$) is equal to an integer multiple of the X- ray wavelength ($n\lambda$).

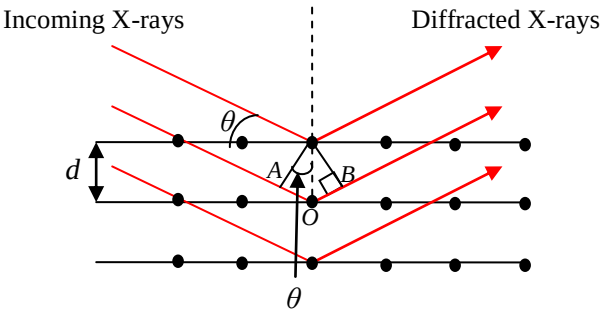


Figure 2.1 Schematic diagram of Bragg diffraction.

2.2.2 Diffraction in reciprocal space

An ideal crystal is built up of molecules arranged on a regular 3-dimensional crystal lattice. A crystal lattice can be explained as a periodic arrangement of molecules in a regular pattern in the crystal. The basic building block for the crystal lattice is known as the unit cell. The length of the unit cell along the three crystallographic axes x, y and z directions are defined as a, b and c, as shown in Fig. 2.2. In real space, any direction in a crystal can be specified using a lattice vector ($\boldsymbol{r}$) and can be written as [41]:

$$\boldsymbol{r} = u\boldsymbol{a} + v\boldsymbol{b} + w\boldsymbol{c} \qquad (2.2)$$

where *u*, *v* and *w* are integers that specify the direction and ***a***, ***b*** and ***c*** are the unit cell vectors describing the lattice, as shown in Fig. 2.2.

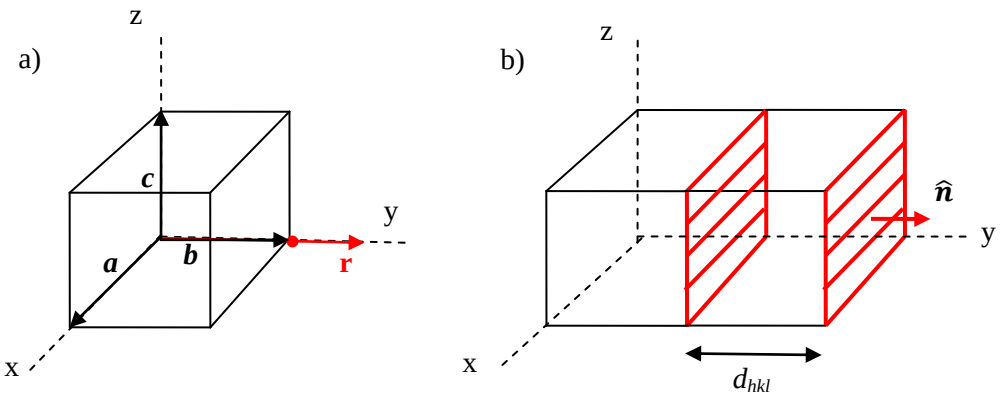


Figure 2.2 Schematic diagrams illustrating a unit cell in real space, a) a direction in a crystal represented by a vector (***r***), and b) a direction of a set of parallel crystal planes (*hkl*) defined by their normal vector ($\hat{\boldsymbol{n}}$) and interplanar spacing (d_{hkl}) [41, 42].

When one considers X-ray diffraction, it is always easier to describe the structure of a crystal in terms of families of planes (*hkl*). This is because X-ray diffraction occurs from different sets of crystals with different reflection planes (*hkl*) and interplanar spacings (d_{hkl}) at different angles, as previously described using Bragg's law. A set of parallel crystal planes (*hkl*), can be characterised by its normal vector ($\hat{\boldsymbol{n}}$) and interplanar spacing (d_{hkl}) [41], as shown in Fig. 2.2b). By using these two quantities, each set of parallel crystal planes (*hkl*) can be represented by a single point in reciprocal space, in which each reciprocal lattice point is defined by a reciprocal lattice vector ($\boldsymbol{g}_{hkl}$). The $\boldsymbol{g}_{hkl}$ is always parallel to $\hat{\boldsymbol{n}}$ of the crystal plane (*hkl*) in cubic crystals, and they are related by [41]

$$\boldsymbol{g}_{hkl} = \frac{1}{d_{hkl}}\hat{\boldsymbol{n}} \tag{2.3}$$

where $|\boldsymbol{g_{hkl}}| = \frac{1}{d_{hkl}}$ is the distance of the reciprocal lattice point from the lattice origin. An example of a 2-dimensional reciprocal lattice of GaAs is depicted in Fig. 2.3 [43]. By way of example, a line drawn from the origin of the reciprocal lattice (typically taken to be a reciprocal lattice point itself) to another point is a reciprocal lattice vector ($\boldsymbol{g_{hkl}}$).

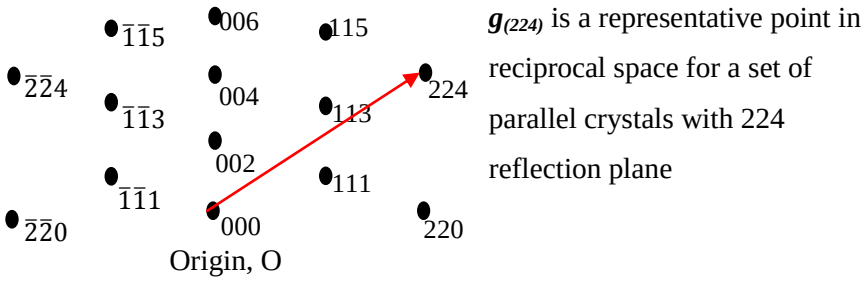


Figure 2.3 Two-dimensional reciprocal lattice for zincblende GaAs [43].

The X-ray diffraction in reciprocal space can be further explained using a geometrical construct called the Ewald sphere, as illustrated in Fig. 2.4. The Ewald sphere is centred on a line representing the X-ray beam direction, and it has a radius of $1/\lambda$ [41]. The reciprocal lattice has its origin at the point where the X-ray beam exits the Ewald sphere. The crystal rotation around the centre of the sphere is equivalent to the rotation of the reciprocal lattice about its origin. A strong diffraction from a crystal with reflection planes (*hkl*) will occur when the corresponding reciprocal lattice point (*hkl*) lies exactly on the circumference of the Ewald sphere [41].

As shown in Fig. 2.4, k_i and k_d represent the wavevectors along the directions of the incident, and diffracted beams, respectively. The scattering vector $\boldsymbol{Q}$ is equivalent to the difference between the diffracted and incident ($\boldsymbol{Q} = \boldsymbol{k_d} - \boldsymbol{k_i}$) wavevectors. This is the condition at which it satisfies Bragg's law and diffraction occurs [41, 44]. This can be shown through the following relationship obtained from the Ewald sphere shown in Fig. 2.4,

$$Sin\theta = \frac{|\boldsymbol{Q}|/2}{1/\lambda} \tag{2.4}$$

For a crystal with reflection planes of *(hkl)* which satisfy Bragg's law, the reciprocal lattice vector ($\boldsymbol{g_{hkl}}$) is identical to the scattering vector ($\boldsymbol{Q}$) [41, 44]. Therefore, the modulus of $\boldsymbol{Q}$, i.e. $|\boldsymbol{Q}|$ is equal to $|\boldsymbol{g_{hkl}}|$ and it is simply $1/d_{hkl}$ in real space, obtained from Eq. 2.3. Substituting $|\boldsymbol{Q}|$ into Eq. 2.4, one can obtain a relationship which is equivalent to Bragg's law,

$$Sin\theta = \frac{\lambda}{2d_{hkl}} \tag{2.5}$$

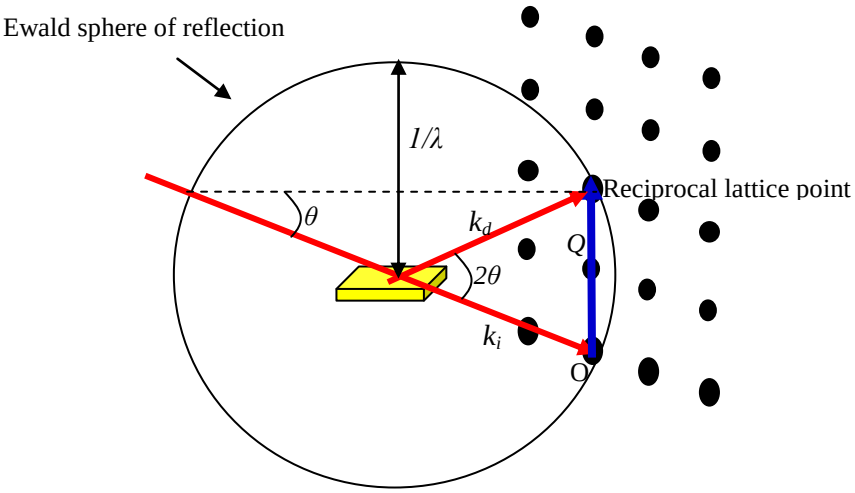


Figure 2.4 Ewald sphere construction illustrating the diffraction X-ray occurs in reciprocal space [41].

2.3 Powder X-ray diffraction (XRD)

This technique is used to characterise micro- or poly-crystalline samples in order to ascertain the crystallographic structure, average crystallite sizes, and the preferred orientation

(texture) in the polycrystalline samples. An unknown substance can be identified from its diffraction pattern, as each individual substance possesses a distinctive diffraction pattern. This can be done by comparing the experimental diffracted pattern against a Powder Diffraction File (PDF) – comprising of data on interplanar spacings *(d)* and relative intensities *(I)* complied for crystalline materials - maintained by the International Centre for Diffraction Data (ICDD) [45]. A powder XRD spectrum can be collected by setting the sample and detector angles together in a *2:1* ratio, which will be explained further in subsequent sections.

One of the most useful features of XRD is its ability to determine the crystallinity of substances. The diffraction pattern of a crystalline material comprises a series of sharp peaks, which are distinguishable from the broad and weak intensity peaks produced by amorphous material. Through the line broadening of the peak, the average crystallite size is computable via the Scherrer equation [41],

$$t \approx \frac{0.9\lambda}{\beta cos\theta} \tag{2.6}$$

where t is the calculated average crystallite size, λ is the wavelength of the X-ray source used, $\beta = \beta_{measured} - \beta_{machine}$ is the full width at half maximum (FWHM) of the diffracted peak in radians (corrected for any instrumentally induced line broadening) and θ is the Bragg diffraction angle of the peak.

2.3.1 Crystallographic texture mapping

A polycrystalline sample might typically comprise of a number of randomly distributed grain orientations and some of these grain orientations might tend to cluster about a preferred orientation. These are known as non-textured and textured materials, respectively.

A pole figure is the stereographic projection mainly used to graphically illustrate the distribution of grain orientations of a polycrystalline material. It can be plotted by recording the conventional powder diffraction *2θ-ω* scans for all rotations (phi, ϕ = 0 - 360 °) and tilts (chi, ψ = 0 - 90 °) of the sample, in order to collect the intensity distribution throughout all reciprocal space [41, 44]. A single *2θ-ω* scan can be recorded by setting the sample and detector angles together in a *2:1* ratio, shown in Fig. 2.5 (a). In this experimental geometry, the scan always moves along the direction normal to the sample surface, and thus, collects only the 'out-of-plane' lattice constant information for a crystalline material. In other words, a *2θ-ω* scan only collects information on grains with Bragg planes parallel to the film plane [41, 44], while a pole figure is a combination of a series of *2θ-ω* scans recorded for different tilts against the X-ray incident beam incidence plane and rotated around the sample normal in order to get all grains in a diffracting position. Therefore, it captures the intensity distribution throughout all of reciprocal space over the surface of a hemisphere with a radius of, $1/\lambda$ (see Fig. 2.5b) [41, 44]. For a crystal with reflection planes of *(hkl)* which satisfy Bragg's law, the reciprocal lattice vector ($\boldsymbol{g_{hkl}}$) is identical to the scattering vector ($\boldsymbol{Q}$) (see Fig. 2.5 b). The resulting collected intensities are plotted onto a two-dimensional pole figure (pole plot as shown in Fig.2.5c. Strong diffractions occur only when Bragg's law is satisfied for lattice planes of the textured grains for a particular (*hkl*) reflection at a certain tilt, ψ, and rotation, ϕ.

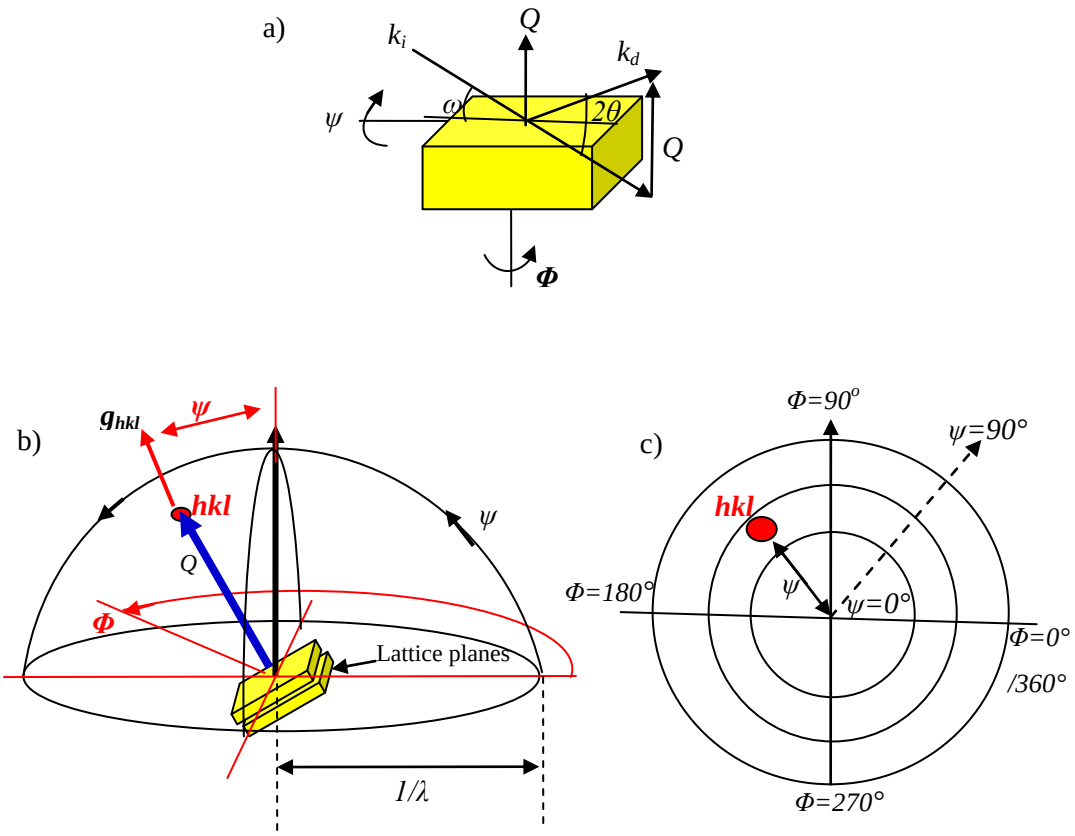
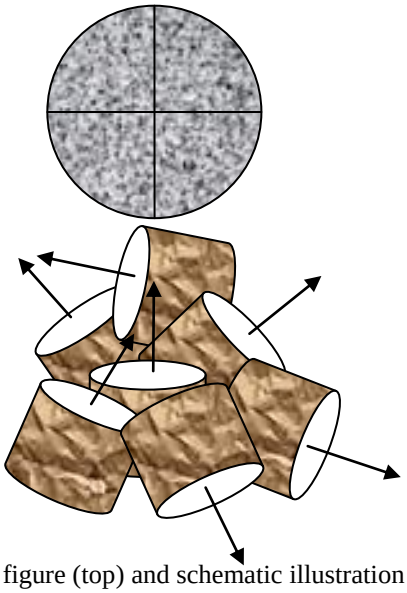
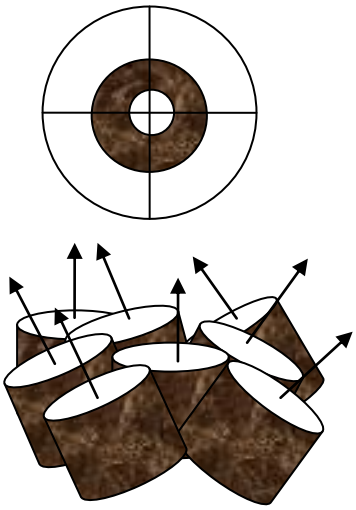


Figure 2.5 Schematic diagrams of a) 2θ-ω scan in reciprocal space, and scanning geometry for a pole figure, b) Hemisphere represents the stereographic projection of all reciprocal space, and c) Top view of the hemisphere (pole plot) [41, 44].

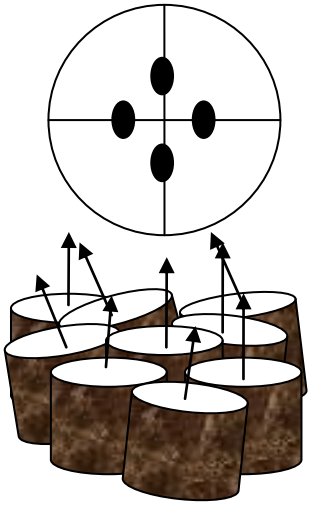
If the material has no texture, the collected signal will be uniformly distributed on the pole figure. Alternatively, poles will tend to group together at certain chi, ψ, and phi, ϕ, angles in the pole figure if the material comprises of some preferential grain orientations. If the preferred orientation is very strongly preferential, the poles will tend to group together in tighter and tighter bands as the texture becomes stronger as illustrated in Fig. 2.6.



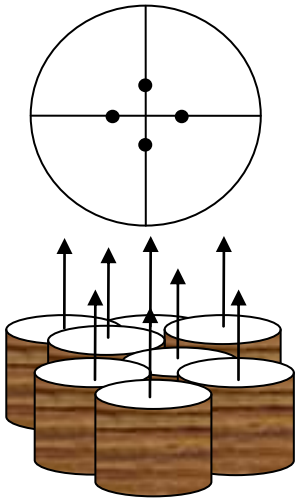
a) Pole figure (top) and schematic illustration of polycrystalline material with random orientation



b) Pole figure (top) and schematic illustration of highly textured polycrystalline material with certain preferred orientation



c) Pole figure (top) and schematic illustration of grain with preferred orientations in [001] direction, i.e. misoriented epitaxial layer



d) Pole figure (top) and schematic illustration of grain with strong orientations in [001] direction, i.e. a perfect single crystal layer

Figure 2.6 Pole figures and schematic illustrations of preferred orientation. The arrows show the direction for a chosen *(hkl)* direction.

2.4 High-resolution X-ray diffraction (HR-XRD)

The most significant difference between high-resolution XRD and conventional XRD measurements is the use of a highly collimated incident monochromatic beam, e.g. of the order of ~12 arc-sec divergence compared to ~ 360 arc-sec for conventional XRD measurements. The divergence of the beam is closely related to the source size (h), slit size (s) and the source-specimen distance (a). As shown in Fig. 2.7, the divergence ($\delta\theta$) is expressed as [43]

$$\delta\theta = \frac{h + s}{a} \tag{2.7}$$

In order to reveal the finest details from the specimen, the divergence of the beam has to be smaller than the angular offset caused by defects in the specimen. For conventional XRD measurements, the divergence of the beam is ~ 360 arc-sec [46] and yields a rocking curve with a broad full-width-at-half-maximum (FWHM). This is far beyond the angular resolution that we require to reveal the details of thin epitaxial films, where typically in the order of 10 arc-sec is necessary [43]. Therefore, a highly monochromatic incident beam is essential to provide sufficient angular resolution for HR-XRD measurements in order to reveal the layer thickness, composition, strain and relaxation of thin epitaxial films at the arc-second scale.

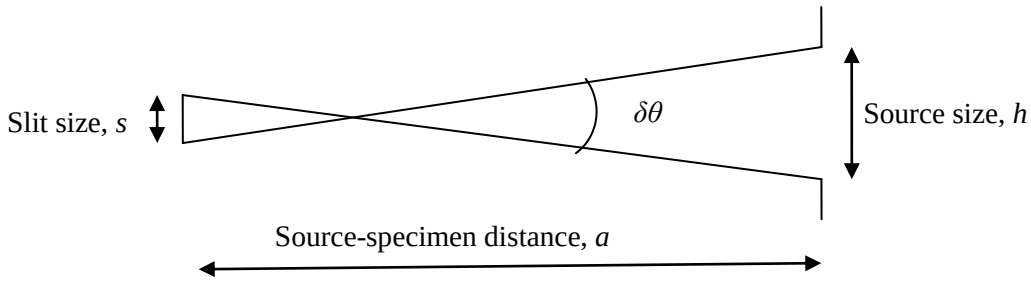


Figure 2.7 Schematic diagram showing the divergence along a single-axis [43].

2.4.1 HR-XRD experimental geometry

Symmetric and asymmetric reflection modes are the two types of experimental geometries typically used in HR-XRD experiments. A symmetric Bragg reflection geometry collects only the information from out-of-plane (direction perpendicular to the layer plane) structural parameters, while the use of asymmetric grazing incidence is exceedingly sensitive to the in-plane structural parameters (parameters of the crystal structure in the layer plane) (see Fig. 2.8) [46]. Combining the data from both geometries provides us with all the meaningful information that we require for analysis.

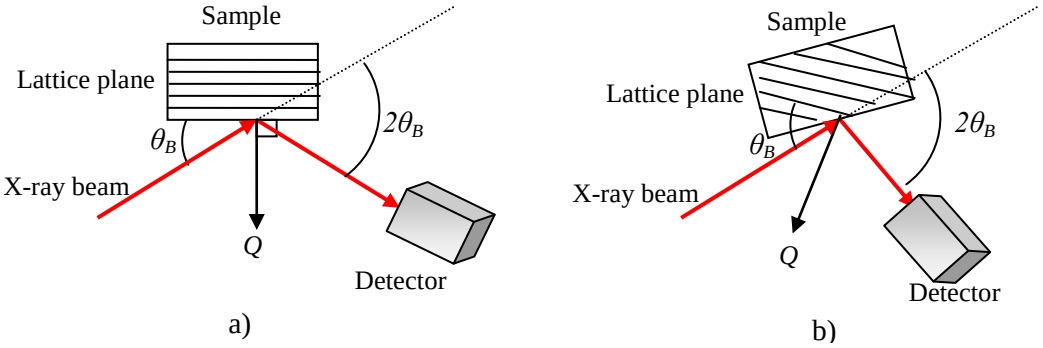


Figure 2.8 a) Symmetric (collects only the out-of-plane lattice parameter) and b) asymmetric (collects in-plane lattice parameter data) diffraction geometry for high-resolution X-ray diffraction.

2.4.2 High-resolution XRD rocking curves and *ω-2θ* scans

Two distinct types of HR-XRD scans are defined as ω (omega) scans and ω-2θ (omega-2theta) scans. An ω scan is used to evaluate the mosaic tilt in a material. It can be recorded by scanning the sample angle (ω) for a specific angular range of arc-sec with the detector angle (2θ) fixed at twice the known Bragg angle. The resulting plot of angle (ω) versus the collected intensity is known as a rocking curve. On the other hand, the ω-2θ scan is recorded by scanning the sample and detector angles together in a 1: 2 (ω: 2θ) ratio. Thus

the scan is collected by moving the 2θ detector axis at the twice the rate of the ω axis. This geometry is particularly useful in revealing the structural parameters of the epitaxial layer, i.e. strain, composition and layer thickness [43]. For instance, for GaAs heteroepitaxially grown on Si, defects such as dislocations are typically predominant due to the large lattice mismatch between GaAs and Si. These extended linear defects generated during the growth process directly impact on the full-width-at-half-maximum (FWHM) and peak splitting of the rocking curves (ω-scans) and ω-2θ scans, respectively [43]. Table 2.1 summarises some of the important parameters that will impact on the characteristics of rocking curves or ω-2θ scans.

Table 2.1 The effect of substrate and epilayer parameters upon the rocking curves and ω-2θ scans [43].

Material parameter	**Effect on rocking curve**	**Distinguishing features**
Mismatch	Splitting of layer and substrate peak	Invariant with sample rotation
Misorientation	Splitting of layer and substrate peak	Changes sign with sample rotation
Dislocation content	Broadens peak	Broadening invariant with beam size. No shift of peak with beam position on sample.
Curvature	Broadens peak	Broadening increases linearly with beam size. Peak shifts systematically with beam position on sample.
Relaxation	Changes splitting	Different effect on symmetrical and asymmetrical reflections.

High-resolution X-ray diffraction rocking curves (HR-XRD RCs) can be measured in either double-axis or triple-axis configuration based on the type of information that is required by the user. A typical double-axis RC experiment can be done in a short period of time. Conversely the time requirements are generally longer for triple-axis analysis as an additional analyser crystal is placed on the detector side for a more precise definition of the detector scattering angle, 2θ. This analyser crystal itself will quench the diffracted intensity, and thus,

longer exposure times are required to increase the signal-to-noise ratio in order to achieve a clean result. This also prevents the disappearance of some smaller peaks [43].

In the double-axis configuration, one collects the scattered intensity from all diffraction angles from the specimen and some vital parameters become indistinguishable, i.e. distinguishing between the lattice tilt and changes in interplanar (*d*) spacing of the crystal, and details such as interference fringes or narrow peaks can be lost or blurred [43]. This deficiency can be resolved unambiguously in triple-axis geometry by inserting the additional analyser crystal before the detector. The auxiliary crystal restricts the angular acceptance of the detector into few arc-seconds which further defines the 2θ angle [43].

2.4.3 HR-XRD analysis by RADs simulations

As previously mentioned parameters of the epilayer such as strain relaxation, thickness and composition can be extracted directly from the peak splitting and position of measured HR-XRD scans. These details are easily determinable by modelling ω-2θ scans using the supplied JV-HRXRD software [46] called RADs (rocking-curve analysis software). Experimental data is compared to the simulated model using a robust goodness-of-fit (GOF) function [46]. Parameters such as background intensity, layer thickness, layer composition and strain relaxation are iteratively adjusted until best-fit-parameter values are achieved (lowest GOF values - a single number that reflects how well the best-fit simulation agrees with the experimental data) [46]. Although RADs simulations provide a lot of information regarding the epilayer it is not a sufficiently sophisticated package to extract all the required detailed information from a complex crystal structure, such as a monocrystalline layer embedded in a highly-textured polycrystalline layer. Despite these deficiencies, RADs simulation is still useful for the full analysis of epilayers, multilayer structures and alloyed semiconductors.

The data-fitting process of RADs simulation includes few main stages, which will be demonstrated through an analysis of the degree of relaxation using a 004 ω-2θ HRXRD scan from a 180 nm thick- GaAs layer deposited on Si substrate:

i) Importing the experimental data

The file containing the experimental HRXRD data is imported into RADs and will be displayed in the form of an (x, y) line chart, as shown in Fig. 2.9.

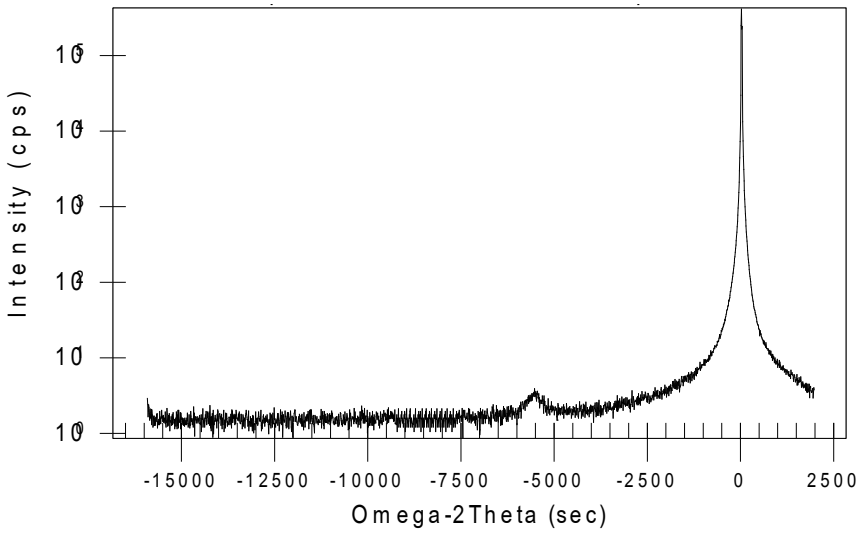


Figure 2.9 ω-2θ HR-XRD scan of GaAs/Si sample imported into Bede RADs.

ii) Creating a simulation model

A simulation model of the sample structure is built using the Model panel. For this case, bare Si is used as the substrate for the model, and then a GaAs layer is added to form the GaAs/Si simulation model. For the initial assumption, the GaAs layer thickness of the simulation model is set to the nominal thickness of 180 nm, and the degree of relaxation is assumed to be 0% (fully matched).

iii) Simulating the diffraction

The model built in the previous step is simulated and displayed as the red (x, y) chart, as shown in Fig. 2.10. It is obvious that the initial simulated HRXRD curve does not match the experimental data. This implies that the GaAs overlayer is relaxed, therefore further data fitting is required in order to determine the actual degree of relaxation.

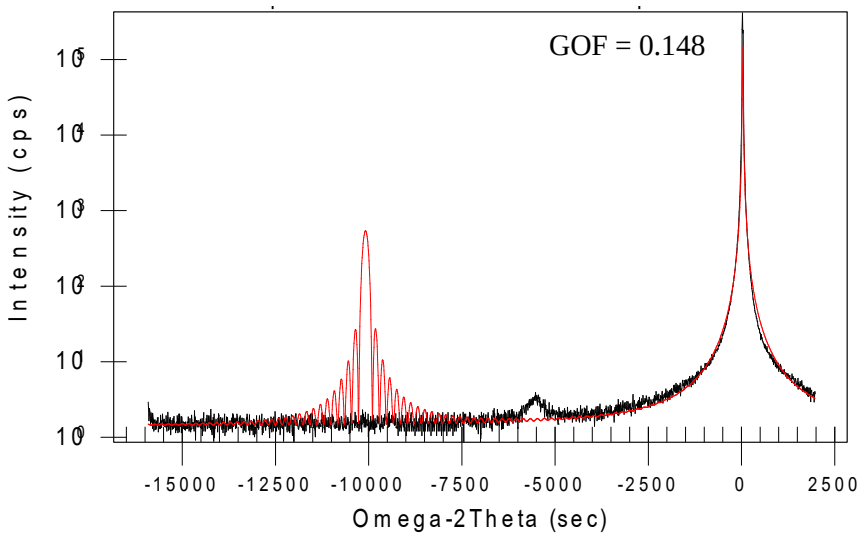


Figure 2.10 ω-2θ HR-XRD scans and corresponding initial simulation of GaAs/Si sample before data fitting.

iv) Fitting the diffraction

In order to obtain the best fit model, each parameter (relaxation degree and thickness) is fitted individually and iteratively by RADs simulation until a lowest GOF value is achieved. For example, Fig. 2.11a) shows the simulation model after the degree of relaxation is fitted and this reduces the GOF value to 0.117. The lowest GOF value or best fit model can be achieved when the thickness is fitted and background noise is introduced, as shown in Fig. 2.11b). From the best fit model, the GaAs/Si layer is determined to be fully relaxed (~100% relaxation) with 15 nm thickness.

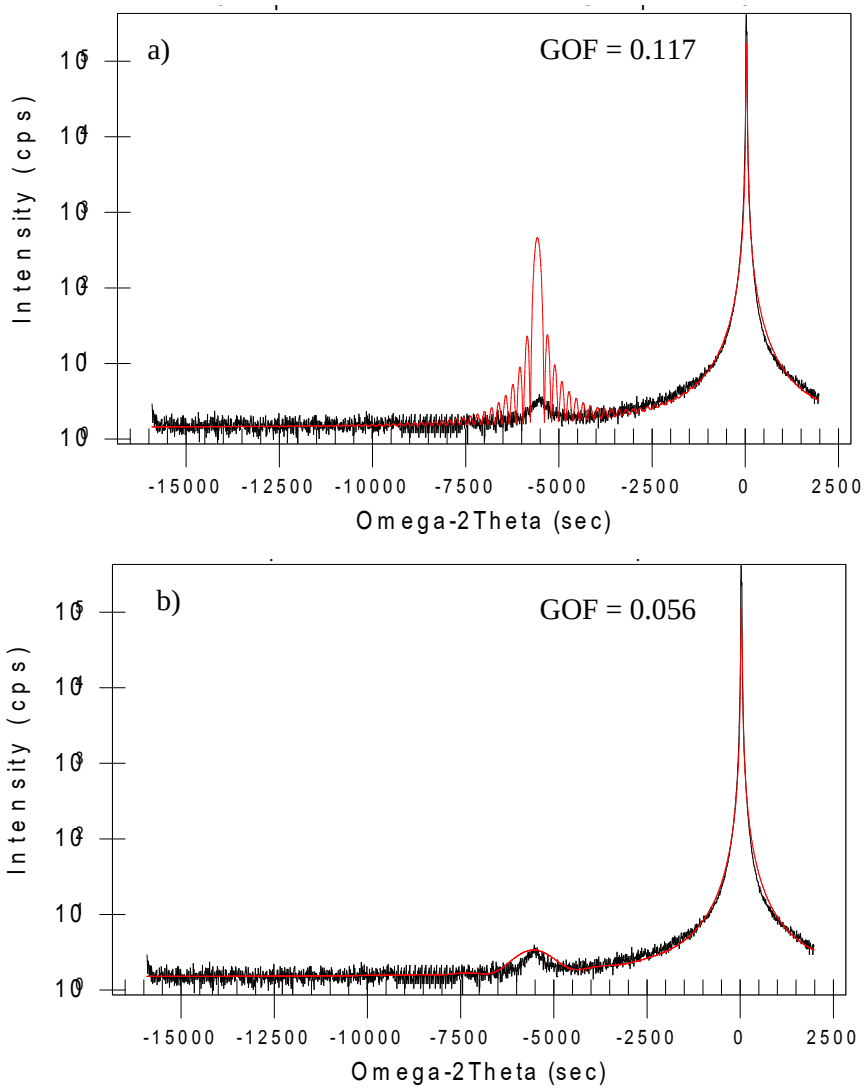
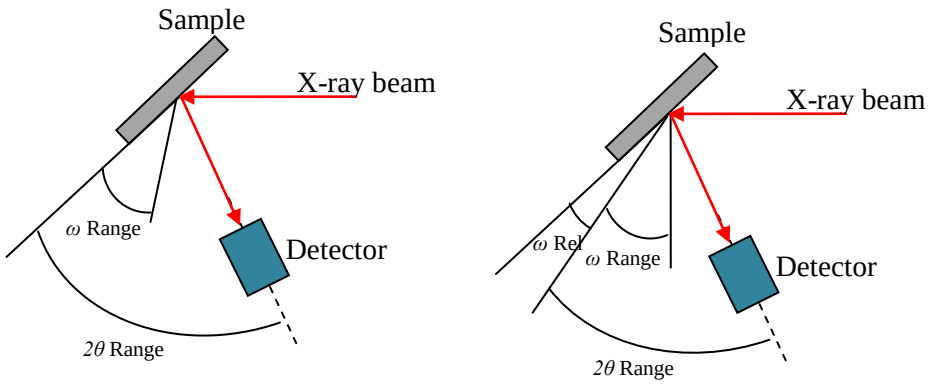


Figure 2.11 *ω-2θ* HR-XRD scans and corresponding simulation of GaAs/Si sample after data fitting. a) Simulation model after relaxation degree is fitted, and b) Best fit model achieved after the thickness and background noise are fitted. Note that the fit parameters can be found in Table 4.3.

2.4.4 Reciprocal space mapping

As described in the previous section, a triple-axis HR-XRD *ω-2θ* scan comprises of only the data from one specific tilt. In order to gather the information for a range of tilts,

reciprocal space mapping (RSM) is needed. This can be obtained by collecting a series of *ω-2θ* scans at different omega offsets (omega_Rel), where *2θ = 2*ω – offset*, as shown in Fig. 2.12. The tilt value recorded in each *ω-2θ* scan is typically different. Therefore, a RSM – a complete map of *ω-2θ* versus tilt (omega_Rel) - is obtained by mapping the intensity distributions of these scans using Contour software. In other words, it is an extension of rocking curve analysis that provides more valuable data in distinguishing the strain or mismatch from tilt or mosaic spread in a sample.



a) b)

Figure 2.12 a) For omega_Rel zero: A *ω-2θ* scan is collected, and b) A RSM can be obtained by collecting a series of *ω-2θ* scans at different omega offsets (omega_Rel), where *2θ = 2*ω – offset* [42].

2.4.5 X-ray diffraction instrument set-up

All X-ray diffraction measurements were carried out using a triple axis Jordan Valley BEDE-D1 X-ray diffractometer as shown in Fig. 2.13. The incident X-ray beam was produced by a Cu rotating anode generator operated at 45 kV and 40 mA. A beam conditioner is used to condition the incident beam into a quasi-parallel beam (with a divergence of ~360 arc-second) or further conditioned into monochromatic beam mode (with a divergence of ~12

arc-second) (Cu-$K_{\alpha 1}$; λ = 1.5405 Å) for standard XRD and high-resolution XRD measurements, respectively [46]. The instrument sample stage allows the sample to move in *x, y, z,* χ (chi, tilt of sample) and ϕ (phi, rotation of the sample about the surface normal). ω is the angle between sample and incident X-ray beam, whereas 2θ is the angle between incident X-ray beam and scattered X-ray beam (see Table 2.2 for the specification). All of these movements can be navigated via the Bede Control – instrument control software from Bede Scientific, and therefore allows the sample to be properly aligned prior to any of the X-ray measurements.

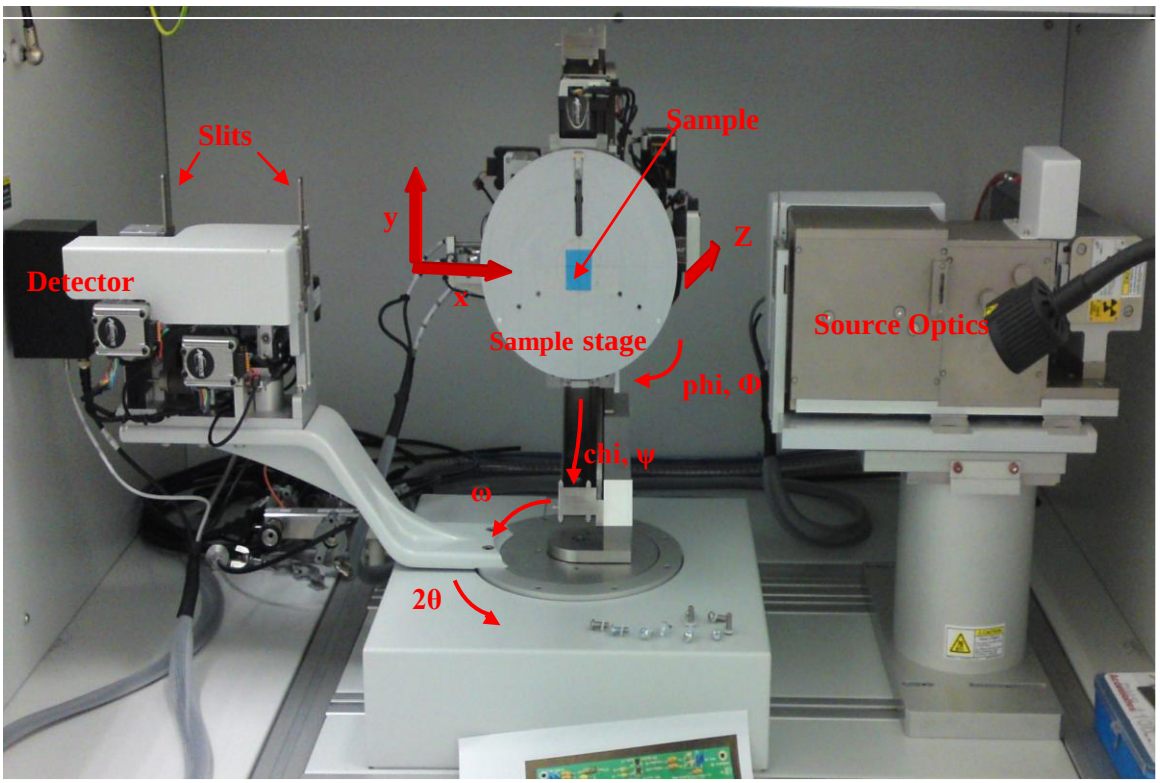


Figure 2.13 Photo of the Jordan Valley D1 X-ray diffractometer system.

Table 2.2 D1 system stage axes specification [46].

Axis	Function	Range	Resolution
x	Specimen translation, *x* direction	150 mm	0.5 µm
y	Specimen translation, *y* direction	150 mm	0.5 µm
z	Specimen translation, *z* direction	10 mm	0.5 µm
X, Chi	Specimen tilt	135^o (-90^o to $+45^o$)	0.0003^o
Φ, Phi	Specimen rotation about surface normal	$\pm 365^o$	0.0001^o
ω	Angle between sample and incident X-ray beam	200^o ($\sim -10^o$ to $\sim +190^o$)	$\sim 0.000045^o$ (~0.16 arc-sec)
2θ	Angle between incident X-ray beam and scattered X-ray beam	210^o ($\sim -70^o$ to $\sim +140^o$)	$\sim 0.000045^o$ (~0.16 arc-sec)

The sample alignment process includes a number of main steps listed below:

i) Mounting the sample onto the stage

- Sample should always be handled with clean tweezers in order to prevent contamination.
- Sample is mounted onto the central region of the stage using "blue tape", as shown in Fig. 2.13. This method of mounting has been found to introduce very little strain into the sample, which is important for high-resolution measurements [46].
- Always mount the sample in a known orientation i.e. the notch or flat or cleaved edge of the sample always placed in the same direction with respect to the X-ray beam. This allows the results from different samples to be easily compared and also to ensure very high reproducibility of the measurements.
- For a miscut sample, the offcut direction should be placed perpendicular to the incident beam, and the offcut can be compensated for by optimising the χ position of the sample, in order to ensure a "real" symmetric experimental geometry [8].

ii) Calibrating the 2θ and ω zero positions

- It is important to remember that the lid of the system should be closed before the X-ray shutter is switched on or prior to any XRD measurement.
- Scan across the direct beam with the sample out of the incident X-ray beam (by moving the *z* position to 9 mm) for a *2θ* range of 0.5°, and this gives us an X-ray intensity curve plotted against the *2θ* scan range. The peak position of the intensity curve is the actual zero position for *2θ*. The *2θ* zero position can be recalibrated by moving the *2θ* to the actual zero position via Bede control. The same process is repeated for *ω* in order to ensure both the *2θ* and *ω* zero positions are recalibrated correctly to avoid any misalignment, and therefore ensures an accurate and repeatable result.

iii) Aligning the sample in the beam by adjusting the position of sample stage

- The sample stage is moved (*z*) until intensity (I) = $I_{full}/2$, where I_{full} is the direct X-ray beam intensity. The position of *ω* is adjusted slightly in steps of 0.01° to observe the maximum intensity. If the intensity is higher than $I_{full}/2$, the position of *z* has to be readjusted slightly in order to ensure that intensity is equal to $I_{full}/2$.
- The incident beam is now properly aligned, which means it is parallel and half-way across the sample surface. This is to ensure that the incident beam is located at the centre of rotation of *2θ* and *ω* or the sample surface is now over the centre of rotation.

iv) Aligning the sample at the diffraction peak

- Move the *ω* axis to the Bragg angle and the *2θ* axis to the position of twice the Bragg angle of the substrate material (substrate peak is always chosen as reference for HR-XRD measurements). However, the Bragg angle is individually dependent on the type of experiments (symmetric or asymmetric) and also the orientation of the substrate material. For an offcut substrate, the incident beam is set perpendicular to the offcut

direction and the offcut can be compensated for by tilting the chi angle (χ) of the stage.

- Optimisations are then carried up for ω, χ and 2θ until the maximum intensity is acquired, this being the last step prior to measurements.

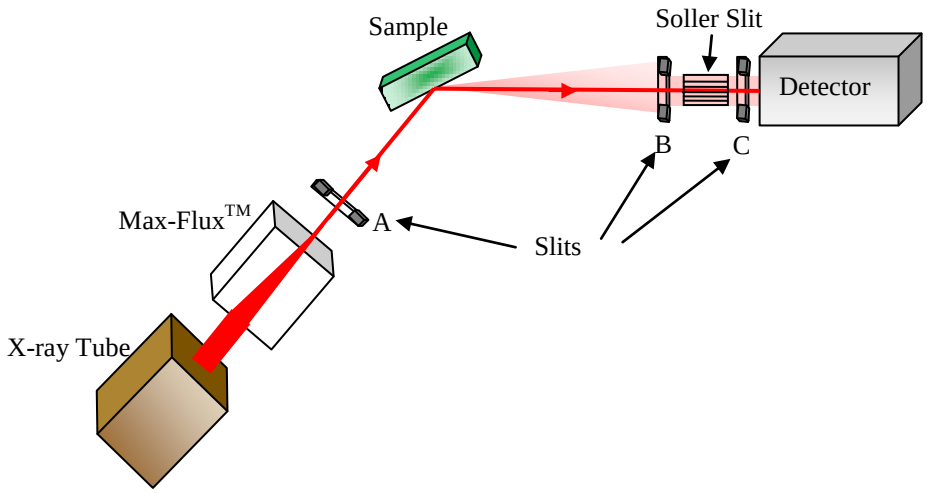
The sample alignment process can also be performed automatically by using scripts or recipes provided by this system. For certain circumstances, such as a sample with a few degrees of offcut, it is however more time efficient to manually align the sample using aforementioned steps ii)-iv).

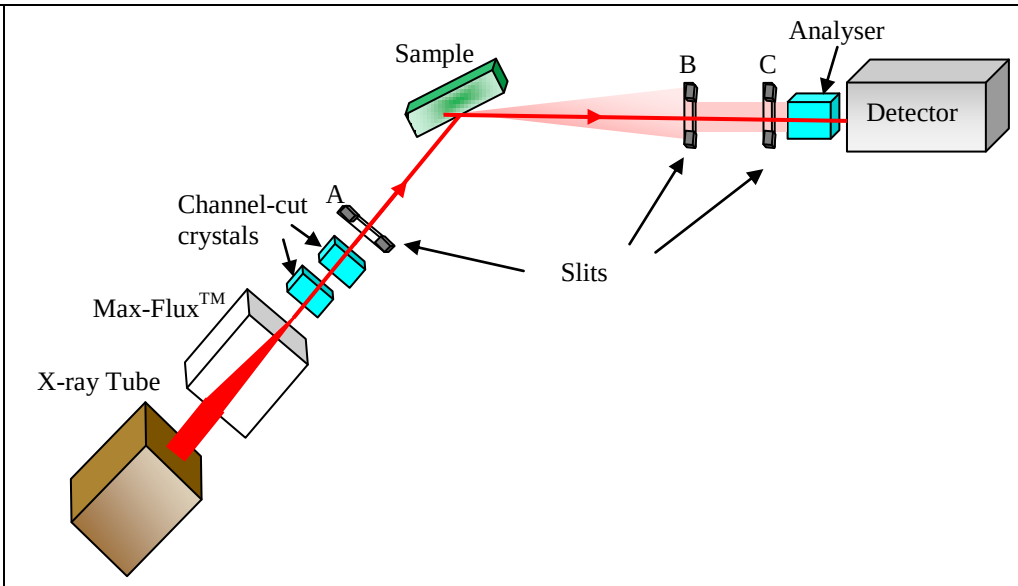
Apart from the sample alignments, the configurations of the XRD instrument such as the source optics and slit sizes have to be appropriately adjusted for distinct measurements and these are presented in Table 2.3.

All the scattered X-ray intensity is collected using an Enhanced Dynamic Range Detector (EDRc). It is a 50 mm, scintillator detector (YAP: Ce) with a background level of ~1 to 1.5 cps and a saturation level of ~ 5 Mcps [46]. In general, the signal-to-noise ratio (S/N) of a diffraction pattern can be improved by using a longer count time (exposure time), but an increase in count time would mean an increase in the scan time. In order to avoid unnecessary long waiting times, different count times are typically selected based on the type of sample or intensities or features of interest, and this is however dependent on many factors such as crystallinity, sample thickness, type of measurement. For example, a 0.01 second count time is sufficient to collect a clean diffraction pattern from a 1000 nm thick Si sample, but a 5 second count time will be needed to collect a clean pattern from a 50 nm thick Si sample due to low diffracted intensities compared to background noise.

It is important to always mount the sample, calibrate the system and align the sample in a consistent way as previously discussed. This allows us to achieve very accurate and highly repeatable results – in the order of the sampling step size [46].

Table 2.3 Tool configuration of X-ray diffraction instruments for different applications [43, 46].

<table>
<tr><th colspan="3">Standard X-ray diffraction – powder diffraction and crystallography texture mapping</th></tr>
<tr><td rowspan="4">Tool configuration</td><td>Schematic diagram</td><td> 
</td></tr>
<tr><td>Source optic</td><td>Max-Flux™ – modulates the divergence of incoming X-ray beam into a quasi-parallel beam of Cu K_α X-rays with a divergence of ~360 arc-second.
Slit – collimating the incoming beam to a width of 2 mm.</td></tr>
<tr><td>Detector</td><td>Slits – B and C are used to restrict the angular acceptance of diffracted X-rays and suppress diffuse scattering effects, respectively.
Soller slit – A set of parallel slits that used to limit the angular divergence or spread of the X-ray beam without restricting the size of the beam.</td></tr>
<tr><td>Axis</td><td>Scan is run by setting the sample and detector angles together in a 2:1 ratio, which is called a 2θ-ω scan. Typically, it is calibrated in $2\theta^o$ for power diffraction scans. This scanning geometry allows the probing of sets of planes which lie parallel to the sample surface, especially in highly-textured polycrystalline samples.</td></tr>
</table>

High-resolution X-ray diffraction – double-axis rocking curve and reciprocal space mapping		
Tool configuration	Schematic diagram	
	Source optic	Max-Flux™ – modulates the divergence of incoming X-ray beam into a quasi-parallel beam of Cu K_α X-rays with a divergence of ~360 arc-second. Channel-cut-crystal – Two Si channel-cut crystals (CCCs) used in opposition after the Max-Flux™ to further condition the beam into monochromatic Cu-$K\alpha_1$ with a divergence of ~12 arc-second. Slit – Slit A collimates the incoming beam to a width of 0.5 mm.
	Detector	Slits– B and C are used to restrict the angular acceptance of diffracted X-rays and suppress diffuse scattering effects, respectively. Analyser – used only in triple-axis diffraction to precisely define the detector position.
	Axis	Scan is run by setting the sample and detector angles together in a 1:2 ratio, called a ω-2θ scan. This scanning geometry is vital in order to probe the different interplanar spacings for the same sample tilt for high-resolution XRD. It was calibrated in arc-seconds prior to the measurements.

2.5 White Beam Synchrotron X-ray Topography (SXRT)

The concept of SXRT is analogous to the conventional laboratory-based XRD measurements, since both techniques are reliant on Bragg's law. Similar to XRD, the principle of SXRT can be explained using the geometrical construction of the Ewald sphere, as depicted in Fig. 2.14. For the lab-based XRD measurement, a monochromatic X-ray with a particular wavelength is used. Diffraction from a crystal plane (*hkl*) will occur only if Bragg's law is satisfied, i.e. if a reciprocal lattice point lies on the Ewald sphere. In other words, only diffraction from a specific set of lattice plane (*hkl*) of the crystal can be collected at one time. The diffraction from different crystal planes of interest can be acquired by orienting the sample to satisfy the Bragg condition for that particular plane [47].

Similar to X-ray diffraction, Synchrotron X-ray Topography (SXRT) is also a non-destructive method that is ideal for studying high quality crystalline materials, and in particular it can image defects and strain fields distributed within the crystals [48]. Using a white beam for SXRT brings several benefits, such as: sample orientation is not necessary, numerous reflections are recorded simultaneously with one exposure, all crystal parts are simultaneously visible, large diffracted intensity, and good geometrical resolution. One uses a continuous radiation spectrum (i.e. a "white beam") consisting of a continuum of wavelengths (λ) each of which can be diffracted subject to the Bragg criterion being satisfied [48], as previously discussed.

As shown in Fig. 2.14b), a white beam comprises of X-ray beams with a continuum of wavelengths, ranging from a minimum wavelength, λ_{min} to some maximum wavelength, λ_{max}. A white beam allows a range of reciprocal lattice points to lie simultaneously on Ewald spheres with different radii [49]. Therefore, multiple diffractions can be recorded simultaneously on a single film with a single white beam X-ray exposure, forming a so-called

Laue pattern (see Fig. 2.14c). Each Laue spot is an X-ray topograph corresponding to a reflection arising from a different crystal plane of distinct (*hkl*).

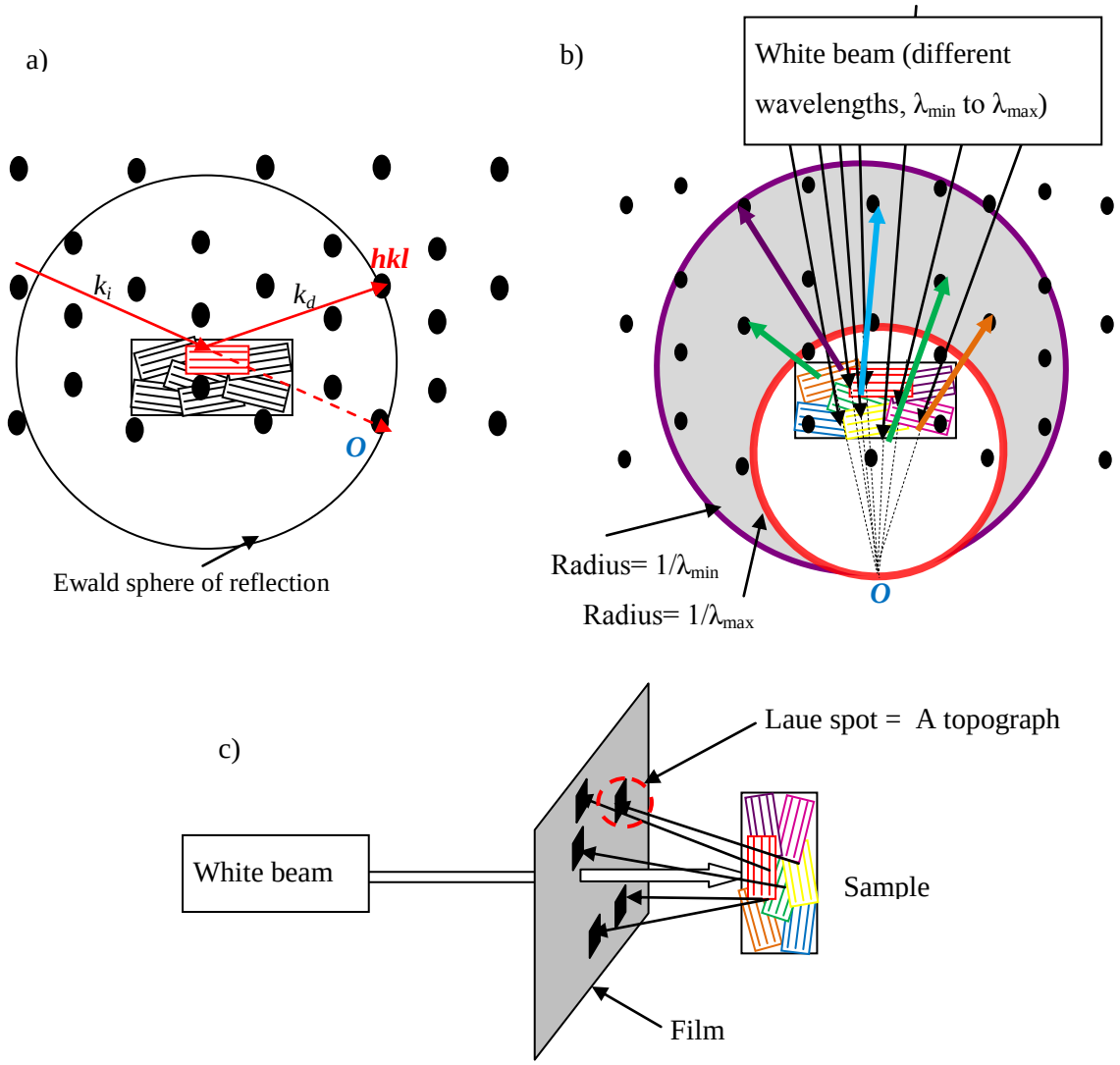
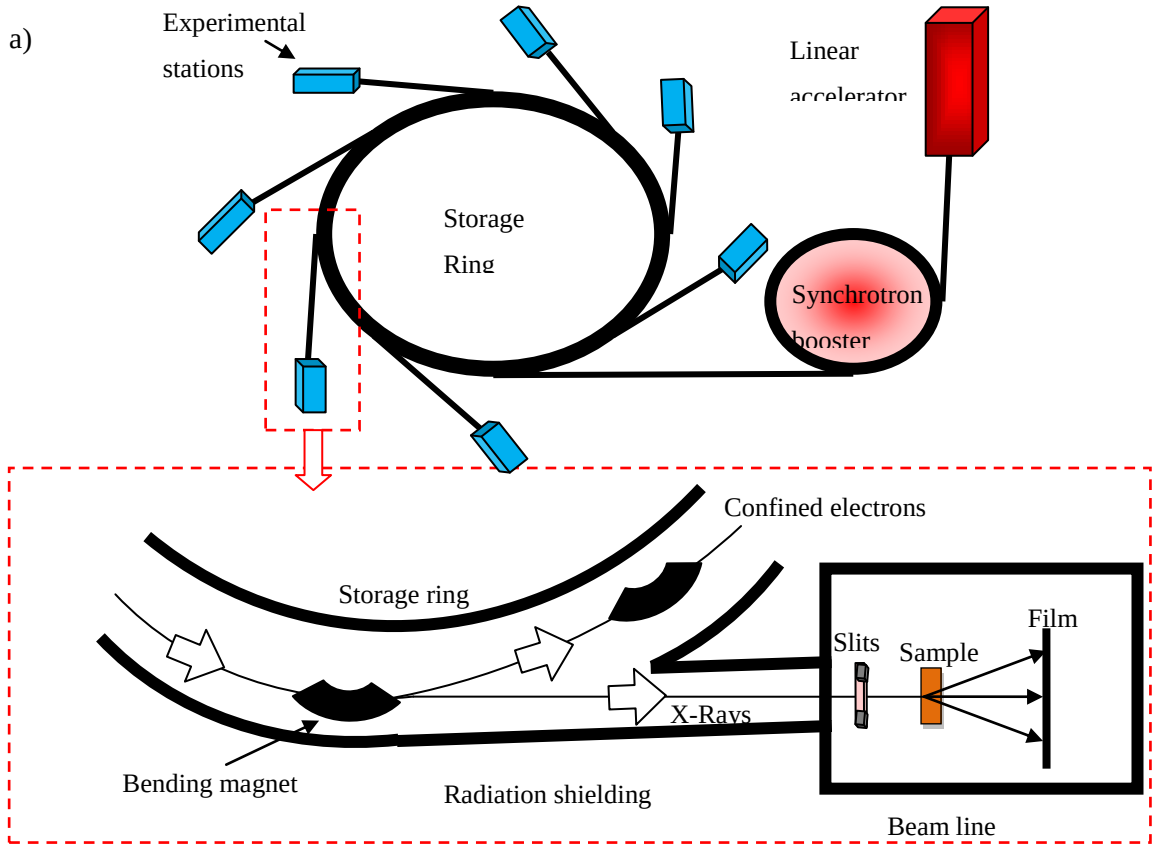


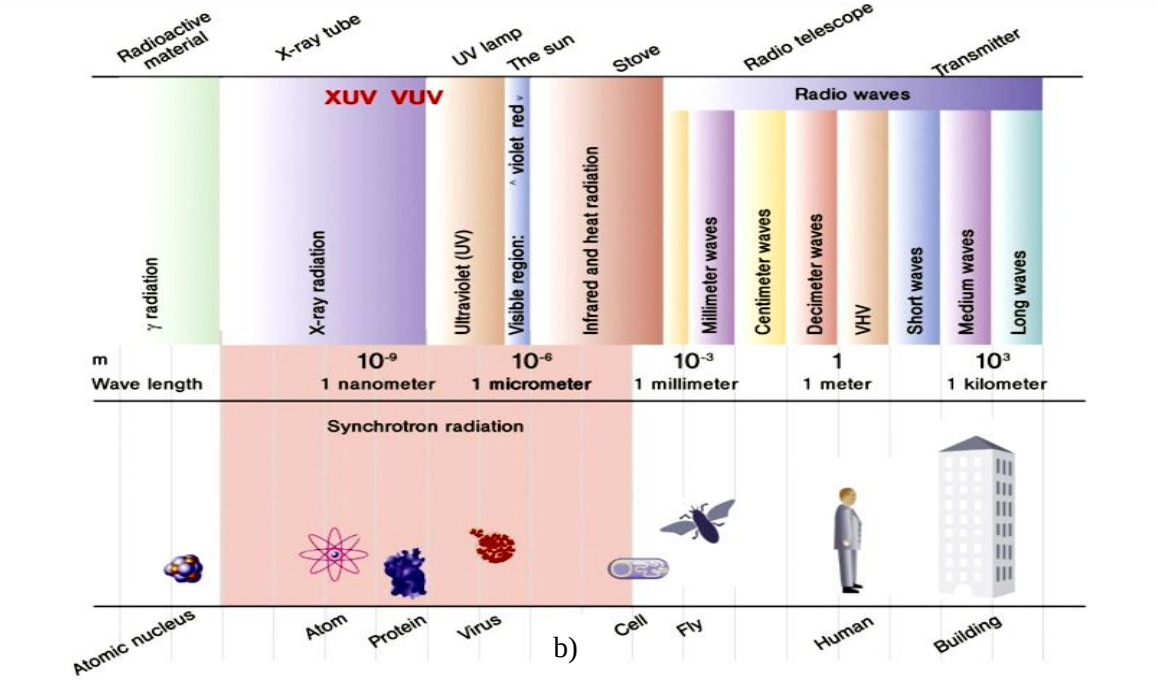
Figure 2.14 Ewald sphere diagrams illustrating the X-ray diffraction in reciprocal space a) using a monochromatic beam and b) using a white beam. Multiple Laue spots recorded on a single film using white beam in back reflection geometry is shown in c) [47, 48].

2.5.1 Synchrotron Radiation X-ray Source

Synchrotron radiation is generated when electrons or positrons, whose velocity is close to the speed of light, are accelerated and confined to a circular orbit in a storage ring by

a magnetic field [49]. The radiation source of a typical synchrotron facility comprises of a linear electron accelerator, a storage ring and beam-lines as illustrated in Fig. 2.15 a). The electrons are initially accelerated by the linear accelerator to a few tens of MeV, and then fully energised by a booster to 2-10 GeV prior to electron injection into the storage ring. The injected electrons travel within the storage ring by lying on the orbit specified by the bending magnets [49]. In addition, insertion devices known as wigglers or undulators are often installed in the straight section between the bending magnets, and these act as enhancers of the radiation intensity. Light is emitted tangentially from the electron paths within the bending magnets or from insertion devices within the straight sections. The light emitted from the bending magnet components is of a continuous spectrum and is now useable at beamlines located off the central storage ring. The electromagnetic spectrum of a typical synchrotron radiation source is shown in Fig. 2.15b).





b)

Figure 2.15 a) Schematic diagram and light output of a typical synchrotron radiation facility [49], and b) The electromagnetic spectrum of a typical synchrotron radiation source [50].

2.5.2 Experimental geometry

X-ray topographs were taken at HASYLAB-DESY, Hamburg, Germany (Hamburger Synchrotronstrahlungslabor am Deutschen Elektronen-Synchrotron) using the continuous radiation spectrum emitted by a bending magnet source in the DORIS III storage ring. The positron ring at DORIS III had a particle energy of 4.45 GeV and a beam current of 100-180 mA.

Prior to SXRT experiments, the position of the incident beam was adjusted in order to make a straight line to the sample. This is one of the most critical initial steps of the experiment, and it can take up to several hours to align the beam back to the correct position if it is misaligned. Generally, the incident beam size was collimated to the dimensions of 2 mm x 2 mm for large-area SXRT. The sample was mounted on a metal holder clamped in

position using a stand (see Fig. 2.16) and the topographs were recorded either on Agfa D3 X-Ray Film (~1 μm grain size) or on a higher resolution Slavich VRP- M holographic film (grain size ~0.04 μm) set ~80 mm in front of or behind the sample in the back reflection and the transmission geometry, respectively (see Table 2.4). Multiple topographs were recorded simultaneously on a single film with a single white beam X-ray exposure, forming Laue patterns (See Table 2.4). Each Laue spot is an X-ray topograph corresponding to reflection arising from a different set of atomic planes of the crystal under test. The individual topographs were magnified using a light microscope and the details of the growth defects could be observed and analysed. Software called LauePT [51] is used to index the individual topographs recorded on the film.

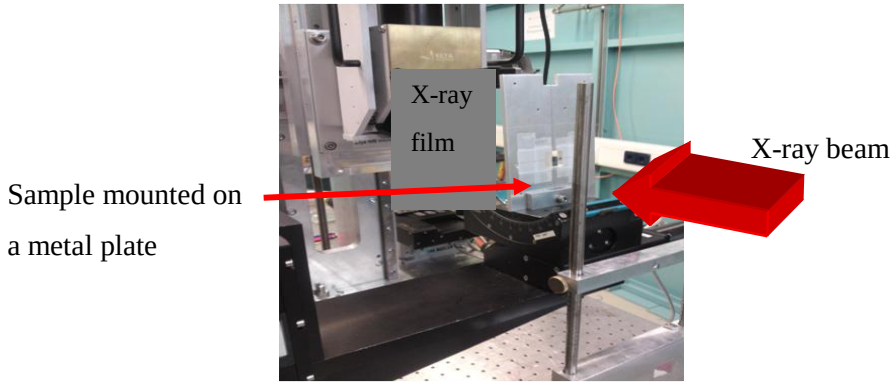
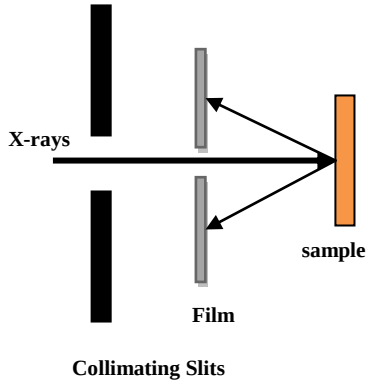
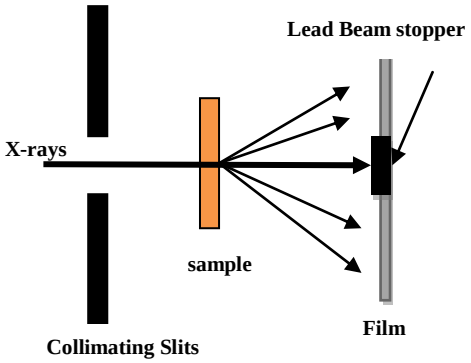
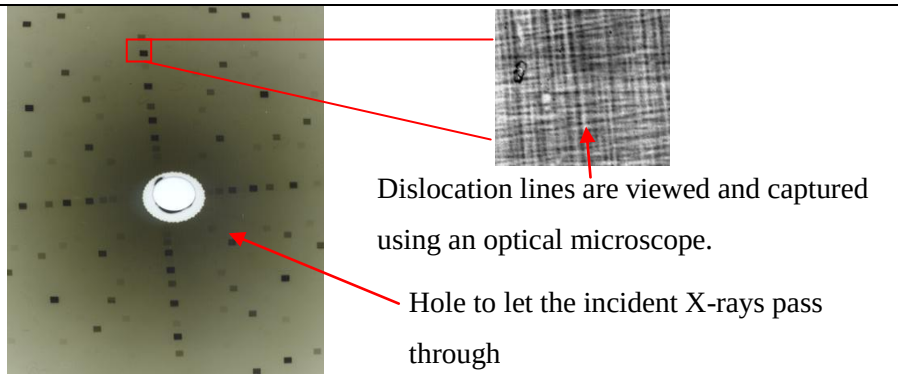


Figure 2.16 Experimental station of SXRT with a sample mounted on the metal plate.

Table 2.4 X-ray topography experiment geometry.

<table>
<tr><th>Back Reflection Set-up Geometry</th><th>Transmission Set-up Geometry</th></tr>
<tr><td> 
</td><td> 
</td></tr>
<tr><td colspan="2">Back Reflection Laue pattern of GaAs/Ge recorded on a film.</td></tr>
<tr><td colspan="2"> 
</td></tr>
</table>

2.5.3 The resolution of SXRT

The spatial resolution refers to the smallest possible feature that can be resolved on a SXRT topograph. The spatial resolution can be calculated through the following relationship [49]:

$$r = \left(\frac{S}{L}\right) h \qquad (2.8)$$

where s is the specimen-to-film distance, L is the source-to-specimen distance and h is the source size. From Eq. 2.8, it is obvious that a better image resolution can be achieved by

using a longer beam line and a smaller source size, as depicted in Fig. 2.17 [49]. From the references [52], the main specifications of the Synchrotron at HASYLAB-DESY are summarised in Table 2.5. In the work, all the large area back reflection (LABR) experiments were carried out using a sample to film distance of 80 mm, and this gives a spatial resolution of ≈3 μm, calculated using Eq. 2.8.

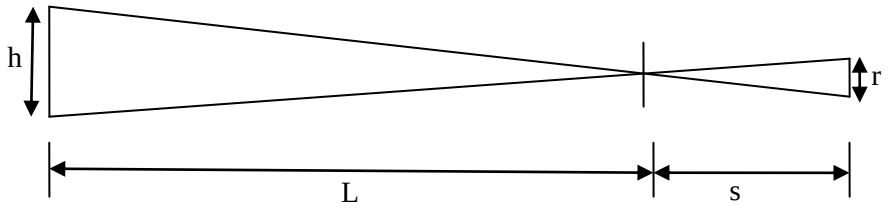


Figure 2.17 Schematic diagram illustrating the geometrical resolution limit set by the projected source height normal to the incidence plane [49].

Table 2.5 Main specifications of the Synchrotron at HASYLAB-DESY [52].

Parameter	**Value**
Source-Sample Distance	35 m
Source Size	1.224 mm x 0.510 mm
Beam Divergence	0.400 mrad x 0.238 mrad

2.5.4 Penetration depth calculation

For back reflection topography, the X-ray penetration depth into the sample for each reflection can be calculated based on conventional kinematical theory (this is applied to imperfect or strained materials, such as GaN, SiC, GaAs or other lattice mismatched materials.) [53, 54]:

$$t_p = \left[\frac{1}{\mu(\lambda)\left(\frac{1}{sin\Phi_i} + \frac{1}{sin\Phi_h}\right)}\right]; \qquad 2.4$$

where t_p is the penetration depth, Φ_i is the incident angle, Φ_h is the diffracted angle and $\mu(\lambda)$ is the wavelength-dependent absorption constant for the material. For back reflection, $\Phi_i = 90^o$ and $\Phi_h = 90^o - \tan^{-1}(\frac{\mathrm{H}}{\mathrm{L}})$, where L and H are the film to sample distance and distance from centre of film, respectively, as illustrated in Fig. 2.18. Table 2.6 summarises the typical penetration depths calculated from different reflections of LABR topographs recorded from Si material.

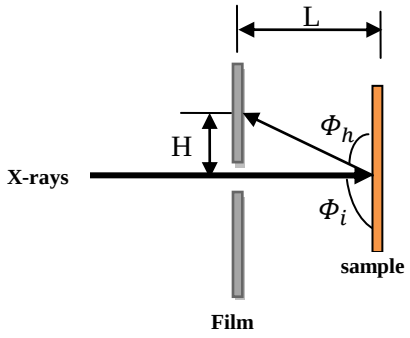


Figure 2.18 Schematic diagram of a typical back reflection process.

Table 2.6 Penetration depths calculated from back reflection topographs of Si material. Note that, the penetration depths presented in this table are calculated from harmonically pure reflections.

Reflection	**L (mm)**	**H (mm)**	**λ (Å)**	**d (Å)**	**Penetration Depth (μm)**
-2 2 8	80	50.5	1.2276	0.6401	63
-1 1 7	80	23.6	1.5046	0.7605	37

2.5.5 Dislocation density estimation

From the dislocation networks observed in a topograph, the area dislocation density (cm^{-2}) of a particular specimen is determinable through the following relation [55],

$$\rho = L/V \qquad 4.20$$

where V is the volume of the specimen exposed to the X-rays and L is the total dislocation line length in that volume. Volume, V can be calculated using the beam size and X-ray penetration depth, t_p.

2.6 Micro-Raman Spectroscopy

Micro- (μ-) Raman spectroscopy is a powerful non-destructive technique for evaluating the quality of a semiconductor. It is extremely sensitive to the presence of lattice disorder, impurities and stresses, and these are detectable via variations observed in the peak intensity, full-width-at-half-maximum (FWHM) and position (wavenumbers) of the peaks recorded in the μ-Raman spectra.

2.6.1 The mechanism of light scattering

The mechanisms of light scattering can be categorised into Rayleigh, Stokes and Anti-Stokes scattering, as illustrated in Fig. 2.19 [56]. Rayleigh scattering occurs when the incident light is elastically scattered, during a process in which an atom or a phonon for condensed matter is excited by a photon (Energy, $E_o = \hbar\omega_o$) from its vibrational ground state to a virtual state, where $\hbar$ and ω_o are the Planck constant and vibrational frequency of the atom or phonon, respectively [56]. The excited atom or phonon can eventually be returned to the ground state by emitting a photon of the same energy, $E = \hbar\omega_o$. Alternatively, the excited state can be returned to another vibrational level. In this case, the energy difference is emitted

as a photon of lower energy, $E = \hbar(\omega_o - \omega_{vib})$, i.e. light emission with a longer wavelength, and this process is called Stokes scattering. The third mechanism is known as Anti-Stokes scattering. This occurs if the atom or phonon starts off in the first excited vibrational level and is then irradiated with photons whose energy is $E_o = \hbar\omega_o$ inducing a transition to the virtual state. When the excitation relaxes, it will be returned to the vibrational ground state by emitting a photon of energy $E = \hbar(\omega_o + \omega_{vib})$ which results in light emission at shorter wavelengths [56].

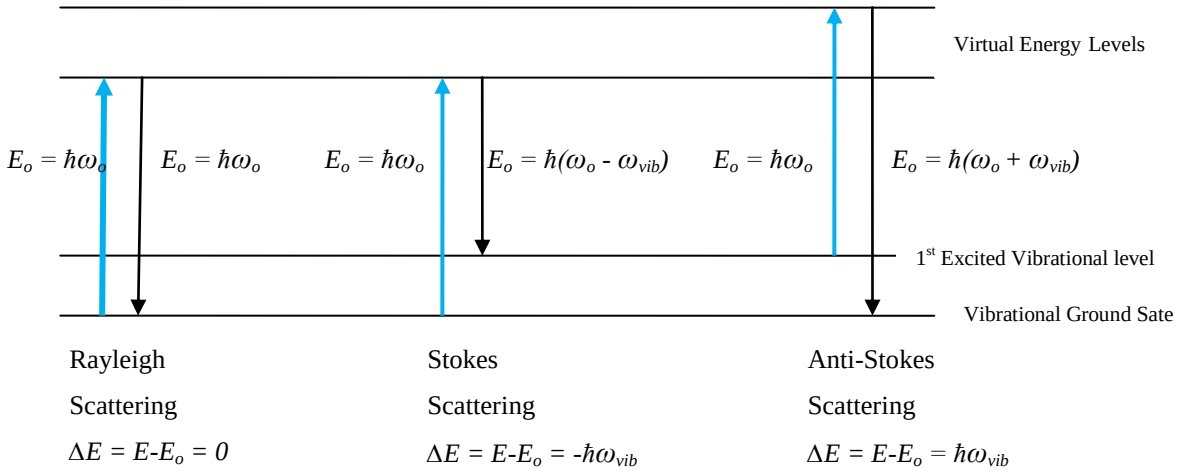


Figure 2.19 Schematics of Rayleigh, Stokes and Anti-Stokes scattering [56, 57].

Both Stokes scattering and Anti-Stokes scattering involve light scattering at different energies, which is manifested as inelastic scattering (Raman scattering). According to the rules of conservation of energy and momentum, the Raman scattered photons gain energy by absorbing a phonon (anti-Stokes shifted), or lose energy by emitting a phonon (Stokes shifted) [19]. For condensed matter energy and momentum conservation are represented by [56]:

$$\hbar\omega_s = \hbar\omega_i \pm \hbar\omega_j \qquad (2.9)$$

$$K_s = K_i \pm q_j \qquad (2.10)$$

where $\hbar\omega_s$, $\hbar\omega_i$ and $\hbar\omega_j$ are the energies of scattered photon, incident photon and phonon of vibration, respectively, while K_s , K_i and q_j are the wavevectors of the scattered photon, incident photon and phonon of vibration, respectively.

In other words, Raman scattering is an inelastic scattering of light as a result of the induced dipole moment due to the interaction between incident light and the vibrational modes of the material. The most straightforward way to model the process is to consider gaseous models, though the results are directly transferable to phonon vibrational modes. The strength of the induced dipole moment, *P*, in a molecule by the electric field, *E*, of the incident EM wave (or incident light) is given by [56, 58]

$$P = \alpha E \tag{2.11}$$

where α is the polarisability of the molecule. The polarisability is a measurement of the extent by which the electron cloud around a molecule is distorted. It depends however on the nature of the bonds. The electric field, *E*, of the incident EM wave may be expressed as [56, 58]

$$E = E_o \cos(2\pi\omega_o t) \tag{2.12}$$

where E_o is the vibrational amplitude and $\omega_o = c/\lambda$ is the frequency of the laser light. Subsituting Eqt. (2.6) into (2.5) yields the time-dependent induced dipole moment [56, 58]

$$P = \alpha E_o \cos(2\pi\omega_o t) \tag{2.13}$$

For a molecular bond vibrating at a vibrational frequency of ω_{vib}, the physical displacement, q of the atoms about their equilibrium position is written as [56, 58]

$$q = q_o \cos(2\pi\omega_{vib} t) \tag{2.14}$$

where q_o is the maximum displacement about the equilibrium position. For a small amplitude of vibration, the polarisability can be written as [56, 58]

$$\alpha = \alpha_o + \frac{\partial \alpha}{\partial q} dq \tag{2.15}$$

where α_o is the polarisability of the molecular mode at equilibrium position and $\frac{\partial \alpha}{\partial q}$ is the changing rate of the polarisability with respect to the change in q (at equilibrium position). By substituting Eqs. 2.8 and 2.9 into Eq. 2.7, we obtain [56, 58]

$$P = \alpha_o E_o \cos(2\pi\omega_o t) + \frac{\partial \alpha}{\partial q} q E_o \cos(2\pi\omega_o t) \cos(2\pi\omega_{vib} t) \tag{2.16}$$

Using a trigonometric identity, the above equation can be rewritten as

$$cosAcosB = \frac{1}{2}\cos(A + B) + \cos(A - B)$$

$$P = \alpha_o E_o \cos(2\pi\omega_o t) + \left(\frac{\partial \alpha}{\partial q}\frac{qE_o}{2}\right)\{cos[2\pi(\omega_o - \omega_{vib})t] + cos[2\pi(\omega_o + \omega_{vib})t]\} \tag{2.17}$$

The first term of Eq. 2.22 represents the oscillation of the induced dipole moment at the frequency, ω_o, of the incident light, leading to elastic scattering (Rayleigh). The later terms correspond to inelastic scattering processes (Raman scattering) in which light scattered at frequencies $\omega_o - \omega_{vib}$ (Stokes) and $\omega_o + \omega_{vib}$ (anti-Stokes), respectively. Raman scattering will only be observed if $\frac{\partial \alpha}{\partial q} \neq 0$, i.e. there must be a change in polarisability with the vibrational mode [56, 58].

2.6.2 Raman selection rules in backscattering geometry

The scattering efficiency or intensity (*I)* of Raman scattering relies on the polarisation vector of the incident and scattered light, and it can be represented by [56]

$$I = |\mathrm{e_i} \bullet \mathrm{R_j} \bullet \mathrm{e_s}|^2 \tag{2.18}$$

where (e_i) and (e_s) are the polarisation vector of the incident and scattered light, respectively, and R_j is the Raman tensor (which carries the geometric information about the crystal). An examination of the Raman tensors for the 32 crystal classes derived by Hayes and Loudon [59], shows that there are three Raman tensors corresponding to the crystal coordinate system (x=[100], y=[010], and z=[001]) of semiconductors with cubic crystal structure:

$$R_x = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & d \\ 0 & d & 0 \end{pmatrix} \; R_y = \begin{pmatrix} 0 & 0 & d \\ 0 & 0 & 0 \\ d & 0 & 0 \end{pmatrix} \; R_z = \begin{pmatrix} 0 & d & 0 \\ d & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \qquad (2.19)$$

where *d* represents the non-zero component in the matrix coordinates of *ij*.

For example, in the backscattering geometry, the Raman spectrum of perfect GaAs (001) surface comprises of only the R_z term, which corresponds to the longitudinal optical (LO) mode polarised along z [001]. However, the transverse optical (TO) mode can be present when there is lattice disorder or other defects distributed in the crystalline structure [60, 61]. This is due to the deviation from the true backscattering geometry inside the material, and therefore R_x and R_y (phonons polarised along x and y directions) are also involved in additional to R_z [62]. Fig. 2.20 shows the scattering process of a Raman system in the backscattering experimental geometry. Fig. 2.20b) illustrates the reason why the intensity ratio of the longitudinal optical (LO) and transverse optical (TO) Raman lines in GaAs are useful as a qualitative signature of the crystal perfection [63].

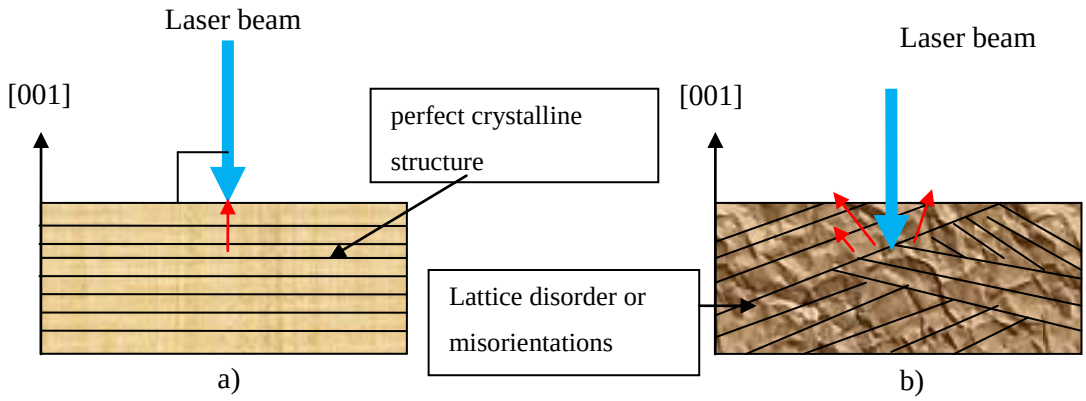


Figure 2.20 Schematic diagram represents the scattering process and geometries of (001) surface in a) a perfect crystalline structure, and b) crystalline structure with lattice disorder or misorientation. Red arrows indicate the scattered light.

2.6.3 Raman spectrum

A Raman spectrum is a plot of measured Raman vibrational frequency in wavenumber, cm^{-1} (x-axis) against the Raman scattering intensity (y-axis). The x-axis represents the Raman shift, which is the wavelength, or conventionally, wavenumber difference between the scattered radiation and the excitation radiation of the probe laser light [64]:

$$Raman\ shift, \Delta\omega\ (cm^{-1}) = \Delta\omega_{Laser} - \Delta\omega_{Scattered} \quad (2.20)$$

The frequencies of the Raman modes are always measured relative to the frequency of the laser light, and are denoted by relative wavenumbers (Rcm^{-1}). Nonetheless, the R is generally omitted and the Raman spectrum is labelled simply in units of cm^{-1}.

2.6.4 Frequencies of Raman peaks

The frequency of the Raman mode is closely related to the masses, the interactomic forces and their bond lengths. Therefore, any alteration in these features will indirectly change the frequency of the Raman modes [65].

The effect of stress on Raman frequency can be qualitatively understood by considering the crystal lattice as an array of atoms interconnected by a series of springs (see Fig. 2.21). The presence of a stress will alter the spring constant (i.e. lattice spacing) leading to Raman shifts [65]. For instance, a compressive stress will reduce the lattice spacing, and thus increases the vibrational frequency of the Raman mode. If tensile stress is present, it increases the lattice spacing which leads to the decrease of the vibrational frequency. For a simple case such as biaxial stress in a (001) GaAs, the Raman shift will change linearly with the magnitude of stress [64]. Therefore, the type of stress present in the (001) GaAs can be easily determined by comparing the Raman peak positions measured from stressed GaAs and bulk GaAs;

$$Type\ of\ stress <=> \Delta\omega_{Bulk\ GaAs} - \Delta\omega_{Stressed\ GaAs}\ (cm^{-1}) \qquad (2.21)$$

where a negative and positive Raman shift is a signature of the presence of tensile and compressive stresses in the specimen under test, respectively.

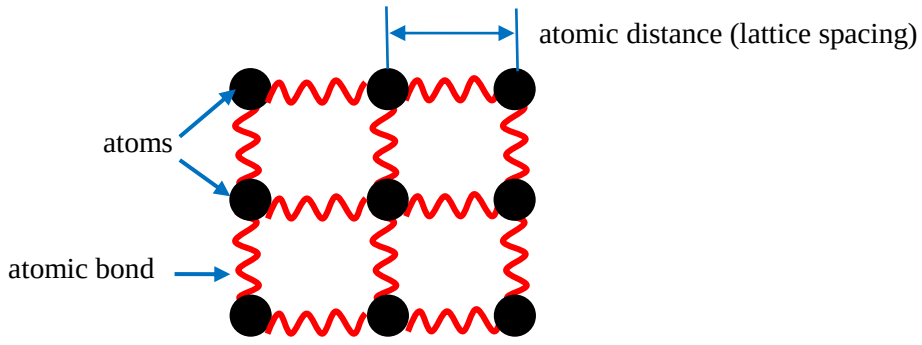


Figure 2.21 Schematic diagram showing 2-dimensional crystal lattice with atomic bonds modelled as springs [37].

2.6.5 Probe depth of the laser light

The Raman intensity collected from a sample is dependent on the volume of the sample being probed. Generally, shorter wavelengths give a smaller penetration depth. The total scattered integrated light intensity, I_s from the surface of the sample to a depth, *d,* is given by [66]

$$I_s = I_o D \int_0^d e^{-2\alpha x}\, dx = \frac{I_o D}{2\alpha} e^{-2\alpha d} \tag{2.22}$$

where I_o, *D*, and α are the incident light intensity, the Raman scattering cross section and the photoabsorption coefficient of the probed material, respectively. If one assumes that the penetration depth, d_p, is given by the depth that satisfies the relationship [66]

$$\frac{I_d}{I_s + I_d} = 0.1 \tag{2.23}$$

then the penetration depth can be defined as [66]

$$d_p = \frac{-ln0.1}{2\alpha} = \frac{2.3}{2\alpha} \tag{2.24}$$

For example, the penetration depth of 488 nm argon ion laser light is 570 nm and 90 nm in crystalline silicon and gallium arsenide, respectively, where the absorption coefficient (α) is obtained from the work reported by Aspnes *et al.* [67].

2.6.6 Spatial resolution of a Raman microscope

The spatial resolution of a Raman microscope is closely related to the laser wavelength and microscope objective being used. It can be approximately predicted by the following equation [68]:

$$Spatial\ resolution = \frac{1.22\lambda}{NA} \tag{2.25}$$

where λ is the laser wavelength, and *NA* is the numerical aperture of the microscope objective being used. For example, the best spatial resolution which can be achieved from a Raman system equipped with a *NA*=0.90/100x objective lens and a 488 nm laser is calculated to be around ~1 μm.

2.6.7 Micro-Raman spectroscopy experimental setup

In this work, a Jobin Yvon Horiba LabRAM 800 spectroscopic system with a 488 nm Ar^+ laser, was used to capture the micro-Raman spectra at room temperature in back scattering geometry. The experimental setup is shown below:

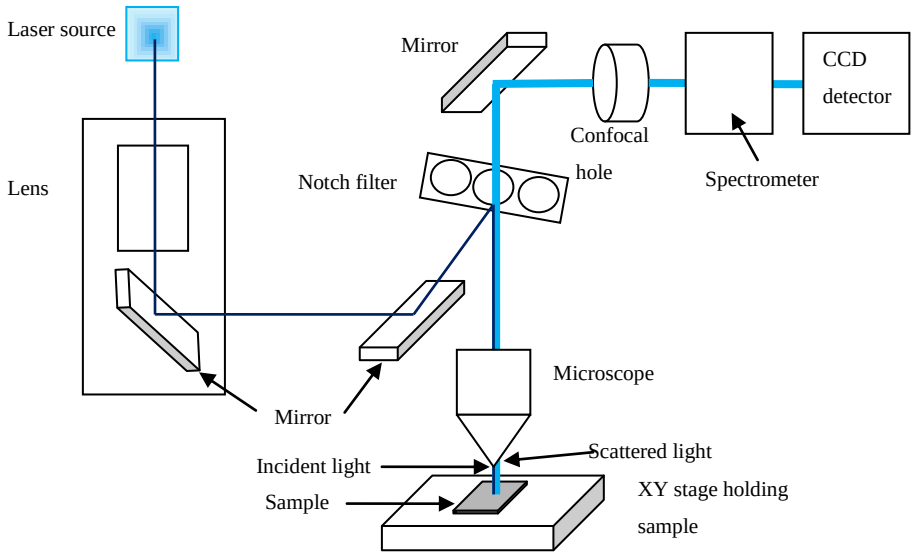


Figure 2.22 Experimental set-up for micro-Raman spectroscopy [69].

The laser was focused on the sample surface with an Olympus 100x microscope objective. The sample was moved by an automatic motorised XY stage whose step resolution is 0.1 μm. The scattered light from the sample was collected via the same microscope objective and passed directly through a notch filter, where the Rayleigh scattering is filtered

out. The filtered beam was then detected as a Raman signal by a liquid nitrogen cooled charge coupled device (CCD) detector using a dispersion grating of 1800 g/mm with a minimum peak shift resolution of 0.02 cm^{-1} and a measurement repeatability on the order of 0.1 cm^{-1}. An integration time of 5 seconds was usually selected and three Raman spectra from the same probe position were averaged to increase the S/N.

The spectroscopy was calibrated prior to the measurement in order to ensure the consistency and accuracy of the results. More specifically, Raman calibration comprises of two major steps: firstly, the spectrograph was calibrated in wavelength (nm) using a white light beam in order to ensure the zero position observed in the spectrograph matches the zero position of the motor of the spectroscope. Secondly, the Raman peak position of a piece of strain-free Si at 520.07 cm^{-1} was used as a reference point for calibrating the step-size of the motor movement. The sample of interest was then placed on the sample stage and positioned underneath the selected optical lens for measurements. In addition, the incident beam which impinges on the sample has to be properly focused, this being another critical step prior to Raman measurements.

In the case of improper calibrations and incident beam focusing, the results can be inaccurate whereby the Raman peaks may be shifted either towards higher or lower wavenumbers (cm^{-1}) and the collected Raman spectrum intensity will be quenched, respectively. Apart from that, the power of the laser source was kept at low levels (~ 10 mW) in order to prevent Raman peak shifting induced by thermal heating or damage to the sample surface.

2.7 Photoluminescence

Photoluminescence is a phenomenon whereby incident light is absorbed by a semiconductor and later released, as illustrated in Fig. 2.23. Photoluminescence will be emitted when there is an electron-hole pair generated by light photon recombination [56].

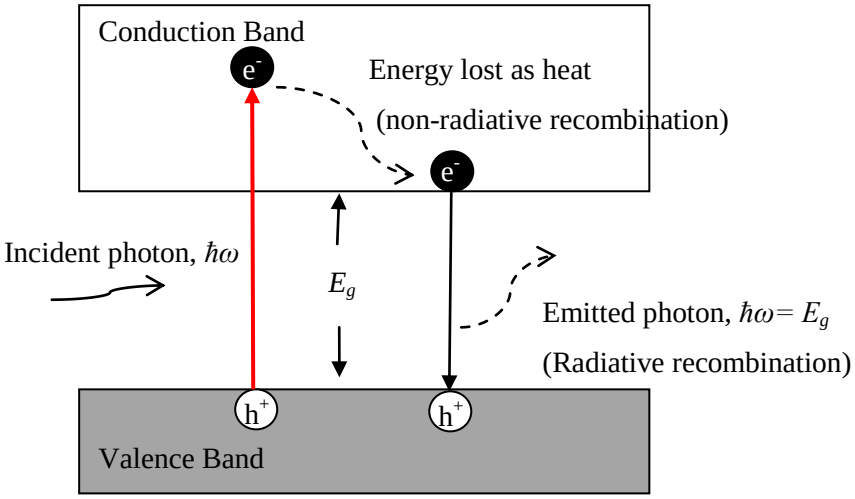


Figure 2.23 Typical mechanism of photoluminescence [56].

An electron-hole (e-h) recombination can occur when the energy of the incident photon, $\hbar\omega$ is equal to or larger than the band gap energy, E_g, of a semiconductor, which excites an electron from the valence band to the conduction band. The electron can lose energy during the transition through non-radiative transitions (a recombination process without releasing photons, where instead one or more phonons are released), or alternatively, the electron could fall from the conduction band into an empty state of the valence band via a radiative transition process, thus emitting a photon of energy $E = E_g$ [56].

The excitation process is nonetheless solely dependent on the type of semiconductor, i.e. whether its bandgap is direct or indirect. For direct bandgaps, an electron at the valence band maximum executes a vertical transition to the conduction band minimum directly

without a change in momentum as shown in Fig. 2.24a), and the energy is conserved according to [56],

$$\hbar\omega = E_f - E_i \tag{2.26}$$

where E_f and E_i are the final and initial state energies, respectively, and $\hbar\omega$ is photon energy. In the case of an indirect bandgap, the electron excitation process requires an additional momentum to reach the conduction band minimum at a non-zero wavevector. It gains this momentum by interacting with a phonon. Then the statement of energy conservation is [56],

$$\hbar\omega = E_f - E_i \pm \hbar\Omega \tag{2.27}$$

where $\hbar\Omega$ is the energy of the phonon or other lattice excitation, and the plus and minus signs correspond to phonon emission or absorption, respectively. Therefore, the efficiency of indirect absorption is much lower than that of direct absorption due to the need for an additional third body interaction with a phonon for indirect absorption.

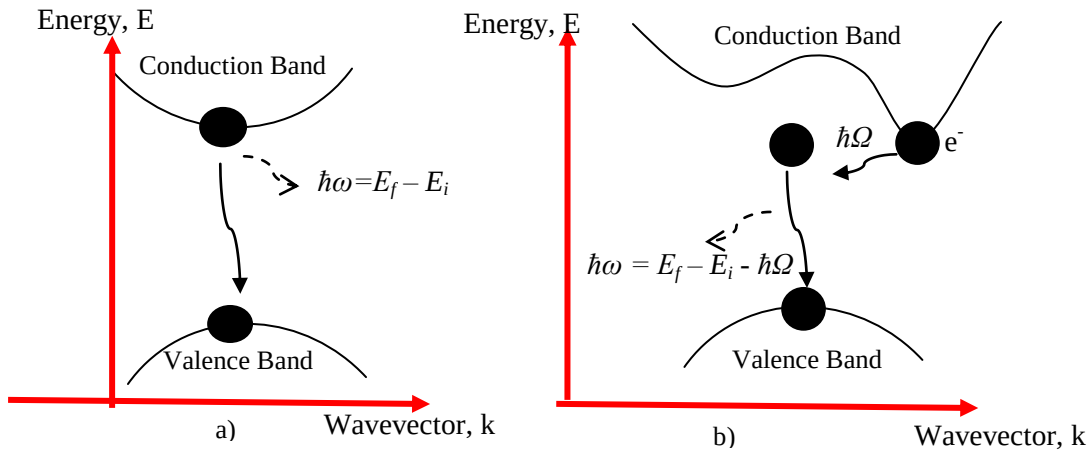


Figure 2.24 Excitation process in a) direct bandgap, and b) indirect bandgap semiconductor plotted as a function of wavevector [56].

2.7.1 Photoluminescence spectroscopy experimental setup

In this work, all photoluminescence spectra were captured at room temperature using a Jobin Yvon Horiba LabRAM 800 spectroscopic system with a 488nm Ar^+ laser, which is the same system as discussed in section 2.6.7. The experiment was carried out under the same instrument geometrical conditions as for micro-Raman spectroscopy, except that the light emitted from the sample under test was recorded as a function of wavelength (nm).

Similar to μ-Raman measurements, calibration is a compulsory step prior to PL measurements. However, only white light was required to calibrate the spectrograph back to zero position as the second step of calibration mentioned in section 2.6.7 was not required for PL measurements. In PL measurements, improper calibrations will lead to errors in recorded peak shifts, and the recorded intensity might be reduced by a few orders of magnitude if the incident beam is out of focus. Therefore, a systematic calibration is a key factor towards reliable, accurate and repeatable results.

2.8 Transmission Electron Microscopy (TEM)

TEM is recognised as a powerful methodology for imaging solid materials at atomic resolution. It is operated analogous to the operation of a light microscope. In contrast to light microscopy, the main strength of TEM is its use of much smaller wavelengths which allows an extremely high-resolution image as small as 0.1 nm to be attained. This has made TEM a vital method in providing valuable data for research in medicine, biology and materials [70].

In micro-structural imaging, various elements within a sample are distinguishable via variations of the image contrast produced by the interaction between the electron beam and the sample [70]. For instance, a heavier element appears darker in a TEM image due to the scattering of the electrons in the sample. Additionally, diffraction contrast introduced by

scattering from crystal planes of a sample comprising of randomly oriented crystals will result a different grey-levels in a TEM image. Consequently, different elements and crystal defects can be resolved unambiguously through the contrast differences from a high resolution TEM image. Apart from that, TEM can also be performed in bright and dark field imaging modes [70]. This has simplified the work for verifying crystal defects, especially defects related to planar defects, stacking faults or particle size.

2.8.1 Experimental geometry of TEM

In this work, cross-sectional TEM images were taken using a 400 kV JEOL JEM 4000 EX instrument with a point resolution of 0.18 nm. All TEM work was carried out by our collaborators led by Dr. Jon Molina at IMDEA, Madrid. Prior to TEM, the cross-sectional specimen was mechanically polished and then thinned to electron transparency using a focused ion beam (FIB) FEI Quanta FEG dual-beam system. Prior to that, the surface was covered with a platinum layer in order to protect the film from the Ga^{+} ion beam during the process of imaging and milling in the FIB. The HR-TEM images were acquired using a Philips Tecnai 20 FEG TEM operated at 200 keV.

Fig. 2.25 shows a schematic diagram of a typical transmission electron microscope. A TEM image was obtained by using a high voltage electron gun. The generated electron beam was focused by a condenser lens onto the electron-transparent specimen. Through the interaction of electrons and specimen, electron diffraction patterns were formed in the back focal plane. Consequently, a magnified image is projected through an electromagnetic lens onto a CCD camera and is viewable from a monitor screen connected to a computer.

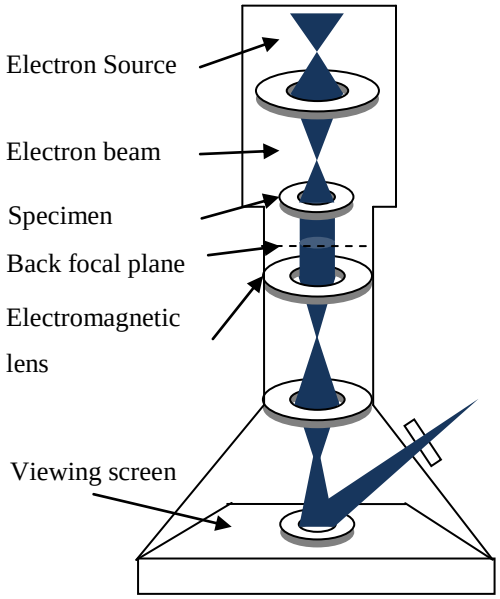


Figure 2.25 Schematic diagram of a transmission electron microscopy [70].

2.9 Atomic force microscopy (AFM)

AFM is a variant of scanning probe microscopy that can provide information on topographical features at resolutions as small as an atomic lattice. Due to the extremely high-resolution demonstrated by AFM, it has been used extensively in imaging, measuring and monitoring the surface morphology of materials. The principle of operation of the AFM is based on attractive or repulsive forces measured between the surface of the specimen and a light, sharp tip attached to a sensitive cantilever, as illustrated in Fig. 2.26 [71]. During the measurements, the sharp tip moves into contact or near-contact with the surface of a specimen, and the interactions between tip and surface cause the cantilever to bend. Bending of the cantilever induces shifting of a probe laser spot and the reflected laser beam is measured by a position-sensitive photodiode detector. The van der Waals force plays an important role in countering any forces that attract the tip to the surface [71]. Any additional forces induced on the tip cause the cantilever to bend rather than forcing the tip against the surface atoms [71]. The deflection as a result of cantilever bends can therefore be used as a

reliable indicator for surface topography. On the other hand, a feedback mechanism is occasionally employed by inducing a constant force between the tip and surface during the measurements. This force is used to adjust the tip-to-surface distance to a constant height to prevent any damage to the specimen surface.

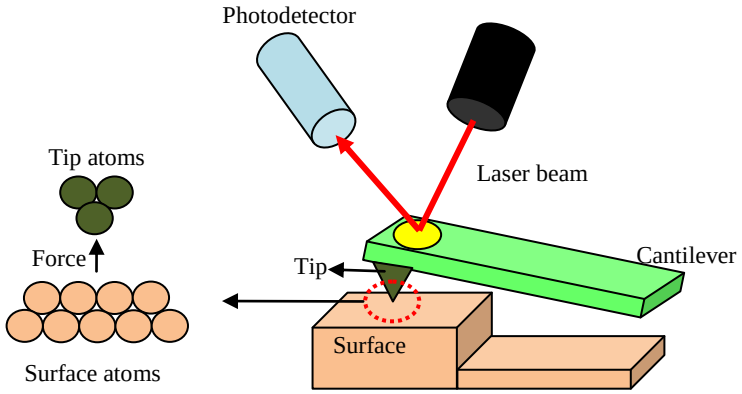


Figure 2.26 Principle of operation of atomic force microscopy (AFM) [71].

All AFM work was carried out by our collaborators led by Dr Paloma Tejedor at CSIC, Madrid. An 5500 Agilent AFM microscope was used to examine the growth morphology of the specimens. Si cantilevers with a nominal radius of 10 nm were used for AFM measurements.

Chapter 3

The challenges facing high quality GaAs heteroepitaxy on Si substrates

3.1 Introduction

Successful heterogeneous integration of GaAs on Si is a target of the electronics industry since compound semiconductors offer a solution to future high speed and low power logic applications. Nevertheless, GaAs epitaxial layers grown directly on Si substrates are typically highly defective (~ 10^8 cm^{-2}) due to their crystal dissimilarity.

This chapter gives the reader an overview of the technological challenges that have to be overcome to realise the successful integration of GaAs on Si substrates. These include the problems due to crystal dissimilarity, existing solutions proposed by various scientists, and the remaining challenges towards the realisation of device quality GaAs materials.

3.2 Difficulties for heteroepitaxial growth of GaAs on Si substrates

The major challenges for the growth of defect-free heteroepitaxial GaAs layers of device quality have been the incompatibility of the polar GaAs compounds and the non-polar substrate (Si or Ge), the thermal expansion coefficient and lattice constant differences between GaAs and Si or Ge, as summarised in Table 3.1 [72]. As a consequence of the technological interest in monolithic integration of GaAs optoelectronics on Si or Ge, some of the problems have now been resolved by great efforts made by scientists. These will be reviewed in the following sections.

Table 3.1 Material parameters for Si, Ge and GaAs [72].

Semiconductor	Lattice Parameter (Å)	Thermal expansion coefficient at 300 K (K^{-1})	Crystal structure
Si	5.4310	2.6×10^{-6}	Diamond cubic
Ge	5.6580	5.9×10^{-6}	Diamond cubic
GaAs	5.6533	5.7×10^{-6}	Zincblende

3.2.1 Incompatibility of the polar/non-polar substrate

A typical polar III-V compound semiconductor comprises of two (or more) elements from group III and group V of the periodic table. Each of these atoms of different elements orientates in the crystal structure of the compound material in a particular sub-lattice [72]. As a consequence of the distinct polarities carried by the group III element and group V elements that occupy the sub-lattices, the overall semiconductor lattice possesses an ionic character. Conversely, a semiconductor containing only one type of elemental atom is a non-polar material. In this case, both of the sub-lattices of the crystal structure are occupied by the same atoms, and thus, result in no charge difference between the atomic bonding as they are neutralised by the adjacent atoms that possess the same charge distributions and bonding symmetries. The dissimilarities in polarity have hampered the integration of III-V compound semiconductors onto non-polar material substrates, and result in the structural defects known as antiphase boundaries (APBs) [18, 73-75].

Due to the fact that GaAs and Si have a face-centred-cubic (fcc) crystal structure, they comprise of two fcc sub-lattices. One of the fcc sub-lattices is offset with respect to the other by half the diagonal of the fcc cube [18, 73]. For elemental semiconductors like Si or Ge, both of the sub-lattices are occupied by the same atoms, and thus it is invariant to a rotation of 90^0 and the [110] and $[\bar{1}10]$ directions are indistinguishable (see Fig. 3.1a)). Conversely, [110] and $[\bar{1}10]$ directions in GaAs are crystallographically dissimilar, as each

fcc lattice is filled by Ga and As, respectively [18, 73]. During heteroepitaxial growth of GaAs on Si or Ge, the Ga and As atoms may preferentially grow on the (001) surface with either the [110] or [$\bar{1}$10] direction parallel with one of the [110] direction in the substrate. That means a Ga and As monolayer may initially form at certain areas of the Si or Ge substrate. At a later stage, arsenic-arsenic (As-As) or gallium-gallium (Ga-Ga) bonds form when two such orientated grains coalesce, which is illustrated in Fig. 3.1 b)i). These bond boundaries are antiphase boundaries. Alternatively, APBs could be formed by the presence of monolayer-high steps on the (001) surface. These monolayer steps lead to a perturbation of the order of the (001) planes as shown in Fig. 3.1 b)ii). It is important to eliminate the APBs because they are typically one of the major concerns impacting the deterioration of electronic and optical properties of GaAs devices [18, 73-75].

Great strides have been made by various scientists in resolving the problems of anti-phase domains (APD), and ultimately, APDs appearing in GaAs epilayers on Si [18, 76, 77] or Ge [78-80] substrates. Successful APD suppression has resulted from using either Ga or As pre-layers and tilted substrates together with an optimised substrate preparation in order to get a clean double-step surface. This technique includes selection of appropriate pre-exposure of either Ga or As for a precise time in order to ensure uniform coverage of the surface by a monolayer, while a tilted substrate is used to provide double-layer high steps. In addition, Noge *et al.* have reported an alternative way to create a double-step surface for growing APB-free GaAs epilayers on exact (001) substrate surfaces, which is by pre-heating the substrate at 1000^{o}C under ultra-high vacuum ambient for 30 minutes [81]. This method is however shown experimentally [76] to generate a much higher dislocation density in the epilayer compared to that of misoriented substrates.

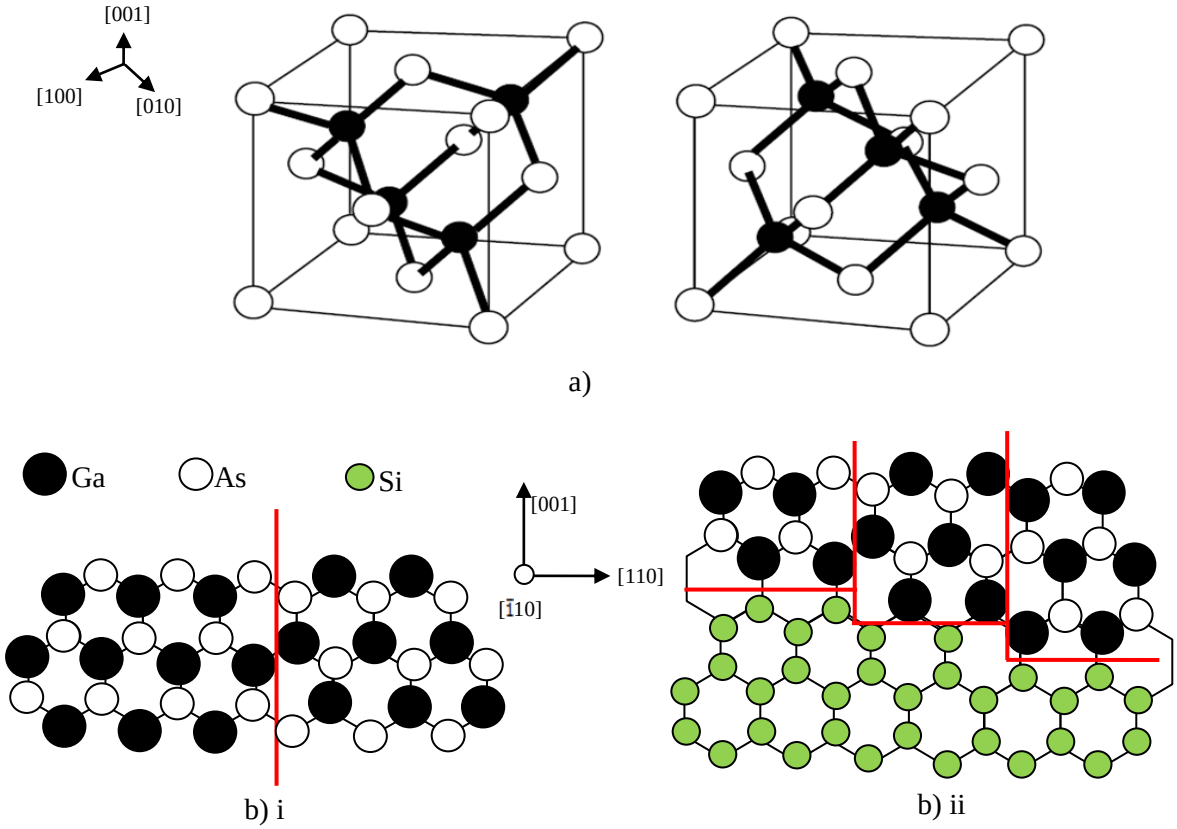


Figure 3.1 a) The two possible orientations of the GaAs zincblende unit cell, and b) Schematic diagram of APB formation in GaAs grown on Si. (i) APBs form due to non-uniform coverage of pre-monolayer, and (ii) APBs appear due to the presence of monolayer high steps as a result of non-uniform pre-monolayer [18, 73-75].

3.2.2 The discrepancy of the thermal expansion coefficients

Apart from the aforementioned problem, another issue of concern is the difference in the thermal expansion coefficients between III-V compound semiconductors and elemental semiconductors, especially between GaAs and Si, where the discrepancy is as large as 60%. Problems arise after the growth of the GaAs layer, upon cooling down from the elevated growth temperature to room temperature. This is because GaAs (larger thermal expansion

coefficient) grown lattice matched to a Si substrate will shrink faster upon cooling, thus resulting in tensile thermal strains in the III-IV epilayers. These residual strains typically lead to the generation of additional dislocations, bending and cracking in the epilayer [76, 82].

Concerning the generation of thermal strains, they can happen in two distinct circumstances. Firstly, if the epilayer is partially relaxed at the elevated temperature during the growing process, it will experience a transition from compressive to tensile strains at a certain epilayer thickess. This transition is nonetheless dependent on the growth temperature and annealing process. For instance, the thickness of the transition for GaAs and InP could vary from 0.1 μm to 1 μm as reviewed by Asai *et al*. and Yamamoto *et al*. [83, 84], respectively. Secondly, if the epilayer is fully relaxed at the growth temperature or annealing temperature, T_g, it will not experience plastic deformation during the cooling process; instead, the thermal misfit $f(m.th)$ will commence generation only at room temperature (RT) and can be represented by [84]

$$f(m.th) = \left(\propto_{th,III-V} - \propto_{th,Si}\right)(T_g - RT) \qquad 4.1$$

where $\left(\propto_{th,III-V} - \propto_{th,Si}\right)$ is the thermal coefficient mismatch between the III-V semiconductor and the Si substrate. As reported by Carlin *et al.* [21], the critical cracking thickness as a result of thermal strain in typical GaAs epilayers on Si is approximately 3-5 μm and preferentially forms in the [110] directions with a crack spacing of < 200 μm.

Several remedies have been proposed in order to reduce the generation of thermal strains in the GaAs epilayer. These including slow cooling rates [79], growth of the epilayer on reduced areas, which allows the growth of a crack-free epilayer [85] and neutralising the tensile strains generated during the cooling process by deliberately induced compressive strain [76].

3.2.3 Lattice mismatch

The major challenge still lies in the large lattice mismatch between the GaAs material and the Si substrate. Comparing their lattice constants, the discrepancies are 4.1% and 0.1% between GaAs and Si and Ge, respectively. Thus the integration of GaAs semiconductors on Si materials is much more challenging than for Ge materials. It is possible to pseudomorphically grow GaAs compound epilayers on Si or Ge substrates provided that the thickness of the epilayer is considerably small - which means keeping the epilayer below the critical thickness. Considering a lattice mismatched system, the misfit strain generated between an epilayer with lattice constant a_f deposited on a substrate with lattice constant of a_s can be defined by [86]

$$f = \frac{a_f - a_s}{a_s} \qquad 4.2$$

If a thin epilayer of larger lattice constant is pseudomorphically grown on a substrate with a smaller lattice constant, the in-place lattice constant of the epilayer will be compressively strained by the substrate. Alternatively, the in-plane lattice constant of the epilayer will be tetragonally tensile strained by the substrate when its lattice constant is smaller. In both cases, the in-plane lattice constants of the overlayer will shrink or stretch in order to match the substrate lattice constants, while the out-of-plane lattice constants change at the same time depending on the type and the amount of strain remaining in the film [82, 86-88]. However, the epilayer will begin to relax when it reaches a certain thickness, as shown in Fig. 3.2. At this point, the misfit strain generated at the interface now exceeds the elastic strength of the coherent semiconductor-semiconductor bonds. Meanwhile, the atomic bonds at the interface between two materials begin to break and ultimately lead to formation of structural defects in the GaAs layer. These broken bonds can be depicted as a one-

dimensional line of broken atomic bonds, which are known as misfit dislocations [82, 86-88], as illustrated in Fig. 3.2.

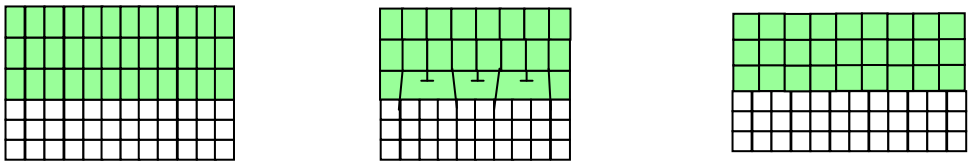


Figure 3.2 Schematic diagram of a) epilayer fully matched to substrate, b) epilayer somewhat relaxed, and c) epilayer fully relaxed.

There are two commonly occurring circumstances that lead to the generation of misfit dislocations [82, 86-88]. They are schematically represented in Fig. 3.3. In the first case, the misfit dislocations originate from a dislocation half-loop that nucleates at the surface and expands towards the interface between the epilayer and the substrate at a later stage. Considering the second case, the existing threading segments at the interface propagate towards the top surface and generate the misfit dislocations.

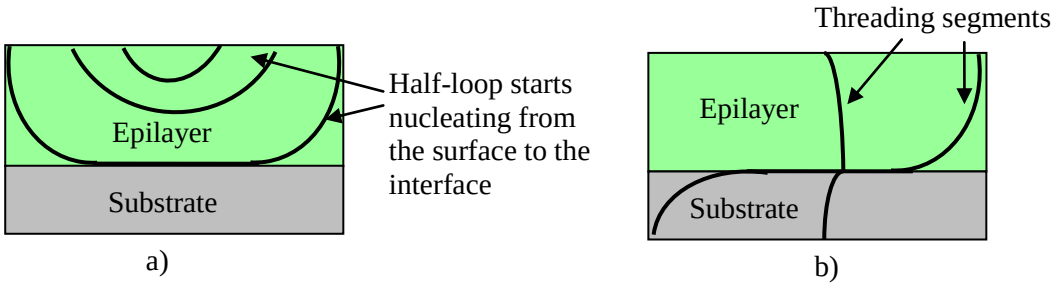


Figure 3.3 Process of misfit dislocation generation. a) the half-loop forms at the surface and expands toward the interface, and b) by threading segments [82, 86-88].

During the direct growth of GaAs material on Si substrates, large defect densities (a combination of misfit and threading dislocations) are generated in the epitaxial layers as a consequence of the significant lattice mismatch. For instance, direct growth of GaAs on Si has typically resulted in misfit defect densities of > $10^9 cm^{-2}$ [18, 89].

So far numerous approaches and solutions have been reported by various scientists in order to address the problems of highly defective heteroepitaxy. To this author's knowledge, these include the use of composition-graded [20, 21] and strained interlayers (InGaAs, Ge, SiGe and $SrTiO_3$) [21, 22, 25, 90] as a buffer layer. Other approaches include thermal cyclic annealing (TCA) [91, 92] and selective area growth on patterned substrates [25, 77, 93], using either molecular beam epitaxy (MBE) or metal-organic vapour phase epitaxy (MOVPE) for III-V epilayer growth. These have successfully brought the defect densities down to as low as 10^5 cm^{-2}. Table 3.2 summarises the contribution of various authors in defect density reduction.

Table 3.2 Numerous approaches have been reported by various scientists in order to address the problems of highly defective heteroepitaxy.

Growth method	**Buffer layer**	**Defect density (cm^{-2})**	**Ref.**
LP-MOVPE and TCA	Single strained InGaAs	$1.2x10^6$	[20]
MBE and TCA	Graded Ge/SiGe	$1x10^6$	[21]
MBE	$SrTiO_3$	$<1x10^5$	[90]
MBE	Ge	$<5x10^5$	[22]
MBE	Ge/SiGe/nanostructured Si	$<6x10^5$	[25]
MOVPE and TCA	a-GaAs/a-Si	$<1x10^6$	[91]
MOVPE	-	$5x10^8$	[92]
MBE	Relaxed Ge layers	$<1x10^7$	[94]
MBE	Graded Ge buffers	$8x10^8$	[95]

Nevertheless, the solution of using a thick buffer layer is not usually cost effective and thermal cycle annealing might deteriorate adjacent devices previously fabricated on the Si substrate. This still remains an immense challenge in using GaAs material on Si to fabricate CMOS devices because the tolerance to dislocations is very low (at most 10^4-10^5cm^{-2}) [18].

3.3 Defect density reduction via epitaxial lateral overgrowth (ELO)

A promising method for defect density reduction is to use lateral overgrowth of III-V compounds on partially masked substrates. In this method, the epitaxial layer is selectively grown on a partially masked substrate [89].

Zytkiewicz *et al.* has demonstrated the ELO growth of low-defect density GaAs layers on silicon substrates by liquid phase epitaxy (LPE). Fig. 3.4 shows a cross-sectional TEM image of the LPE ELO GaAs/Si growth system [96]. The width and thickness of the ELO layers grown are 85 μm and 11 μm, respectively. As expected, the GaAs buffer layer grown directly on a Si substrate exhibited very high dislocation densities, ~ 10^8 cm^{-2}. In contrast, the dislocation densities generated within the ELO layer are greatly reduced, especially on the laterally grown ELO 'wings'. Nevertheless, there are small numbers of dislocations still propagating from the seeding area of the buffer layer and spreading only in a small region throughout the ELO layer as illustrated in Fig. 3.4. They are defined as '60^o-type' dislocations due to their inclination to the interface. This implies the importance of keeping the thickness as low as possible in order to achieve a defect free ELO layer as 60^o-type dislocations are likely to propagate more widely as the layer thickness is increased [97]

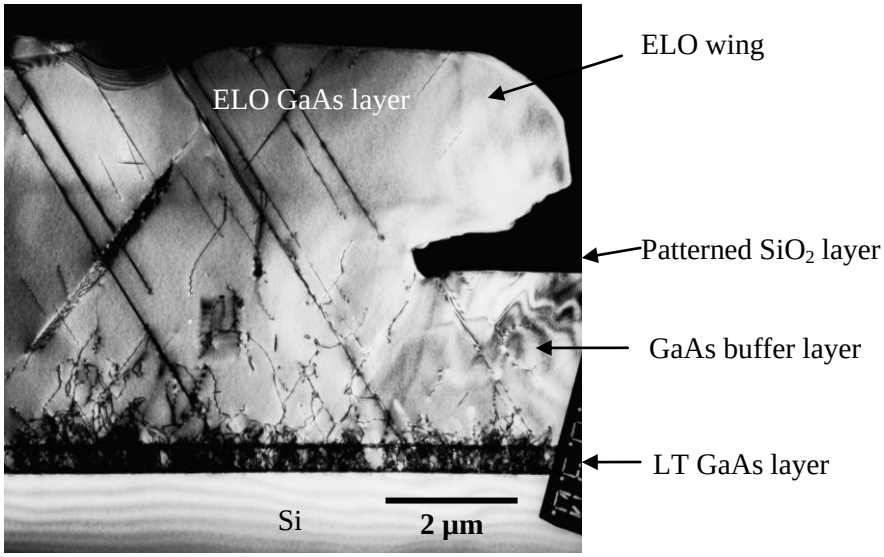


Figure 3.4 Cross-sectional TEM image of LPE grown GaAs on Si ELO structure. The sample comprises a thin GaAs layer grown at low temperature (LT), 2µm MBE GaAs buffer layer and GaAs ELO layer on Si (001) substrate. Threading dislocations propagated from the mask-free area through the top ELO GaAs layer, while the laterally grown ELO parts ("wings") contain a much lower dislocation density [96].

In addition, similar phenomenona have been reported for ELO growth of other semiconductor materials. For instance, Nakamura *et al.* [98] has demonstrated a multi-quantum well InGaN/GaN laser diode fabricated using ELO growth on a GaN/sapphire substrate. This ELO-based laser diode is capable of surviving more than 1000 hr [98] in favorable comparison to the conventional InGaN/GaN/sapphire laser which possesses only a 300 hr life-time [99]. The significant improvement was solely due to the drastic reduction of threshold current density of the devices built on low defect density ELO-based substrates. All these outcomes have shown the potential of ELO technology as an option in developing high performance semiconductor devices containing lattice mismatched epitaxial structures.

3.3.1 Further defect density reduction by nanoscale ELO structures

ELO structures have greatly improved the material quality of lattice-mismatched systems by reducing the dislocation density to the range 10^5-10^6 cm^{-2}. However, this is still not ideal for fabricating CMOS devices as the tolerance to dislocations is even lower ($<10^5$ cm^{-2}). Therefore, further reduction of the dislocation density is necessary, and this has been theoretically and practically predicted as being achievable by extending the ELO technology to the nanoscale [28, 93, 100, 101].

Fig. 3.5a)-b) show cross-sectional schematic diagrams of the conventional ELO structure on a micron-scale masked substrate and a nanometre scale masked substrate, respectively. Reductions of defect density (to $< 10^5$ cm^{-2}) is likely to be achievable by nanoscale ELO structuring, as the nanoscale masks act more effectively at pinning interfaces for the annihilation of structural defects present at the GaAs/Si interface [28, 93, 100, 101]. To date, this mechanism has been identified as being responsible for the improvement in material quality.

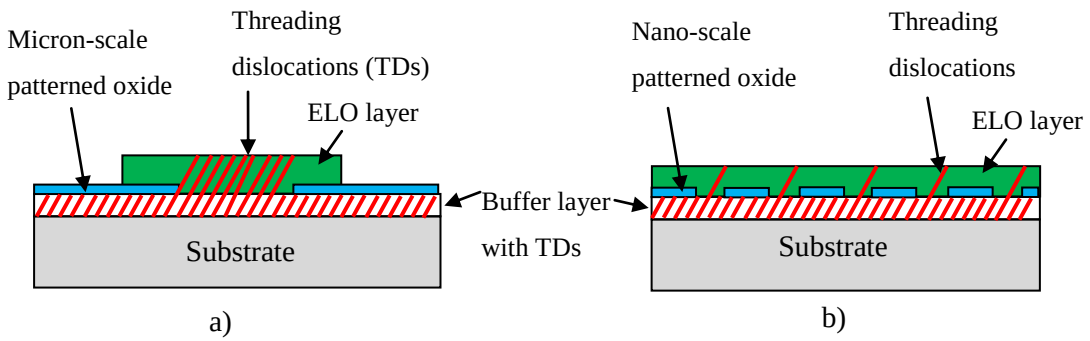
For instance, a relatively low defect density GaAs heteroepitaxy has been reported using this approach by Chao *et al.*, for the selective growth of GaAs on Si substrates using a nanostructured SiO_2 mask [5, 102, 103]. As shown in Fig. 3.5c), the nanoscale masks can act more effectively as a barrier to block the dislocations from propagating towards the surface and this has successfully reduced the defect density of the GaAs overlayer to 3.3×10^5 cm^{-2} [103]. This achievement has shown the potential of this technique for the realisation of high quality GaAs on Si for next generation of commercial semiconductor industry devices. However, the challenges still remain to further optimise the ELO growth process in order to further reduce the defect density to $< 10^5$ cm^{-2} for device applications. That said there are remaining technological challenges that need to be overcome. The main challenges are identified to be [104-107]:

i) The necessity of the deposition of a good GaAs buffer layer on Si as a substrate for subsequent ELO experiments. This is because the quality of the selective lateral grown epitaxial will be greatly affected by what it is grown upon. Therefore, an APD-free and low dislocation density GaAs/Si material will be required [104].

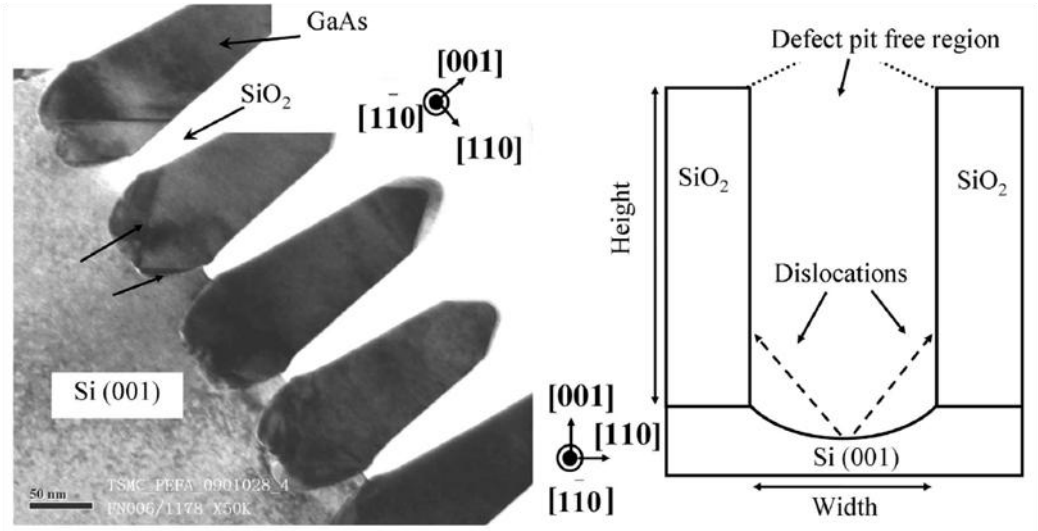
ii) The complete elimination of coalescence defects. This happens when the adjacent laterally grown ELO stripes coalesce, and this leads to lattice misorientation and stress at the coalesced regions [104, 105].

iii) Investigation and reduction of the crystallographic tilt in the ELO layer due the patterned oxide masks. This crystallographic tilt can cause the ELO layer to bend, leading to a non-uniform distribution of strain across the overlayer [106, 107].

With so many diverse challenges to the realisation of high quality ELO GaAs materials, the selection of appropriate characterisation techniques is an essential first step to identify the sources of defect generation or significant effects of each growth step (i.e. growth and annealing temperatures, Ga/As flux ratios and layer thickness), towards the successful realisation of this technique. Therefore, the first aim of this thesis is to demonstrate how the targeted non-destructive X-ray characterisation routine shown in Fig. 1.7 can be used to effectively tackle different issues associated with heteroepitaxial growth and provides useful feedback to III-V to help optimise optimal growth processes. This will be discussed in the following Chapter 4.



a) b)



c)

Figure 3.5 Schematic diagram of III-V layer by epitaxial lateral overgrowth (ELO) on a a) micron-scale patterned oxide, b) nano-scale patterned oxide. Defectivity in the laterally grown III-V layer reduces by extending the ELO approach to the nanoscale and c) Cross-sectional TEM images of GaAs/Si grown in trenches, showing dislocation blocking at the epitaxial layer [5, 102, 103].

Chapter 4

Characterisation of MOVPE-Grown GaAs on Ge or Si substrates

4.1 Introduction

As previously discussed in Chapter 3, the most common problems that are encountered during the hetero-integration of GaAs materials lattice matched to Si substrates have been anti-phase domains, dislocations, strain and lattice tilt distributed within the GaAs layers due to crystal dissimilarities. This chapter has the preliminary aim to demonstrate the capability of the X-ray characterisation routine shown in Fig. 1.7 in examining/identifying various issues associated with heteroepitaxial growth.

In the work presented here, all GaAs materials were grown and provided by collaborators from Instituto de Ciencia de Materiales de Madrid (ICMM-CSIC), Spain. These GaAs materials have been exposed to distinct growth conditions in order to fabricate a series of samples with different defects (strain relaxation, dislocations, antiphase domains, lattice tilt), following advice from the experienced growers at CSIC. These 'problematic' GaAs materials (see Fig. 4.1) were used to demonstrate the capability of the X-ray characterisation routine in evaluating different defects present in the heteroepitaxial grown GaAs materials, as well as identifying significant effects attributable to each growth process.

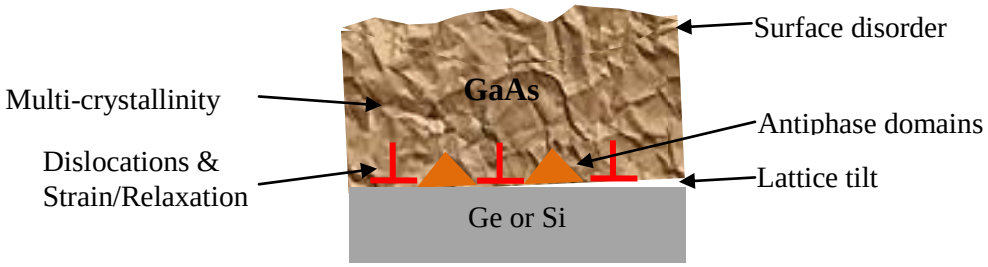


Figure 4.1 Schematic diagram demonstrating different defects appearing in a GaAs heteroepitaxial layer.

4.2 Growth of GaAs heteroepitaxial layers

In order to produce a series of suitable GaAs materials for the purpose of this work, both Ge and Si substrates were used. A series of GaAs/Ge samples with different defects were fabricated by modifying the growth routines that have been previously reported by Galiana *et al*. [108]. Ge substrstes were used due to the relatively small 0.1% lattice mismatch in GaAs on Ge (compared to a 4.1 % lattice mismatch between GaAs and Si), therefore the growth is more controllable.

For comparison, a GaAs/Si sample was also prepared using a similar growth routine. The direct epitaxy of GaAs material on a Si substrate is expected to be much more defective ($> 10^6\,cm^{-2}$) relative to that of growth on Ge substrates. This is due mainly to the larger 4.1% lattice mismatch between GaAs and Si, which corresponds to a critical thickness for strain relaxation of ~ 1 nm [109], and a large density of dislocations is generated upon exceeding the critical thickness. These GaAs heteroepitaxial layers (including both GaAs/Ge and GaAs/Si samples) will serve as a comprehensive set of GaAs materials with different defects or defect densities to test the capability of the characterisation routine shown in Fig. 1.7 in tackling different problems associated with heteroepitaxial growth of III-V materials.

4.2.1 Growth of GaAs/Ge samples

In this work, GaAs/Ge samples were fabricated in a 2" AIX200/4 horizontal metal-organic vapour phase epitaxy (MOVPE) reactor chamber. The MOVPE growth process took place at a pressure of 100 mbar and with a total flow of 14 slpm of palladium-purified hydrogen (as a carrier gas), using arsine (AsH_3) and tri-methyl-gallium (TMGa) precursors, which are the most commonly used group III and V precursors in MOVPE for growing an un-doped GaAs epilayer [86]. The growth of GaAs materials is formed through the surface

reaction between gases transported from sources containing the required chemical elements, as shown in Fig. 4.2.

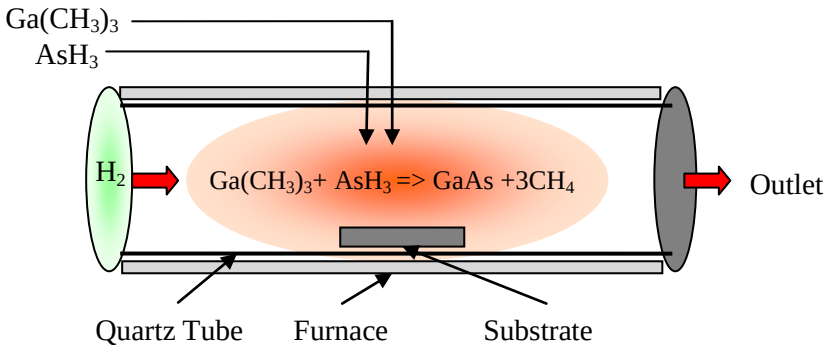


Figure 4.2 Schematic diagram of an arsine (AsH_3) and tri-methyl-gallium (TMGa) precursor MOVPE reactor. A GaAs epilayer is grown via the chemical reaction between the gases from the two precursors [86].

A misoriented Ge wafer, i.e. [001] tilted 6º towards [110] was created by annealing the Ge substrate at a temperature of 700ºC in nitrogen for 30 mins [110]. The Ge substrate was then exposed to arsine (AsH_3) for 900 s at a temperature of 640ºC in order to deposit an arsenic monolayer across the Ge surface. An arsenic monolayer was chosen because of the tendency of As to self-terminate with monolayer coverage on the Ge substrate [111, 112]. This misoriented substrate together with an As monolayer is vital to produce a double-step single-domain surface to suppress the formation of APDs at the GaAs/Ge interface [113, 114].

Concerning the growth of the GaAs epilayer, the selection of an appropriate V/III ratio is relatively important to ensure a high quality nucleation layer. It has been reported that GaAs nucleation using an extremely high V/III flux ratio results in an As-rich film with excessive Ga vacancies that lead to a high densities of defects at the interface. Similarly, high

densities of misfit/threading dislocations are generated at the GaAs interface grown with a relatively low V/III flux ratio [115].

In this experiment, a 50 nm thick GaAs nucleation layer was deposited at a growth temperature of 500ºC under an arsenic/gallium (V/III) flux ratio of 120 [116-118]. This low temperature nucleation, together with the As pre-layer, has been demonstrated by Galiana *et al*. to effectively suppress the formation of APDs at the interface [119].

Although, the low temperature GaAs nucleation at 500°C is helpful in resolving the aforementioned problems, the resulting layer quality is generally unsuitable for device applications. Indeed, it has been reported that MOVPE-grown GaAs layers have a narrow optimal growth temperature within a range from 620 – 680°C [118, 120]. Therefore, a growth temperature at 640ºC was chosen to grow a GaAs buffer layer using a V/III flux ratio of 55, which subsequently formed a double-step growth. Once the growth temperature is beyond 620°C, it is important to keep the V/III flux ratio ~60 in order to achieve a good surface morphology[121].

Five different GaAs/Ge samples were grown (following advice from the collaborator from Spain), namely (i) Ge substrate annealed at a high temperature (700^{o}C), in order to create a double step surface; (ii) an As layer pre-deposition, to achieve a single-domain surface; (iii) a GaAs nucleation layer with a thickness of 50 nm grown at a temperature of 500^{o}C ; and (iv) a GaAs layer of 600 nm grown at a higher temperature (640^{o}C). A set of GaAs/Ge samples - 1) sample A, grown omitting steps (ii) and (iii), i.e. a GaAs layer grown at 640^{o}C just after the Ge substrate annealing at 700^{o}C in H_2; (2) sample B, grown omitting the low temperature nucleation layer and (3) sample C, grown using the full routine. In addition samples D and E were grown in the same way as sample B, but in each case a thicker GaAs overlayer was produced (see Table 4.1).

Table 4.1 Growth parameters for GaAs/Ge samples A-E.

Sample	***High temp annealing at 700ºC***	***As pre-deposition at 640ºC***	***Low temp (500ºC) GaAs nucleation thickness (nm)***	***High temp (640ºC) GaAs buffer thickness (nm)***
A	Yes	No	-	600 ± 10
B	Yes	Yes	-	600 ± 10
C	Yes	Yes	50 ± 10	600 ± 10
D	Yes	Yes	-	800 ± 10
E	Yes	Yes	-	1000 ± 10

4.2.2 Growth of a GaAs/Si sample

In addition to the large lattice mismatch, the existence of a native oxide (SiO_2) on the Si surface can complicate the growth process for GaAs/Si, as a totally clean Si surface is mandatory to ensure a high quality GaAs layer. In the case of improper cleaning, the residue of silicon dioxide (SiO_2) on the Si surface can lead to a polycrystalline GaAs layer [122].

Several methods have been implemented for Si surface cleaning; these include wet-chemical processing with hydrofluoric acid (HF) to dissolve SiO_2 [123] followed by annealing at a temperature of about 950°C under H_2 flow in an MOVPE reactor [124], or thermal absorption in an MBE chamber at a temperature of 900°C [125]. Using atomic hydrogen in an MBE chamber at lower temperature is a feasible alternative for substrate cleaning, which has demonstrated its superior capability for Si substrates [126, 127].

Misoriented Si substrates, i.e. [001] tilted 4º towards [110] were used in these experiments. They were first cleaned in a VARIAN-360 MBE system using atomic hydrogen irradiation at a substrate temperature of 630 ºC at a background pressure of 10^{-6} Torr (high vacuum and impurity free ambient) for 45 min prior to epitaxial deposition. This atomic hydrogen was generated by dissociation of H_2 gas at a W filament (1800ºC) in a home-built cracker cell working at an acceleration voltage of 2.5 kV and ionisation currents in the 30-35

mA range. *Ex situ* cleaning by atomic hydrogen in an MBE system was chosen due to the restriction of the MOVPE reactor which uses conventional halogen lamps. These are not able to elevate the temperature to 950°C for thermal desorption of the native oxide.

After *ex situ* cleaning in the MBE chamber, the silicon substrate was transported into the MOVPE reactor (previously used to grow GaAs/Ge materials). The Si substrate was annealed at a temperature of 735°C, followed by annealing in AsH_3 at 500°C in order to create a double-step surface with single domain As-As dimers for growing an APD-free epilayer [128]. Ultimately, a GaAs nucleation layer was deposited using a growth temperature of 500°C, using same growth parameters previously used for deposition on Ge substrates, as illustrated in Fig. 4.3 below. For GaAs/Si samples, the deposition temperature was kept low at 500°C in order to prevent the generation of additional cracks or dislocations due to the 60% thermal expansion coefficient mismatch upon cooling down the epilayer from elevated growth temperatures [86].

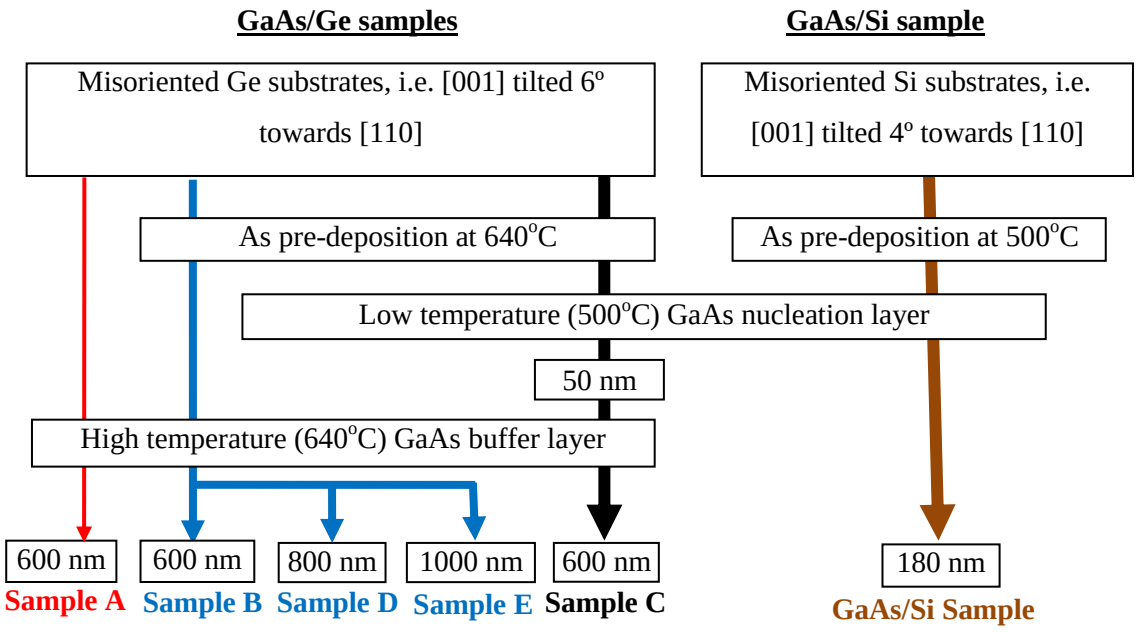


Figure 4.3 Flow diagram illustrating the growth stages for GaAs/Ge or Si samples, respectively.

4.3 Evaluation of the dislocation density by SXRT

These GaAs heteroepitaxy layers were first analysed using SXRT to reveal the type and extent of dislocations formed at the GaAs overlayer interfaces. Fig. 4.4 shows the $\bar{1}\bar{1}7$ large-area back reflection topographs (LABRTs) for GaAs/Ge samples A – E and the GaAs/Si sample, respectively. The projection of the diffraction vector, $\vec{g}$, of the X-ray beam onto the plane of the recording film is represented by the arrow.

Considering the GaAs/Ge samples, no images of extended linear dislocations are observed in the topograph of sample A (Fig. 4.4a). Conversely, varying densities of misfit dislocation networks are clearly observed in the topographs of the other GaAs/Ge samples. From Fig. 4.4b, sample B appears to be at an early stage of the strain relaxation process, as only a small number of misfit dislocation networks are observed. This is followed in ascending order by samples C-E as the thickness of the GaAs overlayers increases, while for sample A the GaAs layer is likely to be in near perfect registry with the underlying substrate. Comparing the topograph for each of the samples, the critical thickness t_c for misfit dislocation generation is estimated to be ~ 600 nm, which is higher than the theoretically expected value (t_c = 300 nm) according to the Matthew-Blakeslee model [129]. A similar phenomenon has been observed by Knuuttila *et al*. [121], where coherent growth for layer thickness in excess of t_c is achievable by carefully selected growth parameters. Although sample C was grown using different routines compared to that of samples B, D and E, it is also found to be relaxed and contains an intermediate density of misfit dislocations (between B and D). This is thought to be due to the total thickness (650 nm) of sample C exceeding the t_c of ~600 nm when the additional 50 nm thick low temperature GaAs nucleation layer is used prior to the deposition of 600 nm GaAs buffer layer at 640^{o}C. Therefore the epilayer is relaxed.

From the dislocation networks observed in the topographs, the dislocation density (cm^{-2}) of the particular specimen is determinable using equation 2.10, as discussed in section 2.5.5. This method provides a non-destructive way of estimating dislocation densities throughout the entire film without the need for chemical etching of the layer. Analysis reveals the highest dislocation density ($8.9 \pm 0.7 \times 10^5$ cm^{-2}) in the thickest film – sample E, as presented in Table 4.2. Misfit dislocations are generated in samples B - E, once the thickness of the GaAs epilayer exceeds the experimental critical thickness of 600 nm, where they are created to accommodate the ~0.1% lattice mismatch between GaAs and the Ge substrate. From the topographs, there is no signature of threading dislocations being observed, and the observed defect images are thought to be comprised mostly of dislocation networks confined at the regions close to the GaAs/Ge interface.

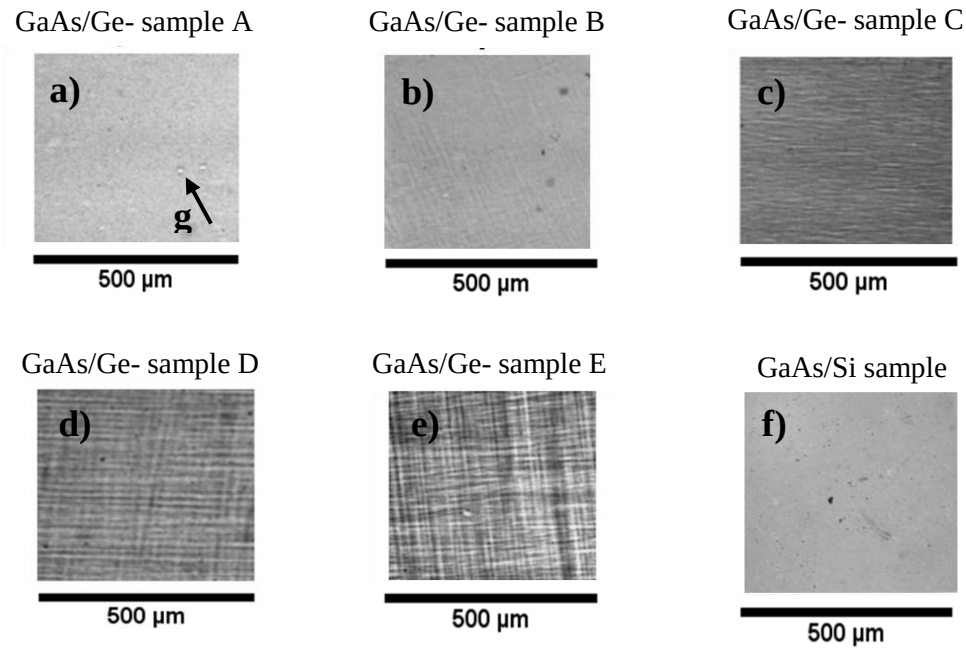


Figure 4.4(a) - (f). $\bar{1}\bar{1}7$ large area back-reflection topographs for GaAs on Ge and Si substrates, respectively. The projection of the diffraction vector, $\vec{g}$, for all topographs is shown in (a).

On first inspection it appears that no individual dislocations are present in the topograph of the GaAs/Si sample (see Fig. 4.4 f), but we must consider the limitation of SXRT spatial resolution (~3 μm), as previously discussed in Chapter 2. When, as is probably the case in this current example, individual dislocation line images are dense, they tend to merge meaning the topographs show only uniform image contrast instead of individual dislocation lines being observed. This implies that the dislocation density in this film exceeds the resolution limit for X-ray topography (i.e. $\sim 10^6/cm^2$). Indeed large densities of dislocations are typically formed in GaAs epilayers that are grown directly on Si substrates which results in a dislocation density of over $10^7 - 10^9 cm^{-2}$ [130], as they are created to accommodate the 4.1% lattice mismatch between the GaAs and silicon substrate. The estimated defect densities for these GaAs heteroepitaxy layers are summarised in Figure. 4.5.

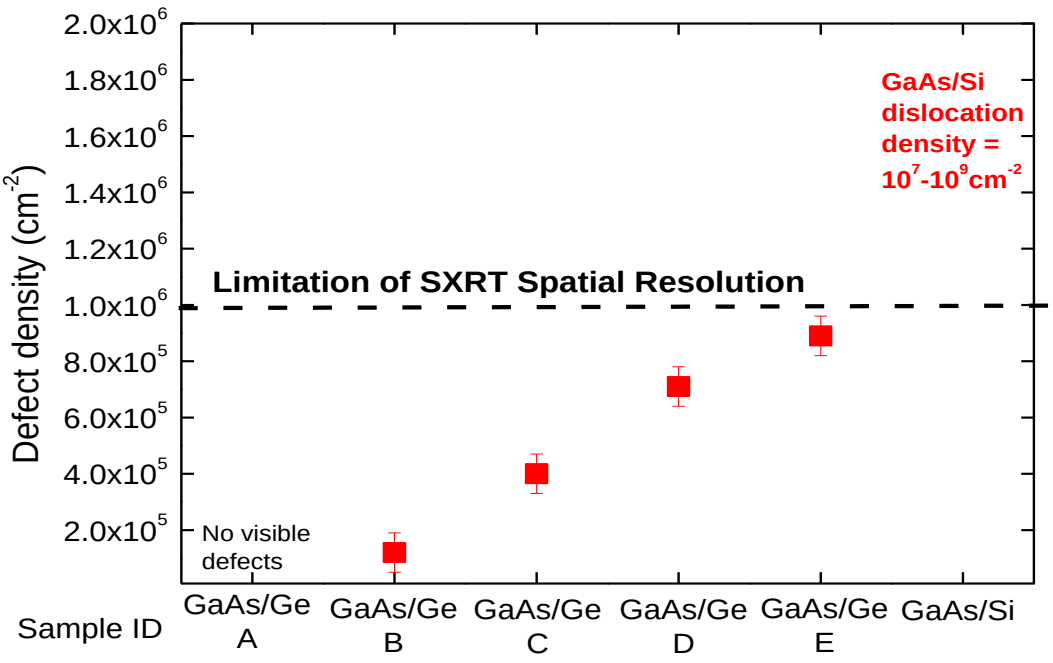


Figure 4.5 Dislocation densities calculated from SXRT for GaAs deposited on Ge and Si substrates. Note that the dislocation density of GaAs/Si sample is an estimated value since no individual dislocations are observed from topograph.

4.4 Evaluation of the strain relaxation process by high-resolution X-ray diffraction (HRXRD).

4.4.1 Preliminary investigation using 004 *ω-2θ* scan

If a GaAs layer is coherently grown onto a Ge or Si substrate, the GaAs material will be tetragonally strained due to the lattice mismatch. Strain changes both the interplanar spacings of the GaAs epilayer and the angles between the reflecting planes ($\Delta\omega$) and the surface, and therefore, leading to the splitting of peak position between GaAs and substrate in the *ω-2θ* scan (see Fig. 4.6). In an *ω-2θ* scan, the angular position of the GaAs overlayer is always measured relative to the substrate peak position located at 0 arc-sec.

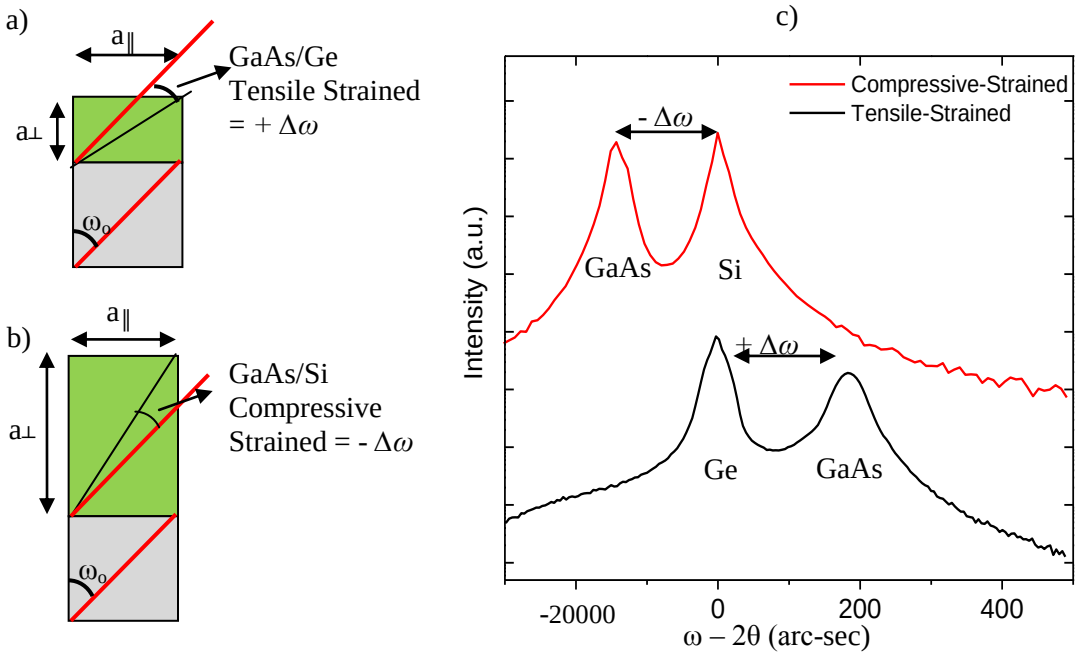


Figure 4.6 A side view of a) tensile strained and b) compressive strained GaAs epilayers. Strain changes both the interplanar spacings of the GaAs epilayer and the angles between the reflecting planes and the surface, and therefore, leading to the splitting of the *ω-2θ* scan, as shown in c). Note that, the x-scale is not symmetrical about 0 arc-sec

These GaAs heteroepitaxy layers were first evaluated by the high-resolution double-axis 004 symmetric *ω-2θ* scans for the preliminary investigation of the crystallinity of these

GaAs overlayers. These scans run in the range from -300 to 500 arc-sec and from -16000 to 2000 arc-sec for GaAs/Ge and GaAs/Si samples, respectively, based on expected peak positions from RADs simulations. From Fig. 4.7a, the double-axis 004 ω-2θ scans for GaAs/Ge samples A-E consistently show an intense GaAs peak located around $\Delta\omega \sim$180 arc-sec. In contrast, a broad (~ 420 arc-sec) and weak intensity GaAs peak is observed around $\Delta\omega \sim$ -5500 arc-sec in the 004 ω-2θ scan of the GaAs/Si sample (see Fig. 4.7b). This peak can be interpreted as being due to diffracted intensities from a mosaic and highly defective GaAs epitaxial layer in which each mosaic region contributing diffracted intensity throughout a particular angular range [131].

The examination of these GaAs heteroepitaial layers was repeated using triple-axis 004 symmetric ω-2θ scans (with an analyser placed before the detector to restrict its angular acceptance) in order to reveal finer details from these materials. Concerning the GaAs/Ge samples A-E (see Fig. 4.7c), it is obvious that Pendellösung fringes are only significant for the thin (600 nm) GaAs/Ge samples A and B. These fringes become indistinguishable for samples C to E as the thickness of these epilayers exceeds the critical thickness of 600 nm. These fringes are formed by the interference effects occurring as a result of an exchange in energy between the forward travelling (incident) X-ray beam and the diffracted beam from the GaAs and Ge layers [132, 133]. The Pendellösung fringes are very sensitive to crystal distortions or crystal defects because crystal defects destroy the perfect periodicity of the crystal lattice, and therefore the fringes disappear [132, 133]. Considering the samples under test, the disappearance of the fringes is typically an indication of the presence of dislocations due to these GaAs layers starting to relax [132-134]. This observation correlates well with the results previously discussed in the SXRT section. However, no GaAs related peak is observed in the triple-axis 004 ω-2θ scan for GaAs/Si sample (see Fig. 4.7d). This is most likely due to the GaAs overlayer of this sample being too defective, and the diffraction intensities from the

highly mosaic crystal structure are typically scattering X-rays at wide angles meaning they are too weak to produce sufficient intensities to pass through the highly restricted angular acceptance angle of the analyser placed before detector for triple-axis measurement. This agrees with the conclusion from SXRT that the GaAs/Si is defective beyond the resolvable SXRT limit.

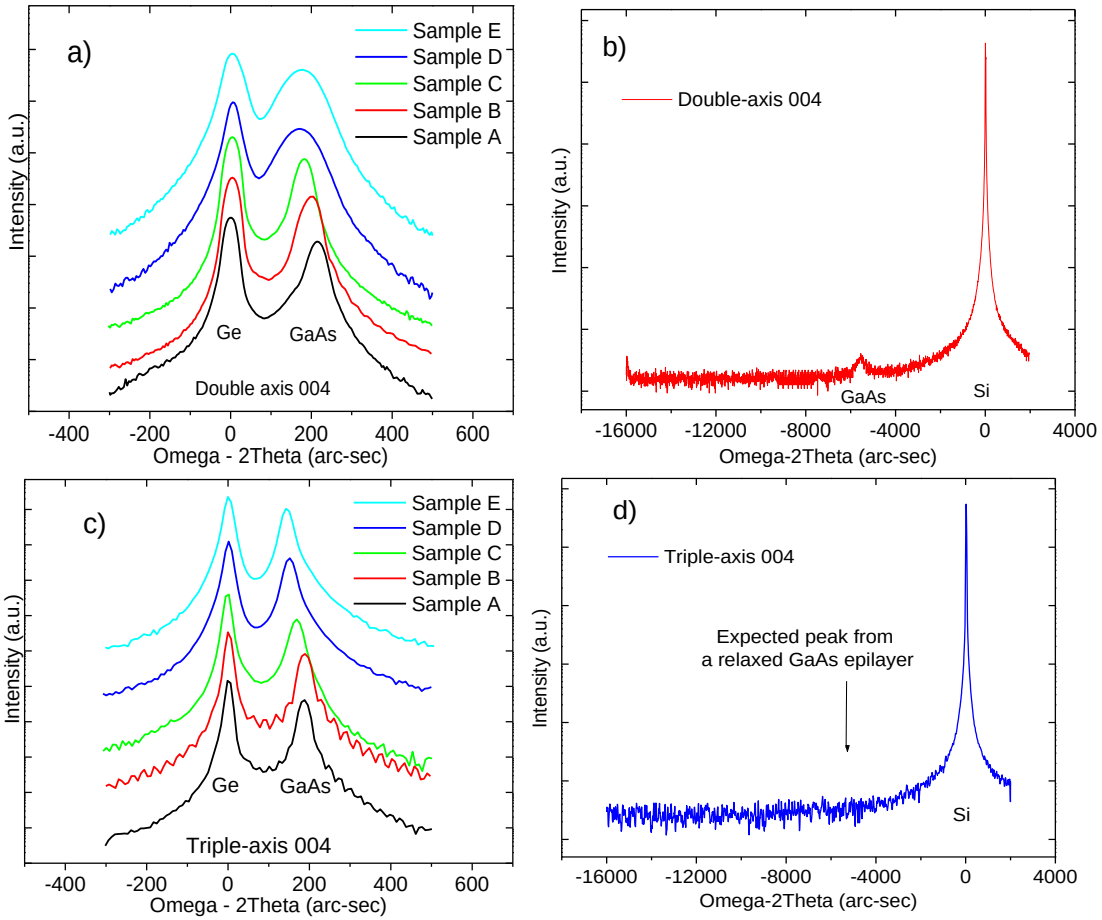


Figure 4.7 a)-b) are the double-axis and c)-d) are the triple-axis 004 ω-2θ scans for GaAs/Ge and GaAs/Si samples, respectively.

4.4.2 Evaluation of degree of relaxation using reciprocal space mapping (RSM)

In order to obtain both the in-plane and perpendicular lattice constants simultaneously, these GaAs heteroepitaxial layers were evaluated using 224 asymmetric RSMs. The degree of relaxation of the GaAs layer was determined by using the average angular peak separations ($\Delta\omega_{average}$) of two RSMs recorded by successive 180° rotations of the sample around the [001] axis. This is important in order to eliminate the tilt [135] thereby ensuring a precise result (see Fig. 4.8). RSM is however inapplicable for the highly defective GaAs/Si sample in this case. Therefore, different characterisation routines were employed for characterising the strain/relaxation and crystallinity for this sample, which will be described in section 4.4.3.

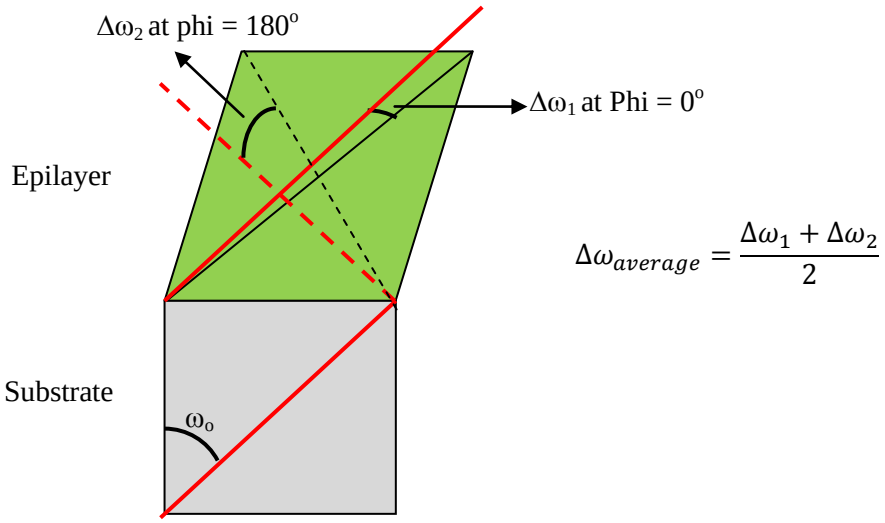


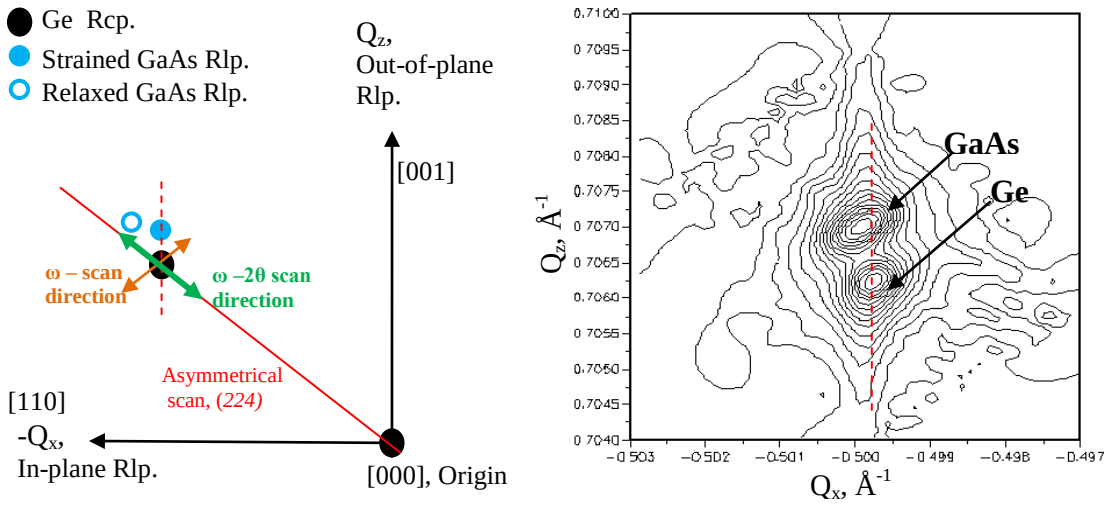
Figure 4.8 Schematic diagram illustrating an epilayer tilted with respect to the substrate. Effect of tilt on the peak splitting between the epilayer and the substrate is reversed if the specimen is rotated by 180° about its surface normal ([001] axis), but the splitting due to the lattice mismatch will not be affected by such a rotation [43].

An RSM can be obtained by collecting a series of triple-axis *ω-2θ* scans recorded across different *ω* offsets, as shown in Fig. 4.9a). Fig. 4.9b) shows the 224 reciprocal space map of sample E, by way of example. When one uses an asymmetric 224 RSM, the lattice

parameter information both in the growth axis [001] and the surface direction [110] are simultaneously recorded. The diffracted intensity contours of the RSM are plotted as a function of reciprocal space axes Q_x and Q_z, where Q_x and Q_z correspond to in-plane and out-of-plane lattice constant of the GaAs epilayer, measured in reciprocal space ($Å^{-1}$). Considering the Q_x axis of sample E, both the GaAs in-plane and out-of-plane lattice points are altered with respect to the degree of relaxation (or strain) associated with the epilayer. From RSM, the extracted Q_x and Q_z positions can be used to calculate the in-plane ($a_{\parallel}$) and out-of-plane ($a_{\perp}$) lattice constants of the GaAs epilayer, which are given by [135]:

$$a_{\parallel} = \sqrt{\frac{h^2 + k^2}{Q_x^2}}, \quad a_{\perp} = \sqrt{\frac{l^2}{Q_z^2}} \qquad 4.3$$

where *h, k, l* are the equal to 224 – the asymmetric reflection order being used.



a) b)

Figure 4.9 a) Schematic diagram illustrating the triple-axis asymmetric *ω*-scans and *ω-2θ* scans in real space, and b) Asymmetric 224 reciprocal space map of sample E . The change in in-plane and out-of-plane lattice constants due to relaxation process alters the position of the reciprocal lattice point (Rlp) in Q_x and Q_z planes, respectively.

The degree of relaxation for samples A - E was calculated using the in-plane lattice constant obtained from equation 4.1 through the following relation [135]:

$$Relaxation, R = \frac{a_{\parallel} - a_{sub}}{a_r - a_{sub}} X100\ \% \qquad 4.4$$

where $a_{\parallel}$, $a_r = 0.56533\, nm$ and $a_{sub} = 0.56575$ are GaAs in-plane lattice constant extracted from RSMs, GaAs lattice constant and substrate lattice constant, respectively. The resulting calculated values (see Table 4.2) correlate well with the dislocation densities estimated from SXRT, in that the degree of relaxation and dislocation density increase in parallel as the layer thickness increases. Fig. 4.10 shows the dislocation densities plotted as a function of in-plane lattice constant for GaAs/Ge samples A-E.

Table 4.2 Degree of relaxation calculated from RSMs and defect densities estimated from SXRT.

Sample ID	***$a_{\parallel}$, in-plane lattice constant calculatedfrom RSMs, nm***	***Degree of relaxation, %***	***Dislocation Density, x10^5cm^{-2}***
A	0.56575	< 1	None visible
B	0.56574	< 2	1.2 ± 0.7
C	0.56569	15	4.0 ±0.7
D	0.56561	33	7.1 ± 0.7
E	0.56555	48	8.9±0.7

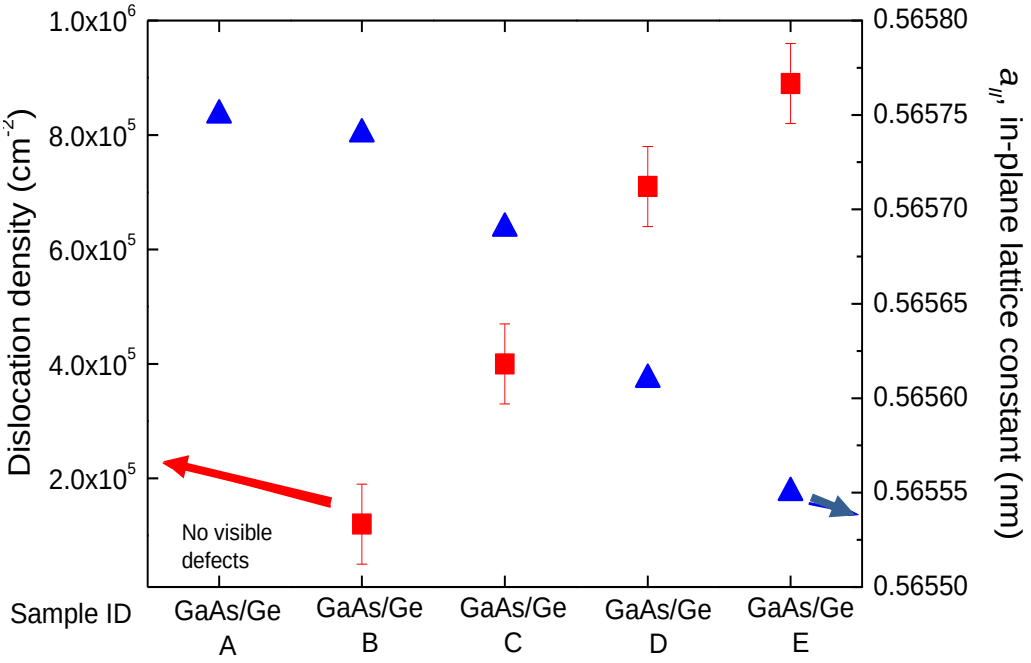


Figure 4.10 Dislocation densities plotted as a function of in-plane lattice constant for GaAs/Ge samples A-E.

Concerning the results presented so far from the GaAs/Ge samples, the use of different nucleation conditions (an As pre-deposition monolayer or the additional low temperature (500°C) deposited GaAs nucleation layer) do not appear to significantly influence the strain relaxation process. In fact, SXRT and 224 RSMs confirm that the overall GaAs overlayer thickness plays the more important role in determining relaxation, as dislocations start forming beyond the critical thickness, and therefore, increase the dislocation densities of the film (see Table 4.2).

4.4.3 Strain/relaxation and crystallinity evaluation of the defective GaAs/Si sample

i) Determination degree of relaxation

As previously discussed, the triple-axis or RSM measurements are inapplicable for the evaluation of relaxation for the GaAs/Si sample due to the defective nature of the GaAs overlayer. Therefore, four pairs of double-axis 004 and 224 ω-2θ scans were repeated by successive 90^{o} rotations of the sample around the [001] axis [46], in order to eliminate the effects of tilt between the epilayer and substrate and the anisotropy of the elastic strain distribution in this highly defective GaAs overlayer. The average angular peak separations were used in estimating the strain/relaxation of the GaAs layer.

Fig. 4.11 shows both the 004 and 224 HR-XRD scans of GaAs/Si sample and the corresponding RADs structural simulations. The GaAs peak located at $\Delta\omega$~-5500 arc-sec of 004 ω-2θ scan corresponds to the GaAs peak located at $\Delta\omega \sim$ -8000 arc-sec in the 224 scan, which is diffracted from fully relaxed epitaxial GaAs material. The shape of the GaAs peak in the 224 scan is asymmetric and thus can be associated with the presence of azimuthal anisotropy of the elastic strain distribution [134]. Table 4.3 shows the structure parameters of this GaAs/Si sample obtained from the RADs simulation. Analysis of the 004 and 224 ω-2θ scans reveals that the epitaxial GaAs is fully relaxed with ~99-100 % relaxation.

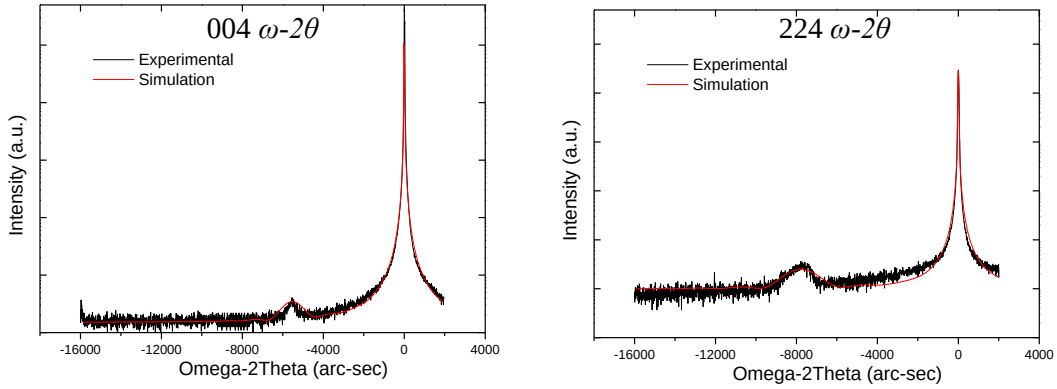


Figure 4.11 Double-axis *ω-2θ* HR-XRD scans and corresponding simulations of GaAs/Si sample.

Table 4.3 Structure parameters of GaAs/Si sample obtained from RADs fitting.

	RADs - HR-XRD	
Geometry of reflection	004	224
Peak Position, arc-sec	-5493	-8041
Thickness of GaAs layer, nm	15	19
Relaxation, %	100	99
Background intensity, cps	1	1
In-plane lattice constant, Å	5.6533	5.6533
Out-of-plane lattice constant, Å	5.6533	5.6533
Type of stress	Relaxed	Relaxed

ii) Polycrystalline X-ray diffraction

In order to confirm the crystallinity of the GaAs/Si sample, the sample was also analysed using polycrystalline XRD. Fig. 4.12 shows the *2θ-ω* X-ray diffraction spectra for the MOVPE-grown sample. The powder diffraction scan for MOVPE-grown GaAs/Si shows evidence of polycrystallinity in this film. GaAs diffraction peaks of the (111), (022), (113) and (004) planes are labelled in Fig. 4.12 [136]. The data clearly show evidence of polycrstallinity in this GaAs overlayer, but at the same time the double-axis HR-XRD measurements have previously confirmed the presence of some relaxed GaAs epitaxial in this GaAs/Si sample. This could imply a circumstance where there is some relaxed epitaxial GaAs

embedded in polycrystalline GaAs material. Therefore, this GaAs/Si sample was further investigated by crystallographic texture mapping to reveal the distribution of crystallographic orientation of this overlayer.

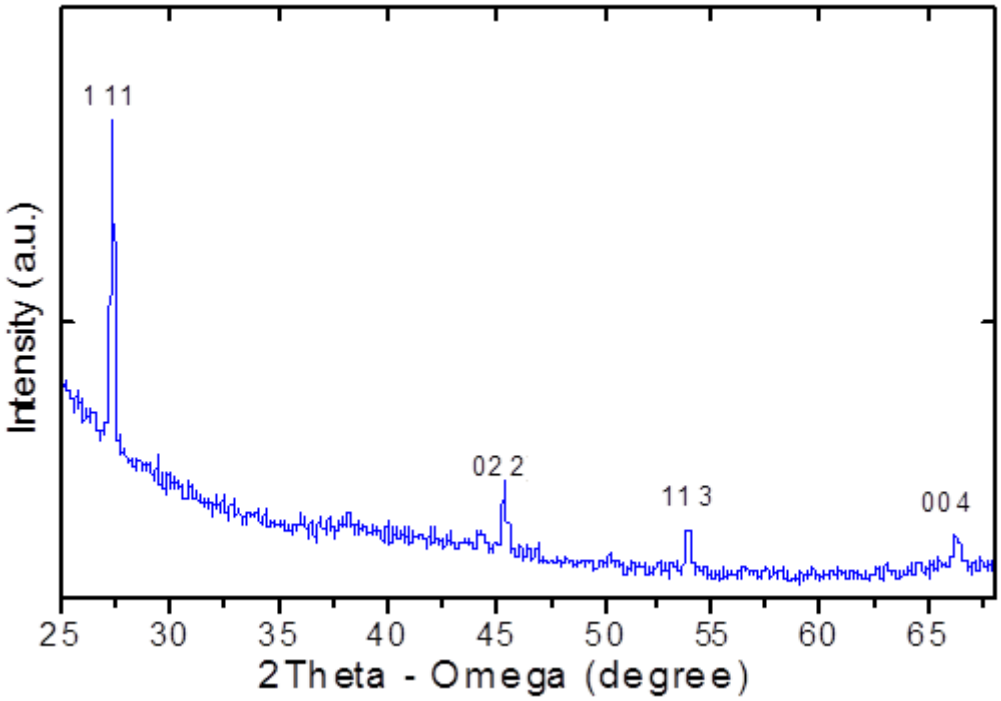


Figure 4.12 *2θ-ω* poly-crystalline XRD measurement for GaAs/Si sample.

iii) Texture analysis by crystallographic texture mapping

A full X-ray pole figure is recorded by rotating the sample for a phi (Φ) range from 0^0 - 360^0 for each incremental value of the chi angle ($\chi = 0^0$- 90^0). Fig. 4.13 shows the {111} pole figure for the GaAs/Si sample recorded using GaAs 111 diffraction angles at 2θ = 27.38º. The {111} pole figure shows the four-fold symmetry peaks located at $\Psi = \sim 54.7$º, which are attributed to epitaxial GaAs orientated to the [001]. However, the peak widths in the pole density distribution are broadened showing that the alignment of the epitaxial grains is not perfect. This is thought to be the signature of misoriented GaAs grains. The misorientation could originate from crystal defects and dislocations generated during growth

[137]. In this case, the crystallites tilt slightly in various directions due to mosaicity or misorientations within the crystal and the four-fold symmetry peaks are broadened. In other words, $\Delta\Psi$ directly reflects the tilt misorientation and $\Delta\Phi$ contains contributions from the tilt and rotational misorientations [138]. For example, if the crystallites completely align to each other, i.e., both tilt (χ) and azimuth (Φ) angles are zero, 4 symmetric points should be expected in the {111} pole figure (see Fig. 4.14 for a {111} pole figure of a bare silicon). One should see likewise for the {111} pole figure for the (001) single crystal.

In addition, a 'ring' contour pattern is observed around the centre in the {111} pole figure. This is attributed to the diffracted intensity collected from highly textured polycrystalline material and it rotates with varying Φ around a centre axis parallel to the substrate normal along [111]. This reveals that, besides the aforementioned epitaxial material, there is some preferentially polycrystalline grain orientated to [111].

There are several peaks with weaker diffraction intensity at $\Psi = \sim 72^0$ (denoted as T_n in Fig. 4.13), in addition to the four-fold symmetry peaks of the epitaxial grains (labelled as A_n in Fig. 4.13). These could result from further epitaxial orientation associations between GaAs and Si. For example, it is well known that twins are commonly formed in zincblende III-V crystals by [5] planes rotating 60^0 around [111]. This consequently leads to the existence of twinning angles $\theta_t = 38.94^0$ and 56.25^0 between certain [111] lattice directions of the two twins [139, 140]. A detailed analysis shows that the orientations of the 8 weaker diffraction intensities denoted as (T_n, n = 1, 2, ... 8) are tilted at $\sim 35^0$ from the high symmetry point. These are within a few degrees of the expected orientations of the {111} poles of the twins generated on epitaxially oriented grains [139-141].

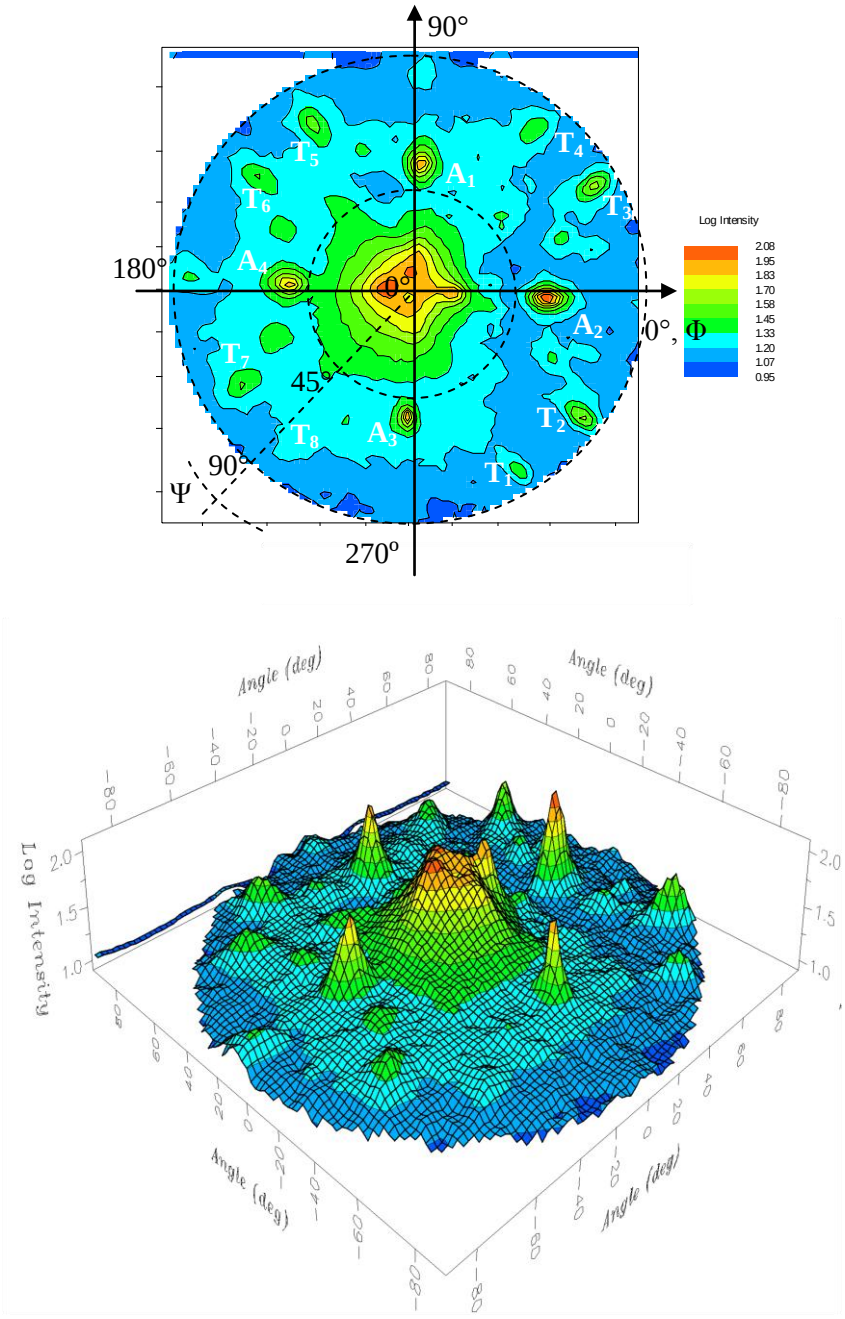


Figure 4.13 GaAs pole plot of GaAs/Si sample for 111 diffraction. Four-fold symmetry of GaAs epitaxial grains is denoted as 'A_n' in the pole figure. 'T_n' refers to diffraction corresponding to twin boundaries.

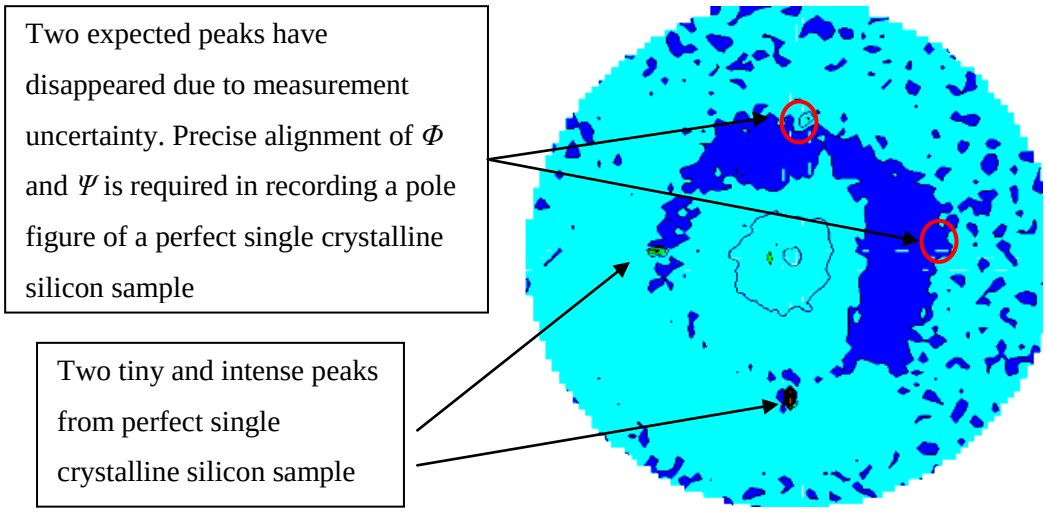


Figure 4.14 Pole plot of bare Si for 111 diffraction.

In order to confirm the results presented in the pole figures section, a series of powder diffraction scans in the experimental range from $2\theta = 26^0$ to 29^0 were recorded. Fig. 4.15 shows the powder diffraction XRD along a "linescan" running from the centre to the edge of the pole figure (chi = 0^0 to 90^0). From the powder diffraction scans, an intense peak located at $2\theta = 27.5^o$ and chi = 55^o has verified the presence of epitaxial GaAs orientated to the [001] direction.

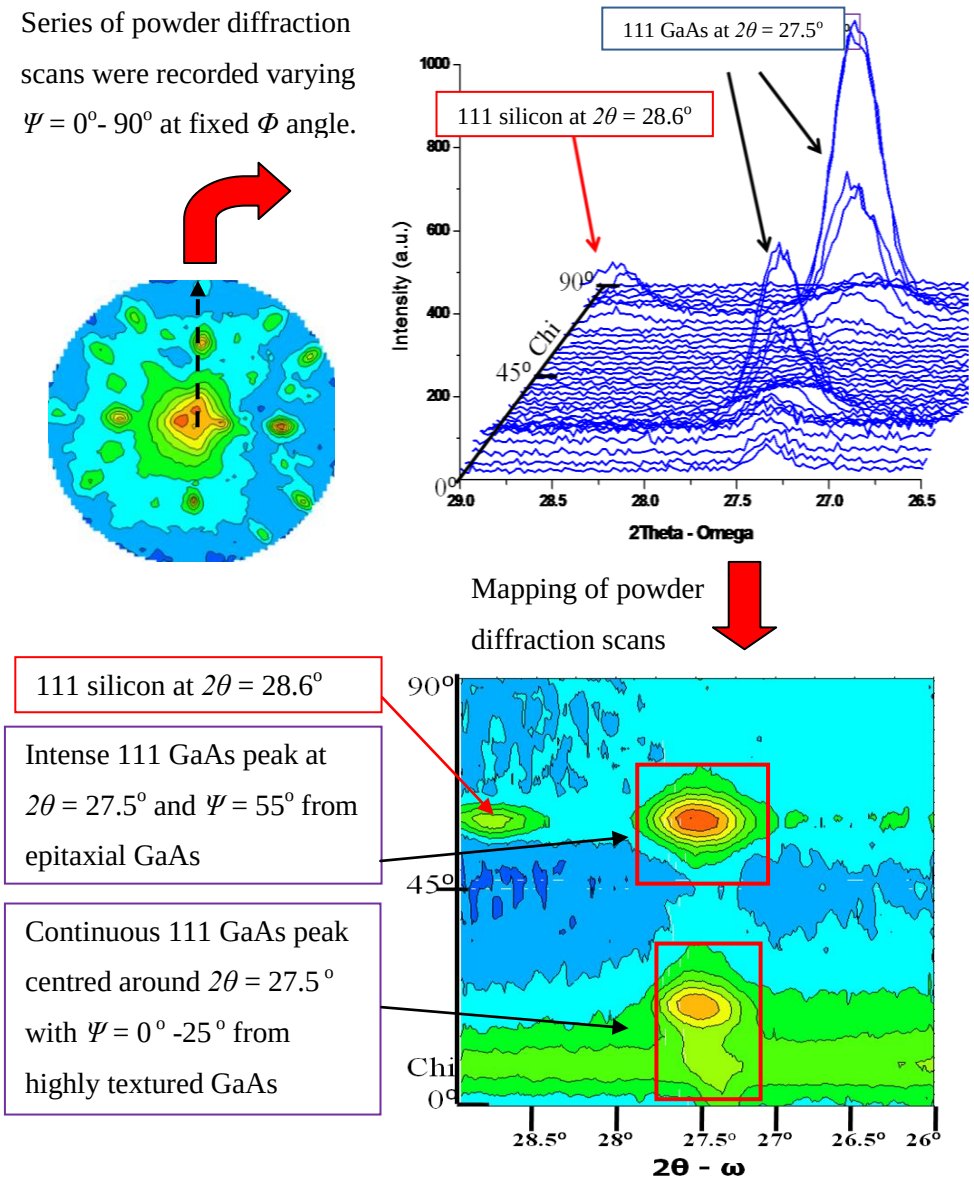


Figure 4.15 A series of powder diffraction scans in the experimental range from $2\theta = 26^0$ to 29^0 were recorded.

Generally, this section has demonstrated the capability of the X-ray diffraction method in evaluating the strain/relaxation in GaAs/Ge and GaAs/Si samples with different crystallinity, fabricated under various growth conditions. Unlike the spatial resolution limitation of SXRT, the resolution or accuracy of the lab-based diffraction tool is limited by the sampling step of 0.003° in both ω and 2θ axes, corresponding in strain sensitivity of ~10^{-5}.

This is the reason why the application ranges of the lab-based XRD tool is not restricted by the defect density of the specimen. Different experimental geometries can be used to perform various types of measurement in order to extract the strain/relaxation or to understand the crystallinity of the GaAs heteroepitaxial layers with different problems. More importantly, this technique is non-invasive, thereby allowing the same sample to be measured a number of times, allowing comprehensive information to be extracted.

4.5 X-ray diffraction investigation of antiphase domains

Antiphase domains are a key concern for GaAs heteroepitaxial layers, so their presence must also be considered. Transmission electron microscopy (TEM) is one of the widely used techniques in revealing and visualising the presence of APDs. Nonetheless, the requirement of destructive sample preparation prior to TEM measurements has made it non-ideal for examining the specimen, as it is excessively time consuming and costly. In contrast, XRD is a non-invasive technique that can be used for non-destructive characterisation of APDs [141-143].

As previously described in Chapter 2, X-ray diffraction occurs when a crystal with (*hkl*) reflecting planes at the correct Bragg angle and the integrated intensity is proportional to $|F_{hkl}|^2$, where F_{hkl} is the structure factor of the relevant crystal plane [41].The structure factor is the summation of all the X-ray scattering strength from each atom (atomic scattering strength, f_n) throughout the whole volume of the crystal [41], in which it is depending on the atomic position of the atoms in the crystal.

For a cubic GaAs crystal, the scattering amplitudes from *00l*-superstructure reflections (l = 2, 6) results from differences in the atomic X-ray scattering strengths ($F_{00l} = 4(f_{Ga} - f_{As}), l = 2, 6$) between the long range ordering of Ga and As atoms in the GaAs

crystals (the relative position between Ga and As atoms). When an APD is present, it disrupts the long range periodic arrangement of the Ga and As atoms where the Ga and As positions are inverted by 180º with respect to adjacent domains, as depicted in Fig. 4.16a). This results in a reduction of the lateral coherence length inside locally ordered GaAs crystal domains of this ordering, and leads to additional broadening of the superstructure reflections [142, 143]. Conversely, the scattering amplitudes of the *00l*-fundamental reflection (l = 4) arise solely from the sum of atomic scattering strengths of Ga and As atoms, $F_{00l} = 4(f_{Ga} + f_{As}), l = 4$ regardless of whether all lattice sites were randomly occupied by either Ga or As atoms [142, 143], and therefore this reflection is not influenced by the presence of APDs.

In reciprocal space, the existence of APDs causes a reciprocal lattice point (Rlp) broadening of the superstructure reflections in the Q_x plane due to small lateral coherence lengths [135, 142, 143]– the distribution of the scattered intensity in a direction parallel to the sample surface (see Fig. 4.16b). In other words, these APD induced Rlp broadenings are directly related to the full width at half maximum (FWHM) of the triple-axis ω-scans performed at superstructure reflections [135, 142, 143]. In addition to the broadening effect due to APD, the mosaic tilt due to the presence of dislocations can also result in Rlp broadening in the Q_x plane [135, 144]. Because the Rlp broadening induced by mosaic tilt is proportional to the reflection order and since the broadening due to small lateral coherence lengths is independent of the reflection order, the superposition of these effects can be separated by performing ω-scans at different reflection orders, and are resolved using a graphical method called the Williamson-Hall (WH) plot [141, 144]. The WH plot is a plot of the FWHM of ω-scans, in reciprocal space units (β ($Sin\theta$)/λ) against the reflection order in reciprocal space units (($Sin\theta$) /λ), where β is the FWHM of the ω-scan, λ is the X-ray wavelength, and 2θ is twice the Bragg angle of the reflection. The WM plot analysis is performed by fitting the data using a linear regression [141, 144]:

$$y = \alpha \cdot x + y_o \qquad 4.5$$

where *y*- and x- coordinates represent the FWHM of the ω-scan and the reflection order in reciprocal space units respectively, α is the mosaic tilt. The intercept of the y-axis (y_0) of the best-fit straight line corresponds to the lateral coherence length ($L_{\parallel} = 0.9/(2y_0)$) of the GaAs crystal [141, 144].

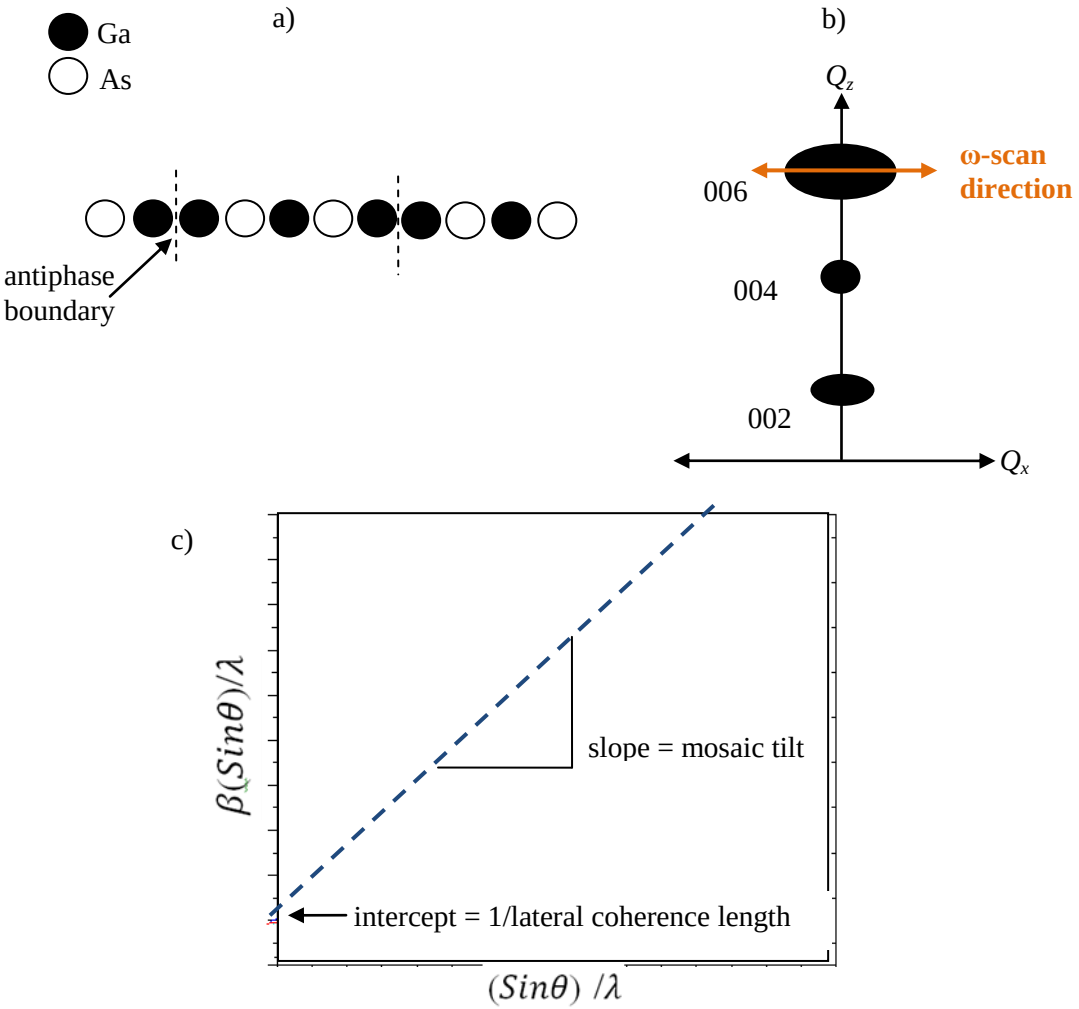


Figure 4.16 a) Schematic diagram illustrating an APD formation in a one-dimensional GaAs crystal, b) APD induced reciprocal lattice broadening of superstructure reflections in Q_x plane [135, 142, 143], and c) Schematic showing a Williamson-Hall plot.

In order to evaluate the presence of APDs, the triple-axis ω-scans were repeated for GaAs/Ge samples A-E, recorded at both *00l*-fundamental reflection (*l* = 4) and *00l*-

superstructure reflections (l = 2, 6). The ω-scan FWHM of each sample was extracted and analysed using WH plots. In this study, the WH plot was used mainly for evaluating the presence of APDs and estimating the $L_{\parallel}$ of the GaAs crystal, and therefore the mosaic tilt is excluded from this discussion. Note that, this method is not applicable to GaAs/Si samples due to the polycrystalline structure of the GaAs overlayer for these samples.

4.5.1 The influence of various growth routines on APD self-annihilation in GaAs/Ge crystals

i) Influence of a low temperature deposited GaAs nucleation layer

Considering samples A-C, growth alterations were employed in order to investigate the effectiveness of growth stages (ii) and (iii) in suppressing the formation of APDs. The WH plot for GaAs/Ge samples A-C is depicted in Fig. 4.17. The best straight-line fit was obtained for sample C, with the other samples consistently showing a selective broadening characteristic for *00l*-superstructure reflections (l = 2, 6). This selective broadening is a signature of the presence of APDs [135, 142, 143] in the GaAs epilayers.

From Fig. 4.17, the evaluation of the WH plot of sample A shows an average APD domain size ($L_{\parallel}$) of 120 ± 20 nm. The selective broadening of the superstructure reflections confirms the presence of APDs in sample A, due most likely to improper GaAs nucleation routines [113, 114, 120], and thus, the estimated $L_{\parallel}$ corresponds to the average domain size of different APDs appearing in GaAs crystals. As growth stage (ii) was introduced for sample B, the WH plot analysis reveals a drastic reduction in average APD size to 21 ± 6 nm. A straight line fit of the WH data points was obtained for sample C when both growth stages (ii) and (iii) were used. This confirms that the sample C was grown under optimised conditions and is either completely APD-free or the APDs in the GaAs crystal have self-annihilated (see Fig. 4.17b) at an early stage of growth [120]. These XRD results clearly highlight the importance

of growth stages (ii) and (iii) for the reduction of the APD size and to a more effective APD self-annihilation routine. Large APDs (120 ± 20 nm) are formed at the heterointerface of sample A due to uncontrolled initial surface nucleation of the GaAs epilayer directly onto the Ge substrate [111-114]. Using just the As pre-deposition (stage ii) does somewhat reduce the domain size by homogenising the Ge surface with As-As dimers to the order of 21 ± 6 nm [111, 112], yet APDs are still significantly present when the low temperature nucleation layer is omitted (stage iii). The implementation of growth stage (iii) could be responsible for the slow initial nucleation growth that allows atomic rearrangements which effectively annihilate APDs, as a large amount of energy is required to form the boundaries between two adjacent domains [142, 145].

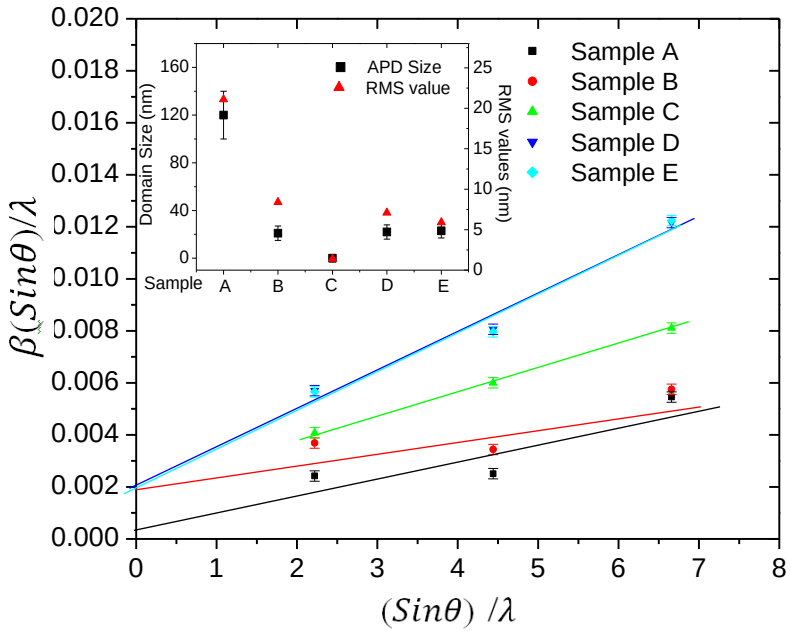


Figure 4.17a) Williamson-Hall plots of GaAs/Ge samples A-E. Inset shows the estimated APD size and RMS roughness values.

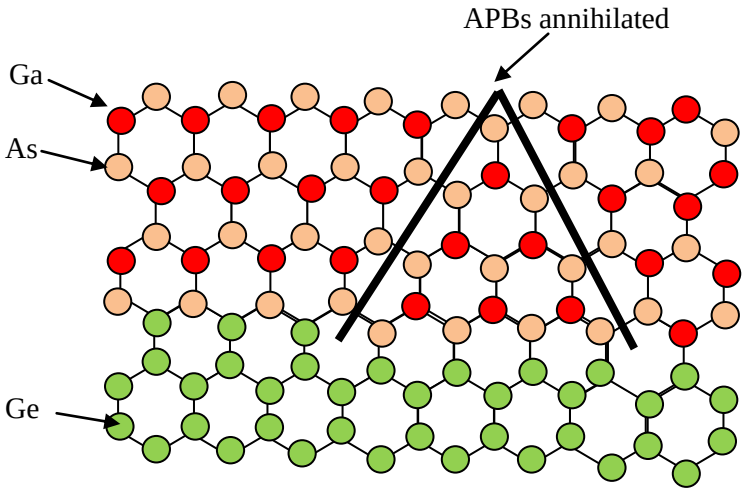


Figure 4.17b) Adjacent APBs of a domain at GaAs/Ge hetero-interface are self-annihilated. Therefore, a small APD size is required in order to annihilate APD at early stage of growth.

In order to monitor how the surface morphology of the GaAs epilayer evolves as the growth conditions vary, these GaAs/Ge films were evaluated using AFM. These measurements were carried out using a Digital Instruments-Multimode IIIa microscope working in tapping mode. Si cantilevers (Veeco) with a nominal radius of 10 nm were used. AFM images with image sizes 5 μm^2 of samples A – E were taken. The features of all images were characterised by cross-section profiles and (root-mean-square RMS roughness) σ values were calculated and are shown inset in each image.

The AFM images for samples A-C are depicted in Figs. 4.18a)-c), respectively. A relatively rough surface morphology has been observed at the GaAs surface of sample A, with valleys of up to 120 nm in depth. The wavy surface morphology is thought to be due to the presence of a high density of APBs in the GaAs layer formed by the co-existence of As-As and Ga-Ga domains, which has been observed by several authors [114, 146, 147]. The low σ value (smoother surface) for sample C confirms the result of the WH analysis, in that this sample is free or nearly-free of APDs or they are self-annihilated, leading to a better surface

morphology [114, 146-148]. In general, the surface roughening of the GaAs buffer layers is highly dependent on the selection of V/III flux ratios, growth temperatures, in addition to the presence of APDs [114, 120, 121, 146-148]. By keeping other growth conditions (i.e. flux ratio and growth temperatures) of the GaAs overlayer the same for samples A-C, it would be reasonable to assume that the surface roughening of the GaAs overlayers is most probably related to the presence of APDs in GaAs crystals. Surface roughening can also be due to the strain relief mechanism of the GaAs epilayer, but this effect is relatively small when compared to that of APDs effect for the samples under test. Our results show that most of the strain is relieved through the generation of misfit-dislocations, that are mostly confined at the near-interface region and do not extend towards the top surface.

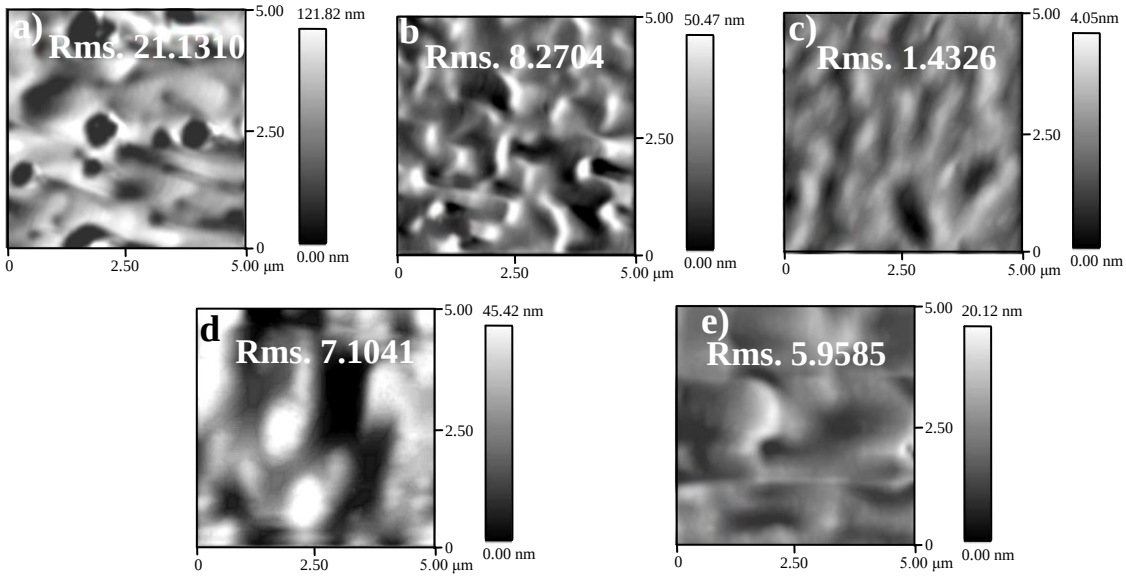


Figure 4.18 (a) - (e). 5 µm x 5 µm AFM topographs for GaAs/Ge samples A - E, respectively.

The existence of APDs was further verified by cross-sectional transmission electron microscopy (X-TEM). In Fig. 4.19a), APDs are clearly observed from the contrast discontinuities of the image at the GaAs/Ge interface for sample A and these APDs are

confined to a region approximately 200 nm from the interface with a domain size of around 100 ± 30 nm and decrease significantly with distance away from the GaAs/Ge interface. The anti-phase boundaries (APBs) of different domains start inclining with adjacent boundaries, and thus, they are self-annihilated [120, 145, 149]. On the other hand, no significant densities of APDs albeit with the presence of a small number of misfit dislocations are observed at the hetero-interface of sample C. These X-TEM observations are in good agreement with and confirm the aforementioned XRD and AFM discussions. Note, that these APDs are of the order of 21-120 nm in size, hence they are too small to be resolved by SXRT.

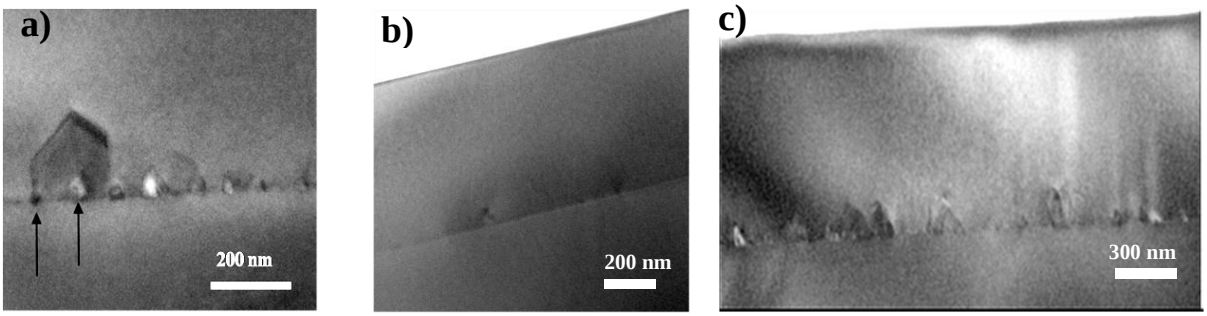


Figure 4.19 (a) - (c). Cross-sectional transmission electron micrographs of samples A, C and E, respectively, demonstrating crystal defects at the GaAs/Ge interface.

ii) Effect of GaAs epilayer thickness

In order to observe how the APDs evolve as the GaAs layer thickness increases, we compared the GaAs epilayer thickness running from 600 nm (sample B) to 800 nm (sample D), through to 1000 nm (sample E). The WH plots of samples B, D and E are depicted in Fig. 4.17. The selective broadening of the superstructure reflections confirm the presence of APDs in these GaAs films. These observed APDs in samples B, D and E are evaluated to be ~ 21-23

± 6 nm in size. This is expected as they were grown using identical growth routines except that a thicker GaAs epilayer was produced.

From the AFM analysis, the surface morphology of these samples is relatively rough due most probably to the presence of APDs in the GaAs crystals [114, 146-148, 150], as shown in Figs. 4.18b), d) and e). The σ value (8.2 nm) of the thin-sample B (600 nm) is high and follows in descending order from sample D and E as the thickness of the GaAs overlayer increases to 800 nm and 1000 nm (7.1 nm and 5.9 nm), respectively. The downward tendency of the σ values might suggest a self-annihilation of APDs with thickness. This is consistent with the observations reported by Li *et al.* [113] and Hudait *et al*. [120], in which the wavy morphology caused by APDs is completely suppressed after the growth of a thick GaAs epilayer.

Fig. 4.19c) shows the cross-sectional TEM image for the 1000 nm thick sample - sample E, demonstrating crystal defects (both APDs and misfit-dislocations) in the GaAs overlayer. From Fig. 4.19c), it appears that the APDs are self-annihilated within a short distance from GaAs/Ge interface, which verifies the aforementioned discussions.

Considering now all five GaAs/Ge samples under test, the results from various characterisation techniques suggest that the generation of APDs gives rise to sample surfaces whose roughness depends on the size of APDs formed at the GaAs/Ge interface. By using a low temperature GaAs nucleation layer and/or a high temperature GaAs epilayer, the results show that most of the APDs are annihilated and do not extend to the free-surface. Nonetheless, the formation of large APDs seems to significantly distort the surface morphology of the subsequently grown GaAs buffer layers. The inset of Fig. 4.17 depicts a clear correlation between these two parameters for samples A-E. Comparing the AFM and XRD results for samples A-E, one can confirm the direct correspondence of the surface roughening to the different size of APDs formed at the GaAs/Ge interface. Therefore, it is

important to annihilate the APDs as early as possible during the growth since this results in a relatively small σ of ~1.4 nm (sample C).

4.5.2 Interaction between misfit dislocations and antiphase boundaries

These findings highlight the importance of using a range of techniques to analyse heteroepitaxial layers where both dislocations and APDs are important considerations. For example, sample A, for which SXRT and 224 RSM measurements show to be dislocation-free and fully matched to Ge substrate, is shown to contain an abundance of large APDs when investigated with *00l*-reflection (l = 2, 4, 6) ω-scans and TEM. Conversely sample B (same thickness), which contains smaller APDs, is found to be at the early stages of the strain relaxation process. This observation implies a strong interaction between APBs and dislocations. Similar observations have been shown by Ringel *et al.* [151] in the GaAs/Ge material system grown by migration enhanced epitaxy, although in that reference the causes were not explained.

This anti-correlation between the density of APDs and the density of dislocations suggests that the APBs of different domains might act to block the formation of misfit dislocations. In general the formation of a dislocation through the strain relaxation process requires the lattice of the GaAs crystal to move by an extra half plane of atoms by the Peierls-Nabarro (PN) driving force [152]. According to this model, the magnitude of the PN driving force is closely related to the width of the dislocation (W), which increases as W decreases as given by the following relation [152]:

$$\tau_{PN} \propto Ge^{-2\pi W/b} \qquad 4.6$$

where G is the shear modulus and b is the Burgers vector of the dislocation.$W = a/(1-v)$, where a is the interplanar spacing and v is the Poisson's ratio. From the PN model analysis,

the strong interaction between APBs and dislocations observed in sample A can be explained by a mechanism where APBs are responsible for the cessation of dislocation propagation by reducing the width of the dislocation. This is because the bonding forces of As-As or Ga-Ga bonds near to the APBs are highly directional, and therefore the dislocation width is narrow and the Peierls stress is accordingly large [152, 153]. Nonetheless, as the APDs size reduces from 100 nm to 25 nm for sample B, APDs no longer act effectively to block the propagation of misfit dislocations, and therefore, the epilayer starts to relax.

Table 4.4 a) Growth parameters, and b) AFM σ value and average APDs size for GaAs/Ge samples A-E, respectively.

a) Growth details				***b) AFM and APDs size***	
Sample	***As pre-deposition at 640°C***	***Low temp (500°C) GaAs nucleation thickness, nm***	***High temp (640°C) GaAs buffer thickness, nm***	***Root-mean-square roughness, nm***	***Average APDs size, nm***
A	No	-	600 ± 10	21.1 ± 5	120± 20
B	Yes	-	600 ± 10	8.2 ± 1	21± 6
C	Yes	50 ± 10	600 ± 10	1.4 ± 0.2	-
D	Yes	-	800 ± 10	7.1 ± 1	22± 6
E	Yes	-	1000 ± 10	5.9 ± 1	23± 6

4.6 Investigation of crystallographic tilt in GaAs heteroeptiaxy layers

The use of a misoriented substrate is vital to produce a double-step surface in order to suppress the formation of APDs at the GaAs on Ge or Si interface. However, the misoriented substrate always induced additional tilt into the overlayer subsequently grown upon it [154]. In addition, the dislocations developed during the strain relaxation process can also induce crystallographic tilt [154]. In order to observe the mechanism of crystallographic tilt as a function of relaxation degree in the GaAs/Ge samples, these samples were further evaluated

using two pairs of double-axis 004 ω-2θ scans recorded by successive 180^o rotations of the sample around the [001] axis. It is important to run the measurements in double-axis geometry (with open detector) for tilt analysis in order to obtain the effective displacement of the layer.

Two pairs of 004 ω-2θ scans have been repeated for both the X-ray incident direction perpendicular and parallel to the misoriented direction of the substrate in order to examine the tilt angle ($\Delta\alpha$) in both [110] and [$\bar{1}$10] directions, respectively. If the epilayer is tilted with respect to the substrate, the angular separation ($\Delta\omega$) between the GaAs and Ge peak positions recorded at each azimuth angle will vary according to the magnitude of tilt associated with the film. The tilt angle for samples A-E was calculated from each of two pairs of 004 ω-2θ scans measured in the X-ray incident direction perpendicular ($\Delta\alpha_{\perp}$) and parallel ($\Delta\alpha_{II}$) to the misoriented direction of the substrate using the following equation [154, 155]:

$$\Delta\alpha_{\perp} = \frac{\Delta\omega_{270^o} - \Delta\omega_{90^o}}{2}, \Delta\alpha_{\parallel} = \frac{\Delta\omega_{180^o} - \Delta\omega_{0^o}}{2} \qquad 4.7$$

where $\Delta\omega_{270^o} - \Delta\omega_{90^o}$ and $\Delta\omega_{180^o} - \Delta\omega_{0^o}$ are the differences in diffraction angles between GaAs and Ge diffraction measured in opposite directions for both [110] and [$\bar{1}$10] directions, respectively. Fig. 4.20 shows the 004 ω-2θ scans of sample E measured at four different azimuth angles. The variation of angular displacement between the GaAs and Ge peak indicates the presence of tilt.

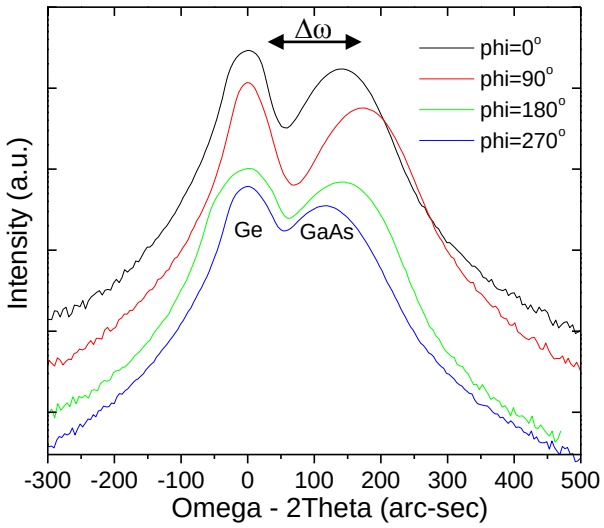


Figure 4.20 Double-axis 004 ω-2θ scans of GaAs/Ge sample E recorded at four azimuthal angles of 0°, 90°, 180° and 270°.

The tilt angle for all the GaAs/Ge samples A-E in both [110] and $[\bar{1}10]$ directions are calculated and depicted in Fig. 4.21. The relaxation data for each sample obtained from section 4.4.2 is included in Fig. 4.20 for comparison. Calculation reveals approximately zero tilt angle in the $[\bar{1}10]$ direction. In contrast, the GaAs epilayers of samples A-C are titled by about -0.0066^0 to -0.0093^0 (-24 to -34 arc-sec) measured in the [110] direction when the degree of relaxation is smaller than 15 %. The negative sign of tilt indicates that these epilayers are tilted towards the [110] direction due to the tensile strained GaAs over layers grown on miscut Ge substrates. However, as the degree of relaxation increases beyond 30% for samples D and E, the GaAs epilayers are titled by 0.0046^o (17 arc-sec) and 0.0086^o (31 arc-sec), respectively, toward the $[\bar{1}\bar{1}0]$ direction, i.e. the opposite direction to the tilt direction of the samples A-C. This reflects a mechanism wherein the crystallographic tilt is

highly dependent on the process of lattice relaxation. The experimental measured tilt angles are compared to that of theoretically calculated tilt according to Nagai's model [155]:

$$\Delta\alpha = tan^{-1}\left(\frac{a_{\perp} - a_{Ge}}{a_{Ge}}\right) tan\ \varphi$$

where $a_{\perp}$ and a_{Ge} are the measured out-of-plane lattice constant of GaAs from 224 RSMs and bulk Ge lattice constant, respectively, while φ is the miscut angle of the substrate.

Considering case 1 (lattice matched or slightly relaxed samples A-C), the crystallographic tilt can be explained by the model proposed by Nagai [155]. According to his model, when an epilayer is pseudomorphically grown with respect to the underlying misoriented substrate the lattice parameters of the overlayer are simultaneously strained in both horizontal and vertical directions. In this case, the out-of-plane lattice parameter of the overlayer is fully registered to the step sites on the surface of the misoriented substrate, and results in crystallographic tilt in the epilayer away from the surface normal (see Fig. 4.22). Base on Nagai's model, the crystallographic tilt in samples A-C can thus be explained.

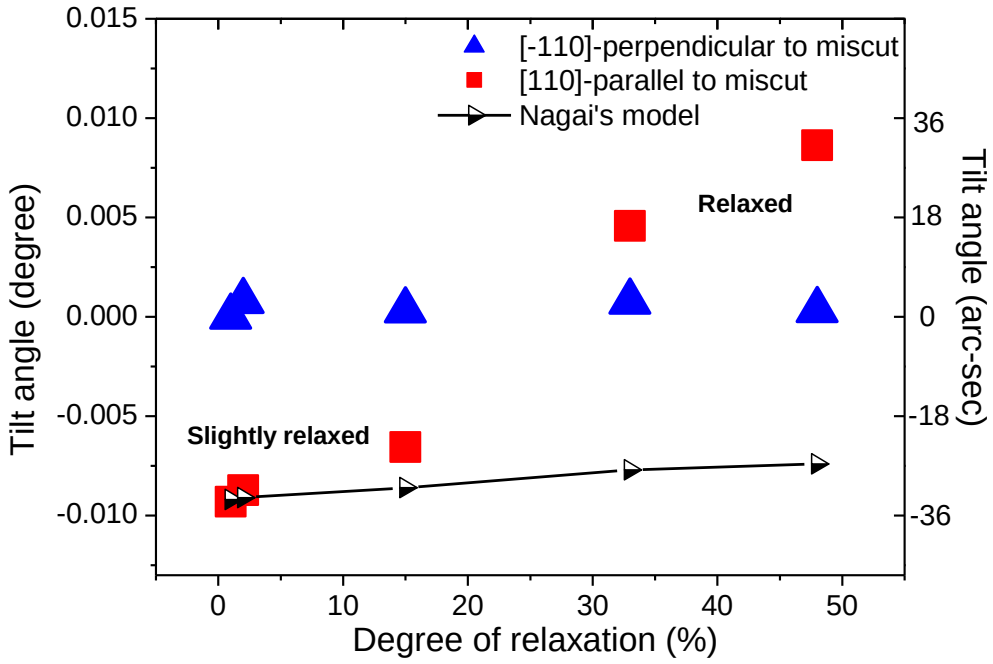


Figure 4.21 Crystallographic tilt plotted as a function of degree of relaxation for GaAs/Ge samples A-E. Squares and triangles represent the tilt angle toward the [**110**] and [$\bar{\mathbf{1}}$**10**] directions, respectively.

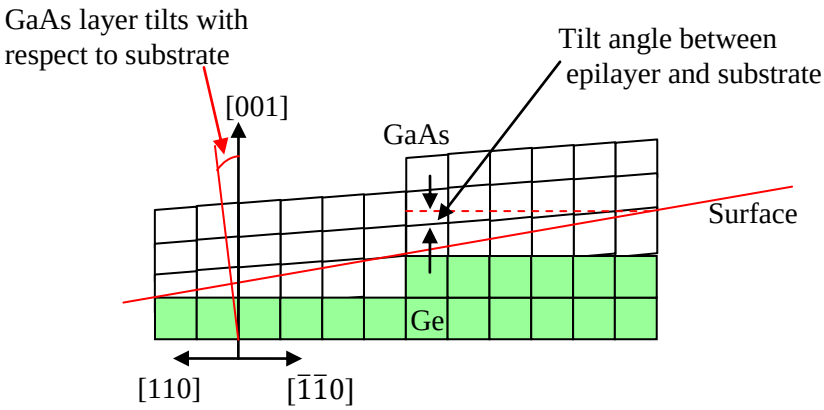


Figure 4.22 Explanation of crystallographic tilt of a pseudomorphically grown epilayer on misoriented substrate using Nagai's model [155].

Concerning the second case – samples D and E represent the situation where the GaAs layers are relaxed through the misfit dislocations generated at the GaAs/Ge interface. In this case, Nagai's model has been experimentally proved by Takagi *et al.* to be inappropriate to explain the mechanism of crystallographic tilt in a relaxed GaAs epilayer, since the epilayers are no longer commensurate with the surface steps of the substrate as a consequence of the lattice relaxation. It has been well investigated that at the early stage of the strain relaxation process, the 60°-type of misfit dislocations are typically predominant (especially in a low lattice mismatched material such as GaAs/Ge), wherein they glide from their nucleating source towards the GaAs/Ge interface at (111) planes [156], Therefore, it would be reasonable to assume 60°-type misfit dislocations are dominant in these GaAs epilayers. As shown in Fig. 4.21, samples D and E with relaxation higher than 30 % are tilted towards the [$\bar{1}\bar{1}$0] direction, and this would be consistent with crystallographic tilt due the imbalanced nucleation of misfit dislocations on each (111) glide plane [157, 158].

4.7 Surface quality investigation by μ-Raman spectroscopy and photoluminescence

The surface quality of MOVPE-grown GaAs/Ge and GaAs/Si samples was characterised using the 488 nm Ar^+ laser probe beam where the average optical penetration depth in crystalline GaAs is ~90 nm [159].

Fig. 4.22 shows the Raman spectra for all of the GaAs/Ge samples. Raman spectra of each GaAs/Ge samples shows two close, intense peaks at ~266 cm^{-1} and ~289 cm^{-1} corresponding to transverse optical (TO) and longitudinal optical (LO) vibration modes of GaAs, respectively . In each case the GaAs LO and TO Raman peaks are red shifted by ~3 cm^{-1} compared with the expected peak position for bulk GaAs [159]. This peak red shifting can result from two factors: 1) Tensile strain in the GaAs epilayer due to the 0.1 % lattice mismatch, and 2) Red shifting induced by the presence of excess arsenic-clusters. Arsenic cluster vibration modes are indeed observed within the spectral region ranging from 150 cm^{-1} – 230 cm^{-1} [60, 160, 161]. Arsenic within the GaAs structure can contribute to the generation of As-As bonds and As-related point defects, such as As_{Ga} antisite defects and Ga vacancies [60]. These indirectly induce changes in the average reduced mass and effective ionic charge that further enhances the red shifting of the Raman peaks [60].

A noteworthy observation occurs because the Raman laser probes only the top ~ 90 nm of the GaAs surface. This is demonstrated by Fig. 4.24, a plot of the Raman TO/LO intensity ratio against normalised photoluminescence intensity. This metric acts an indicator of the surface quality of the sample under test as the presence of a TO peak from a (001) GaAs surface is a signature of lattice misorientation or disorder (dislocations) due to the Raman selection rules in back-scattering experimental geometry [162], as previously discussed in section 2.6.2. The pronounced reduction of the Raman TO/LO intensity ratio (I_{TO}/I_{LO} ratio) of sample E ($I_{TO/LO}$= 0.90) with respect to samples A, B, C and D ($I_{TO/LO}$= 1.25,

1.41, 1.30 and 1.01, respectively) reveals a lower density of lattice disorder or misorientations at the surface of film E [162]. From the characterisation results of X-ray techniques, it is obvious that GaAs overlayer of the samples B-E are relaxed through the generation of dislocations, but the reduction of Raman $I_{TO/LO}$ as a function of thickness increase from samples B-E indirectly implies that the lattice disorder induced by dislocations or lattice disorder reduces at the surface of a thicker film. The Raman spectroscopic analysis therefore allows us to be surface specific whereas the X-ray techniques provide data on dislocation densities throughout the film in its entirety. The Raman intensity ratio, $I_{TO/LO}$= 1.25 of sample A, is relatively high, although it was found to be fully in registry with the Ge substrate by XRD and there are no dislocations images observed in SXRT. This lattice disorder is thought to be induced by the relatively rough surface as a result large APD-related defects present in this film.

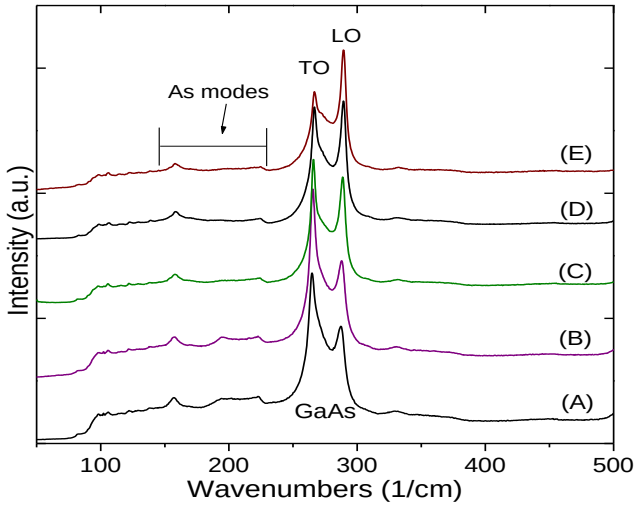


Figure 4.22 Room temperature Raman spectra of GaAs/Ge samples A-E.

The room temperature PL spectra for each of the GaAs/Ge samples A-E are shown in Fig. 4.23 and consistently exhibit a luminescence peak centred at ~ 870 nm, which corresponds to the band-to-band emission from GaAs material [86]. From Fig 4.23, one can observe that increasing GaAs epilayer thickness correlates with an incremental increase in luminescence intensity. An anti-correlation between the Raman intensity ratio and PL intensity of samples B-E is observed, since the luminescence parameter is inversely proportional to the crystalline disorder or dislocation density, as depicted in Fig. 4.24. Comparing samples A-C, sample C shows relatively higher photoluminescence intensity as a result of an improved crystal quality, again consistent with the elimination of anti-phase domain related defects [140]. The use of a pre-deposition As monolayer together with a low temperature GaAs nucleation layer at 500°C prior to GaAs buffer layer growth is responsible for this, as confirmed in the previous section.

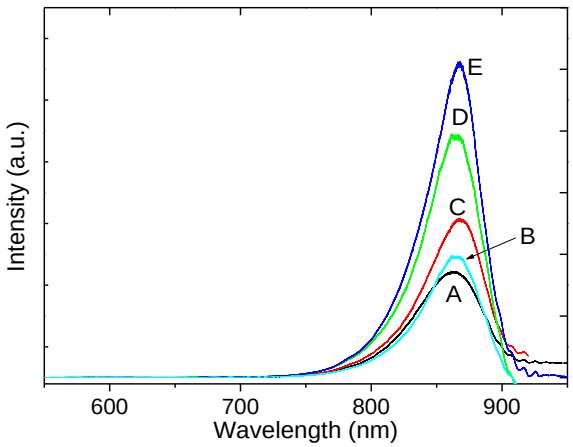


Figure 4.23 Room temperature photoluminescence spectra for GaAs/Ge samples A-E.

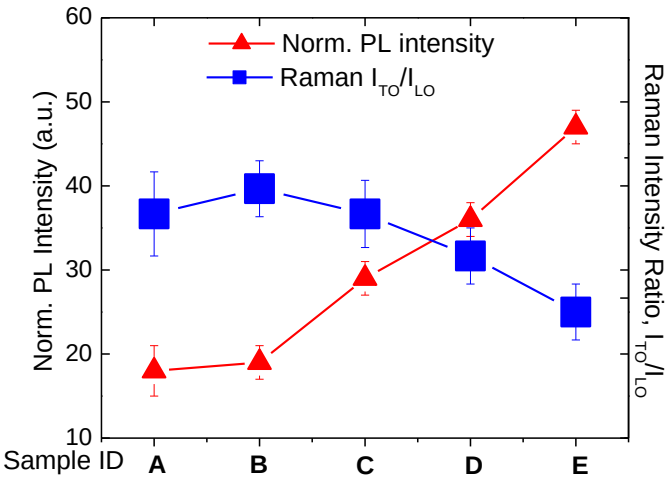


Figure 4.24 Anti-Correlation between PL Intensity and Raman I_{TO}/I_{LO} ratios.

4.7.1 Comparison between MOVPE grown GaAs on Ge and Si substrates

Fig. 4.25a) and b) show the μ-Raman and room temperature PL spectra for MOVPE-grown GaAs/Ge-sample E compared to the MOVPE-grown GaAs/Si-sample. Comparing the μ-Raman data, the GaAs/Ge sample shows a much lower Raman intensity I_{TO}/I_{LO} ratio, which reveals a lower density of disorder or misorientation. This is in good agreement with the PL result, where MOVPE-grown GaAs on Ge substrate results in better overlayer crystallinity, and thus produces the highest luminescence. Consequently, it appears that μ-Raman and PL can be used as easy and quick characterisation techniques to evaluate the surface quality of the GaAs heteroepitaxial layers to complement the X-ray analysis discussed in previous sections.

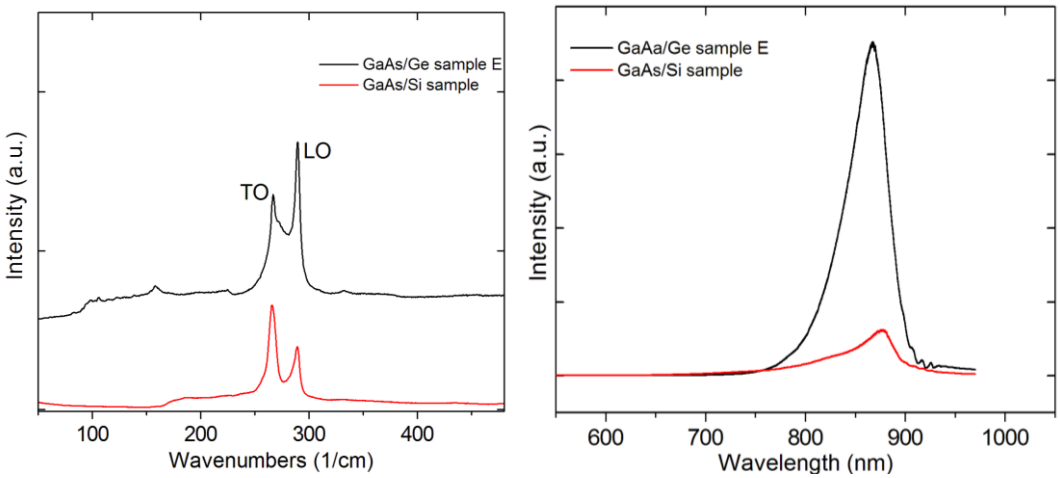


Figure 4.25 Room temperature a) Raman spectra, and b) photoluminescence spectra for GaAs/Ge- sample E and GaAs/Si sample, respectively.

4.8 Summary

The capability of this X-ray characterisation routine in examining/identifying various issues that have to be overcome during the hetero-integration of III-V materials on Si substrates have been demonstrated. Different characterisation work flows were applied for characterising the 'problematic' GaAs heteroepitaxial materials, fabricated using various growth parameters. Problems such as strain relaxation, dislocation formation, antiphase domain formation, crystallinity and lattice tilt can be identified unambiguously by performing appropriate measurements, as summarised in Table 4.5 below.

More importantly, the non-destructive nature of this specially planned characterisation routine meant that a range of measurements could be made on the same sample many times over, allowing comprehensive information to be extracted. This comprehensive information can effectively help the III-V growers in gaining a greater understanding of various issues associated with heteroepitaxial growth, material properties,

and optimal growth processes in the pursuit of low defect density III-V heteroepitaxial layers for future high speed and low power logic applications.

Apart from that, I found that this non-destructive X-ray characterisation routine is not only applicable for characterising the III-V heteroepitaxial layers, but also can be appropriately modified for characterising other semiconductor materials.

Beyond these established methods of XRD, new forms of X-ray analysis have an important role to play in non-destructive characterisation of IC materials. I will expand further on this in Chapter 5 with the introduction of a new X-ray methodology for measuring die stress inside encapsulated packaged chips.

Table 4.5 Summary of the application ranges of the specially planned characterisation routine.

Application Ranges			**Resolution or Accuracy**	**Type of measurem-ent**	**Analysed Depth**
Main Characterisation Technique					
High-resolution X-ray diffraction	**2x ω-2θ scan**	Crystallinity, strain/relaxation, lattice tilt	Depends on the sampling step size = ~ 0.003^{o}	Non-Destructive	> 1μm
	3x ω-2θ scan	Further investigation of crystallinity, antiphase domains	Depends on the sampling step size = ~ 0.003^{o}		
	RSM	Precise measurement of strain/relaxation	Depends on the sampling step size = ~ 0.003^{o}		
X-ray diffraction	**Polycrystalline XRD**	Investigation of polycrystallinity	Depends on the sampling step size = ~ 0.01^{o}	Non-Destructive	> 1μm
	Crystallographic texture mapping	Texture analysis	Depends on the step size of phi and chi		

SXRT	**LABR**	Revealing type of defects and dislocation density estimation	Limited by the spatial resolution of ~3 μm	Non-Destructive	> 1μm
Complementary Technique					
Raman & PL	**Scanning across the sample**	Revealing the lattice disorder or miorientation for the top 90 nm of the surface.	Spectral resolution = ~ 0.02 cm^{-1}	Non-Destructive	~ 90 nm
AFM	**Topography**	Surface morphology characterisation	Limited by probed tip ~ 10 nm	Non-Destructive	Surface characterisation
TEM	**Cross-sectional TEM**	Revealing type of defects in epilayer	0.1 nm	Destructive	Depends on type of material

Chapter 5

Overview of Integrated Circuit (IC) Packaging Technology and Development of Lab-Based X-ray Diffraction 3-Dimensional Surface Modelling (XRD/3DSM)

5.1 Introduction

X-ray-based metrology techniques have a variety of potential applications, not just for epitaxy characterisation in front-end-of-line processes. This thesis has also explored the novel feasibility of using X-ray diffraction with a conventional lab-based tool, as a method to measure stress and warpage of Si die inside chip packaging.

The main aim of this chapter is to demonstrate how the lab-based XRD/3DSM was developed using a different and novel X-ray characterisation routine, for non-destructive analysis of strain/warpage inside fully encapsulated packaged chips. The technique is demonstrated at room temperature and at elevated temperatures up to 115^{o}C by *in situ* XRD annealing experiments. Prior to that, the reader will be given a brief overview of IC packaging technology and the challenges toward the realisation of advanced System-on-Chip (SoC) or System-in-Package (SiP) packages for future microelectronics.

5.2 Overview of IC packaging technology

The integration of many circuits or electronic component into the surface of a thin substrate of semiconductor material such as Si, is known as an Intgrated Circuit (IC) [163]. The IC is typically encapsulated by a moulding compound in order to protect it from being damaged by outside elements or environments. In addition, the IC package also plays an

important role in providing appropriate heat dissipation and acting as a bridge to connect the IC to outside world [163].

Historically, ICs were packaged in leaded packages such as small outline packages (SOP) or quad flat packages (QFP) [164] (see Fig. 5.1). SOP was widely used due to the extermely low fabrication cost, especially for low input/output (I/O) applications such as in modern memory. QFP can be viewed as an extention of SOP for applications that required more I/O connections. These packaging technologies have successfully enabled some level of miniaturisation of microelectronics through reductions of lead pitch and body size of the packages, but they are fast approaching fundamental limits based on the lead pitch rules [164-166].

The innovation of leadless packages such as small outline no-lead (SON) or quad flat no-lead (QFN) packages has displaced conventional leaded packages for many applications [164-166]. This is due mainly to the substitution of the exposed leads by leadless terminals located under the package body of QFN packages, which results in a smaller body size compared to the conventional leaded packages, as shown in Fig. 5.1. The slim package construction of leadless packages together with the use of exposed copper die-pad technology have successfully maximised the board space, as well as improving the electrical and thermal performance of QFN packages by at least 50% over conventional leaded packages [165]. These important features of QFN packages for miniaturisation have produced for extensive growth in semiconductor markets for the past several years, especially for many space-constrained products such as mobile phones, MP3 players, notebook computers, PC cards, and personal digital assistants [165, 166].

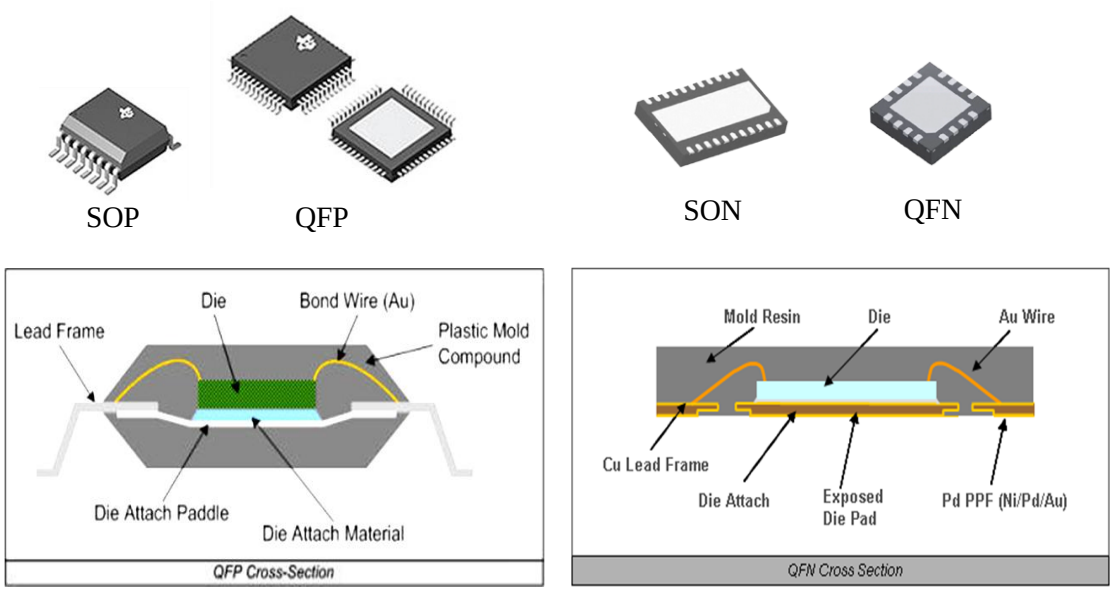


Figure 5.1 Comparison between the conventional leaded packages (SOP, QFP) and the non-leaded packages (SOP, QFN) [163, 166].

Nonetheless, the continued growth of consumer and portable electronics products means that new packaging technologies are necessary in order to meet the ever-increasing demand for low cost, with increased functionality and performance electronic devices. These have driven the development of a new IC packaging technology called the embedded QFN package [167-169]. The most significant advantages of the embedding technology over the traditional packaging technology is allowing the component packages to be embedded into a substrate, and therefore freeing up space for further mounting of components on top of the substrates, thus ensuring a very low profile build up and a very compact 3D wiring architecture (see Fig. 5.2) [167-169]. In addition to that, the substitution of solder interconnections by through silicon vias (TSV) helps improve the electrical performance of the packages, as well as enabling 3D-stacking capability for highly integrated systems [167-169]. Overall, embedding technology is a very promising and feasible technology route towards the realisation of high volume 3D IC integration technology for future

microelectronics, such as 3D SiP or 3D SoC systems [167-169] previously discussed in section 1.1.1. Fig. 5.2 shows a brief overview of the evolution of IC packaging technology.

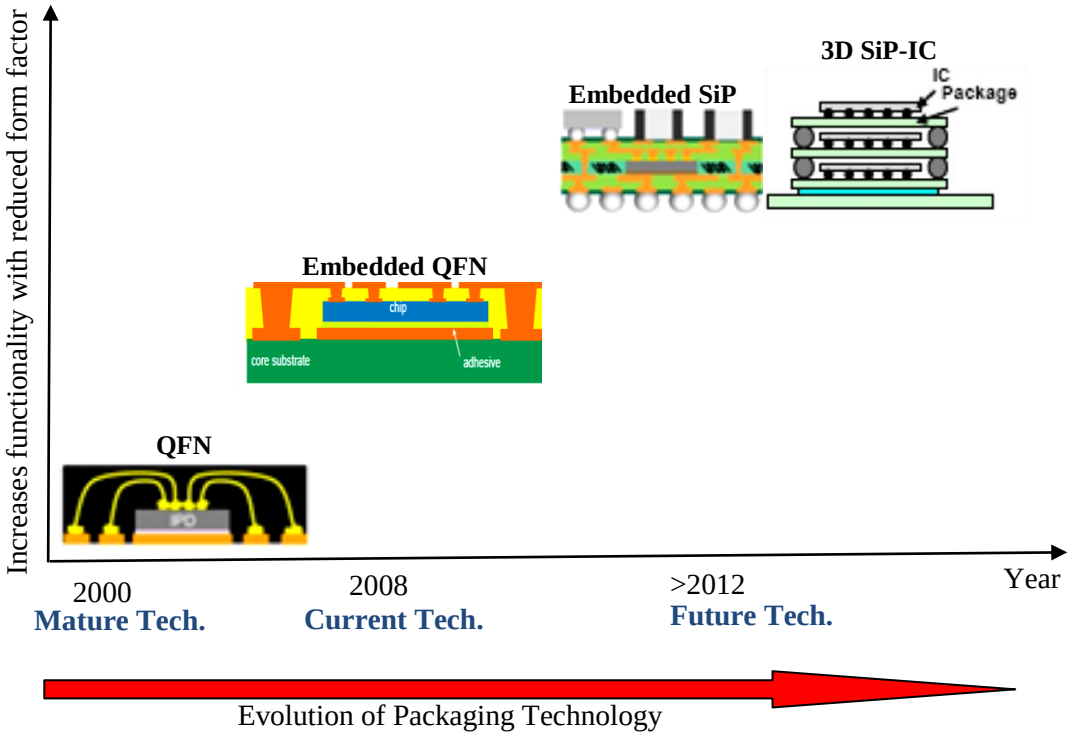
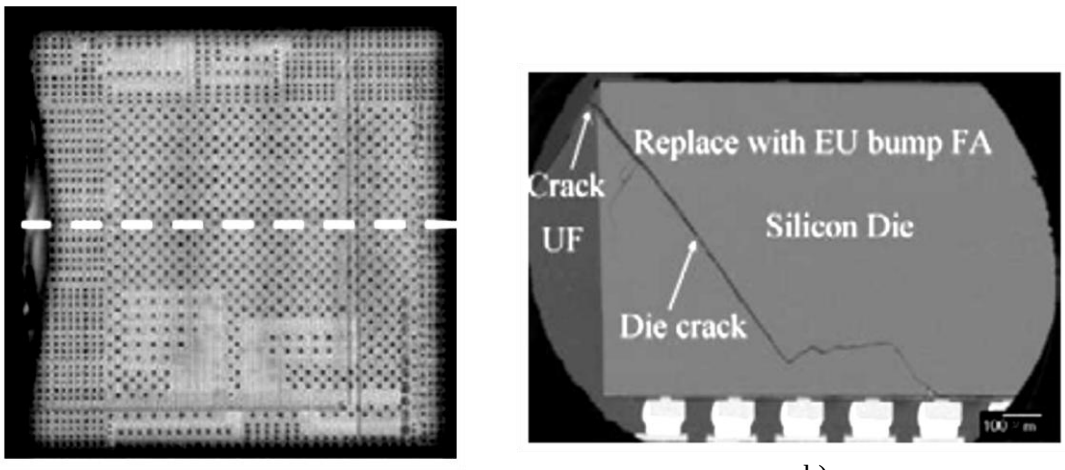


Figure 5.2 Evolution of packaging technology [163, 167].

Existing advanced packaged chips are however plagued by reliability issues. Problems as a consequence of thermal/mechanical stress created during packaging processes are some of the main obstacles towards the realisation of high volume 3D IC integration technology for future microelectronics [54, 170-174]. The fabrication process of a complete packaged IC is a tricky one as it involves the use of different materials of distinct coefficients of thermal expansion (CTEs), *e.g.* die bond pad, die attach adhesive/epoxy glue, moulding compounds and Cu filled TSVs [54, 170-174]. Thermal stress and warpage are frequently generated in the packaged chip during the thermal processing steps as a consequence of the CTE mismatch of

these materials [175-179]. Other factors such as the bonding of wires to the die itself [54], thinning of the wafer/die below 100 μm and embedding/lamination processes can also lead to stress and induced warpage/material deformation [180, 181]. The process-induced stresses can even be large enough to induce cracking or interfacial delamination in the package, which by potentially degrading the performance and reliability of the packaged chip, could ultimately lead to device failure.

Scanning acoustic microscopy (SAM) [182, 183], scanning electron microscopy (SEM) [183] and X-ray radiography [180, 181] are commonly used techniques for characterising packaged chip integrity such as interconnects, voids and delamination inside packaged chips. For instance, Figs. 5.3 a)-b) are the SAM and cross-sectional SEM images of a deformed packaged chip, respectively, showing the die crack which initiated from the upper part edge and then propagated towards the die active circuit side [183]. Although these techniques can image the cracks or delamination inside the packages, none of these techniques is capable of quantitatively measuring the magnitudes of stresses or lattice misorientations inside packaged chips [170], and crucially, they are destructive, i.e. the package has to be opened (SEM) or immersed in water (SAM).



a) b)

Figure 5.3 a) Scanning acoustic microscopy and b) cross-sectional scanning electron microscopy images illustrating die cracking [183].

A recently developed synchrotron X-ray technique, based on 3-dimensional (3D) X-ray diffraction imaging combined with 3-dimensional surface modelling (3DSM), by DCU researchers has, for the first time, enabled the non-destructive imaging and measurement of strain and internal damage in packaged Si chips [38]. This technique has been used to reveal defect images with x-y spatial resolutions of < 5 μm throughout the entire probed Si wafer volume and was used to produce 3D strain/warpage maps of the nature and extent of the strain fields in completely packaged QFN packaged chips. Fig. 5.4 shows an example of 3DSM, showing the warpage/lattice deformation in the Si chip of a completely encapsulated QFN package, created during different manufacturing processes [38].

However, an obvious drawback to widespread implementation of this technique is the fact that until now the techniques have required a synchrotron X-ray source. Therefore, the second aim of this thesis is to demonstrate how I have adapted and transferred the 3DSM technique to a laboratory-based XRD tool in order to non-destructively image, map and measure Si strain/warpage inside a fully encapsulated QFN packaged chip at various stages of the chip manufacturing process.

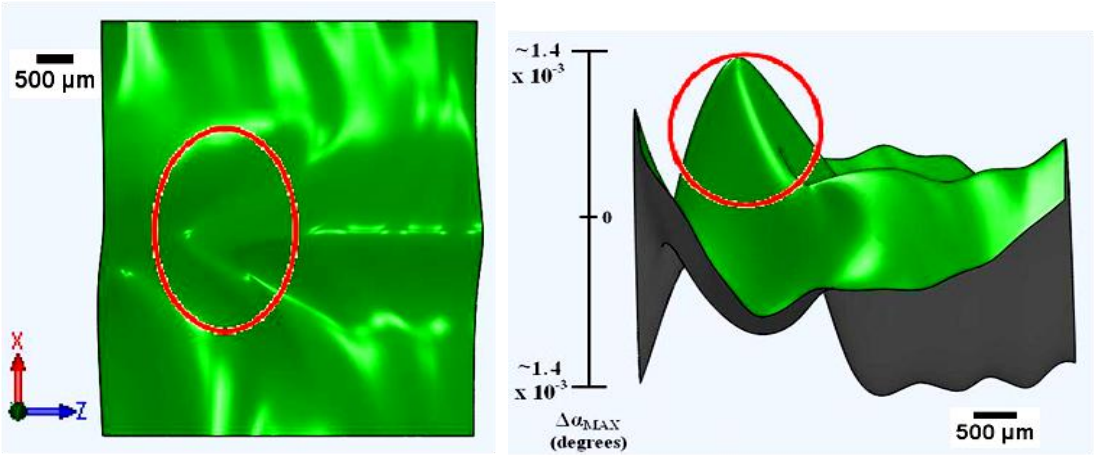


Figure 5.4 3DSM maps of misorientation of (220) Si planes inside a fully encapsulated packaged chip [38].

5.3 Development of a lab-based XRD/3DSM technique

The lab-based XRD/3DSM consists of a data reconstruction technique which monitors the 004 symmetric rocking curve (RC) full-widths-at-half-maximum (FWHMs) as a function of position across fully encapsulated packages, using the advanced freeform modelling capabilities of Solidworks^{TM} to obtain maps of warpage of the entire die inside packaged chips. Solidworks^{TM} is a 3D mechanical computer-aided design (CAD) program, which is also known as a parasolid-based solid modeller and utilises a parametric feature based approach to create models and assemblies [184].

The lab-based XRD/3DSM was developed using two main adaptations of the X-ray characterisation routine shown in Fig. 1.7:

(i) for the ω-scan, or "rocking curve"(RC), the detector angle is fixed at twice the Bragg angle of the crystal planes of interest and the sample is rotated through a suitable angular range about the Bragg angle [46]. The incident X-ray beam was reduced down to a 250 μm x 250 μm square by using horizontal and vertical slits. The small beam size is to ensure a high spatial resolution, as each of the RCs contains information on the lattice deformation averaged across this 250 μm x 250 μm area. As shown in Figs. 5.5 a)-b), the spatial resolution is greatly increased by using a small horizontal slit size, but it is less dependent on the vertical slit size. This is due mainly to the larger X-ray beam divergence in the vertical direction, and therefore the vertical slits have a small impact on the vertical beam rocking curves.

(ii) a series of spatially resolved line scans are performed across the sample under test in steps as small as 200 μm, and this data is reconstructed using lab-based XRD/3DSM – a modified version of the 3DSM reconstruction technique outlined in reference [38]. In general, the data reconstruction of lab-based XRD/3DSM technique includes the following major steps, as depicted in Fig. 5.6 below.

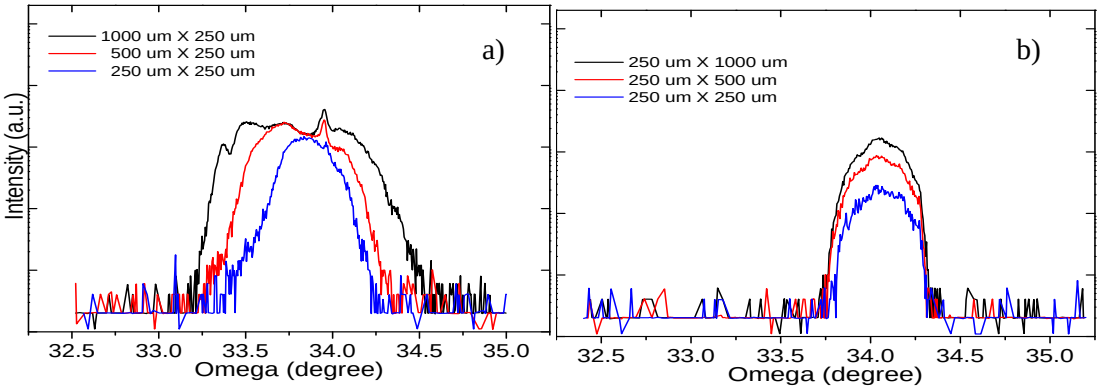


Figure 5.5 a)-b) are the 004 rocking curves as a function of horizontal and vertical slit sizes, respectively.

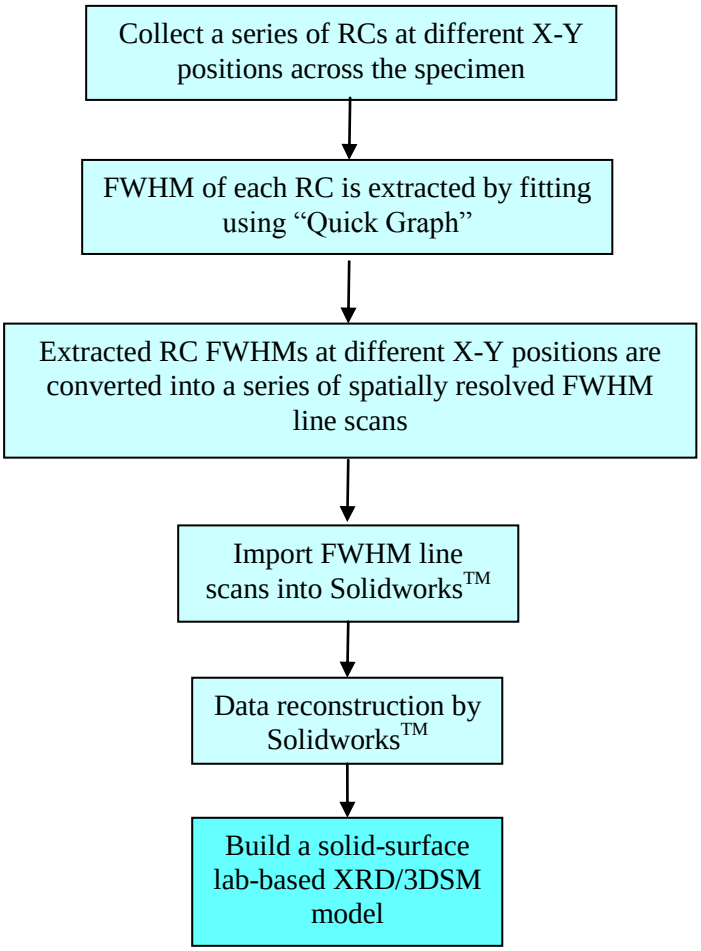


Figure 5.6 Chart illustrating the process flow of lab-based XRD/3DSM technique.

5.3.1 004 Rocking curves

Each RC can be recorded by rotating the specimen (ω axis) through a suitable angular range about the Bragg angle of the Si 004 reflection, with detector (2θ axis) fixed at twice the Bragg angle (see Fig. 5.7a). By using this experimental geometry, the specimen is rotated along the [110] direction with respect to the Si surface normal [001], and therefore the FWHM of the RC is directly related to the lattice misorientation/warpage of the (110) plane in the Si die. Figs. 5.7b)-c) illustrate the RCs of a warped Si die inside the packaged chip compared to a perfect (001) Si specimen without warpage. In the case where the Si die is curved or warped, the FWHM of the RC is broadened (see Fig. 5.7b). The warpage creates a curvature of the Si crystal planes. Therefore there will be a range of angular positions on the distorted Si die for which the Bragg diffraction conditions are satisfied.

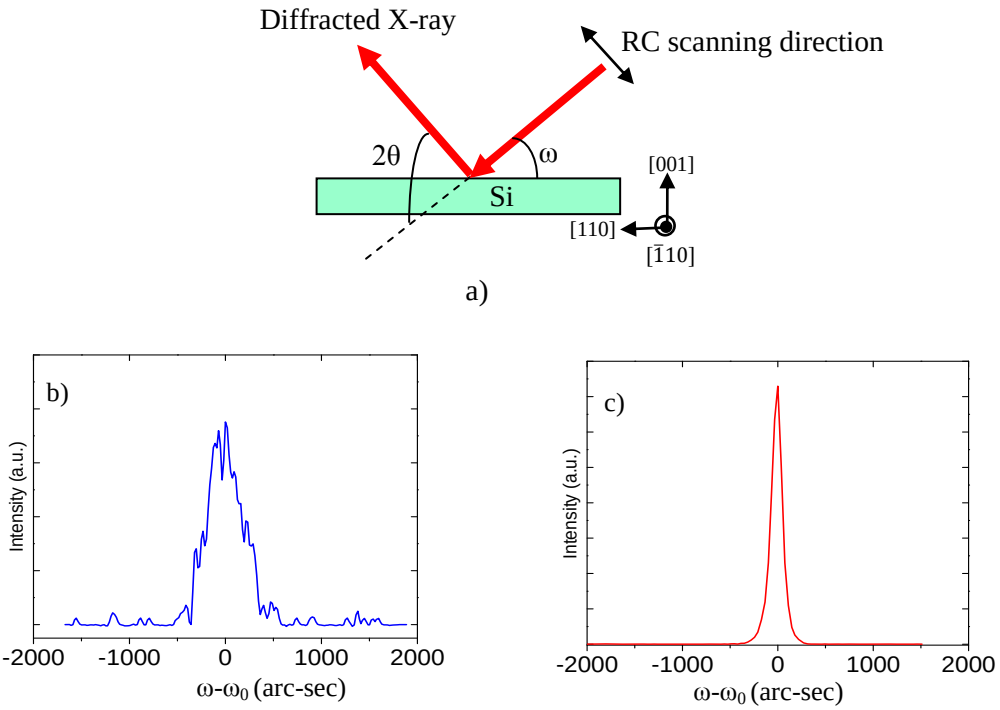
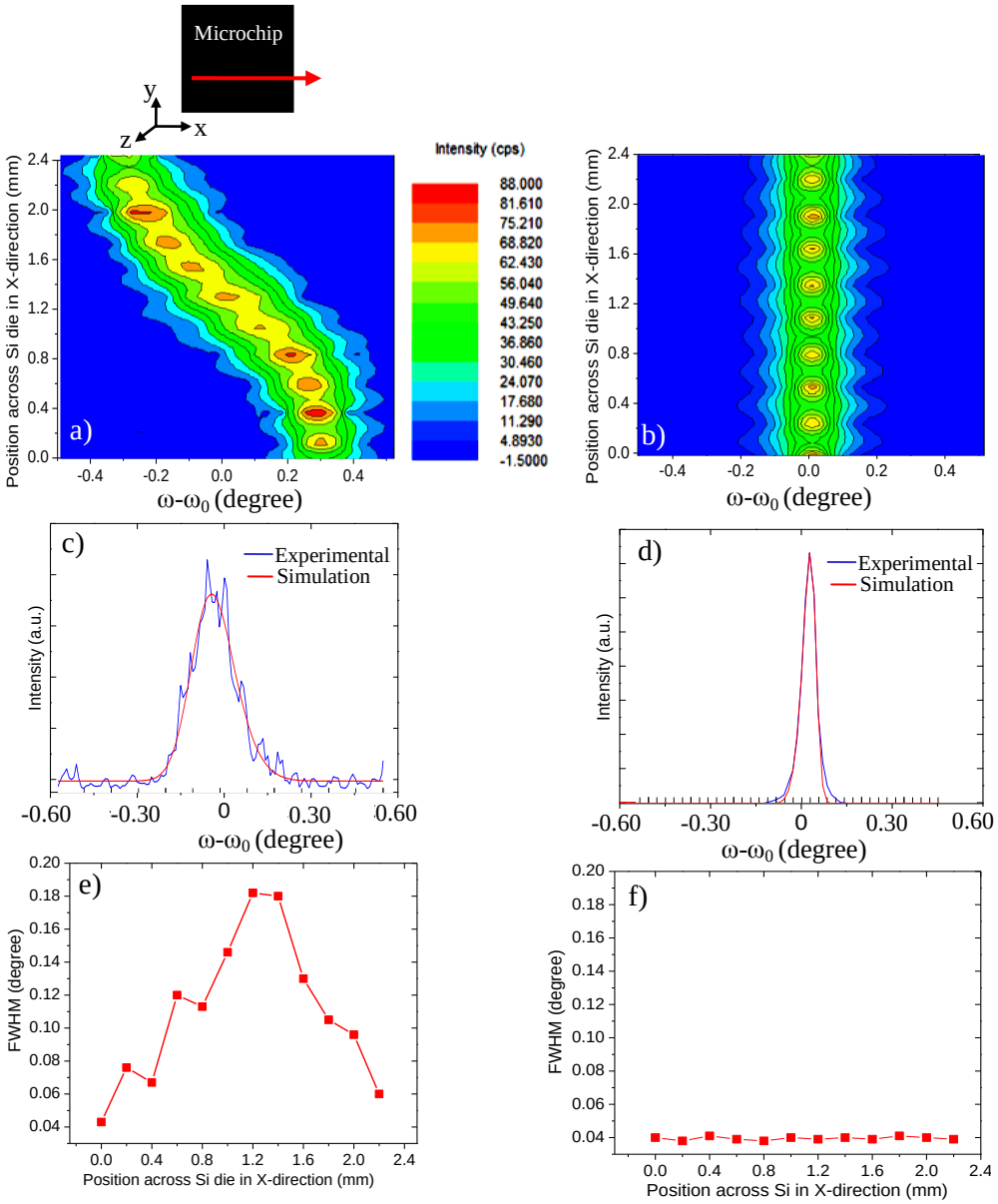


Fig. 5.7 a) Schematic diagram illustrating the experimental geometry of 004 rocking curve analysis. b)-c) are the 004 RCs of a warped Si die and a perfect Si specimen without warpage, respectively.

5.3.2 Obtaining a series of spatially resolved FWHM line scans

A spatially resolved RC map can be produced by integrating a series of RCs collected at different positions across the Si die of the package (in the x-direction) [106]. This is demonstrated in Fig. 5.8a), showing a RC map composed from 12 individual RCs, recorded as a function of x-position across the bottom edge of the Si die - with a step resolution of 200 μm indicated by the red arrow. The RC map of the Si specimen is also shown in Fig. 5.8b) for comparison. Concerning Fig. 5.8a), the variation of RC peak positions (ω-ω_0) across the Si die is a signature of warpage-induced tilt [106]. From the RC map, one can observe that the diffraction angle of the RC recorded from the left part of the Si die (x<1.2) occurs at larger diffraction angles than the centre part of the Si die (ω_o), while it decreases below ω_o for the reflections from the right-hand side of the Si die. This phenomenon explicitly confirms that the Si die is warped in a convex shape [106].

Although the RC map is useful in revealing the type of warpage or direction of tilt developed during the packaging processes, it is not precise enough for a deep insight into the deformation, for instance, in identifying the highly distorted regions of the Si die. Therefore, the approach that I have developed is to convert the RC map into a FWHM line scan by extracting the FWHM of each individual RC of the RC map, fitted using the "Asymmetric Double Gaussian" peak function by Quick Graph [46], the peak analysis software provided with the JV Bede D1 tool (see Figs. 5.8c-d). From the FWHM line scan shown in Fig. 5.8e), the highly distorted region (largest FWHM) can be unambiguously identified to be the centre part of the Si die. In contrast, the FWHM extracted from the perfect Si specimen (Fig. 5.8f)) is rather constant across the whole sample.



Figs. 5.8 a)-b) are the RC maps across the Si die in a packaged chip and the Si specimen in x-direction, respectively, c)-d) are the fitted 004 rocking curves of a warped Si die and a perfect Si specimen without warpage by *Quick Graph*, respectively. The FWHM line scans from the RC maps are shown in Figs. 5.8e)-f).

5.3.3 Importing data into Solidworks™

A series of FWHM line scans were repeated at 200 or 400 μm steps (for high or low resolution) from the bottom edge of the Si die stepping continuously towards the top edge of

the Si die (in the y-direction), controlled using an automatic motorised x-y sample stage on the JV Bede D1 diffractometer. Each FWHM line scan with x, y, z coordinates was saved in a text file in which the x and y coordinates correspond to the on-chip location where each RC was recorded, and z represents the FWHM extracted from each RC recorded at each x-y position. These text files were imported into Solidworks™ using the "Curve Through XYZ Points" tool in Solidworks™, and these formed a series of spline curves through points specified in x, y, z coordinate data (see Fig. 5.9a). The spline curve was created automatically by Solidworks™ through the formation of a sequence of curve segments (base on polynomial models) to connect the imported FWHM data points [185, 186], forming a continuous line (see Fig. 5.9b as an example).

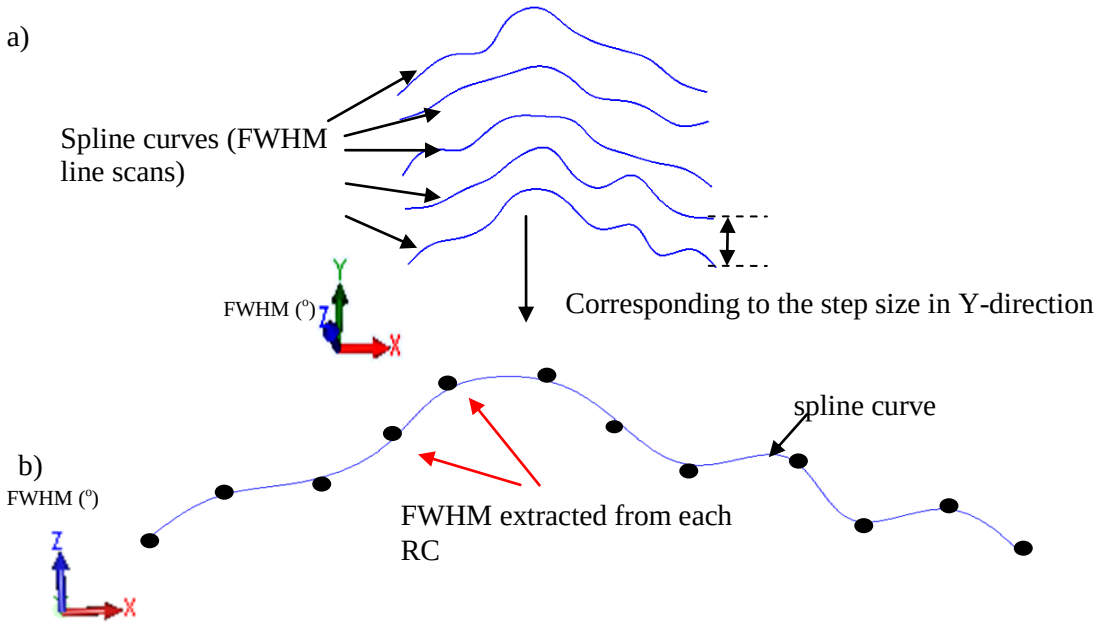


Fig. 5.9 a) A series of recorded FWHM line scans are imported into Solidworks™, and b) A spline curve formed automatically by Solidworks™ using the imported FWHM extracted from each RC.

5.3.4 Data reconstruction by Solidworks™

The final step of the lab-based XRD/3DSM was to connect these spline curves using the boundary surface feature in Solidworks™ [38]. Each spline curve was selected sequentially from the first horizontal spline curve to the last horizontal spline curve, and they were connected to create a boundary surface mesh across these spline curves, as shown in Fig. 5.9a). These spline curves were formed into a solid surface lab-based XRD/3DSM model (see Fig. 5.9b).

Although the "Curve Through XYZ Points" tool and the boundary surface feature are easy and straightforward to use through Solidworks™, the mathematics behind how the spline curves and the boundary surface were created are rather complex. These are beyond the scope of this thesis, but more information can be found in references [186, 187].

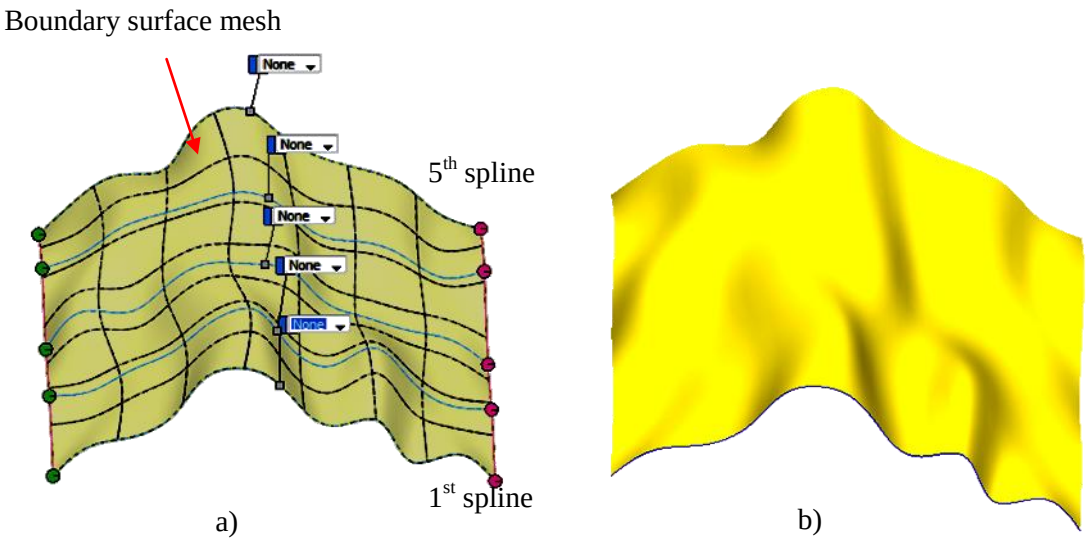


Fig. 5.9 a) Boundary surface feature used to connect the spline curves, and b) A solid surface model of lab-based XRD/3DSM, demonstrating the lattice misorientations of the (110) plane in an example Si die inside a fully encapsulated packaged chip.

5.4 *In Situ* XRD Annealing Experiments

The lab-based XRD/3DSM technique is also applicable at elevated temperatures up to 115^{o}C by *in situ* XRD annealing experiments. This process is a good way of replicating the thermal response of the packaged chip at temperatures it may encounter during manufacture and operation.

These annealing experiments were carried out using the same Jordan Valley's D1 X-ray diffractometer through the following procedures:

i) Fitting an Anton Paar DHS 1100 heating stage

The system was equipped with an Anton Paar DHS 1100 heating stage, as shown in Fig. 5.10 (see Table 5.1 for Anton Paar specifications) [188]. This allows one to perform *in situ* XRD annealing experiments without the need to remove the specimen from the sample stage or further XRD set-up alignment prior to the heating experiments. The *in situ* stage ensured the position of the specimen mounted on the heating stage remained constant, both prior to and after each heating experiment was carried out, ensuring very high repeatability and reliability of results.

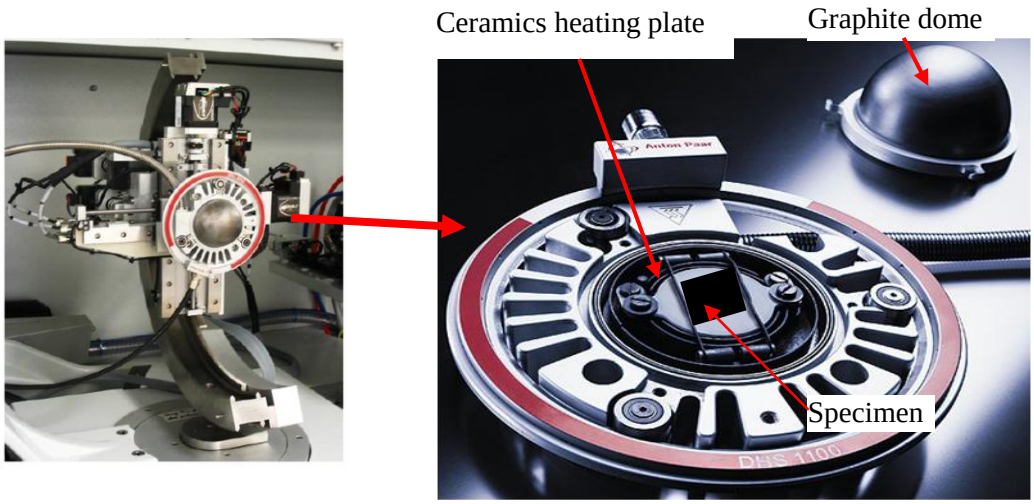


Fig. 5.10 Photo of the Anton Paar DHS 1100 fitted to the sample stage of the Jordan Valley's D1 X-ray diffractometer system [188].

Table 5.1 Specifications of Anton Paar DHS 1100 heating stage [188].

Specifications	
Operating temperature	25°C to 1100°C
Atmospheres	Vacuum (10^{-1} mbar), air, inert gas, nitrogen
Max. operating pressure	Max. 0.3 bar above atmospheric pressure
Transmission (incident and diffracted rays)	~ 65%
Diameter/Height/Weight	128 mm/51 mm/450 g

ii) Mounting the sample onto the stage

The sample was mounted onto the chemically resistant ceramic heating plate (see Fig. 5.10), and then covered by a graphite dome (see Fig. 5.11). This allows the *in situ* XRD annealing experiments to be carried out in various ambients, such as vacuum, air and nitrogen.

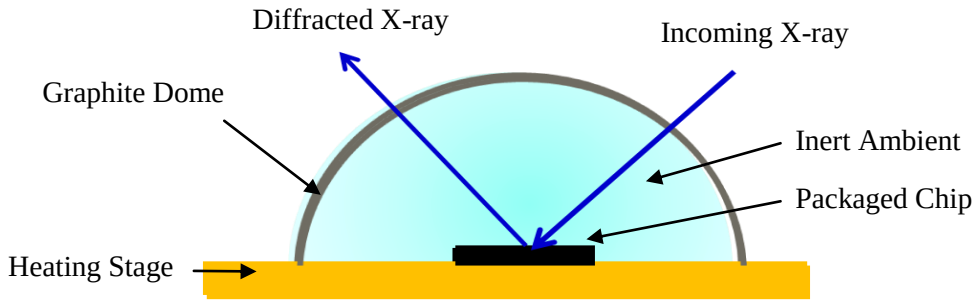


Fig. 5.11 Schematic diagram showing the experimental setup of *in situ* XRD annealing experiments.

iii) Aligning the sample in the beam

Prior to the annealing experiments, the sample was properly aligned in the beam for diffraction using the procedures previously discussed in section 2.4.5.

iv) Performing the *in situ* XRD annealing experiment

During the *in situ* XRD annealing experiments, the annealing temperature was monitored using a thermocouple controlled temperature unit (Anton Paar TCU 200). The system has a temperature range of 25^{o}C to 1100^{o}C with an accuracy of 0.1^{o}C. The annealing temperature can be set through the front control panel of the TCU 200 unit.

When the sample is heated to the desired temperature, the XRD/3DSM measurements can be performed following the sample procedure as described in section 5.3.

5.5 Summary

The evolution of IC packaging technology has been briefly reviewed. Manufacturing-induced thermal stress created during the fabrication of packaged integrated circuits can potentially lead to device failure. Therefore, the need to develop metrologies that can be used to effectively measure stress/strain in systems-on-chip or systems-in-package is identified by the International Technology Roadmap for Semiconductors (ITRS).

A novel lab-based technique called X-ray diffraction 3-dimensional surface modeling (XRD/3DSM) for non-destructive analysis of manufacturing process-induced stress/warpage inside completely encapsulated packaged chips has been developed using a triple-axis Jordan Valley Bede D1 X-ray diffractometer. Results from this technique will be shown in the following chapters 6 and 7, through the charactersation of die stress and warpage inside encapsulated commercially available ultra-thin QFN packages, as well as die stress and warpage in embedded QFN packages at various stages of the chip manufacturing process.

Chapter 6

Characterisation of Die Stress and Warpage Inside Commercially Available Ultrathin-QFN Packages

6.1 Introduction

In order to confirm the feasibility of the lab-based XRD/3DSM technique, I have applied this technique to characterise die stress and warpage inside fully encapsulated commercially available ultra-thin Quad Flat Non-lead (UQFN) packages. For the UQFN package under test, warpage is investigated as a function of the large thermal stresses, mimicking those that are developed during the die attach process, and the moulding compound encapsulation process as a consequence of the coefficient of thermal expansion (CTE) mismatch between different materials. These are carried out by *in situ* XRD annealing experiments, as well as finite element analysis (FEA).

6.2 UQFN packages

In this study, a commercially available 28-pin UQFN flash microcontroller (Manufacturer Part No.PIC16LF1827-I/MV) from Microchip is examined. Fig. 6.1a) is a cross-sectional schematic diagram of a typical UQFN package, in which a die is attached onto a lead frame by die adhesive film/epoxy glue, and finally encapsulated by a moulding compound. The contact pads of the UQFN package are connected to the die using wire-bonding technology creating thin wires. The physical dimensions and the material properties of the UQFN package under test are estimated from X-ray radiographic images of the UQFN package (see Fig. 6.1b) and references [189-192], as summarised in Table 6.1.

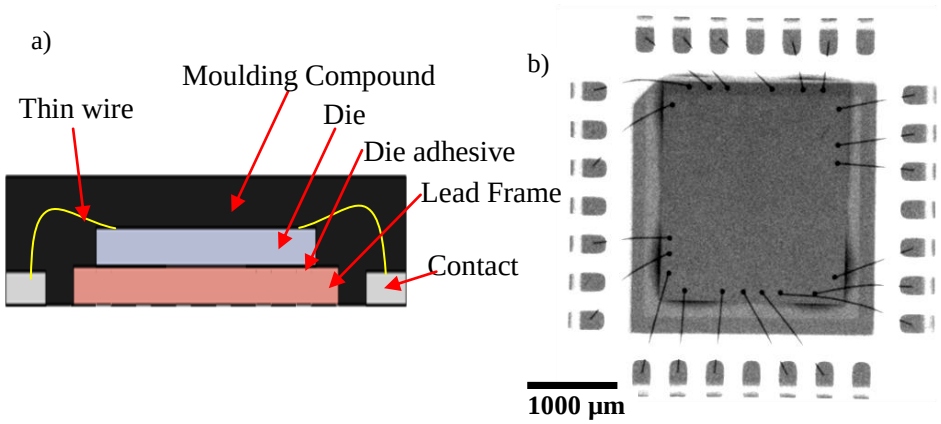


Figure 6.1a) Cross-sectional schematic diagram of a typical QFN package, and b) X-ray radiographic image of the UQFN package under test.

Table 6.1 UQFN package physical attributes.

Attribute	**Materials**	**Dimension, mm**		
		Width	**Length**	**Height**
Lead frame/Exposed pad	Copper alloy	2.80	2.80	0.150
Die adhesive	Silver Epoxy	0.70	0.70	0.025
Die	Silicon	2.20	2.40	0.150
Cap	Epoxy Resin	4.00	4.00	0.175
Overall dimension		4.00	4.00	0.500

6.3 Characterisation of die stress inside UQFN packages

6.3.1 Lab-based XRD/3DSM

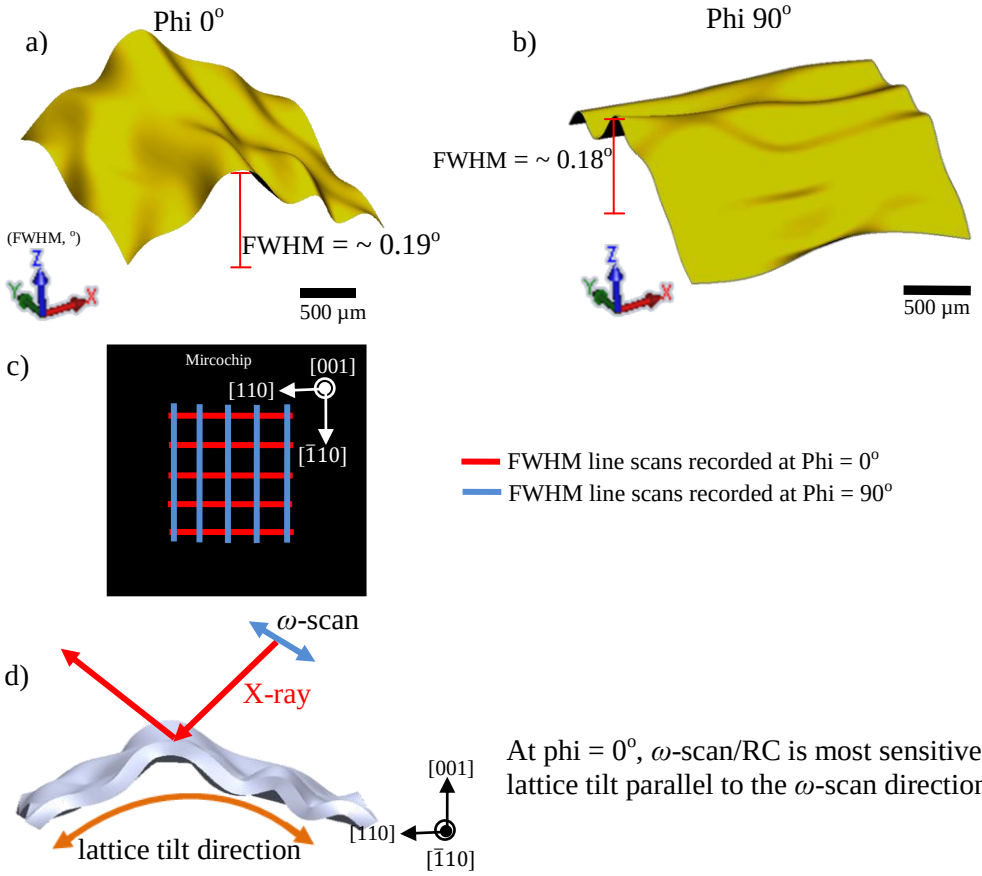
Fig. 6.2a) shows the XRD/3DSM of a UQFN package recorded at phi = 0^{o}, which is, in effect, a 2D map of the warpage/lattice deformations which have developed in the Si die during the packaging process. The sample was then rotated successively by 90^{o} around the [001] axis (surface normal) and the mapping and reconstruction processes were repeated, in order to evaluate the lattice misorientations of the two orthogonal (110) crystallographic

planes in the Si die, as shown in Fig. 6.2b) –i.e. a XRD/3DSM recorded at phi = 90°. Each of the XRD/3DSMs is built up from a total of 5 horizontal (phi = 0°) and vertical (phi = 90°) FWHM line scans, respectively – using a 400 μm step size between two adjacent FWHM line scans. Fig. 6.2c) shows the approximate position where the horizontal and vertical FWHM line scans were recorded.

Measurements at phi = 0° and 90° are required in order to investigate the lattice misorientations of the two orthogonal (110) planes. This is because XRD/3DSM performed at phi = 0° collects only the lattice tilt information of one (110) plane, which is parallel to the scanning direction of the RC measurement (see Fig. 6.2d). Using the crystal axes shown in Fig. 6.2c), the XRD/3DSMs recorded at phi = 0° and 90° correspond to the diffractions from either the (110)/ $(\bar{1}10)$ or $(1\bar{1}0)/(\bar{1}\bar{1}0)$ crystallographic planes, respectively. Each of the XRD/3DSM took approximately 90 minutes scan time, and more details are summarised in Table 6.2.

Table 6.2 Details and scan times for each XRD/3DSM.

Type of scan	**Details**			
004 Rocking curve	**Sampling step size**	**Count time per point**	***ω*-scanning range**	**Approximate scan time per RC**
	0.005°	0.5 sec	0.7°	1.5 minute
FWHM line scan	**Distance between two RCs were recorded**			**Approximate scan time per FWHM line scan**
	200 micron			18 minutes
XRD/3DSM	**Distance between two FWHM line scans were recorded**			**Approximate scan time per map**
	400 micron			90 minutes



Figures 6.2a)-b) are the XRD/3DSMs of the UQFN package recorded at phi = 0° and 90°, respectively, and c) is a schematic diagram illustrating the approximate locations of the line scans at phi = 0° and 90° for the UQFN package. Fig. 2d) demonstrates the ω-scan/RC scan direction versus the lattice tilt direction at phi = 0°.

The XRD/3DSMs of the UQFN package clearly reveal that the warpage is relatively low at the corners of the Si die and increases gradually approaching the centre part of the die. Warpage can be defined as a distortion where the surface is bent or twisted out of shape, especially from a straight or flat form. This non-uniformly distributed warpage is thought to be most probably due to the process-induced thermal stress as a result of the CTE mismatch between different materials. These will be mainly attributable to the die attach process [175-179], and smaller stresses are generated during later processing stages, for instance, during the moulding compound encapsulation process and thermal cycling reliability testing. In

general, the die attach process comprises of the attachment of the die onto the lead frame and the curing of the bonding adhesive at an elevated temperature (> 100^{o}C) [189, 192]. Considering a similar die attach process was used for the UQFN package under test, wherein an epoxy glue was applied to the Si die, and that the thermosetting adhesive crosslinks and hardens during the adhesive curing process, this most likely generates thermal stress upon cooling down to room temperature [175-179], as illustrated in Figs. 6.3a)-b). This stress occurs because the copper lead frame possesses a much larger CTE and is likely to undergo greater expansion at the time at which the Si die was bonded onto the copper lead frame and cured at an elevated temperature (> 100^{o}C). The thermal stress is formed upon cooling down the materials to room temperature as a result of the much faster shrinking rate of the underlying copper lead frame (contraction force or compressive stress), and this therefore induces warpage in the Si die, forming the lattice deformation as observed by XRD/3DSMs in Figs. 6.2a)-b).

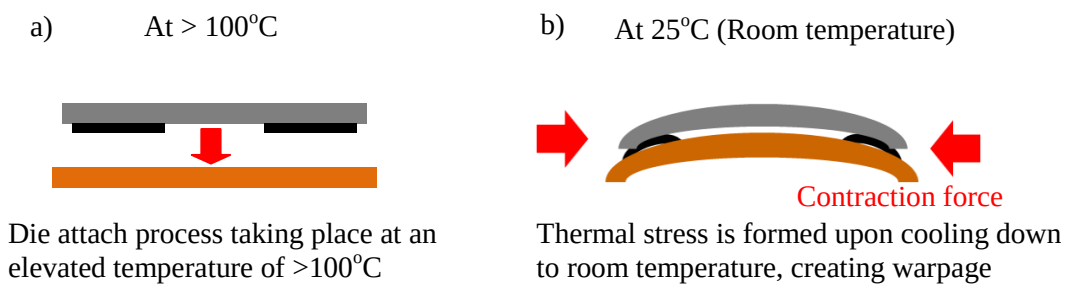


Figure 6.3 a)-b) demonstrate the formation of warpage by thermal stress due to CTE mismatch between different materials.

6.3.2 Synchrotron X-ray topography (SXRT)

In order to validate data obtained from the lab-based XRD/3DSM, the UQFN package was also investigated by SXRT. The 220 reflection for large area transmission topographs (LAT) has been chosen. This is because the 220 reflection (second order of 110

reflection) [193] contains diffraction intensities arising from the (110) plane in the Si die. Therefore, this allows us to make a direct comparison of the results obtained from the lab-based XRD/3DSM and SXRT, for which the 220 LAT topographs recorded at phi = 0^o and 90^o provide us the lattice tilt of the two orthogonal (110) planes in the Si die.

Figs. 6.4 are the 220 LAT topographs of the UQFN package recorded at phi = 0^o and 90^o, respectively. The projection of the diffraction vector, $\vec{g}$ of the X-ray beam onto the plane of the recording film is represented by the arrow. For both cases, the topograph is consistently elongated in the direction parallel to $\vec{\boldsymbol{g}}$, which is due mostly to the high degree of warpage/lattice misorientation in the Si die [38]. This is because the greatest sensitivity of SXRT occurs when $\vec{\boldsymbol{g}}$ is parallel to the direction of the lattice tilt [38]. For ease of comparison, these LAT topographs are normalised in order to eliminate the geometric distortion parallel to $\vec{\boldsymbol{g}}$, as shown in Fig. 6.5. The hemispherical features marked by **S** shown in the topographs are the diffracted intensity from the edges of the warped Si die. These features are formed by orientation contrast phenomena due most likely to the deviation of the Bragg angle as a consequence of the strain-induced tilt of the diffraction planes [38]. At phi = 0^o, only the lattice misorientation in one (110) plane is observed, therefore LAT at phi = 90^o is required in order to reveal the lattice misorientations of the two orthogonal (110) planes. These observations of LAT topographs confirm the XRD/3DSM results discussed in previous section, where the most highly distorted region is identified to be towards the centre of the Si die (marked by **S**) for which the diffracted intensity is "defocused" and recorded at different locations on the film. Apart from that, four elliptical features marked by **D** are consistently observed in the LAT topographs of the UQFN package. These are as a result of the strain field patterns from the epoxy glues applied around the four corners of the Si die, as previously observed in X-ray radiographic images.

In addition, the UQFN package was also investigated by large area back reflection (LABR) topography. The $\bar{2}28$ LABR topograph of the UQFN package is shown Fig. 6.6a). The darker hemispherical features in the LABR topograph (e.g. see arrow **A**) are due to the strain induced tilts in the Si towards the central regions of the edges of the die, leading to the apparent bowing of the recorded die edges as seen in the LABR topograph (see Fig. 6.6b). However, the strain field patterns due to the epoxy glues are not visible on the LABR topograph. This is because, in back reflection mode, the X-ray beam probes only the top ~ 60 um of the Si die, which itseld is ~150 μm thick; therefore it provides only the lattice information from the region near to the top surface. The similar nature of the distortion observed from LAT and LABR topographs confirm the XRD/3DSM results obtained from lab-based XRD measurement.

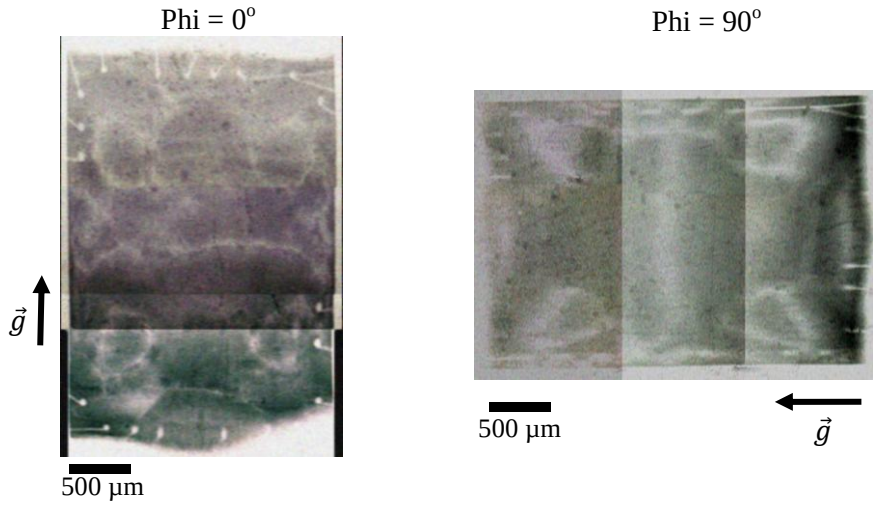


Figure 6.4 220 LAT topographs of the UQFN package recorded at phi = 0° and 90°, respectively.

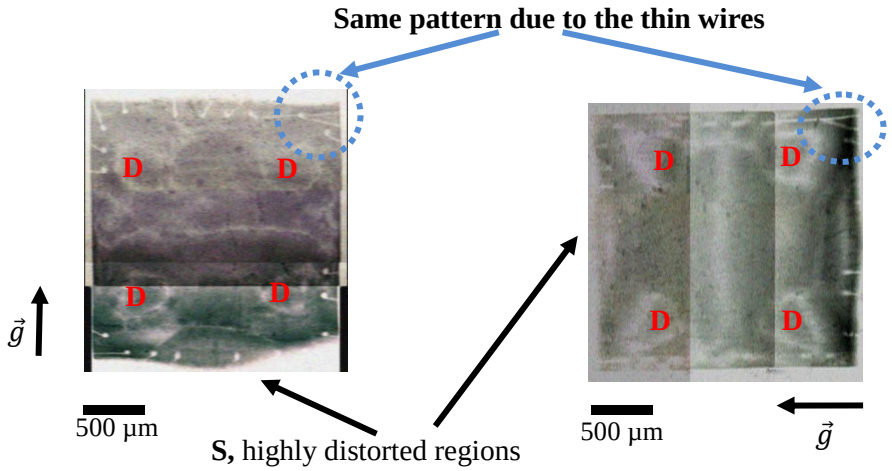


Figure 6.5 Normalised 220 LAT topographs of the UQFN package recorded at phi = 0° and 90°, respectively, as shown in Fig. 6.4, in order to eliminate the geometric distortion parallel to $\vec{g}$.

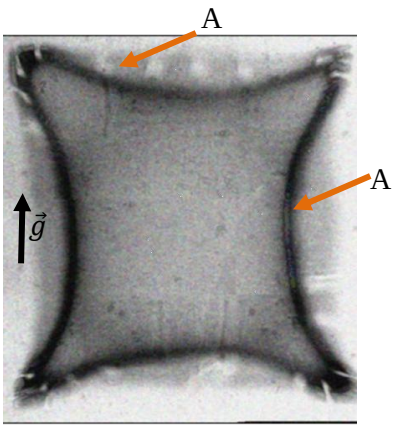
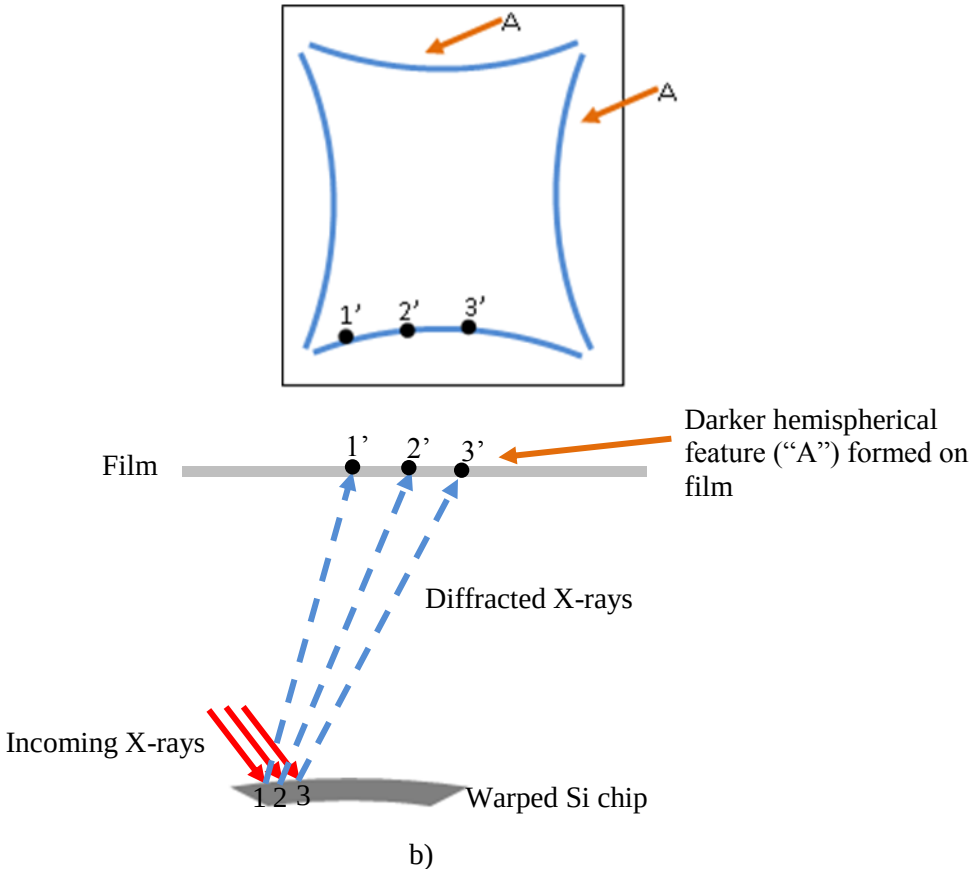


Figure 6.6a)



b)

Figure 6.6a) is the $\bar{2}28$ large area back reflection topograpy of the UQFN package, and b) Formation of darker hemispherical features ("A") in the LABR topograph due to the strain induced tilts in the Si towards the central regions of the edges of the die.

6.3.3 *In Situ* XRD annealing experiments

This warpage as a result of CTE mismatch of different materials is expected to relax back if a thermal load is applied to the UQFN package. In order to verify and observe how the warpage of the Si die evolves as a function of temperature, I have performed *in situ* XRD annealing experiments using the Anton Paar heating stage at temperatures ranging from 25^{o}C to 115^{o}C in 30^{o}C steps, recorded at phi = 0^{o}. For each temperature, the UQFN package was heated using a heating rate of 5^{o}C/minute.

For each case, the RC FWHM was extracted from the highly distorted region of the UQFN package, and is shown in Fig. 6.7. The warpage (FWHM) was greatly reduced as the UQFN package was heated up from 25°C (FWHM = ~0.19°) to 115°C (FWHM = ~0.09°). These observations from *in situ* XRD annealing experiments imply that thermal process-induced strain relief has occurred at elevated temperatures. The greater expansion rate of the underlying copper lead frame most plausibly relaxes the Si warpage. This same experiment has been repeated on a second UQFN package, and the extracted FWHM of the highly distorted region is also shown in Fig. 6.7. Repeat experiments consistently show a similar trend of tilt reduction as a function of temperature, and thus demonstrate a high reproducibility and reliability of results. The slight variation of warpage measured from both chips can be interpreted as due most probably to slight physical differences from chip-to-chip.

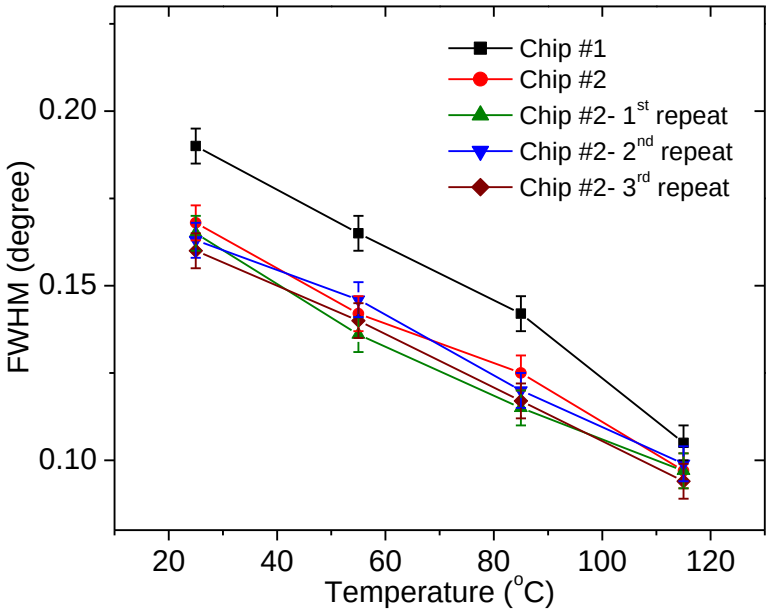


Fig. 6.7 The extracted RC FWHM as a function of temperature, illustrating the reduction of warpage in packaged chips as temperature increases.

6.3.4 Stress estimation

The lab-based XRD technique can be used to quantitatively estimate the warpage stress induced in each chip during the packaging process, using the angular offset between the peak positions of RCs measured at two adjacent regions [194]. This 'warpage stress' is a biaxial stress ($\sigma_{xx} + \sigma_{yy}$) – the sum of stress from two in-plane directions due to the contraction forces, as previously discussed. Considering a warped chip shown in Fig. 6.8, the upper half and lower half of the chip will be experiencing tensile and compressive stresses, respectively, whereas the centre region is stress-free due to the neutralisation of the stresses from the top and bottom of the surfaces. When one assumes the top and centre regions of the chip are two curved regions sharing the same central angle ($\Delta\theta$ = angle between the surface normals of positions X_1 and X_2) but having different arc-lengths, the stress can be estimated through the following relation [194]:

$$Strain, \varepsilon = \frac{change\ of\ length\ (dl)}{Original\ length\ (L_o)} = \frac{L - L_o}{L_o} \tag{6.1}$$

Through the stress-strain relationships relationships[194],

$$Stress, (\sigma_{xx} + \sigma_{yy}) = -\left(\frac{E}{\nu}\right)\left(\frac{L - L_o}{L_o}\right) \tag{6.2}$$

where E = Young's modulus of Silicon. From Fig. 6.8, we know that $L_o = \Delta\theta R$ and $L = \Delta\theta(R + t/2)$ and this means Eq. 6.2 can be simplified to [194]

$$Stress, \sigma = -\left(\frac{E}{\nu}\right)\left(\frac{t}{2R}\right) \tag{6.3}$$

The radius (R) can be calculated through the following relation [194],

$$R = \frac{d}{\Delta\theta} \tag{6.4}$$

where $\Delta\theta$ and d are the peak position difference and the distance between the surface normals of positions X_1 and X_2, respectively. Using this relation, the warpage stresses across the

whole Si die can also be reproduced using the same XRD/3DSM technique. These are demonstrated in Figs. 6.9 showing maps of warpage stresses across the entire Si die in the UQFN package measured at phi = 0° and 90°, in which the warpage stress is comparatively low around the corners of the Si die due to lower warpage or lattice misorientation, as previously discussed.

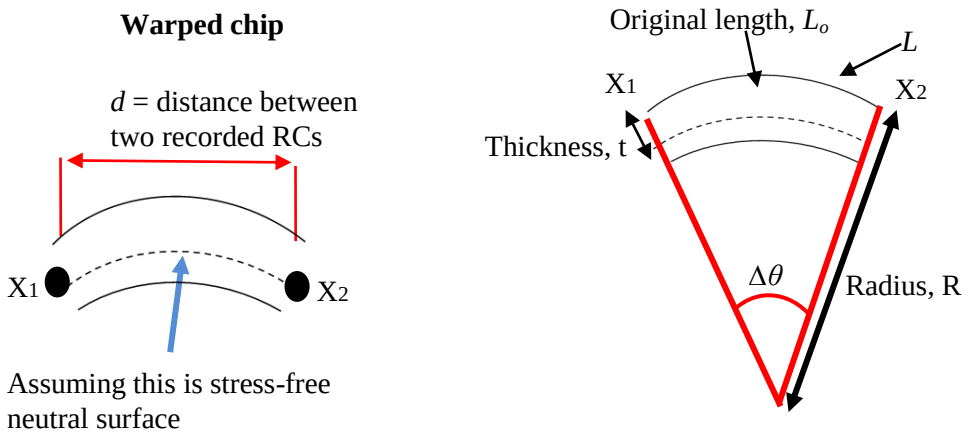


Fig. 6.8 Schematic diagram illustrating the relationship between warpage stress and warpage-induced curvature of wafer [194].

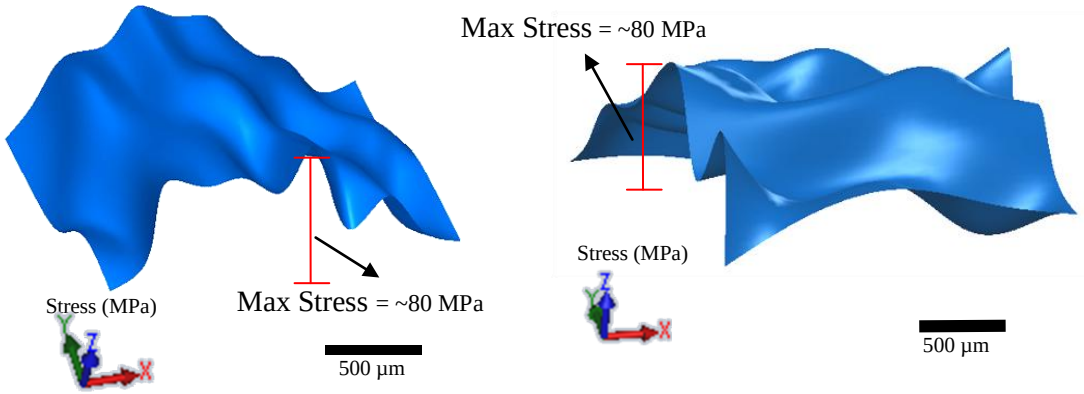


Fig. 6.9 XRD/3DSMs showing the distribution of warpage induced stresses across the whole Si die recorded at phi = 0° and 90° (left/right).

6.3.5 Finite element analysis (FEA)

For the purpose of developing a deeper understanding of the experimental results, I have also adopted a very simple FEA analysis in this study. In general, FEA is a widely used numerical technique for predicting a model's response to various influences such as forces, torques, periodic excitations, and heat [195, 196]. It is very useful, especially for analysing a large or complicated model where analytic solutions are not possible or difficult. The fundamental concept behind the FEA is to break any complex model into thousands of small tetrahedral elements and solving each of the individual elements numerically [195, 196].

In this work, FEA was done with an "Add-In" advanced feature of Solidworks™, called Solidworks™ Simulation. The Solidworks™ Simulation was used to perform two types of FEA studies; i) Static analysis – to predict stresses and displacement caused by static/mechanical loading, and ii) Thermal analysis – to predict stress and displacements due to thermal expansion. The results predicted from FEA will be used for direct comparison with the experimental measurements.

The 3D model used in the Solidworks™ simulations was sketched according to the physical dimensions of the UQFN package as summarised in Table 6.1. The FEA simulations were performed using the following procedure:

Step 1- <u>Construction of the parts using Solidworks™:</u>

Different parts of the UQFN package were sketched using the physical attributes summarised in Table 6.1.

Step 2- <u>Combination of multiple parts into an assembly:</u>

These different parts were imported accordingly into an assembly and combined in order to form a 3D solid model.

Step 3- <u>Discretization of structure:</u>

A mesh was created in order to break the complex 3D solid model into a large number of small tetrahedral elements, forming the 3D FEA model which is required for FEA simulation [195, 196]. Each of these elements occupies a small but finite sub-domain of the original part, and they are called finite elements because there are a known number of elements in a 3D FEA model. Each element is connected to the adjacent element via "nodes", in which they act to define the shape and also to convey physical reactions from one element to another of a FEA model [195, 196]. For the UQFN package, the finite element model of the full UQFN package was created based on 65034 3D brick elements nodes and 41590 mesh elements to produce tetrahedral meshing, as depicted in Figs. 6.10.

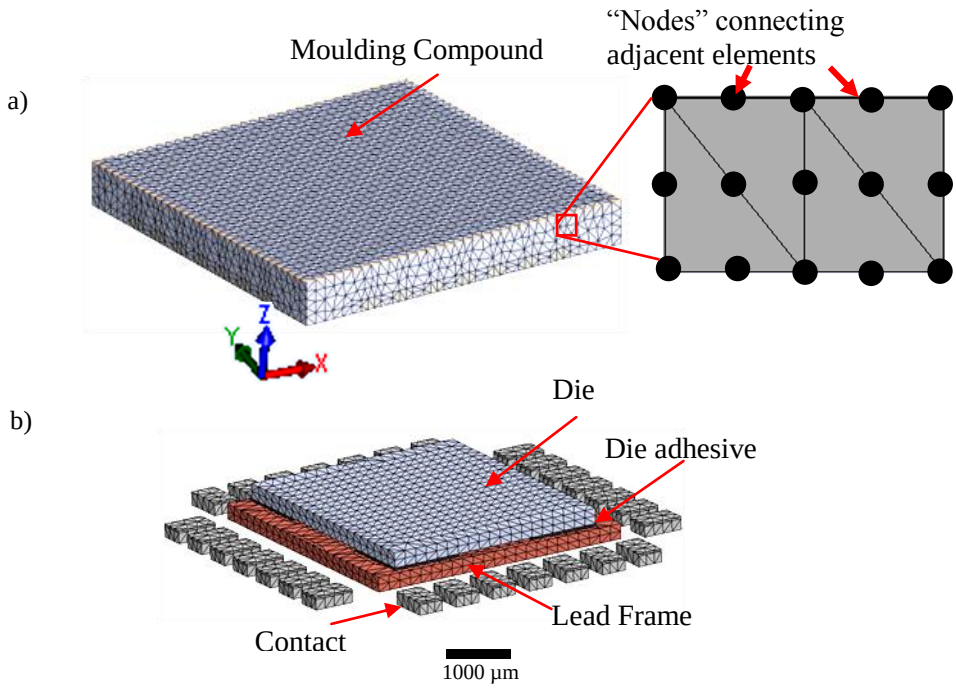


Fig. 6.10 The 3-dimensional FEA model of the UQFN package used in this study a) Fully encapsulated UQFN package, and b) The cap is removed for viewing internal features.

Step 4- <u>Material assignment to each part of the 3D FEA model</u>:

Each part of the 3D FEA model was assigned their respective different material properties, using the Solidworks™ Simulation material library. The properties of the materials used in the FEA simulation are shown in Table 6.2.

Table 6.2 Properties of materials used in FEA simulation [189-192].

Attribute	**Materials**	**Young's modulus (GPa)**	**CTE (10^{-6}/K)**	**Poisson's ratio**
Lead frame/Exposed pad	Copper alloy	110	24	0.370
Die adhesive	Silver Epoxy	12	65	0.394
Die	Silicon	169	2.69	0.3
Cap	Epoxy Resin	2.4	55	0.35

Step 5- <u>Creation of the deformed 3D FEA model:</u>

Mechanical loading was applied to the die adhesive layer (in both x- and y- directions) in order to form a 3D FEA model with warpage (Fig. 6.11b) which is similar to that of experimentally measured results (see Fig. 6.11c)) – a biaxial stress ($\sigma_{xx} + \sigma_{yy}$) of ~ 70 MPa around the region **A** indicated by red arrows in Figs. 6.11b) and 6.11c). This deformed 3D FEA model was used as a model for the simulation study of temperature effects.

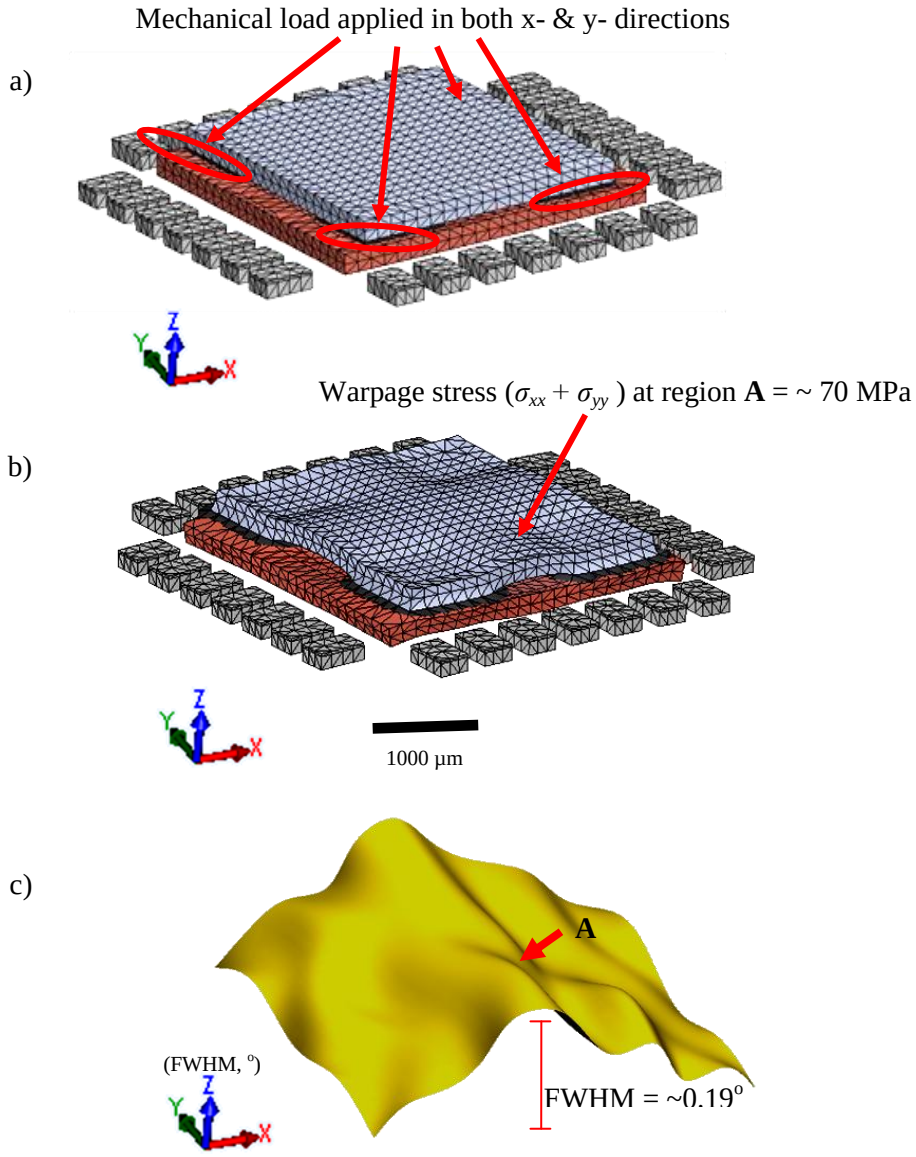


Figure 6.11 a)-b) illustrating the deformed 3D FEA model created by applying the mechanical load to the die adhesive layers, and c) is the XRD/3DSM at phi = 0^{o} obtained from lab-based XRD measurements at 25^{o}C.

Step 6- <u>Effect of thermal loading</u>:

Thermal loading was applied to the deformed 3D FEA model in order to observe the transition of warpage inside the packaged chip. As an example, the simulation result at 115^{o}C is illustrated in Fig. 6.12b).

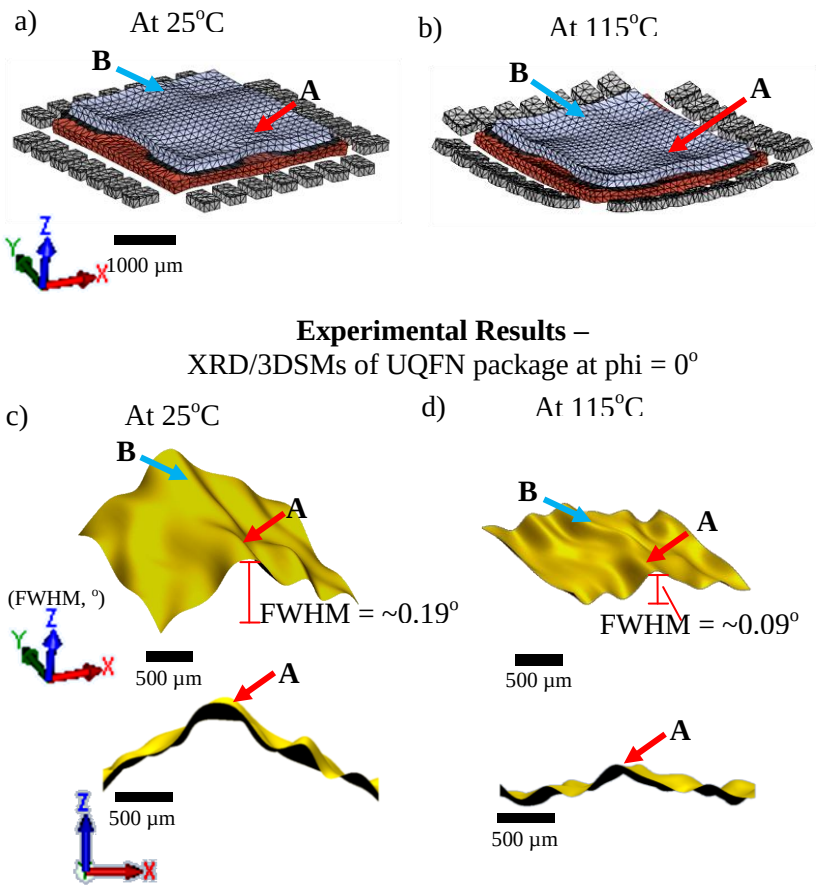


Fig. 6.12 Transition of warpage in the packaged chip as a function of temperature. a) Deformed 3D FEA model at 25°C, b) Deformed 3D FEA model at 115°C, c) and d) are the XRD/3DSMs at phi = 0° obtained from lab-based XRD measurements at 25°C and 115°C, respectively.

For comparison, the distributions of biaxial stress ($\sigma_{xx} + \sigma_{yy}$) across the Si die obtained from FEA simulation at 25°C and 115°C are depicted in Figs. 6.13a)-b), respectively. In addition, the distributions of the biaxial stress ($\sigma_{xx} + \sigma_{yy}$) across the Si die (across the highly distorted region **A** indicated by the red arrow in Fig. 6.13) at the x-z cross section are also shown in Figs. 6.14. From Fig. 6.14a), it is obvious that the upper half and lower half of a warped Si die region are experiencing tensile and compressive stresses, respectively. This

observation has further confirmed the previous assumption used to estimate the biaxial stress from the XRD results, as previously discussed in section 6.3.4. As the thermal load was applied, the underlying copper lead frame expands more rapidly than that of Si die at elevated temperature, and compensates and relaxes the warpage generated initially during the die attach process, as shown in Figs. 6.12, 6.13 and 6.14.

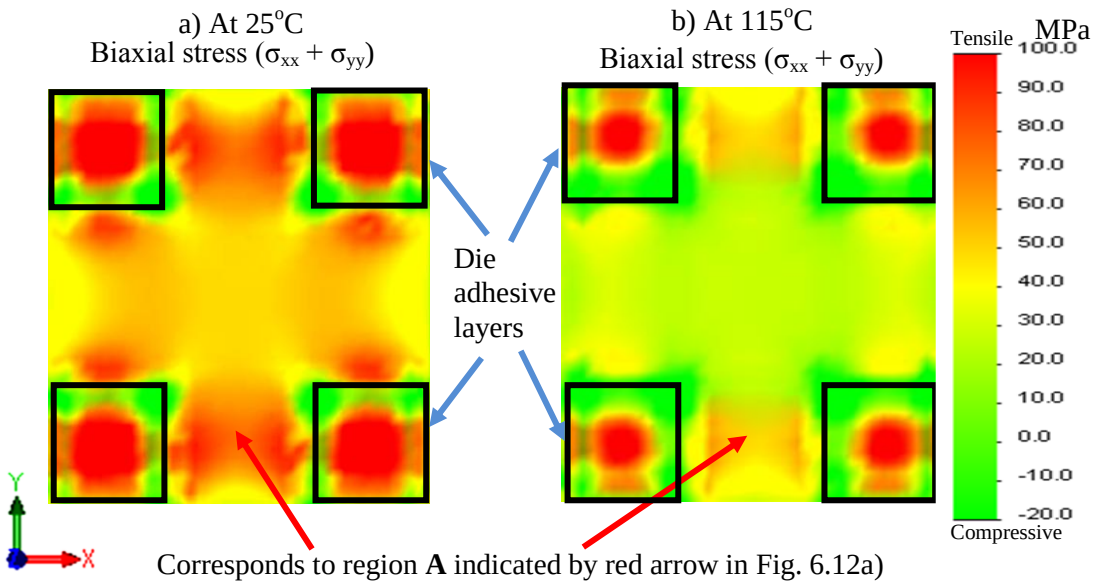


Figure 6.13a)-b) show the distributions of the biaxial stress ($\sigma_{xx} + \sigma_{yy}$) across the Si die obtained from FEA analysis at 25°C and 115°C, respectively.

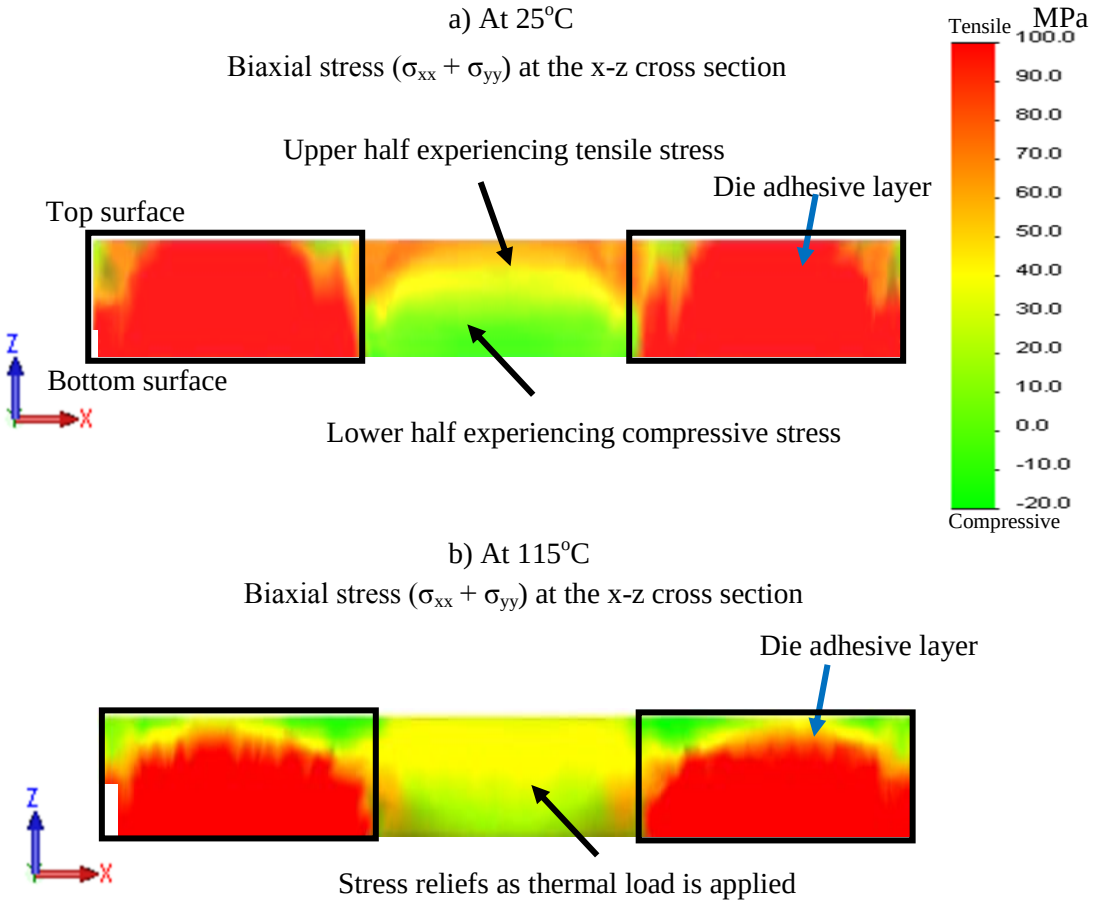


Figure 6.14a)-b) show the distributions of the biaxial stress ($\sigma_{xx} + \sigma_{yy}$) across the Si die at the x-z cross section (across the highly distorted region **A** indicated by red arrow in Fig. 6.13), obtained from FEA analysis at 25°C and 115°C, respectively.

For a deeper comparison, the stress ($\sigma_{xx} + \sigma_{yy}$) extracted from simulations is compared to that of experimental results recorded at phi = 0° (around the regions **A** and **B** indicated by the red and blue arrows in Figs. 6.12, 6.13, 6.14), as shown in Fig. 6.15. The excellent agreement between the simulation and experimental results confirms the aforementioned discussion, where the thermal process-induced strain relief has occurred at elevated temperatures. Therefore, it is believed that most of the stress appears to develop during curing of the die-attach adhesive due to the difference in expansion of the Si die and lead frame, as reported by several authors [177-179, 193].

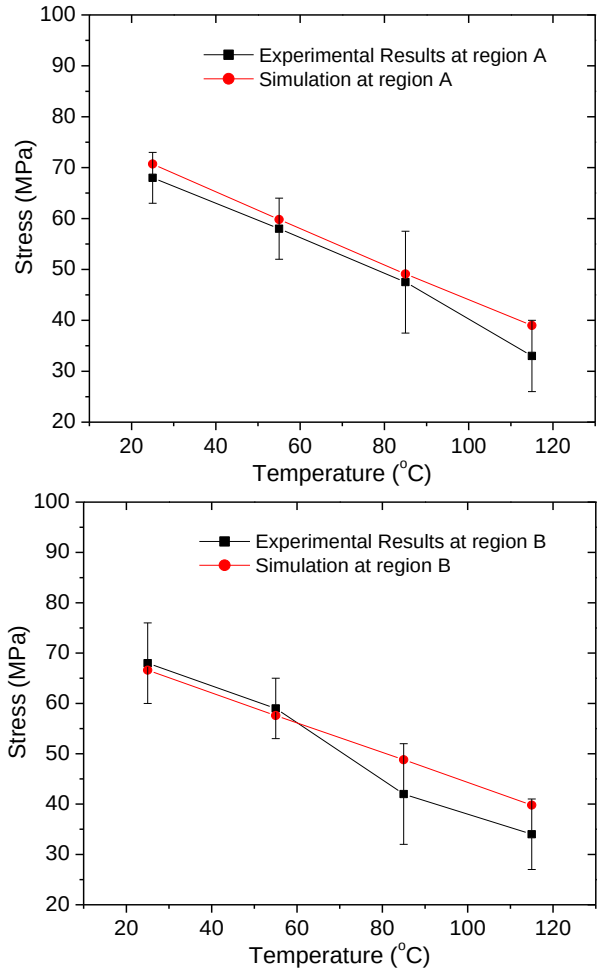


Figure 6.15 Effect of temperature on the stress transition in the silicon die. The stress is measured and calculated around the region A (region B) marked by the red arrows (blue arrows) in Figs. 6.12.

These findings have important implications for the manufacturing and control of stress development in the Si die. Considering the UQFN packages under investigation, it is well known that thermal stress can impact on the reliability and functionality of integrated devices fabricated on a deformed Si die [169, 197, 198]. Therefore, reduction of process-induced stress is a fundamental issue that needs to be addressed for the realisation of high volume 3D IC integration technology for future microelectronics. Diagnosing such stresses will also be key and laboratory-based XRD using 3DSM can serve as a straightforward, non-

destructive and *in situ* characterisation methodology for providing detailed information on the lattice warpage/strain developed in packaged chips including during crucial elevated thermal processing steps.

6.4 Summary

In this chapter we have demonstrated a novel laboratory-based X-ray diffraction analysis technique (XRD/3DSM) which can map major warpage features non-destructively in fully encapsulated packaged chips. Tilt direction and stress can also be evaluated separately from the rocking curve maps and peak deviations between rocking curves measured at two adjacent regions. In the commercially available UQFN packages tested in this study, 3DSM reveals that distortions are considerably lower at the corners of the Si die, but significantly larger at the central regions of the die. *In situ* XRD annealing experiments and FEA simulations confirmed that most of the stress is developed during the die attach process.

The transfer of this technique from a synchrotron X-ray source environment to a laboratory tool makes such lab-based non-destructive imaging and evaluation of warpage/strain characterisation of Si wafer die inside packaged SoC/SiP using XRD/3DSM a realistic possibility within a fab environment.

Chapter 7

Characterisation of Die Stress and Warpage in Embedded Quad-Flat No-Lead (QFN) Packages

7.1 Introduction

The previous chapter has demonstrated the concept of X-ray diffraction 3-dimensional surface modelling (XRD/3DSM) through the implementation of this technique for characterising die stress inside fully encapsulated ultra-thin QFN (UQFN) packages. In order to demonstrate the feasibility of XRD/3DSM in characterising a packaged chip with a more complex structure, I have also applied this technique to investigate embedded QFN packages at different manufacturing processing steps.

7.2 Embedded QFN packages

The second types of package investigated in this study are embedded QFN packages [167, 180], provided by Fraunhofer IZM Berlin. They consist of a 5 mm x 5 mm active die bonded Si chip (50 µm thick), embedded face-up on a substrate, with a peripheral bond pad pitch of 100 µm. The overall dimension of the package is measured to be 10 mm (W) x 10 mm (L) x 160 µm (H) in size (see Fig. 7.1).

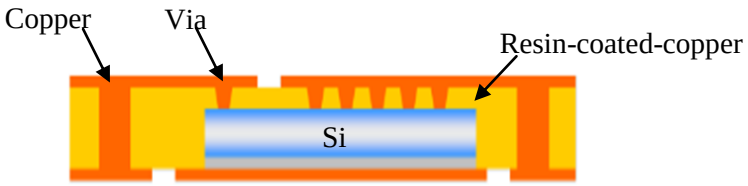


Figure 7.1 Cross-sectional schematic diagram for the embedded QFN package [167, 180].

The five major embedding/processing steps of these embedded QFN packages are listed below [167, 180]:

i) Chip attach – the Si die is bonded onto the core substrate using a 20 µm thick double layered die attach film (DDAF). Prior to the chip attach process, a 6-8 µm thick copper layer was electrolytically deposited on the core substrate.

ii) Embedding by lamination - The die bonded chip is laminated by a ~ 100 µm thick resin coated copper (RCC) dielectric layer from the top side of the chip, using a standard printed circuit board (PCB) multilayer vacuum lamination process.

iii) Microvia drilling – Microvias were drilled through to the chip pads using a pulsed 355 nm UV laser, following by a via cleaning process to remove the residual of epoxy resin in order to ensure good adhesion of the subsequent electroplated copper.

iv) Copper metallisation – A conductive palladium layer was deposited on top of the epoxy surface prior to via electroplating of copper.

v) Structuring of conductor lines – The chip was exposed to negative photoresists by using a laser direct imaging (LDI) system, and followed by an acidic spray etching in order to reveal the Cu line patterning. These Cu lines will serve as connectors to the bond pads, as well as capturing pads on the chip. Finally, the packaging process is complemented by the Cu structuring on the bottom side of the package. These packages were processed in a large panel format and they were separated using a laser or a standard (wafer) saw. More details regarding the QFN chip embedding, assembly and processing steps can be found in references [167, 180]. For the embedded QFN packages, I investigated these packaged chips after two of the most potentially decisive processing steps marked by black rectangular boxes in Fig. 7.2.

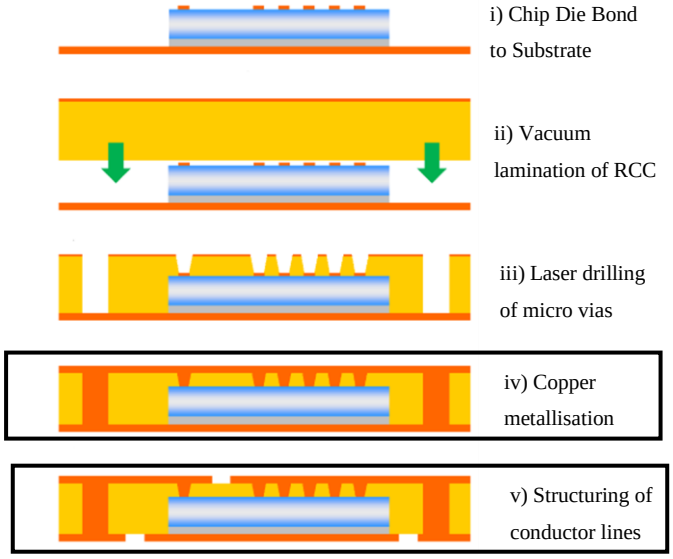


Figure 7.2 Schematic diagram showing the process sequence for embedded QFN package [167, 180].

7.3 Characterisation of die stress and warpage inside embedded QFN packages for selected chip manufacturing process steps

Similar to the UQFN packages, the embedded QFN packages were also characterised using XRD/3DSMs recorded at phi = 0^o and 90^o in order to examine the lattice misorientations of the two orthogonal (110) planes in the Si die. For the embedded QFN package, the FWHM lines were recorded across the Si die using a step size of 200 µm, and therefore the resolution is higher relative to the XRD/3DSM of the UQFN packages, in order to reveal finer detail in the Si die for this more complex embedded package. Each of the XRD/3DSM surfaces is built up from a total of 26 horizontal (phi = 0^o) and 26 vertical (phi = 90^o) FWHM line scans, respectively. During the reconstruction of XRD/3DSM for the embedded QFN packages, additional connectors were added between two adjacent splines. This was done to allow a more precise flow of the boundary surface between adjacent splines with a large change in slope [38, 199]. The estimated scan time for each XRD/3DSM is approximately ~ 15 hours (more details are shown in Table 7.1).

Table 7.1 Details and estimated scan time for each XRD/3DSM.

Type of scan	**Details**			
004 Rocking curve	**Sampling step size**	**Count time per point**	***ω*-scanning range**	**Approximate scan time per RC**
	0.01^{o}	0.2 sec	3.5^{o}	80 sec
FWHM line scan	**Distance between two RCs were recorded**			**Approximate scan time per FWHM line scan**
	200 micron			31 minutes
XRD/3DSM	**Distance between two FWHM line scans were recorded**			**Approximate scan time per map**
	200 micron			15 hours

Chip die bond to substrate, vacuum lamination, laser drilling of microvias, copper metallisation and structuring of conductor lines are the five major embedding/processing steps of these embedded QFN packages. To reiterate, I have focused on characterisation at two stages of embedded QFN manufacture, as shown in Fig. 7.2.

7.3.1 Copper metallisation

During the first of these, copper metallisation, the Si die is laminated by a ~ 100 µm thick RCC dielectric layer and covered entirely by a copper layer. Fig. 7.3 is an optical image of the embedded QFN package after copper metallisation, showing an embedded Si die fully encapsulated by the copper layer.

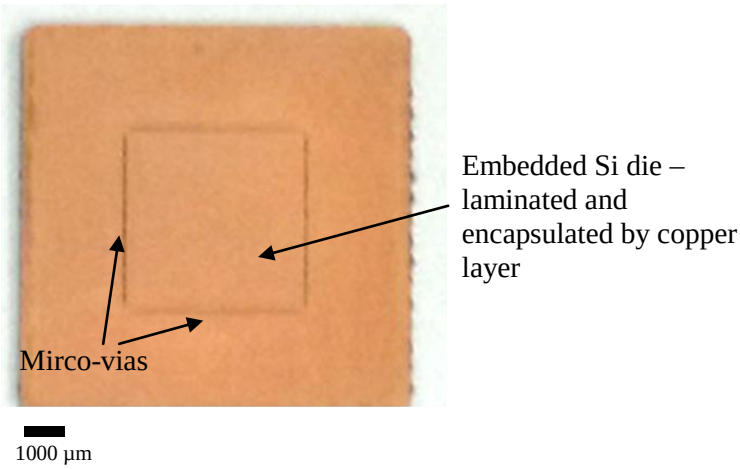


Figure 7.3 An optical image of the embedded QFN package after copper metallisation of micro-vias.

Figs. 7.4a)-b) show the XRD/3DSMs of a typical chip following copper metallisation recorded at phi = 0^o and 90^o, demonstrating lattice misorientation/deformation of (110) planes in the Si chip. From Figs. 7.4a)-b), it is obvious that a distinctive 'rippled' profile with a peak-to-peak pitch of 550 – 600 µm has developed up to or during this processing step. Lattice misorientations are higher around the edges of the Si die ($FWHM_{max}$ = 0.44^o ± 0.02^o), corresponding to an estimated stress in the range ~ 90 MPa - 140 MPa, which are marked by red ovals in Figs. 7.4a)-b). The development of these features is thought to be due either to the microvia laser drilling process or the vacuum lamination process.

In order to confirm this, an X-ray radiographic image of the chip after copper metallisation is shown in Fig. 7.4c). The X-ray radiographic image clearly demonstrates the cross-hatch pattern across the entire QFN package. This is almost certainly a result of the fibreglass weave pattern of the core substrate. The dimension of this cross-hatch pattern is measured to be ~ 550 - 600 µm, which correlates well to the peak-to-peak pitch of the 'rippled' profile observed from XRD/3DSM. Note that, while X-ray radiography reveals this ripple pattern, it is unable to quantitatively reveal stress or warpage, as XRD/3DSM can. The

lattice deformation developed after copper metallisation is thought to be due to vacuum lamination process-induced stress, as these features are not consistent with the patterning of the microvias, which are located around the periphery of the Si die (see Fig. 7.4c). During the lamination process, the die bonded Si chip on the core substrate is covered from the top side with an RCC layer in a pressurised chamber. A pressure > 12 bar is required to ensure sufficient flow of the RCC dielectric in order to prevent the formation of voids around the chips [172]. It is likely that stress is generated during this process as a consequence of the use of high pressure. The Si chip will be pressed against the substrate due to the clamping force, leading to the development of a distinctive 'rippled' profile on the Si chip, following the fibreglass weave surface morphology of the core substrate.

In addition, the embedded QFN package was also examined using synchrotron X-ray topography (SXRT) in order to reveal the type and extent of lattice misorientations formed in the Si die. Fig. 7.5 shows the $\bar{1}17$ LABR topograph of the package after the copper metallisation of vias, which comprised of 24 optical microscopy images patched together, captured from two different topographs. The contrast discontinuities in the topograph are due to the lattice misorientations in the Si die. This is again thought to be related to the "ripple" profile features discussed in previous section, in which these features formed as a consequence of strain-induced tilt, created during the lamination process. Considering a deformed Si die with "ripple" profile features, the diffracted intensities will be respectively focused and defocused for "convex" and "concave" types of misorientations (see Fig. 7.6). Therefore, the diffracted intensities will be recorded at slightly different positions on the topograph due to the deviation of the Bragg angles, creating distinctive bumpy features (darker contrast in the topograph shown in Fig. 7.5) across the embedded chip. From the LABR topograph, the bumpy features around the central region of the chip consistently showing a peak-to-peak pitch of ~ 850 μm. The shape of these features are however vary

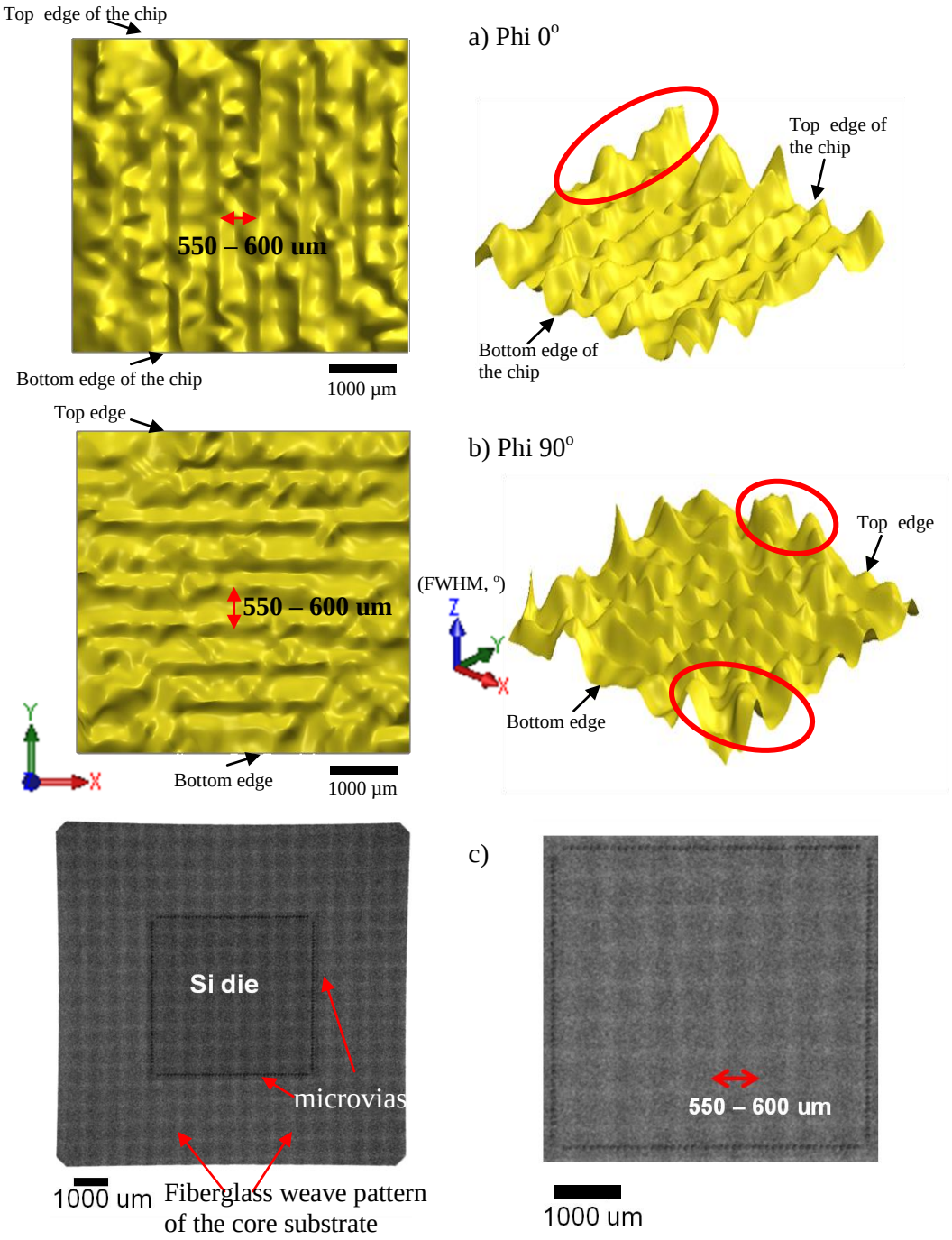


Figure 7.4 a)-b) are, respectively, the XRD/3DSMs of a QFN chip recorded at phi = 0° and 90°, from different viewpoints (left/right), illustrating lattice deformation of the (110) planes in the Si chip after copper metalisation, and c) X-ray radiographic image of package after copper metallisation showing the embedded chip and microvias located around the edges of the embedded Si die (right, shows a magnified view of the centre of the left image).

significantly as we approach the edges of the Si die, especially towards the edges of the right corner of the Si die- with the feature size/pitch approaching ~ 1000 μm, as shown in Fig. 7.5. This observation explicitly shows a phenomenon where the larger magnitude of lattice misorientation around the right corner edge of the chip causes the X-rays to diffract at slightly different diffraction angles (see Fig. 7.6). This is consistent with the results obtained from lab-based XRD measurements, where the lattice misorientations are higher around the edges.

These observed feature sizes from the topographs (~850 to ~ 1000 μm) is nonetheless different to that of the fibreglass substrate induced weave feature sizes of ~550 – 600 μm measured from lab-based XRD. This is thought to be due mainly to these images being formed by different mechanisms for these different techniques. Considering the LABR topographs, the feature size is estimated from the diffraction pattern recorded on the topograph formed by the diffracted intensities arising from the misoriented crystal planes in the deformed Si die. As shown in Fig. 7.6, the diffraction intensities will be recorded at slightly different locations on the topograph depending on the magnitude of lattice misorientation across the Si die, and therefore it will be difficult to predict the actual feature size of the deformed Si die from the topograph. In contrast, the warpage map of the lab-based XRD/3DSM is plotted using the FWHM extracted from the RC recorded at each x-y position across the Si die, for which the largest FWHM corresponds to the highly distorted region of the chip. In other words, the feature size of the deformed chip will be reflected through the change of RC FWHM measured at each x-y position due to the variation of magnitude of lattice misorientations, but not the different diffracted positions recorded on the topograph, as is the case for the LABR technique. From this point of view, XRD/3DSM seems to be a better technique for providing detailed information or to pinpoint the precise location of the lattice warpage developed in packaged chips.

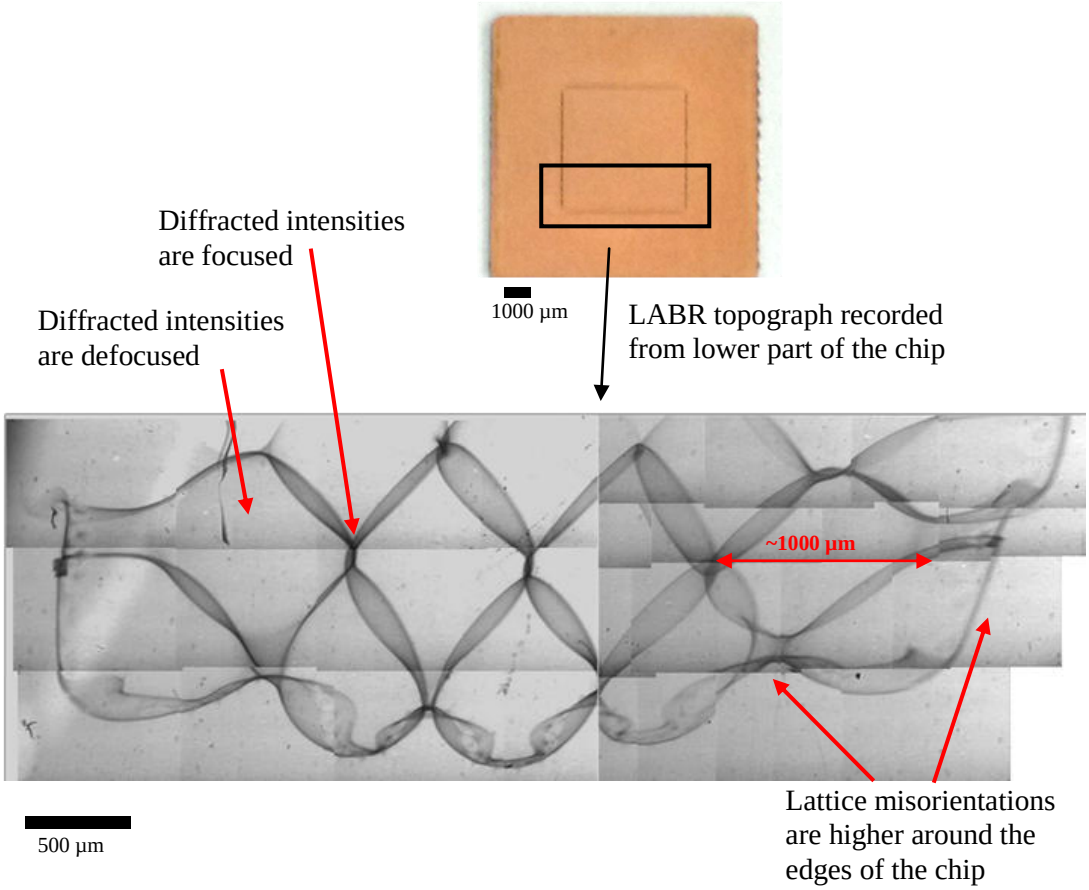


Figure 7.5 $\bar{1}17$ large area back reflection topography (bottom image) of the embedded QFN package after the copper metallisation of vias, recorded from the lower part of the chip marked by a black square box in the optical image (top image).

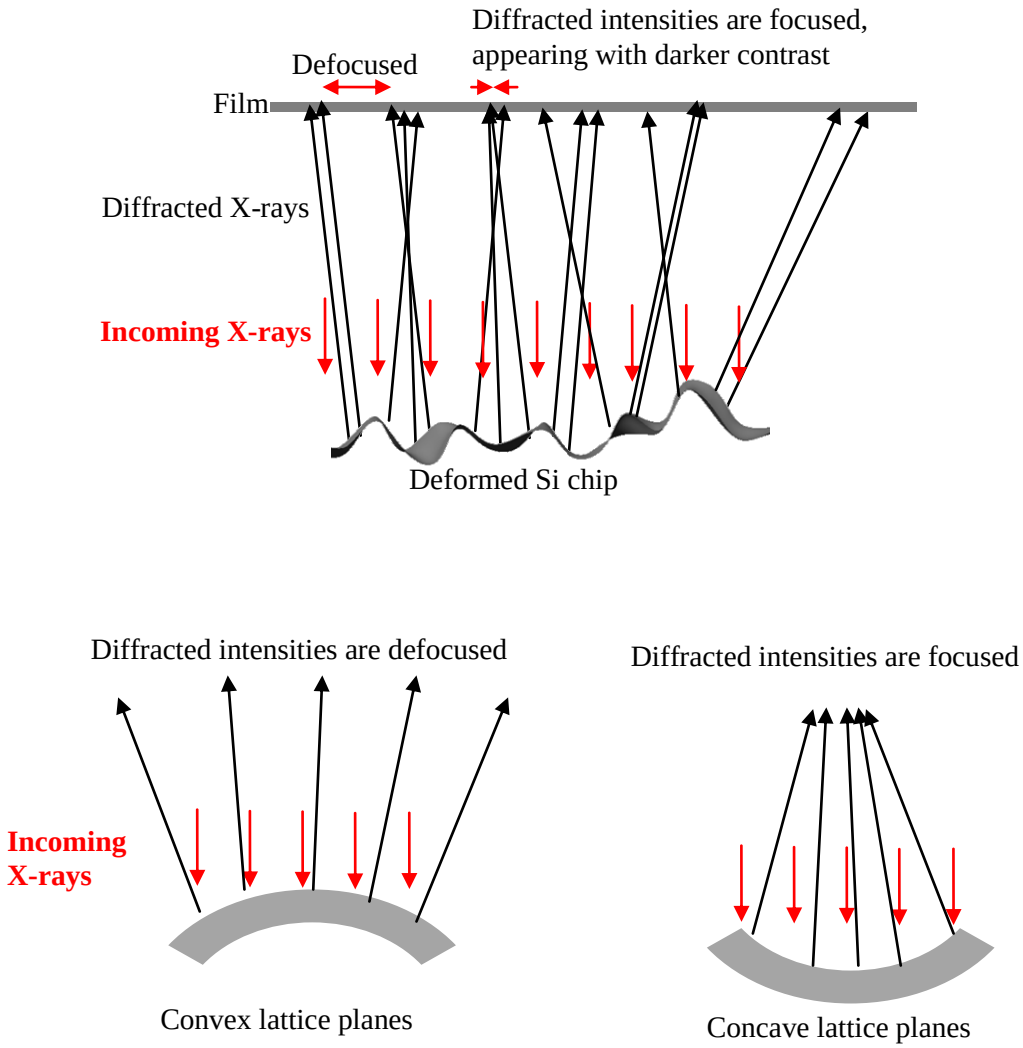


Figure 7.6 The diffracted intensities are focused and defocused due to the strain-induced tilt, arising from a deformed Si chip.

7.3.2 Structuring of conductor lines

The final processing step (see Fig. 7.2) of the embedded QFN package is the Cu structuring on the bottom side of the package. The XRD/3DSMs recorded at phi = 0^{o} and 90^{o}

are shown in Figs. 7.7a)-b), respectively, clearly illustrating that different types of lattice deformation/warpage have developed after this processing step. The stresses in the highly distorted regions ($FWHM_{max} = 0.48^{o} \pm 0.02^{o}$) are estimated to have increased slightly to ~120 MPa - 170 MPa, corresponding to the region marked by a red ellipse in the warpage map.

The large warpage developed after structuring of conductor lines is thought to be linked to manufacturing induced-stresses, which may result from two major factors. Firstly, the placement accuracy during the die bonding or die placement process has been reported to be one of the most crucial processes for chip embedding [172]. This is because a small misalignment of chip position can potentially result in insufficient support from either the top or bottom surface of the chip [38, 172], and subsequently leads to warpage. In addition, the CTE mismatch between silicon and copper-filled TSVs can also induce thermo-mechanical stress, leading to material deformation, delamination and cracking in the packaged chip [173, 174]. These results agree well to that of results previously obtained using 3DSM technique performed using synchrotron radiation source, in which a similar warpage feature has been observed for the chip after the final processing step [38].

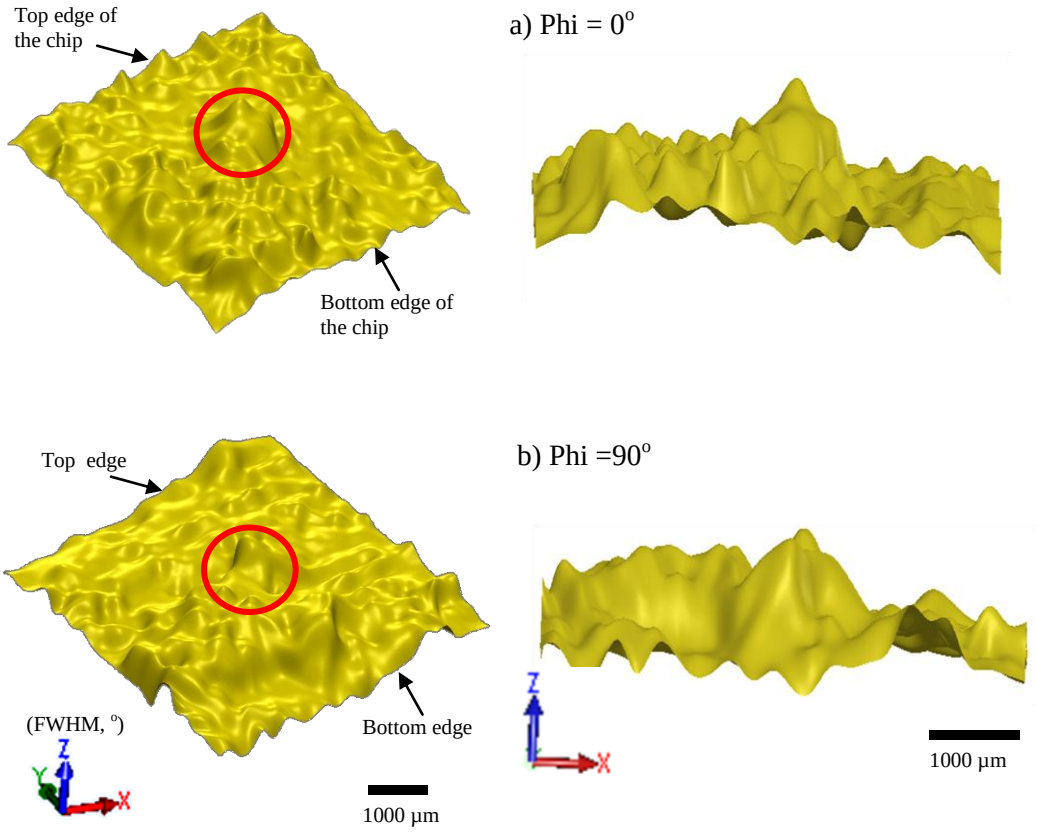


Fig. 7.7a)-b) are the XRD/3DSMs recorded at phi = 0° and 90°, respectively, from different viewpoints (left/right), showing warpage/lattice deformation of the (110) planes inside the packaged chips after the structuring of conductor lines.

Fig. 7.8 shows the $\bar{1}17$ LABR topograph of the embedded QFN package after structuring of conductor lines, which is patched from optical images captured from two different topographs. The highly distorted region is identified to be the central region of the darker elliptical feature (denoted by E) in the topograph - the bottom left part of the chip. This feature is formed on the topograph by the same diffraction mechanism as previously discussed, in which the diffracted intensities from the highly distorted region are "defocused" and recorded at slightly different position on the film, appearing to be lighter on the topograph due to intensity loss. As a result of this the images around the central region are not

included due to the difficulty of patching these together due to a lack of patterning/features on the topographs. The LABR result correlates well to that of the warpage map obtained from the lab-based XRD/3DSM, which confirmed that the development of large warpage is mostly linked to the manufacturing process induced stress.

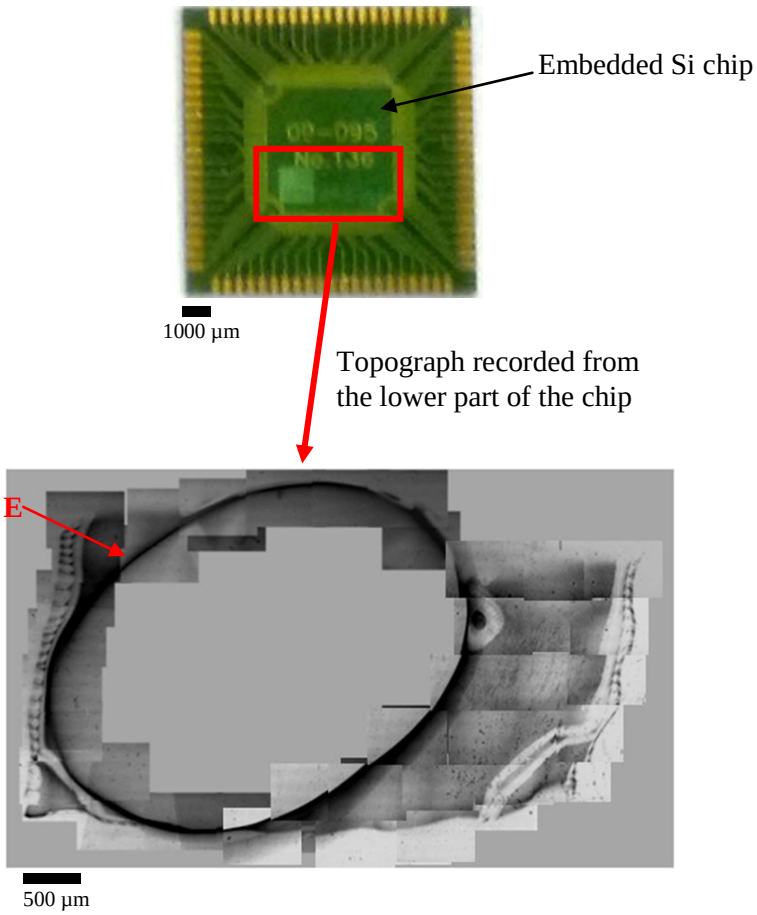


Figure 7.8 $\bar{1}17$ large area back reflection topography (bottom image) of the embedded QFN package after the structuring of conductor lines, recorded from the lower part of the chip marked by red square box in the optical image (top image).

7.4 Summary

The feasibility of the lab-based XRD/3DSM technique has been further confirmed through the characterisation of die stress inside fully encapsulated QFN packaged at various

stages of the chip manufacturing process. For the embedded QFN packaged under investigation, different magnitudes of stress/warpage are generated during different manufacturing processes. More specifically, XRD/3DSM clearly revealed major changes of lattice misorientation/warpage in the Si die after the structuring of conductor lines from the manufacturing process steps for copper metallisation.

The novel lab-based XRD/3DSM technique can serve as a straightforward, non-destructive and *in situ* characterisation methodology in an attempt to gain a better understanding of the sources and distribution of strain inside packaged chips, and thereby help to improve the manufacturing efficiency, performance and reliability of advanced packaging products.

Chapter 8

Conclusions and Future Work

8.1 Conclusions

The aggressive scaling of silicon (Si) complementary metal-oxide-semiconductor (CMOS) technology for the past 40 years has resulted in greater integrated circuit (IC) functionality and improvements in metal-oxide-semiconductor field-effect transistor (MOSFET) performance helping to fulfil the demands of a modern technological society. Nonetheless, traditional Si CMOS scaling is becoming increasingly difficult as physical limits are approached at the 16 nm node and beyond. A significant issue is the limited charge carrier mobility in Si, and so new channel materials that carry relatively higher mobility carriers have been used, such as strained Si. Other materials such as gallium arsenide (GaAs), indium gallium arsenide (InGaAs) and germanium (Ge) are currently under consideration for replacing the conventional Si channel for next generations of low power and high speed electronics. The continued downscaling of CMOS technology following this route is defined by the International Technology Roadmap for Semiconductor (ITRS) as the "More-Moore" (MM) approach. However, challenges still remain for the realisation of high quality III-V material on Si for CMOS devices because the tolerance to dislocations is very low ($<10^5$ cm^{-2}).

As previously discussed in Chapter 3, the most common issues that have to be overcome for the realisation of high quality III-V materials on Si substrates are anti-phase domains, dislocations, strain and lattice tilt distributed within the III-V layers due to their crystal dissimilarities. A non-destructive X-ray characterisation routine which can be used to effectively help III-V growers in tackling these problems has been designed. The significant benefit of X-ray techniques is that they are non-invasive, thereby allowing the same sample to

be measured a number of times, allowing comprehensive information to be extracted. The feasibility of the X-ray characterisation routine has been demonstrated through the characterisation of a series of deliberately fabricated "problematic" (with defects such as antiphase domains (APDs), dislocations, strain/relaxation, lattice tilts) GaAs materials deposited on Ge and Si substrates, using Metal-Organic Vapour Phase Epitaxy (MOVPE) under various growth conditions.

A range of these X-ray characterisation routines has been used to investigate GaAs heterostructures deposited on Ge and Si substrates, as summarised in Table 4.5. Considering the GaAs/Ge samples under investigation, synchrotron X-ray topography (SXRT) and triple-axis high-resolution X-ray diffraction (HRXRD) revealed increasing dislocation density and degree of relaxation in the thicker GaAs epilayers (samples C, D and E). In contrast, thin (600 nm) films (samples A and B) showed few dislocations and very little relaxation. This result implies a lack of correlation between the dislocation density and the nucleation routine. Conversely, triple axis HRXRD ω-scans, atomic force microscopy (AFM) and transmission electron microscopy (TEM) measurements showed that the surface roughness is closely correlated to the APD sizes formed in the GaAs crystal. The formation of large APDs led to rougher surface morphologies. Raman and PL measurements were unable to detect dislocations at the GaAs/Ge interface due to the laser penetration depth being ~90 nm in GaAs, but did allow for near-surface defectivity measurements.

GaAs/Si samples were found to be very defective. This is as expected for III-V material deposited directly on a Si substrate due to the large lattice mismatch. Dislocation density estimation using SXRT and crystallinity evaluation using triple-axis HRXRD are inapplicable for this type of sample due to the limited SXRT spatial resolution of ~ 3 μm and diffraction intensities produced by the highly mosaic GaAs crystals being too weak to be detected, respectively. However, different versions of the characterisation routines can be

implemented for detailed analysis of this defective sample. Double-axis HRXRD ω-2θ scans reveal the existence of some relaxed epitaxial GaAs present in the overlayer. Powder diffraction and X-ray crystallographic mapping confirm the presence of some epitaxial GaAs preferentially oriented along [001] embedded in the highly-textured polycrystalline structure.

Overall, this work demonstrates the importance of using a series of appropriate characterisation methodologies for identifying the presence of different crystal defects or the significant effects of each growth process. X-ray techniques can serve as a rapid characterisation methodology to help III-V growers in gain a greater understanding of various issues associated with heteroepitaxial growth, material properties, and optimal growth processes towards the achievement of low defect density III-V layers of device quality ($< 10^5$ cm^{-2}).

According to industry experts, the future of modern nanoelectronics may well depend on a second trend, which is the implementation of diverse functionality within modern ICs. This "More than Moore" (MtM) approach will be realised through the manufacture of complex Systems on Chip (SoC) and Systems in Package (SiP), evolving towards fully three-dimensional ICs (3D ICs). However, progress in this direction is hampered by the lack of a compelling metrology in order to measure non-destructively and *in situ* the process induced warpage, strain and other defects inside silicon die. Therefore, a novel laboratory-based technique called X-ray diffraction 3-dimensional surface modelling (XRD/3DSM) has been developed in order to address this major stumbling block in the development of "More than Moore" (MtM) integrated circuit technology.

XRD/3DSM has been domenstrated at room temperature and at elevated temperatures up to 115^{o}C by *in situ* XRD annealing experiments. The feasibility of the technique has been confirmed through the characterisation of die stress inside both the fully

encapsulated commercially available ultra-thin quad flat no-lead (UQFN) packages and the embedded QFN packages at different manufacturing of processing stage.

The lattice misorientations of two (110) orthogonal planes in the Si die created during packaging processes can be obtained via the reconstruction of 004 symmetric rocking curve (RC) full-widths-at-half-maximum (FWHMs) as a function of position across fully encapsulated packages performed at phi = 0^o and 90^o, using the lab-based XRD/3DSM technique. More importantly, the warpage stress can also be quantitatively estimated using the angular offset between the peak positions of RCs measured at two adjacent regions, and the map of warpage stress across the entire Si die can also be reconstructed using the same XRD/3DSM technique.

In the commercially available UQFN packages tested in this study, XRD/3DSM reveals that warpage is considerably lower at the corners of the Si die, but significantly larger at the central regions of the die. Most of the stress is found to be developed during the die attach process, in which these have been confirmed by *in situ* XRD annealing experiments and finite element analysis simulations. XRD/3DSM has also been implemented for the investigation of die stress in a more complex embedded QFN package, which clearly reveals that different magnitudes of stress/warpage are developed during different embedding/packaging process. From SXRT have confirmed and validated the results obtained from the lab-based XRD/3DSM.

Results have demonstrated that lab-based XRD/3DSM is a promising technique which can be used to deliever useful feedback to the manufacturer for packaging process optimisation. Importantly, it is a non-destructive method and can be used for packaged systems all the way from virgin wafer pieces through various packaging steps to the completed package.

8.2 Future Work

The X-ray characterisation routine has been shown to be very useful for investigating the structural quality of the III-V heterostructure throughout the film in its entirety. Future work could focus on the grazing-incidence X-ray diffraction (GIXRD) technique. In grazing-geometry, the incident X-ray beam makes a very small angle with the sample surface where the penetration depth is limited to a few tens of nm, and this technique is very surface-sensitive. Therefore, the inclusion of GIXRD techniques will certainly make the X-ray characterisation routine more valuable i.e. it can be used not only for characterising the film quality in its entirety, but also for surface characterisation.

Concerning the lab-based XRD/3DSM technique, there are several different aspects of exploration that are possible in order to improve the XRD/3DSM technique for future metrology challenges:

i) Resolution of XRD/3DSM

The resolution of the XRD/3DSM method is dependent on two major aspects: i) The spatial resolution of the incident X-ray beam, and ii) The step size between two FWHM line scans. The existing XRD/3DSM technique was built using the FWHM extracted from RCs recorded using a 250 μm x 250 μm incident X-ray beam. Further improvement of spatial resolution is achievable by using a small beam size, i.e. a 100 x 100 μm^2 or 50 x 50 μm^2 beam size could be used. In addition to that, a reduced beam size could also be used together with a smaller step size (distance between two FWHM line scans) in order to further improve the resolution of the XRD/3DSM model.

ii) The scan time of XRD/3DSM model

The scan time of the lab-based XRD/3DSM is dependent mainly on the number of data points (RC FWHM) of the surface map. More specifically, it actually depends on how long it takes to measure a single RC. One obvious method to reduce the scan time of a RC is by using a smaller count time (exposure time). The existing RC was recorded using a 0.2 second count time in order to achieve an adequate signal-to-noise ratio (S/N), but a further decrease in count time would mean a reduction in S/N, and therefore the RC pattern would almost certainly be too noisy to analyse. However, the loss in S/N can be compensated for if we are able to increase the intensity of incident X-ray beam. A possible way is to further increase or optimise the voltage or current settings of the X-ray source from current values of 45 kV, 40 mA to some point below the maximum limit of 60 kV, 55 mA, or indeed to replace the existing X-ray source with a more powerful X-ray source. With the improved incident X-ray intensity, the diffracted intensities collected from the specimen with respect to the background noise will be increased drastically, and therefore a very smooth and clean RC can be obtained even when a smaller count time is used (eg. see Table 8.1).

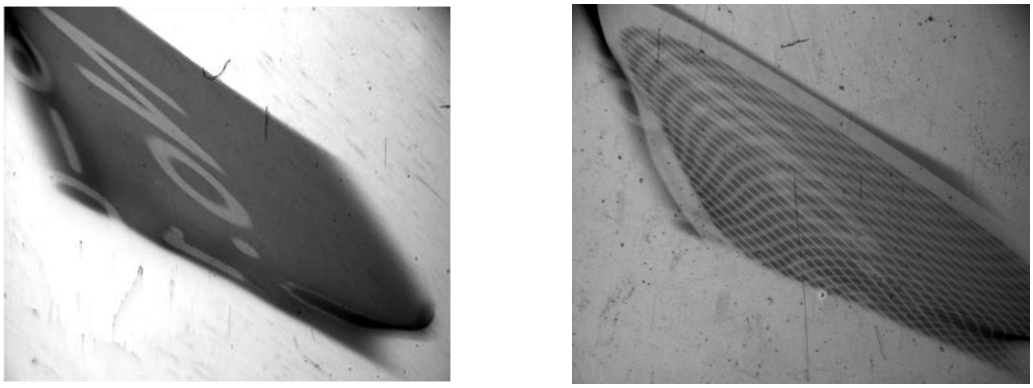
Table 8.1 Estimated scan time for each XRD/3DSM with different X-ray intensity sources.

Chip size (mm)		**Scan step size (mm)**		**Beam size (mm)**	**Count time per point (s)**	**Approximate scan time for each XRD/3DSM**	**Notes**
x	**y**	**x**	**y**				
XRD with current X-ray intensity							
5	5	0.20	0.20	0.25	0.2	15 hours	High resolution
5	5	0.20	0.40	0.25	0.2	7 hours	Med. resolution
5	5	0.20	0.80	0.25	0.2	3.5 hours	Low resolution
XRD with higher X-ray intensity							
5	5	0.20	0.20	0.25	0.05	90 minutes	High resolution
5	5	0.20	0.40	0.25	0.05	45 minutes	Med. resolution
5	5	0.20	0.80	0.25	0.05	20 minutes	Low resolution

Another possible way to reduce the scan time is to perform reflection topography by using the same D1 system with the topography accessory. In order to ensure that as much of the crystalline region as possible is in the Bragg diffraction condition most, if not all, of the beam conditioning at the X-ray source should also be removed. This would ensure that the emergent beam is as polychromatic and divergent as possible in order to mimic the presence of a white beam. A relatively thin slit (eg. 50 μm x 3 mm) could be used to record a series of topograph images across the entire Si die, and these images could be reconstructed using 3DSM technique to form the warpage model.

Apart from that, a fine meshed slit system could also be used to perform X-ray Reticulography [200]. An early proof-of-concept series of X-Ray Reticulography experiments for the non-destructive examination of warpage in packaged chips has been demonstrated using the SXRT technique [200]. In these experiments, the meshed slit is located between the

incoming X-rays and the sample in order to initially decompose the incident beam into a series of micro-beams. For instance, Figs. 8.1a)-b) show the transmission topograph and transmission X-ray recticulograph for a fully encapsulated Si chip inside a QFN package. From Fig. 8.1b), the deviations from the periodic regularity of the mesh pattern reflect localised lattice misorientation in the packaged chip. These earlier results have demonstrated the potential of this technique, and therefore it is believe that this technique could ultimately be transferred into the laboratory.



a) b)

Figure 8.1a) $\bar{3}\bar{1}1$ transmission topograph image of a QFN packaged chip, and b) $\bar{3}\bar{1}1$ X-ray transmission recticulograph of the same region as in a).

iii) XRD/3DSM Optimisation

As previously discussed in section 5.2, the warpage model of XRD/3DSM was made up of RC FWHM extracted by using *"Quick graph"*. However, data fitting using *"Quick graph"* might be too time consuming to extract the all the data for future high resolution XRD/3DSM model, and therefore other software might be needed to improve the efficiency of this technique, as well as making this technique more user-friendly. Programming languages such as C/C++ or Matlab could be used to write a more sophisticated software in order to automatise the data fitting process.

iv) Other applications

In the future this technique will be expanded to measure more sophisticated packaging technologies as they become available. These include the implementation of this technique for characterising the die stress/warpage inside advanced packages such as SoC, SoC/SiP and 3D-SiP or even for the characterisation of die stress inside microelectromechanical systems (MEMS).

In addition to that, the continuous increase in demand and the advancement of technology is ensuring that power integrated circuits (eg. power MOSFETs) play an important role in order to control the generation, distribution, storage and use of energy more effectively [201]. However, the thermal stresses generated due to the CTE mismatch in package materials has also been identified as a major obstacle to the development of power electronic devices. Therefore, this technique could be used to monitor thermal stress/warpage in power integrated circuits to provide quick feedback towards process improvement in order to improve their efficiencies.

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List of Publications

Main publications

1. **C.S. Wong**, N.S. Bennett, D. Manessis, A. Danilewsky, P.J. McNally, "Non-Destructive X-Ray Diffraction Techniques for Analysis of Die Warpage and Stress Inisde Fully Encapsulated Packaged Chips", Proc. China-Ireland International Conference on Information and Communications Technologies (CIICT 2013), Beijing, China, April 2013, ***submitted.***

2. **C.S. Wong**, N.S. Bennett, D. Manessis, A. Danilewsky, P.J. McNally, "Non-Destructive Laboratory-Based X-Ray Diffraction Mapping of Warpage in Si Die Embedded in Packaged Integrated Circuits", Microelectronic Engineering, ***submitted to journal.***

3. **C.S. Wong**, N.S. Bennett, D. Allen, A. Danilewsky, P.J. McNally, "A Novel X-ray diffraction technique for analysis of die stress in side fully encapsulated packaged chips", Proc. 4th Electronics System Integration Technologies Conference (ESTC 2012), Amsterdam, The Netherland, Sept 2012, ***pending publication.***

4. **C.S. Wong**, N.S. Bennett, B. Galiana, P. Tejedor, M. Benedicto, J. M. Molina-Aldareguia, P.J. McNally, "Structural investigation of MOVPE-grown GaAs on Ge by X-ray techniques ", Semicond. Sci. Technol. 27 (2012), 115012**.**

5. **C.S. Wong**, N.S. Bennett, P.J. McNally, B.Galiana, P.Tejedor, M. Benedicto, J.M. Molina-Aldareguia, S. Monaghan, P.K. Hurley, K. Cherkaoui, "Multi-technique characterisation of MOVPE-grown GaAs on Si", Microelectronic Engineering 88 (2011) 472.

6. N.S. Bennett, **C.S. Wong**, P.J. McNally, "Counting Misfit Dislocations in MOVPE-Grown GaAs on Ge at HASYLAB using Synchrotron X-Ray Topography", HASYLAB Annual Report 2010.

Other publications

1. M. Lubwama, B. Corcoran, K.V. Rajani, C.S. Wong, J.B. Kirabira, A. Sebbit, K.A. McDonnell, D. Dowling, K. Sayers, Surface & Coatings Technology,
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2. P.J. McNally, D. Allen, **C.S. Wong**, N.S. Bennett, A.N. Danilewsky, "X-Ray Diffraction Reticulography for the Non-Destructive Analysis of Deformation and Strain Fields for Silicon Indents and Packaged Integrated Circuits", HASYLAB Annual Report 2013.

3. P.J. McNally, N. Bennett, **C.S. Wong**, A. Cowley, A.N. Danilewsky, "New X-ray Diffraction Reticulography Concepths for the Non-Destructive Analaysis of Warpage in Packaged Si Integrated Circuits", HASYLAB Annual Report 2011.

Conference presentations

1. **C.S. Wong**, N.S. Bennett, D. Manessis, A. Danilewsky, P.J. McNally, "Non-Destructive X-Ray Diffraction Techniques for Analysis of Die Warpage and Stress Inisde Fully Encapsulated Packaged Chips", China-Ireland International Conference on Information and Communications Technologies (CIICT 2013), Beijing, China, April 2013.

2. **C.S. Wong**, N.S. Bennett, D. Manessis, A. Danilewsky, P.J. McNally, "A Novel X-ray diffraction technique for analysis of die stress in side fully encapsulated packaged chips", RINCE Research Day, Na Fianna, Mobhi Road, Dublin (16 January 2013).

3. **C.S. Wong**, N.S. Bennett, D. Allen, D. Manessis, A. Danilewsky, P.J. McNally, "Non-destructive laboratory-based X-ray diffraction image (XRDI) mapping of warpage in Si die embedded in packaged integrated circuits", 4th Electronics System Integration Technologies Conference (ESTC 2012), Amsterdam, The Netherland (Sept 2012).

4. N.S. Bennett, **C.S. Wong**, P.J. McNally, S. Monaghan, P. Hurley, K. Cherkaoui, "Structural and Optical Properties of Post-Annealed Atomic-Layer-Deposited HfO_2 Films on GaAs", Intel European Research and Innovation Conference, Dublin, Ireland (2012).

5. N.S. Bennett, **C.S. Wong**, P.J. McNally, S. Monaghan, P. Hurley, K. Cherkaoui, "Structural and Optical Properties of Post-Annealed Atomic-Layer-Deposited HfO_2 Films on GaAs", European Materials Research Society Spring Meeting, Strasbourg, France (2012).

6. **C.S. Wong**, N.S. Bennett, B.Galiana, P.Tejedor, M. Benedicto, J.M. Molina-Aldareguia, S. Monaghan, P.K. Hurley, K. Cherkaoui, and P.J. McNally, "Characterisation of III-V layers by epitaxial lateral overgrowth on nanostructured substrates", European Materials Research Society/Materials Research Society Bilateral Conference on Energy Spring Meeting, Nice, France (2011).

Posters

1. M. Benedicto, B. Galiana, H. Stange, I. Cornago, J. Bravo, E. Bravo, J.M. Molina-Aldereguia, S. Monaghan, K. Cherkaoui, P.K. Hurley, **C.S. Wong**, N.S. Bennett, P.J. McNally, P. Tejedor, "Thermal stability analysis of HfO_2/GaAs nanopatterns fabricated by laser interference nanolithography and selective dry etching", European Materials Research Society/Materials Research Society Bilateral Conference on Energy Spring Meeting, Nice, France (2011).

2. **C.S. Wong**, N.S. Bennett, B.Galiana, P.Tejedor, M. Benedicto, J.M. Molina-Aldareguia, S. Monaghan, P.K. Hurley, K. Cherkaoui, and P.J. McNally, "Characterisation of III-V layers on Si and Ge substrates by epitaxial lateral overgrowth and metal-organic vapour phase epitaxy", Photonic Ireland, Dublin, Ireland (2011).

3. **C.S. Wong**, N.S. Bennett, B.Galiana, P.Tejedor, M. Benedicto, J.M. Molina-Aldareguia, S. Monaghan, P.K. Hurley, K. Cherkaoui, and P.J. McNally, "Investigation of anti-phase boundaries in MOVPE-grown GaAs on Ge using photoluminescence and micro-Raman mapping", Intel European Research and Innovation Conference, Dublin, Ireland (2011).

4. **C.S. Wong**, N.S. Bennett, P.J. McNally, B.Galiana, P.Tejedor, M. Benedicto, J.M. Molina-Aldareguia, S. Monaghan, P.K. Hurley, K. Cherkaoui, "Multi-technique characterisation of MOVPE-grown GaAs on Si", European Materials Research Society Spring Meeting, Nice, France (2010).

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