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Investigation of the Application of UPFC Controllers for Weak Bus Systems Subjected to Fault Conditions

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PhD

2012

INVESTIGATION OF THE APPLICATION OF UPFC
CONTROLLERS FOR WEAK BUS SYSTEMS SUBJECTED
TO FAULT CONDITIONS

An investigation of the behaviour of a UPFC controller: the voltage stability and power transfer capability of the network and the effect of the position of unsymmetrical fault conditions.

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Submitted for the degree of
Doctor of Philosophy

School of Engineering, Design and Technology
University of Bradford

2012

INVESTIGATION OF THE APPLICATION OF UPFC CONTROLLER FOR A WEAK BUS SYSTEM SUBJECTED TO FAULT CONDITIONS

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Mohamed Jalboub

Abstract

In order to identify the weakest bus in a power system so that the Unified Power Flow Controller could be connected, an investigation of static and dynamic voltage stability is presented. Two stability indices, static and dynamic, have been proposed in the thesis. Multi-Input Multi-Output (MIMO) analysis has been used for the dynamic stability analysis. Results based on the Western System Coordinate Council (WSCC) 3-machine, 9-bus test system and IEEE 14 bus Reliability Test System (RTS) shows that these indices detect with the degree of accuracy the weakest bus, the weakest line and the voltage stability margin in the test system before suffering from voltage collapse.

Recently, Flexible Alternating Current Transmission systems (FACTs) have become significant due to the need to strengthen existing power systems. The UPFC has been identified in literature as the most comprehensive and complex FACTs equipment that has emerged for the control and optimization of power flow in AC transmission systems. Significant research has been done on the UPFC. However, the extent of UPFC capability, connected to the weakest bus in maintaining the power flows under fault conditions, not only in the line where it is installed, but also in adjacent parallel lines, remains to be studied. In the literature, it has normally been assumed the UPFC is disconnected during a fault period. In this investigation it has been shown that fault conditions can affect the UPFC significantly, even if it occurred on far buses of the power system. This forms the main contribution presented in this thesis. The impact of UPFC in minimizing the disturbances in voltages, currents and power flows under fault conditions are investigated. The WSCC 3-machine, 9-bus test system is used to investigate the effect of an unsymmetrical fault type and position on the operation of UPFC controller in accordance to the G59 protection, stability and regulation. Results show that it is necessary to disconnect the UPFC controller from the power system during unsymmetrical fault conditions.

Keywords

Voltage Source Converters (VSC), STATic synchronous COMPensator (STATCOM), Static Series Synchronous Compensator (SSSC), Unified Power Flow Controller (UPFC), controller, Multi-Input-Multi-Output, (MIMO), Fast Voltage Stability Index (FVSI), Singular Value Decomposition (SVD), Western System Coordinate Council (WSCC)

Acknowledgements

All praise to the gracious, the greatest **Almighty Allah** who blessed me with the courage and made my efforts fruitful for the completion of this research to a happy ending. Without Allah's assistance, a project like this would never have come to fruition.

It would not have been possible to write this doctoral thesis without the help and support of the kind people around me, to only some of whom it is possible to give particular mention here.

Above all, to the spirit of my parents for their love, support and prayer. I ask Allah to forgive their sins and bring them into paradise. I would like to thank my wife Zineb, my sons (Ahmed and Ali) and my daughters (Inas, Ikram and Arige) for their infinite patience, support and love. They helped me to regain enthusiasm, strength and determination during the difficult times. Thanks for being there for me and believing in me, always. My deepest and sincere gratitude to my brothers and sisters for their unconditional support and encouragement.

This thesis would not have been possible without the help, support and patience of my principal supervisor, Dr. H. S. Rajamani. He has greatly helped me by providing his insight, knowledge, and perspective when required while giving me the space and time to grow on my own. His wide knowledge, his logical way of thinking, and his attitude towards science have been of great value to me over the years.

The good advice, support and friendship of Prof. R. Abd-Alhameed, has been invaluable on both an academic and a personal level, for which I am extremely grateful. My thanks are extended to Dr. D. Liang for his suggestion and advice. My special thanks are expressed to Dr. J. Readle for his help and support.

I also got a nice working environment at the School of Engineering Design and Technology, Bradford University. Thanks to my colleagues there. Special thanks to A. Ihbal, H. Hraga and I. Elfergane.

I gratefully acknowledge my sponsor, the Libyan government, who have given me an opportunity to study abroad by granting me a scholarship. I owe them and promise that we will develop our lovely country together.

Last but not least, I would like to express my ultimate gratitude to all my friends and relatives in Libya for their outstanding support and I would like to express my apologies to those whom I may have inadvertently failed to mention.

I praise and glorify the name of Allah, the Almighty, the Creator who creates all these nice people and these pleasant opportunities.

Table of contents

Abstract	i
Acknowledgements	ii
Table of contents	iii
List of Tables.....	vii
List of Figures	viii
Acronyms	xii
1: INTRODUCTION	1
1.1 Background	1
1.2 Research aims and objectives.....	3
1.3 Thesis organization	4
1.4 References	6
2: LITERATURE REVIEW	9
2.1 Introduction	9
2.1.1 Review of Static Stability Methods	10
2.1.1.1 Jacobian Method	10
2.1.1.2 Voltage Sensitivity Method	11
2.1.1.3 Reduced Jacobian Method	11
2.1.1.4 Power Loss Sensitivity Method	11
2.1.1.5 Energy Function Method	12
2.1.1.6 Singular Value Decomposition Method.....	12
2.1.1.7 Continuations Method.....	12
2.1.2 Review of Dynamic Voltage Stability Methods	13
2.1.2.1 Bifurcation theory	14
2.1.3 Review of Voltage Stability Indicator Methods.....	18
2.1.3.1 P-V and Q-V curves.....	19
2.1.3.2 L index	19
2.1.3.3 V/V_0 index.....	20
2.1.3.4 Line Stability index L_{mn}	20
2.1.3.5 Line Stability index FVSI	21
2.1.3.6 Line Stability index LQP	22
2.1.3.7 Voltage Collapse Point Index VCPI	22
2.1.3.8 On Line Voltage stability Index (L_{VSI}).....	23
2.1.3.9 Analysis of above Indices	23

2.1.3 Review of Flexible AC Transmission Systems.....	25
2.2 Summary	32
2.3 References	33
3: WEAK BUS IDENTIFICATION BASED ON STATIC VOLTAGE STABILITY	47
3.1 Introduction	47
3.1.1 Definition and classification of power system stability	47
3.1.1.1 Definition of voltage stability, voltage instability and voltage collapse	47
3.1.1.2 Classification of power system stability	48
3.1.2 Power Flow Problem.....	50
3.1.3 Modal analysis for voltage stability evaluation	53
3.1.3.1 Reduced Jacobian matrix	54
3.1.3.2 Modes of voltage stability.....	55
3.1.3.3 Identification of the weakest buses	58
3.2 Static voltage stability analysis	59
3.2.1 P-V and P-Q Curves as static voltage stability indicator	61
3.2.2 Proposed Index Formulation.....	67
3.2.3 Test system description	68
3.2.4 Experiments.....	69
3.2.5 Simulation Results and discussion	69
3.2.6 Weak bus identification based on modal analysis.....	71
3.3 Summary	75
3.4 References	76
4: WEAK BUS IDENTIFICATION BASED ON DYNAMIC VOLTAGE STABILITY	79
4.1 Introduction.....	79
4.2 Mathematical model for dynamic voltage stability analysis.....	80
4.3 Singular value analysis.....	81
4.4 Voltage stability analysis based on a multi-variable control technique.....	84
4.5 Effect of Load Modelling.....	88
4.5.1 Voltage Dependent Load.....	89
4.6 Test system description	91
4.6.1 Weak bus identification based on singular value technique	91
4.6.1.1 Exciter Mode.....	91
4.6.1.2 Inter-area Mode.....	93

4.6.2 Analysis considering the effect of load characteristics	95
4.6.2.1 Exciter mode	96
4.6.2.2 Inter-area mode	97
4.7 Summary	103
4.8 References	104
5: UNIFIED POWER FLOW CONTROLLER.....	106
5.1 Introduction	106
5.2 Flexible AC Transmission Systems	106
5.2.1 Series controllers	107
5.2.2 Shunt Controllers	108
5.2.3 Combined Series-Series Controllers	109
5.2.4 Combined Series-Shunt Controllers.....	109
5.2.5 Control system of the UPFC connected to transmission system	111
5.2.6 UPFC power flow equations	112
5.3 UPFC Performance	116
5.4 Test System Description	116
5.5 UPFC connected to the weakest bus of the WSCC test system.....	126
5.5.1 Test system description	126
5.5.2 Simulation results and discussions.....	130
5.6 Summary	133
5.7 References	134
6: THE EFFECT OF FAULT TYPE AND LOCATION ON THE UPFC OPERATION	137
6.1 Aim of the chapter.....	137
6.2 Brief review of faults in power systems.....	138
6.3 Single Line-to-Ground faults	142
6.3.1 Simulations.....	145
6.3.1.1 Simulation A	146
6.3.1.2 Simulation B	156
6.3.1.3 Simulation C	164
6.4 Double Line-to-Ground and Line-to-Line faults	171
6.4.1 D-L-G fault.....	171
6.4.2 L-L Faults.....	173
6.5 Summary	176
6.6 References	177

7: CONCLUSIONS AND RECOMMENDATIONS	181
7.1 Conclusion	181
7.2 Contribution to knowledge.....	184
7.3 Recommendation for future work	184
7.4 References	186
APPENDIX A	187
APPENDIX B	188

List of Tables

Table 3.1 Classification of power system stability	49
Table 3.1 WSCC 3-Machines 9-Bus system eigenvalues	72
Table 3.2 Voltage and reactive power margins for the WSCC 3-Machines 9-Bus system from Q-V curves	74
Table 4.1 Voltage and reactive power stability margins for the test system for bus 5.	102
Table 4.2 Voltage and reactive power stability margins for the test system for bus 8.	102
Table 6.1 Summarises fault voltages at bus B8 during an S-L-G fault at different distances	167

List of Figures

Figure 2.1 Types of bifurcation (a) saddle node; (b) Hopf; (c) singularity induced.....	17
Figure 2.2 Single line diagram of two bus system.....	21
Figure 3.1 The general character of P-V curves	60
Figure 3.2 The general character of Q-V curves.....	61
Figure 3.3 Single line diagram of two bus system.....	61
Figure 3.4 Single line diagrams for the IEEE 14 bus test system.....	64
Figure 3.5 Maximum loading points for active and reactive loads at Bus 14.....	64
Figure 3.6 Maximum loading points for active load at Bus 14.....	65
Figure 3.7 Maximum loading points for reactive load at Bus 14.....	66
Figure 3.8 WSCC 3-machines, 9-bus test system.....	69
Figure 3.9 LSZvs reactive power loading at buses (5, 6, 8) of WSCC test system	70
Figure 3.10 Voltage profiles of all buses of the WSCC test system	72
Figure 3.11 The participating factor of all buses for most critical mode for the test system.....	73
Figure 3.12 The Q-V curves at buses 5, 6 and 8 for the test system.....	74
Figure 4.1 A multi-variable technique: a system with r inputs and m outputs	85
Figure 4.2 Multi-Input Multi-Output (MIMO) for small signal stability modeling	86
Figure 4.3 Plot of maximal singular value vs frequency	92
Figure 4.4 Plot mode of magnitude of the output singular vector vs bus number	93
Figure 4.5 Plot of input singular vector associated with exciter mode 1	93
Figure 4.6 Plot of magnitude of the output singular vector vs bus number	94
Figure 4.7 Plot of magnitude input singular vector vs input number.....	95
Figure 4.8 Plot mode of magnitude of the output singular vector vs bus number at different load characteristics	96

Figure 4.9 Plot of input singular vector associated with exciter mode 1 at different load characteristics	97
Figure 4.10 Plot of magnitude of the output singular vector vs bus number with different load characteristics	98
Figure 4.11 Plot of magnitude input singular vector vs input number with different load characteristics	99
Figure 4.12 Voltage profiles of all buses of the test system at different load models ..	100
Figure 4.13 The Q-V curves at bus 5 for the test system at different load models	101
Figure 4.14 The Q-V curves at bus 8 for the test system at different load models	101
Figure 5.1: Static series FACTS controller	108
Figure 5.2 Shunt FACTS controller	108
Figure 5.3: Combined series-series FACTS controller	109
Figure 5.4 Combined series-shunt FACTS controller	110
Figure 5.5 Main circuit configuration of the Unified Power Flow Controller (UPFC)	111
Figure 5.6 Unified power flow controller equivalent circuit	112
Figure 5.7 Single line daigram for proposed test system	117
Figure 5.8 MATLAB implementation of the test system	118
Figure 5.9 Step change in the AC voltage reference from 0.95 to 1.05 and from 1.0455 to 0.95 p.u. applied at 2 ms and 4.5 and lasting 250 ms	121
Figure 5.10 Response to a step change in the active and reactive power reference	123
Figure 5.11 Performance of the UPFC controller	125
Figure 5.12 WSCC 3-machines, 9-bus test system	127
Figure 5.13 The steady state power flow of WSCC test system (UPFC out of service)	129
Figure 5.14 Bus voltages when UPFC out of service	130

Figure 5.15 The performance of the UPFC in voltage stability and power flow control	131
Figure 5.16 Test system with and without UPFC	132
Figure 5.17 Bus voltage of the test system with and without UPFC.	133
Figure 6.1 Types of Faults on a Three Phase System.	139
Figure 6.2 the single-line diagram illustrating the fault mechanism.....	140
Figure 6.3 MATLAB model for the single line diagram illustrating the fault mechanism	141
Figure 6.4 Voltage and current waveform as a result of Single L-G fault is applied at line 1 of the test system.....	142
Figure 6.5 WSCC 3-machines, 9-bus test system	143
Figure 6.6 The steady state power flow of the WSCC 3-machine, 9-bus test system ..	144
Figure 6.7 Comparing the currents and voltages of WSCC test system at B7 and B9 with UPFC and without UPFC (a) Fault current, (b) Fault Voltage	148
Figure 6.8 Basic block of PI controller	150
Figure 6.9 Possible control configurations for the UPFC shunt converter employing fundamental frequency switching	151
Figure 6.10 Effect of controller gain on the fault current waveform	152
Figure 6.11 Effect of capacitor size on the DC voltage during fault	153
Figure 6.12 Effect of capacitor size on the voltage at B8 as a result of S-L-G fault applied at B7	154
Figure 6.13 Effect of capacitor size on the overshoot and settling time at B8 as a result of S-L-G fault applied at B7	155
Figure 6.14 Effect of S-L-G fault at bus B7 on the bus voltages of each bus in the test system.....	157

Figure 6.15 Effect of S-L-G fault at bus B7 on the fault current of other buses in the WSCC test system.....	158
Figure 6.16 Effect of S-L-G fault at bus B7 on the active power of all buses in the test system.....	159
Figure 6.17 Effect of S-L-G fault at bus B7 on the reactive power of other buses in the test system	160
Figure 6.18 The effect of UPFC in damping power system oscillations	162
Figure 6.19 UPFC converter voltage magnitudes during fault at different distances ...	165
Figure 6.20 UPFC direct current component as a result of an S-L-G fault applied at each bus of the test system	166
Figure 6.21 Fault voltages at bus B8 an S-L-G fault applied at different locations of test system.....	167
Figure 6.22 UPFC converter phase angle during fault conditions	169
Figure 6.23 Tripping and reconnecting the UPFC during fault period	170
Figure 6.24 Effect of D-L-G fault at bus B7 on the bus voltages of each bus in the test system.....	172
Figure 6.25 Effect of D-L-G fault at bus B7 on the fault current of other buses in the test system.....	173
Figure 6.26 Effect of L-L fault at bus B7 on the bus voltages of each bus in the test system.....	174
Figure 6.27 Effect of L-L fault at bus B7 on the fault current of other buses in the test system.....	175

Acronyms

AC	Alternating Current
ASD	Automatic Speed Drives
ASVD	Advanced Static Var Compensators
ATP	Alternative Transient Program
AVR	Automatic Voltage Regulator
AUTO	Automatic
CPU	Central Processing Unit
DAE	Differential Algebraic Equations
DC	Direct Current
DLG	Double Line-to-Ground
EAC	Equal Area Criterion
ED	Eigenvalue Decomposition
EHV	Extra High Voltage
EMPT	Electro-Magnetic Transient Program
ETMPS	ExTended Mid-term Simulation Program
EUROSTAGE	EURO STAlite GEneralise`e
FACTS	Flexible Alternating Current Transmission Systems
FVSI	Fast Voltage Stability Index
GTO	Gate Turn Off
HB	Hopf Bifurcation
HVDC	High Voltage Direct Current
IEEE	Institute of Electrical and Electronic Engineers
IGBT	Insulated gate Bipolar Transistors
IGCT	Integrated Gate Commutated Thyristors
IPFC	Interline Power Flow Controller
JM	Jacobian Matrix

LL	Line-to-Line
LOTDYS	Long Term Dynamic Stability
LVSI	Line Voltage Stability Indicator
MIMO	Multi-Input Multi-Output
MOS	Metal Oxide Semiconductor
MVA	Mega Volta Amber
NN	Neural Network
NPC	Neutral Point Clamping
OLTC	On-Load Tap Changer
PEBS	Potential Energy Boundary Surface
PI	Proportional Integral
PLC	Programmable Logic Design
PLL	Phase Locked Loop
PSS	Power System Stabilizer
PWM	Pulse width Modulation
QSS	Quasi Steady State
RGA	Relative Gain Array
RTS	Reliability Test System
SEP	Stable Equilibrium Point
S _i C	Silicon Carbide
SIB	Singular Induced Bifurcation
SLG	Single-Line-to-Ground
SNB	Saddle Node Bifurcation
SPFC	Series Power Flow Controller
SSR	Sub-Synchronous Resonance
SSSC	Static Synchronous Series Compensators
STATCOM	STATic synchronous COMpensators
STATCON	STATic CONDenser

SVC	Static Var Compensators
SVD	Singular Value Decomposition
TCR	Thyristor Controlled Reactor
TCPAR	Thyristor Controlled Phase Angle Regulator
TCSC	Thyristor Controlled Series Capacitor
THD	Total Harmonic Distortion
TSC	Thyristor Switched Capacitor
UEP	Unstable Equilibrium Point
UPFC	Unified Power Flow Controller
UPS	Uninterruptible Power Supply
UWPFLOW	University of Waterloo Power FLOW
VC	Voltage Collapse
VCPI	Voltage Collapse Point Indicator
VSC	Voltage Source Converter
VSM	Voltage Stability Margin
WSCC	Western System Coordinate Council
ZOH	Zero Order Hold

1: INTRODUCTION

1.1 Background

Environmental constraints limit the expansion of transmission networks and generation near load centres. This has a negative influence on power system voltage stability. Simultaneous growth in the use of electrical power without a corresponding increase of transmission capacity has brought many power systems closer to their voltage stability limit.

Voltage stability is concerned with the ability of a power system to maintain acceptable voltages at all buses under normal conditions and after being subjected to a disturbance [1]. The assessment of voltage stability has become more complicated due to the complexity of power systems. For example, voltages do not indicate the proximity to voltage collapse points in heavily compensated systems even in heavy loading conditions.

The main cause of voltage collapse affecting the power system is faults on the power system, often resulting from weather conditions, e.g. lightning, wind, and ice hitting overhead lines [2, 3]. On underground cables, typically used in urban areas, insulation problems and the operation of excavators are the main causes of voltage interruptions [4].

Voltage collapse has become a major power system voltage stability problem causing significant large financial losses for industries [5-7]. Although the duration of a voltage collapse from a remote fault is only a few cycles and the voltage can totally be recovered a few cycles afterwards, process equipment often cannot keep normal operation during these collapses and may trip or shut down.

Voltage collapses are very dependent upon the maximum load [8-11] that can be supported at a particular load bus. Any attempt to increase the load beyond this point could force the entire system into instability, leading to voltage collapse. This would indicate that the power system physically could not supply the amount of the connected load as stated [9, 12].

At high voltage networks (transmission system), the task of controlling the power flow of an AC transmission system through a pre-determined corridor is not simple. As the power (electricity) flows along each path are determined by the lines and voltage characteristics involved in the network. Loop flows may take power far from the most direct route from a generator to a load centre [8].

Transmission systems in the past were over-dimensioned with large stability margins. Therefore, dynamic compensators, such as synchronous condensers, were seldom required. Over the last 10-20 years, this situation has changed as the construction of new generation facilities and new transmission lines has become difficult due to financial and environmental constraints [13]. Therefore, better utilization of existing power systems has become essential [8]. The interconnection of separate power systems allows better utilization of power generation capability, but the interconnected system must also be able to recover from faults and supply the necessary power at load changes.

Recently there have been significant breakthroughs in power semiconductor technology. The voltage and current ratings of commercially available power semiconductor devices have continuously been increased, improving the performance and reducing the necessity of series and parallel connections for achieving the desired rating, making their applications more compact with decreasing costs [14, 15]. Until the beginning of the nineties, the only semiconductor device applied to high power applications was the

thyristor, employed in High Voltage Direct Current (HVDC) transmission systems and Static Var Compensators (SVC) [16, 17]. Recent advances in high power semiconductor devices such as Gate Turn-Off (GTO) thyristor and Insulated Gate Bipolar Transistors (IGBT) have led to the design of fast controllable reactive power source utilization and converter technology, such as the Flexible AC Transmission System (FACTS) and HVDC [18, 19]. The Unified Power Flow Controller (UPFC) is the most versatile and complex of the FACTS devices that can provide the control of the transmission line impedance, phase angle, power transfer and voltage control [20]. This versatility of the UPFC makes it a prime FACTS device that can provide many of the control functions required to solve a wide range of dynamic and steady state problems encountered in power systems [21, 22]. However, these controllers are very expensive and, hence, their optimal location in the network must be properly ascertained.

1.2 Research aims and objectives

The aim of this thesis is:

- Modelling the elements that are used to build the UPFC in the MATLAB (Simulink) environment in order to investigate the effect of unsymmetrical fault types and positions on the operation of the UPFC in accordance to G59 protection, stability and reliability regulations as vital information regarding the ratings of devices and protection.

The objectives of this thesis are as follows:

- To investigate measures used to identify the weakest bus and the weakest line in a power system, which is prone to voltage collapse based on static and dynamic voltage stability criteria. In addition, to determine the reactive power (MVar) margins that could be added to the weakest bus before suffering from voltage collapse

- Whilst much literature exists on fault conditions, it is not clear in the literature what happens if a UPFC is included in a weak grid. It may have been assumed that faults near the UPFC would naturally damage the UPFC and hence the lack of published materials. However, it is essential to investigate the effect of unsymmetrical (Single Line-to-Ground, Double line-to-Ground and Line-to-Line) faults type and position on the operation of UPFC connected grid system, (in accordance to G59 protection, stability and reliability regulations as vital information regarding the ratings of devices and protection). The system will require an understanding of the voltage, current and power deviation during the fault condition.

1.3 Thesis organization

In chapter 2, a literature review is presented, discussing the voltage stability and voltage collapse problem in an electric power system. A review of voltage stability analysis methods based on static and dynamic criteria is presented and discussed together with line stability indices. The detailed history of the application of power electronics devices to High Voltage Direct current (HVDC) and Static Var Compensators (SVC) is also included.

Chapter 3 emphasizes some topics related to static voltage stability analysis as well as the identification of the weak bus in the power system. A new static voltage stability index called *LSZ* is proposed based on the transmission line impedance and the apparent power at the receiver. To investigate the effectiveness of the proposed index, the IEEE 14 bus reliability test system and WSCC 3-machine, 9-bus test system models are used. The modal analysis method is applied to the load flow of the reduced Jacobian matrix in order to generate the eigenvalues of the test system, and then the participation factors

are generated to identify the critical nodes to predict the critical buses. The results are presented and compared with other static voltage stability indices

In chapter 4, the singular value decomposition technique is applied to the multi-input multi-output (MIMO) transfer function of the test system in order to carry out the dynamic voltage stability analysis. The MIMO system is defined by taking into account the critical nodal voltages as outputs and possible control variables as the input. Simulations are carried out to validate the proposed technique using the WSCC 3-machine, 9-bus test system. The effect of a non-linear load model on the critical modes of the singular value decomposition is also investigated and the results are presented and discussed.

Chapter 5 focuses on the UPFC controller topologies based on semiconductor switches with turn-off capability. Two MATLAB (Simulink) test system models are studied. The first test is the modified IEEE-4 buses test system, which is used to investigate the different functions of the SSSC, STATCOM and UPFC. The second is the WSCC test system, used to investigate the operation of the UPFC when connected to the weakest bus. The simulation results are presented and discussed

Chapter 6 demonstrates the effects of the unsymmetrical fault type and positions on the operation of the UPFC. Simulations are conducted in a MATLAB (Simulink) environment for unsymmetrical faults: single line-to-ground, double line-to-ground and line-to-line applied to WSCC 3-machine, 9-bus test system with UPFC connected to the weakest bus. The results are presented and discussed.

Finally, the conclusions of the thesis are pointed out in Chapter 7 as well as suggestions for future work.

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2: LITERATURE REVIEW

2.1 Introduction

To meet an ever-increasing electrical load demand, modern power systems are undergoing numerous changes and becoming more complex from operation, control and stability maintenance standpoints. The major problem that is associated with such a stressed system is voltage instability or collapse. A system is said to enter a state of voltage instability when a disturbance causes a progressive and uncontrollable decline in voltage, which can occur because of the inability of the network to meet the increased demand for reactive power. Therefore, voltage stability analysis is essential in order to identify the critical buses in a power system, i.e. buses which are close to their voltage stability limits, and thus enable certain measures to be taken by the operators in order to avoid any incidence of voltage collapse. At its earlier developmental stage, voltage stability used to be analysed by static analysis methods, such as power flows. However, as understanding of voltage stability developed, it expanded to dynamic stability and dynamic analysis could be applied.

In this chapter, a review of static and dynamic voltage stability methods as well as static and dynamic voltage stability indicators are presented. Next, a review of power electronic based devices that are used to enhance the power system performance in terms of voltage stability are stated. Finally, the different types of faults that affect the operation of power system are discussed.

2.1.1 Review of Static Stability Methods

Voltage instability reveals different phenomena as we change the observing point such as low voltage profiles, heavy reactive power flows, inadequate reactive support, and heavily loaded systems. This has led to the introduction of a number of analysis methods according to their specific observing point. The Jacobian method [1, 2], reduced Jacobian method [3, 4], voltage sensitivity method [5, 6], real and reactive power loss sensitivity method [7, 8] energy function method [9, 10], singular value decomposition method [11, 12] and continuation method [13, 14] are the main methods used in static voltage stability analysis. Each method has been developed on the basis of acute observations of a particular phenomenon of voltage collapse, yielding its own voltage collapse conditions.

2.1.1.1 Jacobian Method

Voltage instability is due to the structural instability of the system caused by a change in a system parameter, such as a power demand or faulted system. The steady state changes continuously as the system parameter changes until it disappears at a saddle node bifurcation point (discussed later in section 2.1.2.1). A saddle-node bifurcation point of the power flow equations of a power system can provide information regarding the margin of static voltage stability at the current operating point of the power system. The information gained is used in voltage stability control. Several methods have been developed for computing saddle node bifurcation points of power flow equations [15-17]. The Jacobian method exploits the condition of saddle node bifurcation by examining power flow solutions with changes in bus injection powers.

2.1.1.2 Voltage Sensitivity Method

The voltage sensitivity method [5, 6] is the most direct approach using the voltage sensitivity to system parameters. Voltage dip sensitivities are derived for the following parameter changes: generation levels, real and reactive elements, loads, and generator terminal voltages. It is assumed that the magnitude of the changes are small and do not modify the set of advanced machines, i.e., the mode of disturbance is not altered. It is also assumed that the slack generator will compensate any required change in generation level of the system due to any network parameter variation. The amount of change in the slack generator is determined by the power flow equations.

2.1.1.3 Reduced Jacobian Method

It is practically known that when the real power P changes, both the voltage magnitude V and angle θ will change. However, the voltage angle will change much more than the voltage magnitude. When the reactive power Q changes both voltage magnitude V and angle θ also change. However, the voltage magnitude will change much more than the voltage angle. By utilizing this coupling between Q and V and P and θ the shortage of the reactive power Q mainly causes the voltage instability in the power system [18]. Also, by performing modal analysis technique to the reduced ($V-Q$) Jacobian matrix, the bus, branch and generator participation factors can be used as an indicator to voltage stability. Moreover, the stability margin and the shortest distance to instability can also be determined.

2.1.1.4 Power Loss Sensitivity Method

The voltage collapse phenomenon is accompanied with the rapid increase in line flows. The power flow Jacobian matrix, J , gives the sensitivity between power flow and bus

voltage changes. Both P and Q are affecting the system voltage stability. However, at each operating point, P can be kept constant and the voltage stability analysis will consider the incremental relation between Q and V. Based on this consideration the sensitivity equation can be written [3].

2.1.1.5 Energy Function Method

The energy function method [19] is used to determine the system stability by comparing the energy difference between Unstable Equilibrium Points (UEPs) and a Stable Equilibrium Point (SEP). If the voltage of SEP and the voltage of UEP coincide, the energy difference between them will be zero and bring about voltage collapse. The saddle node bifurcation phenomenon (discussed later in section 2.1.2.1.3) occurs when UEP coincides with SEP, which also makes the energy difference zero. Consequently, the energy function method provides the same voltage collapse condition as the saddle node bifurcation method.

2.1.1.6 Singular Value Decomposition (SVD) Method

Singular Value Decomposition (SVD) is a very useful tool for analysing matrices and related problems in many fields. It has been applied to power systems for voltage stability analysis to obtain a decomposition of the Jacobian matrix [18]. The smallest singular value is an indicator of the proximity to the steady state stability limit and the right singular vector indicates sensitive voltage.

2.1.1.7 Continuations Method

Continuation methods overcome the singular problem by reformulating the differential algebraic equations, so that they will remain well-conditioned at all possible loading conditions. Continuation techniques are generally composed of two or three

steps. The first step is a predictor step, the second is a corrector step, and the last step is a parameterization routine. From a known operating point and the change of parameters, a prediction step is made, and from the new point, a corrector routine is used to calculate the new equilibrium point. A parameterization is used to ensure that the Jacobian matrix used in the continuation method does not become singular at saddle node bifurcations. The University of Waterloo Power FLOW program (UWPFLOW), uses a continuation method to detect the voltage stability limit of a power system [20]. Another public program AUTO [21] is also mentioned in the literature. AUTO applies a continuation method to solve the differential algebraic equations of the system. AUTO has been used for theoretical studies of bifurcations in small power systems [22, 23].

2.1.2 Review of Dynamic Voltage Stability Methods

Dynamic analysis (also referred to as time-domain analysis) is commonly employed in the study of power system voltage stability to reveal the system trajectory after a disturbance. A power system is a typical large dynamic system and its dynamic behaviour has great influence on the voltage stability. The latest blackouts have shown that voltage stability is very closely associated with issues of frequency and angle stability [24, 25]. Most of the power system blackouts occurring all over the world in the past 30 years have been mainly voltage collapse. Therefore, in order to get more realistic results it is necessary to take the full dynamic system model into account. Some literature has been presented on the dynamic voltage stability analysis [3, 26, 27]. The dynamic analysis implies the use of a model characterized by nonlinear differential and algebraic equations which include generators dynamics, induction motor loads, tap changing transformers, etc. [3]. Dynamic simulations and bifurcation theory [28, 29] are the mostly used method in analysis of dynamic voltage stability. Dynamic simulators

are based on time domain simulation for the linearised system dynamic model while bifurcation based on eigenvalue computation for the linearised system dynamic model. Dynamic analysis uses time-domain simulations to solve nonlinear system differential algebraic equations.

Dynamic analysis provides the most accurate replication of the time responses of the power system. Accurate determination of the time sequence of the different events leading to system voltage instability is essential for post-mortem analysis and the co-ordination of protection and control. However, time-domain simulations are time consuming in terms of Central Processing Unit (CPU) and the engineering required for analysis of results. Also, dynamic analysis does not readily provide information regarding the sensitivity or degree of instability. These limitations generally make dynamic analysis impractical for examination of a wide range of system conditions or for determining stability limits.

2.1.2.1 Bifurcation theory

The methods of bifurcation theory can be effectively used to analyse various types of stability problems in power systems, such as voltage stability, voltage collapse and oscillatory phenomena [30-37]. Therefore, bifurcation analysis has become an important tool in the practical analysis of power system stability [38-42].

Power system model for dynamic analysis

The power system is modelled with algebraic and differential equations. The differential Equations 2.1 is the state space representation of a power system. Equation 2.1a represent the dynamics of generators (stator transients neglected), control systems and loads, while the algebraic Equations 2.1b describe current or power node balances.

$$\dot{x} = f(x, y, \zeta) \quad (2.1a)$$

$$0 = g(x, y, \zeta) \quad (2.1b)$$

where x is the dynamic state vector, y is the vector of the algebraic variables (complex node voltages) and ζ is a scalar parameter defined as in the static methods.

For a given ζ_0 , an equilibrium point (x_0, y_0, ζ_0) is a constant solution of Equations 2.1 and thus can be obtained by solving Equations 2.1 with their time derivatives set at zero:

$$0 = f(x_0, y_0, \zeta_0) \quad (2.2a)$$

$$0 = g(x_0, y_0, \zeta_0) \quad (2.2b)$$

Eigenvalues of the linearised dynamic system model

The small-disturbance stability analysis at each equilibrium point (x_0, y_0, ζ_0) of the dynamic system described by Equation 2.1 requires the linearization of the system equations. With $\Delta x = (x - x_0)$ and $\Delta y = (y - y_0)$, the linearised system becomes:

$$\Delta \dot{x} = J_{fx} \Delta x + J_{fy} \Delta y \quad (2.3a)$$

$$0 = J_{gx} \Delta x + J_{gy} \Delta y \quad (2.3b)$$

where J_{fx} , J_{fy} , J_{gx} , J_{gy} , are the Jacobian sub-matrices containing the partial derivatives of Equations 2.2 with respect to the state and algebraic variables. The dynamic Jacobian matrix J_{DYN} , calculated at the equilibrium point (x_0, y_0, ζ_0) , is defined as:

$$J_{dyn} = \begin{vmatrix} J_{fx} & J_{fy} \\ J_{gx} & J_{gy} \end{vmatrix} \quad (2.4)$$

The eigenvalues are the solutions of the characteristic equation:

$$\det \left(j_{dyn} - \lambda \begin{vmatrix} I & 0 \\ 0 & 0 \end{vmatrix} \right) = 0 \quad (2.5)$$

where I is the identity matrix. The equilibrium point (x_0, y_0, ζ_0) is stable for small disturbances if all the eigenvalues λ are in the left complex half-plane.

Bifurcation analysis

The evolution of the dynamic voltage stability of the dynamic system described by Equation 2.1, as the parameter ζ varies, may be interpreted within the framework of bifurcation theory [43]. From a practical viewpoint, bifurcations may be interpreted in two different ways as follows:

- Migration of the linearised system eigenvalues from one complex half-plane to the other, which can modify the stability of the linearised system and thus the small-disturbance stability of the non-linear system.
- Changes in the number of equilibrium points (i.e. solutions of Equations 2.2) or in the type (constant/periodic) of steady-state behaviour of Equation 2.1.

Starting from a stable equilibrium point and monotonically varying ζ , the system voltage stability may be changed in three different ways as shown in Figure 2.1, corresponding to different types of bifurcations and to different eigenvalue trajectories in the complex plane.

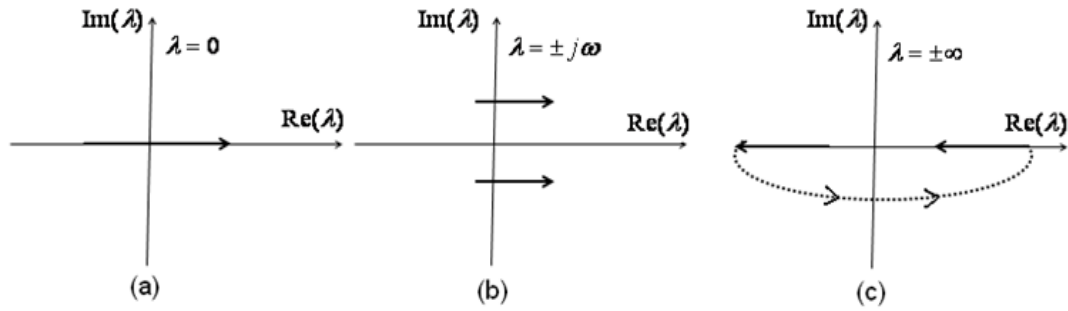


Figure 2.1 Types of bifurcation (a) saddle node; (b) Hopf; (c) singularity induced.

- **Saddle-node bifurcation (SNB)** (Figure 2.1a): a real eigenvalue crosses the origin along the real axis. The saddle node bifurcation corresponds to a null eigenvalue. The loss of voltage stability is of an aperiodic type, and the number of equilibrium points changes.
- **Hopf Bifurcation (HB)** (Figure 2.1b): two complex eigenvalues cross the imaginary axis. The Hopf bifurcation corresponds to a pair of purely imaginary eigenvalues. The loss of voltage stability is of an oscillatory type. Two cases are possible: in the supercritical case, the equilibrium point becomes unstable and a stable periodic solution (limit cycle) appears; in the subcritical case, the equilibrium point becomes unstable after coalescing with an unstable limit cycle.
- **Singularity Induced Bifurcation (SIB)** (Figure 2.1c): a real eigenvalue moves from the left to the right complex half-plane through the infinity point. This bifurcation corresponds to an infinite eigenvalue and to the impossibility of solving the algebraic Equations 2.1b for y , given x , that is, the Jacobian matrix $J_{g,x}$ is singular. The loss of stability is of an aperiodic type. A complete description of this bifurcation is given in [44]

The author in [45], uses bifurcation techniques to minimize oscillations of the state and network variables in order to achieve the objective of dynamic voltage stability. Then, a

parameter optimization technique is applied to limiting the magnitude of oscillations. In this case, the dynamic voltage stability is decoupled from the angle dynamics. The authors assume that all electromechanical oscillations are stable. By neglecting the power-angle dynamics, the voltage response of the unregulated power system can be approximated by the eigenvalues of the voltage stability matrix.

2.1.3 Review of Voltage Stability Indicator Methods

Different voltage instability indicators are used to quantify the proximity of a particular operating state to the point of voltage collapse. These indicators can classify different power system conditions. A more practical indicator is the distance between actual load and maximum load at the stability margin in the direction of an estimated or forecasted load increase [46, 47-49]. The calculation can be done using the continuation method [58, 50]. This method considers all non-linearities of the power system, but is very time consuming for sufficient accuracy [50]. The energy method has also been used for voltage security assessment [47, 51], but it is highly nonlinear and complex for numerical routines to solve. Attempts have been made to set up a direct mapping [47, 51] from operating states to Voltage Stability Margin (VSM) using supervised Neural Networks (NNs) [46]. NN based approaches for voltage stability determination are system dependent and a contingency or a preventive action can highly decrease the accuracy of these methods. Moreover, expert systems and fuzzy expert systems have been proposed for voltage security control [51, 52], but these methods are dependent on the experiences of operators and power system configuration. Determination of the start point of voltage instability is important to remedy this problem. Both operators and system planners require knowledge of the probable starting points of voltage instability. In [47, 51], sensitivity analysis has been proposed for the determination of the start point of voltage instability. The proposed sensitivity analysis not only requires large

amounts of data but also suffers from a lack of accuracy and in some cases obtained results do not match with the expectation of experienced operators.

The condition of voltage stability in a power system can be known using voltage stability indices. These indices can either reveal the critical bus of a power system or the stability of each line connected between two buses in an interconnected network or evaluate the voltage stability margins of a system. The indices used to examine the system stability are briefly described in the following sections.

2.1.3.1 P-V and Q-V curves

The P-V curves are the most used method of predicting voltage security. They are used to determine the loading margin of a power system. The power system load is gradually increased and, at each increment, it is necessary to re-compute power flows until the nose of the PV curve is reached. The margin between the voltage collapse point and the current operating point is used as the voltage stability criterion [53].

With Q-V curves it is possible, for the operators, to know the amount of maximum reactive power that can be achieved or added to the weakest bus before reaching a minimum voltage limit. The reactive power margin is the pu distance from the operating point to the bottom of the Q-V curve. The Q-V curve can be used as an index for voltage instability. The point where dQ/dV is zero indicates the voltage stability limit [3].

2.1.3.2 L index

Kessel *et al.* [54] developed a voltage stability index based on the solution of the power flow equations. The L index is a quantitative measure for the estimation of the distance

of the actual state of the system to the stability limit. The L index describes the stability of the complete system and is given by:

$$L = \max_{j \in \alpha_L} \{L_j\} = \max_{j \in \alpha_L} \left\{ \left| 1 - \frac{\sum_{i \in \alpha_G} F_{ji} * V_i}{V_j} \right| \right\} \quad (2.6)$$

$$F_{ji} = |F_{ji}| \angle \theta_{ji}$$

where V_i and V_j are the complex sending and receiving end voltages, α_L is the set of load buses, α_G is the set of generator buses and F_{ji} is the element of hybrid-F matrix. The [F] is computed using $[F] = [Y_{LL}]^{-1}[Y_{LG}]$, where $[Y_{LL}]$ and $[Y_{LG}]$ are sub-matrices of the Y-bus matrix. L index is a local indicator that determines the busbars from where collapse may originate. The L index varies in a range between 0 (no load) and 1 (voltage collapse).

2.1.3.3 V/V₀ index

Assuming the bus voltage values (V) to be known from load flow or state estimation studies, new bus voltages (V₀) are obtained solving a load flow for the system at an identical state but with all loads set to zero. The ratio V/V₀ at each node yields a voltage stability map of the system, allowing for immediate detection of weak and effective countermeasure spots [53].

2.1.3.4 Line Stability index L_{mn}

M. Moghavemmi *et al.* [55] derived a line stability index based on the power transmission concept in a single line. Figure 2.2 illustrates a single line of an interconnected network where the L_{mn} is derived from.

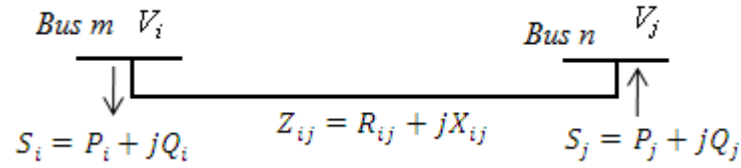


Figure 2.2 Single line diagram of two bus system

The line stability index, for this model, can be defined as:

$$L_{mn} = \frac{4XQ_n}{[V_i \sin(\theta - \delta)]^2} \quad (2.7)$$

where m and n are the sending and receiving end buses, X is the transmission line reactance, Q_n is the reactive power at the receiving end, θ is the line impedance angle and δ is the angle difference between the supply voltage and the receiving end voltage. Lines that presents values of L_{mn} close to 1, indicates that those lines are closer to their instability points. To maintain a secure condition, the L_{mn} index should be less than 1.

2.1.3.5 Line Stability index FVSI

The Fast Voltage Stability Index (FVSI) proposed by I. Musirin *et al.* [56] is also based on a concept of power flow through a single line. For a typical transmission line, the stability index is calculated by:

$$FVSI_{ij} = \frac{4Z^2 Q_j}{V_i^2 X} \quad (2.8)$$

where Z is the line impedance, X is the line reactance, Q_j is the reactive power flow at the receiving end and V_i is the sending end voltage. The line that gives an index value closest to 1 will be the most critical line of the bus and may lead to voltage collapse. The calculated FVSI can also be used to determine the weakest bus on the system. The determination of the weakest bus is based on the maximum load allowed on a load bus.

The most vulnerable bus in the system corresponds to the bus with the smallest maximum permissible load.

2.1.3.6 Line Stability index LQP

The LQP index derived by A. Mohamed *et al.* [57] is obtained using the same concept as [55] and [56], in which the discriminant of the power quadratic equation is set to be greater or equal than zero. The LQP is obtained as follows:

$$LQP = 4 \left(\frac{X}{V_i^2} \right) \left(\frac{X}{V_i^2} P_i^2 + Q_j \right) \quad (2.9)$$

where X is the line reactance, Q_j is the reactive power flow at the receiving bus, V_i is the voltage on sending bus and P_i is the active power flow at the sending bus. To maintain a secure condition, the value of LQP index should be maintained less than 1.

2.1.3.7 Voltage Collapse Point Index VCPI

The VCPI index proposed by M. Moghavammi *et al.* [58] investigates the stability of each line of the system and are based on the concept of maximum power transferred through a line.

$$VCPI(1) = \frac{P_R}{P_{R(max)}} \quad (2.10)$$

$$VCPI(2) = \frac{Q_R}{Q_{R(max)}} \quad (2.11)$$

The values of P_R and Q_R are obtained from conventional power flow calculations, and $P_{R(max)}$ and $Q_{R(max)}$ are the maximum active and reactive powers that can be transferred through a line. VCPI (1) and VCPI (2) are the active and reactive power ratio between

the real or reactive power respectively transferred to the receiving end and the maximum real or reactive power that can be transferred.

The two indicators, VCPI (1) and VCPI (2), are calculated for each line to represent the stressed conditions of the lines. The power system is stable if both indicators less than 1, when both of the two indicators are equal to 1, the point of voltage collapse is reached.

2.1.3.8 On Line Voltage stability Index (L_{VSI})

An on-line voltage stability index referred as L_{VSI} was proposed from the viewpoint of the relations between line active power and bus voltage with the line [59]. The index is formulated as:

$$L_{VSI} = \frac{4P_j * R}{\left(V_i \cos(\theta - \delta)\right)^2} \quad (2.12)$$

where P_j is the receiving end active power and R is the transmission line resistance. For the system to operate in stable operation L_{VSI} must be less than 1.

2.1.3.9 Analysis of above Indices

- I. In P-V and Q-V curves, the effects of changes in both active and reactive powers on voltage stability cannot be observed simultaneously. In addition, because of the heavy dependence of these methods to system conditions and type of simulation, the possibility of error is high in these methods.
- II. The main drawback of V/V_0 Index is that it presents a highly non-linear profile with respect to changes on the system parameters, not allowing for accurate predictions of proximity to voltage collapse [60].
- III. Line indices $FVSI$, L_{mn} , LQP and L_{VSI} are formulated either from the relationship between reactive power and voltage or from the relationship

between the active power and voltage. All these indices may fail under some special conditions. Examples of possible failure are:

- Special branch parameters: the transmission line resistance $r = 0$, thus the index L_{VSI} fails.
- L_{VSI} may mis-identify a heavy line as a bottleneck when $(\theta-\delta)$ approaches 90^0 . When $(\theta-\delta)$ approaches 90^0 , $\cos(\theta-\delta)$ approaches zero. As $\cos(\theta-\delta)$ is in the denominator, there may be a dramatic increase in L_{VSI} . It implies that a healthy line may be identified as a critical line.
- L_{VSI} is more sensitive to δ than L_{mn} because $\cos(\theta-\delta)$ changes much faster than $\sin(\theta-\delta)$ around 90^0 .
- $FVSI$ is derived assuming voltage angle difference is zero. It implies that simplified $FVSI$ is not suitable for heavy load lines due to large angle difference.
- LQP directly involves both of active power and reactive power in the calculation while $FVSI$ and L_{mn} directly involve only reactive power, the performance of the LQP index is slightly better than that of the others.

Based on the basic understanding of voltage collapse and voltage stability analysis, a new index of analysing static stability is proposed utilizing the power flow solution based on the transmission line impedance and the apparent power at the receiving end. The proposed line stability index has the capability to identify the weakest bus and the weakest line in the interconnected power. Also, a second index for the assessment of dynamic voltage stability is studied. The method is based on the advantages of modern multi-variable control theory. Based on the Multi-Input Multi-Output (MIMO) transfer function, interactions between properly defined input and output variables affecting dynamic voltage stability can be analysed at different frequencies. These variables

define the weakest mode in the system which corresponds to the weakest bus and the suitable control action that should be taken to compensate the weakest mode.

2.1.3 Review of Flexible AC Transmission Systems (FACTS)

The application of power electronics until the beginning of the nineties was greatly dominated by equipment connected to the low-voltage network. Exceptions to these applications were thyristors employed in High Voltage Direct Current (HVDC) transmission systems and Static Var Compensators (SVC). In most of the cases, the simplest and often least expensive solution of reinforcing a transmission or distribution network was to build a new line. However, this has become more difficult due to environmental issues and difficulties in obtaining concessions for new rights-of-way. In parallel with this constraint, the electricity market has progressively been deregulated worldwide with the purpose of stimulating competition between the power utilities. Moreover, the number of process industries requiring clean and undisturbed supply is increased. The whole scenario demands new solutions, not only advantageous from the technical point of view, but also cost-effective.

At the same time as these changes in transmission and distribution systems, power semiconductor technology has experienced very fast development in the last two decade. The voltage and current ratings of commercially available power devices have continuously increased, reducing the necessity of series and parallel connections for achieving the desired rating, making the design of power electronics converters more compact.

Development of Gate Turn-Off Thyristors (GTO) technology has led to a variety of applications in the power range of 1-20 MVA. However, GTOs still have some drawbacks, mostly related to the turn-off process, e.g. high switching losses (which

reduce the maximum allowable switching frequency) and the necessity of snubber circuits. The novel IGCT (Integrated Gate Commutated Thyristors) technology opens the possibility to combine the turn-off characteristics of the Insulated Gate Bipolar Transistors (IGBT) with the superior conduction properties of thyristors. It is expected that IGCTs will, in the near future, take the place occupied by GTOs. A new group of medium voltage AC drives based on IGCTs has been designed, resulting in compact drives with fewer semiconductor devices [61, 62].

It can thus be concluded, that the mature devices with turn-off capability that can be considered in high power applications (MVA range) are Insulated Gate Bipolar Transistors (IGBT) and the Gate Turn-Off Thyristors (GTO) [63].

From a longer time point of view, it is also expected that semiconductor devices based on new materials, e.g. Silicon Carbide (SiC) [63, 110], will make it possible to design semiconductors for higher voltages and lower losses. They will also allow the operation at considerably higher temperatures (around 400°C), thus alleviating cooling requirements.

Based on the above mentioned challenges for improving the system performance for distribution and transmission systems, associated to the development of the power semiconductor technology, the concepts of Flexible AC Transmission Systems (FACTS) devices can be a solution to these problems [64, 65]. They are able to provide rapid active and reactive power compensation to power systems, and therefore can be used to provide voltage support and power flow control, increase transient stability and improve power oscillation damping. Suitably located FACTS devices allow more efficient utilization of the existing transmission systems [66].

Among the FACTS families, fast shunt VAR compensators are needed to address voltage stability problems more effectively as has been pointed out in much literature [67-70]. Shunt FACTS devices such as the STATic synchronous COMPensator (STATCOM) [66, 71-73] have been widely used to provide smooth and reliable voltage control at points in the network. Series FACTS devices, such as Static Synchronous Series Compensators (SSSC) [74-77], can regulate the power flow of active and reactive power by injecting a controllable capacitive and inductive impedance compensation into a line at the point of connection. In addition, the SSSC has an excellent performance in damping low frequency power oscillations in power networks [78, 79].

Recently, the UPFC has been proposed as one of the most versatile FACTS devices that has been used for control and optimization of power flow in electric power transmission systems [80-83]. It is primarily used for independent control of real and reactive power in transmission lines for a flexible, reliable and economic operation and loading of power system. Until recently, all three parameters that affect real and reactive power flow on the line, i.e. the line impedance, voltage magnitudes at the terminals of the line or power angle, were controlled separately using either mechanical or other FACTS devices such as Static Var Compensator (SVC), Thyristor Controlled Series Capacitor (TCSC), phase shifter. However, the UPFC allows simultaneous or independent control of these parameters with transfer from one control scheme to another in real time. Also, the UPFC can be used for voltage support, transient stability improvement and damping of low frequency power system oscillations. Due to its attractive features, modelling and controlling UPFC has come under intensive investigation in the recent years.

Several references in technical literature can be found on development of UPFC steady state, dynamic and linearised models. Steady state models, referred to as an injection model are described in [84]. The UPFC is modelled as a series reactance together with

the dependent loads injected at each end of the series reactance. The model is simple and helpful in understanding the UPFC impact on the power system. However, the amplitude modulation and phase angle control signals of the series voltage source converter have to be adjusted manually in order to find the desired load flow solution.

If a UPFC is operated in the automatic control mode (i.e. to maintain a pre-specified power flow between two power system buses and to regulate the sending end voltage at the specific value), the UPFC sending end bus is transformed into a PV bus while the receiving end bus is transformed into a PQ bus, and conventional load flow (LF) program can be performed [85]. This method is simple and easy to implement but it will only work if real and reactive power flows and the sending bus voltage magnitude are controlled simultaneously. It should be also mentioned that there is no need for iterative procedure used in [85] to compute UPFC control parameters. This can be computed directly after the conventional load flow solution is obtained. Due to the advantages that the automatic power flow control mode offers, this mode will be used as the basic operation mode for most of the practical applications. A Newton-Raphson based algorithm for large power systems with embedded FACTS devices is derived in [86]. In [87] this algorithm was extended to include UPFC application. It allows simultaneous or independent control of real and reactive powers and voltage magnitude. The algorithm itself is very complicated and hard to implement. It considerably increases the order of the Jacobian matrix in the iterative procedure and is quite sensitive to initial condition settings. Improper selection of the initial condition can cause the solution to oscillate or diverge.

The UPFC dynamic model known as a fundamental frequency model and can be found in [85, 88-90]. This model consists of two voltage sources, one connected in series and the other one in shunt, with the power network to represent the series and the shunt

voltage source inverters. Both voltage sources are modelled to inject voltages of fundamental power system frequency only. The model in [88] neglects the DC link capacitor dynamics which may make results obtained using this model inaccurate. Models in [85], [89] and [90] include DC link capacitor dynamics and can be used for the study of UPFC effect on the real power system behaviour.

The linearised model of the power network including UPFC is useful for small signal analysis and damping controller design. The UPFC linearised model can be found in [88] and [91]. While deriving these models some simplification have been made, i.e. the model described in [88] does not include DC link dynamics, the model derived in [91] assumes that the UPFC sending and receiving buses are also generator terminal buses. However, the UPFC can be connected between any two buses in the network. Therefore, these models do not represent the general form of the linearised network.

UPFC basic control design involves control of real and reactive power flow, sending bus voltage magnitude and DC voltage magnitude. The most frequently used control scheme is based on the vector-control approach proposed by Schauder and Metha in 1991 [92]. This scheme allows decoupled control of the real and reactive powers which makes it suitable for UPFC application. The proposed approach can be accomplished by transforming the three-phase balanced system into a synchronously rotating orthogonal system. A new coordinate system is chosen in such a way that its d component coincides with the instantaneous voltage vector and q component is orthogonal to it. In this coordinate system the d -axis current component contributes to the instantaneous real power and q -axis current accounts for the reactive power. This control scheme can be applied both for series and shunt converter control [88, 89, 93-95].

Another approach for automatic power flow control for the series converter is to decompose the voltage drop between the sending and the receiving buses into two components: one in phase with the sending bus and the other one orthogonal to it. The component in phase with the sending bus has a strong influence on the reactive power flow and the component orthogonal to it mainly influences the real power flow [90]. The shunt converter can be controlled using two PI controllers to control the sending bus voltage magnitude and the DC link voltage [90, 96]. This control scheme is simple and easy to implement.

UPFC damping controller design can be found in [90, 91, 95-97]. The supplementary control can be applied to the shunt inverter through the modulation of voltage magnitude reference signal or to the series inverter through modulation of power reference signal. In [95] and [96] the slip of the desired machine $\Delta\omega$ is used as the input signal to the damping controller. In general it is difficult to obtain this signal. Therefore, this kind of control is not feasible, and controllers depending on local measurements such as the tie-line power flow or the UPFC terminal voltage phase angle difference are more appropriate [91], [90]. All controllers in the references above are of lead-lag type, they are designed for a specific operating condition using a linearised model. However, changes in operating conditions might have a negative effect on the controller performance. More advanced control schemes such as self-tuning control, sliding mode control, and fuzzy logic control offer better dynamic performance than conventional controllers. Power system stabilizers and SVC damping controllers have been designed using some of these techniques [98-104].

The performance and impact of UPFC on the power system behaviour during fault conditions is presented in [105-107]. The author in [105] focuses on the capability of the UPFC to maintain the active and reactive powers in the compensated line including

UPFC and to diminish the fall-off of the bus voltage when there is unsymmetrical fault on the transmission line. In [78] dynamic control and performance of a UPFC under a transient condition in an interconnected three-phase transmission system is presented. The author in [79, 80] show the effectiveness of UPFC in improving system transient stability after an external transient event is validated.

Electric power systems are vulnerable to faults. The state of the power system during fault period changes to abnormal, bus voltages drop and line currents exceed their ratings, generators undergo stability problems and strong mechanical forces, consumers' loose supply, protection systems operate and major equipment may go off the system. A thorough knowledge of the state of the electric power system during a fault assists the protection experts to carefully coordinate the protection system and to minimize danger and loss of supply. The state of the power system during a fault depends on the type, the location of the fault and the pre-fault conditions. The fault may be symmetrical or unsymmetrical; unsymmetrical faults occur as single faults at a single bus or as multiple faults at several buses. The most common faults are line to ground, line-to-line and double line to ground faults. However, complex faults that involve combinations of these common faults may occur at the same bus. Since any unsymmetrical faults cause unbalanced currents to flow in the power system, the method of symmetrical components [106] is very useful in an analysis to determine the currents and voltages in all parts of the power system after occurrence of the fault.

It is of interest to explore the extent of UPFC capability in maintaining the power flow even under fault conditions, not only in the line where it is installed, but also in the adjacent line in complex power systems. The impact of UPFC in minimizing the disturbances in voltages, currents and power flows in the fault affected power system needs to be assessed. Furthermore, the effect of unsymmetrical fault positions and how

the UPFC can contribute to the faster recovery of the power system to the pre-fault conditions is of importance. However, not enough attention has been given to the effect of fault type and location on the operation of UPFC controller.

2.2 Summary

In this chapter, the methods that are used to assess the state of the power system during normal operating conditions and after being subjected to disturbances were presented. It was found that the Jacobian method which is based on the general power flow equations is the most popular method followed by the reduced Jacobian matrix, singular value decomposition, continuation method and the bifurcation method in case of dynamic stability analysis.

Many static and dynamic voltage stability indices were stated. Most of these indices are based on the solution of the quadratic equation of the two bus system. These indices may fail under some special conditions. In order to overcome these fail conditions, a new static voltage stability index is proposed. This index involves all the parameters that affecting the power system operation which is the voltage, the phase angle between voltages and the transmission line impedance. The proposed line stability has capability to identify the weakest bus and the weakest line in the interconnected power system. The assessment of the dynamic voltage stability based on MIMO transfer function and on the interaction between properly spaces defined input and output variable affecting dynamic voltage stability is presented and investigated.

The development of the power semiconductors and their effect on the power system performance were stated. FACTS controllers can be the solution to the most of the power system problems. FACTS controller can provide rapid active and reactive compensation to the power system, and therefore can enhance the power system

stability and improve power transfer capability. Among FACTS family, the UPFC controller has been selected as one of the most versatile devices that has the capability to improve power transfer capability and enhance voltage stability. A UPFC consists of two voltage source converter based controllers; one connected in series, called an SSSC converter, and used to control power transfer capability in the line where it is connected. The shunt connected converter, called STATCOM, is used to control the bus voltage at the point of common connections.

The operation of the UPFC controller connected to a weak grid and subjected to external disturbances such as unsymmetrical fault conditions and how the UPFC can contribute to faster recovery of the power system to pre-fault condition is investigated in this thesis.

2.3 References

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3: WEAK BUS IDENTIFICATION BASED ON STATIC VOLTAGE STABILITY

3.1 Introduction

This chapter describes the voltage stability phenomena. First voltage stability, voltage instability and voltage collapse are defined and the aspects of voltage stability are classified. Second the relation of voltage stability with the insufficient reactive power support at critical system nodes is presented. Thirdly, the relationships between reactive imbalances and voltage instability are discussed. Fourthly, a new static voltage stability index, based on a static criterion, is proposed and investigated. Fifthly, the static stability margin, calculated on a modal analysis method, is shown. Simulations were carried out to validate the proposed index using the Western System Coordinate Council (WSCC) 9-bus test system and IEEE 14-bus Reliability Test System (RTS). The results are presented and compared with indices found in the literature.

3.1.1 Definition and classification of power system stability

3.1.1.1 Definition of voltage stability, voltage instability and voltage collapse

The authors in [1-3] define voltage stability as follows: “Voltage stability is the ability of a power system to maintain steady acceptable voltages at all buses in the system at normal operating conditions and after being subjected to a disturbance.”

According to [1] the definition of voltage instability is “the attempt of load dynamics to restore power consumption beyond the capability of the combined transmission and generation system.”

The voltage collapse is defined as “a process by which the sequence of events accompanying voltage instability leads to a blackout or abnormally low voltages in a significant part of the power system.”

The main factor causing voltage instability is the inability of the power system to meet the demands for reactive power in heavily stressed systems by keeping the desired voltages [4]. The reactive characteristics of AC transmission lines, transformers and loads restrict the maximum power over long distances or through high reactance due to extremely high reactive power losses, which is why the reactive power required for voltage control is produced and consumed at the control area.

3.1.1.2 Classification of power system stability

A classification of power system stability based on time scale and driving force criteria is presented in Table 3.1. The driving forces for an instability mechanism are named generator-driven and load-driven. It should be noted that these terms do not exclude the effect of other components to the mechanism. The time scale is divided into short and long-term time scales.

The rotor angle stability is divided into small-signal and transient stability. The small-signal stability is present for small disturbances in the form of undamped electromechanical oscillations. The transient stability is due to a lack of synchronising torque and is initiated by large disturbances [1]. The time frame of the angle stability is that of electromechanical dynamics of the power system. This time frame is called short-term time scale, because the dynamics typically last for a few seconds.

Table 3.1 Classification of power system stability [1]

<i>Time scale</i>	<i>Generator-driven</i>		<i>Load-driven</i>	
Short-term	Rotor angle stability		Short-term voltage stability	
	Small-signal	transient		
Long-term	Frequency stability		Long-term voltage stability	
			Small disturbance	Large disturbance

When the voltage stability problem is load-driven, the voltage stability may be divided into short and long-term voltage stability according to the time scale of the load components dynamics. Short-term voltage stability is characterised by components such as induction motors, excitation of synchronous generators, and electronically controlled devices such as HVDC and FACTS compensators [2]. The time scale of short-term voltage stability is the same as the time scale of rotor angle stability.

When short-term dynamics have died out some time after the disturbance, the system enters a slower time frame. The dynamic state of the long-term time scale lasts for several minutes. Two types of instability emerge in the long-term time scale: frequency and voltage problems. Frequency problems may appear after a major disturbance resulting in power systems islanding [1]. This is because of the active power imbalance between generators and loads. An island may be either under or over-generated when the system frequency either declines or rises.

For purpose of analysis, it is sometimes useful to classify voltage stability into small and large disturbances. Small disturbance voltage stability considers the power system's

ability to control voltages after small disturbances, e.g. changes in load [1]. The analysis of small disturbance voltage stability is done in a steady state. In this case the power system can be linearised around an operating point and the analysis is typically based on eigenvalue and eigenvector techniques. Large disturbance voltage stability analysis is the response of the power system to large disturbances e.g. faults, switching or loss of load, or loss of generations [1]. Large disturbance voltage stability can be studied by using non-linear time domain simulations in the short-term time frame and load-flow analysis in the long-term time frame [5]. The voltage stability is, however, a single problem on which a combination of both linear and non-linear tools can be used

3.1.2 Power Flow Problem

The power flow or load flow is widely used in power system analysis. It plays a major role in planning the future expansion of the power system as well as helping to run existing systems in the best possible way. The network load flow solution techniques are used for steady state and dynamic analysis programs [2, 3].

The solution of power flow predicts what the electrical state of the network will be when it is subject to a specified loading condition. The result of the power flow is the voltage magnitude and the angle at each of the system nodes. These bus voltage magnitudes and angles are defined as the system state variables. This is because they allow all other system quantities to be computed such as real and reactive power flows, current flows, voltage drops, power losses etc. Power flow solution is closely associated with voltage stability analysis; it is an essential tool for voltage stability evaluation. Much of the research on voltage stability deals with the power flow computation method.

The power-flow problem solves the complex matrix equation:

$$I = YV = \frac{S^*}{V^*} \quad (3.1)$$

where,

I = nodal current injection matrix.

Y = system nodal admittance matrix.

V = unknown complex node voltage vector.

S = apparent power nodal injection vector representing specified load and generation at nodes;

where,

$$S = P + jQ \quad (3.2)$$

The Newton-Raphson method is the most general and reliable algorithm to solve the power flow problem. It involves iterations based on successive linearization using the first term of Taylor expansion of the equation to be solved. From Equation (3.1), we can write the equation for node k (bus k) as:

$$I_k = \sum_{m=1}^n Y_{km} V_m \quad (3.3)$$

where n is the number of buses and.

$$P_k - jQ_k = V_k^* I_k = V_k^* \sum_{m=1}^n Y_{km} V_m \quad (3.4)$$

with the following notation:

$$V_k = V_k e^{j\theta_k}, \dots, V_m = V_m e^{j\theta_m}, \dots, Y_{km} = Y_{km} e^{j\gamma_{km}} \quad (3.5)$$

where V_k and V_m are the voltages at nodes (buses) k and m respectively, Y_{km} is the mutual admittance between nodes k and m .

Therefore, Equation 3.4 becomes:

$$P_k + jQ_k = \sum_{m=1}^n Y_{km} V_m V_m \cos(\theta_k - \theta_m - \gamma_{km}) + j \sum_{m=1}^n Y_{km} V_m V_m \sin(\theta_k - \theta_m - \gamma_{km}) \quad (3.6)$$

The mismatch power at bus k is given by:

$$\Delta P_k = P_k^{rated} - P_k \quad (3.7)$$

$$\Delta Q_k = Q_k^{rated} - Q_k \quad (3.8)$$

The P_k and Q_k are the active and reactive power at node (bus) k calculated from Equation (3.6), P^{rated} is the rated active power.

The Newton-Raphson method solves the partitioned matrix equation:

$$\begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} = J * \begin{bmatrix} \Delta \theta \\ \Delta V \end{bmatrix} \quad (3.9)$$

where,

ΔP and ΔQ = mismatch active and reactive power vectors.

ΔV and $\Delta \theta$ = unknown voltage magnitude and angle correction vectors.

J = Jacobian matrix of partial derivative terms calculated from Equation (3.6)

Let $Y_{km} = G_{km} + jB_{km}$ where, G_{km} and B_{km} are the mutual conductances and susceptances between nodes k and m , G_{kk} and B_{kk} are the self-conductances and susceptances of the nodes k and m .

The Jacobian matrix can be obtained by taking the partial derivatives of Equation (3.6)

as follow:

$$\frac{\partial P_k}{\partial \theta_m} = V_k V_m (G_{km} \sin \theta_{km} - B_{km} \cos \theta_{km}) \quad (3.10)$$

$$V_m \frac{\partial P_k}{\partial \theta_m} = V_k V_m (G_{km} \cos \theta_{km} + B_{km} \sin \theta_{km}) \quad (3.11)$$

$$\frac{\partial Q_k}{\partial \theta_m} = -V_m \frac{\partial P_k}{\partial V_m} \quad (3.12)$$

$$V_m \frac{\partial Q_k}{\partial V_m} = \frac{\partial P_k}{\partial \theta_m} \quad (3.13)$$

$$\frac{\partial P_k}{\partial \theta_k} = -Q_k - B_{kk} V_k^2 \quad (3.14)$$

$$V_k \frac{\partial P_k}{\partial V_k} = P_k + G_{kk} V_k^2 \quad (3.15)$$

$$\frac{\partial Q_k}{\partial \theta_k} = P_k - G_{kk} V_k^2 \quad (3.16)$$

$$V_k \frac{\partial Q_k}{\partial V_k} = Q_k - B_{kk} V_k^2 \quad (3.17)$$

Then, the Jacobian matrix is:

$$J = \begin{bmatrix} \frac{\partial P_k}{\partial \theta} & \frac{\partial P_k}{\partial V} \\ \frac{\partial Q_k}{\partial \theta} & \frac{\partial Q_k}{\partial V} \end{bmatrix} \quad (3.18)$$

A MATLAB program based on Equation 3.18 is used to generate the power flow for the 14-bus IEEE reliability test system and the Western System Coordinate Council WSCC 3-machine 9-bus test system by using the Newton-Raphson method.

3.1.3 Modal analysis for voltage stability evaluation

Modal analysis approach [5] involves the computation of a small number of eigenvalues and associated eigenvectors of a reduced Jacobian matrix which retains the Q-V

relationships in the network and includes the appropriate characteristics of generators, loads, reactive power compensating devices (FACTS devices), and HVDC converters. By using the reduced Jacobian matrix instead of the system state matrix, the focus is on the voltage and reactive power characteristics. The eigenvalues of the Jacobian identify different modes through which the system could become voltage unstable. The magnitudes of the eigenvalues provide a relative measure of proximity to instability. The eigenvectors, on the other hand, provide information related to the mechanism of loss of voltage stability.

A system is voltage stable at a given operating condition if, for every bus in the system, the bus voltage magnitude increases as reactive power injection at the same bus is increased. A system is voltage unstable if, for at least one bus in the system, bus voltage magnitude decreases as the reactive power injection at the same bus is increased. In other words, a system is stable if V-Q sensitivity is positive for every bus and unstable if V-Q sensitivity is negative for at least one bus.

3.1.3.1 Reduced Jacobian matrix

The linearised steady state system power voltage equations are given by [6, 7]:

$$\begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} = \begin{bmatrix} J_{P\theta} & J_{PV} \\ J_{Q\theta} & J_{QV} \end{bmatrix} \begin{bmatrix} \Delta\theta \\ \Delta V \end{bmatrix} = [J] \begin{bmatrix} \Delta\theta \\ \Delta V \end{bmatrix} \quad (3.19)$$

where

J is the Jacobian matrix

ΔP is the incremental change in bus real power.

ΔQ is the incremental change in bus reactive power.

$\Delta\theta$ is the incremental change in bus voltage angle.

ΔV is the incremental change in bus voltage magnitude.

It's well known that, the system voltage is affected by both real and reactive power variations. In order to focus the study of the reactive demand and reducing dimensions of the Jacobian matrix J , the real power term in Equation 3.19 is eliminated by setting $\Delta P = 0$. Therefore;

$$\Delta Q = \begin{pmatrix} J_{QV} & -J_{Q\theta} * J_{P\theta}^{-1} * J_{PV} \end{pmatrix} * \Delta V = J_R \Delta V \quad (3.20)$$

and

$$\Delta V = J_R^{-1} \Delta Q \quad (3.21)$$

where

$$J_R = \begin{pmatrix} J_{QV} & -J_{Q\theta} * J_{P\theta}^{-1} * J_{PV} \end{pmatrix} \quad (3.22)$$

J_R is called the reduced Jacobian matrix of the system; J_R is the matrix which directly relates the bus voltage magnitude and reactive power injection. Eliminating the real power and angle from the system steady state equation allows us to focus on the study of the reactive power demand, supply problem of the system and minimize computational effort.

The application of singular value decomposition to the reduced Jacobian matrix J_R also allows the static voltage stability analysis [8-10].

3.1.3.2 Modes of voltage stability

Let [6],

$$J_R = \xi \wedge \eta \quad (3.23)$$

where,

ξ is the left eigenvector of J_R .

η is the right eigenvector of J_R .

Λ is the diagonal eigenvalue matrix of J_R .

and

$$J_R^{-1} = \xi \Lambda^{-1} \eta \quad (3.24)$$

from equation 3.19 we have:

$$\Delta V = \xi \Lambda^{-1} \eta \Delta Q \quad (3.25)$$

or

$$\Delta V = \sum_i \frac{\xi_i \eta_i}{\lambda_i} \Delta Q \quad (3.26)$$

where λ_i is the i^{th} eigenvalue, ξ_i is the i^{th} column left eigenvector and η_i is the i^{th} row right eigenvector of J_R .

Similar to the concept used in linear dynamic system analysis [6]. Each eigenvalue λ_i and the corresponding left and right eigenvectors ξ_i and η_i define the i^{th} mode of the system. The i^{th} modal reactive power variation is defined as:

$$\Delta Q_{mi} = K_i \xi_i \quad (3.27)$$

where K_i is a scale factor to normalize vector ΔQ_i so that;

$$k_i^2 \sum_j \xi_{ji}^2 = 1 \quad (3.28)$$

with ξ_{ji} the j^{th} element of ξ_i .

The corresponding i^{th} modal voltage variation is:

$$\Delta V_{mi} = \frac{1}{\lambda_i} \Delta Q_{mi} \quad (3.29)$$

It is seen that, when the reactive power variation is along the direction of ξ_i , the corresponding voltage variation is also along the same direction with the magnitude is amplified by a factor which is equal to the magnitude of the inverse of the i^{th} eigenvalue. In this sense, the magnitude of each eigenvalue λ_i determines the weakness of the corresponding modal voltage. The smaller the magnitude of λ_i , the weaker the corresponding modal voltage. If $\lambda_i = 0$, the i^{th} modal voltage will collapse because any change in that modal reactive power will cause infinite modal voltage variation.

In equation 3.26, let $\Delta Q = e_k$, where e_k has all its elements zero except the k^{th} one being 1. Then:

$$\Delta V = \sum_i \frac{\eta_{ik} \xi_i}{\lambda_i} \quad (3.30)$$

with η_{ik} the k^{th} element of η_i .

Therefore, $V-Q$ sensitivity at bus k is:

$$\frac{\partial V_k}{\partial Q_k} = \sum_i \frac{\eta_{ik} \xi_{ik}}{\lambda_i} = \sum_i \frac{P_{ki}}{\lambda_i} \quad (3.31)$$

A system is voltage stable if the eigenvalues of the Jacobian are all positive [1, 6]. From control system view point, the analysis of small signal stability using eigenvalue techniques may find the condition for the eigenvalues of the Jacobian to be positive for voltage stability analysis, a little confusing, because a positive real eigenvalue indicates that the system is unstable. The relationship between system voltage stability and eigenvalues of the reduced Jacobian matrix J_R is best understood by relating the eigenvalues of the J_R with the $V-Q$ sensitivities, (which must be positive for stability), at each bus.

For practical purposes, the reduced Jacobian matrix J_R can be taken as a symmetric matrix as a result, the eigenvalue of J_R are close to being purely real. The system is stable, if all the eigenvalues are positive, J_R is positive definite, thus $V-Q$ sensitivities are also positive. As the system is stressed, if the eigenvalues J_R become smaller until, at the critical point of system voltage stability, at least one of the eigenvalues of J_R becomes zero. The system is unstable, if some of the eigenvalues of J_R are negative. In this case, the system has passed the critical point of voltage stability because the eigenvalues of J_R change continuously from positive to zero to negative as the system is stressed.

Therefore, by using modal analysis technique, the magnitude of the eigenvalues can provide a relative measure of the proximity of the power system to voltage instability. The main drawback of this technique it does not provide an absolute measure because of the non-linearity of the problem. This analogous to the damping factor in small signal stability analysis, which is indicative of the degree of damping but is not an absolute measure of stability margin. In order to determine the amount of active power (MW) that can be added to the system before suffering from voltage instability, the system is stressed incrementally until it becomes unstable and modal analysis applied at each operating point. The application of modal analysis is to help in determining how stable the system is, how much extra load or power transfer level should be added when the system reaches the voltage stability critical point, the voltage stability critical areas and to describe the mechanism of instability by identifying elements which participate in each mode.

3.1.3.3 Identification of the weakest buses

The participation factor of bus k to mode i is defined as:

$$P_{ki} = \xi_{ki} \eta_{ki} \quad (3.32)$$

From equation (3.32), P_{ki} indicate the contribution of the i^{th} eigenvalue to the $V-Q$ sensitivity at bus k . The bigger the value of P_{ki} , the more λ_i , contributes in determining $V-Q$ sensitivity at bus k . For all the small eigenvalues, bus participation factors determine the areas close to the voltage instability.

3.2 Static voltage stability analysis

Static voltage instability is mainly associated with reactive power imbalances. Reactive power increase can limit the load-ability of the bus that receives power. If the reactive power reaches its limit, the system will approach the maximum loading point or voltage collapse point. In static voltage stability, any changes in the power system conditions will lead to a shortage of reactive power and declining voltage. This phenomenon can be seen from the plot of the voltage at the receiving end versus the power transfer as shown in Figure 3.1 The plot is popularly referred to as the P-V curve or ‘Nose curve’. As the power transfer increases from the normal operating point, the voltage at the receiving end decreases. Eventually, the critical (nose) point is reached at which any increase of active power transfer beyond the point will lead to a very rapid decrease in voltage magnitude leading to voltage collapse. Before reaching the critical point or voltage collapse point, a significant drop in voltage magnitude can be observed. The upper part of the P-V curve is considered to be stable whilst the lower part is considered to be unstable. Consequently normal operation is restricted to the upper part of the curve. In addition, normal loading margin P_{margin} is usually applied between the maximum permissible demand and the nose. The maximum load that can be increased prior to voltage collapse point is called static voltage stability margin or loading margin of the system. The only way to save the power system from voltage collapse is by

reducing reactive power losses in the transmission system or by adding additional reactive power support [11]. This has to be carried out at the planning stage. At its earlier development stage, voltage stability used to be analysed by static analysis methods, such as load flow programs. Load flow analysis is used to determine the maximum permissible demand by gradually increasing the load until the flow fails to converge.

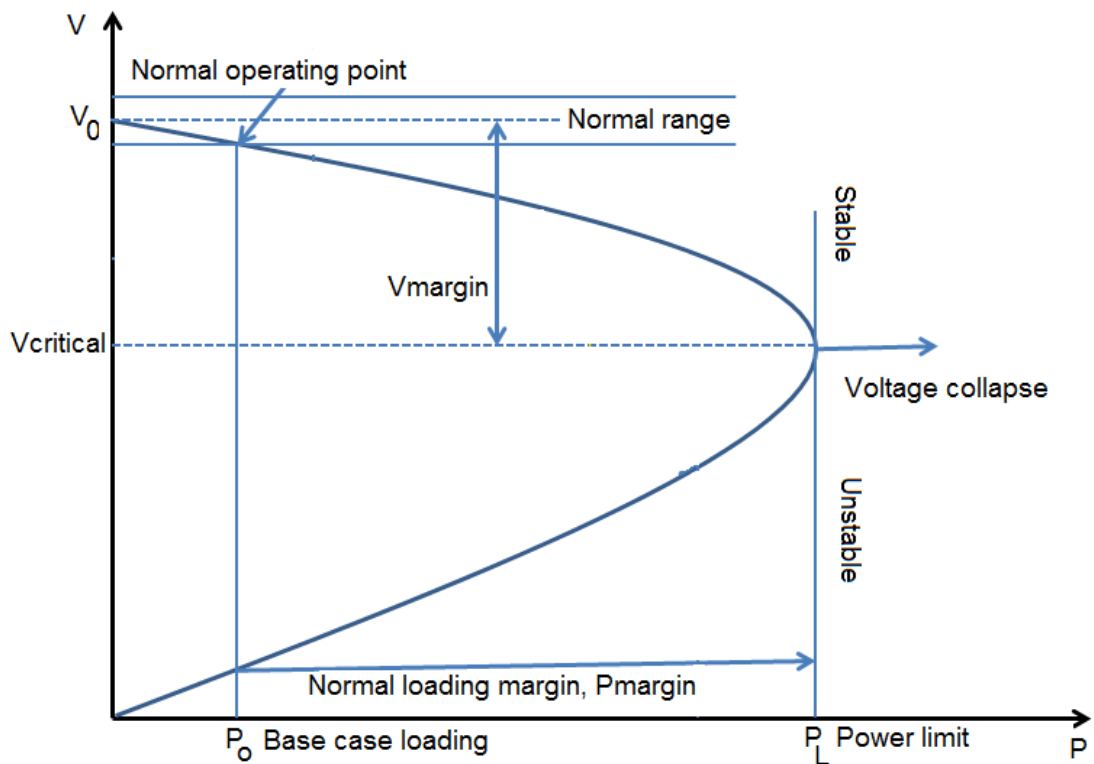


Figure 3.1 The general character of P-V curves [1]

With Q-V curves, it is possible to know the maximum reactive power that can be achieved or added to a bus before reaching the minimum voltage limit. A typical Q-V curve is presented as in Figure 3.2. The curve can be produced by varying the reactive power demand (or injection) at the load bus while maintaining the active power constant, so corresponding load voltage is determined through load flow recalculation. The reactive power margin is the MVar distance from the operating point to the bottom

of the Q-V curve. The Q-V curve can be used as an index for voltage instability. The point where dQ/dV is zero is the point of voltage instability.

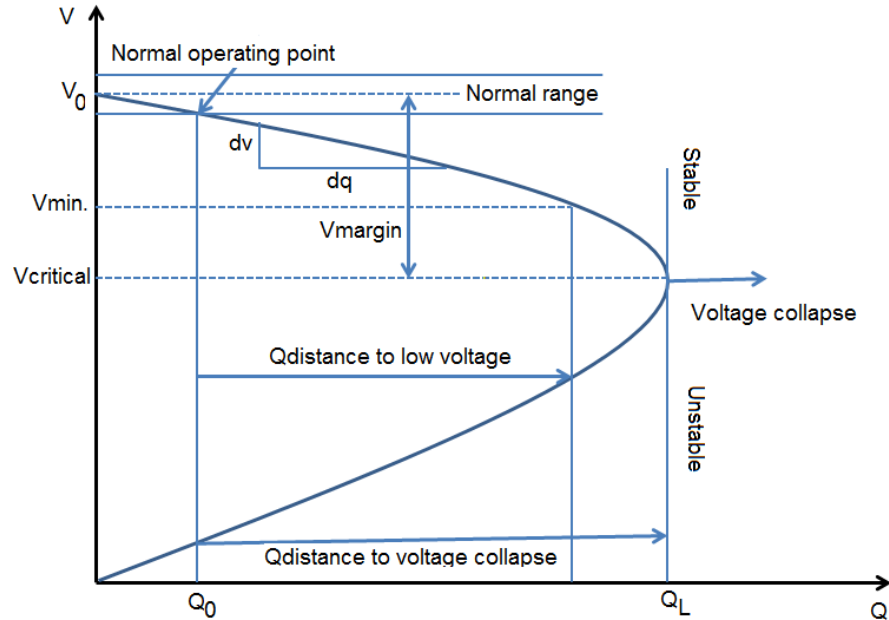


Figure 3.2 The general character of Q-V curves [1]

3.2.1 P-V and P-Q Curves as static voltage stability indicator

P-V and Q-V curves are used as static voltage stability indicators to analyse steady state voltage stability which is the stability of the power system in normal operation. The characteristics of voltage stability are illustrated by a simple two bus power system shown in Figure 3.3 V_i sending end voltage, V_j receiving end voltage, Z_{ij} transmission line impedance, S_i sending apparent power, and S_j receiving end apparent power.

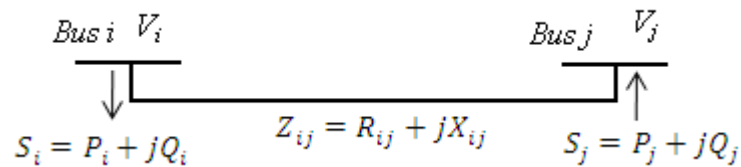


Figure 3.3 Single line diagram of two bus system

The purpose of the study is to calculate the receiving end voltage V_j with different values of load power. The receiving end voltage can be calculated analytically in this simple power system. Generally voltages are solved with a load flow program. The quadratic equation for the voltage at receiving end is given by:

$$\begin{aligned} |V_j|^4 + |V_j|^2 \left[2(P_j R_{ij} + Q_j X_{ij}) - |V_i|^2 \right] + R_{ij}^2 P_j^2 + X_{ij}^2 Q_j^2 + X_{ij}^2 P_j^2 + R_{ij}^2 Q_j^2 \\ = 0 \end{aligned} \quad (3.33)$$

The solution for the receiving end voltage V_j is:

$$\begin{aligned} |V_j| = \\ \pm \sqrt{\frac{|V_i|^2 - 2(P_j R_{ij} + Q_j X_{ij}) \pm \sqrt{\left[|V_i|^2 - 2(P_j R_{ij} + Q_j X_{ij}) \right]^2 - 4(R_{ij}^2 + X_{ij}^2)(P_j^2 + Q_j^2)}}{2}} \end{aligned} \quad (3.34)$$

The solutions of Equation 3.34 are often presented as P-V and Q-V curves as shown in Figure 3.1 and Figure 3. 2.

Different P-V and Q-V curves can be simulated and load flow equations are solved with the help of MATLAB program, depending on the system parameters chosen to plot these curves. The most commonly test power system found in the literature is IEEE 14 bus Reliability Test System (RTS) [12, 13], shown in Figure 3.4 is used to plot a family of P-V and Q-V curves. P-V curves are plotted by maintaining the sending end voltage constant while the load at the receiving end is varied at a constant power factor and the voltage at the receiving end is calculated. The process starts from the current operating point (base case), which indicates the initial load level of the power system. In each step, a load flow for the power system is performed. This process continues until the

voltage collapse occurs. The Q-V curve are produced by varying the reactive power demand (or injection) at the load bus while maintaining the active power constant and the corresponding load voltage is determined through load flow recalculation. The power flow test is performed to all buses of the IEEE 14 bus reliability test system but only bus 14 is presented here because it has the minimum loadability compared with the other buses and it is ranked as the weakest bus in the test system. It requires special care in the planning stage to provide the necessary power support to prevent it from voltage collapse and the transmission line connecting bus 13 to bus 14 is identified as the weakest transmission line. More details are presented in [12, 13]. In order to plot the PV and Q-V curves, the base value of the transmission line impedance between bus 13 and bus 14 is $Z_{13-14} = R+jX = 0.174 + j0.348 \Omega$.

The Q-V curves of bus 14 are shown in Figure 3.5 In this figure, each curve is plotted by increasing the active and reactive power at bus 14 simultaneously by the same step values and at a different value of the transmission line reactance of the line L_{13-14} . From the figure, it is clear that, as the apparent power increases the voltage reaches the voltage collapse point (0.575 per unit (pu)) at around 0.7 pu load with minimum stability margin. As the transmission line reactance decreases (i.e. power factor), the stability margin increases and the maximum load-ability of bus 14 increases.

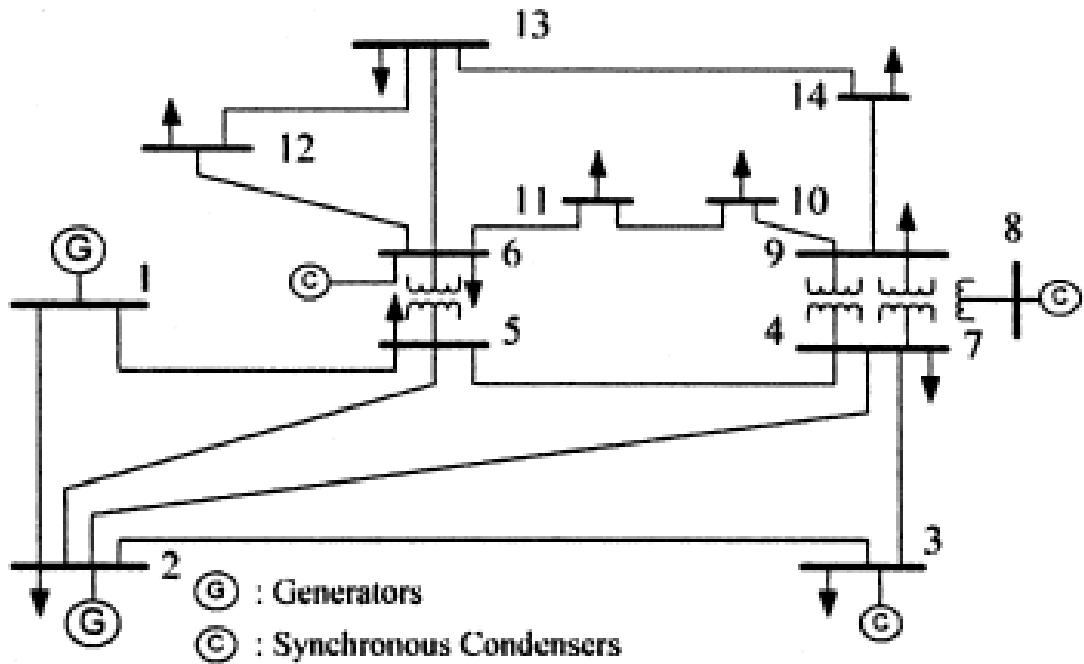


Figure 3.4 Single line diagrams for the IEEE 14 bus test system [12]

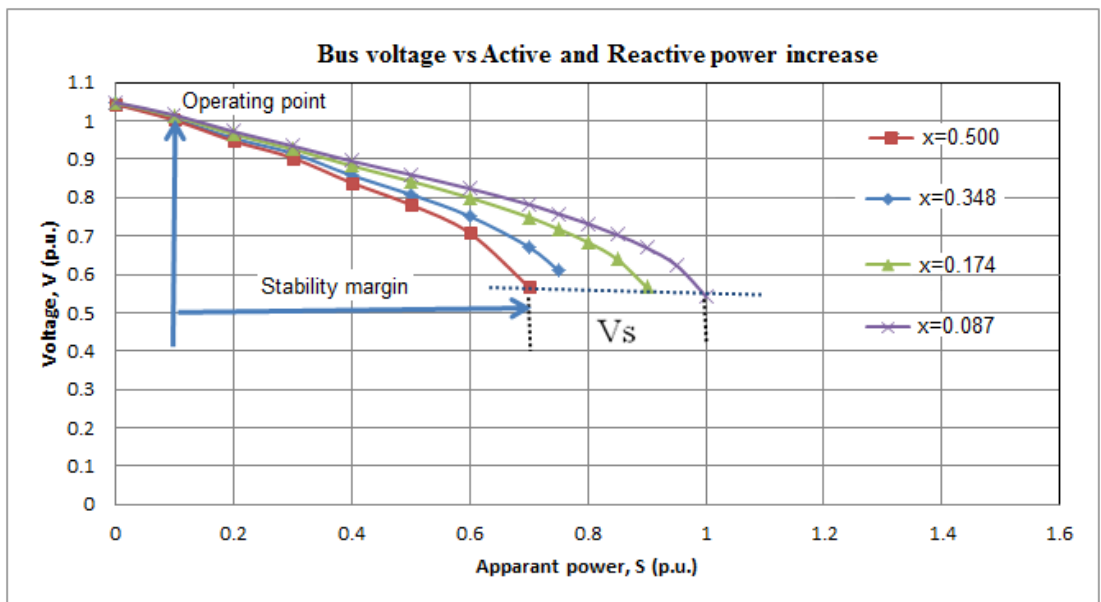


Figure 3.5 Maximum loading points for active and reactive loads at Bus 14

Figure 3.6 show PV curves at bus 14 for IEEE 14 bus RTS. Each curve in the figure is plotted at constant power factor by increasing the active power gradually until the maximum loading point is reached, which is also referred to as the maximum system

load-ability, which in turn corresponds to a singularity of the Jacobian power flow equations. Any attempt to increase the active power beyond its maximum values and the result is a voltage collapse of the system. The minimum operating point of the active power is approximately 0.25 pu and the maximum operating point is 1.3 pu in the base case and it changes as the transmission line reactance changes. The voltage stability margin is increases by decreasing the loading factor.

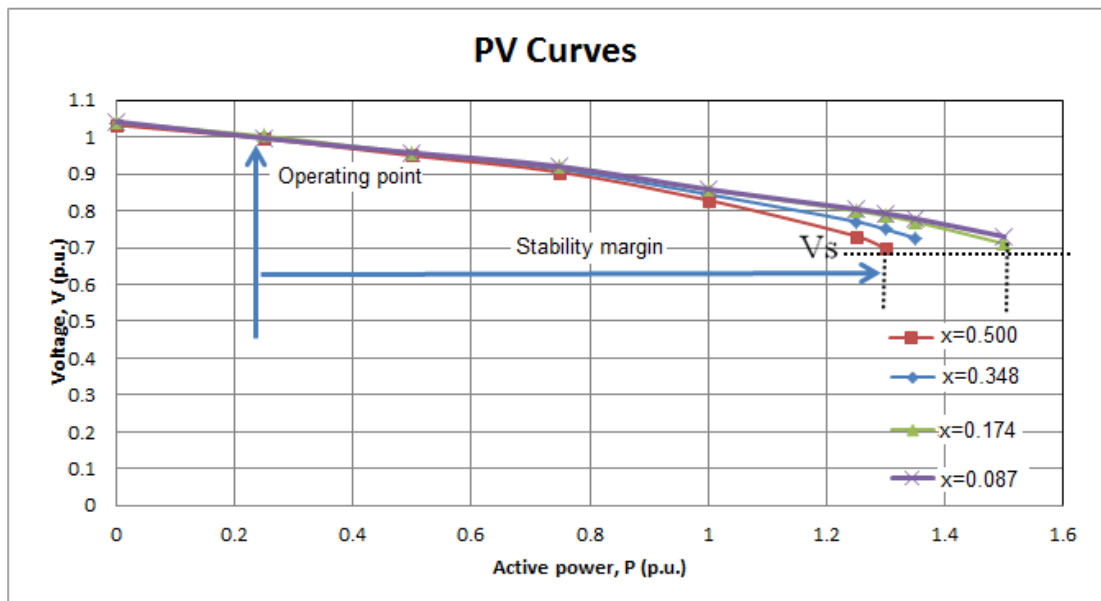


Figure 3.6 Maximum loading points for active load at Bus 14

Figure 3.7 show Q-V curves at bus 14 for the IEEE 14 bus RTS. Each curve in the figure is plotted at constant active power by increasing the reactive power gradually until the maximum loading point is reached. Q-V curves give the maximum reactive power demand at a particular bus that can be handled before the system suffers from voltage collapse. The minimum operating reactive power point is 0.1 pu and the maximum point is 1.15 pu in the base case and it changes depending on the loading factor.

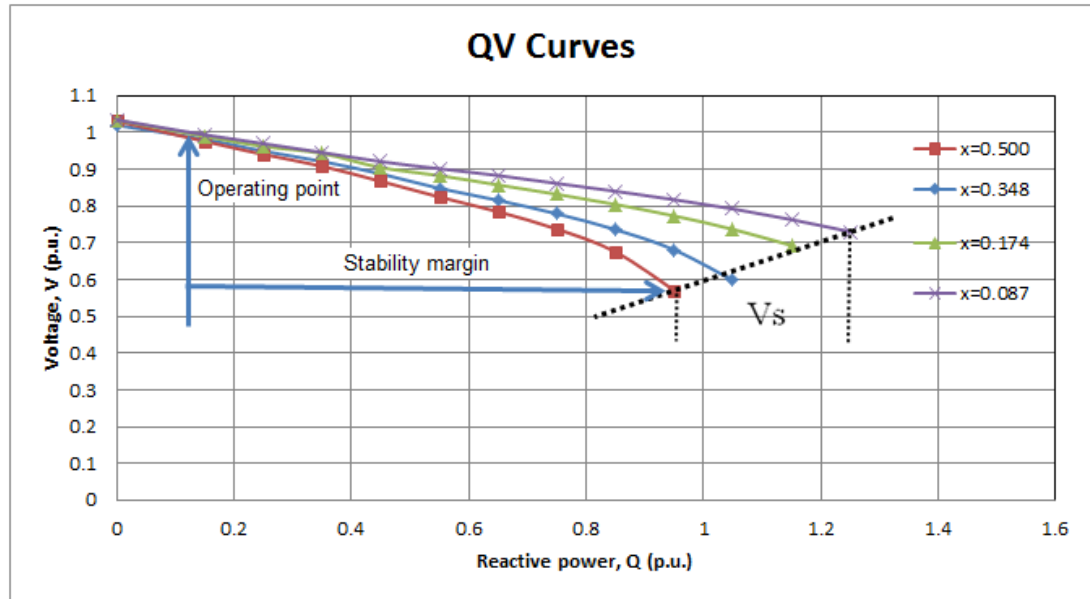


Figure 3.7 Maximum loading points for reactive load at Bus 14

Analysing figures 3.5-7, the voltage stability margin can be easily calculated with P-V curves. These curves show the bus voltage level as the loading factor increases. We observe that, as the power system load is gradually increased, the voltage at the busbars decreases. The Q-V curve shows the voltage stability margin of a particular bus, i.e. these curves show how much reactive power demand can be increased before the system suffers a voltage collapse.

In order to get smooth and reliable operation as well as uninterrupted dispatching loads, a new simple index for online voltage stability monitoring based on the solution of quadratic equation (Equation 3.34) for the voltage at the receiving end of the two bus system shown in Figure 3.3 is proposed, aiming to detect the system load-ability and identifying the weakest bus as well as a critical line in the power system. The proposed index is validated using a MATLAB (Simulink) program and compared with two indices found in literature presented in section 2.1.3 [14, 15].

3.2.2 Proposed Index Formulation

As discussed in section 3.2.1 the solution for the receiving end voltage V_j is given by Equation 3.34. Therefore, in order to simplify Equation 3.34 some simplification must be made. Let:

$$a = |V_i|^2 - 2(P_j R_{ij} + Q_j X_{ij}) \text{ and } b = (R_{ij}^2 + X_{ij}^2)(P_j^2 + Q_j^2) \quad (3.35)$$

$$\therefore |V_j| = \pm \sqrt{\frac{a \pm \sqrt{a^2 - 4b}}{2}} \quad (3.36)$$

There are four solutions for V_j : two positive and two negative, V_j must be non-negative, therefore the two negative solution are not true. To derive a positive feasible solution for a real system, the expression under the square root signs must be positive. Therefore,

$a \pm \sqrt{a^2 - 4b} \leq 1$ or $a^2 - 4b = 0$. Since b is greater than zero, therefore a must be non-negative for the condition to be satisfied. or $0 < \frac{2\sqrt{b}}{a} \leq 1$

By substituting a and b we define a new line voltage stability index LSZ based on the apparent power S and the transmission line impedance Z is proposed as:

$$LSZ = 2 \frac{\sqrt{(R_{ij}^2 + X_{ij}^2)(P_j^2 + Q_j^2)}}{|V_i|^2 - 2(P_j R_{ij} + Q_j X_{ij})} \quad (3.37)$$

Simplifying:

$$LSZ = 2 \frac{|Z||S|}{|V_i|^2 - 2|Z|(P_j \cos \theta + Q_j \sin \theta)} \leq 1 \quad (3.38)$$

where Z is the transmission line impedance, S is the apparent power P_j and Q_j are the active and reactive power at the receiving end, θ is the impedance angle and V_i is the sending end voltage.

The line that exhibits LSZ close to 1.00 implies that it is approaching its instability point. If LSZ goes beyond 1.00, one of the buses to the connected line will experience a sudden voltage drop leading to voltage collapse. The transmission line with the largest value of LSZ is taken as the weakest line and must receive special care to maintain voltage stability within a certain limit.

In order to investigate the effectiveness of the proposed index, a MATLAB (Simulink) simulation was conducted on two well-known test systems known as the IEEE 14 bus reliability test system and the Western System Coordinate Council (WSCC) 3-machine, 9- bus test system. The simulation result for the IEEE 14-bus test system is presented in [12, 13]. In the following section the simulation for the WSCC test system is presented and investigated.

3.2.3 Test system description

To test the proposed index, the voltage stability analysis was conducted on the well-known Western System Coordinate Council (WSCC) 3-machine, 9- bus test system [1] shown in Figure 3.8. The test system connected in a loop configuration, consists essentially of nine buses (B1 to B9) interconnected through transmission lines (L1, L2, L3), three power plants and three loads connected at buses B5, B6, and B8 respectively.

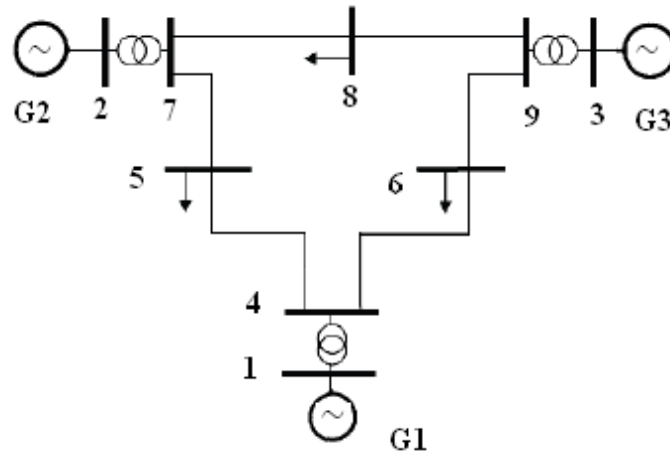


Figure 3.8 WSCC 3-machines, 9-bus test system [1]

3.2.4 Experiments

To assess the static voltage stability of the WSCC test power system the reactive power loading is increased gradually at a chosen bus each time until it is near to voltage collapse whilst keeping the loads on the other buses constant. From the results, the proposed index LSZ was calculated at each line for every load change. Performing power flow programs on the proposed test system, the following steps been calculated:

- Calculation of LSZ by increasing the reactive power at each bus until near to voltage collapse.
- Calculating the voltage profile for all buses.
- Determination of voltage stability margin.

3.2.5 Simulation Results and discussion

The test system described in the previous section is simulated and load flow equations are solved to study the effectiveness of the proposed index and to determine the weakest bus in the WSCC test system. The stability index was calculated for all buses but only buses 5, 6, and 8 are presented here as they are ranked as the weakest buses in the test

system. Figure 3.9 shows the *LSZ* is plotted versus reactive power load change at buses (5, 6, and 8).

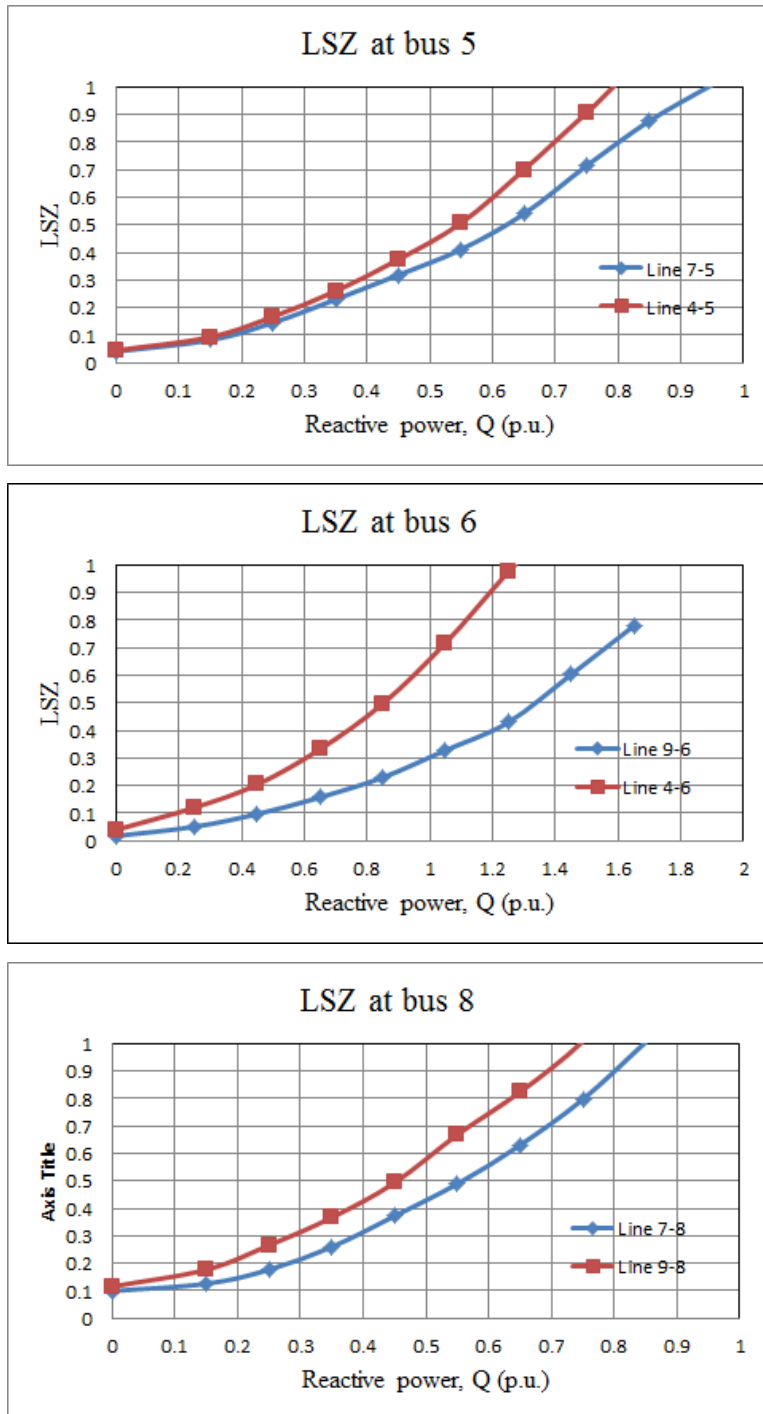


Figure 3.9 *LSZ* vs reactive power loading at buses (5, 6, 8) of WSCC test system

It is clear from the figures that the line with highest *LSZ* is ranked as the most sensitive line. Therefore, the line connecting bus 4 to bus 5 is the most critical line with respect to

bus 5, and the line connecting bus 4 to bus 6 is the most critical line with respect to bus 6. Similarly the line connecting bus 9 to bus 8 is the most critical line with respect to bus 8. From the results, bus 8 is ranked as the most sensitive bus (weakest bus) because it has the minimum load-ability compared with the other lines.

3.2.6 Weak bus identification based on modal analysis

The modal analysis method is applied to the same test system. The voltage profile of the buses is presented from the load flow simulation. Then, the minimum eigenvalue of the reduced Jacobian matrix is calculated. After that, the weakest load buses, which are subject to voltage collapse, are identified by computing the participating factors. The results are shown in Figure 3.10 to Figure 3.12.

Figure 3.10 shows the voltage profile of all buses of the Western System Coordinating Council (WSCC) 3-Machines 9-Bus system as obtained from the load flow program. It can be seen that all the bus voltages are within the acceptable level ($\pm 10\%$). The lowest voltage compared to the other buses can be noticed in bus 8. The load flow result agrees with the proposed index simulated results

Since there are nine buses among which there is one swing bus and two PV buses, then the total number of eigenvalues of the reduced Jacobian matrix J_R^{-1} is expected to be six as shown in Table 3.1.

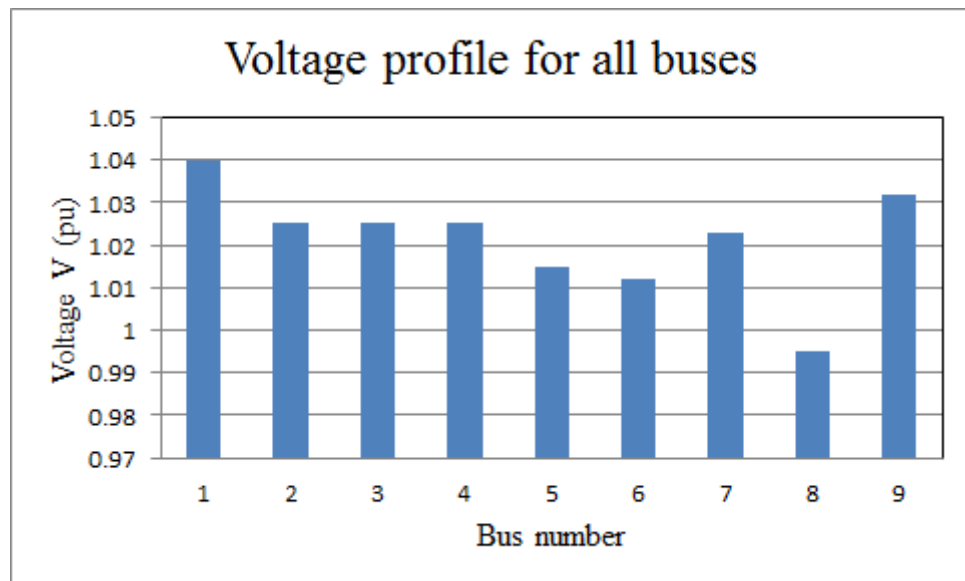


Figure 3.10 Voltage profiles of all buses of the WSCC test system

Table 3.1 WSCC 3-Machines 9-Bus system eigenvalues

#	1	2	3	4	5	6
Eigenvalue	51.094	46.6306	5.9590	12.9438	14.9108	36.305

Note that from Table 3.1, all the eigenvalues are positive which means that the system voltage is stable. Also, it can be noticed that the minimum eigenvalue $\lambda = 5.9590$ is the most critical mode.

The participating factor for this mode has been calculated and the result is shown in Figure 3.11. The result shows that the buses 5, 6 and 8 have the highest participation factors to the critical mode. The largest participation factor value (0.3) at bus 8 indicates the highest contribution of this bus to the voltage collapse.

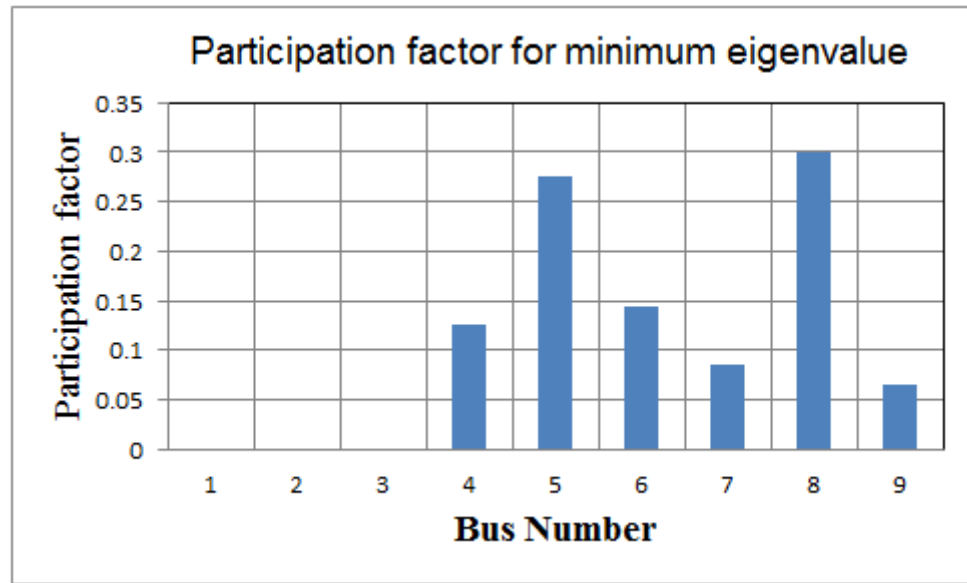


Figure 3.11 The participating factor of all buses for most critical mode for the test system

The Q-V curves are used to determine the pu distance to the voltage instability point or the voltage stability margins as discussed in section (3.2.1). The margins were determined between the base case loading points and the maximum loading points before the voltage collapse. Consequently, these curves can be used to predict the maximum-stability margins that can be reached. In other words, by using Q-V curves, it is possible for the operators and the planners to know what is the maximum reactive power is that can be achieved or added to the weakest bus before reaching minimum voltage limit or voltage instability. In addition, the calculated Mvar margins could relate to the size of shunt capacitor or static Var compensation in the load area.

The Q-V curves were computed for the weakest buses of the test system as expected by the modal analysis. The curves are shown in Figure 3.12.

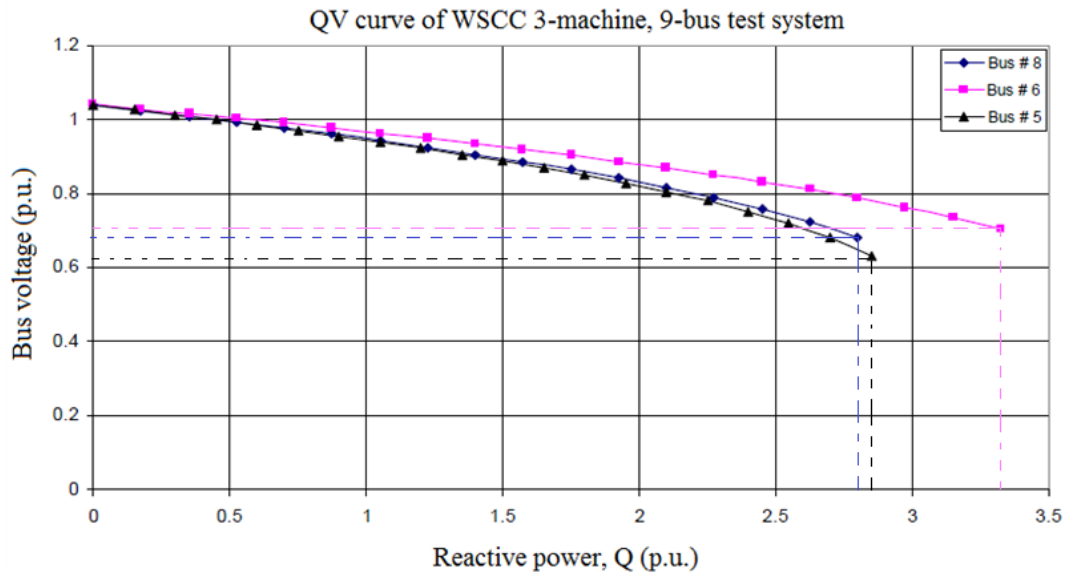


Figure 3.12 The Q-V curves at buses 5, 6 and 8 for the test system

Table 3.2 shows evaluation of the buses 5, 6, and 8 Q-V curves. These results can be used effectively in planning stage.

Table 3.2 Voltage and reactive power margins for the WSCC 3-Machines 9-Bus system from Q-V curves

Bus 5					Bus 6					Bus 8				
Operating Point		Max. withstand		Stability margin	Operating Point		Max. withstand		Stability margin	Operating Point		Max. withstand		Stability margin
V (pu)	Q (pu)	V (pu)	Q (pu)	Q (pu)	V (pu)	Q (pu)	V (pu)	Q (pu)	Q (pu)	V (pu)	Q (pu)	V (pu)	Q (pu)	Q (pu)
1.0	0.3	0.63	2.85	2.55	1.0	0.35	0.704	3.33	2.98	1.0	0.5	0.72	2.625	2.125

The Q-V curves obtained in section 3.2 and shown in Figure 3.12 confirm the results by the proposed index. It can be seen clearly that bus 8 is the most critical bus compared with the other buses. This means the disturbances on the reactive load power will cause the largest variation on the voltage magnitude at bus 8. Therefore, bus 8 is identified as the weakest bus in the test system.

3.3 Summary

In this chapter, a new static voltage stability index related to the voltage drop in the critical bus was proposed and investigated. It is referred to as the LSZ index. It is based on the transmission line impedance and the apparent power at the receiving end. The proposed index determines the maximum load that is possible to be connected to a bus in order to maintain the voltage stability margin before the system suffers from voltage collapse. In order to investigate the effectiveness of the proposed index, IEEE 14 bus reliability test system and the WSCC 3-machine, 9-bus test system was used. The simulation result detects clearly the stressed condition of the lines, identifies with degree of accuracy the weakest buses prone to voltage collapse and determines the static stability margin of the power to work in save operation. The most effective way for power networks to improve the voltage profile and static voltage stability margin at the weakest bus is by introducing FACTS system.

The advantages of the developed monitoring index *LSZ* are:

- The proposed index involves both active and reactive power in the calculation, so, it is slightly better compared to the previously stated indices.
- The proposed index includes all the parameters that affecting the power transfer capability such as voltage, voltage angle and the transmission line impedance.
- Easy in calculation and less computational time.
- The proposed index identifies with the degree of accuracy the weakest line, the weakest bus and the distance to voltage collapse point (stability margin).

The disadvantages of the developed monitoring index *LSZ* is:

- The proposed index is derived from two bus system quadratic equation assuming the voltage angle difference between the voltage angle and the transmission line impedance angle is zero, it implies that *LSZ* may be not suitable for very heavy load lines due to the large angle difference between them.

The modal analysis method was applied to the reduced Jacobian matrix in order to identify the weakest based on the calculation of the minimum eigenvalue and the highest participating factor corresponding to that eigenvalue which represent the most critical bus in the test system. The result shows an agreement with the proposed index.

The Q-V curve was used to determine the Mvar distance to the voltage instability point. The margins were determined between the base case loading points and the maximum loading points before the voltage collapse. Consequently, these curves can be used to predict the maximum-stability margins that can be reached.

The simulation shows an agreement between the studied line stability indices with the best result obtained by the proposed line stability index *LSZ*. The computed results show an agreement with other indices found in the literature [14, 15].

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4: WEAK BUS IDENTIFICATION BASED ON DYNAMIC VOLTAGE STABILITY

4.1 Introduction

In the previous chapter, static voltage stability was investigated. However, a power system is typically a large dynamic system and its dynamic behaviour has great influence on the voltage stability. Therefore, in order to get more realistic results it is necessary to take the full dynamic system model into account.

Dynamic phenomena causing voltage instability, occurring in electric power systems subjected to strong load demands, lead to a progressive decreasing of the voltage magnitude at one or more buses, resulting sometimes in network islanding, thus leading to local or global blackouts. Oscillatory instability and voltage instability are two major problems. Consequently, dynamic voltage stability poses a primary threat to system security and reliability.

Dynamic voltage stability plays a very important role during the planning and design stages of an electric power network as well as during the system operation. In the last years in various countries worldwide, several power network collapses caused by voltage problems have been reported. This can be produced by a lack of sufficient reactive power reserve during a heavy load or by the occurrence of severe contingencies. The collapse effect can be characterized by a continuous decrease of the power system voltage. In the initial stage the decrease of the system voltage starts gradually and then decreases rapidly.

In this chapter, the singular value decomposition technique was applied to the multi-input multi-output (MIMO) transfer function of the test system in order to carry out the dynamic stability analysis. The MIMO system is defined takes into account the critical nodal voltages as outputs and possible control variables as the input. The proposed technique takes the advantages of the classical static voltage stability analysis and the modern multi-variable feedback control theory. The singular values and singular vectors are calculated for frequencies corresponding to the critical system modes. The output singular vectors shows at which bus the voltage magnitude is the most critical. Using the magnitudes of the input singular vectors the most suitable inputs for countermeasures can be selected. Simulations were carried out to validate the proposed indices using the Western System Coordinate Council (WSCC) 3-machine, 9-bus test system. The results were presented and discussed.

4.2 Mathematical model for dynamic voltage stability analysis

The mathematical model for the dynamic voltage stability study of a power system comprises a set of first order differential equations and a set of algebraic equations [1-3] as:

$$\dot{x} = f(x, y) \quad (4.1)$$

$$0 = g(x, y) \quad (4.2)$$

where x is the state vector of the system represent the input and y vector containing bus voltages represent the output of the system.

Equations 4.1 and Equation 4.2 are usually solved in the time domain by means of the numerical integration and power flow analysis methods [1, 4]

The steady state equilibrium values (x_0, y_0) of the dynamic system can be evaluated by setting the derivatives in Equation 4.1 equal to zero. Through the linearization about (x_0, y_0) , Equations 4.1 and Equation 4.2 are expressed as follows [3, 4]:

$$\frac{d\Delta x}{dt} = A\Delta x + B\Delta y \quad (4.3)$$

$$0 = C\Delta x + D\Delta y \quad (4.4)$$

where A, B, C and D are the sub-matrices of the Jacobian matrix. Further, by eliminating Δy , the linearised state equation can be rewritten as [3, 4]:

$$\frac{d\Delta x}{dt} = \left(A - BD^{-1}C \right) \Delta x = \tilde{A}\Delta x \quad (4.5)$$

where \tilde{A} is the reduced Jacobian matrix. The static bifurcation will occur when $\det(D) = 0$. For the dynamic bifurcation phenomenon, it is always assumed that $\det(D) \neq 0$ and that D^{-1} exists [3, 4]. By analysing the eigenvalue of \tilde{A} , dynamic voltage stability can be obtained.

4.3 Singular value analysis

Singular value decomposition is an important and practically useful orthogonal decomposition method used for matrix computations [5]. If the matrix A is an n by n quadratic real matrix, then the singular value decomposition is given by:

$$A = USV^T = \sum_{i=1}^n \sigma_i u_i v_i^T \quad (4.6)$$

where U and V are n by n orthonormal matrices, the singular vectors u_i and v_i are the columns of the matrices U and V respectively, and S is a diagonal matrix with:

$$S(A)=diag\{\sigma_i(A)\} \quad i=1, 2, 3,\dots,n \quad (4.7)$$

where $\sigma_i \geq 0$ for all i . The diagonal elements in the matrix S are usually ordered so that; $\sigma_1 \geq \sigma_2 \geq \dots \geq \sigma_n \geq 0$. If the matrix A has rank r ($r \leq n$) its singular values are the square roots of the r positive eigenvalues of $A^T A$, which also are the r positive eigenvalues of AA^T . These square roots $\sigma_1, \sigma_2, \dots, \sigma_r$ are the only nonzero entries in the n by n diagonal matrix S . U and V are orthonormal matrices of the order n , and their columns contains the eigenvectors of $A^T A$ and AA^T respectively. If this is the case then σ_i is the i^{th} singular value of A , the vector u_i is the i^{th} left singular vector and the vector v_i is the i^{th} right vector.

To use the above theory on power system analysis a linearised relation between the active and reactive powers at nodes versus the voltage magnitudes and node angles has to be found, which is established by with the power flow Jacobian matrix as:

$$\begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} = \begin{bmatrix} J_{P\theta} & J_{PV} \\ J_{Q\theta} & J_{QV} \end{bmatrix} \begin{bmatrix} \Delta \theta \\ \Delta V \end{bmatrix} = [J] \begin{bmatrix} \Delta \theta \\ \Delta V \end{bmatrix} \quad (4.8)$$

The Jacobian matrix J , in equation 4.8, thus contains the first derivatives of the active power part F , and the reactive power part G , of the power system flow equations with respect to voltage magnitudes V and node angle θ .

If the singular value decomposition [6] is applied to the Jacobian matrix J , the obtained matrix decomposition can be written as:

$$J = USV^T \quad (4.9)$$

The minimum singular value, $\sigma_n(J)$ is a measure of how close to singularity the power system flow Jacobian matrix is. If the minimum singular value is equal to zero, the

studied matrix is singular and no power flow solution exists. The singularity of the Jacobian matrix corresponds to that the inverse of the matrix does not exist. This can be interpreted as an infinite sensitivity of the power flow solution to small perturbations in the parameters values. At the point where $\sigma_n(J)=0$ several branches of equilibria may come together and the studied system will experience a qualitative change in the structure of the solutions due to a small change in parameter values. This point called a static bifurcation point of the power system [7].

The effect on the $\begin{bmatrix} \Delta\theta & \Delta V \end{bmatrix}^T$ vector of a small change in the active and reactive power injection, according to the above theory of singular value decomposition of matrices, can be computed as:

$$\begin{bmatrix} \Delta\theta \\ \Delta V \end{bmatrix} = VS^{-1}U^T \begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} \quad (4.10)$$

The inverse of the minimum singular value σ_i^{-1} will be, thus, from a small signal disturbance point of view, indicating the largest change in the state variables. Let:

$$\begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} = u_n \quad (4.11)$$

where u_n is the last column of U , then?

$$\begin{bmatrix} \Delta\theta \\ \Delta V \end{bmatrix} = \sigma_n^{-1}v_n \quad (4.12)$$

where v_n is the last column of V . From equations 4.11, 4.12 and discussion about singular value decomposition of the power flow Jacobian matrix, the following interpretations can be made for the minimum singular value and the corresponding left and right singular vectors.

- The smallest singular value of σ_n is an indicator of the proximity to the steady state stability limit.
- The right singular vector v_n corresponding to σ_n indicates sensitive voltages (and angles).
- The left singular vector u_n corresponding to σ_n indicates the most sensitive direction for changes of active and reactive power injections.

Another property of singular value decomposition which could be worth noticing is that by adding a column to the studied matrix, the largest singular value will increase and the smallest singular value will diminish [9]. The size of the power flow Jacobian matrix will increase with one row and one column each time a generator node (P - V node) hits its limitation for reactive power capability and changes into a P - Q node.

4.4 Voltage stability analysis based on a multi-variable control technique

By a multi-variable technique we mean a process with several inputs and several outputs as shown in Figure 4.1. In general, every input is connected to every output through some dynamic coupling. We can assume that the i^{th} output y_i is connected to the j^{th} input u_j through a transfer function $g_{ij}(s)$, we can write:

$$y_i(s) = \sum_{j=1}^r g_{ij}(s)u_j(s) \quad (4.13)$$

or

$$\begin{bmatrix} y_1(s) \\ u_i(s) \\ \vdots \\ y_m(s) \end{bmatrix} = g_{ij}(s) \begin{bmatrix} u_1(s) \\ u_i(s) \\ \vdots \\ u_r(s) \end{bmatrix} \quad (4.14)$$

where the notation $(g_{ij}(s))$ indicates the transfer function matrix, that is:

$$g_{ij}(s) = \begin{bmatrix} g_{ij}(s) & \cdots & g_{ir}(s) \\ \vdots & \vdots & \vdots \\ g_{mj}(s) & \cdots & g_{mr}(s) \end{bmatrix} \quad (4.15)$$



Figure 4.1 A multi-variable technique: a system with r inputs and m outputs [10]

In this section, voltage dynamic stability analysis based on the Multi-Input Multi-Output (MIMO) transfer technique is carried out. Figure 4.2 shows the MIMO system which is widely used in control engineering. The requirement for this analysis is a detailed dynamic power system model including generators, governors, static exciter, power system stabilizer, non-linear voltage and frequency load models is necessary. Furthermore, dynamic load models may also be included. In general, the dynamic models described by Equation 4.1 and Equation 4.2 must consider all the factors affecting voltage stability.

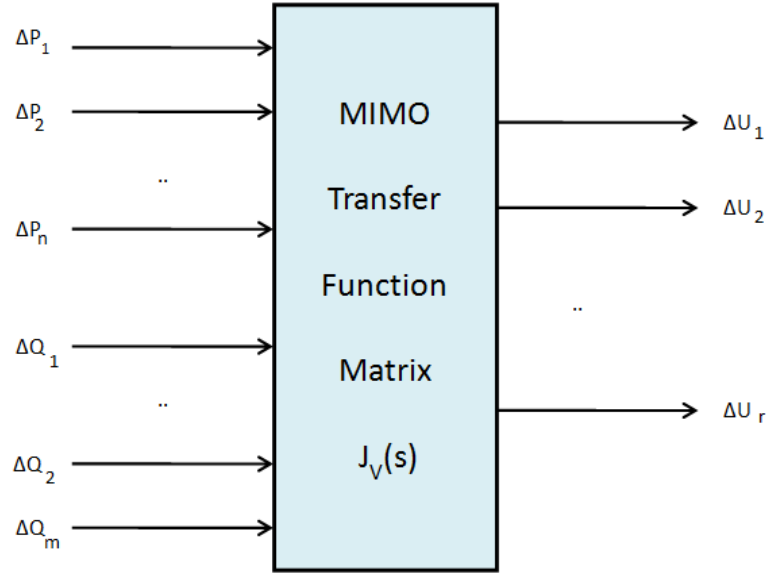


Figure 4.2 Multi-Input Multi-Output (MIMO) for small signal stability modeling

At the first step, variables that are affecting dynamic voltage stability must be selected as input variables to the MIMO system. These are usually the real and reactive power controls of selected generators and loads. Some other variables, such as the tap-changer position and FACTS control signals, can also be included as inputs. The voltage magnitudes at the most critical nodes are considered as output signals. In this thesis, a MIMO system transfer function matrix is employed by using all the generation and load controls as the input signals. Also, the set output signals are extended to all bus voltages due to the small size of the simulated power system model. The transfer function $J_v(s)$ that corresponds to MIMO model shown in Figure 4.2 is described by Equation 4.17:

$$\begin{bmatrix} \Delta U_1 & \Delta U_2 & \cdots & \Delta U_n \end{bmatrix}^T = J_v(s) * \begin{bmatrix} \Delta P_1 & \Delta P_2 & \cdots & \Delta P_n & \vdots & \Delta Q_1 & \Delta Q_2 & \cdots & \Delta Q_n \end{bmatrix}^T \quad (4.16)$$

where

$$J_v(s) = \begin{bmatrix} f_{p1_U1}(s) & \dots & f_{pn_U1}(s) & f_{Q1_U1}(s) & \dots & f_{Qn_U1}(s) \\ f_{p1_U2}(s) & \dots & f_{pn_U2}(s) & f_{Q1_U2}(s) & \dots & f_{Qn_U2}(s) \\ \vdots & & \vdots & \vdots & & \vdots \\ f_{p1_Un}(s) & \dots & f_{pn_Un}(s) & f_{Q1_Un}(s) & \dots & f_{Qn_U2}(s) \end{bmatrix} \quad (4.17)$$

$J_v(s)$ is a $n_{output} * n_{input}$ transfer function matrix.

To obtain each sub-transfer function in the $J_v(s)$ numerical methods can be applied to the power system dynamic model.

In order to analyse the MIMO system, SVD of $J_v(s)$ is carried out at every fixed frequency [6, 9, 10]:

$$J_v(s) = USV^T \quad (4.18)$$

where

S an n_{output} by n_{output} matrix with $k = \min \{ n_{output}, n_{input} \}$ non-negative singular values, σ_i are arranged in descending order along its main diagonal; the other entries are zero. The singular values are the positive square roots of the eigenvalue of $J_v^T(s) * J_v(s)$, where $J_v^T(s)$ is the complex conjugate transpose of $J_v(s)$ [10]:

$$\sigma_i(J_v(s)) = \sqrt{\lambda_i(J_v^T(s) * J_v(s))} \quad (4.19)$$

where U is an n_{output} by n_{output} unitary matrix of output singular vectors, u_i and V is an n_{input} by n_{input} unitary matrix of input singular vectors, v_i .

The column vectors of U , denoted u_i , represent the directions of the output variables.

They are orthogonal and of unit length. Likewise, the column vectors of V , denote v_i ,

represent the directions of input variables. These input and output directions are related through the singular values [10, 11].

For dynamic stability, the singular values and their associated directions vary with the frequency. In power system dynamic voltage stability analysis, critical frequencies corresponding to poorly damp dominant modes must be considered.

By analysing the maximum singular values and their associated related input and output singular vectors, the relationship between input and output can be obtained at each frequency. The output singular vector shows which bus voltage magnitude is the most critical bus. The input singular vectors indicate which input has the greatest influence on the corresponding output. Therefore, by means of the singular value analysis, the dynamic voltage stability can be performed.

4.5 Effect of Load Modelling

Normally, power system stability was often regarded as a problem of generators and their controls, while the effect of loads was considered as a secondary factor. The load representation can play an important factor in the power system stability. The effects of load characteristics on power system stability have been studied. Many of research results showed that the load characteristics affect the behaviour of the power system.

The load characteristics can be divided into two categories; static characteristics and dynamic characteristics. The effect of the static characteristics is discussed in chapter 3. Recently, the load representation has become more important in power system stability studies [12, 13]. In the previous analysis, the load was represented by considering the active power and reactive power and both were represented by a combination of constant impedance (resistance, R or reactance, X), constant current, I and constant

power (active, P or reactive, Q) elements. This kind of load modelling has been used in many of the power system steady state analyses. However the load may be modelled as a function of voltage and frequency depending on the type of study. On the other hand, there is no single load model that leads to conservative design for all system configurations [14].

Dynamic load models whose active power P and reactive power Q vary as functions of positive-sequence voltage. Negative- and zero-sequence currents are not simulated. The effect of the dynamic load modelling on voltage stability is presented in this section. A voltage dependent load model is studied. A significant change in the stability limit or distance to voltage collapse should be noticed clearly.

4.5.1 Voltage Dependent Load.

Voltage dependency of reactive power affects the stability of power system. This effect primarily appears on voltages, which in turn affects the active power. It is well known that the stability improves and the system becomes voltage stable by installing static reactive power compensators or synchronous condensers [15]. The active and reactive dynamic load model for a particular load bus is an exponent function of the per unit bus voltage as shown in the following equations:

$$P_k = P_0 \left(\frac{V}{V_0} \right)^{np} * (1 + T_{p1} * s) / (1 + T_{P2} * s) \quad (4.20)$$

$$Q_k = Q_0 \left(\frac{V}{V_0} \right)^{nq} * (1 + T_{q1} * s) / (1 + T_{q2} * s) \quad (4.21)$$

where:

V_0 is the initial positive sequence voltage.

P_0 and Q_0 are the initial active and reactive powers at the initial voltage V_0 .

V is the positive-sequence voltage.

n_p and n_q are exponents (usually between 1 and 3) controlling the nature of the load.

T_{p1} and T_{p2} are time constants controlling the dynamics of the active power P .

T_{q1} and T_{q2} are time constants controlling the dynamics of the reactive power Q .

Then the load flow presented in Equation (3.6) at load bus k can be written as:

$$0 = P_0 * \left(\frac{V}{V_0} \right)^{np} * (1 + T_{P1}s) / (1 + T_{P2}s) + \sum_{m=1}^n Y_{km} V_m V_m \cos(\theta_k - \theta_m - \gamma_{km}) \quad (4.22)$$

$$0 = Q_0 * \left(\frac{V}{V_0} \right)^{nq} * (1 + T_{q1}s) / (1 + T_{q2}s) + \sum_{m=1}^n Y_{km} V_m V_m \sin(\theta_k - \theta_m - \gamma_{km}) \quad (4.23)$$

Equation 4.8 and Equation 4.9 will update the load equations in the load flow, then, the nonlinear equations will be solved to obtain a new load flow solutions. A load flow MATLAB based program is developed to include the dynamic load model.

In the following sections, the singular value decomposition techniques were applied to the reduced Jacobian matrix which is corresponding to the transfer matrix of the MIMO system in order to determine the maximum singular value and the critical modes of oscillations were identified. After that, the magnitudes of the output and input singular vectors that relate the critical buses and the most suitable control action were calculated.

Finally, the effects of dynamic load model on these modes were studied. Results are presented and discussed.

4.6 Test system description

The detailed model of the WSCC 3-machines, 9-bus test system shown in Figure 3.8 is used to demonstrate the singular value decomposition methods applied to the MIMO system to identify the weakest bus. The corresponding power system dynamic model consists of generators described by 6th order model, governors, static exciters, Power System Stabilizer (PSS) and non-linear voltage and frequency dependent loads. The detailed generator, controller and load model can be found in [1, 15-16].

4.6.1 Weak bus identification based on singular value technique

Based on the detailed dynamic power system model, the maximum singular value of reduced Jacobian matrix that provide the maximal gain between the input and output variables is calculated. It describes how the observed outputs can be influenced by the inputs [5]. Figure 4.3 shows the maximal singular value of the reduced Jacobian matrix J_R over the frequency range of [0.1 Hz to 10 Hz]. It is clear from the figure that the peaks of the maximal singular value plot correspond to the inter-area mode and exciter mode 1 respectively (The exciter mode 1 and inter-area mode are determined using the modal analysis). Based on this result, the singular value is generated for the two critical oscillation mode frequencies i.e. exciter mode and inter-area mode.

4.6.1.1 Exciter Mode

The control/exciter mode is directly related to the control equipment of the generator and is a version of the local oscillation mode. The exciter mode has frequencies ranging from 0.7 to 3.0 Hz [1]. These oscillations could be a result of poorly coordinated

regulators in the system such as excitation systems, HVDC converters, and static VAR compensators. As a result of these oscillations the generator shaft may be affected and the torsion mode will then be more noticeable [1].

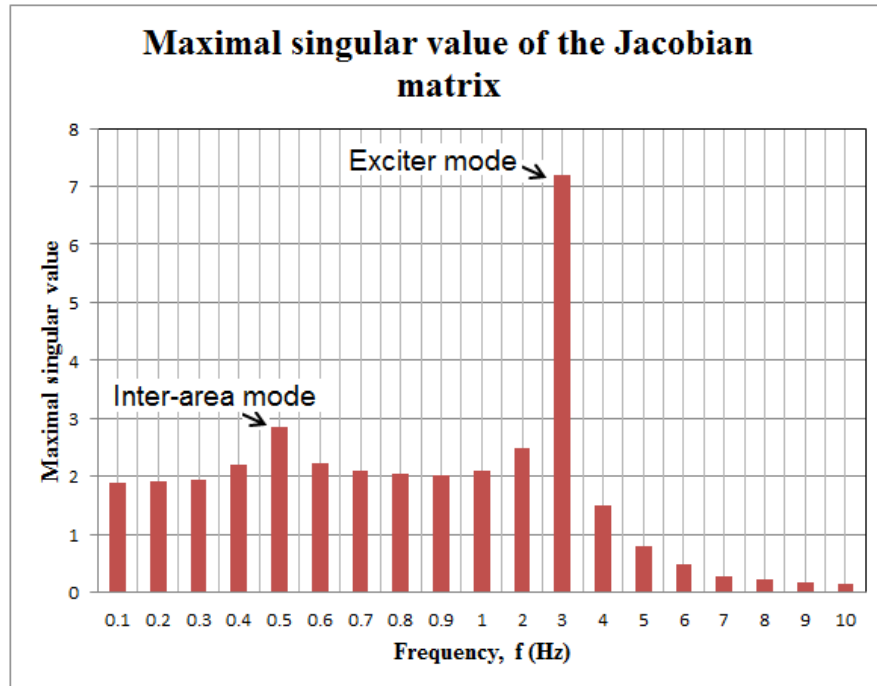


Figure 4.3 Plot of maximal singular value vs frequency

The singular value decomposition and their associated input and output singular vectors applied to modal analysis are used to identify the most critical bus and the most suitable signals for dynamic stability analysis.

The results of singular value analysis show that the output singular vectors that correspond to the maximum singular value at the exciter mode frequency are given in Figure 4.4. It can be seen that the buses 5, 6, and 8 are related to the dynamic voltage stability with bus 8 standing out as the most critical bus. The analysis of the input singular vector associated with this mode shows that the input signals of Q_2 , Q_3 , and Q_1 (input number 16, 17 and 18) are the most suitable signals for this mode of dynamic voltage stability control. The other input signals have relatively weak influences as can be seen in Figure 4.5.

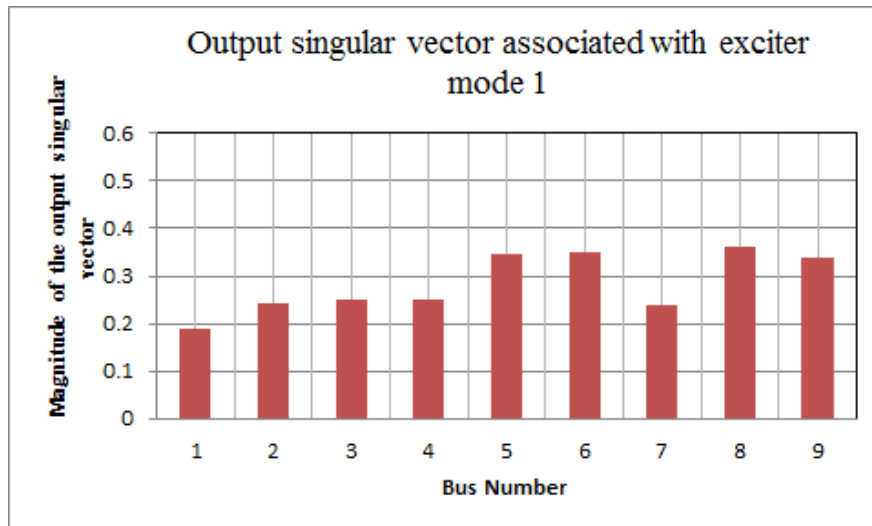


Figure 4.4 Plot mode of magnitude of the output singular vector vs bus number

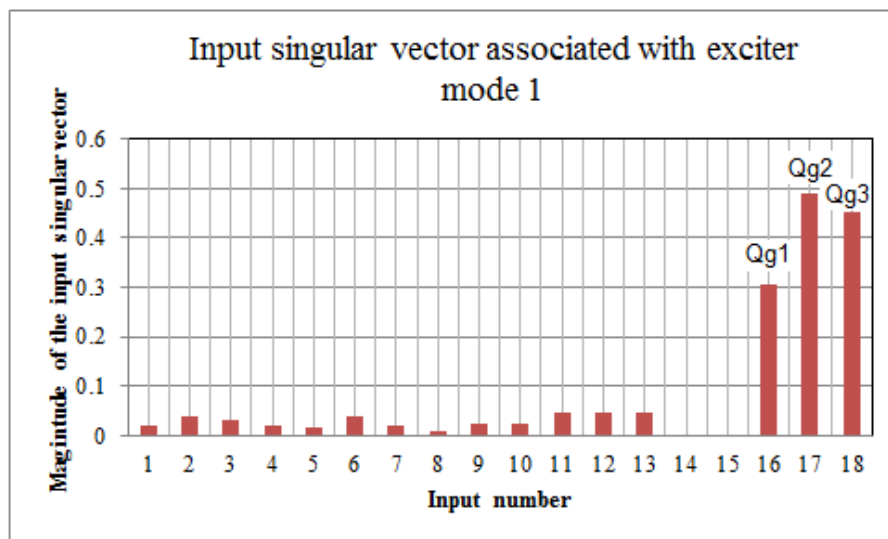


Figure 4.5 Plot of input singular vector associated with exciter mode 1

4.6.1.2 Inter-area Mode

The inter-area oscillation mode can be seen in a large part of a network where one part of the system oscillates against other parts at a frequency below 0.5 Hz. Since there is a large number of generating units involved in these oscillations, the network operators must cooperate, tune and implement applications that will damp this mode of oscillation. A PSS is often a good application to provide positive damping of the inter-

area modes [19]. Also a higher frequency inter-area oscillation can appear (from 0.4 to 0.7 Hz) when side groups of generating units oscillate against each other [1].

Figure 4.6 shows the critical output singular vector associated with the inter-area mode oscillation mode. From the figure, it is clear that bus 8 is the most critical bus. In comparison with exciter mode 1, the inter-area mode has larger output singular vectors.

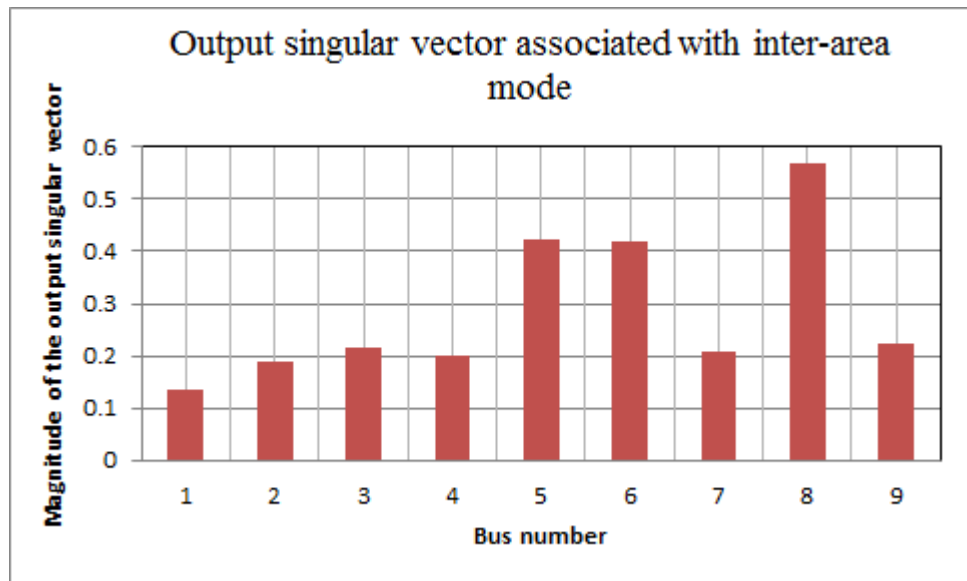


Figure 4.6 Plot of magnitude of the output singular vector vs bus number

The analysis of the input singular vector associated with inter-area mode is shown in Figure 4.7 it is clear that the input signal of Q_2 , Q_3 and Q_1 are the most suitable signals for dynamic stability analysis and control (input number 16, 17 and 18).

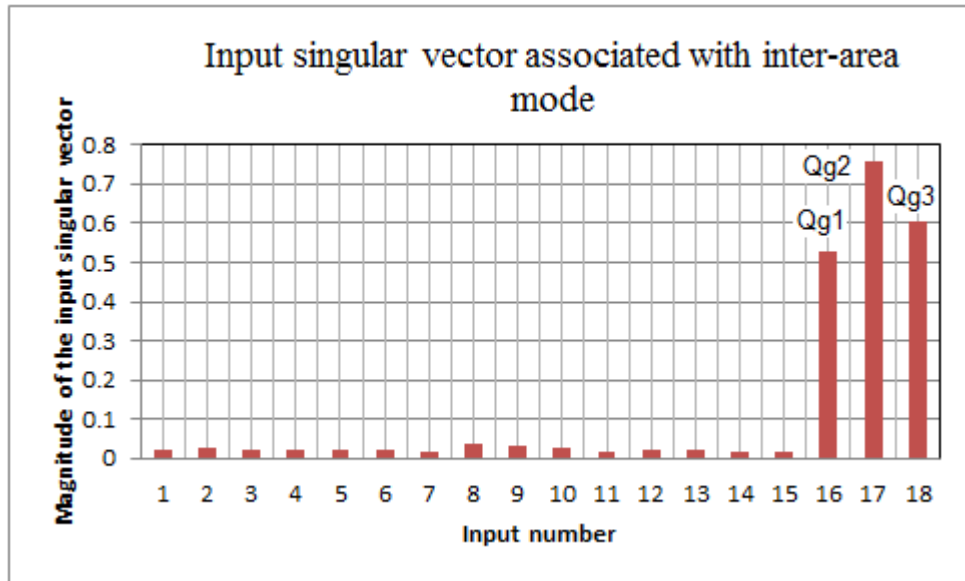


Figure 4.7 Plot of magnitude input singular vector vs input number

The simulation result shown in Figures 4.4-7, identifies the weakest bus in the test system and suitable control action should be taken. The results show that bus 8 is the weakest bus in the test system, and the results agree with results obtained by Q-V curves and those obtained by the proposed static voltage stability index and with results obtained by other indices.

4.6.2 Analysis considering the effect of load characteristics.

Singular value decomposition including load characteristics is performed for the test system. Different voltage dependent load models can be implemented by changing the n_p and n_q values in Equations (4.20) and (4.21). The singular value is performed from the two critical modes of frequencies. Then, voltage profile of the buses is then presented from the load flow solution. After that, the Q-V curves are generated for selected buses in order to monitor the voltage stability margin. The results are shown in Figure 4.8 to Figure 4.14.

4.6.2.1 Exciter mode

The simulation results shown in Figure 4.8 show the output singular vectors that correspond to the maximum singular value at the exciter mode for different load characteristics ($n_p = n_q = 1, 2$ and 3 respectively). In general, the results show that, buses 5, 6 and 8 have the highest singular value to the critical mode, which is similar as obtained before. The largest output singular value at bus 8 indicates a high contribution of this bus to the voltage collapse. There is an insignificant change in the magnitude of the output singular vector but this change does not change the position of the critical mode.

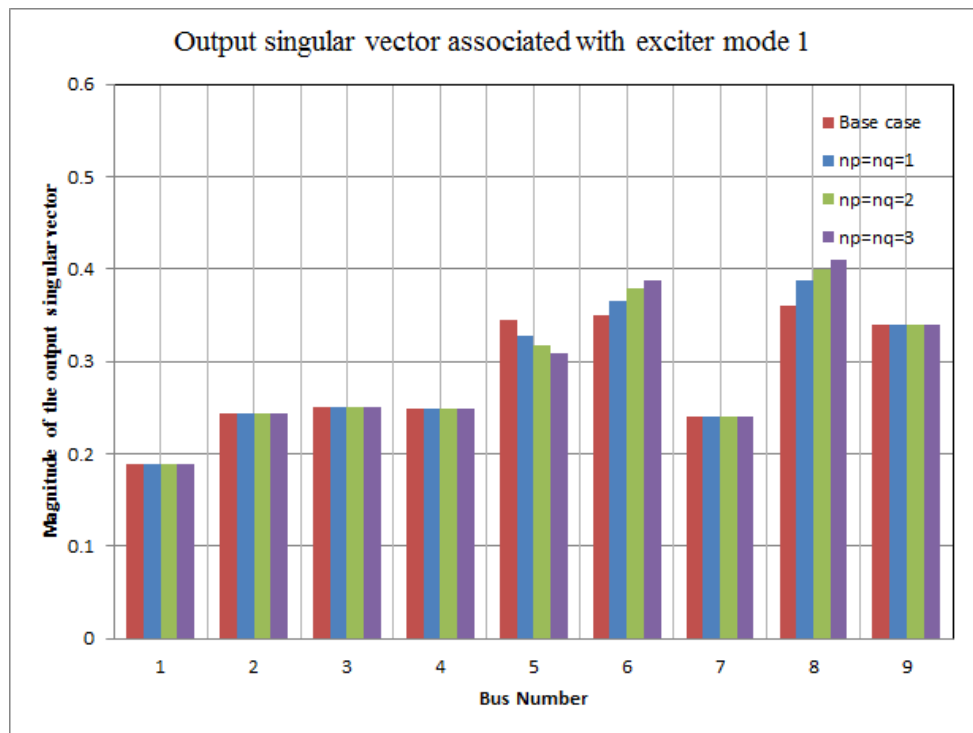


Figure 4.8 Plot mode of magnitude of the output singular vector vs bus number at different load characteristics

In Figure 4.9, the magnitude of the input singular vector associated with this mode is presented. The simulation results show that there is also a slight change in the

magnitude of the input singular vector due to the load characteristics and still the input numbers 16, 17 and 18 are the most suitable signals for this mode.

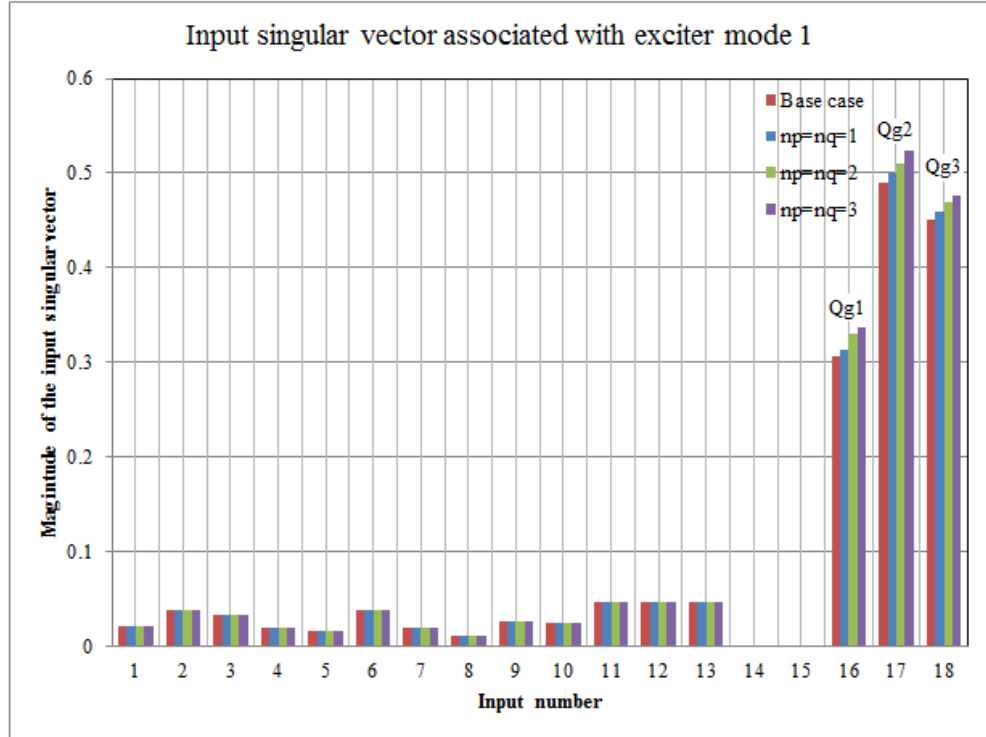


Figure 4.9 Plot of input singular vector associated with exciter mode 1 at different load characteristics

4.6.2.2 Inter-area mode

The effect of load model on the magnitude of the output singular vector associated with the inter-area mode is given in Figure 7.10. Also, there is an insignificant change in the magnitude of the output singular vector due to the change in load characteristics. There is no change in the critical mode position due to load changes and bus 8 is the most critical bus.

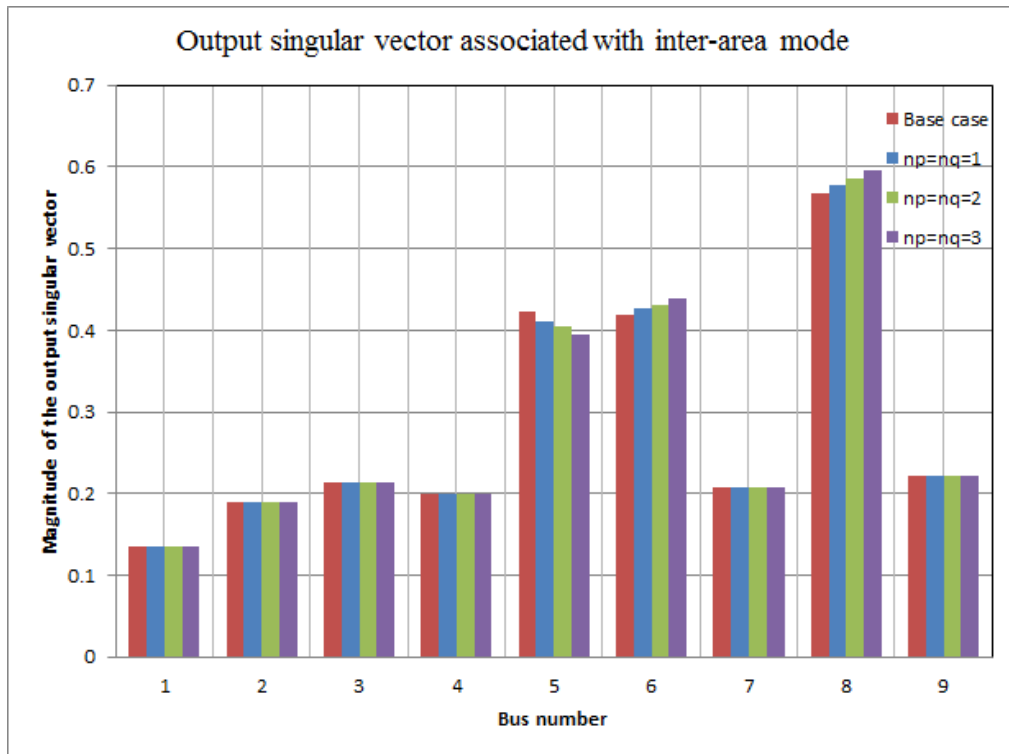


Figure 4.10 Plot of magnitude of the output singular vector vs bus number with different load characteristics

Figure 4.11 shows the magnitude of the input singular vector due to changes in the load model. From the results, there is no change in the position of the input signal that is suitable for dynamic stability analysis. Although, there is insignificant change in the magnitude of the input signal but this does not change the position of critical nodes.

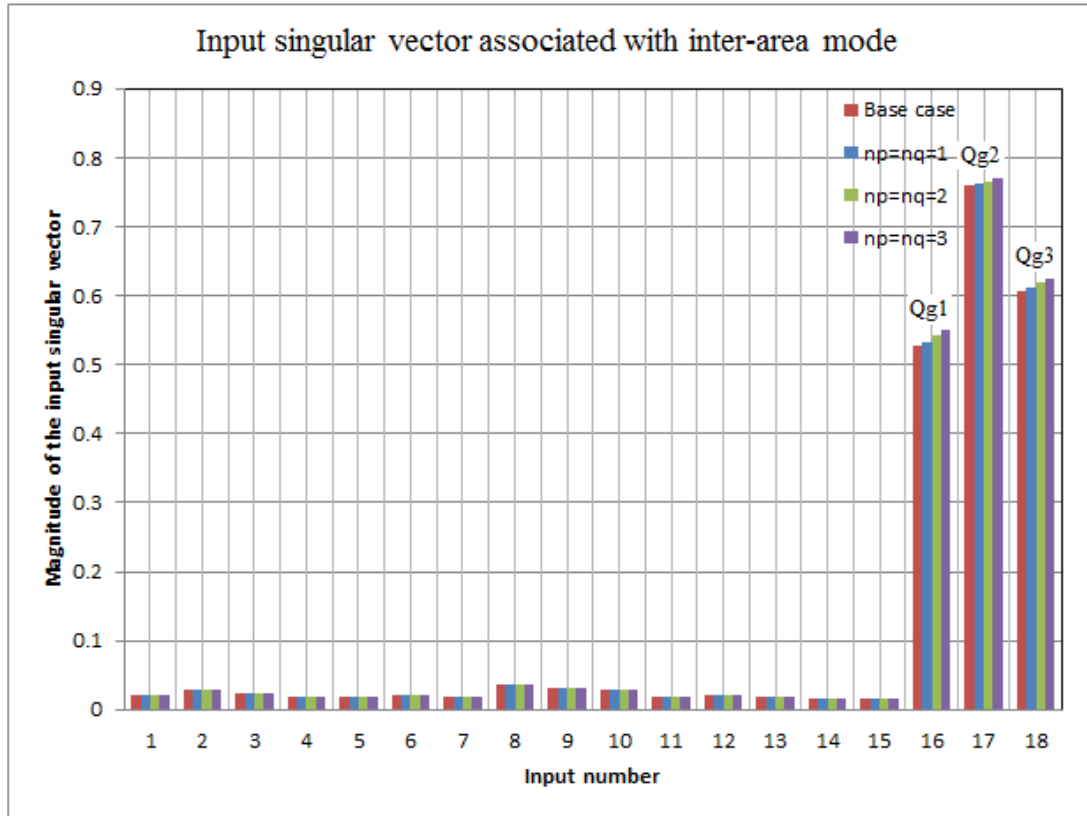


Figure 4.11 Plot of magnitude input singular vector vs input number with different load characteristics

The simulation results shown in Figure 4.12 show the voltage profiles of all buses of the test system as obtained from the load flow by changing the n_p and n_q values in Equations (4.20) and (4.21). The result shows four types of nonlinear loads, including the base case and three different voltage dependent loads ($n_p = n_q = 1, 2$ and 3 respectively). The simulation results show that all the bus voltages are within the acceptable level (± 10). Also, it can be noticed that the lowest voltage in all cases compared to the other buses is at bus 8.

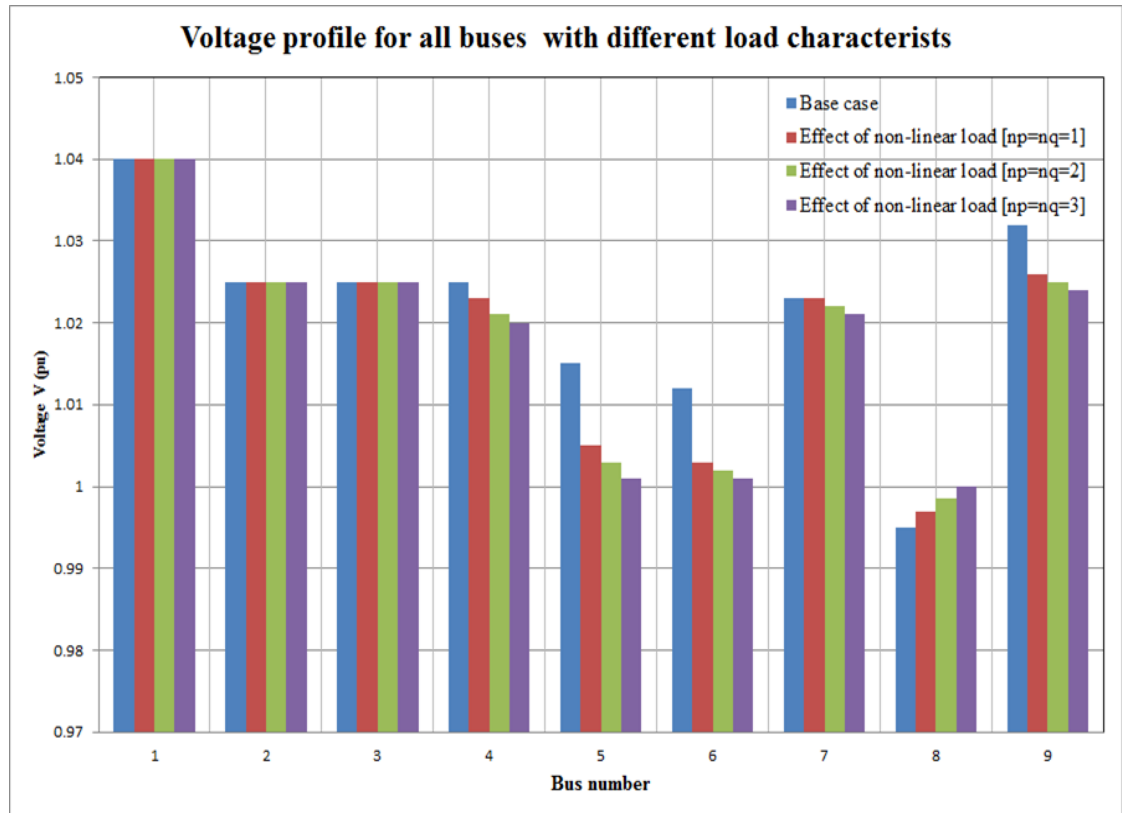


Figure 4.12 Voltage profiles of all buses of the test system at different load models

The Q-V curves were generated for the weakest buses, bus 5 and bus 8, of the critical mode in the test system as expected by the singular value decomposition method at different voltage dependent load models. The curves are shown in Figure 4.13 and Figure 4.14.

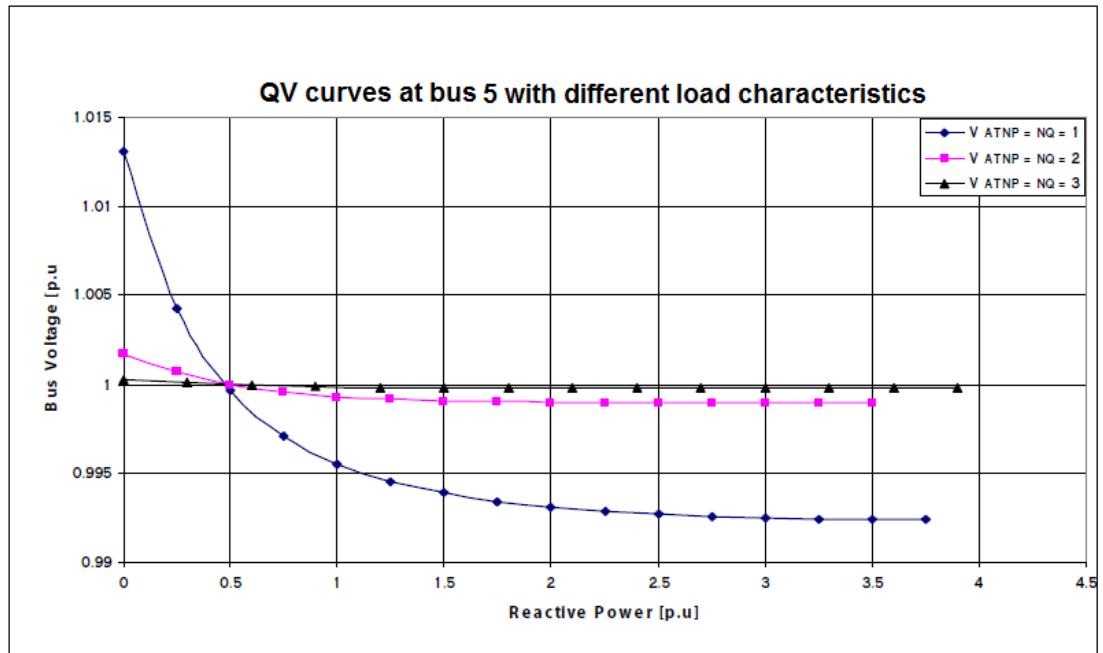


Figure 4.13 The Q-V curves at bus 5 for the test system at different load models

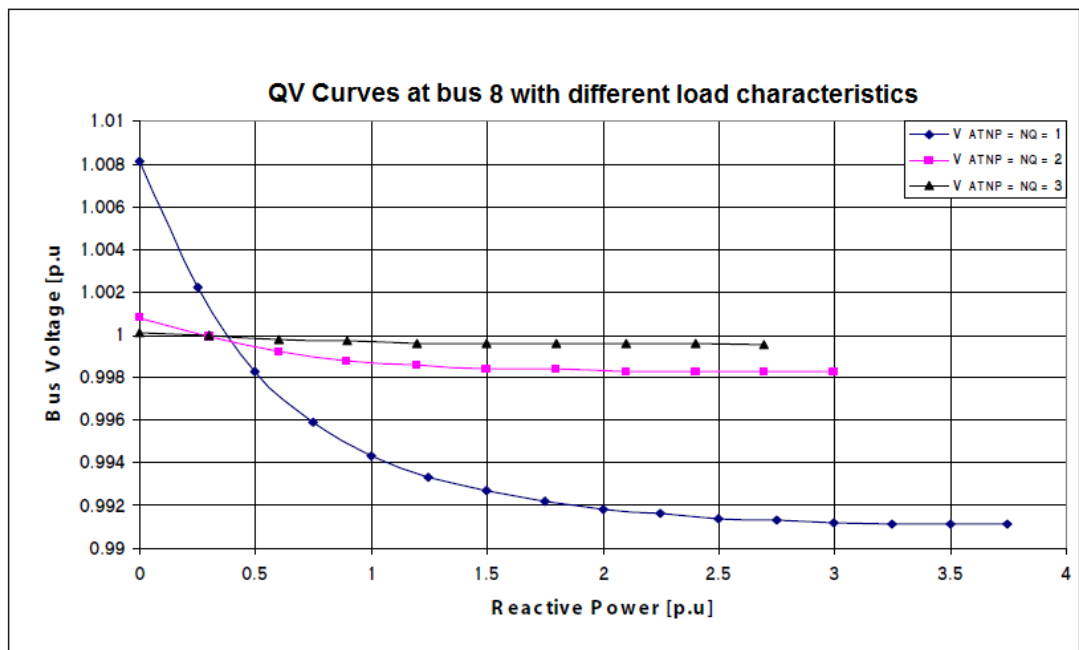


Figure 4.14 The Q-V curves at bus 8 for the test system at different load models

Table 4.1 and Table 4.2, show the reactive power and voltage stability margins calculated based on the Q-V curves for the weakest bus 5 and bus 8.

Table 4.1 Voltage and reactive power stability margins for the test system for bus 5.

Operating point		Static stability				np=nq=1				np=nq=2				np=nq=3			
		Max. withstand		Stab. margin		Max. withstand		Stab. margin		Max. withstand		Stab. margin		Max. withstand		Stab. margin	
V	Q	V	Q	ΔV	ΔQ	V	Q	ΔV	ΔQ	V	Q	ΔV	ΔQ	V	Q	ΔV	ΔQ
1.0	0.3	0.63	2.85	0.37	2.55	0.9924	3.75	0.01	3.45	0.999	3.5	0.001	3.2	0.999	3.9	0.0002	3.6

Table 4.2 Voltage and reactive power stability margins for the test system for bus 8.

Operating point		Static stability				np=nq=1				np=nq=2				np=nq=3			
		Max. withstand		Stab. margin		Max. withstand		Stab. margin		Max. withstand		Stab. margin		Max. withstand		Stab. margin	
V	Q	V	Q	ΔV	ΔQ	V	Q	ΔV	ΔQ	V	Q	ΔV	ΔQ	V	Q	ΔV	ΔQ
1.0	0.5	0.72	2.625	0.28	2.125	0.9910	3.75	0.009	3.25	0.998	3.0	0.002	2.5	0.999	2.7	0.001	2.2

From the reactive power and voltage stability margins shown in Table 4.1 and Table 4.2, the voltage dependent load model affected the stability margin. However, these models did not change the location of the weakest buses allocated by static stability analysis presented in previous chapter. On the other hand a noticed change in the voltage level as well as in the distance to voltage collapse appeared clearly. The voltage level improved by increasing the value of np and nq, while the distance to voltage collapse increased as the value of np and nq increased.

4.7 Summary

This chapter introduced a new method for dynamic voltage stability studies. The method is based on the MIMO transfer function. Interactions between properly defined input and output variables affecting the dynamic voltage stability are analysed based on the singular value decomposition at different frequencies. The elements of the input singular vectors indicate the impact of the input variables on the output variables, and the output singular vectors can be used to evaluate the influence of voltage stability on the selected buses. Moreover, the input singular vector can be used for choosing the most suitable control action to improve voltage stability and the output singular vector can provide information about the weakest buses that are affected by voltage stability. A typical WSCC 3-machine, 9-bus test power system is used to validate this technique and the results were presented. The simulation results show that the application of singular value decomposition and their associated output and input singular vectors based on the MIMO transfer function identify the critical modes (weakest buses) of the test system and the suitable control action (compensation) to prevent the test system from voltage collapse. The most suitable position for control action is the weakest bus; FACTS controller can offer greater control power system, improve voltage stability and increase power transfer capability. The results agree with that obtained by static voltage stability analysis (LSZ and modal analysis). These results help operators and planners to know the maximum reactive power that can be achieved or added to the weakest bus before reaching minimum voltage limit or voltage instability

The effect of the dynamic load on critical modes and voltage stability margin were also studied. The results shows that there is an effect of the dynamic load model on the critical mode and voltage stability margin but these effects did not change the position

of the critical mode (weakest buses) and their associated control signals. In addition, a noticeable change in the voltage level appeared clearly.

The method is highly accurate and suitable for dynamic stability analysis; it can also be applied to large power systems.

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5: UNIFIED POWER FLOW CONTROLLER

5.1 Introduction

In the previous two chapters, studies have been described which identify the weakest bus which is prone to voltage collapse in power systems, based on static and dynamic criteria. In order to prevent that bus from voltage collapse, suitable control action should be taken. A FACTS controller can play an important role in mitigating voltage stability problems and power transfer capability. In this chapter, the different categories of FACTS controller based on their connection in the network are presented. Then, the steady state operation of the most common FACTS controller (i.e. UPFC) is investigated. After that, the steady state operation of the UPFC when connected to the weakest bus of the WSCC 3-machine, 9-bus test system is discussed.

5.2 Flexible AC Transmission Systems

The FACTS initiative [1-10] was originally launched in the 1980s to solve the emerging problems faced due to restrictions on transmission line construction, and to facilitate growing power export/import and wheeling transactions among utilities. The two basic objectives behind the development of FACTS technology are to increase the power transfer capability of transmission systems, and to keep the power flowing over designated routes, therefore significantly increasing the utilization of existing (and new) transmission assets. This plays a major role in facilitating contractual power flow in electricity markets with minimal requirements for new transmission lines.

Injecting a series voltage phasor, with a desirable voltage magnitude and phase angle in a line, can provide a powerful means of precisely controlling the active and reactive

power flows, by which, system stability can be improved, system reliability can be enhanced while operating and transmission investment cost can be reduced. It is possible to vary the impedance of a specific transmission line to force power flow along a desired “contract path” in the emerging power systems, to regulate the unwanted loop power flows and parallel power flows in the interconnected system. Dynamic reactive power compensation and damping power system oscillations can also be achieved using FACTS controllers. In general, FACTS controllers can be divided into four categories based on their connection in the network as follows;

- Series Controllers.
- Shunt Controllers.
- Combined Series-Series Controllers.
- Combined Series-Shunt Controllers.

5.2.1 Series controllers

Series controller can be switched impedance, such as capacitor, reactor, etc. or power electronics based variable source of main frequency, sub-synchronous and harmonic frequencies to serve the desired need. In principle, all series controllers inject voltage in series with the line. Even variable impedance, provided by some of the FACTS controllers, multiplied by the current flow through it, represents an injected series voltage in the line. A TCSC is one of the widely used series controllers. As long as the voltage is in phased quadrature with the line current, the series controller only supplies or consumes variable reactive power. Any other phase relationship will involve the handling of real power as well. A typical connection in a line, having series impedance is shown in Figure 5.1.

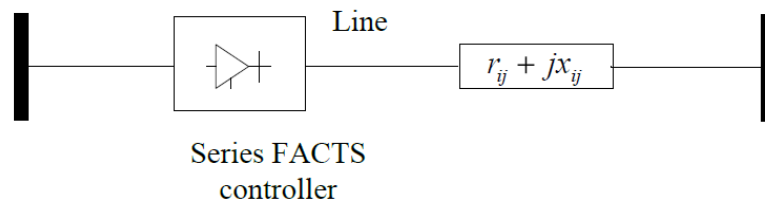


Figure 5.1: Static series FACTS controller

5.2.2 Shunt Controllers

Similar to the series controllers, the shunt controllers shown in Figure 5.2, may also be variable impedance, variable sources, or a combination of these. In principle, all shunt controllers inject the current into the system at the point of connection. SVC and STATCOM are the two most widely used shunt controllers. Even variable shunt impedance provided by shunt controller, such as SVC, cause a variable current injection into the bus/line. As long as the injected current is in phase quadrature with the bus voltage, the shunt controller only supplies or consumes variable reactive power. Any other phase relationship will involve the handling of real power as well.

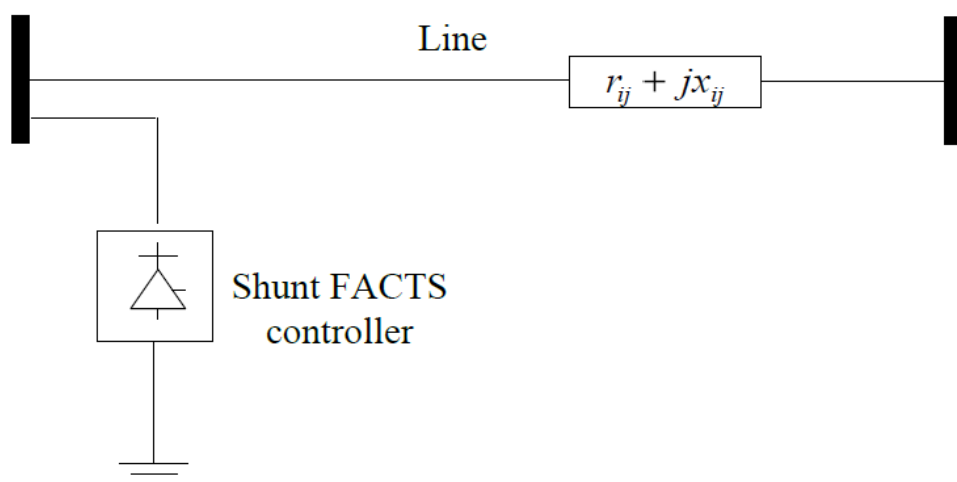


Figure 5.2 Shunt FACTS controller

5.2.3 Combined Series-Series Controllers

Combined series-series controllers can be a combination of multiple series controllers, which are controlled in a co-ordinated manner, in a multi-line transmission system. Alternatively, combined series-series controllers could be a unified controller, in which series controllers provide independent series reactive compensation for each line but also transfer real power among the lines via the power link. The real power transfer capability of the unified series-series controller, referred to as the Interline Power Flow Controller (IPFC), makes it possible to balance both the real and reactive power flow in the lines, thereby, maximizing the utilization of the transmission system. Note that the term “unified” here means that the DC terminals of the controller converters as show in the Figure 5.3 are connected together for real power transfer.

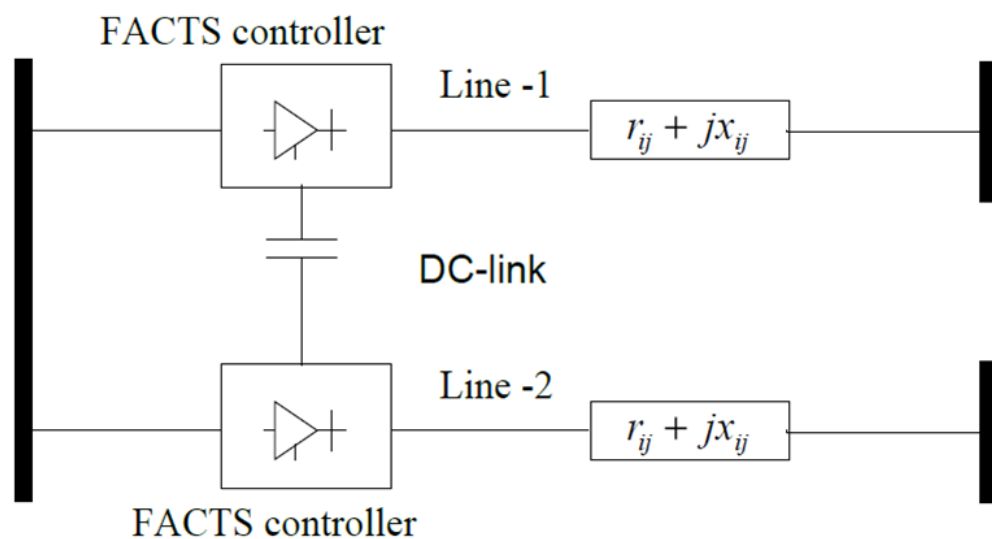


Figure 5.3: Combined series-series FACTS controller

5.2.4 Combined Series-Shunt Controllers

These could be a combination of separate shunt and series controllers, which are controlled in a co-ordinated or unified manner. The UPFC is one of the series shunt

controllers. In principle, combined shunt and series controllers inject current into the system with the shunt part of the controller and voltage in the line with the series part of the controller. However, when the shunt and series controllers are unified, there can be a real power exchange between the series and shunt controllers via a DC link as shown in Figure 5.4.

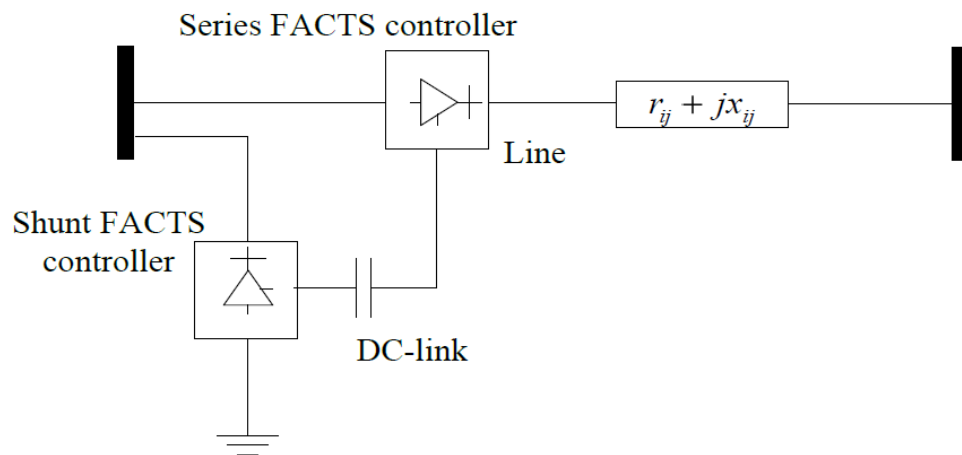


Figure 5.4 Combined series-shunt FACTS controller

UPFCs have deserved a lot of attention in the last few years [11-14]. UPFCs are able to control, simultaneously or selectively, all the parameters affecting power flow in the transmission line. Alternatively, they can independently control both the real and reactive power flow in the line, unlike any of the other controllers.

Figure 5.5 shows the general arrangement of UPFC which consists of an advanced shunt (STATic synchronous COMPensator (STATCOM)) and series (Series Static Synchronous Compensator (SSSC)) compensators connected through a common DC link. Each converter can independently generate or absorb reactive power. This configuration enables free flow of active power in either direction between the AC terminals of the two converters. The main function of the shunt converter (STATCOM) is to supply or absorb the active power ordered by the series (SSSC) branch. STATCOM shunt converter is connected to AC terminal through a shunt connected

transformer. If required, it may also generate or absorb reactive power, which can provide independent parallel reactive power compensation for the transmission line. The second series (SSSC) connected converter provides the main function of the UPFC by injecting an AC voltage with controllable magnitude and phase angle to the power network. The transmission line current flows through SSSC converter resulting in an active and reactive power exchange with the power system. The active power exchange at the AC terminal is provided by the STATCOM, with the reactive power exchange generated internally by the converter.

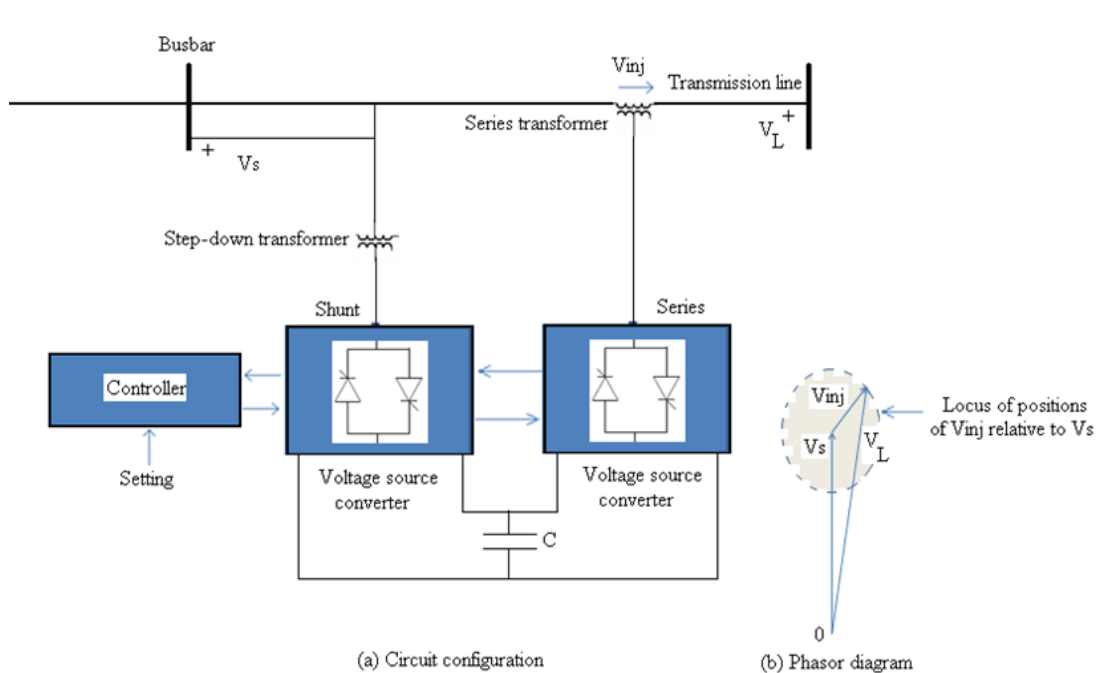


Figure 5.5 Main circuit configuration of the Unified Power Flow Controller (UPFC)

5.2.5 Control system of the UPFC connected to transmission system

The UPFC controller can control either one or a combination of the three functions as its control objective, depending on the system requirements. The UPFC operates on the following modes [15]; the series-injected voltage magnitude; the line current through series converter; the shunt-converter current; the minimum line-side voltage of the UPFC; the maximum line-side voltage of the UPFC; and the real-power transfer between the series converter and the shunt converter.

The UPFC-control design and equipment rating has got a lot of intentions and are well-explained in [16-19] and [20-22]; hence they are not described here. (not a sentence!_)

5.2.6 UPFC power flow equations

The equivalent circuit consisting of two coordinate synchronous voltage sources should represent the UPFC adequately for the purpose of fundamental frequency steady-state analysis. Such an equivalent circuit is shown in Figure 5.6. The synchronous voltage sources represent the fundamental series component of the switched voltage waveforms at the AC converter terminals [12, 13].

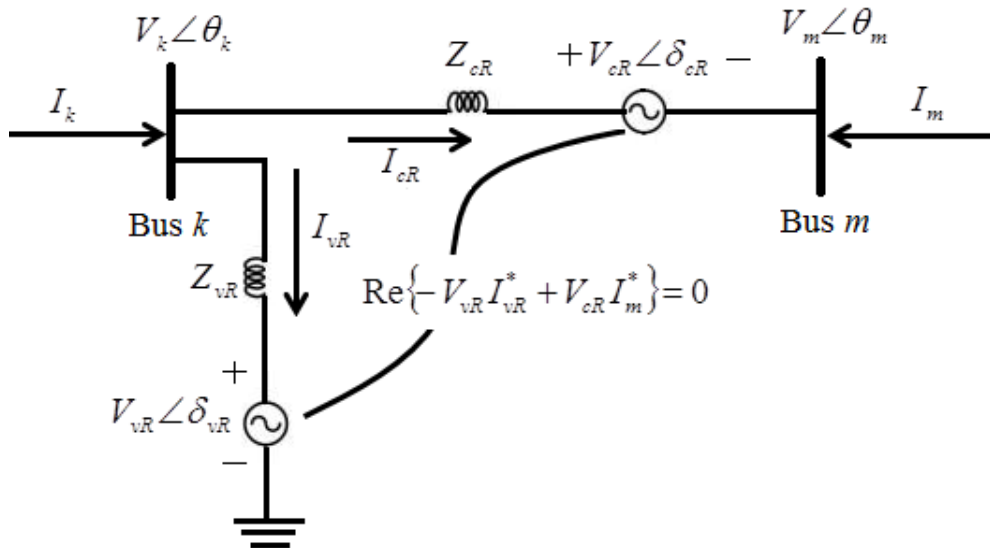


Figure 5.6 Unified power flow controller equivalent circuit

The UPFC voltage sources are:

$$E_{vR} = V_{vR} (\cos \delta_{vR} + j \sin \delta_{vR}), \quad (5.1)$$

$$E_{cR} = V_{cR} (\cos \delta_{cR} + j \sin \delta_{cR}), \quad (5.2)$$

where V_{vR} and δ_{vR} are the controllable magnitude ($V_{vR \min} \leq V_{vR} \leq V_{vR \max}$) and phase angle ($0 \leq \delta_{vR} \leq 2\pi$) of voltage source representing the shunt converter. The magnitude

V_{cR} and phase angle δ_{cR} of the voltage representing the series converter are controlled between limits ($V_{cR\ min} \leq V_{cR} \leq V_{cR\ max}$) and ($0 \leq \delta_{cR} \leq 2\pi$), respectively.

The phase angle of the series injected voltage determines the mode of power flow control. If δ_{cR} is in phase with the nodal voltage angle θ_k , the UPFC regulates the terminal voltage. If δ_{cR} is in quadrature with respect to θ_k , it controls active power flow, acting as a phase shifter. If δ_{cR} is in quadrature with the line current angle then it controls active power flow, acting as a variable series compensator. At any other value of δ_{cR} , the UPFC operates as a combination of voltage regulator, variable series compensator and phase shifter. The magnitude of the series injected voltages determines the amount of power flow to be controlled.

The transfer admittance equation for the currents can be written as:

$$\begin{bmatrix} I_k \\ I_m \end{bmatrix} = \begin{bmatrix} (Y_{cR} + Y_{vR}) & -Y_{cR} & -Y_{cR} & -Y_{vR} \\ -Y_{cR} & Y_{cR} & Y_{cR} & 0 \end{bmatrix} \begin{bmatrix} V_k \\ V_m \\ E_{cR} \\ E_{vR} \end{bmatrix} \quad (5.3)$$

in which the transfer admittance equation for the shunt converter is:

$$Y_{vR} = \begin{bmatrix} Y_{vRk}^a & 0 & 0 \\ 0 & Y_{vRk}^b & 0 \\ 0 & 0 & Y_{vRk}^c \end{bmatrix} \quad (5.4)$$

and the transfer admittance equation for the series converter is:

$$Y_{cR} = \begin{bmatrix} Y_{cRk}^a & 0 & 0 \\ 0 & Y_{cRk}^b & 0 \\ 0 & 0 & Y_{cRk}^c \end{bmatrix} \quad (5.5)$$

where a , b and c in Equation 5.4 and Equation 5.5 indicates phase quantities.

Based on the equivalent circuit shown in Figure 5.6 and Equations 5.1 and Equation 5.2, the active and reactive power equations are [14, 15];

At bus k :

$$\begin{aligned} P_k &= V_k^2 G_{kk} + V_k V_m [G_{km} \cos(\theta_k - \theta_m) + B_{km} \sin(\theta_k - \theta_m)] \\ &+ V_k V_{cR} [G_{km} \cos(\theta_k - \delta_{cR}) + B_{km} \sin(\theta_k - \delta_{cR})] \\ &+ V_k V_{vR} [G_{vR} \cos(\theta_k - \delta_{vR}) + B_{vR} \sin(\theta_k - \delta_{vR})] \end{aligned} \quad (5.6)$$

$$\begin{aligned} Q_k &= -V_k^2 B_{kk} + V_k V_m [G_{km} \sin(\theta_k - \theta_m) - B_{km} \cos(\theta_k - \theta_m)] \\ &+ V_k V_{cR} [G_{km} \sin(\theta_k - \delta_{cR}) - B_{km} \cos(\theta_k - \delta_{cR})] \\ &+ V_k V_{vR} [G_{vR} \sin(\theta_k - \delta_{vR}) - B_{vR} \cos(\theta_k - \delta_{vR})] \end{aligned} \quad (5.7)$$

At bus m :

$$\begin{aligned} P_m &= V_m^2 G_{mm} + V_m V_k [G_{mk} \cos(\theta_m - \theta_k) + B_{mk} \sin(\theta_m - \theta_k)] \\ &+ V_m V_{cR} [G_{mm} \cos(\theta_m - \delta_{cR}) + B_{mm} \sin(\theta_m - \delta_{cR})] \end{aligned} \quad (5.8)$$

$$\begin{aligned} Q_m &= -V_m^2 B_{mm} + V_m V_k [G_{mk} \sin(\theta_m - \theta_k) - B_{mk} \cos(\theta_m - \theta_k)] \\ &+ V_m V_{cR} [G_{mm} \sin(\theta_m - \delta_{cR}) - B_{mm} \cos(\theta_m - \delta_{cR})] \end{aligned} \quad (5.9)$$

The active and reactive powers at the series converter are:

$$\begin{aligned} P_{cR} &= V_{cR}^2 G_{mm} + V_{cR} V_k [G_{km} \cos(\delta_{cR} - \theta_k) + B_{km} \sin(\delta_{cR} - \theta_k)] \\ &+ V_{cR} V_m [G_{mm} \cos(\delta_{cR} - \theta_m) + B_{mm} \sin(\delta_{cR} - \theta_m)] \end{aligned} \quad (5.10)$$

$$\begin{aligned} Q_{cR} &= -V_{cR}^2 B_{mm} + V_{cR} V_k [G_{km} \sin(\delta_{cR} - \theta_k) - B_{km} \cos(\delta_{cR} - \theta_k)] \\ &+ V_{cR} V_m [G_{mm} \sin(\delta_{cR} - \theta_m) - B_{mm} \cos(\delta_{cR} - \theta_m)] \end{aligned} \quad (5.11)$$

The active and reactive powers at the shunt converter are:

$$P_{vR} = -V_{vR}^2 G_{vR} + V_{vR} V_k [G_{vR} \cos(\delta_{vR} - \theta_k) + B_{vR} \sin(\delta_{vR} - \theta_k)] \quad (5.12)$$

$$Q_{vR} = V_{vR}^2 B_{vR} + V_{vR} V_k [G_{vR} \sin(\delta_{vR} - \theta_k) - B_{vR} \cos(\delta_{vR} - \theta_k)] \quad (5.13)$$

Assuming loss-less converter values, the active power supplied to the shunt converter,

P_{vR} , equals the active power demanded by the series converter, P_{cR} ; that is

$$P_{vR} + P_{cR} = 0 \quad (5.14)$$

Furthermore, if the coupling transformers are assumed to contain no resistance then the

active power at bus k matches the active power at bus m . accordingly,

$$P_{vR} + P_{cR} = P_k + P_m = 0 \quad (5.15)$$

The UPFC power equations, in linearised form, are combined with those of the AC network. For the case when the UPFC controls the following parameters:

- Voltage magnitude at the shunt converter terminal (bus k),
- Active power flow from bus m to bus k ,
- Reactive power injected at bus m , and taking bus m to be a PQ bus, the

linearised system of equations is as follows:

$$\begin{bmatrix} \Delta P_k \\ \Delta P_m \\ \Delta Q_k \\ \Delta Q_m \\ \Delta P_{mk} \\ \Delta Q_{mk} \\ \Delta P_{bb} \end{bmatrix} = \begin{bmatrix} \frac{\partial P_k}{\partial \theta_k} & \frac{\partial P_k}{\partial \theta_m} & \frac{\partial P_k}{\partial V_{vR}} V_{vR} & \frac{\partial P_k}{\partial V_m} V_m & \frac{\partial P_k}{\partial \delta_{cR}} & \frac{\partial P_k}{\partial V_{cR}} V_{cR} & \frac{\partial P_k}{\partial \delta_{vR}} \\ \frac{\partial P_m}{\partial \theta_k} & \frac{\partial P_m}{\partial \theta_m} & 0 & \frac{\partial P_m}{\partial V_m} V_m & \frac{\partial P_m}{\partial \delta_{cR}} & \frac{\partial P_m}{\partial V_{cR}} V_{cR} & 0 \\ \frac{\partial Q_k}{\partial \theta_k} & \frac{\partial Q_k}{\partial \theta_m} & \frac{\partial Q_k}{\partial V_{vR}} V_{vR} & \frac{\partial Q_k}{\partial V_m} V_m & \frac{\partial Q_k}{\partial \delta_{cR}} & \frac{\partial Q_k}{\partial V_{cR}} V_{cR} & \frac{\partial Q_k}{\partial \delta_{vR}} \\ \frac{\partial Q_m}{\partial \theta_k} & \frac{\partial Q_m}{\partial \theta_m} & 0 & \frac{\partial Q_m}{\partial V_m} V_m & \frac{\partial Q_m}{\partial \delta_{cR}} & \frac{\partial Q_m}{\partial V_{cR}} V_{cR} & 0 \\ \frac{\partial P_{mk}}{\partial \theta_k} & \frac{\partial P_{mk}}{\partial \theta_m} & 0 & \frac{\partial P_{mk}}{\partial V_m} V_m & \frac{\partial P_{mk}}{\partial \delta_{cR}} & \frac{\partial P_{mk}}{\partial V_{cR}} V_{cR} & 0 \\ \frac{\partial Q_{mk}}{\partial \theta_k} & \frac{\partial Q_{mk}}{\partial \theta_m} & 0 & \frac{\partial Q_{mk}}{\partial V_m} V_m & \frac{\partial Q_{mk}}{\partial \delta_{cR}} & \frac{\partial Q_{mk}}{\partial V_{cR}} V_{cR} & 0 \\ \frac{\partial P_{bb}}{\partial \theta_k} & \frac{\partial P_{bb}}{\partial \theta_m} & \frac{\partial P_{bb}}{\partial V_{vR}} V_{vR} & \frac{\partial P_{bb}}{\partial V_m} V_m & \frac{\partial P_{bb}}{\partial \delta_{cR}} & \frac{\partial P_{bb}}{\partial V_{cR}} V_{cR} & \frac{\partial P_{bb}}{\partial \delta_{vR}} \end{bmatrix} \begin{bmatrix} \Delta \theta_k \\ \Delta \theta_m \\ \frac{\Delta V_{vR}}{V_{vR}} \\ \frac{\Delta V_m}{V_m} \\ \Delta \delta_{cR} \\ \frac{\Delta V_{cR}}{V_{cR}} \\ \Delta \delta_{vR} \end{bmatrix} \quad (5.16)$$

where ΔP_{bb} is the power mismatch given by Equation 5.14 .

If the voltage control at bus k is deactivated, the third column of Equation 5.16 is replaced by partial derivatives of the bus and the UPFC mismatch powers with respect to the bus voltage magnitude V_k . Moreover, the voltage magnitude increment of the shunt source, $\frac{\partial V_{vR}}{V_{vR}}$ is replaced by the voltage magnitude increment at bus k , $\frac{\partial V_k}{V_k}$.

If both buses, k and m , are PQ, the linearised system of equations is as follows:

$$\begin{bmatrix} \Delta P_k \\ \Delta P_m \\ \Delta Q_k \\ \Delta Q_m \\ \Delta P_{mk} \\ \Delta Q_{mk} \\ \Delta P_{bb} \end{bmatrix} = \begin{bmatrix} \frac{\partial P_k}{\partial \theta_k} & \frac{\partial P_k}{\partial \theta_m} & \frac{\partial P_k}{\partial V_k} V_k & \frac{\partial P_k}{\partial V_m} V_m & \frac{\partial P_k}{\partial \delta_{cR}} & \frac{\partial P_k}{\partial V_{cR}} V_{cR} & \frac{\partial P_k}{\partial \delta_{vR}} \\ \frac{\partial P_m}{\partial \theta_k} & \frac{\partial P_m}{\partial \theta_m} & \frac{\partial P_m}{\partial V_k} V_k & \frac{\partial P_m}{\partial V_m} V_m & \frac{\partial P_m}{\partial \delta_{cR}} & \frac{\partial P_m}{\partial V_{cR}} V_{cR} & 0 \\ \frac{\partial Q_k}{\partial \theta_k} & \frac{\partial Q_k}{\partial \theta_m} & \frac{\partial Q_k}{\partial V_k} V_k & \frac{\partial Q_k}{\partial V_m} V_m & \frac{\partial Q_k}{\partial \delta_{cR}} & \frac{\partial Q_k}{\partial V_{cR}} V_{cR} & \frac{\partial Q_k}{\partial \delta_{vR}} \\ \frac{\partial Q_m}{\partial \theta_k} & \frac{\partial Q_m}{\partial \theta_m} & \frac{\partial Q_m}{\partial V_k} V_k & \frac{\partial Q_m}{\partial V_m} V_m & \frac{\partial Q_m}{\partial \delta_{cR}} & \frac{\partial Q_m}{\partial V_{cR}} V_{cR} & 0 \\ \frac{\partial P_{mk}}{\partial \theta_k} & \frac{\partial P_{mk}}{\partial \theta_m} & \frac{\partial P_{mk}}{\partial V_k} V_k & \frac{\partial P_{mk}}{\partial V_m} V_m & \frac{\partial P_{mk}}{\partial \delta_{cR}} & \frac{\partial P_{mk}}{\partial V_{cR}} V_{cR} & 0 \\ \frac{\partial Q_{mk}}{\partial \theta_k} & \frac{\partial Q_{mk}}{\partial \theta_m} & \frac{\partial Q_{mk}}{\partial V_k} V_k & \frac{\partial Q_{mk}}{\partial V_m} V_m & \frac{\partial Q_{mk}}{\partial \delta_{cR}} & \frac{\partial Q_{mk}}{\partial V_{cR}} V_{cR} & 0 \\ \frac{\partial P_{bb}}{\partial \theta_k} & \frac{\partial P_{bb}}{\partial \theta_m} & \frac{\partial P_{bb}}{\partial V_k} V_k & \frac{\partial P_{bb}}{\partial V_m} V_m & \frac{\partial P_{bb}}{\partial \delta_{cR}} & \frac{\partial P_{bb}}{\partial V_{cR}} V_{cR} & \frac{\partial P_{bb}}{\partial \delta_{vR}} \end{bmatrix} \begin{bmatrix} \Delta \theta_k \\ \Delta \theta_m \\ \frac{\Delta V_{vR}}{V_{vR}} \\ \frac{\Delta V_m}{V_m} \\ \Delta \delta_{cR} \\ \frac{\Delta V_{cR}}{V_{cR}} \\ \Delta \delta_{vR} \end{bmatrix} \quad (5.17)$$

In this case, V_{vR} is maintained at a fixed value within prescribed limits: $V_{vR \min} \leq V_{vR} \leq V_{vR \max}$. The Jacobian terms in Equations 5.16 and 5.17 are given in Appendix C. In order to investigate UPFC further under unsymmetrical fault positions, the MATLAB implementation of these equations using SimPower model are used [14]

5.3 UPFC Performance

In order to study the performance of the UPFC controller, simulations have been performed for the MATLAB implementation test system model studied in [15, 17] by employing the Static Synchronous Series Controller (SSSC) and the STATic synchronous COMPensator (STATCOM) converters that are used here. The operation of the UPFC in STATCOM Var control mode, SSSC power control mode and UPFC power flow control mode are studied. Results are presented and discussed.

5.4 Test System Description

A UPFC is used to control the power flow in a 500 kV transmission system given in [20-22] shown in Figure 5.7. The UPFC located at the left end of the 60-km line L2, between the 500 kV buses B1 and B2, is used to control the active and reactive powers

flowing through bus B2 while controlling voltage at bus B1. It consists of two 100-MVA, three-level, 48-pulse GTO-based converters, one connected in shunt at bus B1 and one connected in series between buses B1 and B2 at bus B-UPFC. The shunt and series converters can exchange power through a DC bus. There are three transmission lines (transmission line $L1_{200}$ km, transmission line 2 is divided into segments ($L2a_{60}$ Km, $L2b_{120}$ km), and transmission line $L3_{20}$ km).

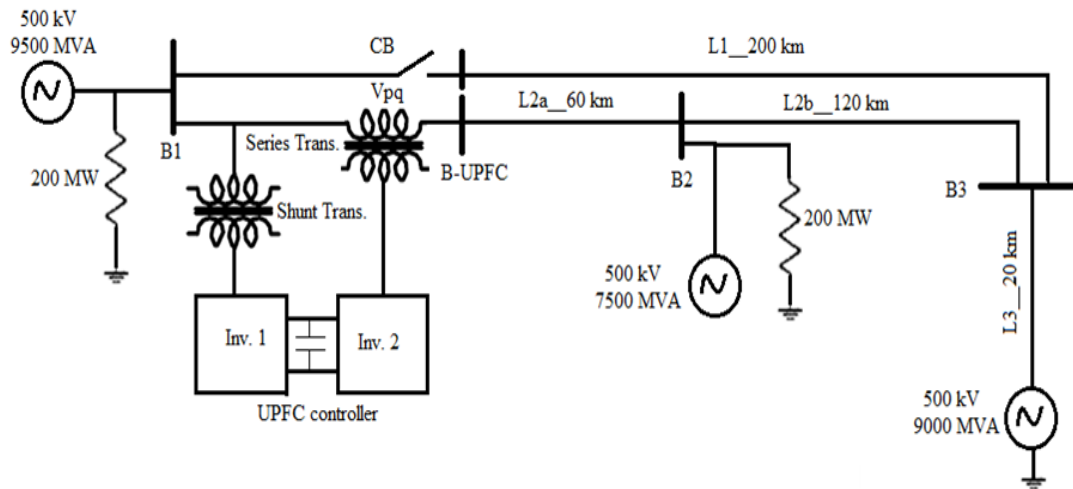


Figure 5.7 Single line daigram for proposed test system [24]

The MATLAB (Simulink) implementation of the test system shown in Figure 5.8 consists of a 3- three phase voltage sources each rated: 500 kV/9500 MVA, 500 kV/7500 KVA and 500 kV/9000 KVA respectively. The three distributed parameter transmission lines are L1 (200 km), L2 (two segment 75 km and 180 km) and L3 (0 km) and. The line parameters R, L, and C are specified by $[N \times N]$ matrices. 2-Three-Phase Parallel RLC load blocks implement a three-phase balanced load as a parallel combination of RLC elements connected at bus B1 and B2. A UPFC phasor model of two 100 MVA IGBT based converters is used (one connected in shunt (STATCOM), and one in connected series (SSSC) with both interconnected through a DC link bus on the DC side and to the AC power system, through coupling reactors and transformers.

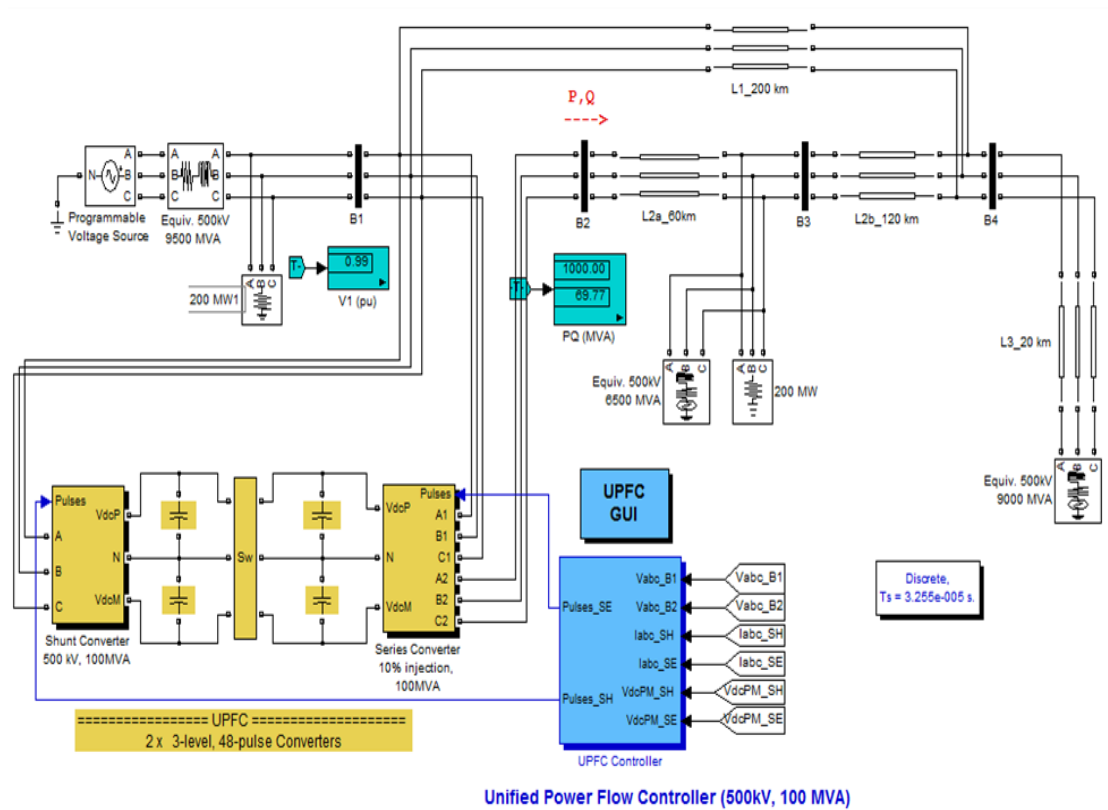


Figure 5.8 MATLAB implementation of the test system

Case 1: UPFC operation in STATCOM Var control mode

The performance of the UPFC in STATCOM Var control mode is given in [20, 21] and some of these simulation is presented here. To study the performance of the UPFC in Var control mode, the reactive power reference is set to + 0.8 pu at $t = 0.2$ s and -0.8 at $t = 0.45$ s. The AC reference voltage is programmed to transiently change from 0.955 pu to 1.045 pu, from 1.0455 pu to 0.955 pu and from 0.955 pu to 1.0 pu, causing the STATCOM operating point to change from fully capacitive to fully inductive mode. The simulation results are shown in Figure 5.8.

For an AC reference voltage equals to 0.955 pu, the initial STATCOM converter current is zero as shown in Figure 5.9c. The DC voltage side is 19.4 kV as shown in Figure 5.9f which is initially lower than its nominal value. For an AC voltage equal to 0.955 pu, the

initial operating point of the STATCOM corresponds to a reactive current absorption equal to 0.85 pu (as shown in Figure 5.9b). The slope adopted for voltage current characteristics is equal to 3%. The initial amplitude of the AC voltage at the connection bus is equal to 0.85 pu (as shown in Figure 5.9a). At steady state, the phase shift angle (δ) is very close to zero, as there is no active power circulating from the STATCOM converter (as shown in Figure 5.9h).

As soon as the step change in the reference voltage is applied around 2 s, the voltage error signal is increased by the step size of 10% (as seen in Figure 5.9g), the positive voltage error makes the voltage regulator order an increase of the reactive current reference to be produced by the STATCOM converter. In the current case, this reference is increased up to 0.72 pu (Figure 5.9b), i.e. the STATCOM converter should generate a full reactive current in order to raise the voltage at the connection bus, so, the STATCOM reacts by generating reactive power ($Q = 70$ Mvar) in order to maintain the voltage level at 0.98 pu (as shown in Figure 5.9d). With the STATCOM switched at fundamental frequency, it is necessary to increase the DC voltage which is achieved by the current regulator control; the DC voltage has been increased to 20.1 kV (as shown in Figure 5.9f). The phase shift angle (δ) becomes transiently negative (Figure 5.9h), charging the DC capacitor. As the reactive reference current is not abruptly increased, the capacitor is smoothly charged without causing oscillations in the control variables.

At $t = 0.45$ s, the voltage source is increased to 1.045 pu of its nominal voltage, The AC voltage error signal is decreased (Figure 5.9g), the negative voltage error makes the voltage regulator order a decrease of the reactive reference current to -0.72 pu (Figure 5.9b). For example, the STATCOM should absorb full reactive current in order to drop the voltage at the connection bus. In this situation, the STATCOM reacts by absorbing the reactive power of ($Q = 70$ Mvar) in order to maintain the voltage at the connection

bus at 1.0 pu as seen in Figure 5.9d. As soon as, the STATCOM changes from generating to absorbing (Capacitive to Inductive modes), the DC voltage has been lowered to 18.2 kV (as shown in Figure 5.9f). The phase shift angle (δ) becomes transiently positive (Figure 5.9h) discharging the DC capacitor.

The measured reactive current is also shown in (Figure 5.9b), where it is observed that the measured current follows the reference value with a time delay of a half cycle approximately.

Figure 5.9c shows the STATCOM current in one phase, as it can be visualized that the current is shifted by an angle of 180° after the step change is applied. The change of the reference voltage together with the measured value is shown in Figure 5.9e. At $t = 0.7$ s, the system returns to its steady state operation because there is no reactive power exchange and the STATCOM follows the reference value.

From Figure 5.9, it is clear that the STATCOM responds to the variation of the reactive power and it can change very quickly and smoothly.

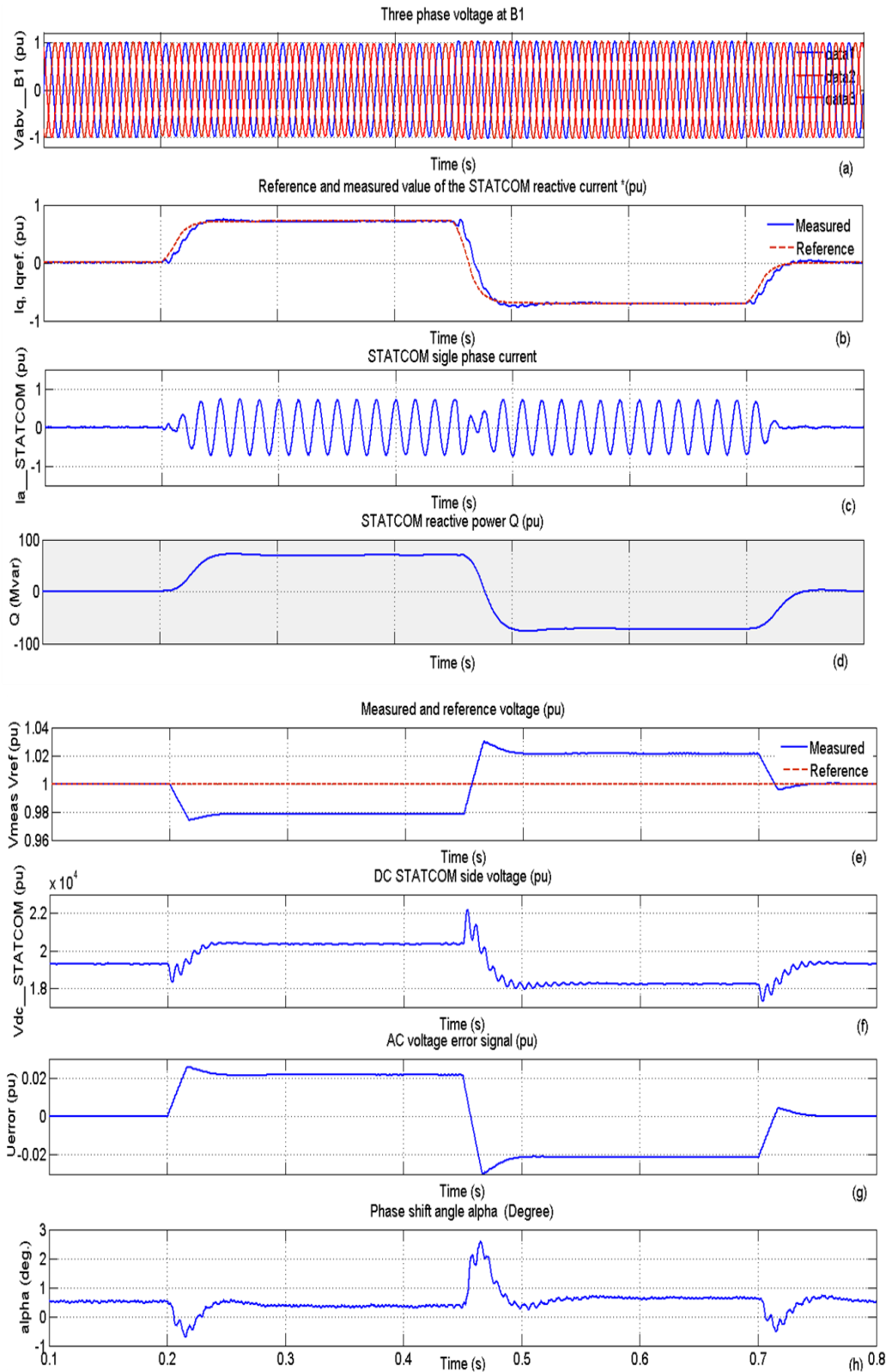


Figure 5.9 Step change in the AC voltage reference from 0.95 to 1.05 and from 1.0455 to 0.95 pu. applied at 2 ms and 4.5 and lasting 250 ms

Case 2: UPFC operation in SSSC power flow control mode

The performance of the UPFC in SSSC power flow control mode is presented in [20] and some of these simulations is presented here. To study the performance of the UPFC in SSSC power flow control mode, the active and reactive power reference (steady state power flow) is set to 7.8 and -0.6 pu respectively. Then, at $t = 0.2$ s and $t = 0.5$ s, the active and reactive power reference are increased by 1.0 and 0.15 pu respectively (The simulation results are shown in Figure 5.10).

The initial reference values of active and reactive power are equal to 8.7 and -0.6 pu., resulting in a series voltage close to zero, as seen in Figure 5.10f. Steps changes with amplitudes equal to 1.0 and 0.15 pu. are applied around 200 ms and 500 ms in the active and reactive power reference values. The purpose is to increase the transmission capacity of the line as well as to reduce the reactive power generation by the receiving bus.

The active and reactive power rise time is similar to the pure current control (as shown in Figure 5.10a, b). It needs to be pointed out that changes in the power reference will affect both d and q components of the line current reference, [15, 17], the response due to the step changes would be considerably worsened if the decoupling function was not employed because the interaction between the controllers would be stronger.

The final operating point of the series SSSC converter is different from the previous cases because the positive step change in the reactive power makes the q-component of the line current decrease (as shown in Figure 5.10d).

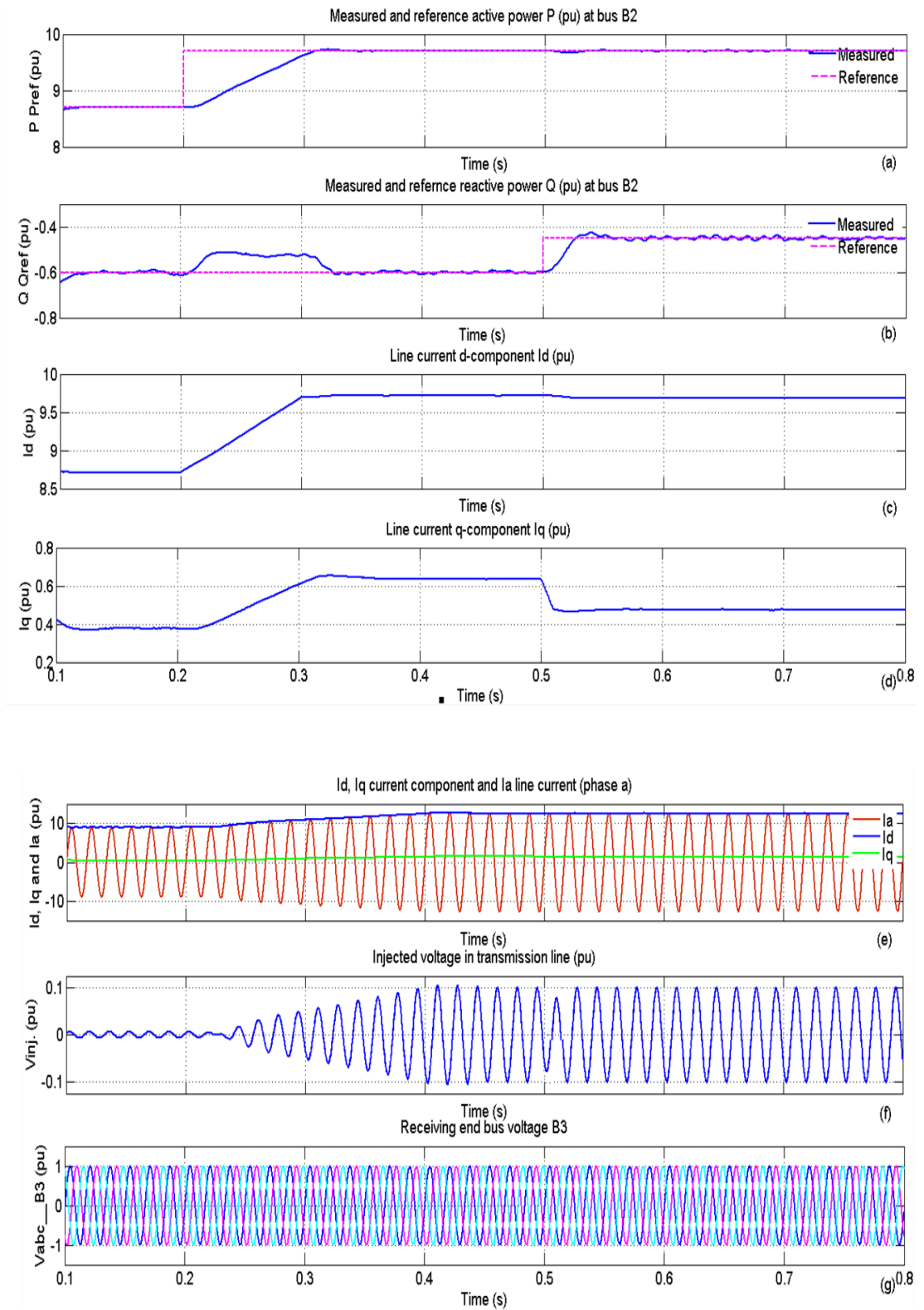


Figure 5.10 Response to a step change in the active and reactive power reference

At $t = 200$ ms and $t = 500$ ms the step changes are applied, there are changes in amplitude and the angle of the line current, by means of the insertion of the series voltage (shown in Figure 5.10f). Looking closer to (Figures 5.10e, f) it is noticed that the injected series voltage decreases after the step change in the reactive power is applied. Figure 5.10c shows the change in q component of line current according to step changes in active and reactive power. Figure 5.10g shows the receiving end voltage at bus B3.

From Figure 5.10, the operation of the UPFC in SSSC Var effectively controls the transmitted active and reactive power. The active and reactive power follows the changes in the reference signals and reacts quickly to these changes.

Case 3: UPFC operation in power flow control mode

In this experiment, the natural power flow through bus B2 when zero voltage is generated by the series converter is $P=+870$ MW and $Q=-60$ Mvar is taken as a reference.

The reference active and reactive powers are specified initially to $+8.7$ pu ($+870$ MW) and $Q_{ref}=-0.6$ pu (-60 Mvar). At $t=0.25$ s the active power is changed to $+10$ pu ($+1000$ MW). Then, at $t=0.5$ s, Q_{ref} is changed to $+0.7$ pu ($+70$ Mvar). The reference voltage of the shunt converter will be kept constant at $V_{ref}=1$ pu during the whole simulation.

The simulation results are shown in Figure 5.11. Steady state is reached ($P=+8.7$ pu; $Q=-0.6$ pu as shown in Figure 5.11 a, b), then, at $t = 0.2$ s the active power is smoothly ramped to the new setting ($+ 10$ pu) in approximately 150 ms (Figure 5.11a).

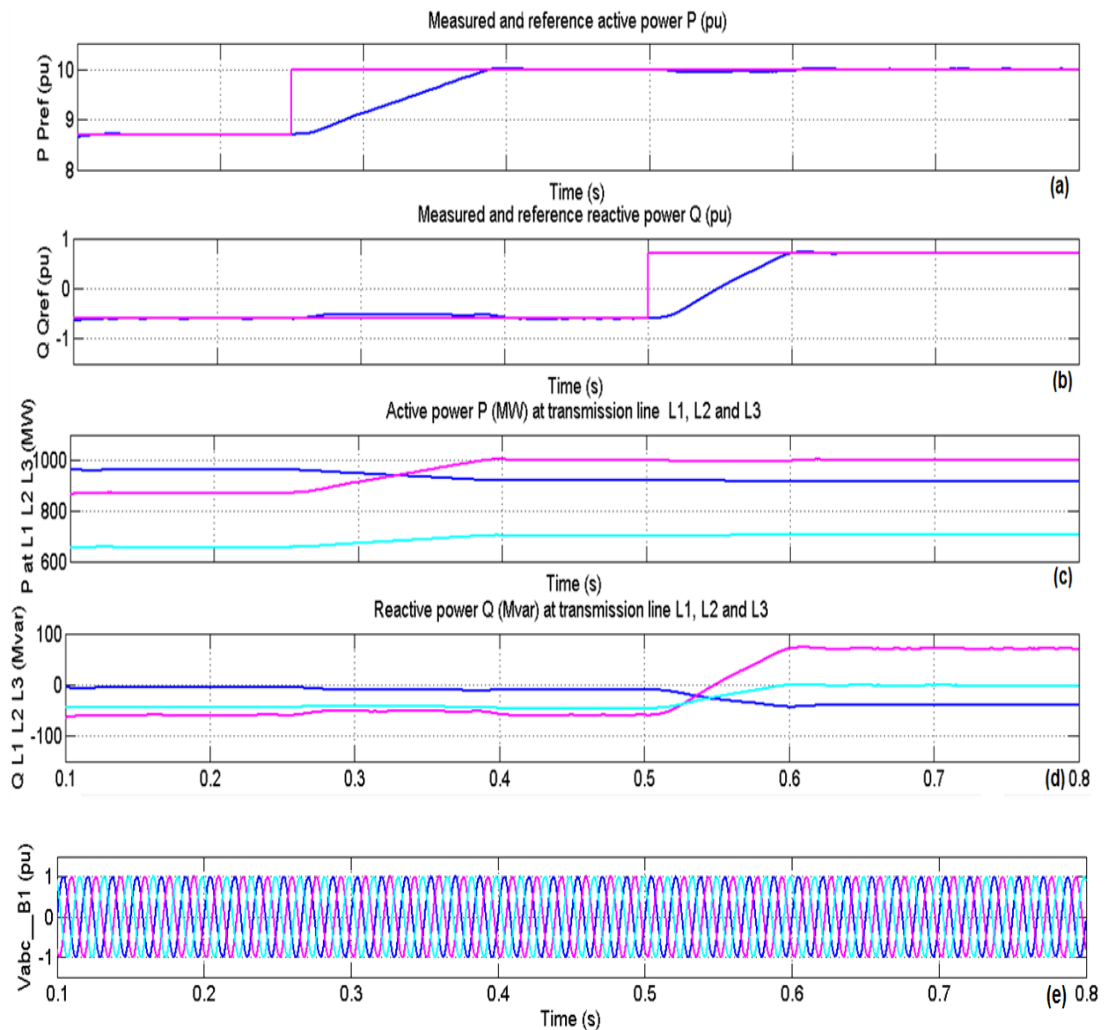


Figure 5.11 Performance of the UPFC controller

As a result, the transmitted power in transmission L2a is ramped from its steady state (8.7 pu) to the new state (10 pu) and the transmitted power in transmission line L1 is reduced to 9 pu as shown in Figure 5.11c.

At $t = 0.5$ s, the reactive power is increased to its new setting (+0.7 pu) very quickly. As a result, the reactive power in transmission line L2a is increased from its steady state value to the new value while the reactive power in transmission line L1 is decreased to about -0.5 pu (as shown in Figure 5.11d).

The sending end voltage is kept constant throughout the whole simulation (as shown in Figure 5.11e).

As a result, UPFC is a very effective tool in controlling the active and reactive power flow through the line and the voltage at the point of common connection.

5.5 UPFC connected to the weakest bus of the WSCC 3-machine, 9-bus test system

Voltage stability analysis based on static and dynamic criteria has been discussed in chapter 3 and chapter 4. The results show that bus B8 in the WSCC 3-machine, 9 bus test system is the weakest bus and required special care to prevent it from voltage collapse. An AUPFC can have the ability to control power transfer capability and improve power system voltage stability. In this section a UPFC is connected to the weakest bus in the WSCC test system in order to control the voltage at bus B8 to 1.0 pu and improve power transfer power capability in transmission line L2.

5.5.1 Test system description

A UPFC is used to control the power flow in a 500 kV transmission system. The Western System Coordinate Council (WSCC) 3-machine, 9-bus test system used in section 3.4 [23] is used here as shown in Figure 5.12. The test system connected in a loop configuration, consists essentially of nine buses (B1 to B9) interconnected through transmission lines (L1, L2, L3). Three power plants located on the 500 kV systems generate a total of 2500 MW power which is transmitted to a 500 kV, 8100 MVA equivalent load centre and a (100, 90, 125) MW load connected at buses B5, B6, and B8 respectively. The power plant models include a speed regulator, an excitation system as well as a Power System Stabilizer (PSS).

The UPFC located at the right end of line L1a is used to control the active and reactive powers at the transmission line L1b, as well as the voltage at bus B8 which is identified as the weakest bus in previous sections. It consists of a phasor model of two 100 MVA IGBT based converters (one connected in shunt (STATCOM), and one in connected series (SSSC)) and both interconnected through a DC link bus on the DC side and to the AC power system, through coupling reactors and transformers. The series converter can inject a maximum of 10 % of nominal line-to-ground voltage (28.8 kV) in series with transmission line L1a.

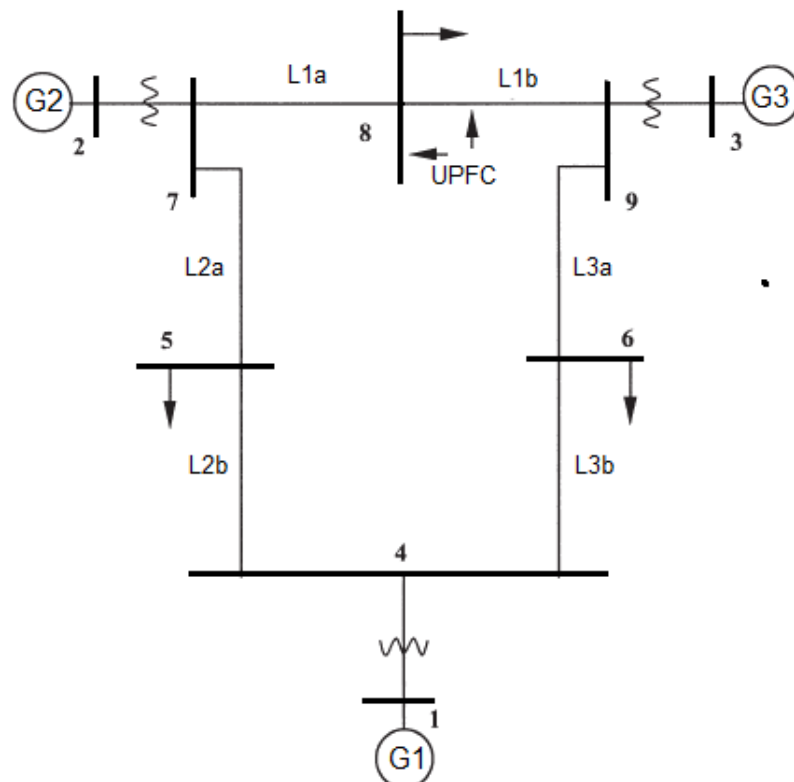


Figure 5.12 WSCC 3-machines, 9-bus test system [1]

The MATLAB implementation of the WSCC test shown in Figure 5.13 consists of a three generation substation designated by G1, G2 and G3 each consists of a Synchronous Machine block which operates in generator mode each rated at 1200 MVA, 16.5 kV; 1000 MVA, 18 kV and 1200 MVA, 13.8 kV respectively. Three D/Yg connected step up transformers each rated at 1200 MVA, 16.5 kV/230 kV; 1000 MVA, 18 kV/500 kV and 1200 MVA, 13.8 kV/500 kV. Six Three-Phase PI Section transmission line blocks implement a balanced three-phase transmission line model with parameters lumped in a PI section. The line parameters R, L, and C are specified as positive and zero sequence parameters that take into account the inductive and capacitive couplings between the three phase conductors, as well as the ground parameters. Three Three-Phase Parallel RLC Load blocks implement a three-phase balanced load as a parallel combination of RLC elements connected at bus B5, B6 and B8. The UPFC phasor model consists of two 100 MVA IGBT based converters (one connected in shunt (STATCOM), and one in connected series (SSSC)) both of them interconnected through a DC link bus on the DC side and to the AC power system through coupling reactors and transformers.

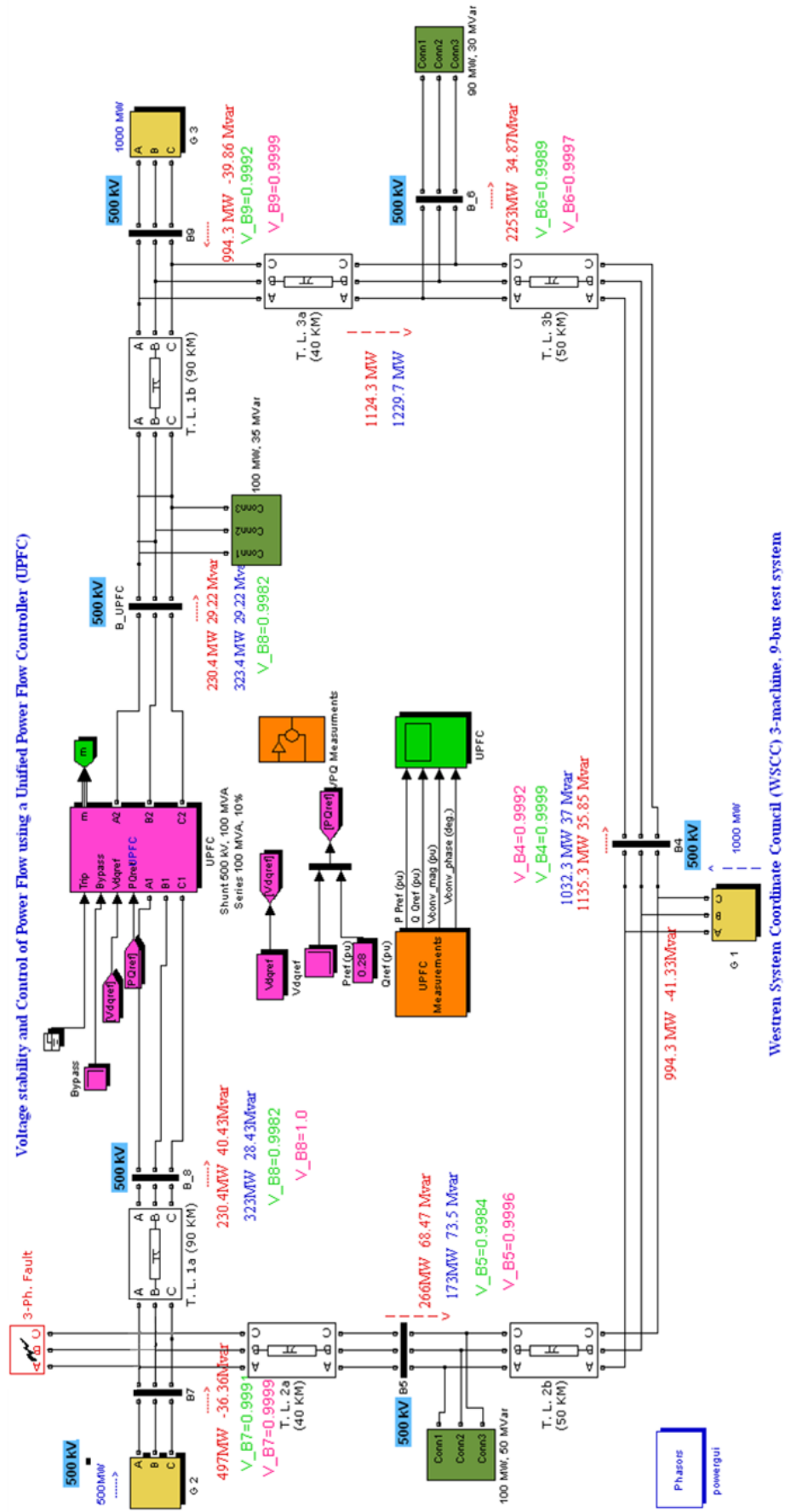


Figure 5.13 The steady state power flow of WSCC test system (UPFC out of service)

5.5.2 Simulation results and discussions

Using the load flow option of the UPFC, the test system has been initialized with plants G1, G2 and G3 generating respectively 1000 MW, 500 MW and 1000 MW, and the UPFC out of service (bypass breaker closed). The resulting steady state power flow obtained at buses B4 to B9 is indicated by red numbers on the circuit diagram shown in Figure 5.13. The green numbers on the circuit diagram show the steady state voltage obtained at buses B4 to B9. From the obtained bus voltages it is clear that B8 is the weakest bus in the test system as shown in Figure 5.14 and this confirms the results obtained in section 3.4.2.

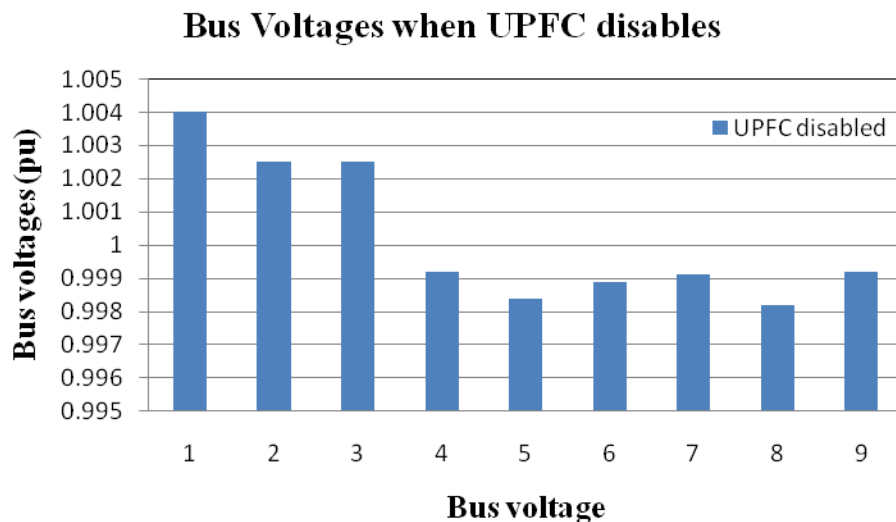


Figure 5.14 Bus voltages when UPFC out of service

In order to study the performance of the UPFC in voltage stability and power flow control, the UPFC reference active and reactive powers are set equal to the active and reactive power obtained from steady state power flow when the bypass breaker is closed. The natural power flow at bus B_UPFC was 223.5 MW and 28 Mvar. This reference active power is programmed with an initial active power of 2.235 pu corresponding to the natural flow. Then, at $t = 3$ s, the reference power is increased by

0.1 pu (100 MW), from 2.235 pu to 3.235 pu, while the reference reactive power is kept constant at 0.28 pu as shown in Figure 5.15.

The simulation results of the UPFC (shown in Figure 5.15a, b) show how the active and reactive power measured at B-UPFC follow the reference values. At $t = 1$ s, when the bypass breaker is opened the natural power is diverted from the bypass breaker to the UPFC series branch without noticeable transient. At $t = 3$ s, the power increases at a rate of 0.1 pu/s. It takes less than one second for the power to increase to 323 MW. This 100 MW increase of active power at bus B-UPFC is achieved by injecting a series voltage of 0.089 pu with an angle of 92.5 degrees as shown in Figure 5.15c, d. This results in an approximate 100 MW decrease in the active power flowing through transmission line L2 (from 266 MW to 173 MW).

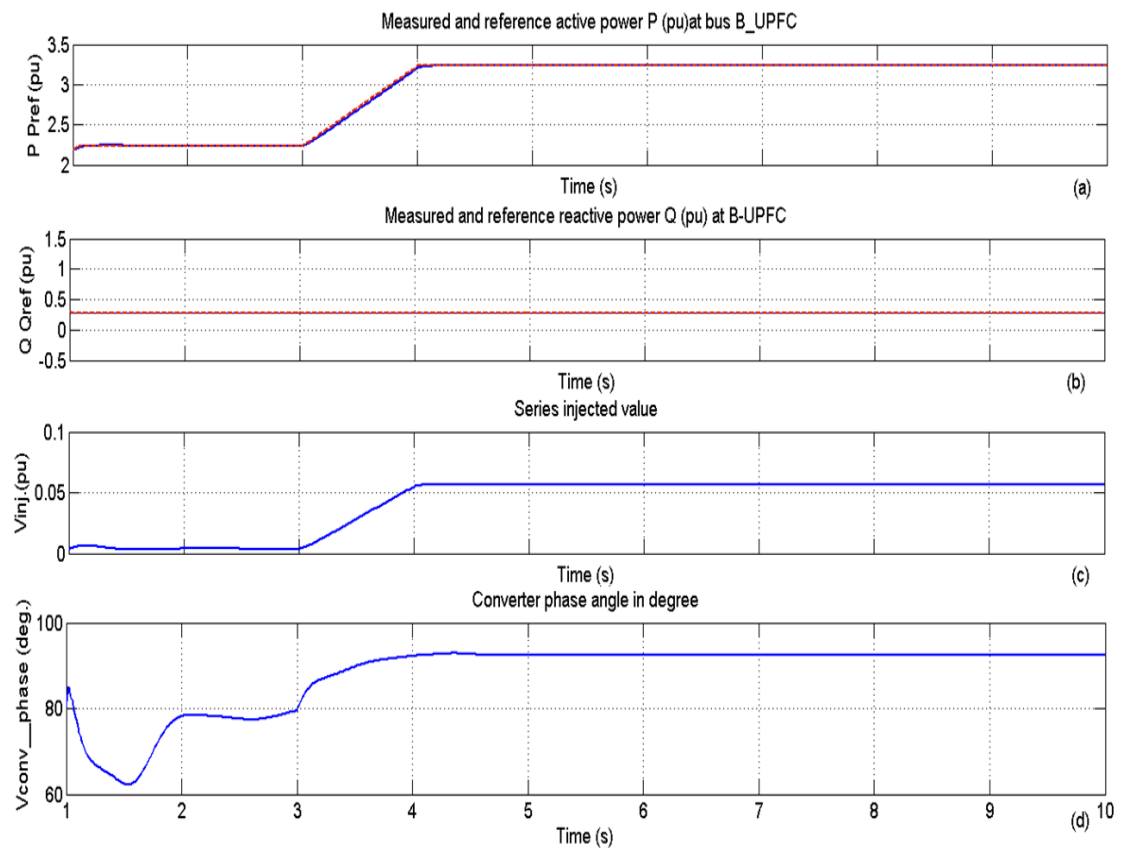


Figure 5.15 The performance of the UPFC in voltage stability and power flow control

The resulting steady state power flow and voltages obtained at buses B4 to B9 when the UPFC is in operation is indicated by blue and magenta numbers on the circuit diagram shown in Figure 5.13.

Figure 5.16 shows the response of the UPFC according to reference active power changes. It is clear that the UPFC changes smoothly to the new reference in approximately one second.

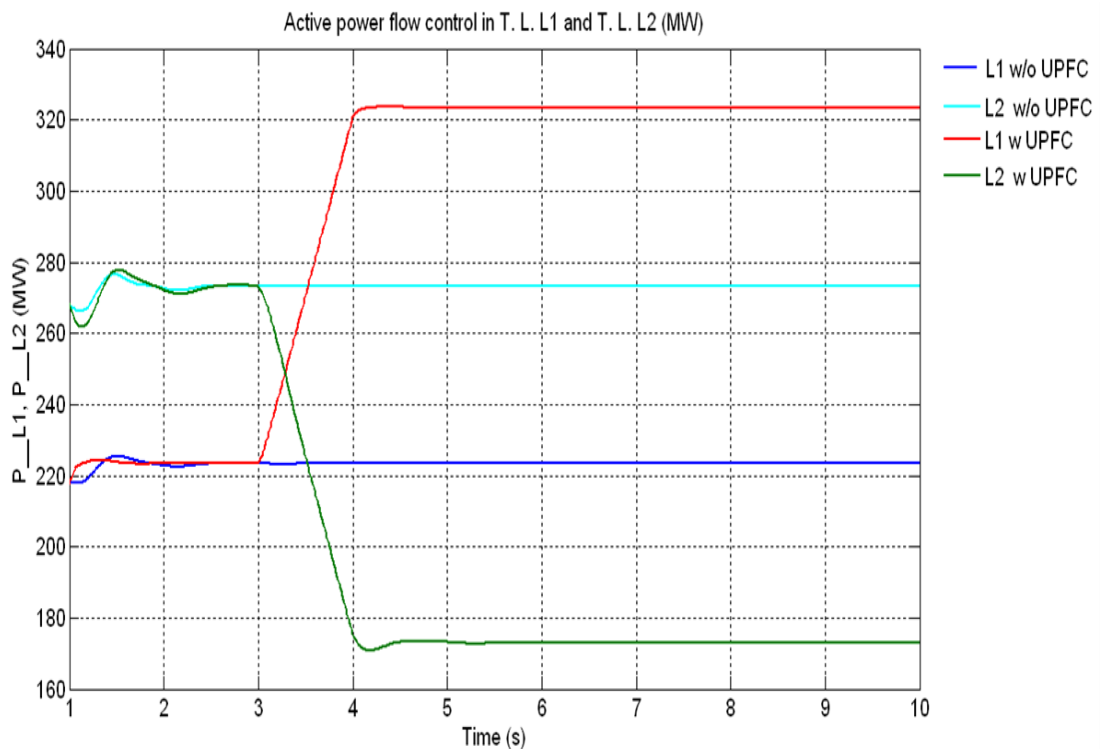


Figure 5.16 Test system with and without UPFC

Figure 5.17 shows the measured value of the bus voltages when the UPFC is in/out operation. The simulation results show that there is a good improvement in the test system voltage stability and power flow control when the UPFC is installed at the weakest bus.

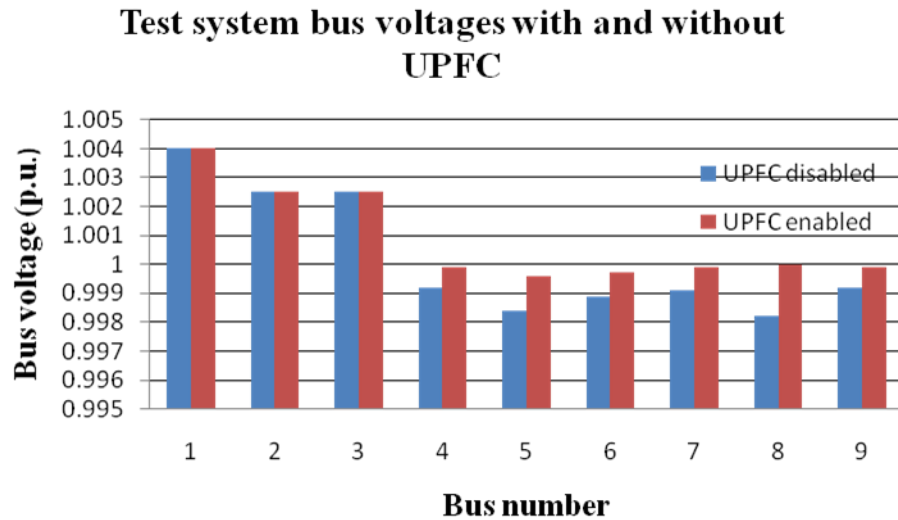


Figure 5.17 Bus voltage of the test system with and without UPFC.

5.6 Summary

This chapter has presented UPFC controller topologies based on semiconductor switches with turn-off capability. Two MATLAB (Simulink) test system models were studied. The first test is the modified IEEE-4 buses test system used to investigate the different functions of the SSSC, STATCOM and UPFC. The simulation results show these controllers have a significant impact on the power flow and voltage levels when tested separately or in common structure with UPFC. Also, the results show that these controllers follow the changes in the reference signal smoothly and very quickly.

The second test is the WSCC test system used in previous chapters to identify the weakest bus. In this test, the UPFC is connected to the weakest bus; the simulation results present an improvement in the voltage level of the weakest bus as well as the transmitted power through the transmission line. This test is the basis of further analysis of the UPFC when subjected to unsymmetrical faults in the next chapter.

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6: THE EFFECT OF FAULT TYPE AND LOCATION ON THE UPFC OPERATION

6.1 Aim of the chapter

Whilst much literature exists on fault conditions, it is not clear in the literature what happens if a UPFC is included in a weak grid. It may have been assumed that faults near the UPFC would naturally damage the UPFC and hence the lack of published materials. However, it is essential to investigate this area as vital information regarding the ratings of devices and protection systems will require an understanding of the voltage, current and power deviation during the fault condition. In this chapter, an investigation is carried out to study unsymmetrical faults in a UPFC connected grid system and how they may be resolved. The effect of unsymmetrical fault positions and type on the UPFC is investigated according to G59 protection, stability and reliability regulations [15-18].

The main focus of the G59 requirement that the phase voltage excursions outside limits of -10% and $+10\%$ for over 0.5 seconds are not permitted.

In this chapter three types of unsymmetrical fault are investigated. They are:

1. Single Line-to-Ground (S-L-G) faults,
2. Double Line-to-Ground (D-L-G) faults,
3. Line-to-Line faults.

6.2 Brief review of faults in power systems

A weak power system is typically affected by faults on the grid. A fault in a circuit is any failure which interferes with the normal flow of current [5, 6]. Permanent faults [7] are caused by a line being on the ground, by insulator strings breaking because of ice loads [8], by permanent damage to towers [9] or and by lightning arrester failure [10]. Most faults of 115 KV and higher are caused by lightning [11], which results in the flashover of insulators. Line-to-line faults (not involving ground) are less common and temporary [12]. The vast majority of transmission line faults (75 %) are of the single line to ground type [13], which arises from the flashover of only one line to the tower and ground. The smallest numbers of faults, roughly about 5 %, involve all three phases and are called three-phase faults [4]. Other types of transmission line faults are line-to-line faults which do not involve the ground [14], and double line-to-ground faults [15]. All the above faults except the three phase type are unsymmetrical and cause an imbalance between phases. In this thesis, the unsymmetrical (Single Line-to-Ground, Double Line-to-Ground, and Line-to-Line) faults are being examined.

Figure 6.1 shows the types of faults that can occur on a three phase AC system. These faults are Single Line-to-Ground, Line-to-Line, Double Line-to-Ground, Three Line, Three Line-to-Ground, Line-to-Pilot and Pilot-to-Ground faults.

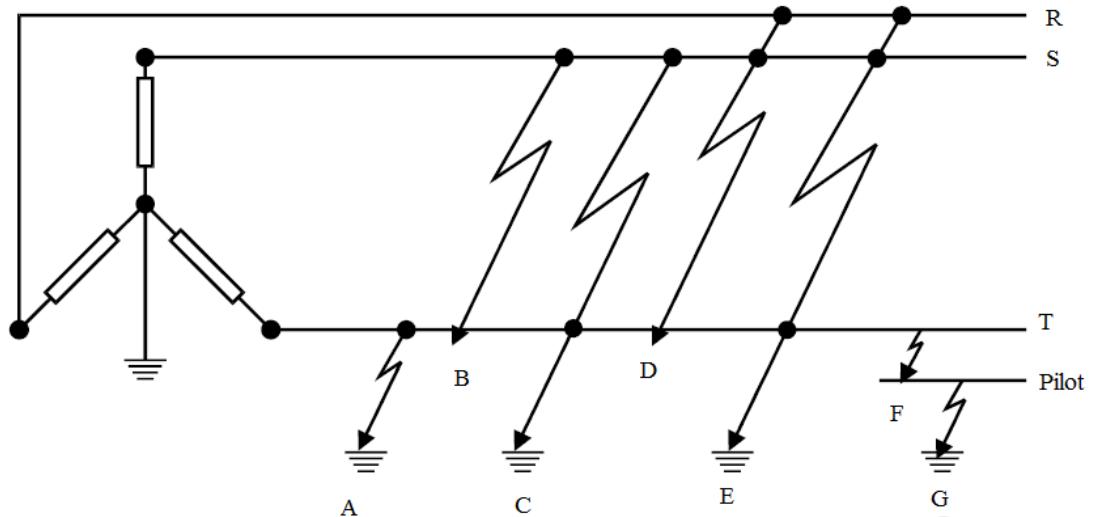


Figure 6.1 Types of Faults on a Three Phase System. (A) Line-to-Ground fault, (B) Line-to-Phase fault, (C) Line-to-Line-to-Ground fault (double Line-to-Ground fault), (D) Three Line fault, (E) Three Line -to-Ground faults, (F) Line -to-pilot fault *, (G) Pilot-to-Ground fault *, * In underground mining applications only

The single-line diagram [16, 25] shown in Figure 6.2 is used to illustrate the mechanism of the fault in a three phase system. It consists of a three-phase, 60 Hz, 735 kV power system transmitting power from a power plant consisting of six 350 MVA generators to an equivalent system through a 600 km transmission line. The transmission line is split into two 300 km lines connected between buses B1, B2 and B3. To increase the transmission capacity, each line is series compensated by capacitors representing 40% of the line reactance. Both lines are also shunt compensated by a 330 MVar shunt reactance. The shunt and series compensation equipment is located at the B2 substation where a 300 MVA-735/230 kV transformer feeds a 230 kV-250 MW load. Each series compensation bank is protected by metal-oxide varistors (MOV1 and MOV2). The two circuit breakers of line 1 are shown as CB1 and CB2.

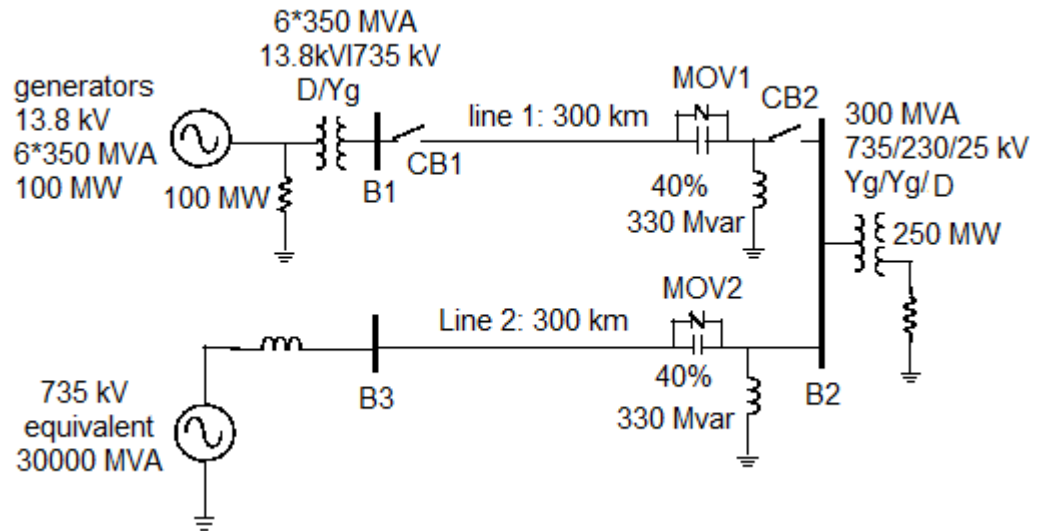


Figure 6.2 the single-line diagram illustrating the fault mechanism [16, 25]

The MATLAB implementation [16, 25] of Figure 6.2 is shown in Figure 6.3. The generation substation is modeled by six simplified synchronous machine block library models [17, 18]; both the electrical and mechanical characteristics of a simple synchronous machine each rated 350 MVA 13.8 kV. The electrical system of the synchronous machine for each phase is modeled by a voltage source connected in series with R - L impedance, which implements the internal impedance of the machine. The step up transformer is modeled also by six three-phase transformer (two windings) library blocks which? Implement a three-phase transformer using three single-phase transformers each rated at 350 MVA 13.8/750 kV. The three-phase circuit breaker model implements a three-phase circuit breaker where the opening and closing times can be controlled either from an external Simulink signal (external control mode), or from an internal control timer (internal control mode). whereas the transmission line is modelled by a distributed parameter line block models which implements an N-phase distributed parameter line model with lumped losses. The three-phase source block model implements a balanced three-phase voltage source with internal R - L impedance. The three voltage sources are connected in Y with a neutral connection that can be

internally grounded or made accessible with 30000 MVA rated power and 750 kV rated voltage. Four three-phase series *RLC* load blocks implement a three-phase balanced load as a series combination of *RLC* elements.

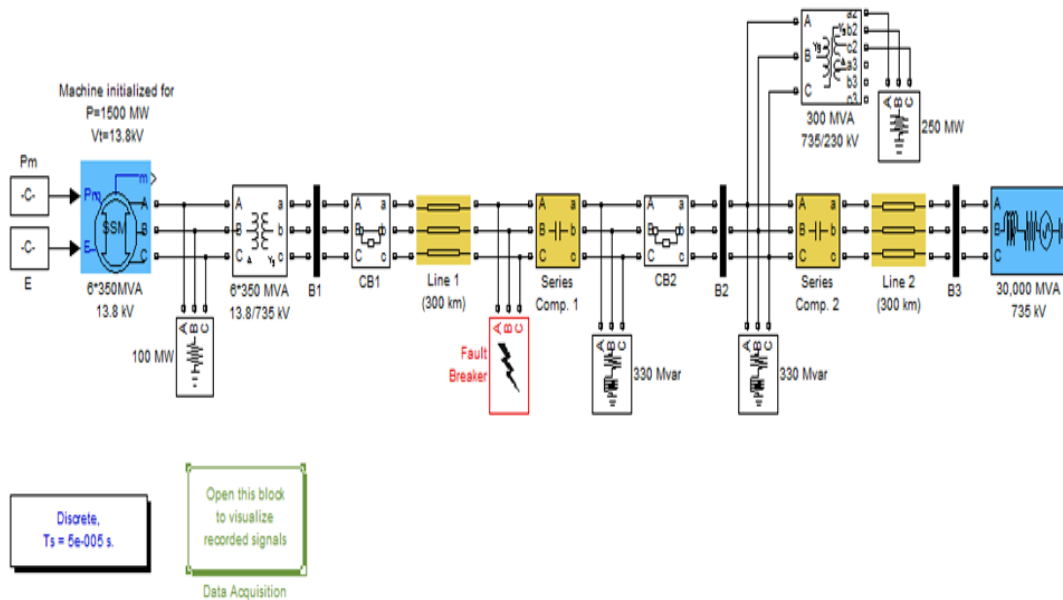


Figure 6.3 MATLAB model for the single line diagram illustrating the fault mechanism [25]

A single Line-to-Ground fault is applied on phase a of line 1, on the line side of the capacitor bank at $t = 0.02$ s and lasting for 10 ms. Once the fault is applied and the system is allowed to reach the steady state, the current has a peak value of 20 kA as shown in Figure 6.4. However, it can be seen that the current rises suddenly and the first peak following the fault, is 35 kA which is about 75% higher than the post-fault steady-state value. Also note that the peak value of the current will vary with the instant occurrence of the fault. However, the peak value of the current is nearly 2.5 times the pre-fault current value in this case. In general, depending on the ratio of source and load impedances, the faulted current may shoot up anywhere between 10 and 20 times the pre-fault current [19].

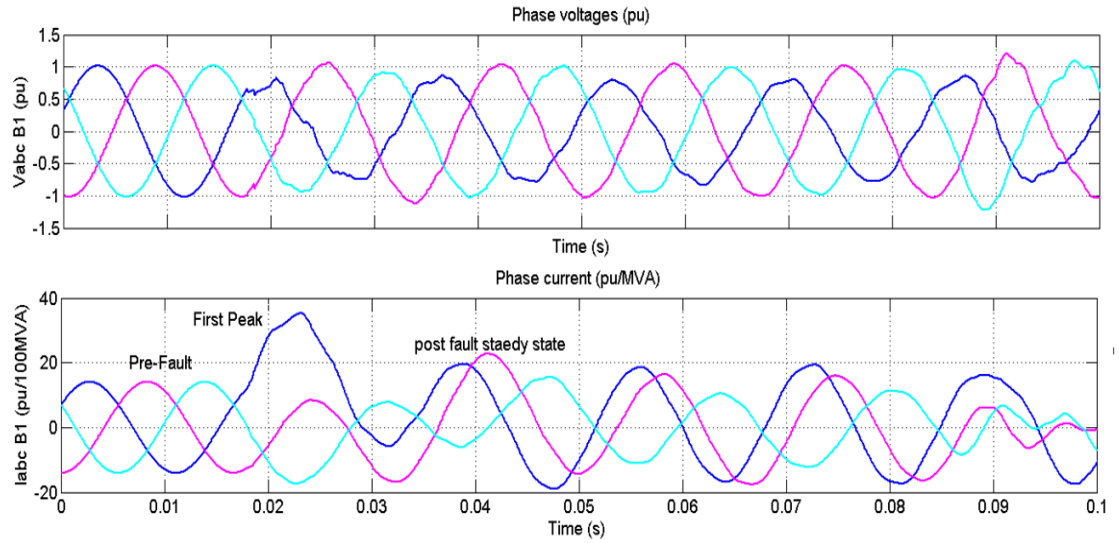


Figure 6.4 Voltage and current waveform as a result of Single L-G fault is applied at line 1 of the test system

6.3 Single Line-to-Ground faults

In this section, the performance of the UPFC and the grid to a Single Line-to-Ground (S-L-G) fault is investigated using the well-known WSCC 3-machine, 9 bus 500 kV test system previously used in section 3.2 and shown again here in Figure 6.5.

For purpose of readability, to summarise from chapter 5, the UPFC is used in a 500 kV transmission system MATLAB model for the WSCC test system shown in Figure 6.5. The UPFC located at the right end of line L1a is used to control the active and reactive powers at the transmission line L1b, as well as the voltage at bus B8 which was identified as the weakest bus in the previous chapters. The UPFC consists of a phasor model of two 100 MVA IGBT based converters (one connected in shunt (STATCOM), and one in connected series (SSSC) and both interconnected through a DC link bus on the DC side and to the AC power system, through coupling reactors and transformers). The series converter can inject a maximum of 10 % of the nominal line-to-ground voltage (28.8 kV) in series with transmission line L1a.

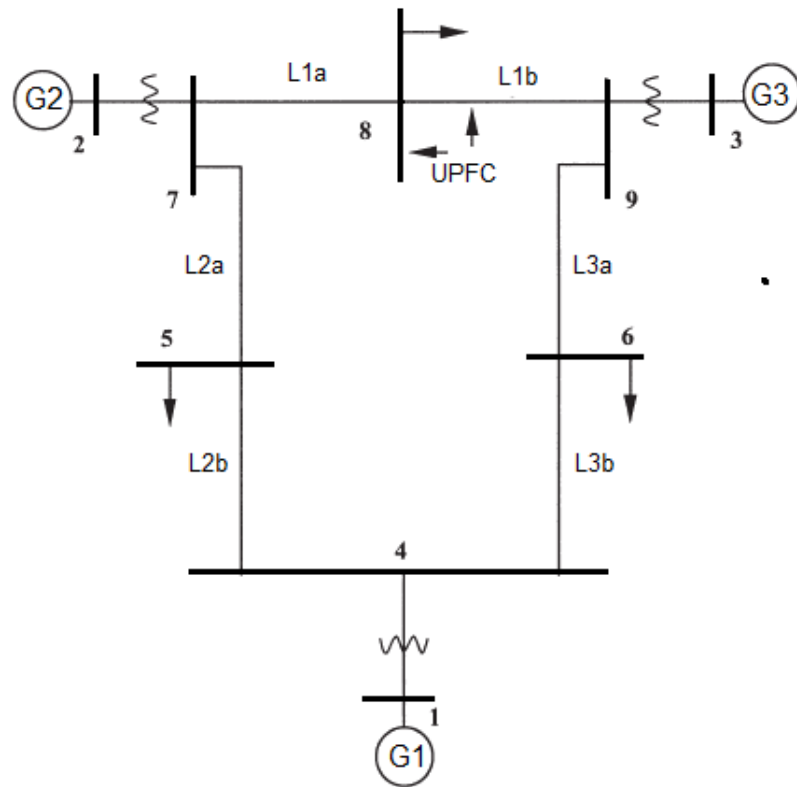


Figure 6.5 WSCC 3-machines, 9-bus test system

The resulting steady state power flow obtained at buses B4 to B9 when UPFC is out of service is indicated by red numbers on the circuit diagram shown in Figure 6.6.

(Repeated from section 5.3). Details of the model are given in section 5.4

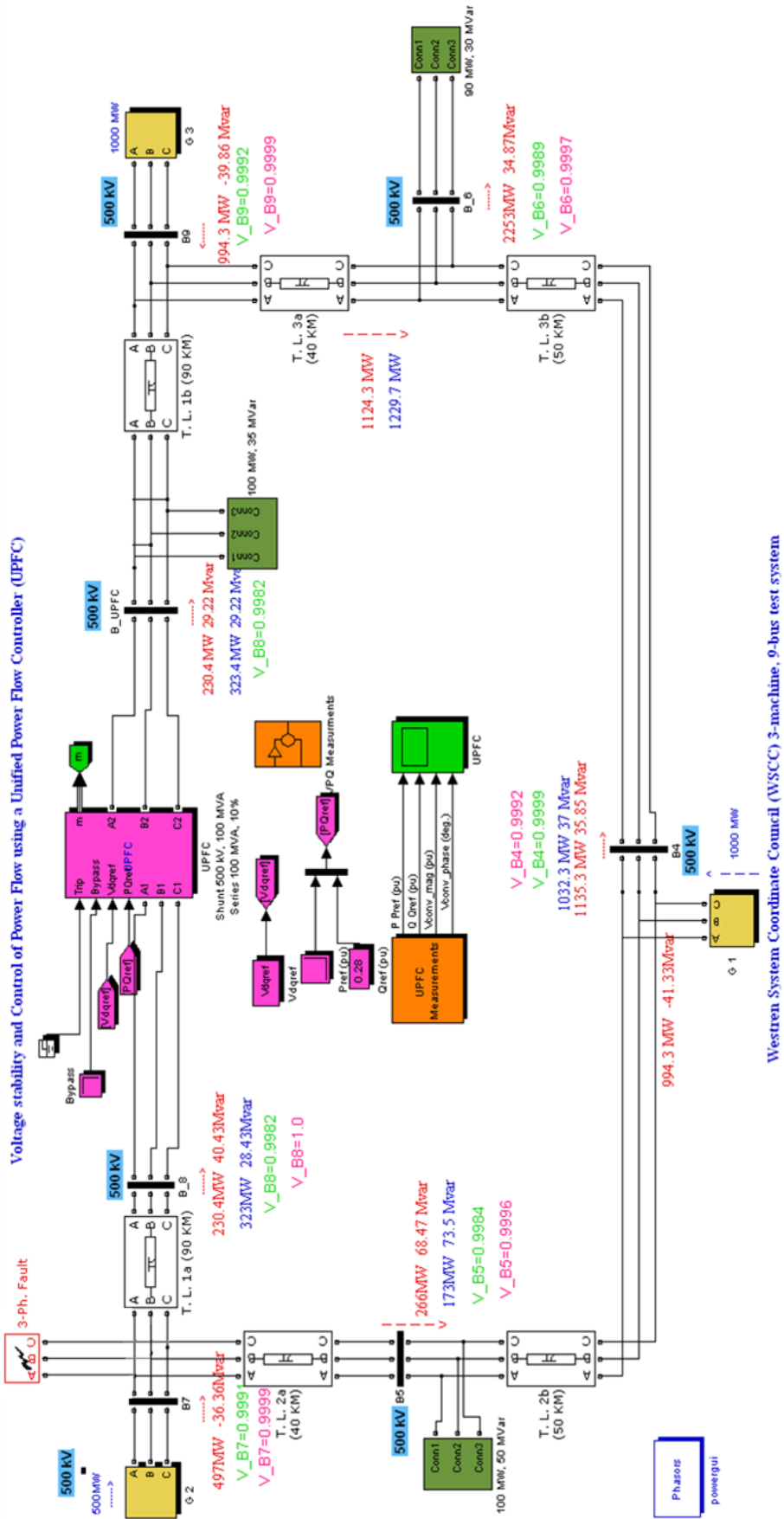


Figure 6.6 The steady state power flow of the WSCC 3-machine, 9-bus test system

6.3.1 Simulations

The following simulations have been conducted in the MATLAB (Simulink) environment in order to investigate the effect of S-L-G faults on the operation of a UPFC connected to the weakest bus of the WSCC test power system:

- a. Applying an S-L-G fault at bus B7 with and without a UPFC and investigating the effect of the UPFC on the two buses feeding the nearest bus.
- b. Applying an S-L-G fault at bus B7 when the UPFC is connected to bus B8 and measuring V, P, Q and I in all other buses.
- c. Applying an S-L-G fault at different locations of the grid and measuring the UPFC converter voltage magnitude, UPFC converter current and voltages at bus B8 as a result of S-L-G fault applied at the other buses

The MATLAB block measurement is used to measure the test system parameters; Voltage V, Current I, Active power Q, and Reactive power Q.

The three-phase V-I Measurement block in MATLAB (Simulink) is used to measure instantaneous three-phase voltages and currents in a circuit. When connected in series with three-phase elements, it returns the three phase-to-ground or phase-to-phase peak voltages and currents. This can output the voltages and currents in per unit (pu) values or in volts and amperes.

The active power and reactive power MATLAB block measures the active and reactive power associated with a periodic voltage-current pair that can contain harmonics. P and Q are calculated by averaging the VI product with running an average window over one cycle of the fundamental frequency, so the powers are evaluated at fundamental frequency. More detail is given in Appendix B.

6.3.1.1 Simulation A

An S-L-G fault is applied at the sending end bus B7 of the transmission line L1a of WSCC test system at $t = 6$ s and lasting for 150 ms with UPFC and without UPFC. The following are measured at B7 and at the receiving end bus B9; (a) the bus voltages, (b) the fault current I.

The simulation results as shown in Figure 6.6 show the response of the test system when the UPFC is disconnected and when connected to bus B8.

- a. Referring to Figure 6.7a (current waveforms when the UPFC is disconnected).

Before the fault at bus B7, the steady state current at bus B7 is 2.3 kA. The peak fault current is 94 kA. During the fault it has a steady state of around 77 kA. After fault clearing, the current returns to steady state in 220 ms. The pre-fault steady state current at bus B9 is 1.6 kA. The peak fault current is 20 kA. During the fault it is around 17 kA. It returns to its post fault steady state current in 220 ms. When UPFC is connected; before the fault at bus B7, the steady state current at bus B7 is 3.3 kA. The peak of the fault current is 94 kA. During the fault, it has steady state of around 77 kA. After fault clearing, the current returns to its steady state in 220 ms. The pre-fault steady state current at bus B9 is 2.3 kA. The peak fault current is 20 kA. During the fault it is around 14 kA. It returns to its post fault steady state current in 220 ms.

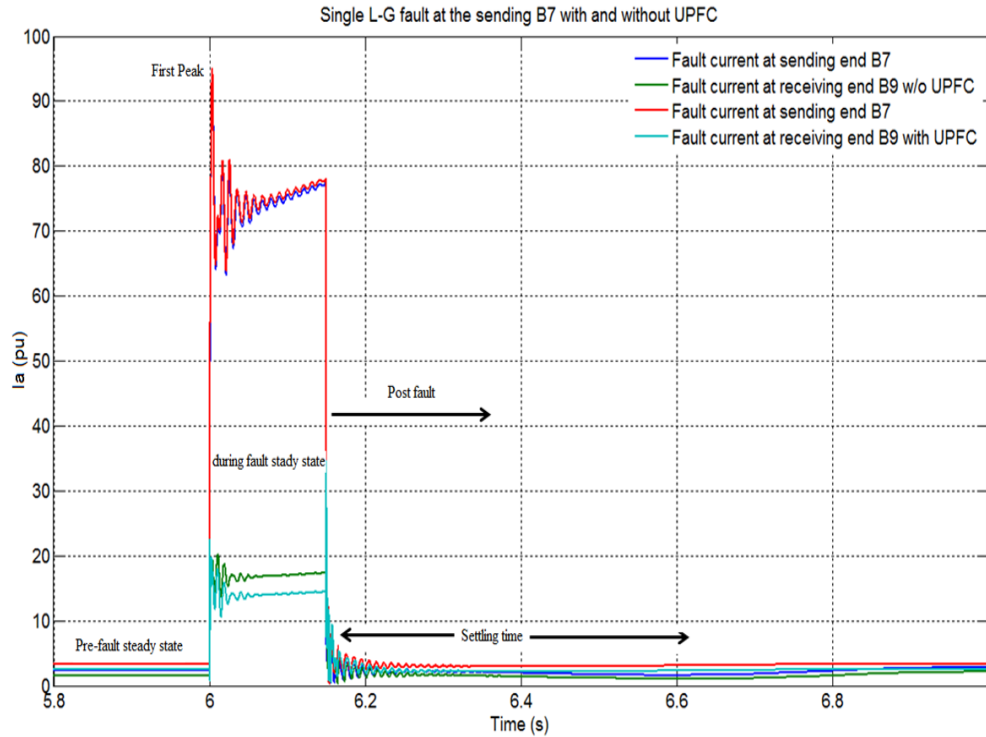
- b. Referring to Figure 6.7b (voltage waveforms when the UPFC is disconnected).

Before the fault at bus B7, the steady state is 1 pu. The peak fault voltage 0.58 pu. During the fault it has a steady state fault of 0.625 pu, after fault clearing, the voltage at B7 returns to its steady state in about 1 s. The pre-fault steady state voltage at bus B9 is 1 pu. The peak of fault voltage is 0.7 pu. During fault, its steady is 0.875 pu. After fault clearing, the voltage at bus B9 returns to its steady

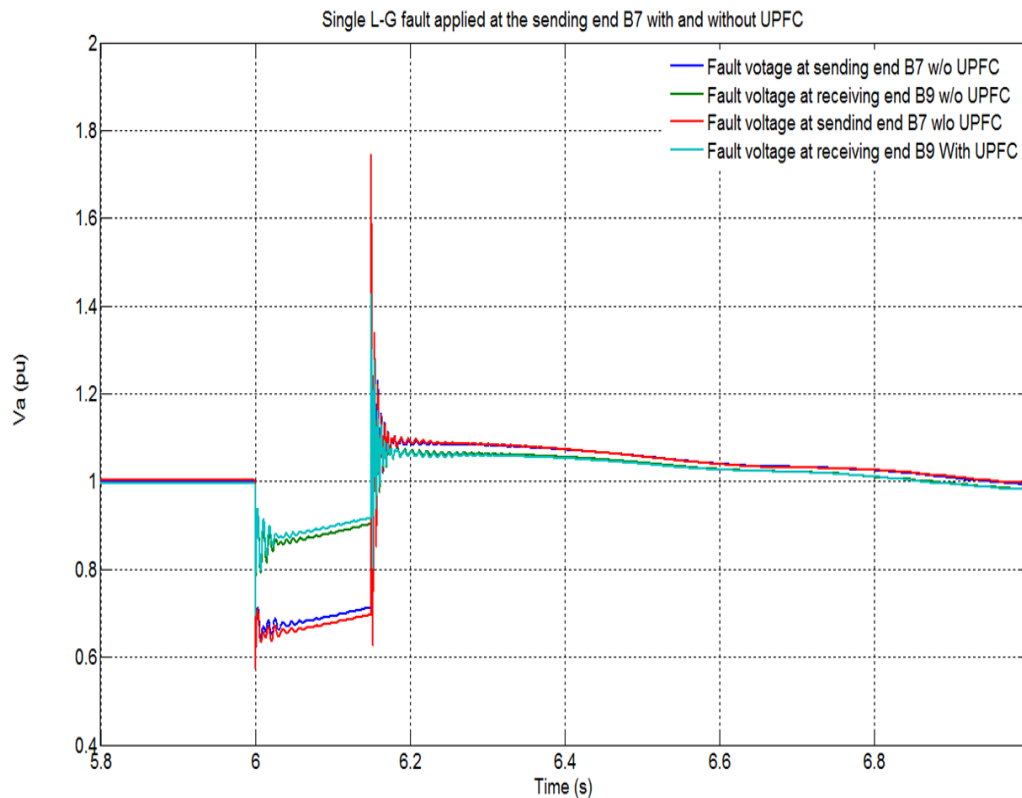
state in roughly 1s. When UPFC is connected; before the fault at bus B7, the steady state voltage is 1 pu. The peak fault voltage is 0.58 pu. During the fault it has a steady state fault of 0.65 pu. It takes 1 s to reach its pre-fault steady state. The peak fault voltage at bus B9 is 0.7 pu. The steady state fault voltage during fault is 0.9 pu. About 1s is required to reaching pre-fault state conditions.

Referring to Figure 6.7a, the pre-fault steady state current is naturally affected by the UPFC as the purpose of the UPFC is to strengthen bus B8. The current at bus B7 is increased by 10 % in the presence of UPFC. The current at bus B9 is larger by about 7 %. The steady state operation of the WSCC test system has been covered in chapter 5.

During the fault period, the fault current at bus B7 does not see any significant difference in the current due to the UPFC. The current at bus B9 is improved by about 10 % lower than the case when the UPFC is disconnected. This improvement results from introducing the UPFC at bus B8 which plays an important role in controlling the transmitted power, which in turn, improves the transmission line current. During the fault period the transmission line current will increase, in this case, the series converter SSSC will inject series voltage to the transmission line with opposite sign. This will cause an increase in the transmission line total reactance of line L1b which results in a decrease in the line current and the transmission power at bus B9. After the fault period, both buses return to their steady state in about 220 ms and this settling time is depending on the controller current gains of the UPFC and will be explained in the next section.



(a) Fault current



(b) Fault voltage

Figure 6.7 Comparing the currents and voltages of WSCC test system at B7 and B9 with UPFC and without UPFC (a) Fault current, (b) Fault Voltage

Referring to Figure 6.7b (as explained in chapter 5), at steady state, UPFC is used to control the voltage at bus B8 and control the power transfer in transmission line L1b and therefore increasing the power performance of the test system. So, we can observe that the bus voltages at B7 and B9 are 1.0 pu prior to the fault. During the fault, buses B7 and B9 experience an improvement in their voltage magnitude when UPFC is connected to B8 by around 10 %. This is because the UPFC will try to keep the voltage at bus B8 within certain limit by injecting reactive power to it which will impact the voltages at the other buses. In addition, the UPFC does have an impact of keeping the bus voltage in the test system within the permissible limit. After the fault period, from simulation results, it can be observed that the post voltage steady state voltage differs from the pre-fault steady voltage by 10% to 20% and takes a long time to reach its normal operation, which is not acceptable in practice. The voltage regulation controller plays an important role, practically, in the post fault period.

The most common issue observed in Figure 6.7 is the oscillations in current and voltage waveforms during and after the fault period. In steady state operation there is usually a low frequency oscillation in the range of 0.2 to 3.0 Hz, this exist due to the interaction between the different power stations and the interconnected transmission lines. This kind of oscillation is known as inter – area oscillations. During the fault condition, the frequency of oscillation may increase in the ranges of few hundreds. The most common control technique used in controlling the UPFC (PI controller) [20] and the size of the DC capacitor may help in damping an oscillatory mode during fault conditions when they are properly tuned. In the following section the effect of the control gains of the PI controller and the DC capacitor size on the oscillation mode are investigated.

The main control in the UPFC is the proportional-integral (PI) controller which is used in the control of DC voltage, AC voltage and power transfer. The basic block diagram for the PI controller is shown in Figure 6.8.

The controller output is given by:

$$K_p \Delta + K_i \int \Delta dt \quad (6.1)$$

where Δ is the error or deviation of actual measured value (PV) from the set-point (SP).

$$\Delta = SP - PV \quad (6.2)$$

A PI controller can be modelled easily in MATLAB (Simulink) using a "flow chart" box involving Laplace operators:

$$C = \frac{G(1 + \tau s)}{\tau s} \quad (6.3)$$

where:

$$G = K_p = \text{proportional gain}$$

$$G / \tau = K_i = \text{integral gain}$$

Setting a value for G is often a trade-off between decreasing overshoot and increasing settling time.

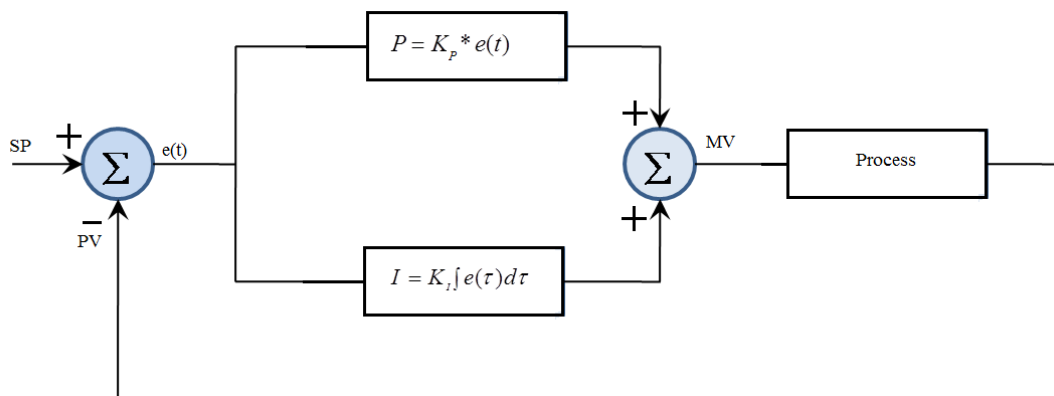


Figure 6.8 Basic block of PI controller

Figure 6.9 shows the three possible control configurations for the UPFC shunt converter employing fundamental frequency switching. Configuration C is used in the UPFC. In this configuration, the voltage response (U_{resp}) signal is compared with the reference

voltage (U_{ref}) plus a voltage contribution to the desired slope of the voltage-current characteristics of the converter. The error signal (U_{error}) goes through a PI regulator that results in the reactive current order (i_{vq-ref}) to be generated by the converter. The voltage regulator function resembles thus that one employed for the UPFC, with control equation given by:

$$U_{resp} = U_{ref} - Slope * i_{vq} \quad (6.4)$$

A positive value of i_{vq} indicates reactive power generation by the UPFC. The current reference is compared to the calculated value (i_{vq}) and another PI regulator forms the reactive current controller. The output of this controller gives the phase-shift angle order (δ_{order}), sent to the firing control Digital Signal Processing (DSP) system of the UPFC.

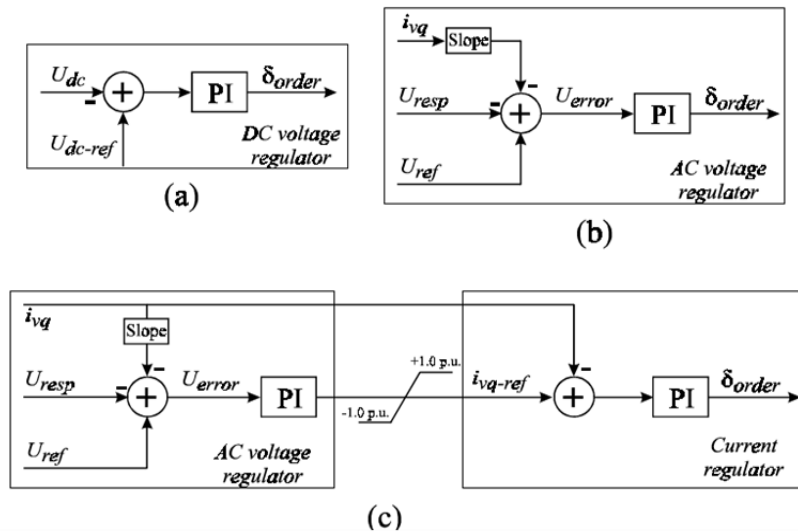


Figure 6.9 Possible control configurations for the UPFC shunt converter employing fundamental frequency switching

Figure 6.10 shows the effect of varying the controller gain K_p on the fault current at bus B7. It clearly shows that especially after the fault period the settling time and the overshoot is increased as a result of increasing K_p . the same will when K_I is increased.

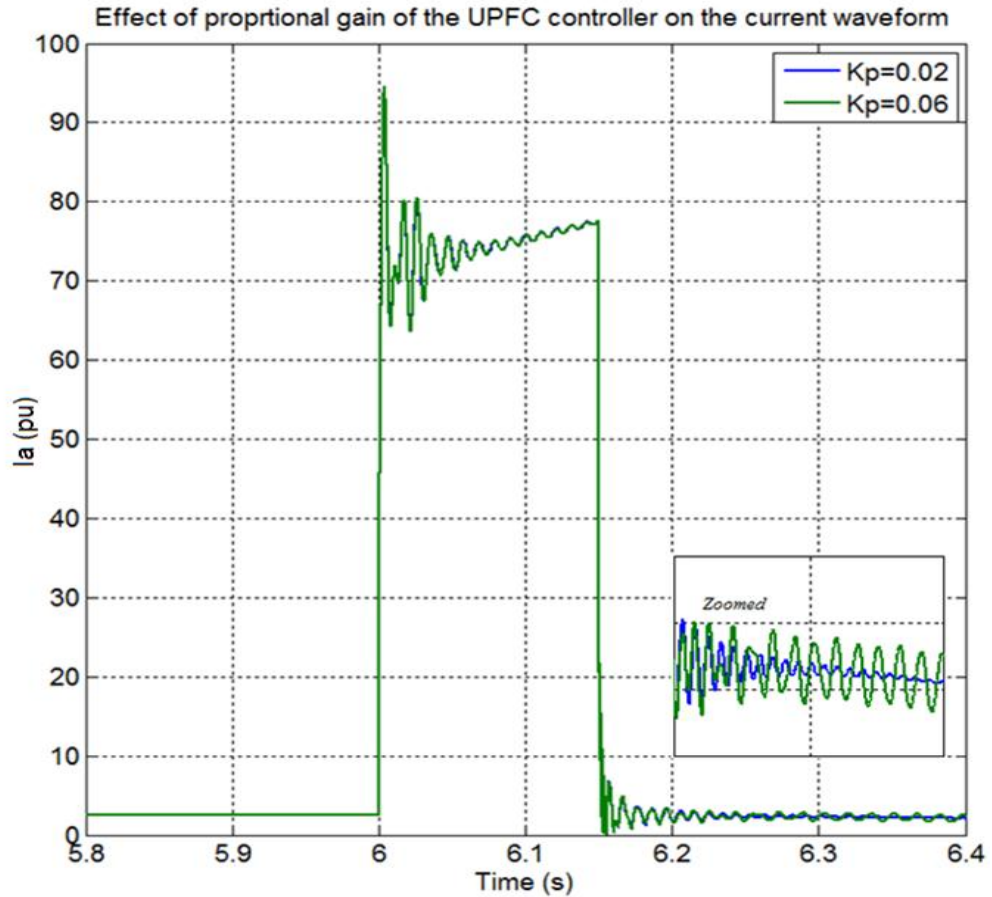


Figure 6.10 Effect of controller gain on the fault current waveform

Ratings of the DC-link capacitor bank of a voltage source converter may have a significant impact on the cost and physical size of a FACTS controller. The capacitor is sized typically 10% of the nominal voltage. In practice, the finite DC capacitance used would result in the formation of ripple voltages which are dependent on the capacitance value and the capacitor current. The UPFC operation in voltage regulation mode (i.e., current and voltage in quadrature) yields the highest ripple current in the capacitor and hence the highest voltage ripple.

The effect of capacitor size on the DC voltage is presented in Figure 6.11. From the figure, we can see that as the capacitor size increases, the ripple in DC voltage during an S-L-G fault is increased. Also, the oscillation in the DC voltage is increased.

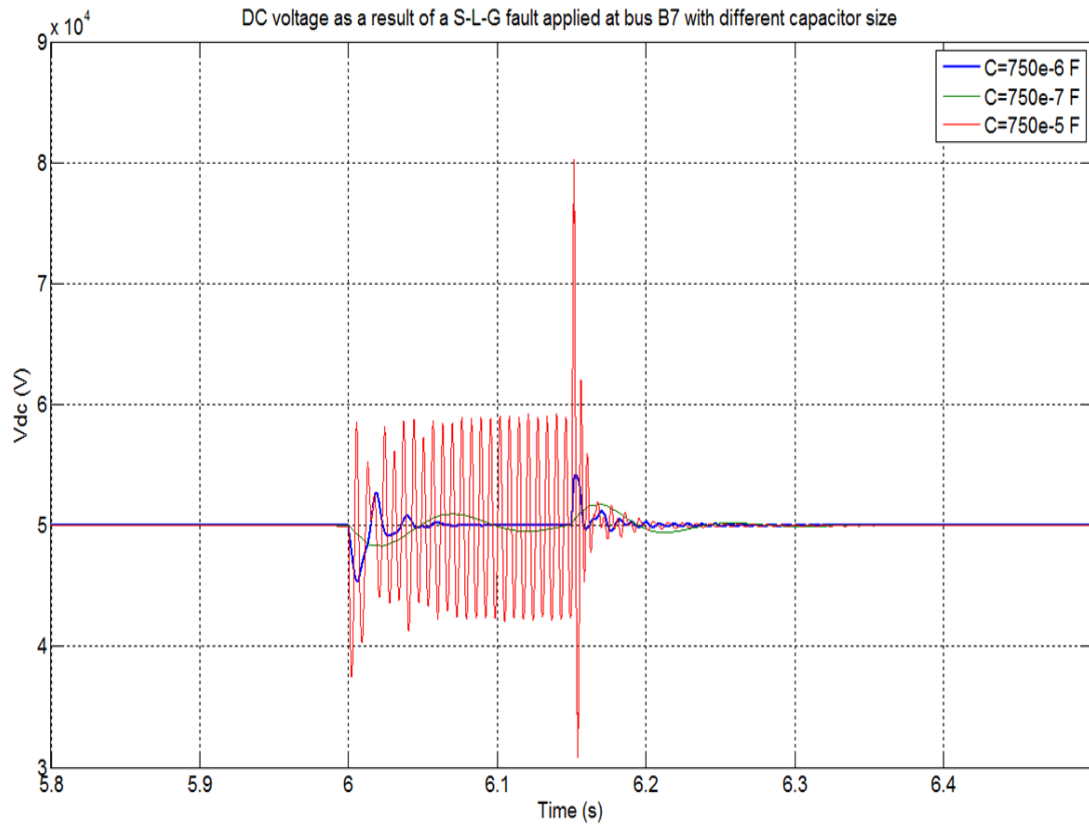


Figure 6.11 Effect of capacitor size on the DC voltage during fault

Figure 6.12 shows the effect of the capacitor size on the voltage at bus B8 as an S-L-G fault applied at bus B7. From the figure we can see that the voltage at bus B8 is increased as the capacitor size of the UPFC is increased.

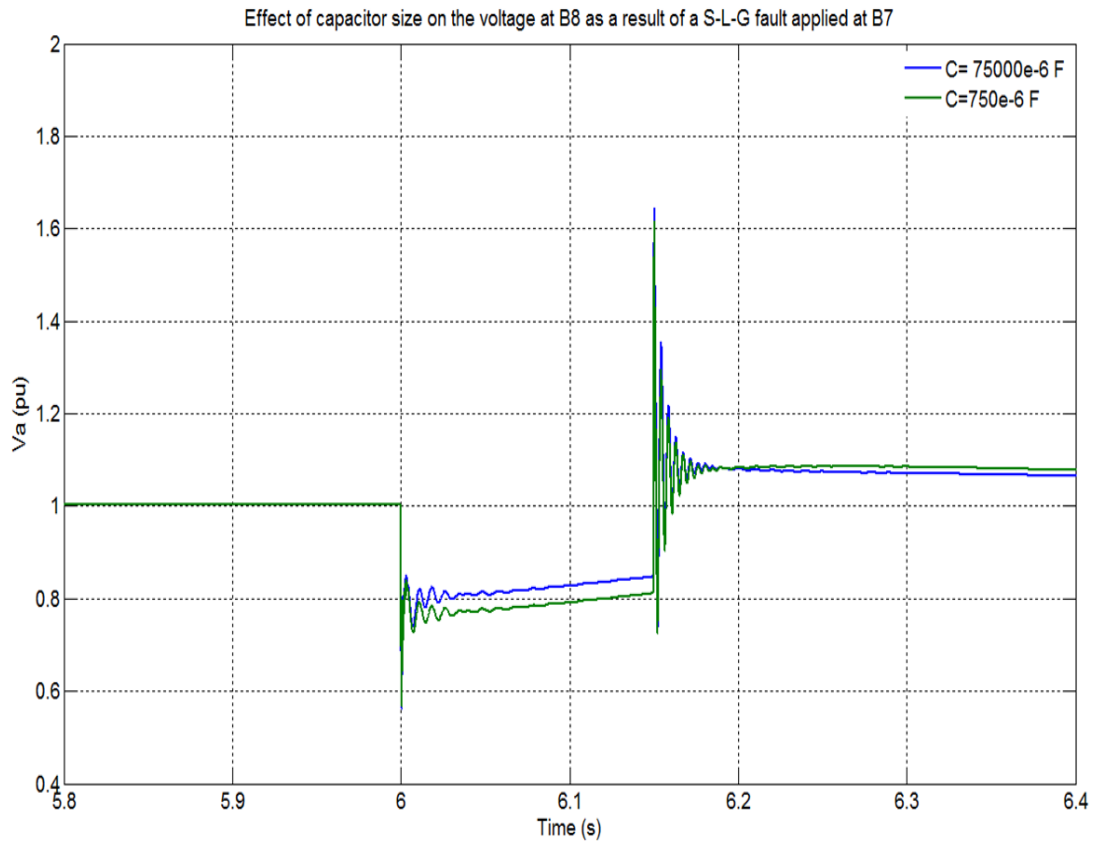


Figure 6.12 Effect of capacitor size on the voltage at B8 as a result of S-L-G fault applied at B7

The effect of capacitor size on the overshoot and settling at bus B8 as a result of an S-L-G fault at bus B7 is shown Figure 6.13.

From the figure, as the capacitor size increases there are slight increase in oscillations, ripples and settling time of the voltage waveform at bus B8. Therefore, by proper selection of the capacitor size, the voltage waveform can be improved even during fault conditions.

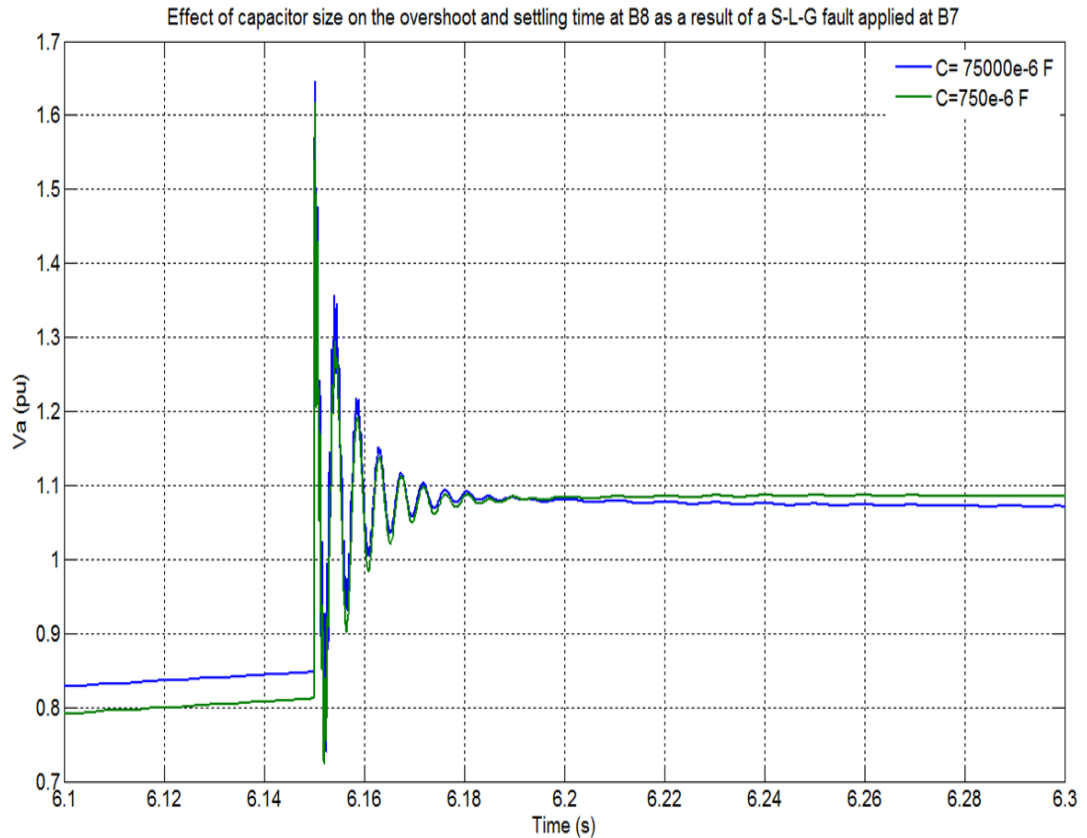


Figure 6.13 Effect of capacitor size on the overshoot and settling time at B8 as a result of S-L-G fault applied at B7

Important aspects

- A UPFC has the capability to improve the voltage profile of the nearest buses even during fault conditions, as well as regulating the active and reactive power of the buses and the lines within specified limits even during the fault conditions.
- During the fault conditions, there can be oscillations at the DC link capacitor and correct sizing is required.
- The larger size of the DC capacitor can improve the bus voltage at which the UPFC is connected and the nearest buses.

- Proper control of the proportional gain K_p and the integral gain K_I of the UPFC controller can improve the settling time and the overshoot of the signal responses after fault duration.
- Proper selection of the DC capacitor can improve the damping oscillations, ripples and the settling time of the system during fault conditions.

6.3.1.2 Simulation B

An S-L-G fault is at bus B7 with UPFC is connected to bus B8 and measuring V, P, Q and I in all other buses.

The simulation results are (shown in Figure 6.14-17).

- a. From the simulation results shown in Figure 6.14, we can see that the steady state voltage of buses B-UPFC, B4, B5, B6, B7, B8 and B9 is 1 pu. During the fault period the steady state fault voltages of all these are; 0.85, 0.90, 0.775, 0.90, 0.625, 0.775 and 0.0.86 pu respectively. After the fault period all test system buses reached post fault steady state in about 1 s with slight oscillations observed.

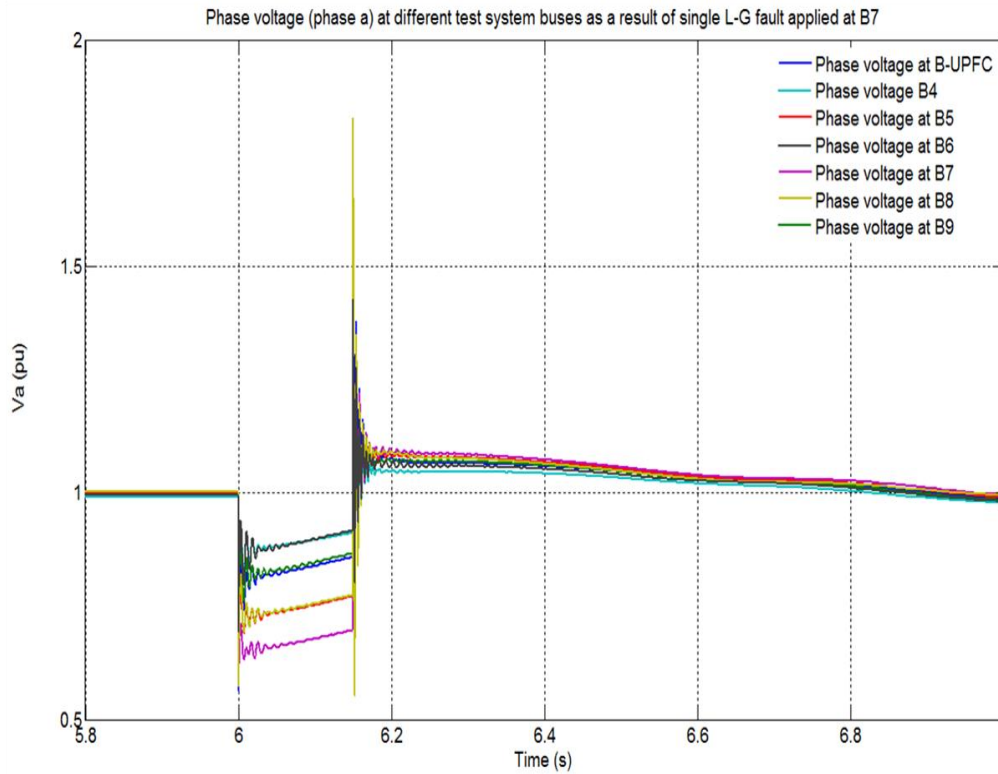


Figure 6.14 Effect of S-L-G fault at bus B7 on the bus voltages of each bus in the test system

- b. In Figure 6.15, the steady state currents of buses B-UPFC, B4, B5, B6, B7, B8 and B9 are: 2.4, 10, 2.7, 22.8, 3.3, 3.3 and 2.3 kA respectively. The fault currents during the fault period are: 16.5, 22.5, 30, 24, 77, 18, 18 and 14 kA. After the fault has been cleared, the settling time at buses B4, B5 and B6 are about 1 s with slight oscillations. Whereas, the settling time at bus B7, B8 and B9 are 220 ms.

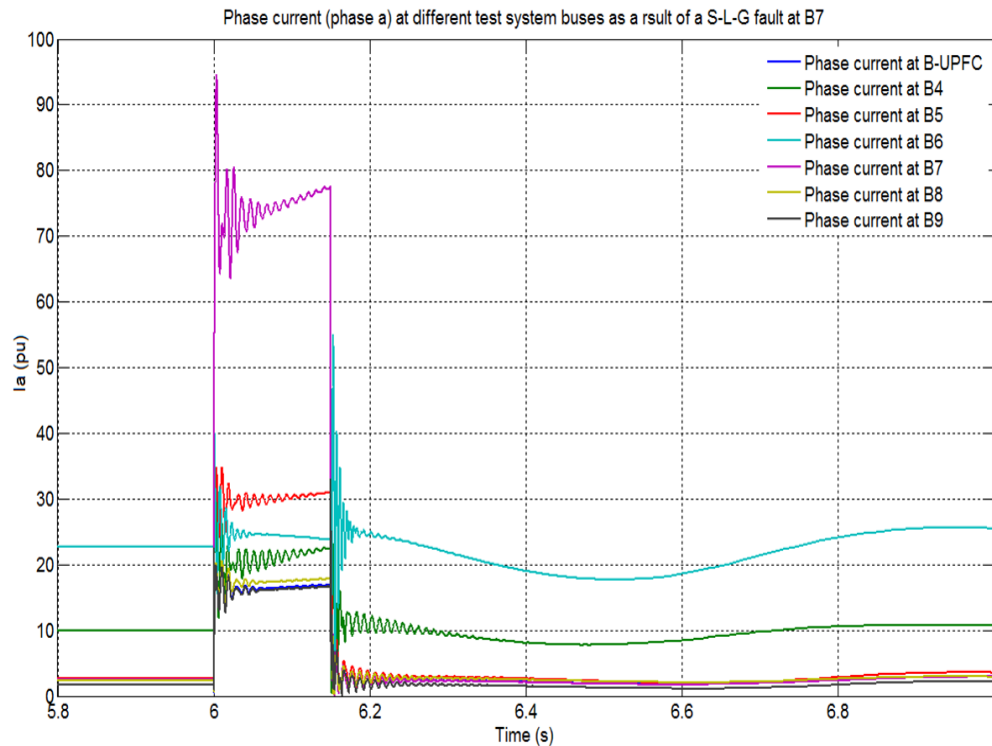


Figure 6.15 Effect of S-L-G fault at bus B7 on the fault current of other buses in the WSCC test system

- c. The variation of the active power of the test system as a result of the S-L-G fault is applied at bus B7 (shown in Figure 6.16). The steady state active power of buses B-UPFC, B4, B5, B6, B7, B8 and B9 are: 223, 1000, 273, 2162, 223,223 and 223 MW respectively. The active power during fault period of all these buses are: 100, 750, -200, 1200, 1000, 100 and -100 MW respectively. . After fault period, buses B7, B8, and B9 reached steady state at 220 ms. Buses B4 and B5 and require about 1s to reach its steady state operation with slight oscillations.

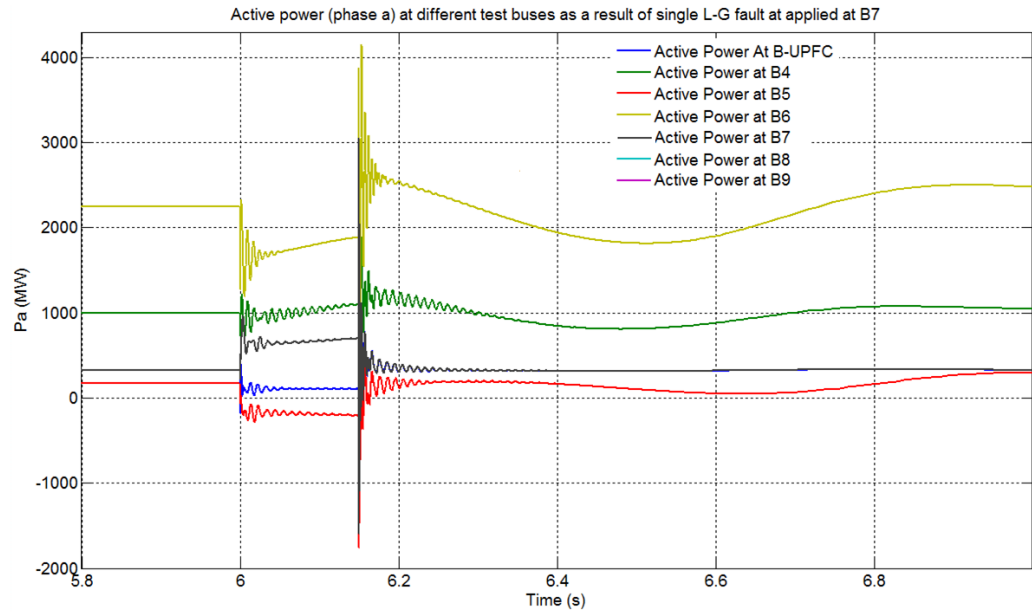


Figure 6.16 Effect of S-L-G fault at bus B7 on the active power of all buses in the test system

- d. The variation of the reactive power is shown in Figure 6.17. The steady state reactive power of buses B-UPFC, B4, B5, B6, B7, B8 and B9 are: 37, -72, 59, 25, 89, 37 and 97 Mvar respectively. The reactive power during the fault period of all these buses are: -250, 600, 0600, -1000, -200, -300 and -400 Mvar. After the fault has been cleared all buses B7, b8, and B9 reached steady state at 220 ms. Buses B4, B5 and B6 requires about 1s to reach steady state operation with slight oscillations.

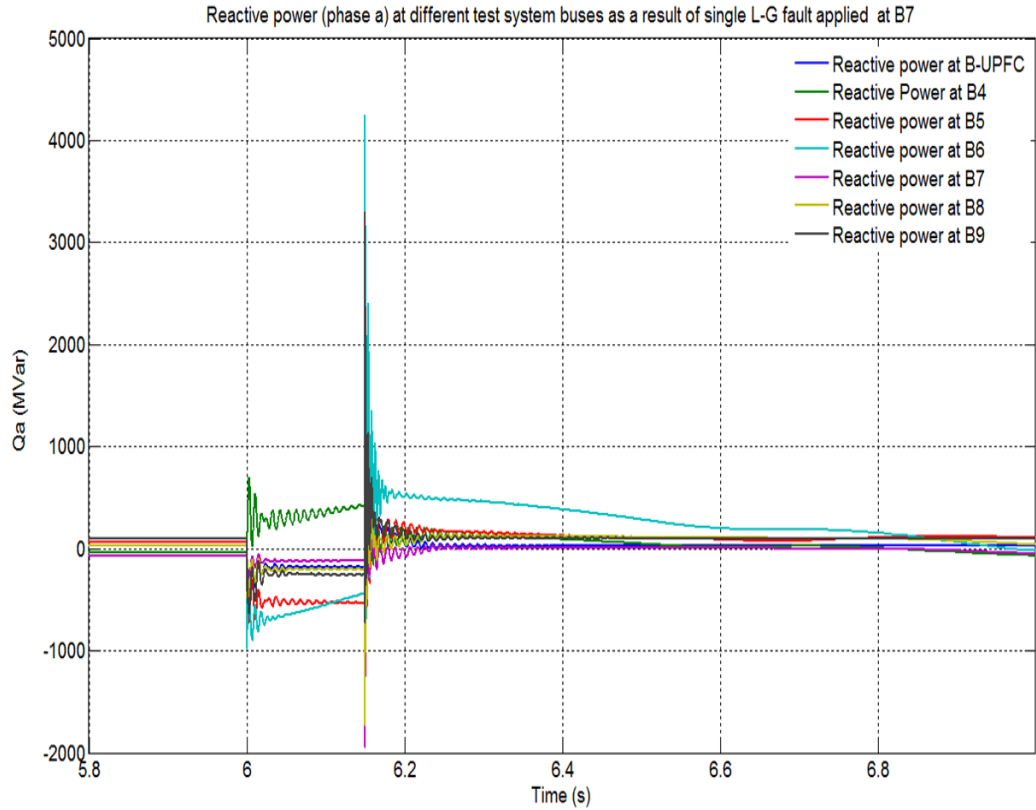


Figure 6.17 Effect of S-L-G fault at bus B7 on the reactive power of other buses in the test system

Before discussing Figures 6.14-17, an explanation is presented to illustrate the relation between the inductive reactance of the transmission line and the line current.

The series inductive reactance of a transmission line depends on both the inductance of the line and the frequency of the power system. Denoting the inductance per unit length as l , the inductive reactance per unit length will be:

$$x_L = j\omega l = j2\pi f l \quad (6.5)$$

where f is the power system frequency. Therefore, the total series inductive reactance of a transmission line can be found X_L as:

$$X_L = x_L * d \quad (6.6)$$

where d is the length of the line.

The inductive reactance at 50 Hz for overhead lines is typically much larger than the resistance of the line so that the transmission line resistance can be neglected. Therefore, for a simple two machine power system, the transmission line current can be calculated as:

$$I = \frac{V_S - V_R}{X_L} \quad (6.7)$$

where I is the transmission line current, V_S sending end voltage, V_R receiving end voltage and X_L is the inductive reactance of the transmission line per unit length.

From Equation 6.7, it is clear that the transmission line current decreases as the inductive reactance of the transmission line increase.

Referring to Figure 6.14, naturally the steady state conditions of the voltage at all buses are 1 pu. During the fault period, the fault voltage is decreased to some extent depending on the distance from the fault location (distances in km is given in Figure 6.5) and on the system configuration. As expected bus B7 is the most affected bus because of the fault that is applied at B7. Bus B9 is less affected as the result of the presence of this in the UPFC path which will try to keep the voltages within the regulation limit and the effective transmission reactance is increased because of the distance from the fault location. The fault voltage at the other buses is decreased depending on how far it is from the fault location. The voltages at buses B4 and B9 are within the permissible voltage level. After the fault period, the settling time for the voltages is about 1 s.

The simulation results shown in Figure 6.15 show the pre-fault steady state of current waveform as described in chapter 5. During the fault period, as expected, the highest fault current is observed at bus B7 where the fault is applied. Buses B-UPFC, B8 and

B9 are less affected because they are in the fault path of the UPFC which will try to compensate the test system by reactive power in order to force the test system to pre-fault conditions. Buses B4, B5 and B6 are not part from the UPFC path and their location is far from the fault location. So, the fault current depending on the effective impedance of the transmission line which is increased by the distance and on the system configuration. It is clear that the UPFC control system plays an important role in controlling the buses B-UPFC, B7, B8 and B9. At buses B4, B5 and B6, the settling and the overshoot are higher because they are not part of the UPFC path. To illustrate the effect of the UPFC on damping power oscillation and decrease the settling time an S-L-G fault is applied at bus B6 with and without UPFC and the current waveform is observed at bus B8 where the UPFC is connected, the result is shown in Figure 6.18. From the figure, it is clear that UPFC improves the overshoot, oscillation and settling time when it is connected to weak bus.

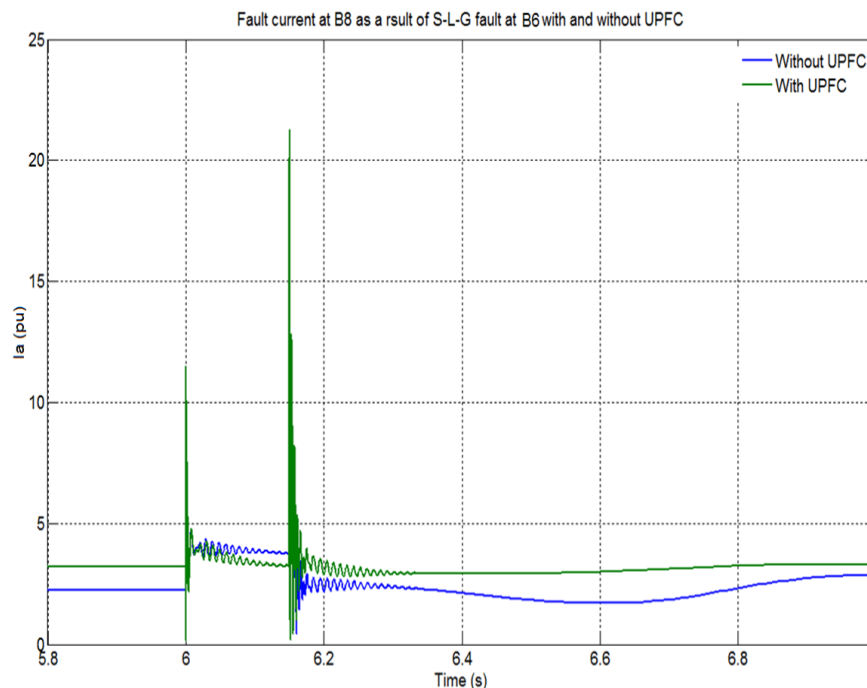


Figure 6.18 The effect of UPFC in damping power system oscillations

The pre-fault active power steady state shown in Figure 5.13 is described in chapter 5. During the fault period, the active power at buses B-UPFC, B5, B6, B7, B8 and B9 are

decreased. There is no significant change in active power at bus B4. The active power at bus B7 is increased as expected. Buses B4, B5 and B6 have higher oscillations and requires more than 1s to reach a steady state compared to buses B-UPFC, B7, B8 and B9 which require 220 ms to reach steady state because they are not part of the UPFC path.

Figure 6.17 shows simulation results in the steady state reactive power before fault as described earlier. During the fault period, the reactive power at all buses are decreased except bus B4 where the reactive power is increased and this is expected because B4 is connected directly to the generation station G1 in which the reactive power will increase as a result of fault. After the fault, an oscillation and a longer settling time in buses B4, B5 and B6 can be seen in the active power signal and they require more than 1s to reach pre-fault conditions.

Important aspects

- Without UPFC, there will be oscillations after the fault is cleared. Therefore it is necessary to have a UPFC at bus B8, the weakest bus to post fault operation
- During the fault period, all the buses were below 0.9 pu voltage. This implies that the UPFC could disconnect from the grid. However, it would be possible to increase the capacitor size of the UPFC, and thereby result in some buses meeting the required regulation limit.
- The buses that are not in the UPFC path do suffer from oscillations in active and reactive power waveforms.

6.3.1.3 Simulation C

In this experiment an S-L-G fault is applied at buses (B4, B5, B6, B7, B7, B8 and B9 respectively) of the test system and measuring; (a) the converter voltage magnitude, (b) UPFC direct current component and (c) the voltage at bus B8 as a result of S-L-G fault applied at other buses.

The simulation results shown in Figure 6.19-21 show the response of the UPFC connected to the weakest bus B8 of the test system when it is subjected to an S-L-G fault at different locations.

- a. The simulation results shown in Figure 6.19 illustrate the effect of the fault position on the UPFC converter voltage magnitude of the UPFC. The steady state converter voltage magnitude of UPFC before the fault is 0.056 pu. During the fault period, the converter magnitude is increased from its steady state value to 0.103 pu. After fault, the oscillation amplitude before reaching steady state is 0.08 pu and the converter voltage magnitude reaches its steady state in time about 1s.

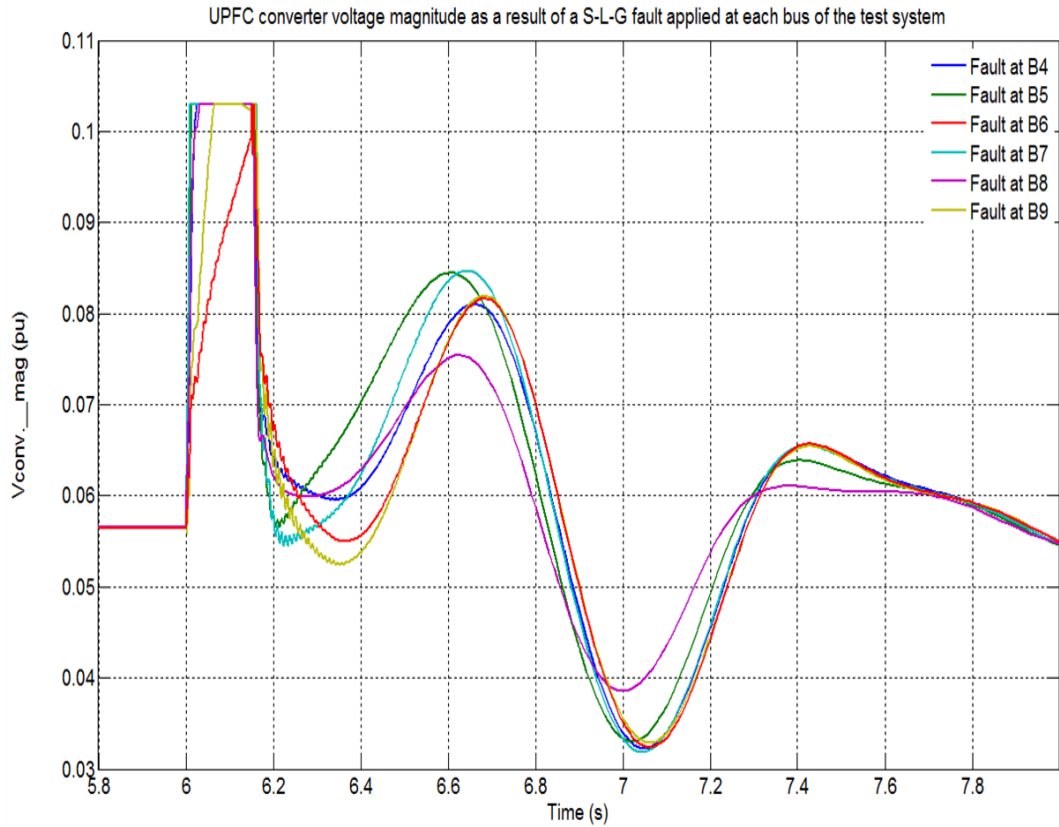


Figure 6.19 UPFC converter voltage magnitudes during fault at different distances

- b. The steady state direct current component of the UPFC is -0.02 pu as shown in Figure 6.20. During the fault period, the steady state UPFC direct current, as a result of fault at buses B4, B5, B6, B7, B8 and B9 are: 0.22 , 0.31 , -0.41 , 0.66 , 0.90 and -0.64 pu. After the fault period, there are slight oscillations in the current signals and require 1 s to reach pre-fault steady state conditions.

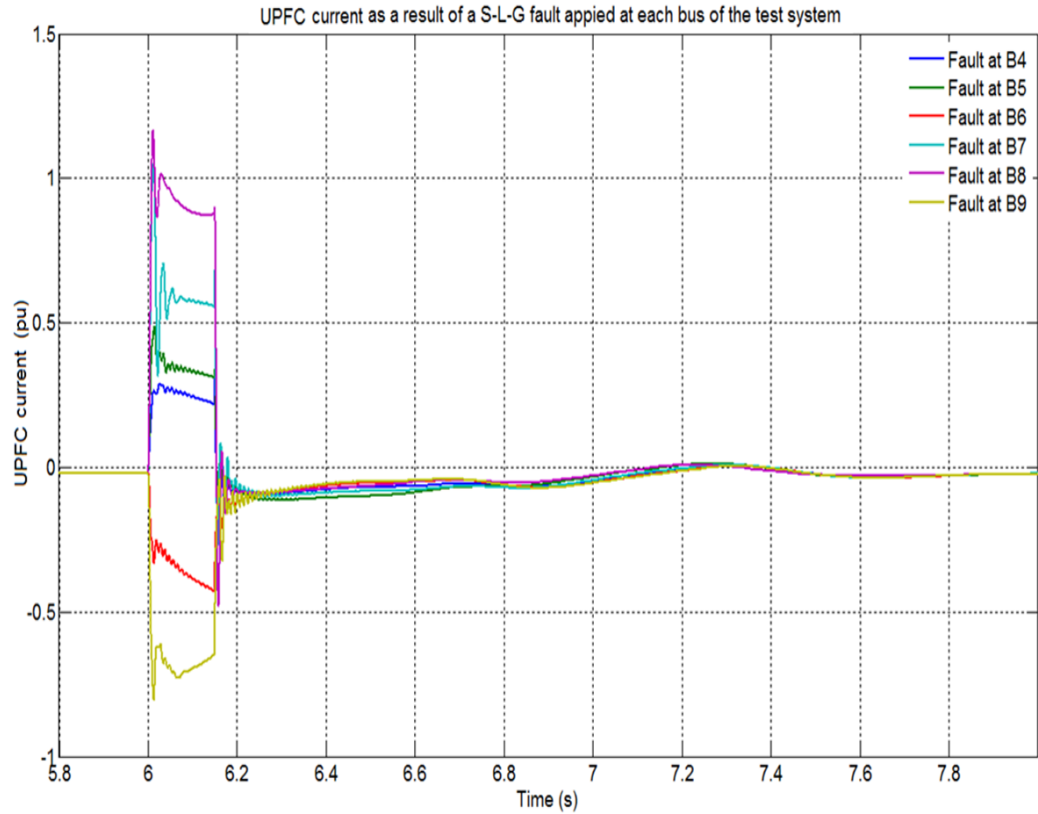


Figure 6.20 UPFC direct current component as a result of an S-L-G fault applied at each bus of the test system

- c. The steady state voltage of the test system is 1 pu as shown in Figure 6.21. During the fault period, the voltage at bus B8 as a result of an S-L-G fault applied at buses B4, B5, B6, B7, B8 and B9 are: 0.859, 0.832, 0.8557, 0.8416, 0.7847, and 0.8369 pu respectively. After the fault, there are slight oscillations and oscillation and the settling time required to reach steady state is about 1s. Table 6.1 Summarizes fault voltages at bus B8 during an S-L-G fault at different distances.

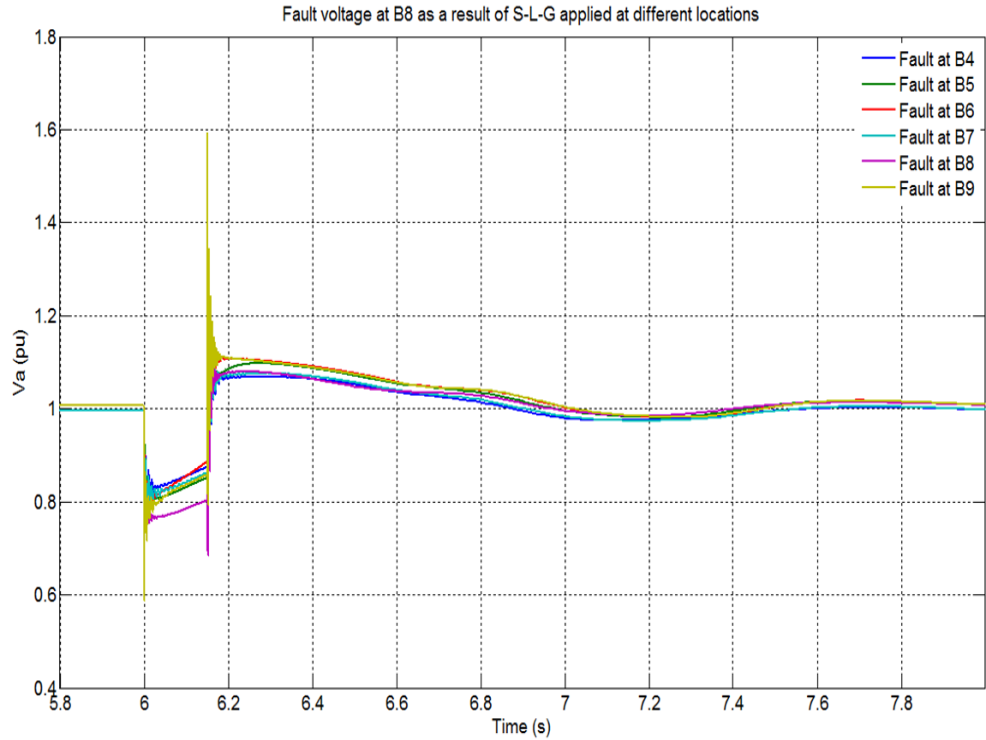


Figure 6.21 Fault voltages at bus B8 an S-L-G fault applied at different locations of test system

Table 6.1 Summarises fault voltages at bus B8 during an S-L-G fault at different distances

	Pre-Fault S. S.	during fault steady state	After fault S. S.	Settling time (s)
B4	1	0.859	1	1
B5	1	0.831	1	1
B6	1	0.8557	1	1
B7	1	0.8416	1	1
B8	1	0.7847	1	1
B9	1	0.8369	1	1

All fault voltages value are in pu.

The steady state value of the UPFC converter voltage magnitude waveform is 0.056 pu as presented in Figure 6.19. During the fault period, the UPFC reacts to control the transmitted power in L1b by injecting series voltage with a magnitude of 0.103 pu in order to increase the transmission line total reactance which results in a decrease in line current and the transmitted power during the fault period. The injected voltage by the UPFC is more than the rated value of the series converter (0.1 pu) and this increase of the injected voltage over the rated value will produce an oscillation in active and reactive power waveforms. In addition to this, there are as oscillations of the voltage after the fault has been cleared with a maximum peak of 0.085 pu and this value can be taken as an indicator of the rated value of the UPFC after the fault period.

Referring to Figure 6.20, during the fault period, the UPFC fault current is increased depending on how far the fault position is from the UPFC. The UPFC fault current is increased at buses B4, B5, B7 and B8 with the highest value observed at bus B8 where the UPFC was connected with the value of about 1.0 pu. These UPFC fault currents are very high compared with the rating of the UPFC and we have to avoid this as it results to increase in the size of the UPFC converter, which, in turn, will increase the cost and the physical size. The UPFC fault currents at buses B6 and B9 are decreased during the fault period as a result of the UPFC converter phase angle reaching about 150° [21] as shown in Figure 6.22, which shows that the transient stability is less at these buses. Naturally, there is a slight oscillation after the fault period and the time required to reach pre-fault steady state is about 1s.

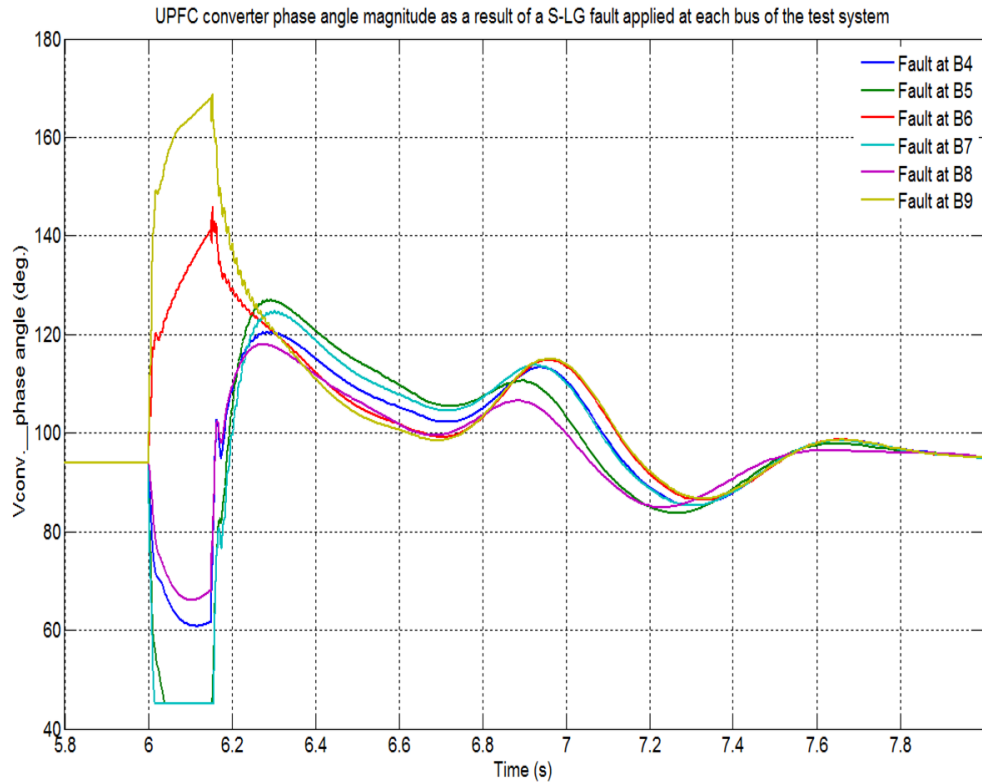


Figure 6.22 UPFC converter phase angle during fault conditions

Referring to Figure 6.21, the steady state fault voltages at the weakest bus B8 as a result of the S-L-G fault applied at different buses of the test system are 1.0 pu. During the fault period, the fault voltages at all buses are decreased with the highest value at bus B8 (80 %) of its steady state value. All buses are below the regulation limit with slight oscillations during the fault and high spike at the end of the fault. The operation of the UPFC during the fault can help in damping the oscillations but due to the high drop in voltage during the fault and also high currents, it is necessary to disconnect the UPFC from the grid during the fault period. The high spike at the end of the fault period is due to the loss of synchronization of the UPFC with the grid as shown in Figure 6.23 and can be corrected in practice. After the fault period, the UPFC can help the grid to regain its steady state very quickly.

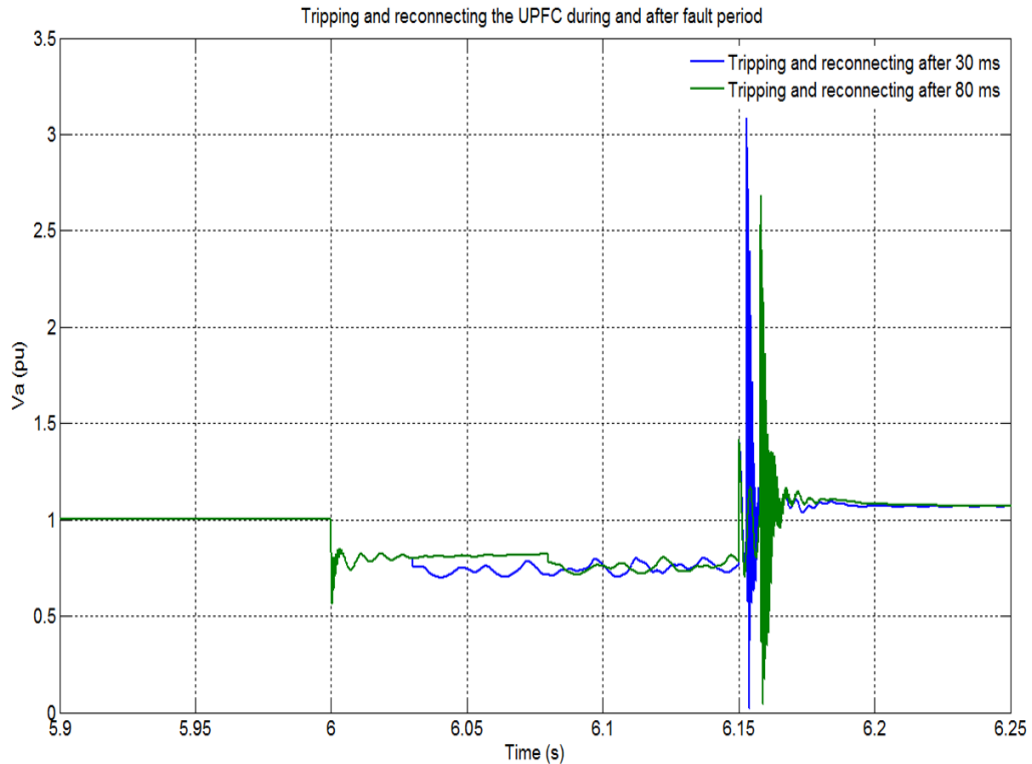


Figure 6.23 Tripping and reconnecting the UPFC during fault period

Important aspects

- The operation of the UPFC under S-L-G fault conditions can help in selecting the ratings voltages of the converter.
- The magnitude of the phase angle of the UPFC during fault conditions can be taken as an indicator for voltage instability. The transient stability is less when the converter phase angle reaches about 150° .
- UPFC is used to improve the voltage at the weakest bus (B8) in the test system, therefore, during fault conditions it will try to keep the voltage at bus B8 within the pre-defined limit. However, this is not sufficient as it is at a high price for capacitor size.
- During fault conditions, the UPFC is unable to meet the G59 voltage regulation requirement and hence it could be disconnected from the grid.
- UPFC is an effective tool in recovery from fault conditions (post fault period).

- The effect of the fault condition in another bus in the test system on the operation of the UPFC is also pronounced. The bus voltage during fault period drops below the regulation limit.

6.4 Double Line-to-Ground and Line-to-Line faults

Identification of power system faults has been dealt with by various researchers [22-24]. They found that the severity level of these faults on the power system is high in the case of D-L-G and L-L faults. S-L-G is less severing on the power system even though it sometimes produces higher fault current compared with the others. In previous sections, detailed explanation and simulation has been given illustrating the effect of an S-L-G fault on the operation of the UPFC converter. It was found that due to high currents and voltage drops below the regulation during the fault period, the UPFC could be disconnected from the grid. Based on this, there is no reason to discuss the D-L-G and L-L faults in details in relation to the effect of these faults on the UPFC converter because we already know that the UPFC should be disconnected from the grid during the fault period.

In this section, the voltages and currents of the WSCC test system used in previous section are measured in all buses of the test system as a result of a D-L-G and L-L faults applied at bus B7.

6.4.1 D-L-G fault

A D-L-G fault which occurs between two lines also commonly occurs due to storm damage. This type of fault is the second most commonly occurring fault so consequently the severity will be higher on the power system components. The results for D-L-G fault are shown in Figure 6.24-25.

- a. From the simulation results shown in Figure 6.24, it shows that the steady state voltage of buses B4, B5, B6, B7, B8 and B9 is 1 pu. During the fault period the steady state fault voltages of all these are; 0.67, 0.50, 0.775, 0.36, 0.050 and 0.76 pu respectively. After the fault period all test system buses reached post fault steady state in about 1 s with slight oscillations observed.

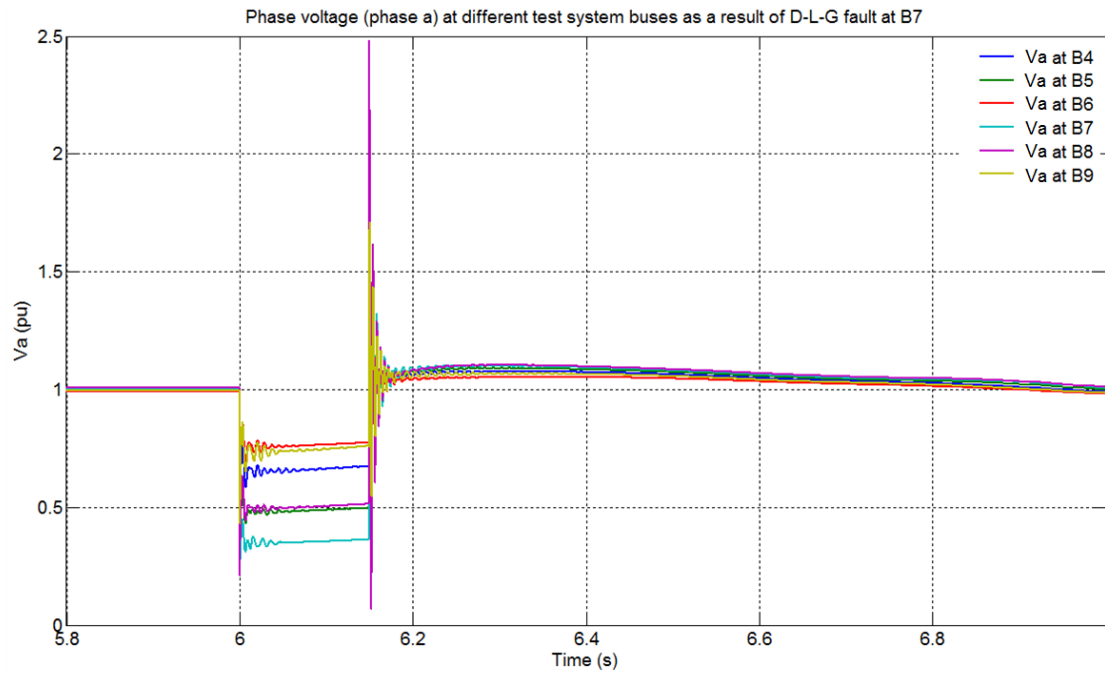


Figure 6.24 Effect of D-L-G fault at bus B7 on the bus voltages of each bus in the test system

- b. In Figure 6.25, the steady state currents of buses B4, B5, B6, B7, B8 and B9 are: 10, 2.7, 22.8, 3.3, 3.3 and 2.3 kA respectively. The fault current during the fault period are: 24, 35, 22, 72, 17 and 17.5 kA. After the fault has been cleared, the settling time at buses B4, B5 and B6 are about 1 s with slight oscillations. whereas, the settling time at bus B7, B8 and B9 is 220 ms.

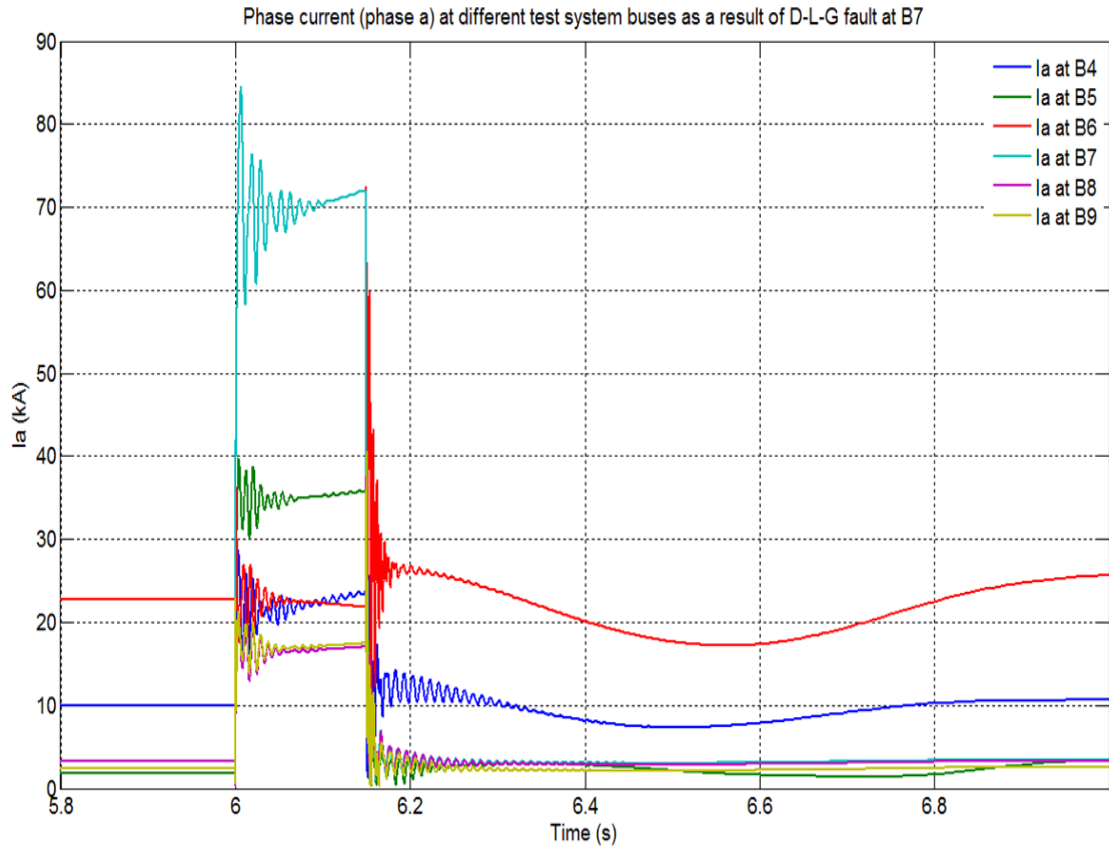


Figure 6.25 Effect of D-L-G fault at bus B7 on the fault current of other buses in the test system

6.4.2 L-L Faults

A line-to-line fault is generally caused by ionization of air, or when lines come into physical contact, for example due to a broken insulator. The results for L-L fault are shown in Figure 6.26-27.

- a. From the simulation results shown in Figure 6.26, that the steady state voltage of buses B4, B5, B6, B7, B8 and B9 is 1 pu. During the fault period the steady state fault voltages of all these are; 0.78, 0.85, 0.85, 0.5, 0.65 and 0.85 pu respectively. After fault period all test system buses reached post fault steady state in about 1 s with slight oscillations observed.

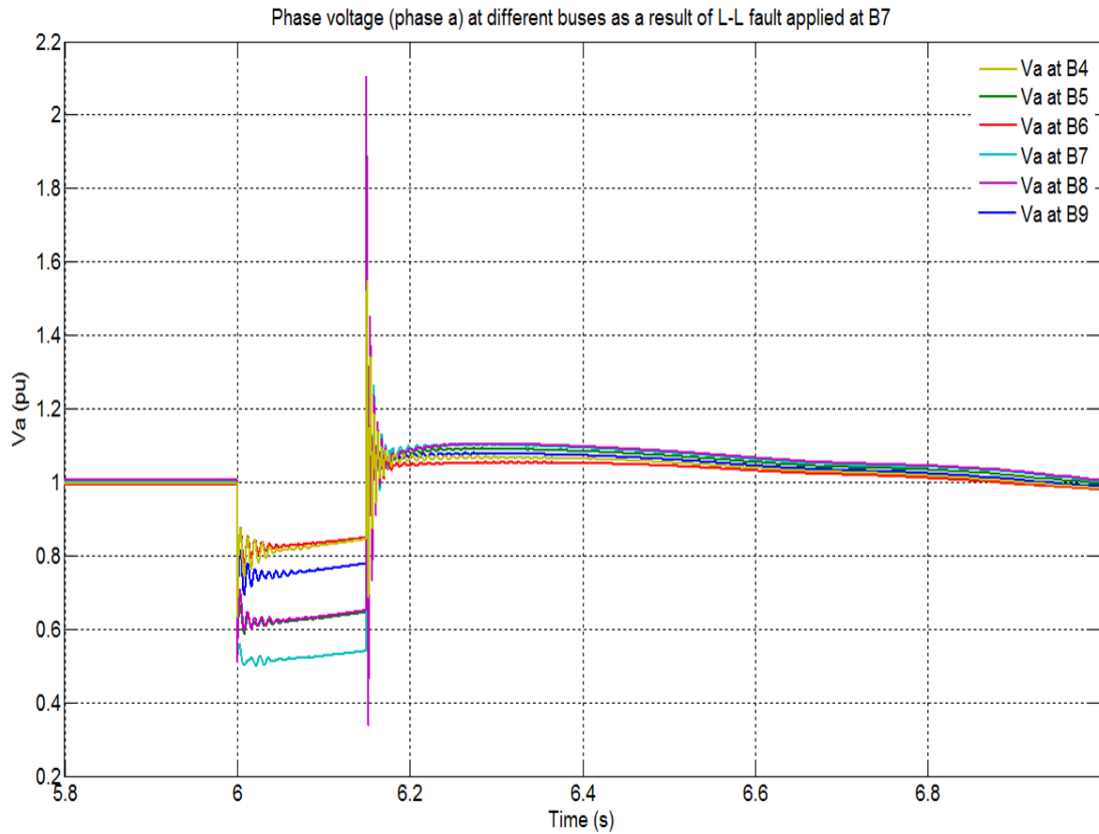


Figure 6.26 Effect of L-L fault at bus B7 on the bus voltages of each bus in the test system

- b. In Figure 6.27, the steady state currents of buses B4, B5, B6, B7, B8 and B9 are: 10, 2.7, 22.8, 3.3, 3.3 and 2.3 kA respectively. The fault currents during the fault period are: 25, 32, 15, 60, 15, and 16 kA. After the fault has been cleared, the settling time at buses B4, B5 and B6 are about 1 s with slight oscillations. whereas, the settling time at bus B7, B8 and B9 are 220 ms.

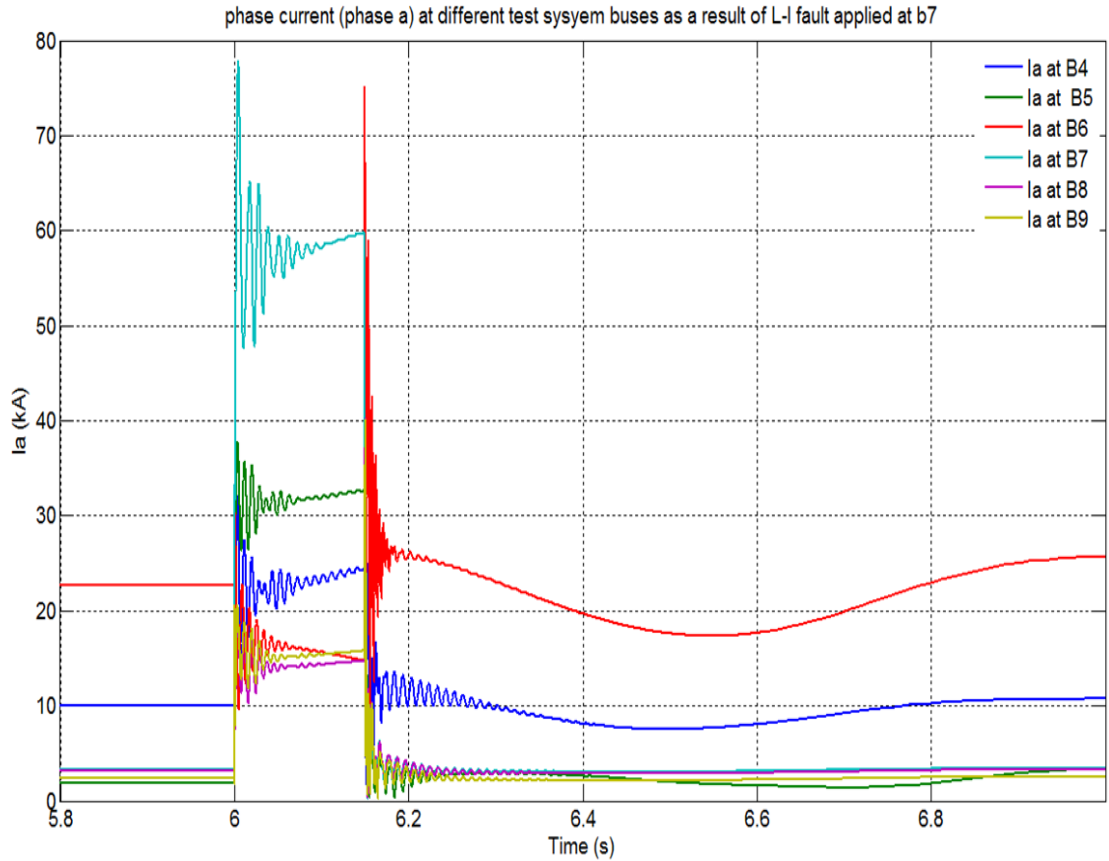


Figure 6.27 Effect of L-L fault at bus B7 on the fault current of other buses in the test system

Referring to Figure 6.24-27, the fault voltages decrease depending on how far the bus is from the fault location with the highest fault value (more than 60 % in case of D-L-G fault and about 50 % in case of L-L faults), when the fault near to the UPFC, which is connected to bus B8. The fault currents increase as the distance between the bus and fault position increase. The highest fault current is measured at bus B7 (about 20 times the steady state current) in the case of D-L-G fault.

Important aspects

- The voltage drops during D-L-G faults to more than 60 % in the case of D-L-G fault and 50 % in case of L-L fault at the fault location with a very high current.

- The UPFC is an effective tool in damping power oscillation, minimizing the settling time and overshoots during recovering from fault conditions. It is more effective on the buses nearest to it.
- Due to the higher voltage drop and higher currents during the test, the UPFC should be disconnected from the grid during all D-L-G and L-L faults.

6.5 Summary

This chapter focuses on the effect of unsymmetrical fault types and position on the operation of the UPFC controller in accordance to the G59 protection, stability and reliability regulations. The simulation result shows that;

- UPFC has the capability to improve the voltage profile to the nearest buses even during fault conditions, as well as regulating the active and reactive power of the buses and the lines within specified limits even during the fault conditions. In addition, UPFC improves the overall performance of the test system during and after fault conditions.
- The size of the DC capacitor can improve the bus voltage at which the UPFC is connected and the nearest buses. Correct capacitor size helps in reducing power damping oscillation, ripples and the settling time of the system during fault conditions.
- The proper control of the UPFC control algorithm (i.e. AC voltage control, current control and DC voltage control loops) can improve the test system performance after fault duration.
- The operation of the UPFC under unsymmetrical fault conditions can help in selecting the ratings voltages and currents of the converter.

- During the unsymmetrical fault period, all the buses were suffering from high currents and low voltages below the G59 protection, stability and reliability regulations. This implies that the UPFC could disconnect from the grid. However, it would be possible to increase the capacitor size of the UPFC and thereby result in some buses meeting the required regulation limit, but this will increase the cost of the UPFC which is already high.

6.6 References

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7: CONCLUSIONS AND RECOMMENDATIONS

This chapter provides the conclusions of the work and some suggestions for future research related to the operation of the UPFC converter under unsymmetrical fault type and positions and how to alleviate the voltage stability problems.

7.1 Conclusion

Static voltage instability is mainly associated with reactive power imbalance. Reactive power increase at the bus that receives power from the system can limit the loadability of that bus. If the reactive power reaches its limit, the system will approach the maximum loading point or voltage collapse point. In this thesis, a new static voltage stability index the *LSZ*, related to the voltage drop in the critical bus was proposed and investigated (in chapter 3). It takes into consideration all factors affecting the power system transfer capability i.e. the transmission line impedance (R, X), the voltage (V_s, V_r) and the phase angle. The proposed index determines the maximum load that is possible to be connected to a bus in order to maintain a voltage stability margin before the system suffers from voltage collapse. In order to investigate the effectiveness of the proposed index, IEEE 14 bus reliability test system and WSCC 3-machine, 9-bus test system was used. The simulation result detects clearly the stressed condition of the lines, identifies with a degree of accuracy the weakest buses prone to voltage collapse and determines the static stability margin of the power to work in safe operation.

The power system is a typical large dynamic system and its dynamic behaviour has great influence on the voltage stability. Therefore, in order to gain more realistic results it is necessary to take the full dynamic system model into account. A new method for dynamic voltage stability study is introduced in chapter 4. In this method, the

interactions between properly defined input and output variables of MIMO transfer function that affect the dynamic voltage stability are analysed based on the singular value decomposition at different frequency modes of operation. The elements of the input singular vectors indicate the impact of the input variables on the output variables and the output singular vectors can be used to evaluate the influence of voltage stability on the selected buses. Moreover, the input singular vector can be used for choosing the most suitable control action to improve voltage stability, and the output singular vector can provide information about the weakest buses that is affected by voltage stability. A typical WSCC 3-machine, 9-bus test power system is used to validate this technique and the results were presented. The simulation results show that the application of singular value decomposition and their associated output and input singular vectors based on the MIMO transfer function identified the critical modes (weakest buses) of the test system and the suitable control action (compensation) to prevent the test system from voltage collapse. The most suitable position for control action is the weakest bus. The results agree with that obtained by the static voltage stability analysis.

The effect of the dynamic load on critical modes and voltage stability margin was also studied. The results show that there is an effect of the dynamic load model on the critical mode and voltage stability margin but these effects did not change the position of the critical mode (weakest buses) and their associated control signals. In addition, there was a noticeable change in the voltage level which appeared clearly.

The effect of unsymmetrical fault types and position on the operation of the UPFC converter in accordance to the G59 protection, stability and reliability regulations is presented in chapter 6. The main conclusion is to disconnect the UPFC from the grid during the fault period because all buses of the test system suffer from high currents and low voltages below the G59 protection, stability and reliability regulations even the

fault is accord at another buses of the system. However, the simulation results show the following improvement in the test system during the fault period when the UPFC is still connected:

- UPFC has the capability to improve the voltage profile to the nearest buses even during fault conditions as well as regulating the active and reactive power of the buses and the lines within specified limits even during the fault conditions. In addition, UPFC improves the overall performance of the test system during and after fault conditions.
- The size of the DC capacitor can improve the bus voltage at which the UPFC is connected and the nearest buses. Correct capacitor size helps in reducing power oscillations damping, ripples and the settling time of the system during fault and after fault conditions. Although, it would be possible to increase the capacitor size of the UPFC, and thereby result in some buses meeting the required regulation limit but this will increase the cost of the UPFC which is already high.
- The proper control of the UPFC control algorithm (i.e. AC voltage control, current control and DC voltage control loops) can improve the test system performance during and after fault duration.
- The operation of the UPFC under unsymmetrical fault conditions can help in selecting the ratings voltages and currents of the UPFC converter.
- The effect of the fault condition in another bus in the test system on the operation of the UPFC is also pronounced. The bus voltage during fault period drops below the regulation limit.

7.2 Contribution to knowledge

The following are the main contributions to knowledge made in this thesis:

- The proposed line stability index *LSZ* can provide accurate information regarding the weakest bus and the weakest line that prone to voltage collapse in the power system.
- The application of singular value decomposition to the well-defined MIMO transfer function can provide information about the weakest buses that affect the power system stability.
- The unsymmetrical fault types and positions have a great effect on the operation of the UPFC controller even when the fault is applied at a long distance from the controller.
- Correct capacitor size and proper control algorithm of the UPFC can improve the power system performance during and after the fault condition when UPFC is in operation.

7.3 Recommendation for future work

- Based on MIMO systems and the singular value decomposition, the interaction among the dynamic voltage stability controllers and controller design for different frequencies and the most suitable control loop could be analysed further by means of Relative Gain Array [1, 2].
- The effect of various models for the loads in the system, Power system stabilizer, Automatic Voltage Regulator and On-Load Tap Changer on the critical modes of the MIMO system can be taken into account

- From the FACTS view point, future prospects are mostly dependable on a number of practical applications of the FACTS controllers. Expecting increased numbers of their installations, raised concern appears within their co-ordination in overall planning and operational procedures. Systems with several FACTS devices are to be analysed. Possible overlapping or interactions between control systems could be investigated.
- An advanced approach is needed in determination of the parameters that belong to each individual proportional-integral regulations. In this case, for each operating mode of the UPFC, different sets of gains and time constants are needed. A more robust solution is to be sought, which could be effective for the wider spectrum of the UPFC operation.
- Fault detection, advanced monitoring, analysis, control and communication facilities are the basic concept of Smart Grid which can play a very important role for the optimal functioning of the UPFC controller. Fast and accurate algorithms for fault detection applied to the control of the UPFC controllers, are necessary.
- The future work should include the design of a control system that allows the UPFC to operate reliably under unbalanced power system fault conditions.
- Green power, sustainable, affordable and economic developments are the multi-dimensional benefits associated with wind energy. As a result, wind turbine installation is increasing rapidly all over the world. In some power system networks, wind power penetration is significantly high and the performance of wind turbine has great effect on power system operation, stability and control. The operation of wind turbines during a power system faults or any external disturbances would affect power system operation, stability and control. The

operation of some existing wind turbines are still dependent on fixed speed induction generators, the effects of capacitor bank on such generators could be analysed and investigated in more detail.

7.4 References

- [1] Fatehi, A.; Shariati, A.; “Automatic pairing of MIMO plants using normalized RGA,” *Mediterranean Conference on Control & Automation, MED '07*. pp.1-6, June 2007.
- [2] Li-Jun Cai; Erlich, E.; “Identification of the Interactions among the Power System Dynamic Voltage Stability Controllers using Relative Gain Array,” *Power Systems Conference and Exposition, (PSCE '06). IEEE PES* , pp.970-977, Nov. 2006.

APPENDIX A

A.1 List of Author Publications

Following are the publications in conjunction with the author during his PhD candidacy.

Journal Papers:

- [1] **Jalboub**, M. K.; Rajamani; H. S.; Readle; J.C.; Abd-Alhameed; R. A.; Ihal; A. M.; , “Weakest bus identification for optimal location for FACTS systems in multi-machine power network,” *Int. J. Power and Energy Conversion*, Vol. 3, Nos. 1/2, pp. 127-142, 2012.
- [2] **Jalboub**, M.K.; Rajamani, H.S.; Abd-Alhameed, R.A.; Ihal, A.M.; , “Weakest Bus Identification Based on Modal Analysis and Singular Value Decomposition Techniques,” *Iraqi Journal for Electrical and Electronic Engineering* vol.2, no.2, pp. 157-162, 2011.

Conference Papers

- [1] **Jalboub**, M. K.; Rajamani; H. S.; Readle; J.C.; Abd-Alhameed; R. A.; Ihal; A. M.; , “ Modelling of Two-level, Multi-Pulse Voltage Source Converter for FACTS Systems,” International Conference and Exhibition on Green Energy & Sustainability for Arid Regions & Mediterranean countries (ICEGES 2009), Jordan, Nov. 2009.
- [2] **Jalboub**, M. K.; Rajamani; H. S.; Liang, D. T. W.; Abd-Alhameed; R. A.; Ihal; A. M.; “Investigation of Voltage Stability Indices to Identify Weakest Bus),” 6th International ICST Conference on Mobile Multimedia Communications, EERT-3, Lisbon, Portugal, 6-8 Sept.2010, Paper No.7, pp.1-8, ISBN: 978-963-9799-98-1.
- [3] **Jalboub**, M. K.; Rajamani; H. S.; Ihal; A. M.; Amer, A.; , “Static Synchronous Series Compensator to Improve Power Oscillation Damping,” the Libyan Arab International Conference on Electrical and Electronic Engineering (LAICEEE-2010), Tripoli, October 23-26, 2010.
- [4] **Jalboub**, M.K.; Rajamani, H.S.; Abd-Alhameed, R.A.; Ihal, A.M.; , "Weakest bus identification based on modal analysis and Singular Value Decomposition techniques," *Energy, Power and Control (EPC-IQ)*, 2010 1st International Conference on , vol., no., pp.351-356, Iraq, Dec. 2010
- [5] **Jalboub**, M.K.; Ihal, A.M.; Rajamani, H.S.; Abd-Alhameed, R.A.; , “Determination of static voltage stability-margin of the power system prior to voltage collapse,” *Systems, Signals and Devices (SSD)*, 2011 8th International Multi-Conference on , vol., no., pp.1-6, 22-25 March 2011.

APPENDIX B

Voltage, current, active and reactive power measurements

If phase-to-ground voltages chosen to be measure in per unit, the MATLAB measurement block converts the measured voltages based on peak value of nominal phase-to-ground voltage:

$$V_{abc}(pu) = \frac{V_{phasetogrand}(V)}{V_{base}(V)} \quad (B.1)$$

where:

$$V_{base}(V) = \frac{V_{nom}(V_{rms})}{\sqrt{3}} * \sqrt{2} \quad (B.2)$$

If phase-to-phase voltages chosen to measure in per unit, the MATLAB measurement block converts the measured voltages based on peak value of nominal phase-to-phase voltage:

$$V_{abc}(pu) = \frac{V_{phasetophase}(V)}{V_{base}(V)} \quad (B.3)$$

where:

$$V_{base}(V) = V_{nom}(V_{rms}) * \sqrt{2} \quad (B.4)$$

If currents chosen to measure in per unit (?), the MATLAB measurement block converts the measured currents based on the peak value of the nominal current:

$$I_{abc}(pu) = \frac{I_{abc}(A)}{I_{base}(V)} \quad (B.5)$$

where

$$I_{base}(pu) = \frac{P_{base}(VA)}{\frac{V_{nom}(V_{rms})}{\sqrt{3}} * \sqrt{2}} \quad (B.6)$$

V_{nom} and P_{base} are the nominal and base voltages of the power system.

$$P = \int_{t-T}^t V(\omega t).I(\omega t)dt \quad (B.7)$$

$$Q = \int_{t-T}^t V(\omega t).I\left(\omega t - \frac{\pi}{2}\right)dt \quad (B.8)$$

Appendices

where $T = 1/f$ (fundamental frequency).