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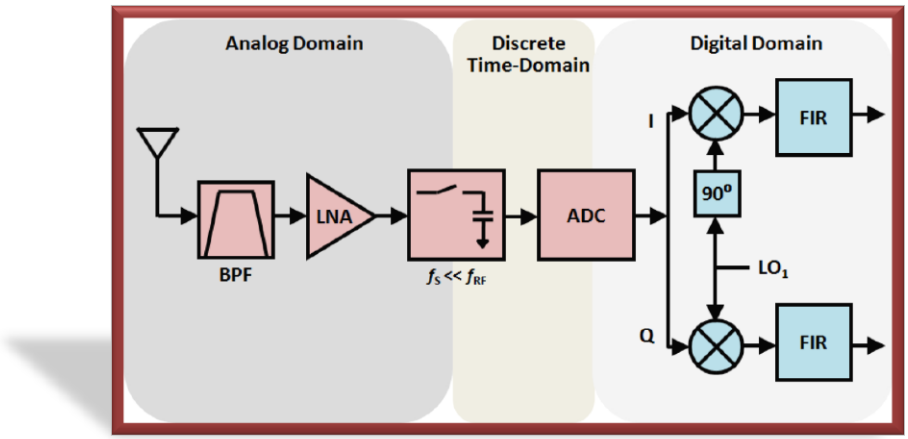
Characterization and Modelling of Software Defined Radio Front-Ends



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Characterization and Modeling of Software Defined Radio Front-Ends

Tese apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Doutor em Engenharia Electrotécnica, realizada sob a orientação científica do Professor Doutor Nuno Miguel Gonçalves Borges de Carvalho, Professor Associado com Agregação do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro.

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Dedico este trabalho à Clara, à Rita, aos meus pais Alice e Vítor e ao meu orientador Prof. Nuno Borges Carvalho, pelo incansável apoio e motivação.

"Simple things should be simple, complex things should be possible"

"The best way to predict the future is to invent it"

by Alan Curtis Kay

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agradecimentos / acknowledgements

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A todos o meu Muito Obrigado!

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palavras-chave

Rádio definido por software, rádio cognitivo, instrumentação multi-domínio, distorção não-linear, multi-portadora, gama dinâmica, largura de banda.

resumo

O presente trabalho tem por objectivo estudar a caracterização e modelação de arquitecturas de rádio frequência para aplicações em rádios definidos por software e rádios cognitivos. O constante aparecimento no mercado de novos padrões e tecnologias para comunicações sem fios têm levantado algumas limitações à implementação de transceptores rádio de banda larga. Para além disso, o uso de sistemas reconfiguráveis e adaptáveis baseados no conceito de rádio definido por software e rádio cognitivo assegurará a evolução para a próxima geração de comunicações sem fios. A ideia base desta tese passa por resolver alguns problemas em aberto e propor avanços relevantes, tirando para isso partido das capacidades providenciadas pelos processadores digitais de sinal de forma a melhorar o desempenho global dos sistemas propostos.

Inicialmente, serão abordadas várias estratégias para a implementação e projecto de transceptores rádio, concentrando-se sempre na aplicabilidade específica a sistemas de rádio definido por software e rádio cognitivo. Serão também discutidas soluções actuais de instrumentação capaz de caracterizar um dispositivo que opere simultaneamente nos domínios analógico e digital, bem como, os próximos passos nesta área de caracterização e modelação.

Além disso, iremos apresentar novos formatos de modelos comportamentais construídos especificamente para a descrição e caracterização não-linear de receptores de amostragem passa-banda, bem como, para sistemas não-lineares que utilizem sinais multi-portadora.

Será apresentada uma nova arquitectura suportada na avaliação estatística dos sinais rádio que permite aumentar a gama dinâmica do receptor em situações de multi-portadora. Da mesma forma, será apresentada uma técnica de maximização da largura de banda de recepção baseada na utilização do receptor de amostragem passa-banda no formato complexo.

Finalmente, importa referir que todas as arquitecturas propostas serão acompanhadas por uma introdução teórica e simulações, sempre que possível, sendo após isto validadas experimentalmente por protótipos laboratoriais.

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keywords

Software defined radio, cognitive radio, mixed-domain instrumentation, nonlinear distortion, multi-carrier, dynamic range, bandwidth maximization.

abstract

This work investigates the characterization and modeling of radio frequency front-ends for software defined radio and cognitive radio applications. The emergence of new standards and technologies in the wireless communications market are raising several issues to the implementation of wideband transceiver systems. Also, reconfigurable and adaptable systems based on software defined and cognitive radio models are paving the way for the next generation of wireless systems. In this doctoral thesis the fundamental idea is to address the particular open issues and propose appropriate advancements by exploring and taking profit from new capabilities of digital signal processors in a way to improve the overall performance of the novel schemes.

Receiver and transmitter strategies for radio communications are summarized by concentrating on the usability for software defined radio and cognitive radio systems. Available instrumentation and next steps for analog and digital radio frequency hardware characterization is also discussed.

Wideband behavioral model formats are proposed for nonlinear description and characterization of bandpass sampling receivers, as well as, for multi-carrier nonlinear systems operation. The proposed models share a great flexibility and have the freedom to be simply expanded to other fields.

A new design for receiver dynamic range improvement in multi-carrier scenarios is proposed, which is supported on the useful wireless signals statistical evaluation. Additionally, receiver-side bandwidth maximization based on higher-order bandpass sampling approaches is evaluated.

All the proposed designs and modeling strategies are accompanied by theoretical backgrounds and simulations whenever possible, being then experimentally validated by laboratory prototypes.

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List of Acronyms

ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
AWG	Arbitrary Waveform Generator
BPSK	Binary Phase Shift Keying
BPSR	Bandpass Sampling Receiver
CR	Cognitive Radio
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processing
EER	Envelope Elimination and Restoration
FFT	Fast Fourier Transform
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile Communications
I/Q	In-phase/Quadrature
IF	Intermediate Frequency
IFFT	Inverse Fast Fourier Transform
LINC	Linear Amplification with Nonlinear Components
LO	Local Oscillator
LNA	Low Noise Amplifier
LTE	Long Term Evolution
NMSE	Normalized Mean Square Error
NZ	Nyquist Zone
OFDM	Orthogonal Frequency Division Multiplex
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PDF	Probability Density Function
PWM	Pulse-Width Modulation
QAM	Quadrature Amplitude Modulated
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SDR	Software Defined Radio

SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SPI	Six-Port Interferometer
VGA	Variable Gain Amplifier
W-CDMA	Wideband Code Division Multiple Access

Chapter 1 – Introduction

Radio communications are seeing significant changes and improvements every day, with several ideas being delineated for radio architectures approaching multiband and multi-carrier designs, as for instance, novel and demanding concepts being planned for long term evolution (LTE) and LTE-advanced standards with carrier aggregation [1].

Recent developments on software defined radio (SDR) technology are paving the way for next generation of wideband communications and will certainly drive the implementation of a universal radio.

Moreover, SDR as proposed by Mitola [2] is now being accepted as the most probable solution for resolving the need of integration between actual and future wireless communication standards. SDRs take advantage of the processing power of modern digital processor technology to replicate the behavior of a radio circuit. Such a solution allows inexpensive, efficient interoperability between the available standards and frequency bands, because these devices can be improved, updated and change its operation by a simple change in software algorithms.

The ultimate goal for a SDR architecture is to push the digitization closest to the antenna as much as possible and thus, providing an increased adaptation and reconfigurability in the digital domain by the use of current digital signal processors (DSP, FPGA, etc.) capable to correctly treat the incoming signals. A common implementation for the SDR concept is shown in Fig. 1.1.

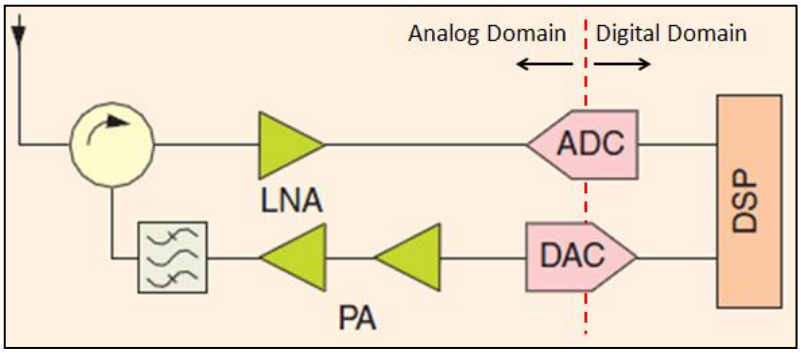

Fig. 1.1 – Typical implementation for an ideal software-defined radio, [2].

This SDR concept is also the basis for cognitive radio (CR) approaches [3], in which the underneath concept imposes strong changes in terms of both complexity and flexibility of operation due to its potential adaptation to the air interface. A promising application for this CR technology is to implement a clever management of spectrum occupancy by use opportunistic radios, in which the radio will adapt and employ spectrum strategies in order to take profit from portions of spectra that are not being used by other radio systems at a given moment.

Furthermore, latest wireless communications standards have been increasingly adopting orthogonal frequency-division multiplexing (OFDM) scheme because of OFDM's spectral efficiency and capability to transmit high data rates over broadband radio channels subjected to multipath fading and shadowing issues. The scenario of conjugation between both multiband systems and OFDM-based schemes will lead to high peak waveforms, commonly characterized by its peak-to-average power ratio (PAPR), and thus limits the amount of power that can be received or transmitted without distortion, [4] [5].

In this sense, the expected developments will impose huge impairments in the design of radio receivers and associated characterization techniques. In fact, a major bottleneck for the deployment of SDR/CR systems is the enabling hardware to realize such spectrum agile radio transceivers.

For example, high dynamic range is a very important figure of merit when dealing with multi-carrier multiband digital receivers, [6], since the receiving unit should cope with signals having very different power levels at same time. Associated to this concern is the PAPR problem that immediately degrades the quality of the transmitted and received signal, either by requiring high values of input power back off in power amplifiers, and thus reduce its efficiency, or by the fact that it imposes a degradation of the signal-to-noise and distortion ratio (SNDR) in receiver analog-to-digital converters (ADCs) [7]. This still remains a problem to be fully resolved and not much worth literature is available on the subject, mainly when concentrating on multiband multi-carrier wireless systems.

Wideband multi-carrier receiver design is also another important theme to evaluate. Some techniques have been presented as hybrid filter banks [8] and also second-order bandpass sampling receivers (BPSR), [9] and [10], but the presented ideas are mainly focused on the mathematical forms of this signal processing theory and not necessarily based on true hardware implementations.

In this context another matter that still lacks a solution is on how to model multiband multi-carrier nonlinear transceivers. Despite several papers has been published on nonlinear models, few are dedicated to multi-carrier systems and normally only studied the transmitter path, [11] [12].

A transversal subject is the test and measurement of such SDR/CR systems, which will demand for specifically designed mixed-signal instrumentation capable to operate in the two domains [13]. Several solutions suitable for SDR/CR characterization are available in the instrumentation market, such as mixed-signal oscilloscopes that are capable of operating in the analog and digital domains at same time, allowing time synchronization between those waveforms. Other approach combines several instruments, including logic analyzers, oscilloscopes, vector signal analyzers, or real-time signal analyzers, [14] and [15]. Nevertheless, those solutions demonstrate some limitations and are yet not able to characterize a complete SDR/CR front-end. This subject will be introduced in more detail in chapter 2.3 (below), but recent advances in this area achieved by the student's research group have not been considered for the present doctoral thesis.

1.1 Motivation and Outline

The motivation for this thesis was exactly to address some of the open issues listed in the previous section, having in mind the determination to expand the scientific state-of-the-art within SDR and CR areas.

In this sense, important goals have been accomplished during this doctoral study as follows:

- Wideband behavioral model for bandpass sampling receivers nonlinear operation
- Nonlinear behavioral model for multi-carrier devices covering inter-modulation and cross-modulation distortion mechanisms
- Architecture to enhance the receiver dynamic range when in presence of multiband multi-carrier wireless signals
- Design for receiver bandwidth maximization based on second-order bandpass sampling receivers

The basic operation principle behind the majority of proposed concepts was to pass, as much as possible, to the digital domain any type of processing on the incoming signals, in order to take profit from the increased capabilities of digital signal processors. Regarding the modeling theme the idea was mainly to create behavioral strategies to improve the understanding of real-world nonlinear processes.

It is worth mention that experimental work was carried out with the purpose of validating all concepts. Theoretical modeling and simulations were also performed whenever possible or useful.

The introductory part of the thesis provides a brief background about the SDR and CR areas, to which all the work performed for this thesis belongs. In chapter 2 is presented a high-level overview of solutions for receiver and transmitter architectures for SDR and CR front-end design and measurement instrumentation needed for these new paradigms. Chapter 3 deals with behavioral model strategies based on Volterra series theory for representation of specific bandpass sampling receiver operation, but also to describe general multi-carrier nonlinear situations. Receiver's dynamic range and bandwidth limitations are discussed in chapter 4. In this chapter are proposed techniques for receiving dynamic range increase and bandwidth maximization. The last chapter presents the final conclusion and an outlook on future projects originated from the work done for this thesis.

As detailed in the following section, all the concepts discussed in this thesis were either published or submitted to prestigious scientific journals of the present research areas [J1]–[J3], presented in relevant international conferences [C1]–[C5], and other additional works published in the most appropriate places [A]–[K] not used as basis of the thesis.

1.2 Main Contributions

On the purpose of this thesis writing the contents of most relevant publications, inside each particular topic, have been considered. In this line, the document is largely supported on the following papers:

[J1] P.M. Cruz, N.B. Carvalho and K.A. Remley, "Designing and Testing Software-Defined Radios", *IEEE Microwave Magazine*, vol. 11, no. 4, June 2010.

[J2] P.M. Cruz and N.B. Carvalho, "Wideband Behavioral Model for Nonlinear Operation of Bandpass Sampling Receivers", *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 4, April 2011.

[J3] P.M. Cruz, N.B. Carvalho and K.A. Remley, "Improving Dynamic Range of SDR Receivers for Multi-Carrier Wireless Systems", Submitted to *IEEE Transactions on Circuits and Systems Part I: Regular Papers*.

[C1] P.M. Cruz and N.B. Carvalho, "PWM Bandwidth and Wireless System Peak-to-Minimum Power Ratio", *European Microwave Integrated Circuits Conference*, Rome, Italy, September 2009.

[C2] P.M. Cruz and N.B. Carvalho, "Modeling Band-Pass Sampling Receivers Nonlinear Behavior in Different Nyquist Zones", *IEEE MTT-S International Microwave Symposium*, Anaheim, CA, May 2010.

[C3] P.M. Cruz and N.B. Carvalho, "Multi-Carrier Wideband Nonlinear Behavioral Modeling for Cognitive Radio Receivers", *European Microwave Integrated Circuits Conference*, Manchester, United Kingdom, October 2011.

[C4] P.M. Cruz and N.B. Carvalho, "Enhanced Architecture to Increase the Dynamic Range of SDR Receivers", *IEEE Radio and Wireless Symposium*, Phoenix, AZ, January 2011.

[C5] P.M. Cruz, N.B. Carvalho and M.E. Valkama, "Evaluation of Second-Order Bandpass Sampling Receivers for Software Defined Radio", *European Microwave Integrated Circuits Conference*, Amsterdam, Netherlands, October 2012.

Additionally, several other contributions have been accomplished but are not included in the thesis. Their content partially overlaps with the annexed papers or are out of the scope of this thesis. The following list of publications is enumerated by the date of appearance.

[A] P.M. Cruz and N.B. Carvalho, "Multi-Mode Receiver for Software Defined Radio", *2nd Congress of the Portuguese Committee of URSI*, Lisboa, Portugal, November 2008.

[B] P.M. Cruz and N.B. Carvalho, "PAPR Evaluation in Multi-Mode SDR Transceivers", *European Microwave Conference*, Amsterdam, Netherlands, October 2008.

[C] P.M. Cruz and N.B. Carvalho, "Characterization of a SDR Front-End Receiver with Multisine Excitations", *7th Conference on Telecommunications – ConfTele 2009*, Santa Maria da Feira, Portugal, May 2009.

[D] P.M. Cruz and N.B. Carvalho, "Architecture for Dynamic Range Extension of Analog-to-Digital Conversion", *IEEE International Microwave Workshop Series on RF Front-ends for Software Defined and Cognitive Radio Solutions*, Aveiro, Portugal, February 2010.

[E] P.M. Cruz, H.C. Gomes and N.B. Carvalho, "Receiver Front-End Architectures - Analysis and Evaluation" – Chapter in *Advanced Microwave and Millimeter Wave Technologies Semiconductor Devices Circuits and Systems*, Edited by Moumita Mukherjee, In-Tech, Austria, March 2010.

[F] P.M. Cruz, D.C. Ribeiro and N.B. Carvalho, "Virtualized Instrumentation for Emergent Radio Technologies", *5th Congress of Portuguese Committee of URSI*, Lisboa, Portugal, November 2011.

[G] D.C. Ribeiro, P.M. Cruz and N.B. Carvalho, "Two-Tone Measurement Technique to apply on Mixed-Domain Instrumentation", *5th Congress of Portuguese Committee of URSI*, Lisboa, Portugal, November 2011.

[H] P.M. Cruz, N.B. Carvalho and M.E. Valkama, "On the Implementation of a Mixed Frequency-Time Simulator for Band-Pass Sampling Receivers", *Conference on Electronics, Telecommunications and Computers*, Lisboa, Portugal, November 2011.

[I] D.C. Ribeiro, P.M. Cruz and N.B. Carvalho, "Corrected Mixed-Domain Measurements for Software Defined Radios", *European Microwave Conference*, Amsterdam, Netherlands, October 2012.

[J] P.M. Cruz and N.B. Carvalho, "Characterization of Software Defined and Cognitive Radio Front-Ends for Multi-mode Operation" – Chapter in *Microwave and Millimeter Wave Circuits and Systems: Emerging Design, Technologies and Applications*, Edited by A. Georgiadis, H. Rogier, L. Roselli, P. Arcioni, Wiley, November 2012.

[K] P.M. Cruz, D.C. Ribeiro, N.B. Carvalho and M.E. Valkama, "Measurement-based Modelling of Analogue-to-Digital Converters under RF Impairments", Submitted to *IET Circuits, Devices & Systems*.

Chapter 2 – Designing and Testing Multiband Radio Architectures

This chapter will start first by presenting the most used receiver strategies for radio communications and concentrate on the usability for SDR/CR systems.

Afterwards, several architectures for transmitter front-ends are described including traditional heterodyne and zero-IF, but also emergent configurations as digitally-aided "polar" and Doherty designs that account for with some improvements in the efficiency of the vital amplifier block.

Finally, the available instrumentation in the market for analog and digital SDR/CR characterization is summarized. Also, a completely synchronous mixed analog-digital instrumentation proposed in [13] is discussed.

The chapter is mainly supported in the annexed paper [J1] for contributions on architectures for receivers and transmitters of SDR front-ends, and required instrumentation for a correct analog and digital characterization. It is also considered the study made in paper [C1], which shows a relationship between sampling frequency and PAPR of input waveforms. The previous work also demonstrated that coding efficiency of input waveforms will become a key figure of merit for switched power amplifier (PA) transmitter efficiency.

2.1 Architectures for SDR/CR Receivers

For SDR/CR applications several receiver architectures may be used, ranging from common super-heterodyne, zero-IF, and low-IF designs to band-pass sampling approaches, but also recent proposals of six-port interferometers and direct RF sampling with analog decimation. All these are valid and practical receiving architectures, but some are gaining visibility over the others mainly because of the actual advancements in ADC and digital-to-analog converter (DAC) technology and the enormous increase in the capabilities of digital signal processors.

The basic review that is done here is mostly based on [16] and [17]. Starting with the well-known super-heterodyne receiver (Fig. 2.1), where the received signal at the antenna is translated to an intermediate frequency (IF) using a down conversion mixer, band-pass filtered and amplified. This is followed by a second stage for down conversion to baseband based on in-phase/quadrature (I/Q) demodulation and then converted to the digital domain to be treated. This architecture is now adopted mostly for higher radio frequency (RF) and millimeter-wave frequency designs, [18] and [19], such as point-to-point wireless links. In these applications, the solutions discussed below are not practical. Actually, super-heterodyne receivers have a number of substantial problems when they are applied to SDR applications. Generally, a number of fabrication technologies are used, making full on-chip integration difficult. As well, they are usually designed to a specific channel (in a particular wireless standard). This prevents the expansion of the receiving band for use with signals having various modulation formats and occupied bandwidths. Therefore, the super-heterodyne configuration is not attractive for use in SDR receivers due to its complicated expansion for multiband reception.

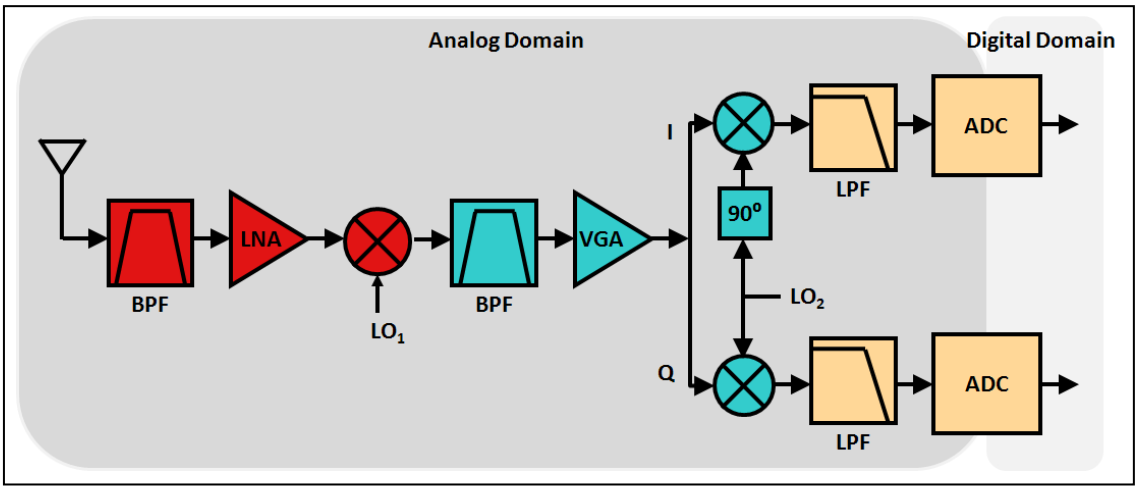

Fig. 2.1 – A super-heterodyne receiver architecture.

Another approach is the zero-IF receiver, [20] and [21], shown in Fig. 2.2, which is a simplified version of the super-heterodyne architecture. The whole received RF band is selected by a band-pass filter and amplified by a low-noise amplifier (LNA), as in the previous architecture. It is then directly down converted to DC by a mixer and converted to the digital domain using an ADC. Compared to the heterodyne architecture, this has a clear reduction in the number of analog components and also allows the use of a filter having

much less stringent specifications than the image-reject filter. As a result, this architecture can make use of a high level of integration, making it a common architecture for multiband receivers such as the one described in [22] and for complete transceiver architectures as in [22] and [23]. However, some of these components can be much more difficult to design due to the required performance of each. Also, the direct translation to DC can generate some issues such as a DC offset [24]. Other issues are related to second-order intermodulation products that are generated around DC, and, since the mixer output is a baseband signal, it can be easily corrupted by the large flicker noise of the mixer [25]. Its advantages and the possibility to minimize the cited disadvantages make this the most commonly used configuration in radio receivers currently.

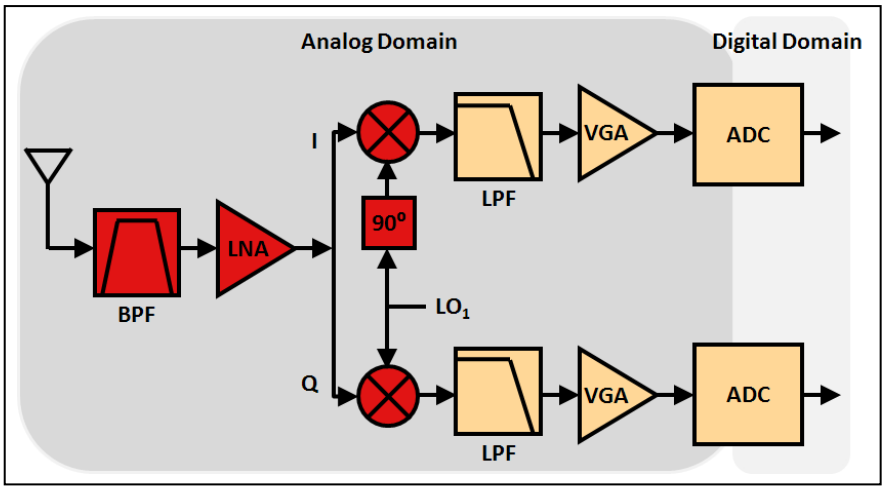

Fig. 2.2 – A zero-IF receiver architecture.

A similar configuration to the zero-IF architecture is the low-IF receiver [26], in which the RF signal is mixed down to a nonzero low or moderate IF instead of going directly to DC. In this case, a RF band-pass filter is applied to the incoming signal which is then amplified. The signal is converted to the digital domain with an ADC of relatively robust performance, which allows the use of digital signal processing for digital filtering for channel-selection, mitigate I/Q imbalances in quadrature demodulators, etc. This architecture still allows a high level of integration and, in addition, does not suffer from the problems of the zero-IF architecture because the desired signal is not situated around DC. However, in this architecture, the image frequency problem is reintroduced and the ADC power consumption is increased because now a higher conversion rate is required.

Finally, an alternative to the previous solutions is the band-pass sampling receiver [27] and [28], shown in Fig. 2.3. In this architecture, the received signal is filtered by an RF band-pass filter that can be a tunable filter or a bank of filters. It is amplified using a wideband LNA. The signal is sampled and converted to the digital domain by a high sampling rate ADC and digitally processed. This configuration is based on the fact that all energy from DC to the input analog bandwidth of the sample and hold circuit of the ADC will be folded back to the first Nyquist zone (NZ), [0, $f_S/2$], without any mixing down conversion needed. This architecture takes advantage of some properties of sample and hold circuit. As was described in [28], it is possible to pinpoint the resulting intermediate frequency, f_{IF}, based on the relationship:

$$if \quad fix\left(\frac{f_C}{f_S/2}\right) \quad is \quad \begin{cases} even, & f_{IF} = rem(f_C, f_S) \\ odd, & f_{IF} = f_S - rem(f_C, f_S) \end{cases} \tag{2.1}$$

where f_C is the carrier frequency, f_S is the sampling frequency, *fix(a)* is the truncated portion of argument *a*, and *rem*(*a*,*b*) is the remainder after division of *a* by *b*.

In this case, the RF band-pass signal filtering plays an important role because it must reduce all signal energy (essentially noise) outside the NZ of the desired frequency band that otherwise would be aliased. If not filtered, the signal energy (noise) outside the desired NZ is folded back to the first zone together with the desired signal, producing a degradation of the signal-to-noise ratio (SNR). This may be given by:

$$SNR = 10 * \log_{10}\left(\frac{S}{N_i + (n-1) * N_0}\right) \tag{2}$$

where *S* represents the desired-signal power, N_i and N_0 are in-band and out-of-band noise, respectively, and *n* is the number of aliased NZs.

The advantage of this configuration is the sampling frequency needed and the subsequent processing rate are proportional to the information bandwidth, rather than to the carrier frequency. This reduces the number of components.

However, some critical requirements exist. For example, the analog input bandwidth of the sample and hold circuit inside the ADC must include the RF carrier, which is a serious problem, considering the sampling rate of modern ADCs. Clock jitter can also be a vital problem. As well, RF band-pass filtering is required to avoid overlap of signals.

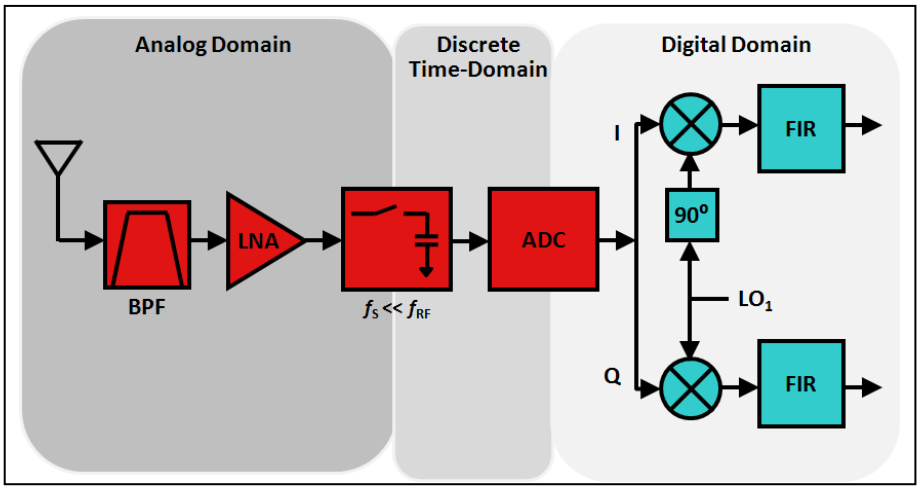

Fig. 2.3 – A bandpass sampling receiver architecture.

Other architectures being proposed for use in SDR receivers involve use of direct RF sampling techniques based on discrete-time analog signal processing to receive the signal, such as the ones developed in [29] and [30]. These methods are still in a very immature stage but should be further studied due to their potential efficiency in implementing reconfigurable receivers.

Furthermore, a quite old technique known as six-port interferometer (SPI) is now being proposed to become an outstanding architecture for SDR receivers and transmitters [31]. This technique was mainly utilized for instrumentation and measurement applications as in [32], [33] and [34]. Nevertheless, quite recent works demonstrate the use of a SPI radio receiver with some required modifications to operate at millimeter-wave frequencies for quadrature-phase-shift-keying (QPSK) and binary-phase-shift-keying (BPSK) modulated signals [35]. An SPI demodulator eliminates the use of down-converting mixers and obtains directly the base-band data with a decoder (by means of new phase spectrum demodulation schemes) from the four interferometer output signals.

On the other hand, the support of quadrature-amplitude-modulated (QAM) signals by the SPI radio needs for more research and some developments are ongoing to include it.

The possible operation of a SPI radio at very high transmission rates (large bandwidths) by using mostly passive devices and its low-cost implementation can be confirmation factors for these SPI radio techniques.

2.2 Architectures for SDR/CR Transmitters

In this section, we discuss several transmitter architectures that have potential application to SDR systems. As we know, a transmitter is not only the PA but a variety of other circuit components collectively known as the front-end. The design of the PA is one of the most challenging aspects of transmitter design, having a high impact on the coverage, the product cost and the power consumption of a wireless system. Here we begin with a consideration of the complete transmitter architecture and in the following it is discussed the PA as it relates to SDR. This review is mainly based on [36].

The first architecture, Fig. 2.4, is the common super-heterodyne transmitter, which is the dual of the super-heterodyne receiver presented in Fig. 2.1. The signal is created in the digital domain and then converted to analog domain using simple DACs. The signal is modulated at an intermediate frequency, where it is amplified and filtered to eliminate harmonics that were generated during modulation. Finally, the signal is up-converted to RF using a local oscillator (LO_2), filtered to remove unwanted image sidebands, amplified by a RF power amplifier and applied to the transmit antenna. As well, the I/Q modulator works at IF, which means hardware components are easier to design than they would be for an RF-based modulator. Finally, the overall gain can be controlled at IF where it is easier to build high-quality variable gain amplifiers. However, such architecture has a significant number of problems, as in the receiver's case. Due to that, this architecture is mostly adopted for microwave point-to-point wireless links as, for example, in backhaul communications [18], [19] and of course in the already mentioned field of radio transmitters. The amount of circuitry and low integration level, as well as the required linearity of the PA and the difficulty to implement multi-mode operation generally prevent the use of super-heterodyne transmitters in SDR applications.

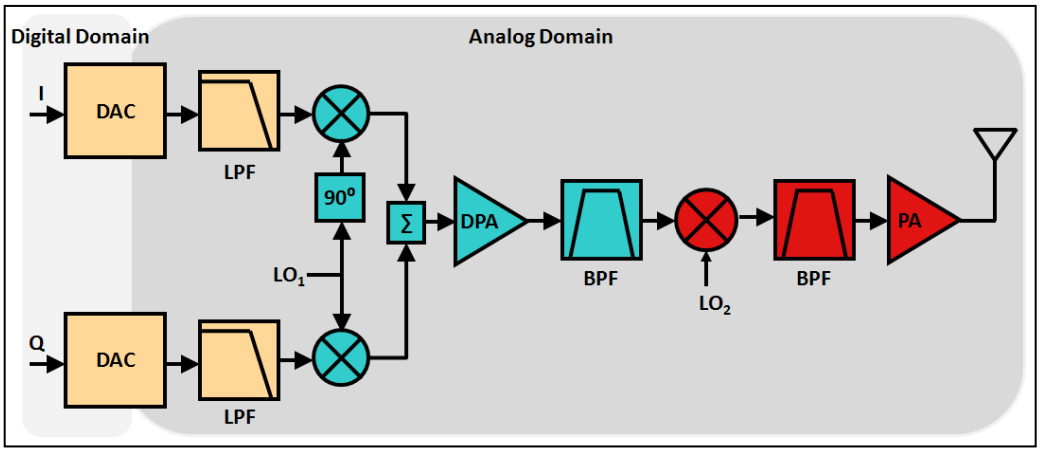

Fig. 2.4 – A super-heterodyne transmitter architecture.

Fig. 2.5 shows a block diagram of a direct-conversion transmitter, [37] and [38], that is a simplified version of the super-heterodyne front-end. As in the last case, two DACs are used to convert the baseband digital I and Q signals to the analog domain. The low-pass filters that follow eliminate Nyquist images and improve the noise floor. These signals are directly modulated to RF by the use of a high-performance I/Q modulator. After that, the signal is filtered by a band-pass filter centered at the desired output frequency and is amplified by a PA.

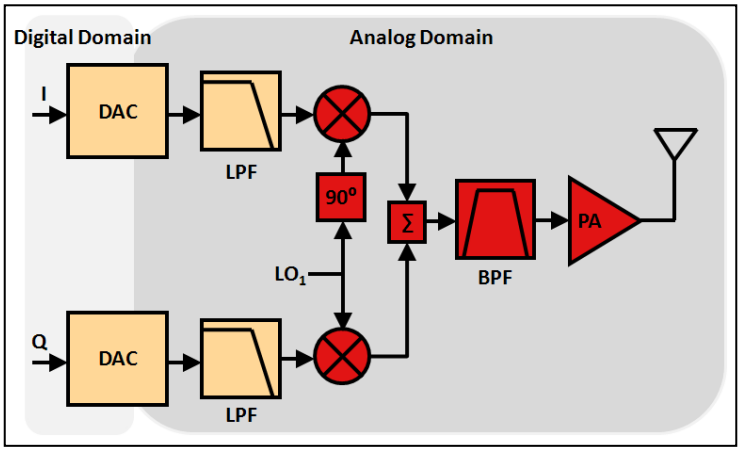

Fig. 2.5 – A direct-conversion transmitter architecture.

In a frequency-agile system, the signal chain must be designed so that carrier frequencies can be synthesized over a defined range that will require a broadband post-modulator or a tunable post-modulator filtering to attenuate out-of-band noise. Thus, due to a phenomenon known as injection pulling, [39], the strong signal at the output of the PA

may couple to the LO. As a result, the frequency of the LO can be pulled away from the desired value.

Even though this architecture reduces the amount of circuitry required and easily allows high-level integration, it carries some disadvantages such as possible carrier leakage, phase-gain mismatch. As well, gain control may need to be carried out at RF and, this architecture also requires a PA with good linearity. With careful design, these transmitters can be employed in SDR applications, and, with the development of integrated technologies, we have witnessed a fast migration from the super-heterodyne architecture to direct-conversion transmitters.

In the previous architectures, the RF PA blocks used are class-A, AB or B, which demonstrate the highest efficiency when operated in the compression region, or are class-D, E and F operated in switching mode [40]. The latter highly efficient PAs operate in a strongly nonlinear mode. As a result, they can only amplify constant-envelope modulated signals such as those used in the GSM access format. Modulation types such as QAM that are used in new access formats, such as wideband code-division multiple access (W-CDMA) and OFDM have inherently high PAPRs. The standard way to avoid compression of PAs is to operate them in "back-off" mode, that is, to reduce the input power until the PA is not driven into compression. Unfortunately, this lowers efficiency significantly, especially for high PAPR signals. Several linearization techniques, for example, feedback, feed-forward or digital pre-distortion, [40] and [41], have been proposed and evaluated, but these are not yet widely used in fully integrated power amplifiers.

The problem of transmitting a high PAPR signal efficiently has been thoroughly investigated over the years. To increase efficiency, a technique proposed some years ago, the Kahn technique, [42], is now being studied for use in new transmitter architectures.

Envelope elimination and restoration (EER), proposed by Kahn, is one method to linearize highly nonlinear, highly efficient transmitters. In these systems, the supply voltage of the output RF power amplifier is dynamically adjusted to restore the amplitude onto a phase-modulated representation of the signal. Fig. 2.6 shows the traditional EER architecture.

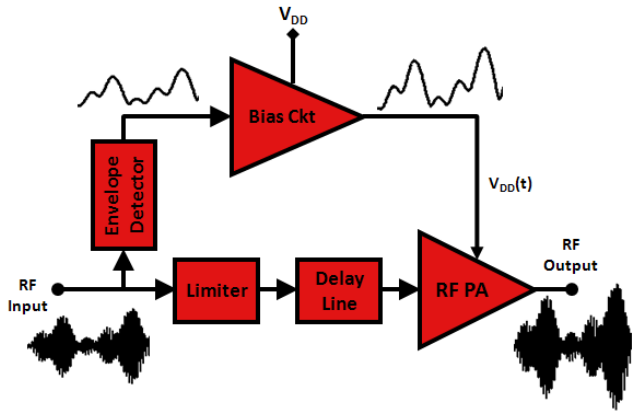

Fig. 2.6 – Block diagram of a Kahn amplifier section.

Although it is a very appealing concept, the actual implementation is very challenging. The challenge arises mainly from the design of a perfect delay line, an accurate limiting stage, an improved bias circuitry that could allow high PAPR and high bandwidths, and also from the required bandwidth that the switched/saturated RF PA should cover to amplify the phase-modulated signal [43].

For this reason, in modern realizations, with the enormous improvements in digital signal processing capabilities, it has been advantageous to implement the envelope detector, the limiter and the delay line (time delay) digitally. Such a digital version of an EER transmitter is used in the "polar" transmitter, which will be explained later.

A visionary solution uses pulse-width modulation (PWM) to create the so-called all-digital transmitter that will be described next. This all-digital approach is important because of the implementation of novel SDR configurations that will enable cognitive approaches. This approach also enables a green environment because it allows the use of very-high-efficiency transmitters, such as the class-S PA shown in Fig. 2.7.

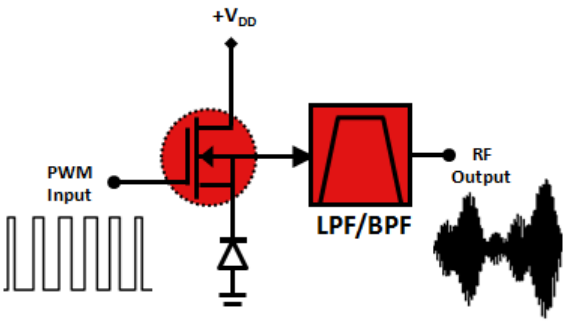

Fig. 2.7 – Simplified circuit of a class-S power amplifier.

Furthermore, as the speed of digital signal processors advances, algorithms in which an FPGA provides signals at RF can be envisioned (particularly for switching amplifiers in which the inputs are digital PWM signals and the outputs are RF modulated signals) in order to develop the so called “all-digital transmitter”.

As shown in Fig. 2.7, the class-S amplifier [44] can be a pure switching amplifier followed by a low-pass filter (to create an envelope signal) or a band-pass filter (to create an RF signal). This amplifier ideally will consume no DC power because the output voltage and the current are equal to zero alternately and, as a result, the efficiency achieved will be 100% in the ideal case. In reality, the class-S amplifier will consume some power in the signal transitions. This is because in real devices, interconnecting components and parasitic capacitance will produce some losses, and finite switching times will occur. The input PWM signal can be generated by a DSP, eliminating the need for a wideband DAC and potentially saving cost.

Unfortunately, if one looks at real-world configurations, it is not possible, yet, to design a high-efficiency class-S amplifier to operate at very high frequencies. Nevertheless, some contributions are appearing in the field [45]. Similar approaches are being tried with sigma-delta modulators to obtain better SNRs, [46] and [47]. Actually, in [C1] a flavor to this implementation difficulty has been introduced by presenting a relationship to determine the required sampling frequency for different input signals having quite different PAPRs. There it was also verified a direct dependency between the PWM coding efficiency of several input signals and the resultant PA efficiency, which has been evaluated for an H-bridge class-S modulator approach.

Because of this, switching amplifiers that are being widely used in new configurations are based on envelope elimination and recovery in a “polar” transmitter configuration, [43] and [48], in which the envelope information is modulated. As a result, the required bandwidth is much smaller since it is a baseband signal that is being amplified. This allows the use of high-efficiency class-S amplifiers, Fig. 2.8.

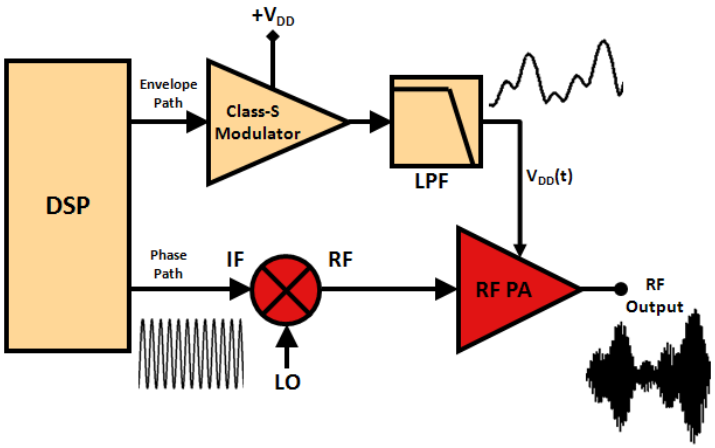

Fig. 2.8 – Block diagram of a "polar" transmitter.

If we look at the schematic of Fig. 2.8, the class-S amplifier only amplifies the envelope of the input signal (detected in the digital domain by the DSP). In this case, the class-S amplifier is only used to vary the bias voltage, $V_{DD}(t)$, of the RF high-power amplifier. In the phase path, a constant-envelope phase-modulated signal is generated in the DSP and then up-converted to RF and applied to the RF PA. This RF PA is always saturated, providing high efficiency. Nonetheless, the major concern of such schemes is the time alignment between the baseband envelope path and the RF path. This can be compensated in the digital domain by use of DSP. Other issue is on the signal passages close to zero voltage of high PAPR waveforms, which could put the RF PA in an inactive operation status. These issues are preventing the architecture to gain more practical visibility.

Other architectures being proposed include amplifier sections based on the Doherty, [49] and [50], and outphasing [51] techniques. The Doherty scheme combines two PAs (a "carrier" PA biased in class-B and a "peak" PA biased in class-C) of equal capacity through quarter-wave-length lines or networks. In modern implementations, DSP can be used to improve the performance of the Doherty amplifier by controlling the drive and bias to the two PAs. For ideal class-B PAs the average efficiency can be as high as 70% for large PAPR signals.

The outphasing design, also known as linear amplification using nonlinear components (LINC), produces an amplitude-modulated signal by combining the outputs of two PAs driven with signals of different time-varying phases. As well as in the previous case using ideal class-B amplifiers the average efficiency now can be around 50% for the same large PAPR signals. More details about these designs can be seen in [36].

With regard to SDRs, both the Doherty and outphasing techniques can be of high interest for future exploration. This is due to the fact that improvements in the particular PA section efficiency will lead to higher efficiencies in the entire transmitter. As well, this transmitter architecture holds the promise of operating correctly for several multi-standard and multiband signals.

As well as in the receiver case, the SPI can also be designed for an SDR transmitter [31] without the use of up-conversion mixers as in the usual configurations. The signal transmission with SPI techniques was successfully implemented for BPSK/QPSK signals due to a new phase spectrum modulation scheme that is able to modulate digital data on the entire phase spectrum of monocycle pulse (ultra wideband, UWB, signals), on single carrier frequency, or on multiple carriers which provides an increased flexibility. In order to modulate the baseband data into RF signals the SPI architecture uses a reference signal and a modulated signal (phase modulation with some algorithms made in the DSP), which are fed to separate input ports of the SPI modulator.

Actually, SPI radio platforms are now being developed in SDRs for new car models intended to be fabricated in Germany [52]. Nevertheless, this architecture should be further investigated in order to be completely applied to SDR transmitting front-ends.

2.3 SDR/CR Measurement Instrumentation

After introducing the candidate architectures of both receivers and transmitters for use in SDR front-ends, we next address another important theme: the test and measurement of SDR systems. Key to this discussion is the concept of a mixed-domain measurement technique because the SDR system always has one input in the analog domain and other in the digital logic domain. Additionally, in the SDR concept the main idea is to push the ADC/DAC as close as possible to antenna and, in that sense, more signals will be in the digital domain. Thus, an easy and complete characterization of both SDR receivers and transmitters will demand for mixed analog-digital instrumentation.

In [13], a new mixed-domain, analog-digital instrument was presented that is specially tailored to the characterization of SDR systems. Fig. 2.9 shows the fundamental concept for this type of instrument. As can be seen, the analog channel has the configuration of a network analyzer, allowing the measurement of the reflection coefficient at the input port.

The second channel is a digital channel taking the properties of a logic analyzer, in which the signals are no longer analog, but are actually bit sequences.

In this work, the authors also discussed signal timing, synchronization requirements and proposed some solutions, for example, embedding a trigger signal in the test excitation. It is also important to refer that the system presented in Fig. 2.9 is able to generate and characterize each standard in its arbitrary waveform generator (AWG). As well, it is capable to treat/relate the analog input with the digital output in order to find a transfer function or even the complete behavioral model for the SDR system.

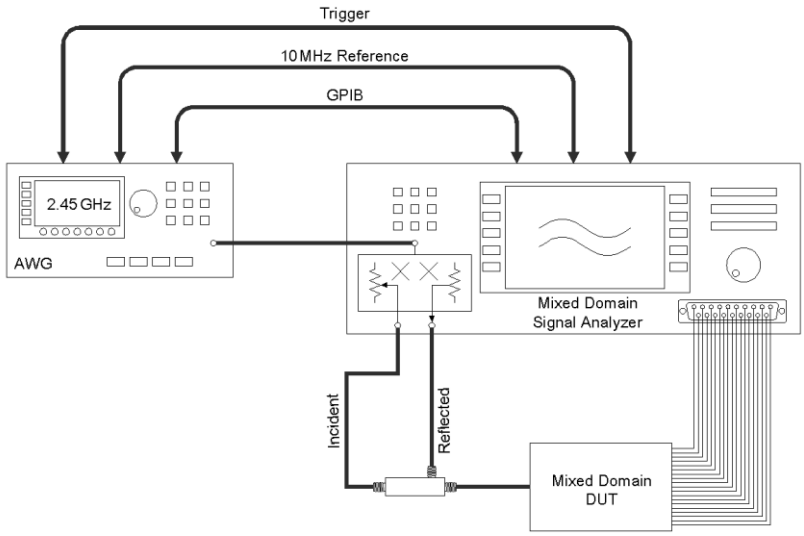

Fig. 2.9 – Mixed-domain instrumentation for SDR characterization.

However, some important problems remained unresolved such as a calibration procedure for this type of mixed-signal instrumentation. Exactly to address the open issues, the authors have presented later on in [I] a calibration procedure for such type of instrumentation, which is based on a two-tone signal excitation. In this recent work the authors were able to propose and verify the calibration scheme for relative phase measurements making a step forward on this subject.

As well, the instrumentation industry, [53], [54] and [55], has some developed instruments suitable for SDR characterization, such as mixed-signal oscilloscopes that are capable of operating in the analog and digital domains at same time. This allows the time correlation of both analog and digital signals in a single instrument. However, mixed-signal oscilloscopes only provide asynchronous sampling. This means that, like an oscilloscope, the mixed-signal oscilloscope uses its internal clock to sample data. As

discussed in [56], the correct evaluation of phase and amplitude transfer functions require coherent sampling between the input, output and clock signals when using such type of SDR devices (including ADCs). This is due to the fact that if they are asynchronous then the spectral leakage that will arise in the transfer function characterization will completely degrade any amplitude and phase information from the SDR. Other problems include, for instance, the memory size necessary to obtain a behavioral model. Thus, these types of instruments are not able to characterize a complete SDR front-end in its entirety.

Other approaches also proposed by the instrumentation industry combine several instruments, including logic analyzers, oscilloscopes, and vector signal analyzers, such as [14], [15] and [57]. For testing an SDR transmitter configuration, these instruments can be used in an arrangement similar to the one shown in Fig. 2.10. We can acquire information from all these instruments and, with the use of reference signals, trigger signals, and markers, provide synchronized measurements between digital and analog domains and between time and frequency domains. Typical measurements that may be used to evaluate the transmission or reception chains are the progression of error vector magnitude, adjacent-channel power ratio, etc. Nevertheless, such characterization requires a substantial set of equipment, a vast knowledge of triggering, and the characterization cannot be done in an "easy" way as, for example, a device characterization with a vector network analyzer.

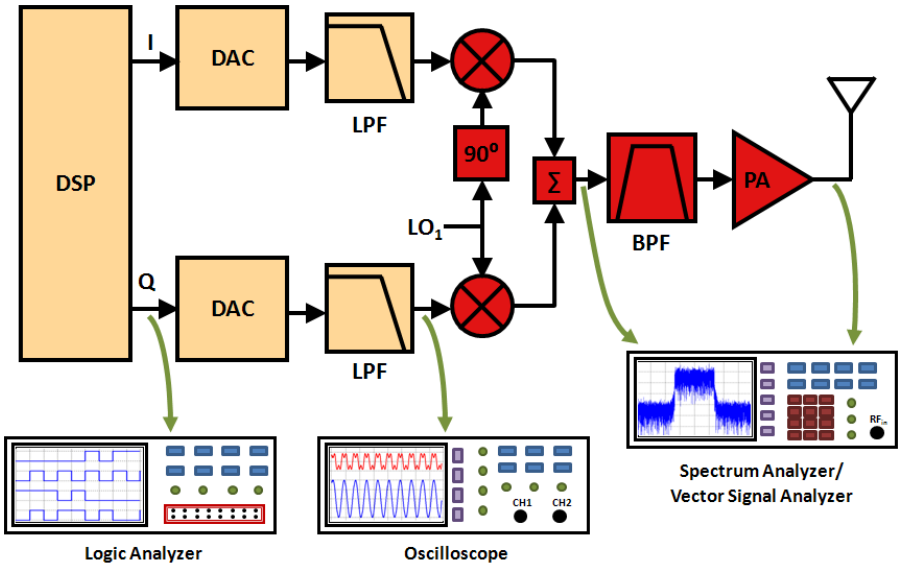

Fig. 2.10 – Combination of several instruments employed in a SDR transmitter.

2.4 Concluding Remarks

In the previous sections a revision of both receivers and transmitters that may be used in the SDR front-ends was presented. There, it was discussed the advantages and disadvantages of each. As was seen, a well-designed architecture for a multi-band multi-mode receiver should optimally share the available hardware resources and make use of tunable and software-programmable devices, which are not features existent in any receiver architecture. In that sense, the SDR receiver front-end will be based either on the zero/low-IF architecture or on the band-pass sampling design when it is more mature. Moreover, the mentioned SPI radio receivers can also be an attractive solution, at least, for low-cost CMOS radio transmitters to operate at high frequencies, for instance above 60GHz.

For the transmitter, the EER technique and its adaptations ("polar" arrangement) are promising choices because their efficiency is largely independent of signal level. They may be readily applied to multi-standard and multiband operation [58]. Such SDR and CR transmitter architectures will require not only highly efficient PAs but also wideband PAs [59]. The SDR community is putting effort toward a green technology, by moving from analog to digital approaches, and thus the demands on the switching speed of RF PA are becoming more evident and more stringent, leading in the future to class-S based transmitters. Also, as in the receiver's case, the SPI radio transmitters can also be possible solutions for SDR commercial applications [60].

Concerning the measurement instrumentation used to characterize SDR/CR systems, some improvements have to be made in order to develop a synchronous instrument that will characterize analog-digital RF front-ends rapidly, automatically, and with impedance-mismatch correction. For instance, such an instrument would ideally provide information such as error vector magnitude for different types of modulation, adjacent channel power ratio for different technologies, and can be able to test multi-standard multiband radio configurations.

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Chapter 3 – Wideband Nonlinear Behavioral Modeling

Practical SDR/CR architectures for receivers and transmitters will require a correct characterization and modeling of the RF front-end as a way to optimize the performance by constructing digital equalizers that would increase the receiving signal quality and, thus, maximize dynamic range, bandwidth, and so on. Moreover, the simulation of such complex architectures (entire receiver and transmitter RF front-ends) is quite computer intensive, mainly when the objective is to simulate RF signals modulated with high bandwidth excitations. Thus, the construction of accurate behavioral models for practical designs, accounting with single and multi-carrier signals, will facilitate the simulation and on the optimistic vision provide a faster time to market for the developed systems.

The chapter is supported in paper [C2] for the initial contributions on BPSR modeling, in paper [J2] for contributing with an improved behavioral model for BPSRs and paper [C3] for contributions on the multi-carrier modulated signals modeling subject.

3.1 Behavioral Modeling of Bandpass Sampling Receivers

Having in mind the receiving architectures previously discussed in chapter 2.1 (above), one of the most promising for SDR/CR applications is the BPSR design (Fig. 2.3) because of its approximation to the initial idea from Mitola [2]. This architecture is also becoming a feasible and practical solution due to the constant advancements achieved in ADCs.

In this manner, the focus of this section is to give a more detailed overview of the BPSR architecture operation and then propose a suitable wideband behavioral model, accompanied by the respective parameter extraction procedure, to cover RF/IF and baseband frequency responses, within the first and over several different NZs. Finally, the proposed behavioral model will be validated in different NZs using a common modulated signal as excitation.

The key element of BPSR architecture is the ADC component (commonly in a pipeline structure) that contains a sample-and-hold circuit, which in theory allows all of the energy from DC to the input analog bandwidth of the ADC to be folded back to the first NZ. This process occurs without any mixing down-conversion because a sampling circuit is

somehow replacing the mixer module. Indeed, this behavior will allow an RF signal of higher frequency to be sampled by a much lower clock frequency. The basic concept is depicted in Fig. 3.1, in which it is observed that all the input signals present in the allowable bandwidth of the sampling circuit are folded back to the first NZ. This folding process occurs for all the available signals at the input of the circuit but also for any nonlinearity that may be generated previously or even in the particular sampling circuit.

Thus, in order to better understand the operation of the explained BPSR in different NZ's let us assume a BPSR sampled by a clock of 100 MHz and excited firstly by a signal excitation present in the first NZ (e.g. 14 MHz) and then by a signal excitation situated in the second NZ (e.g. 78 MHz). Consider as an example a third-order nonlinear system, for the first excitation frequency and taking into account the frequency folding phenomena, the fundamental and respective harmonics will fall within this same 1st NZ. However, the same will not happen for the second excitation frequency, where the baseband will fall on the first NZ, the fundamental and 2nd harmonic will fall in the 2nd and 4th NZ's, respectively, and are folded back in the reversed way. The 3rd harmonic will fall in the 5th NZ and is folded back in the normal mode. Therefore, to describe the nonlinear behavior of such architecture, a huge bandwidth should be covered and accompanied by different dynamic effects, which is represented by different memory lengths in the nonlinear model.

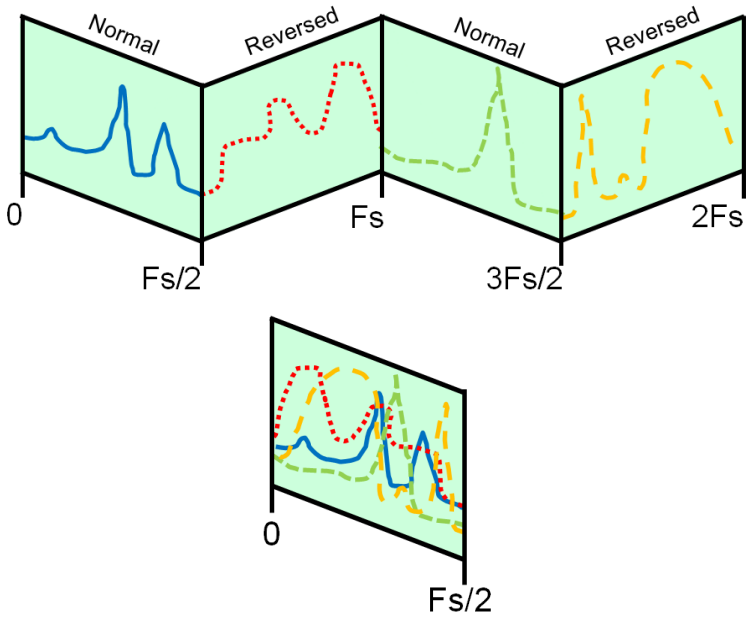

Fig. 3.1 – Process of folding that occurs in the sample-and-hold circuit showing the folding and overlapping of signals in the first NZ.

3.1.1 Proposed Nonlinear Behavioral Model

The last section confirmed that the produced behavioral model should be wideband and take into account the NZ where the signal is sampled in a way to effectively represent the BPSR nonlinear behavior. Additionally, several spectral components may appear in the first NZ case of the low-frequency baseband nonlinearities (defined by an even-order nonlinear product), with high-frequency components also possibly appearing at higher NZs where they are folded back to the resultant ADC bandwidth. This will impose conditions where the dynamic response of the BPSR will have time constants of highly different orders, with some at the RF time frame and others inside the baseband time frame.

So, an appropriate behavioral model that produces the required mathematical description for describing the nonlinear behavior of the BPSR may be supported on the Volterra series theory [61], due to its good performance in this type of mildly nonlinear scenarios. The Volterra series conditions represent a combination of linear convolution and nonlinear power series providing a general structure to model nonlinear systems with memory. As such, it can be used to describe the relationship between the input and output of the addressed BPSR, which may present a nonlinear behavior having memory effects. This relationship can be written as:

$$y(t) = \sum_{n=0}^{\infty} \int_{-\infty}^{\infty} \cdots \int_{-\infty}^{\infty} h_n(\tau_1, \cdots, \tau_n)\, x_{in}(t-\tau_1) \cdots x_{in}(t-\tau_n)\, d\tau_1 \cdots d\tau_n \tag{3.1}$$

where $x_{in}(t)$ and $y(t)$ are the input and output signal waveforms, respectively, and $h_n(\tau_1,\ldots,\tau_n)$ is the n^{th} order Volterra kernel.

The applicability of such an RF time-domain Volterra series model to account with all these nonlinearities at once is complex because of the complicated model structure, which leads to an exponential increase in the number of coefficients for higher degrees of nonlinearities and memory lengths. Furthermore, the overall system description can behave very differently because, for instance, the even-order coefficients can generate signals at very high frequencies (such as in the case of the second harmonic) and at baseband frequencies near DC. In that sense, the Volterra approach as presented in (3.1) is not optimum for this situation since it uses the same descriptor for the second harmonic as for the baseband responses and thus does not provide the required flexibility. In fact, this problem was observed in the work presented in [C2], where a good approximation was

achieved at higher frequencies but it had some problems at lower frequencies and vice versa. To overcome this issue the Volterra series model can be applied in a low-pass equivalent format [62], in which a selection of each nonlinear cluster (baseband, fundamental, second harmonic, etc.) is firstly made and the respective complex envelope is then digitally obtained. As a result, the Volterra low-pass equivalent behavioral model is applied individually to each complex envelope cluster, taking into consideration the nonlinearity that has originated it. Actually, it can be seen as a model extraction based on the envelope harmonic balance method, where each cluster is addressed individually [63]. This low-pass equivalent conversion is exemplified in Fig. 3.2, which considers a third-order degree nonlinear scenario.

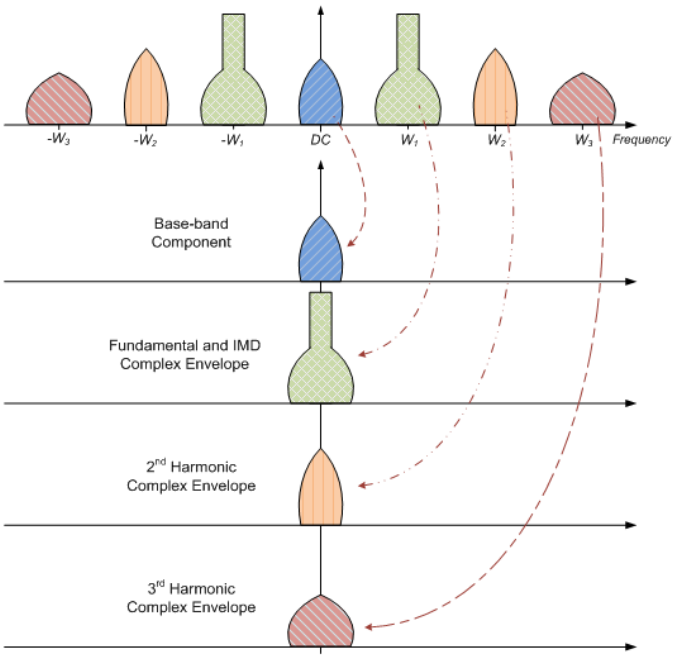

Fig. 3.2 – Diagram of the low-pass equivalent conversion of each cluster.

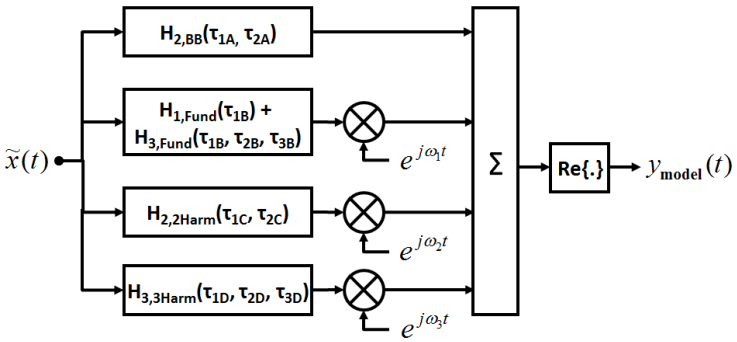

Fig. 3.3 – Proposed design for the BPSR behavioral model.

As illustrated in Fig. 3.3, the resulting model will be a collection of different sub-models obtained and extracted individually for each nonlinear cluster. Generally, this begins with the application of different Volterra operators in the extracted complex envelopes, followed by an up conversion of each cluster to the correct carrier frequency and finally summed together to create the resulting model output. In this way, the input of the proposed model will be the complex envelope of the desired excitation signal, which will then produce a real waveform representing the output of the nonlinear component/system.

Thus, as an example, the baseband and second harmonic arise from a second-order multiplication and are represented in this circumstance as:

$$\tilde{y}_{BB}(k) = \tilde{h}_0 + \sum_{q_1=0}^{Q_{A1}} \sum_{q_2=q_1}^{Q_{A2}} \tilde{h}_{2,BB}(q_1, q_2) \cdot \tilde{x}(k-q_1) \cdot \tilde{x}^*(k-q_2) \tag{3.2}$$

$$\tilde{y}_{2Harm}(k) = \sum_{q_1=0}^{Q_{C1}} \sum_{q_2=q_1}^{Q_{C2}} \tilde{h}_{2,2Harm}(q_1, q_2) \cdot \tilde{x}(k-q_1) \cdot \tilde{x}(k-q_2) \tag{3.3}$$

where h_0 is the DC value of the output, $h_{2,\mathrm{BB}}$ and $h_{2,2\mathrm{Harm}}$ are the 2nd-order Volterra kernels for the baseband and 2nd harmonic responses, respectively. The character ~ refers to a complex signal or value, and the symbol * means the complex conjugate.

For the proposed modeling strategy it can be noticed the different memory lengths used in the baseband and 2nd harmonic components (represented in equations (3.2) and (3.3) by Q_{A1}/Q_{A2} and Q_{C1}/Q_{C2}), which provides an augmented flexibility to these models. As regards to the fundamental signal and associated intermodulation distortion it arises from a first order function combined with a third-order nonlinear product:

$$\begin{aligned} \tilde{y}_{Fund}(k) = & \sum_{q_1=0}^{Q_{B1}} \tilde{h}_{1,Fund}(q_1) \cdot \tilde{x}(k-q_1) \quad + \\ & \sum_{q_1=0}^{Q_{B1}} \sum_{q_2=q_1}^{Q_{B2}} \sum_{q_3=q_2}^{Q_{B3}} \tilde{h}_{3,Fund}(q_1, q_2, q_3) \cdot \tilde{x}(k-q_1) \cdot \tilde{x}(k-q_2) \cdot \tilde{x}^*(k-q_3) \end{aligned} \tag{3.4}$$

In the same line, the third harmonic arises uniquely from a third-order degree polynomial:

$$\tilde{y}_{3Harm}(k) = \sum_{q_1=0}^{Q_{D1}} \sum_{q_2=q_1}^{Q_{D2}} \sum_{q_3=q_2}^{Q_{D3}} \tilde{h}_{3,3Harm}(q_1, q_2, q_3) \cdot \tilde{x}(k-q_1) \cdot \tilde{x}(k-q_2) \cdot \tilde{x}(k-q_3) \tag{3.5}$$

Moreover, when higher orders are requested more Volterra kernels should be determined. When extracting the kernels for each nonlinear cluster it is desirable to include all the possible contributions for each specific case, since it will deeply affect the extraction performance. For example, if expecting a component/system with fifth-order nonlinearities, then the third harmonic will not be exclusively characterized by a polynomial of third-order but also including the contributions from a fifth-order coefficient.

In summary, it should be emphasized that in each cluster any nonlinear order and memory depth can be used and thus there are separate clearly different approaches. Also, the proposed behavioral model scheme has the feasibility to be extended and applied into multi-carrier nonlinear components/systems, as demonstrated in chapter 3.2 (below).

3.1.3 Parameter Extraction Procedure

This section is devoted to describe the parameter extraction procedure that has been employed in a BPSR design similar to Fig. 2.3. The constructed laboratory prototype of this BPSR architecture considered several band-pass filters to select the desired NZ to be modeled connected to a wideband (2 – 1200 MHz) LNA, which has a 1-dB compression point close to +11 dBm, an approximated gain of 23 dB, and a noise figure near to 5 dB. This is then followed by a commercially 10-bit pipeline ADC that has a linear input range of around +10 dBm (2 Vpp for a 50 Ω source) and an analog input bandwidth (-3 dB bandwidth of the sampling circuit) of 160 MHz. This ADC component was then sampled by a sinusoidal clock of 90 MHz.

Evaluating the BPSR at such clock frequency will virtually create several NZ's of 45 MHz ($f_s/2$) each at the output of the BPSR. In this sense, the chosen excitation carrier frequencies are 11.5 MHz for the 1st NZ and 69 MHz for the 2nd NZ.

To correctly measure the BPSR design, a laboratory setup based in the mixed-domain test bench proposed in [13] was used, shown briefly in Fig. 3.4. As illustrated in [J1] it is specifically dedicated to mixed-domain radio front-ends (SDR/CR) characterization.

As was widely discussed in [J2] it is quite difficult to have a setup for mixed-domain measurements with synchronized samplers between the different domains. The solution for this situation was to embed a triggering pulse in the input signal followed by the waveform excitation of interest. In this way, all the measurements will be corrected accordingly to

that trigger signal and become fully synchronous. Further details about this practice can be seen in [J2].

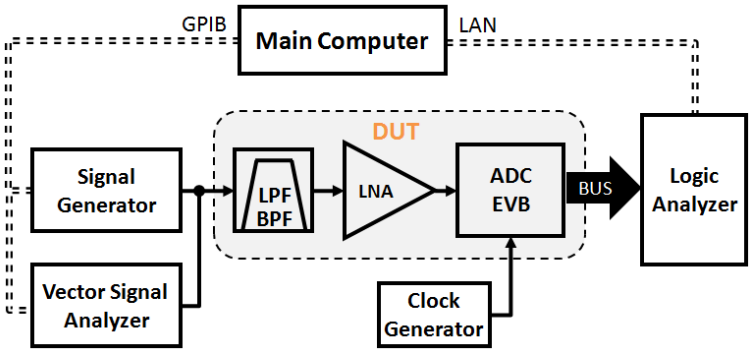

Fig. 3.4 – The experimental test bench proposed in [13].

In addition to this, the treatment of the measured signals revealed in certain situations a huge corruption of these measurements by noise (instrumentation noise and noise generated in the BPSR components), which is very close to the small distortion products desired to be modeled, turning the parameter extraction impractical. Once again to minimize this issue a new approach was pursued consisting on the following steps:

1. Apply a Fourier transform (FFT) to the output RF time-domain signals.
2. Select only the desired frequency bins [64] taking into account the nonlinearity order considered and construct a noise-free signal, only with the selected frequency components, for each cluster to be extracted.
3. Afterwards, apply an inverse Fourier transform (IFFT) in order to obtain a cleaner (without undesired frequency components and out-of-band noise) time-domain signal for each cluster.
4. Calculate the complex envelopes (e.g., using the Hilbert transform) for each cluster of the rearranged output signals.
5. Apply the low-pass equivalent Volterra series model, expressions (3.2)-(3.5), into these new output signals using also the measured input complex envelope and obtain the desired low-pass complex Volterra kernels.
6. Up-convert each output complex signal to the corresponding cluster center frequency, depending on the resultant frequency from expression (2.1), and finally assess the model performance.

A generalized flow diagram for the overall parameter extraction procedure is illustrated in Fig. 3.5. Such an approach allows, in step 5, the selection of nonlinear orders and memory taps that are more convenient in each specific cluster, reducing in some sense the required number of parameters. As well, it is important to notice that when the signal is within an even order NZ, the output signal at the output of the BPSR will appear rotated (reversed), see Fig. 3.1. Thus, in these circumstances an inversion of the signal is required, prior the extraction of the particular cluster behavioral model.

Taking into consideration a few assumptions about the input signals, the extraction process of the low-pass complex Volterra kernels was based in a least-squares technique, expressed by:

$$\mathrm{H} = \left(\mathrm{X}^T \mathrm{X}\right)^{-1} \mathrm{X}^T \, \mathrm{Y} \tag{3.6}$$

where **X** and Y are the input complex signal matrix and the output signal vector, respectively, and H is the vector of complex kernels being searched. This least-squares extraction is then executed for each one of the previously selected clusters.

As an example, if the complex parameters are being investigated for a baseband cluster with a memory length of Q taps, the input signal matrix (**X**) will be designed in the following way:

$$\mathrm{X} = \begin{bmatrix} 1 & \tilde{x}(0)\tilde{x}^*(0) & \tilde{x}(0)\tilde{x}^*(-q) & \cdots & \tilde{x}(-Q)\tilde{x}^*(-Q) \\ \vdots & \vdots & \vdots & & \vdots \\ 1 & \tilde{x}(n)\tilde{x}^*(n) & \tilde{x}(n)\tilde{x}^*(-q) & \cdots & \tilde{x}(n-Q)\tilde{x}^*(n-Q) \\ \vdots & \vdots & \vdots & & \vdots \\ 1 & \tilde{x}(N)\tilde{x}^*(N) & \tilde{x}(N)\tilde{x}^*(N-q) & \cdots & \tilde{x}(N-Q)\tilde{x}^*(N-Q) \end{bmatrix} \tag{3.7}$$

and the complex output at base-band frequencies (Y) is defined as:

$$\mathrm{Y} = \left[\tilde{y}_{BB}(0) \quad \cdots \quad \tilde{y}_{BB}(n) \quad \cdots \quad \tilde{y}_{BB}(N)\right]^T \tag{3.8}$$

where Q represents the memory length and N is the number of captured samples for both input and output complex envelope signals.

Afterwards, the seek vector of complex kernels (H) for the baseband cluster is calculated using (3.6), which is actually composed of the following Volterra operators:

$$\mathrm{H} = \left[\tilde{h}_0 \quad \tilde{h}_{2,BB}(0,0) \quad \tilde{h}_{2,BB}(0,q) \quad \cdots \quad \tilde{h}_{2,BB}(Q,Q)\right]^T \tag{3.9}$$

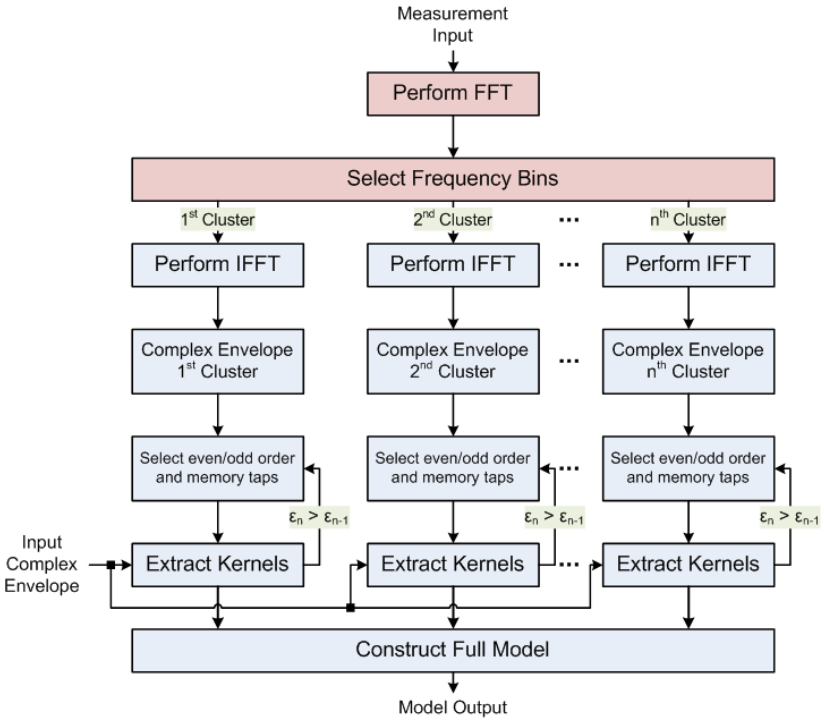

Fig. 3.5 – Flowchart diagram of the kernels extraction procedure.

This process is then executed for each individual cluster and then the final response of the behavioral model is achieved by employing the design depicted in Fig. 3.3, wherein each cluster is up converted to the exact carrier frequency, based in equation (2.1), as shown in the following expression:

$$y(k) = \mathrm{Re}\{\tilde{y}_{BB}(k) + \tilde{y}_{Fund}(k).e^{jw_1 t} + \tilde{y}_{2Harm}(k).e^{jw_2 t} + \tilde{y}_{3Harm}(k).e^{jw_3 t}\} \quad (3.10)$$

As a final remark about the proposed behavioral model and respective parameter extraction strategy it should be emphasized that great care should be taken when choosing carrier frequencies, signal bandwidth, etc. due to the folding process that happens in the addressed DUT and the model extraction will become not valid if different clusters fall within overlapping frequency bins.

3.1.4 Model Validation with QPSK Signal

In order to evaluate the performance of the proposed behavioral model for a BPSR, a QPSK modulated signal with a symbol rate of around 1 Msymb/s filtered with a square-root raised cosine (RRC) filter with a roll-off factor of 0.25, which determined a signal PAPR of approximately 5.4 dB, has been applied. It has been used the laboratory setup

shown in Fig. 3.4 to perform the various measurements. The extraction of the seek parameters was executed in part of the captured input and each cluster output complex envelopes. After that, an equal number of remain samples were used to assess the accuracy of the complete behavioral model when compared with the obtained measurement results.

3.1.4.1 Frequency Domain Results

The obtained results are shown in Fig. 3.6 and Fig. 3.7 for the two different NZ's evaluated. Looking to the figures it can be said that the proposed behavioral model and related parameter extraction procedure is estimating well the unknown parameters and producing good results for the two NZ signals. Moreover, in Fig. 3.6 the different memory depths (taps) for each nonlinear cluster can be checked for different NZ's.

In order to be more precise in this evaluation, the integrated power within the frequency band of the fundamental signal, lower and upper adjacent channels, baseband component, and 2nd and 3rd harmonics were calculated. These results are revealed in Table 3.A for the two NZ's evaluated. It is clear the good approximation to the BPSR measurements achieved by the proposed behavioral model.

Other figure of merit commonly used to express the error of a given model is the normalized mean square error (NMSE), [65]. The comparison between the complete measured output signals and the proposed behavioral model results reached NMSE values of -33.0 dB for the 1st NZ excitation and -32.9 dB for the 2nd NZ excitation.

The previous demonstrated results validate in some sense this behavioral model proposed for BPSR application.

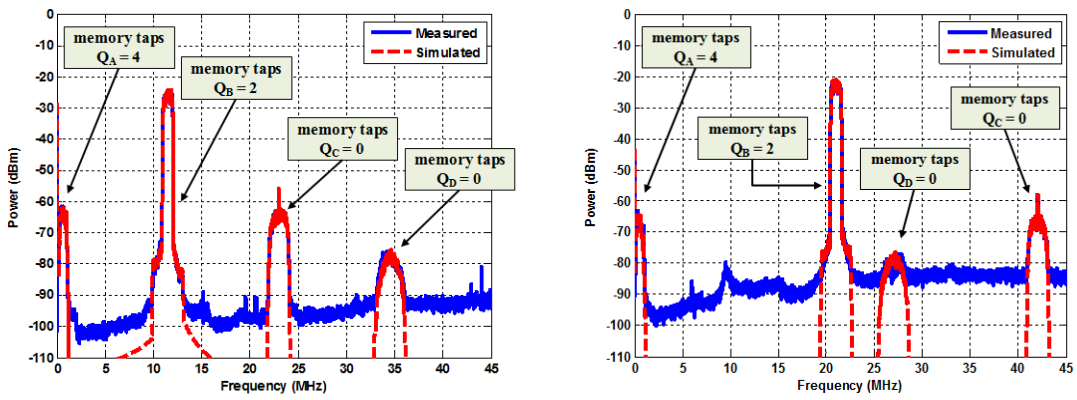

Fig. 3.6 – Entire bandwidth (smoothed) of measured and modeled outputs for a QPSK signal centered at 11.5 MHz (left) and 69 MHz (right).

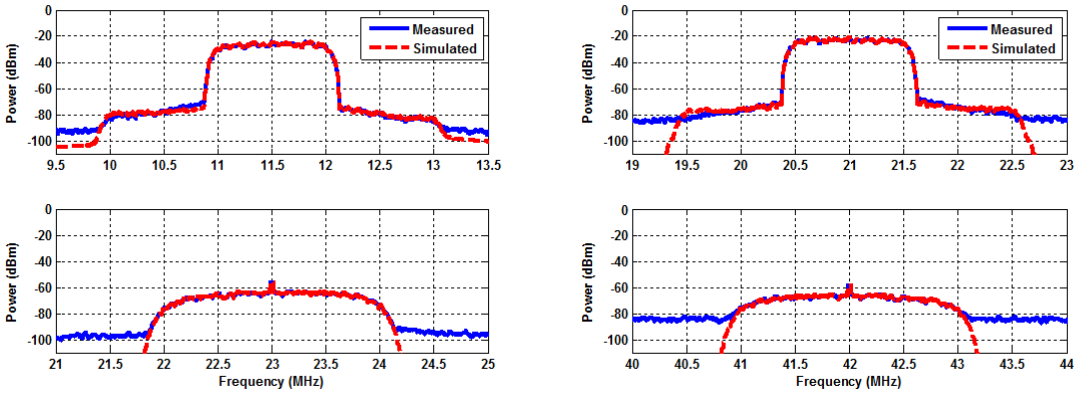

Fig. 3.7 – Spectrum of measured and modeled results, at carrier band and 2nd harmonic band for a QPSK signal centered at 11.5 MHz (left) and 69 MHz (right).

Table 3.A – Measured and modeled integrated powers for the QPSK excitation.

	1st NZ (f_c = 11.5 MHz)		2nd NZ (f_c = 69 MHz)	
	Meas. [dBm]	**Model [dBm]**	**Meas. [dBm]**	**Model [dBm]**
Baseband	-41.7	-42.9	-44.6	-45.4
Fundamental	-3.01	-3.02	0.40	0.38
Adj. Ch. (Lower)	-53.3	-54.6	-52.7	-52.5
Adj. Ch. (Upper)	-55.9	-56.0	-50.3	-51.2
2nd Harmonic	-38.5	-38.5	-40.8	-40.9
3rd Harmonic	-51.6	-52.2	-52.8	-53.0

3.1.4.2 Symbol Evaluation Results

In order to further validate the presented model, a digital version of a QPSK demodulator was implemented in order to obtain the symbol information (around 1000 data symbols) from the previously measured and modeled QPSK signals, being evaluated in the two different NZ's.

Fig. 3.8 illustrates the obtained normalized constellation diagrams for each NZ addressed. There, it can be verified once again the good performance of the proposed behavioral model and respective parameter extraction procedure. These assumptions are fully confirmed by the values presented in Table 3.B, where a good matching in terms of root-mean square (rms) EVM and also in peak EVM is observed.

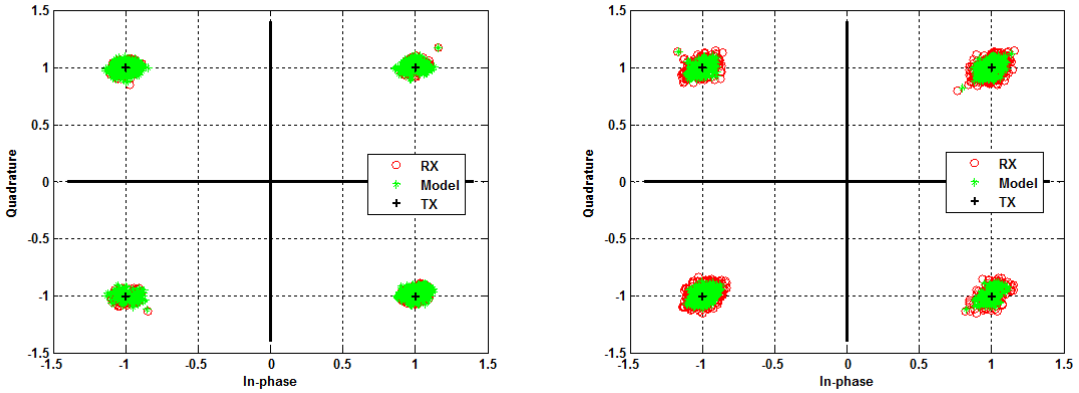

Fig. 3.8 – Normalized constellation diagrams for the QPSK signal centered at 11.5 MHz (left) and 69 MHz (right).

Table 3.B – Measured and modeled EVM values for the QPSK excitation.

	1st NZ (f_c = 11.5 MHz)		2nd NZ (f_c = 69 MHz)	
	Meas.	**Model**	**Meas.**	**Model**
EVM *rms*	4.23 %	4.97 %	6.85 %	5.2 %
EVM peak at Symbol	16.39 % (703)	16.15 % (703)	22.13 % (898)	19.24 % (898)

3.2 Behavioral Modeling of Multi-Carrier Devices

In the introductory section it was stated that the appearance of SDR/CR technology have significantly raised the design complexity of the receiving and transmitting stages, which would request that modeling stratagems predict the operation over very wide bandwidths and take into consideration multi-carrier signal excitations.

In this sense, the aim of this section is to propose a general behavioral model based on Volterra series for nonlinear devices, which is able to cover intermodulation and cross-modulation distortion mechanisms that appears in multi-carrier nonlinear devices.

3.2.1 Review of Multi-Carrier Nonlinear Effects

The interaction of multi-carrier signals when passed through nonlinear devices lead to a very complex problem due not only to self-distortion from each carrier, but also due to the rather important phenomena of cross-modulation that will occur between those multiple

carriers. These distortion mechanisms will manifest themselves as extra in-band and out-of-band alterations, which could completely degrade the carrier signal-to-noise ratio and increase the adjacent channels interference. Other spurious components will appear at intermodulation frequencies that result in interference with other carriers within the operating bandwidth of the device.

Thus, in order to clearly comprehend these phenomenon's we will considered a simple static nonlinearity represented by a power series model truncated at the third-order degree,

$$y[x(t)] = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \tag{3.11}$$

where *x(t)* is the input signal, *y(t)* is the output signal, and a_1, a_2, and a_3 are the power series coefficients.

Thus, considering that a multi-carrier signal passes through the previous nonlinear model, at the output, we will get several mixtures due to self- and cross-modulations. The mixing outcomes resulting from (3.11) are shown in Table 3.C, which give a brief idea about the complexity in terms of the number of mixtures and the wideband necessity for an appropriate behavioral modeling. In this example, two multi-carrier signals with different bandwidths and centered at different carrier frequencies were considered.

This quite simple nonlinear model, as expressed in (3.11), was then excited with two multisine signals centered at different carrier frequencies (ω_1 and ω_2) and with different bandwidths (BW_1 and BW_2) respectively for first and second multisine signals. In Fig. 3.9 can be observed the resultant smoothed spectra centered at carriers one and two when the other carrier (multisine signal) is switched on or off.

As can be seen, the action of switching on carrier two will cause a high impact on the in-band and out-of-band distortions in the region of carrier one. This happens because third-order cross-modulations will appear and completely deform the expected performance. It is also important to notice that spectral regrowth appearing at carrier one zone is broader when carrier two is on due to the respective larger bandwidth. Regarding the impact of 3rd-order cross-modulation in carrier two it is not so noticeable due to the lower bandwidth of carrier one but it will occur in the same fashion.

Thus, it is very welcome and appropriate to find suitable behavioral models capable of predict the behavior of nonlinear devices covering not only self-modulation distortion but also cross-modulations between two or more carriers.

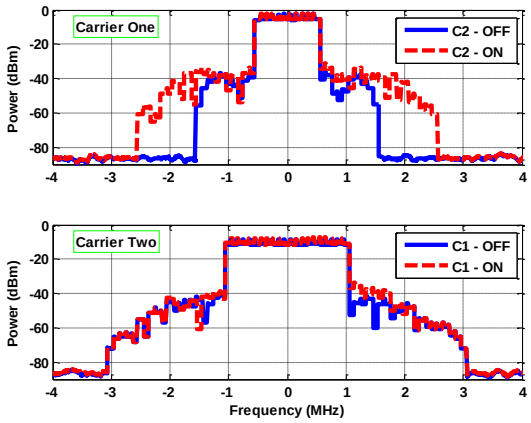

Fig. 3.9 – Obtained spectrum from the nonlinear model of expression (3.11) when excited by a multi-carrier signal.

Table 3.C – Obtained mixtures from the model in (3.11) for two excitation signals.

First-Order (Linear Output)	**Output Central Frequency (Bandwidth)**
Linear signal output at ω_1	ω_1 (BW_1)
Linear signal output at ω_2	ω_2 (BW_2)
Second-Order Mixtures	
2^{nd}-order self-modulation (ω_1 - ω_1)	DC ($2BW_1$)
2^{nd}-order self-modulation (ω_2 - ω_2)	DC ($2BW_2$)
2^{nd}-order cross-modulation lower	ω_2 - ω_1 (BW_2 + BW_1)
2^{nd}-harmonic of ω_1	$2\omega_1$ ($2BW_1$)
2^{nd}-harmonic of ω_2	$2\omega_2$ ($2BW_2$)
2^{nd}-order cross-modulation higher	ω_1 + ω_2 (BW_1 + BW_2)
Third-Order Mixtures	
3^{rd}-order cross-modulation ($2\omega_1$ - ω_2)	$2\omega_1$ - ω_2 ($2BW_1$ + BW_2)
3^{rd}-order self-modulation (ω_1 + ω_1 - ω_1)	ω_1 ($3BW_1$)
3^{rd}-order cross-modulation (ω_1 + ω_2 - ω_2)	ω_1 (BW_1 + $2BW_2$)
3^{rd}-order self-modulation (ω_2 + ω_2 - ω_2)	ω_2 ($3BW_2$)
3^{rd}-order cross-modulation (ω_2 + ω_1 - ω_1)	ω_2 (BW_2 + $2BW_1$)
3^{rd}-order cross-modulation ($2\omega_2$ - ω_1)	$2\omega_2$ - ω_1 ($2BW_2$ + BW_1)
3^{rd}-harmonic of ω_1	$3\omega_1$ ($3BW_1$)
3^{rd}-order cross-modulation ($2\omega_1$ + ω_2)	$2\omega_1$ + ω_2 ($2BW_1$ + BW_2)
3^{rd}-order cross-modulation ($2\omega_2$ + ω_1)	$2\omega_2$ + ω_1 ($2BW_2$ + BW_1)
3^{rd}-harmonic of ω_2	$3\omega_2$ ($3BW_2$)

3.2.2 Proposed Multi-Carrier Nonlinear Model

This section will explain the proposed behavioral model scheme for the prediction of multi-carrier operation of general nonlinear systems. As was seen in the previous point the correct description of a multi-carrier nonlinear component behavior requires that it must be wideband and it must depend on several input signals. Additionally, using the information shown in Table 3.C we can state that nonlinear signal generation could force spectral components to appear at very different output frequencies. This fact will impose that the dynamic response of the nonlinear device might have delays of different orders and this should be gathered by the projected behavioral model.

In that way, the same approach based on Volterra series, [61], that has been followed for the BPSR nonlinear modeling will be considered at this point. Similarly, in order to cover such a wideband nonlinear system (as multi-carrier devices) the nonlinear clusters to be modeled will be addressed independently, which will facilitate the parameter extraction and possibly reduce the needed parameters for the entire model. Once again, the suggested multi-carrier Volterra model will be a collection of different sub-models for each nonlinear cluster that are being extracted individually.

The underlying concept of the proposed model is depicted in Fig. 3.10 for the nonlinear clusters associated to the carrier's one and two, lower and higher cross-modulations of second-order and third-order cross-modulations arising from $2\omega_1$-ω_2 and $2\omega_2$-ω_1. This proposed model could be extended to account for an augmented number of mixtures occurring in the multi-carrier nonlinear device but, obviously increasing the model complexity.

For example, the mathematical description to the signals centered at carrier one (or two) zone should account for several contributions such as: linear signal output; in- and out-of-band self-modulations; and in- and out-of-band cross-modulations:

$$\begin{aligned}\tilde{y}_{C_1}(k) = &\sum_{q_1=0}^{Q_{C1}} \tilde{h}_{1,C_1}(q_1)\cdot\tilde{x}_1(k-q_1) \quad + \\ &\sum_{q_1=0}^{Q_{C1}}\sum_{q_2=q_1}^{Q_{C2}}\sum_{q_3=q_2}^{Q_{C3}} \tilde{h}_{3,C_1}(q_1,q_2,q_3)\cdot\tilde{x}_1(k-q_1)\cdot\tilde{x}_1(k-q_2)\cdot\tilde{x}_1^{*}(k-q_3) \quad + \\ &\sum_{q_1=0}^{Q_{C1}}\sum_{q_2=q_1}^{Q_{C2}}\sum_{q_3=q_2}^{Q_{C3}} \tilde{h}_{3,CM_3}(q_1,q_2,q_3)\cdot\tilde{x}_1(k-q_1)\cdot\tilde{x}_2(k-q_2)\cdot\tilde{x}_2^{*}(k-q_3)\end{aligned} \tag{3.12}$$

where $h_{1,C1}$ is the linear signal kernel, $h_{3,C1}$ and $h_{3,CM3}$ are the third-order kernels for the self-modulation and cross-modulation responses, respectively.

As well, the lower second-order cross-modulation arises from a second-order multiplication:

$$\tilde{y}_{CM_2L}(k) = \sum_{q_1=0}^{Q_{A1}} \sum_{q_2=q_1}^{Q_{A2}} \tilde{h}_{2,CM_2L}(q_1, q_2) \cdot \tilde{x}_2(k-q_1) \cdot \tilde{x}_1^*(k-q_2) \tag{3.13}$$

The remaining nonlinear components are obtained in a similar reasoning. Moreover, if higher orders are needed, then more Volterra kernels should be determined. The determination of the low-pass complex Volterra kernels was again based in a least-squares extraction.

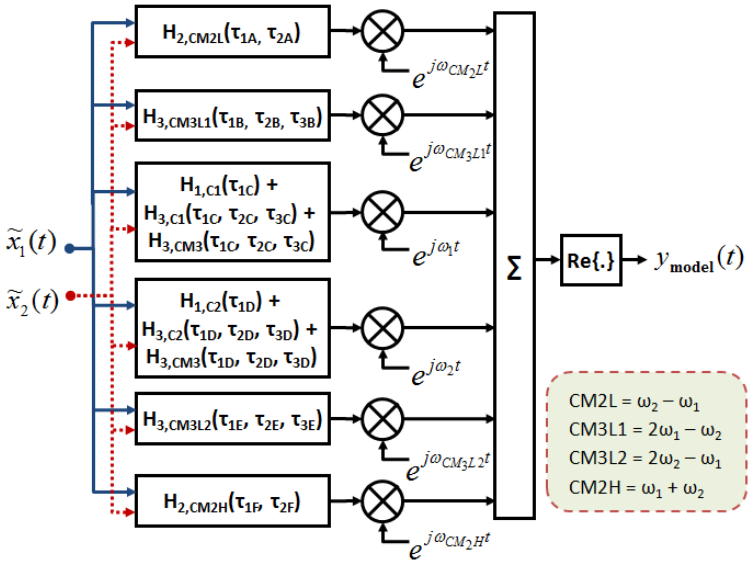

Fig. 3.10 – Proposed design for the multi-carrier nonlinear behavioral model.

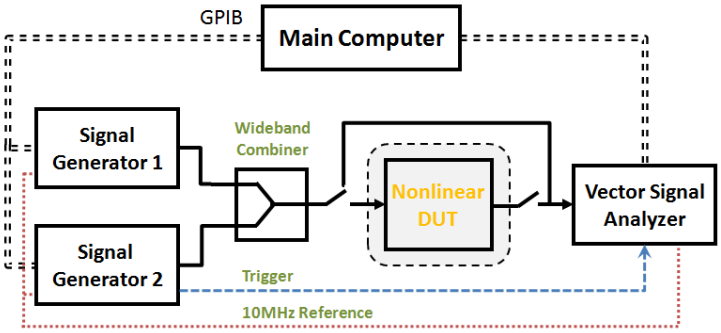

Fig. 3.11 – The experimental test bench used.

3.2.3 Measurements Validation

For this case study the nonlinear device was represented by a commercial wideband amplifier with a 1-dB compression point of +11 dBm and an approximate gain of around 23 dB. To do a correct characterization of the device and perform the necessary measurements a setup as displayed in Fig. 3.11 has been implemented. As can be observed two signal generators followed by a wideband combiner are used in order to produce the input signals, and a vector signal analyzer to directly acquire the input complex envelopes and desired output complex envelopes (carrier one; carrier two; 2^{nd}-order cross-modulations; 3^{rd}-order cross-modulations; etc.).

Then, in order to evaluate the performance of the proposed behavioral model the device has been excited by two simultaneous multisine signals, the first with 11-tones carrying random phases in a bandwidth of 1 MHz and the second composed of 21-tones with random phases in a bandwidth of 2 MHz. The average input power of each signal was set to -24 dBm and the selected carrier frequencies were fixed at 200 MHz and 350 MHz for the first and second excitations, respectively.

The obtained results are shown in Fig. 3.12 and Fig. 3.13. There it can be roughly observed that the proposed behavioral model and parameter extraction is estimating well the unknown parameters and producing quite similar results. It was also verified the integrated power in several important bands and the results are exposed in Table 3.D. As a final confirmation of the model performance, a calculation of the normalized mean squared error (NMSE) for the two carriers was done and resulted in -32.4 dB for the first excitation and -27.5 dB for the second excitation executed in the time envelopes shown in Fig. 3.14.

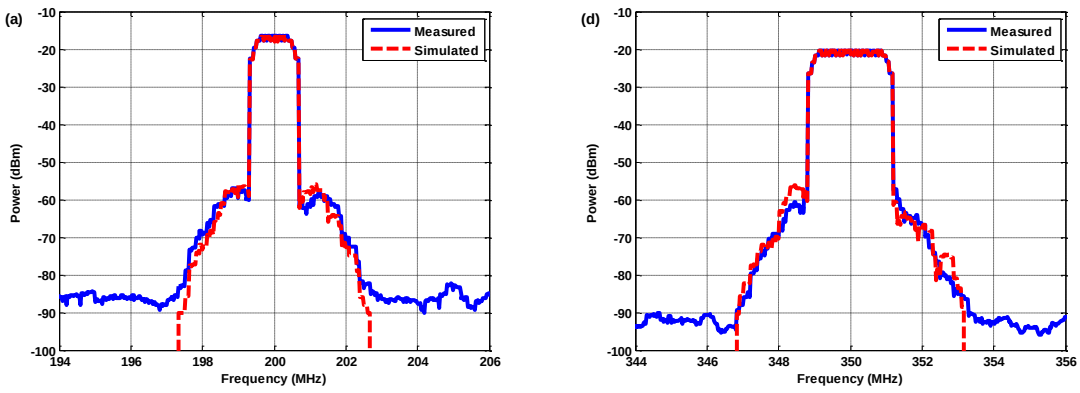

Fig. 3.12 – Measured and simulated results of the spectrum at carrier one (left) and spectrum at carrier two (right).

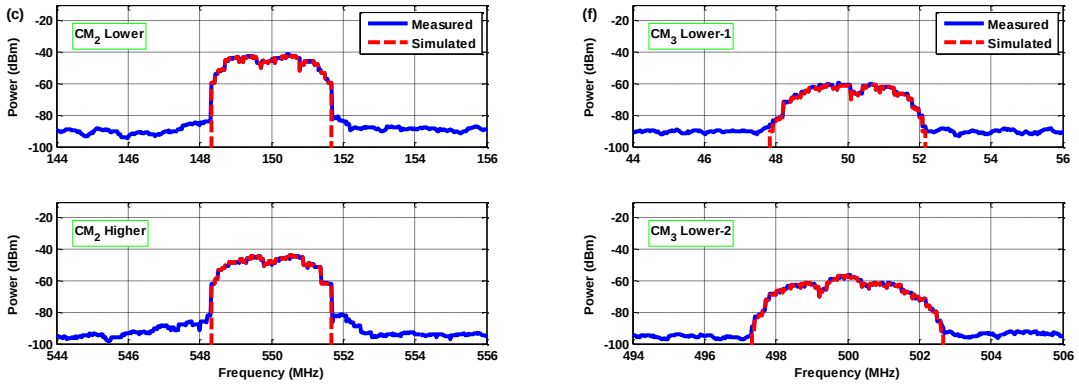

Fig. 3.13 – Measured and simulated results of the spectrum at 2nd-order cross-modulations (left) and spectrum at 3rd-order cross-modulations (right).

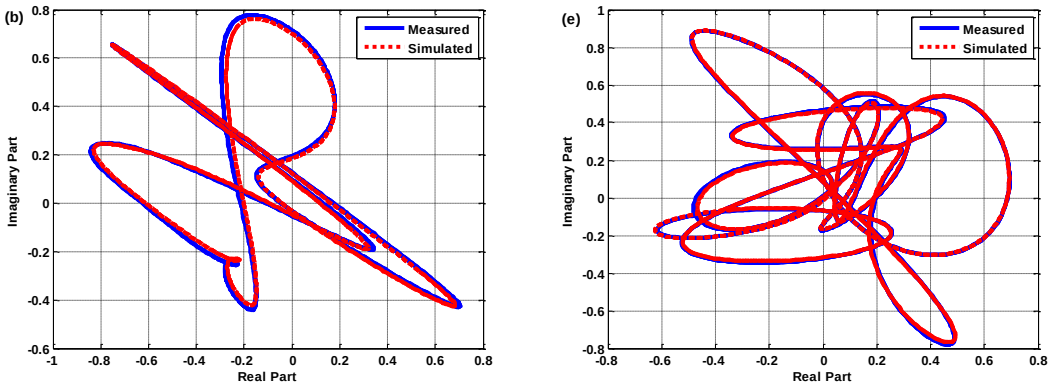

Fig. 3.14 – Measured and simulated results for the time envelope of carrier one (left) and time envelope of carrier two (right).

Table 3.D – Measured and simulated output powers for each nonlinear cluster.

	Meas. [dBm]	**Model [dBm]**			**Meas. [dBm]**	**Model [dBm]**
Carrier 1	-6.17	-6.27		*CM_2 Lower*	-29.7	-29.7
Adj. Ch.-C_1 (Lower)	-48.0	-47.7				
Adj. Ch.-C_1 (Higher)	-48.8	-47.9		*CM_2 Higher*	-32.2	-32.1
Carrier 2	-7.24	-7.26		*CM_3 Lower-1*	-47.3	-47.5
Adj. Ch.-C_2 (Lower)	-50.7	-48.2				
Adj. Ch.-C_2 (Higher)	-49.9	-52.0		*CM_3 Lower-2*	-45.2	-45.2

3.3 Concluding Remarks

In the previous sections different wideband behavioral models have been proposed covering both single and multi-carrier excitations. The proposed models are based in Volterra series matching of input/output measurements and have been practically validated in one case for a BPSR design and in the other case for a nonlinear amplifier.

It should be emphasized that both strands of the models are suitable for large bandwidths as demonstrated for the two case studies. This is due to the specific structure of the innovative parameter extraction scheme based in a low-pass equivalent format that considers each nonlinear cluster separately.

Even though both models have been explained and validated considering third-order degree nonlinearities, they can be practically extended to higher nonlinear orders and number of excitations.

As well, these new behavioral models may facilitate in the future straightforward implementations of digital linearizers, either for receiver side or for transmitter side, which would allow an improvement in the performances of the devices/systems modeled.

These statements allow me to conclude that the scientific state-of-the-art has been extended in the fields of nonlinear modeling and characterization dedicated to SDR and CR approaches.

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Chapter 4 – Dynamic Range and Bandwidth Constraints

To make SDR and CR technology a reality, the RF front-ends must be able to operate with large bandwidths in order to handle multiband and multi-carrier wireless signals. Also, high dynamic range is a prerequisite to allow the simultaneous reception of low power signals combined with high power ones in multi-carrier scenarios.

These requirements are tough challenges to be solved or at least minimized and must take profit from digital-aided implementations as a way to allow improved performances when compared to existent solutions.

The proposed alternatives will always have in mind a real-world implementation perspective, attempt to impose the less degradation possible on the incoming signals and will be focused on multiband and multi-carrier SDR/CR designs.

The chapter is supported in paper [C4] for initial contributions on receiving dynamic range improvement, in paper [J3] that is, at the moment, in review process and aims to contribute on the increase of instantaneous dynamic range in multi-carrier wideband digital receivers, and in paper [C5] for contributions on the bandwidth maximization of digital receivers for SDR/CR application.

4.1 Dynamic Range in Wideband Receivers

To start this discussion several concepts about dynamic range and its importance in multi-carrier wideband digital receivers will be given. A digital receiver [6] offers several advantages over their analog version because once a signal is digitized, the subsequent signal processing will be entirely done at the digital domain, allowing highly flexible and adaptable designs. These types of receivers become even more attractive due to the constant advancements in ADCs and FPGA/DSPs speeds and capabilities.

Assuming that dynamic range of a certain radio receiver is essentially the range of signal levels over which it can operate, it is not always easy to compare one set with another because it can be quoted in a couple of ways. Therefore, in order to clarify the concept of receiver dynamic range, two different cases will be considered, single signal dynamic range and instantaneous dynamic range.

The single signal dynamic range is understood as the ratio between the strongest signal power properly received without being clipped and the lowest signal power properly detected by the receiver (sensitivity level). Contrarily, instantaneous dynamic range is related to the power ratio of the maximum and minimum incoming signals that can be properly received at the same time. For instance, considering these definitions it is possible to have a receiver with 60 dB of single signal dynamic range, but having only 20 dB of instantaneous dynamic range, as can be understood in Fig. 4.1.

For this kind of digital receivers the ADC is typically one of the limiting components because of its fixed dynamic range, which is delimited up and down by certain intrinsic characteristics. Ideally, the low end of the range is governed by the SNR referenced to the ADC full-scale input, which is controlled by the inherent quantization error. This quantization error varies with the ADC number of bits, and the best case SNR is given by:

$$SNR_{dBFS} = 6.02 * N + 1.76 \tag{4.1}$$

where N is the number of bits of the ADC. Equation (4.1) is only valid if the noise is measured over the entire Nyquist bandwidth, whereas if the signal bandwidth (BW) is less than $f_s/2$, the achievable SNR may be increased and, thus, a more correct expression for this condition is given by:

$$SNR_{dBFS} = 6.02 * N + 1.76 + 10 * \log_{10}\left(\frac{f_s}{2 * BW}\right) \tag{4.2}$$

The above equation reflects the condition called oversampling, where the sampling frequency is higher than twice the signal bandwidth. Nonetheless, in a common receiver implementation, this low end limitation is managed most of the times either by the input noise floor or other associated effects, such as the clock and internal timing jitter [66] mainly when it is operating at higher frequencies (IF sampling).

On the other hand, the high end is governed by its overload or strong signal handling performance. In the ADC component, this is known as clipping distortion, which occurs when the input signal exceeds the ADC full-scale range and results in significant distortion (harmonic related or not) because the signal is rightly hard-clipped. This distortion is amplitude dependent and is of great importance in wideband multi-carrier digital receivers, due to the high PAPR of their signals and potential blockers in adjacent channels.

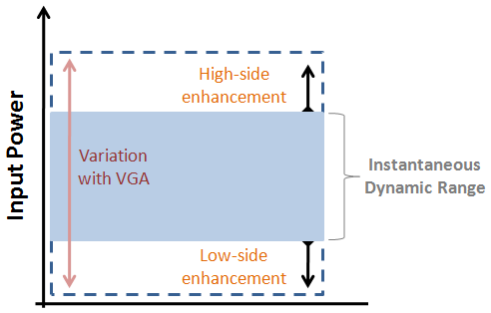

Fig. 4.1 – Illustration of limited instantaneous dynamic range and its potential improvements.

Taking into account what has been said, Fig. 4.1 presents a sketch that summarizes the limitations in terms of dynamic range and points where it can be improved, which is appointed by potential techniques to augment the high-side and low-side margins of the instantaneous dynamic range. Existent techniques to improve receiving dynamic range will be addressed in the following section.

As a result, considering the situation of a single signal excitation it is possible to use an automatic gain control (AGC) circuit to follow the power variation of that signal. In a typical AGC device, a feedback loop is used, wherein the output power level of this device is monitored and directly provides the regulation of the device gain itself, thereby maintaining its output power at a relatively constant level. For example, in a common situation the AGC device may be configured to maintain the output power level between the limits of the ADC dynamic range as close as possible to its upper limit in order to maximize the attainable SNR.

Nevertheless, a SDR/CR operating over multiple bands, it is likely to encounter signals with very different power levels, either by the conjunction of several desired high and low power signals or by the combination of strong interferences and weak received signals. Thus, in such a situation no AGC device can compensate for the varying signal strengths because reducing the gain to cope stronger signals will reduce the sensitivity to weaker ones. In some cases the received signal from one wireless standard can block another, for instance, when a Wi-Fi access point is nearby, yet one wish to receive a GSM signal having a much lower power [67].

Obviously, some sort of AGC (variable or stepped) will continue to be used in practical radios to prevent receiver overload but this should be managed in a careful way and accompanied by other instantaneous dynamic range enhancement techniques.

4.1.1 Techniques for Dynamic Range Improvement

As was seen in the previous chapter, it is very desirable to come up with techniques to extend the instantaneous dynamic range of ADCs. As a matter of fact, there are a few existing solutions to make such an improvement, which range from the addition of variable gain amplification preceding the ADC stage, non-uniform quantization based on compression and expanding the signal, averaging of several ADC outputs, as well as other practical alternatives such as, oversampling and interleaving followed by digital filtering. In the following we will briefly address the general operation of the referred solutions.

4.1.1.1 VGA plus ADC

One of the possible solutions that is widely used and valid in every receiver architecture, is to employ a variable gain amplifier (VGA) jointly with a power detector circuit before the ADC stage to execute the abovementioned AGC function. In principle, this will place the incoming signal within the ADC limited dynamic range allowing the linear digitization of the received signal and maximizing the respective SNR value.

However, considering the case of a multi-carrier wideband digital receiver, we might have high power signals simultaneously conjugated with low power ones, which makes the VGA working strategy totally impractical. This happens because the VGA commonly controls the exact gain to apply in the current signal by measuring the integrated average or peak power, which will only focus on the high-power signal and could lead to the actual loss of the lowest signals.

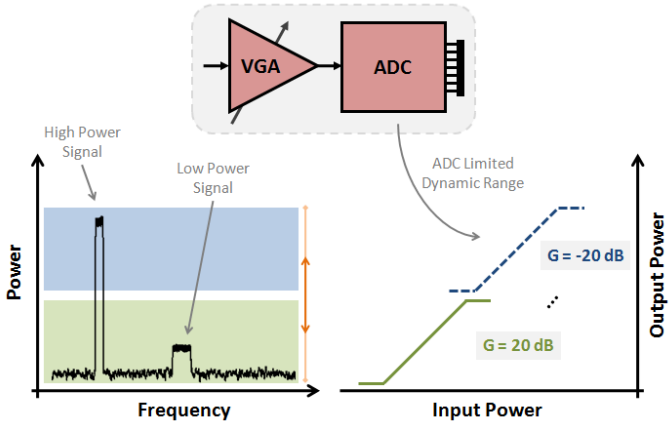

Fig. 4.2 – Explanation of the VGA plus ADC limitation when in a multi-carrier wideband scenario.

On the other hand, if the VGA is capable to decide which signal to follow and focus on the low-power signal, the associated gain would increase in order to receive the lower signal. However, in this situation, the high-power signal will completely saturate the upcoming device (ADC) and thus, generate a lot of distortion conducting to the loss of both signals. Fig. 4.2 shows in detail that varying the gain of the VGA does not truly increase the effective dynamic range of a multi-carrier system, just move up and down the fixed ADC dynamic range. Assuming that the dominant error is the ADC quantization, the VGA plus ADC will employ a constant error on the input signal despite its input power, as illustrated in Fig. 4.6 for a 4-bit (16 levels) quantization state.

4.1.1.2 Non-Uniform Quantization by Companding

A different approach that tries to overcome the limited ADC dynamic range issue is to perform non-uniform quantization on the input signal, [68], in order to concentrate the lower quantization levels in voltage regions with highest probability. In fact, observing the previous approach and especially Fig. 4.6, it can be detected that uniform quantization will be only optimal for uniformly distributed signals, which is not the experimented situation in actual wireless systems.

The works of Lloyd [69] and Max [70] are greatly recognized in the field of non-uniform quantization (also known as floating-point quantization), wherein an algorithm to determine the optimal (at a given time - require dynamic changes) non-uniform distribution of the quantization levels was proposed, which requires some knowledge about the distribution of the input signal. Although, the flexibility of this algorithm makes it seem attractive for SDR/CR applications, its implementation is unable to provide the required performance for wireless mobile applications. One difficult yet feasible solution to design a non-uniform quantizer is to directly implement the partition and respective reconstruction levels in the conversion process, i.e., purposely construct a non-uniform ADC, as for example in [71].

A much easier and practical approach can be achieved by first passing the input signal through a nonlinear function (“compressor”) followed a uniform quantizer and terminated by the inverse nonlinear function (“expander”), see Fig. 4.3.

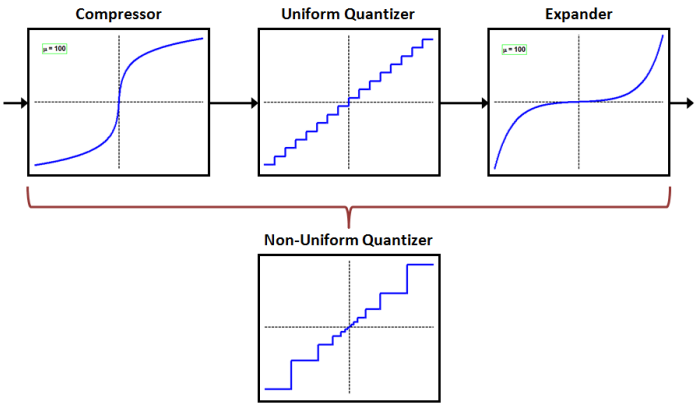

Fig. 4.3 – Block diagram implementation of the companding function.

The "compressor" and respective "expander" stages are represented by the following functions:

$$F(x) = sign(x)\frac{\log_{10}(1+\mu|x|)}{\log_{10}(1+\mu)} \qquad -1 \le x \le 1 \tag{4.3}$$

$$F^{-1}(y) = sign(y)\frac{\left[10^{(\log_{10}(1+\mu).abs(y))}-1\right]}{\mu} \qquad -1 \le y \le 1 \tag{4.4}$$

where x is the input signal at the "compressor", y is the input of the "expander", μ defines the degree of nonlinear compression, and *sign(a)* represents the signum function.

The complete process of these three consecutive stages is called "companding" and is the basis of μ-law and A-law algorithms [72], primarily used in the analog telecommunication systems to reduce the instantaneous dynamic range of audio signals. In a generic receiver implementation this approach may be realized by the use of a logarithmic amplifier (to perform the nonlinear gain curve) prior to the ADC device and then apply the inversion operation in the digital domain. Once again, assuming that the ADC quantization is the dominant error, the "companding" approach performs a non-uniform quantization as shown in Fig. 4.6 using a 4-bit quantizer and a μ value in the "compander" function (4.3) of one hundred. It is clear that the quantizing error affecting the input signal is smaller for low level values, which allows the signal to be represented more accurately and presents a larger error for higher level signals leading to a coarsely representation. Moreover, this technique performs an enhancement in the low-side of the ADC instantaneous dynamic range, when compared to Fig. 4.1.

4.1.1.3 Averaging Multiple Analog-to-Digital Converters

Another well-recognized approach to augment the receiving dynamic range can be performed by either parallelizing several ADCs and simply average the digital outputs or increasing (in multiples of two) the sampling rate of a single ADC and then use each other sample to average [73]. Nevertheless, this second option is less desirable because faster ADCs may not yet be available and a faster sampling clock with low jitter is required.

In this implementation, the signals are added directly, while the noise coming from each individual ADC if assumed to be uncorrelated will sum as the square root of the sum of the squares (root-sum-squares) which will improve the total SNR. The processing required to execute this functioning is commonly realized in a digital signal processor (e.g., FPGAs and DSPs).

Therefore, considering the case of two parallel ADCs having at the input a signal term (V_S) and a noise component (V_N) when applying this method it will result in a total output voltage that is given by:

$$V_T = V_{S\_ADC1} + V_{S\_ADC2} + \sqrt{V_{N\_ADC1}{}^2 + V_{N\_ADC2}{}^2} \tag{4.5}$$

So, the signal has effectively been multiplied by two, while the noise part has been multiplied by $\sqrt{2}$, thereby increasing the achievable SNR by a factor of $2/\sqrt{2}$ or 3.01 dB. As well, if more ADCs are implemented in parallel we may get even more improvement on the SNR value, yielding around 6 dB using four equivalent ADCs, and so on. Theoretically, the achievable enhancement is dictated by the number of used ADCs (N) as $10*\log_{10}(N)$ decibels.

Obviously, this finding will only be true if the root-sum-square of the non-correlated noise sources (thermal noise, clock jitter noise, etc.) is higher than the intrinsic ADC quantization noise. Thus, an improvement in the overall noise floor may be obtained but its effectiveness is highly dependent on the characteristics of its dominant noise sources. Nonetheless, this averaging technique is able to reduce the uncorrelated noise power but has no effect on distortions inherent to the specific ADC design, improving in that sense the SNR, but not the spurious free dynamic range. Moreover, the accomplishment of a system like this requires a huge design effort and strictly careful processes on the prototyping, qualification and testing phases. As in the case of the technique shown in the

previous section, this procedure enhances the low-side of the ADC instantaneous dynamic range, as regards to what was presented in Fig. 4.1.

4.1.1.4 Other Feasible Techniques

Other proposed techniques include oversampling and interleaving of ADCs, [74] and [75]. As previously mention in chapter 4.1 (above) and pointed out in expression (4.2), sampling a signal with a rate higher than twice of the bandwidth can bring gains in terms of signal SNR. Actually, the faster the signal is sampled the lower will be the noise floor, since having a constant total integrated noise it will spread out over more frequencies. However, the full effect of this process can only be achieved when the signal is decimated and filtered. Moreover, using the last part of (4.2), it is possible to observe that each time the sampling rate doubles the effective noise floor will improve by an amount of 3 dB.

On the other hand, instead of increase the sampling of a single ADC we could interleave several ADCs, which equally allow the sample rate to be increased and obtain SNR improvements in the same fashion. In order to realize this, each ADC should be drove with clock signals properly phased. This fact may create implementation difficulties when compared to the averaging method, because in that case the clock signals can be derived directly from a common signal splitter, as apart the interleaved situation requires a more complicate circuit. In addition, when time-interleaving ADCs it is common to obtain, in the reconstructed output, beyond the desired signals other non-harmonic distortion products known as offset and image spurs, [76], which are directly related to channel-to-channel gain, phase and offset matching errors. Thus, a very tight channel matching condition is required when searching for high SNR values.

In summary, oversampling and time-interleaving represent non-direct methods to increase the receiving dynamic range. Also, these two techniques are more complex to implement than the averaging procedure described above, but these should not be discarded due to their potential effectiveness in specific situations.

4.1.2 Proposed Architecture for Dynamic Range Enhancement

This section is devoted to explain a novel technique to increase the instantaneous receiving dynamic range when subjected to wideband multi-carrier excitations. A first approach to this technique has started in [C4] where a comparable architecture

accompanied by a digital reconstruction procedure was validated by several simulations for a single-carrier application.

The proposed architecture is based on a coupler followed by two parallel paths of ADCs sampled with equally phased clocks and then, digital signal processing is applied to reconstruct the incoming signal. A block diagram for the proposed design is sketched in Fig. 4.4. A quick look into a few scientific publications encounters similar strategies employed in different fields of applications, such as in power meters [77] and in successive detection logarithmic amplifiers [78].

The main idea of the proposed architecture is to pass, as much as possible, to the digital domain the required processing in the sampled waveforms to then digitally reconstruct the incoming information. In this way, the signal that comes from subsequent RF/IF front-end components pass through a passive coupler that separate the signal into two different portions, the highest part goes to the output being feed to ADC_1 and a small part of the signal is coupled with a certain coupling ratio and goes to ADC_2. As can be seen in Fig. 4.4, the input signal is intentionally clipped in the upper ADC_1 in order to take full profit from the ADC_1 dynamic range. Afterwards, digital signal processing is used in the two digitized waveforms to reconstruct the incoming signal. It is fair to say that more parallel paths can be added resulting in higher dynamic range but also in a highly complex implementations. An important part of the proposed architecture rely on the capabilities provided by current digital processors to execute the digital reconstruction of the received signal, which is performed in a discrete-time sample-by-sample approach and its flowchart diagram is depicted in Fig. 4.5.

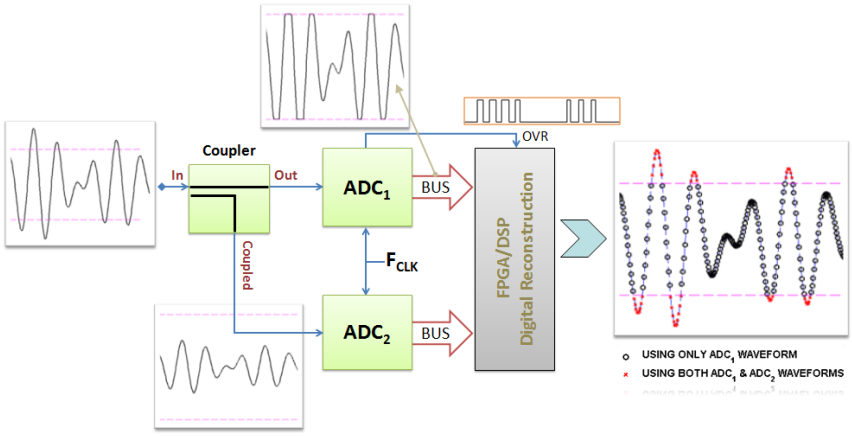

Fig. 4.4 – Proposed architecture to enhance the receiver instantaneous dynamic range with representative waveforms in relevant branches.

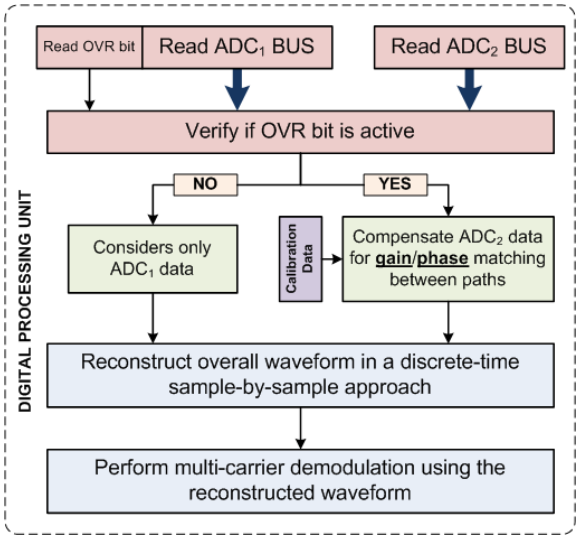

Fig. 4.5 – General flowchart diagram of the digital reconstruction procedure.

The digital processing unit has to read the two ADC buses and an over-range indicator bit (OVR bit). Then, this OVR bit is used to control whether the information from the two ADCs is used or not in the signal reconstruction procedure. If it is inactive, only the data from ADC_1 is considered from these specific time samples, but if it is active, the data from ADC_2 is compensated with gain and phase values obtained during a calibration period and used in conjunction with ADC_1 data to reconstruct the received signal.

Assuming once again the ADC quantization as the dominant error, the proposed design will work with two different constant quantization errors, as shown in Fig. 4.6 considering a 4-bit quantizer. Looking to that figure we can say that the improved performance of the proposed architecture is dependent on the statistics of the input signal, i.e., if the signal is mainly concentrated in the smaller values, then the minimum quantization error will be considered, while the large quantization error will be applied only to the high peaks of the input signal.

In that sense, Fig. 4.7 presents several probability density functions (PDF) for different wireless signals conjunctions. Over imposing these PDFs on the quantization patterns and respective errors depicted in Fig. 4.6, it can be stated that the proposed architecture when compared to the others is able to take advantage from the statistical distribution of the typical wireless input signals because they are mainly concentrated on the lower quantization part, except the constant envelope signals, as for instance a GSM signal.

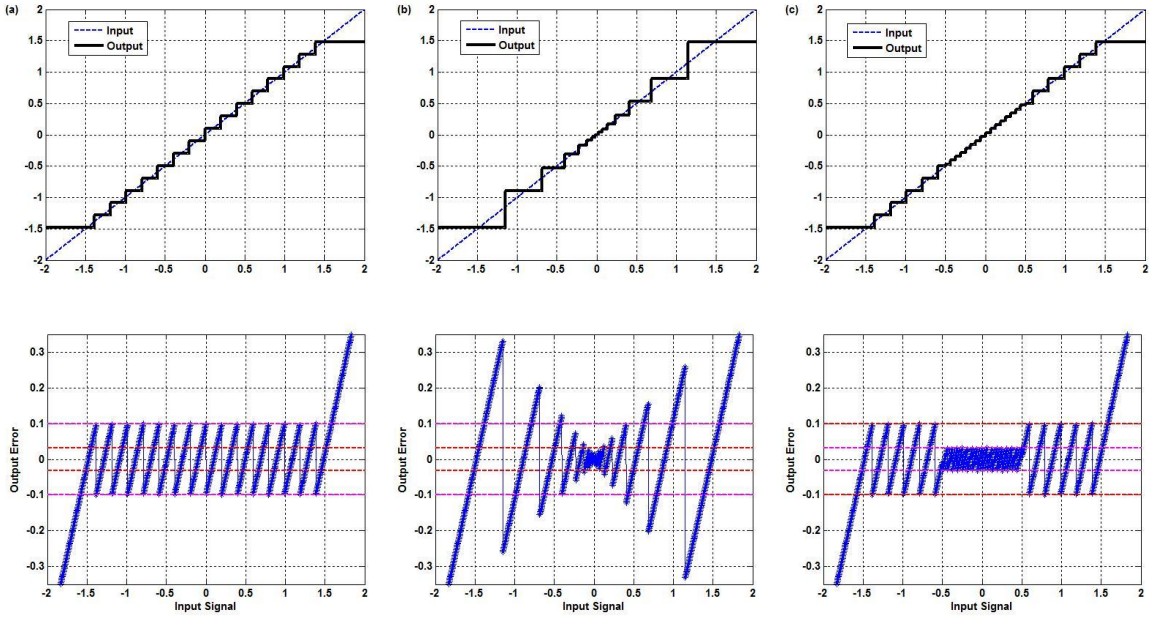

Fig. 4.6 – Different types of quantization (4-bit case) schemes produced by the different architectures: (a) VGA plus ADC, (b) companding, and (c) proposed.

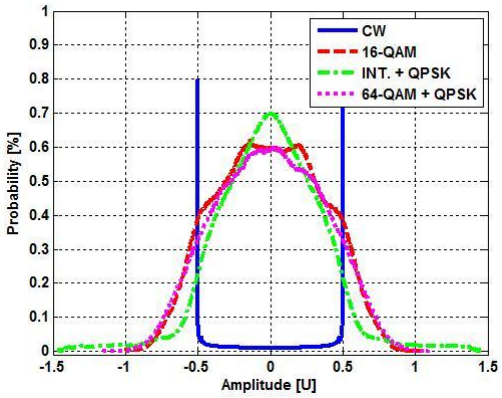

Fig. 4.7 – Probability density functions of different signals.

Therefore, a correct evaluation of the input signal statistics mainly for wideband multi-carrier excitations [5] should be done in order to search for an optimal driving point that maximize the achievable dynamic range with the proposed architecture.

In summary, the instantaneous receiver dynamic range can be increased by using the proposed technique, which provides gains that are dependent on the employed coupling ratio and input waveform PAPR. Also, contrarily to the techniques described along chapter 4.1.1 (above), which focus on the low-side of the ADC dynamic range, the proposed technique is projected to enhance the high-side of the ADC instantaneous dynamic range.

This functionality makes it suitable to receive high PAPR signals, typically in OFDM based systems, to resist to undesired strong interference signals, and to work on multiband multi-carrier scenarios.

4.1.3 Measurement Results

In order to validate the proposed architecture for instantaneous dynamic range enhancement two laboratory prototypes have been implemented one for the VGA plus ADC and another for the proposed architecture. A practical validation of the companding architecture was not prepared mostly due to the weaker results obtained in the simulation experiments available in [J3], but also because of the difficulty in the implementation, mainly in the process of calculating the exact inverse logarithmic function.

In these laboratory experiments a VGA device has been used for the driving of the proposed architecture as in the case of the VGA plus ADC design. Thus, in both cases a commercial stepped-gain VGA was employed being the gain parameter adjusted in order to drive each design at the associated optimal point. A commercial wideband directional coupler with around 10 dB of coupling (ZFDC-10-21 from Mini-Circuits) was connected to this VGA, followed by two parallel 8-bit ADCs, which were properly clocked in phase using the same sinusoidal signal. Obviously, for the VGA plus ADC case it was just followed by a similar 8-bit ADC. The laboratory setup implemented is shown in Fig. 4.8, in which it is possible to identify two independent signal generators used because of the very different power levels addressed for each specific input signal.

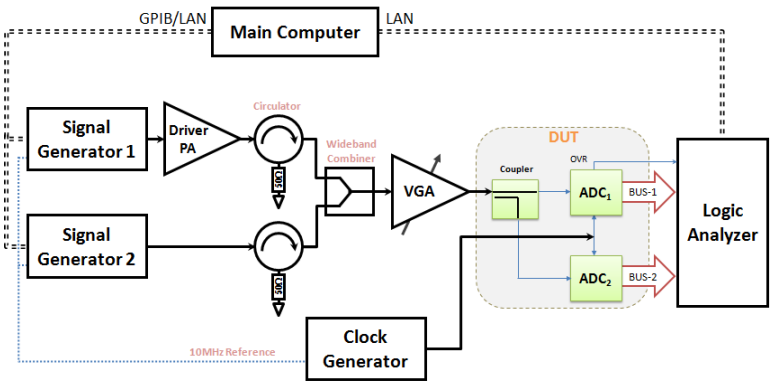

Fig. 4.8 – Laboratory setup used in the measurement validation example.

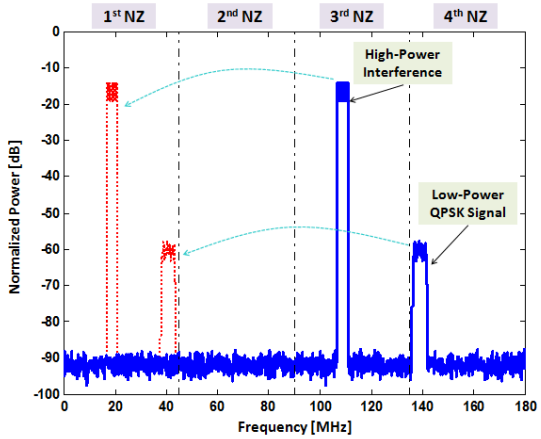

Fig. 4.9 – Multi-carrier signal composed of a high-power interferer and a low-power QPSK signal, before (solid line) and after BPSR procedure (dashed line).

The measurement validation procedure was based on a multi-carrier excitation subjected to a digital IF receiver with bandpass sampling characteristics (see chapter 2.1, above), which attempts to assess the impact of a high-power interferer in a low-power QPSK modulated signal. An illustrative input spectrum is shown in Fig. 4.9.

In that way, the high-power interferer is performed by a multisine signal carrying random phases in a bandwidth of 2 MHz and centered at 109 MHz (3rd NZ) appearing in the output after bandpass sampling at 19 MHz. The low-power QPSK signal is situated at a carrier frequency of 139 MHz, transmitting a symbol rate of 5 Msymb/s and filtered by a RRC filter with a roll-off factor of 0.22, determining a conjugated PAPR of 9.2 dB.

Thus, in order to determine the truly dynamic range of each design, the input power level of the interferer was fixed at +10 dBm and the QPSK signal has been swept between -20 dBc and -45 dBc, and then the resultant QPSK EVM has been calculated.

The obtained measured results for the two evaluated architectures are shown in Fig. 4.10, wherein the achieved simulation performance is also plotted. Analyzing the figure we can observe a great improvement in the instantaneous dynamic range by the proposed architecture. This means in other words that we still continue to properly demodulate a signal being received at a lower input level. Also, it is obvious the nice matching of the measured results against the simulations, accessible in [J3], with just a small degraded performance. These deteriorated results are mainly because of higher laboratory instrument noise levels and non-ideal performance of ADCs, likewise sampling clock jitter and small time misalignments between paths that adds phase mismatch and thus, further degrading

the overall SNR. Additionally, the constellation diagrams for the low-power QPSK signal measured for each design at different input power levels are plotted in Fig. 4.11. This confirms again the better performance of the proposed architecture compared to a VGA plus ADC design.

Thus, it could be said that in a wide-ranging observation the conjunction of obtained results verifies the proper operation of the proposed architecture for dynamic range improvement under realistic signal environments.

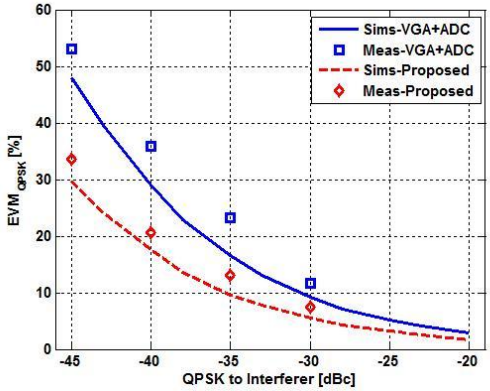

Fig. 4.10 – Measured EVM for a low-power QPSK signal received simultaneously with a high-power interferer for the VGA plus ADC and proposed cases.

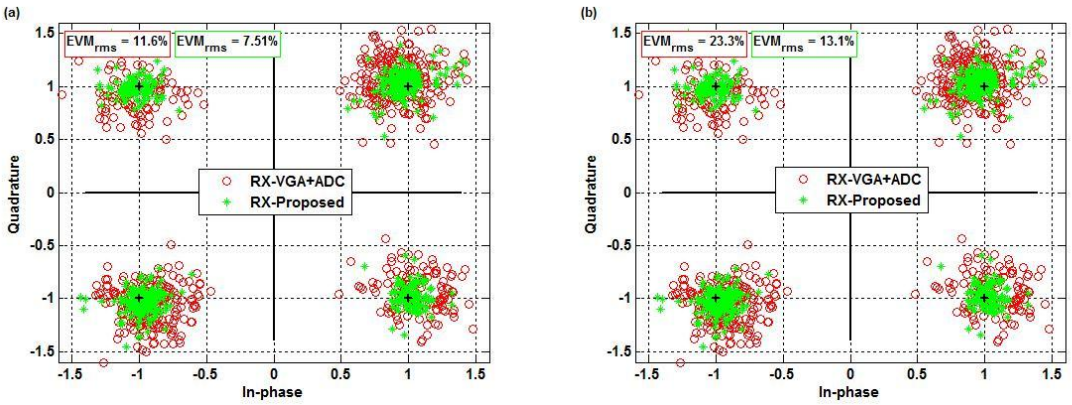

Fig. 4.11 – Constellation diagrams of the low-power QPSK signal for the VGA plus ADC and proposed architectures, when received at (a) -30dBc and (b) -35dBc to the interferer.

4.2 Bandwidth Maximization by Second-Order Sampling

It has been said in the previous chapters that digital receivers are advantageous because once the signal is digitized all the capabilities of signal processing can be exploited. The process of converting the signals between domains is only possible by the ADCs and DACs, which became crucial components for the next frontier SDR/CR solutions. Until now nothing has been referred about the complexity to implement such wideband receiving bandwidths.

A possibility could be to continuously increase the sampling rate of those data converters, but this will increase the switching speed of the internal circuitry forcing a raise on the device power consumption and thus reducing the overall system efficiency.

An interesting alternative is the use of second-order sampling approaches [9] (also known as complex sampling) to augment the working bandwidth and associating this to bandpass sampling [27], allowing higher frequency signals to be sampled at lower sampling rates, see chapter 3.1 (above) for details about BPSR.

So, the first step is to understand the principles behind these different BPSR schemes [10]. A general block diagram to implement this concept is presented in Fig. 4.12. The underneath idea is to separate the incoming signal into two paths having equal amplitude performance over the frequency band of interest and shifted by 90º in terms of phase description. This is known as the Hilbert transformation and has a frequency response as:

$$H(f) = \begin{cases} -j, & 0 \le f < f_A \\ +j, & -f_A \le f < 0 \end{cases} \tag{4.6}$$

Nevertheless for the microwave community this can be approximated by a broadband 90º phase shifter.

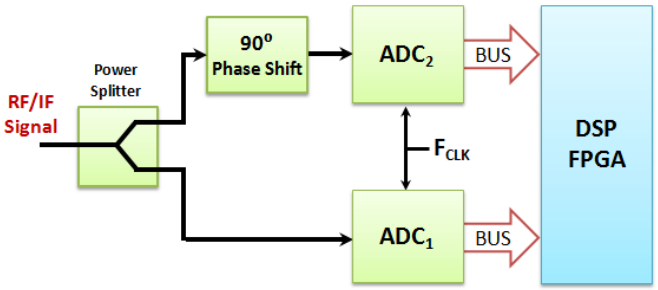

Fig. 4.12 – General block diagram of a second-order BPSR.

In the ideal situation, by pursuing such an approach should be possible to completely eliminate any image signal created either in the sampling process or actually present at the input of the system. In this sense, the use of both positive and negative parts of the incoming spectra will be possible doubling the working bandwidth when compared to a single path, as for example, the case of a first-order bandpass sampling receiver, see chapter 3.1 (above).

However, it is known that analog implementations are not perfect and suffer from several impairments. Therefore, when employing such a design in wideband receiver architectures, it would be expected that the Hilbert transform requirements (equal amplitude and 90º phase balances) are not perfectly fulfilled. Considering the path without 90º phase shift as I-path and the one with 90º shift as Q-path, the I/Q imbalance of such a system is defined as:

$$\begin{pmatrix} S_I'(t) \\ S_Q'(t) \end{pmatrix} = \begin{pmatrix} 1 & 0 \\ -g\sin(\varphi) & g\cos(\varphi) \end{pmatrix} \begin{pmatrix} S_I(t) \\ S_Q(t) \end{pmatrix} \tag{4.7}$$

where $S_I(t)$ and $S_Q(t)$ are the signals at the input, $S_I'(t)$ and $S_Q'(t)$ represent the signals after the imperfect system, and g and φ are amplitude and phase imbalances, respectively. Thus, the created amplitude and phase imbalances will induce an imperfect image rejection and achieve a certain sideband suppression, which is given by:

$$Sideband\_Suppression(dBc) = 10\log_{10}\left(\frac{g^2 - 2g\cos(\varphi) + 1}{g^2 + 2g\cos(\varphi) + 1}\right) \tag{4.8}$$

As a matter of fact, this topic of second-order sampling has been attracting the interest of scientific community, which resulted in several works dedicated to evaluate different points of view. Those studies range from the construction of algorithms to determine optimum sampling frequencies [79] to the construction of digital compensation schemes based either on variable delay fixed interpolants [80] or fractional delay filters [81]. Anyway, those techniques do not present yet practical and feasible FPGA/DSP implementations with acceptable performances for multiband multi-carrier operation within different input power levels.

4.2.1 Proposed Design with Digital Compensation

A reflection on implementation constraints for this second-order BPSR is fundamental to design a feasible multiband architecture. In that sense, the proposed idea is based on the use of a 90º hybrid to approximate, in a limited but wide frequency range, the desired Hilbert transformation. To the author knowledge this is the first time that a hybrid solution is used in conjunction with digital compensation to implement a complex BPSR. The respective block diagram is shown in Fig. 4.13. As can be seen, the ADCs share an equal clock signal that facilitates the circuit implementation and takes profit from digital signal processing elements to make use of entire sampled bandwidth.

Additionally, by looking to Fig. 4.14 it is possible to witness that a simple commercial hybrid presents very interesting characteristics in terms of amplitude and phase imbalances (relatively constant over the measured band) even for different input powers, which allow the execution of wideband Hilbert transformation with satisfactory sideband suppression.

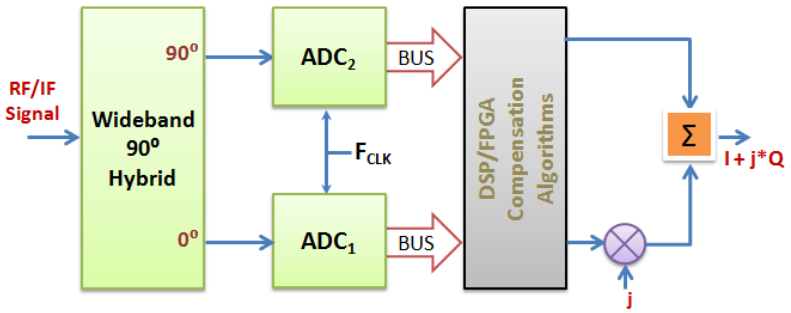

Fig. 4.13 – Block diagram of the proposed design for complex BPSR.

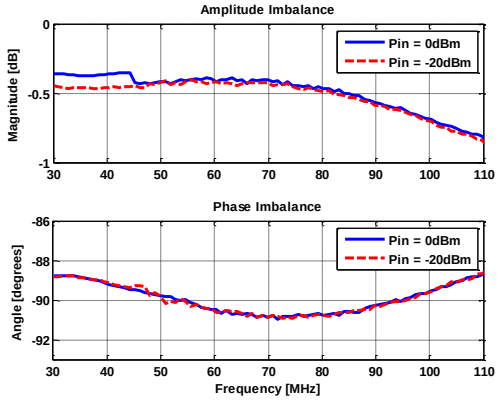

Fig. 4.14 – Performance of a commercial 90º hybrid within the band of interest measured in a commercial vector network analyzer.

Similarly to other receiving architectures the incoming signal has to previously be filtered and down-converted to reasonable IF frequencies. For example, Fig. 4.15 shows two signals (S_A and S_B) previously down-converted to the 2nd and 3rd NZ's respectively. Afterwards, the process of bandpass sampling will move it to the 1st NZ (positive and negative parts) and at same time create image components that are attenuated because of the used configuration. In the same way higher NZ's can be exploited for this second-order BPSR operation, as represented in Fig. 4.15 by the 4th and 5th NZ's (Band 2). Employing the proposed architecture and just by the single use of a 90º hybrid, image attenuations in the range of 30 to 35 dBc have been obtained.

In order to reduce even further these image components a simple compensation algorithm is implemented on the digital domain. At this point, the reverse matrix of equation (4.7) is directly applied on the previously received I and Q waveforms:

$$\begin{pmatrix} C_I(t) \\ C_Q(t) \end{pmatrix} = \frac{1}{\cos(\varphi)} \begin{pmatrix} \cos(\varphi) & 0 \\ \sin(\varphi) & 1/g \end{pmatrix} \begin{pmatrix} S_I'(t) \\ S_Q'(t) \end{pmatrix} \tag{4.9}$$

These C_I and C_Q waveforms are afterwards combined to generate the final complex output (C_I + j*C_Q). As can be understood the employed compensation scheme can only be optimal at a particular frequency. This fact allow us to optimize its operation to reject the high power signal images when falling close by to low power ones, permitting an enhancement on the respective SNR important for signal demodulation.

Also, because of its simplicity, the proposed design demands a lower processing power from the FPGA/DSP to obtain comparable image attenuations of existent architectures.

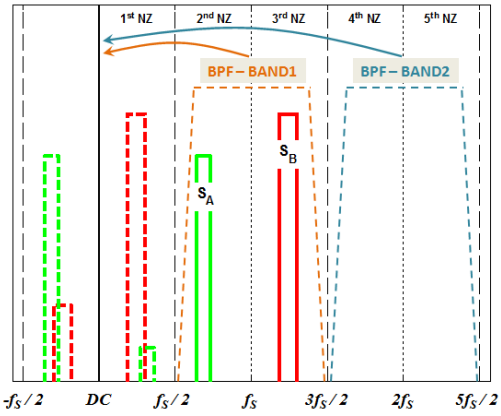

Fig. 4.15 – Frequency domain illustration of the working process for the proposed design.

4.2.2 Measurement Results

In order to validate the operation of the described complex BPSR architecture for the 2nd and 3rd NZ's (band 1 in Fig. 4.15), a demonstrator has been implemented using laboratory components. This was accompanied by a careful development of an experimental setup to characterize it. After the band-pass filter to select the desired band (35 MHz – 105 MHz) a commercial 90º hybrid (performances depicted in Fig. 4.14) has been used. This was then followed by a two-channel 10-bit pipeline ADC with a linear input range of approximately +10 dBm, an analog input bandwidth of 200 MHz and sampled with a clock frequency of 70 MHz. This value was chosen because of limitations on the laboratory components.

Then, several experiments were conducted in the proposed design. Firstly, the performance of the proposed architecture was evaluated when excited by two sinusoidal signals. The carrier frequencies chosen were 49 MHz and 88 MHz in order to fall in the 2nd and 3rd NZ's. The second test attempts to assess the performance when it is excited by a QPSK signal with 1.75 Mbps of symbol rate and being interfered by a multisine signal with 4 MHz carrying random phases. The last test consisted on the computation of the error vector magnitude (EVM) for two modulated signals being received simultaneously. In this situation we have used a 16-QAM signal centered at 88 MHz (which resulted in 18 MHz after bandpass sampling) carrying a symbol rate of 3.5 Mbps. The second channel has a QPSK signal with 1.75 Mbps and situated at 49 MHz (resulting in -21 MHz after bandpass sampling). The obtained results for the previous three experiments are presented in Fig. 4.16, Fig. 4.17 and Fig. 4.18. Analyzing those figures, it can be noticed by the shown frequency domain spectra's a high rejection of the image signals in the several tests conducted. Moreover, it should be stressed that the applied compensation scheme is able to further improve the image rejection obtained with the complex BPSR. As mentioned above, this compensation algorithm is focused on the lower power signal in a way to increase the associate SNR parameter, important aspect in the baseband signal demodulation. It can also be seen the improved QPSK demodulation when in presence of a multisine interferer. These differences could even be higher if the image signal falls on top of the desired one. As well, the calculated EVM values for the different situations addressed when varying the power levels of the input signals are demonstrated in Table 4.A and Table 4.B. There it can be observed that the proposed design is always better than

a single path situation, but the differences are not so noticeable because the image signal is not falling on top of the desired lower power signal.

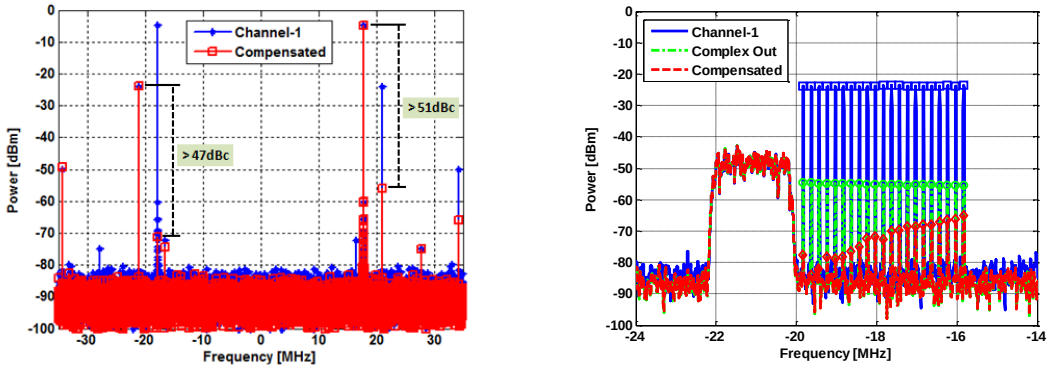

Fig. 4.16 – Frequency domain results for two sinusoidal signals (left) and a QPSK signal interfered by a multisine signal (right).

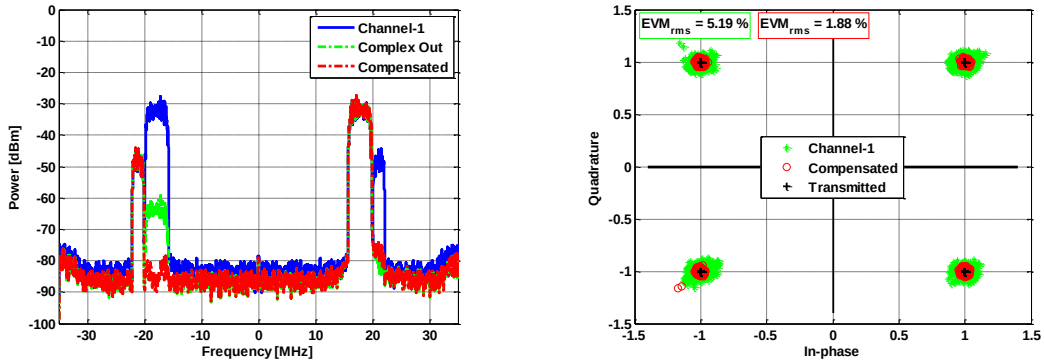

Fig. 4.17 – Frequency domain results for multiband reception (left) and signal demodulation of a QPSK signal under multisine interference for single path and proposed design (right).

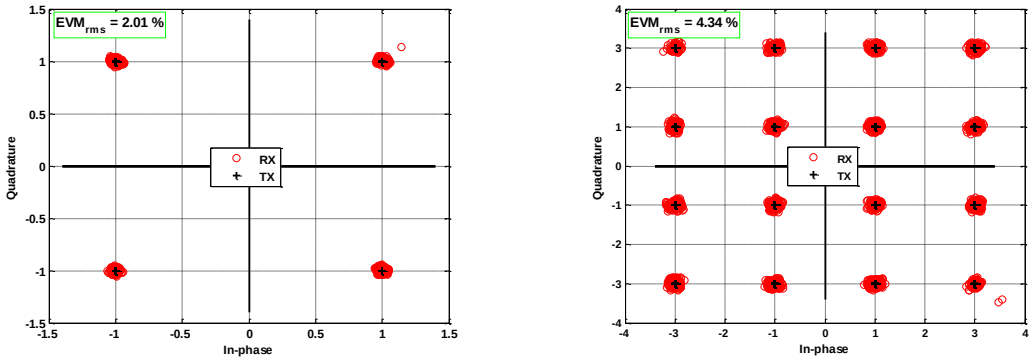

Fig. 4.18 – Signal demodulation results illustrating the QPSK and 16-QAM baseband I/Q information for a multiband reception system.

Table 4.A – Measured EVM results for a QPSK signal with a multisine interferer.

Pin (MS)	Pin (QPSK)	EVM (Proposed)	EVM (Single Path)
0 dBm	0 dBm	1.52 %	2.65 %
0 dBm	-10 dBm	1.49 %	2.78 %
0 dBm	-20 dBm	1.88 %	5.19 %
5 dBm	-5 dBm	1.48 %	2.66 %
5 dBm	-15 dBm	2.67 %	6.56 %

Table 4.B – Measured EVM results for multiband modulated signal reception using the proposed design.

Pin (16-QAM)	Pin (QPSK)	EVM (16-QAM)	EVM (QPSK)
0 dBm	0 dBm	1.33 %	1.77 %
0 dBm	-10 dBm	2.46 %	1.77 %
0 dBm	-20 dBm	4.34 %	2.01 %
5 dBm	-5 dBm	1.59 %	2.29 %
5 dBm	-15 dBm	3.86 %	5.91 %

4.3 Concluding Remarks

In the previous sections have been proposed innovative solutions for instantaneous dynamic range improvement and bandwidth maximization, which have been fully validated in laboratory environments.

Concerning on the dynamic range subject the proposed technique is capable to achieve substantial improvements when in rough scenarios, such as under strong interferences and multi-carrier operation that are very common situations to SDR and CR. It has been proved that in the worst case, the proposed solution can provide an increase of near 1-bit of resolution in conventional receivers. In summary, the proposed technique can improve significantly the operation of RF front-ends in real SDR/CR scenarios.

On what concerns to the bandwidth maximization topic, a novel and straightforward design for second-order BPSR based on passive 90º hybrids has been proposed. This will create room for potential improvement on the performance of current FPGAs and DSPs. As well, reductions in the overall system power consumption will be expected. Very promising results (focusing the high image rejection) were obtained by using a simple

digital correction algorithm conceivable in current FPGA solutions. Further developments can be then achieved in the digital compensation scheme to improve the image rejection for a wider operation.

Once again the previous stated achievements lead me to conclude that the state-of-the-art has been comprehensively improved in the fields of dynamic range and bandwidth maximization to SDR and CR approaches.

Chapter 5 – Conclusions and Outlook

In this thesis several ideas to solve current open issues in the SDR and CR fields have been proposed. Receiver and transmitter schemes were initially introduced and accompanied by pioneering mixed analog-digital instrumentation. The discussion was mainly concentrated on the specific usability for SDR and CR systems, [J1]. In what regards to the transmitter side, a relationship to determine the required PWM sampling frequency of switched PAs for different signals was shown, in which a direct dependency between the PWM coding efficiency and the resultant PA efficiency was recognized, [C1]. A new wideband behavioral modeling format for BPSR nonlinear operation was exhaustively presented, [C2] and [J2]. As well, an upgraded version of the former behavioral model has been executed for general multi-carrier nonlinear systems, [C3]. It was also addressed a new strategy for dynamic range improving in multi-carrier receivers, which takes profit from the careful wireless signals statistical conditioning, [C4] and [J3]. An advanced architecture for second-order BPSRs that maximizes the receiving bandwidth by improving the image sideband suppression has also been shown, [C5]. This short summary shows that this thesis has successfully focused on many diverse topics such as radio frequency transceivers, measurement instrumentation, behavioral modeling, multi-carrier excitations, dynamic range improvement and bandwidth maximization.

The work done in the area of nonlinear modeling and characterization is fairly advanced and is now asking for a widespread extension of the proposed principles into more real-world applications. In this line, the evaluation with actual wireless modulated signals in multi-carrier situations and respective linearization schemes to optimize signal quality should be a must. Even though, the used Volterra theory should be highly exploited for small/medium-signal characterization, in the meantime other possibilities have appeared as, for instance, the concept of X-parameters for large-signal characterization, which should also be considered because of their good performance and easiness of implementation. As well, the parameter extraction procedure should be maintained as accurate as possible and easily applied to real laboratory environments.

On what regards to the receiver dynamic range improvement there is sufficient future work to be done and should be directed to real implementations of the proposed structures. This implementation has to consider the construction of integrated on chip solutions to minimize non-idealities and mismatches and provide a wrapped solution for limited dynamic range of wideband receivers. Moreover, further evaluations can be executed by studying the impact of adding more parallel channels and changing the coupling level applied into each path. Concerning on the receiver bandwidth limitations, the strategy for future developments should consider real implementations of integrated on chip solutions to minimize non-idealities and mismatches, as in the previous case. In this sense, wideband passive 90^0 hybrids as the phase delay mechanism should be implanted in existent ADC solutions to allow the doubling of received bandwidth when in BPSR designs. Again, these designs should also be greatly improved on the digital compensation schemes to improve the image rejection for a wider band operation.

A topic that has not been thoroughly discussed in this thesis is the design of novel mixed analog and digital instruments that accounts simultaneously with both domains, which is of paramount importance and strategic for a correct evaluation of SDR/CR based transceivers. Having this in mind, in order to make practical and valid measurements, the proposed instruments should be fully calibrated in amplitude and phase for a range of input frequencies and powers, so that all specificities can be included in the measurement approach. This imposes that new manageable calibration schemes are also a key point for future work.

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Appendix A – Annexed Papers

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[J1] – Designing and Testing Software Defined Radios

Pedro M. Cruz, Nuno B. Carvalho and Kate A. Remley

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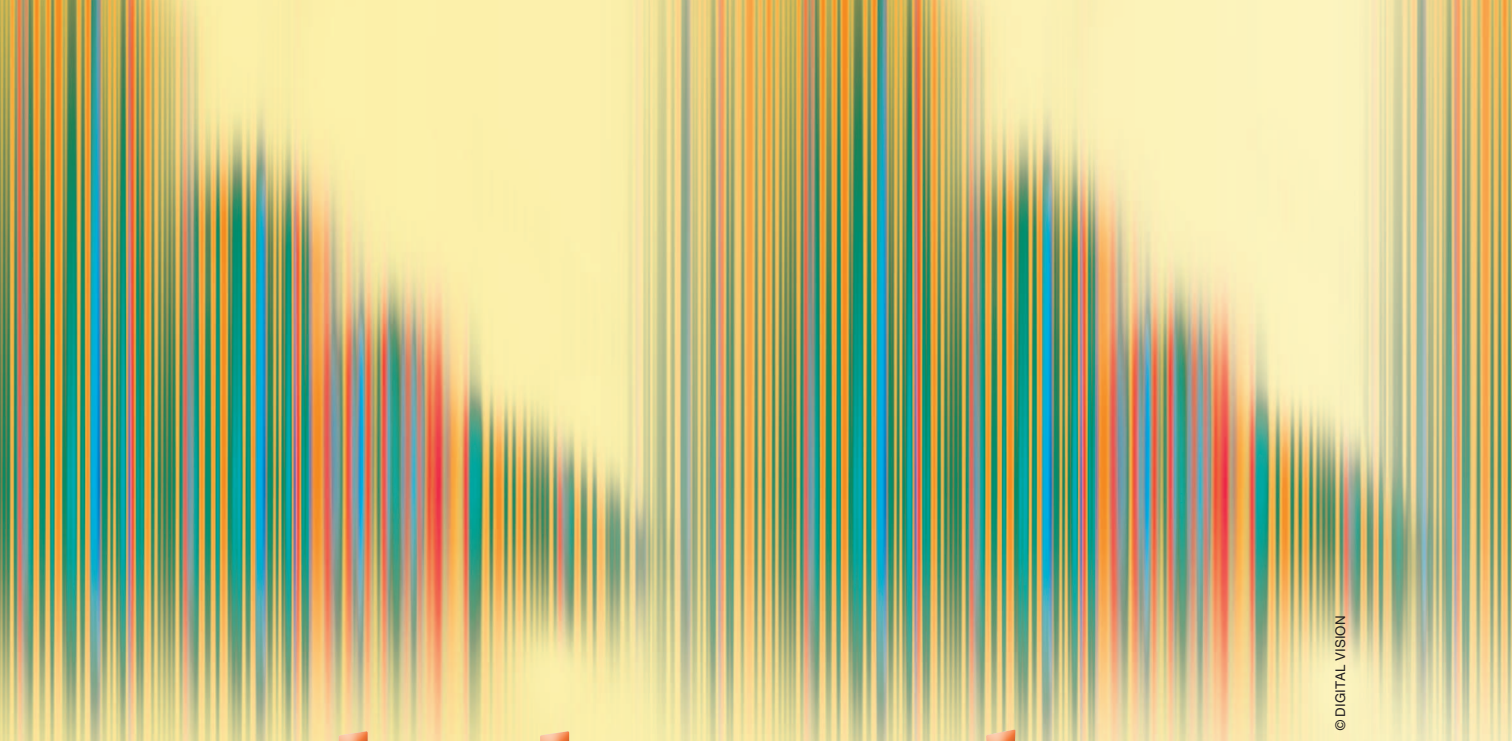

Designing and Testing Software-Defined Radios

Pedro Cruz, Nuno Borges Carvalho, and Kate A. Remley

Software-defined radios (SDRs) will play a key role in future radio configurations because the emergence of new wireless technologies and their integration in a fourth generation of communication standards will necessitate the use of multistandard and multiband radios. SDRs use a single hardware front end but can change their frequency of operation, occupied bandwidth, and adherence to various wireless standards by calling various software algorithms. Such a solution allows inexpensive, efficient interoperability between the available standards and frequency bands.

This article reviews the main parts of an SDR to emphasize several possible implementations of both receivers and transmitters. Many of these architectures are actually fairly old techniques that have been recently made practical due to the enormous increase in the capabilities of digital signal processors. We describe solutions for testing and

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characterizing these types of devices as well. SDRs typically operate in both the analog and the digital domains, thus mixed-domain instrumentation is necessary to carry out testing.

The concept of the SDR first appeared with the work of Mitola [1] in 1995. In this work, he proposed to create a radio that is fully adaptable by software, enabling the radio to adjust to several communication scenarios automatically. The concept is presented in Figure 1.

SDR front ends consist of the standard subsystems used in most transceivers: modulators and demodulators, frequency converters, power amplifiers (PAs), and low-noise amplifiers (LNAs). However, the modulation and encoding as well as the frequency of operation are determined in software. Such radios typically rely on digital signal processing (DSP) for much of their agility. The SDR is able to adapt itself to the transmission scenario in order to minimize interference to other signals that are present in the air interface. Implementation of such a system requires the ability to scan the spectrum from low to high frequencies using software. This concept has driven many researchers to study cognitive radio (CR) approaches, an idea also proposed by Mitola in [2], where the radio adapts itself to the air interface by optimizing the carrier frequency, modulation, and choice of radio standard to minimize interference and maintain communication in a given scenario.

One of the most promising applications of CR technology is to increase the spectrum occupancy by use of opportunistic radios, where the radio will utilize

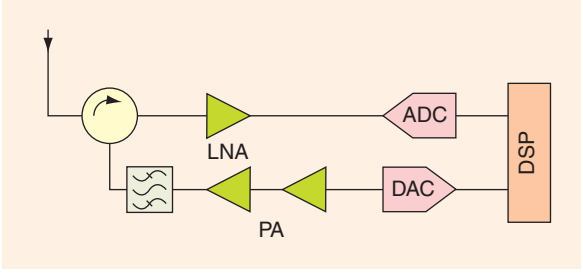

Figure 1. *Common implementation of the software-defined radio concept as described in [1]. A signal incident on the antenna port is routed to a low-noise amplifier (LNA) through a circulator and is then digitized. Demodulation and decoding are accomplished for a number of modulation formats and access schemes using digital signal processing (DSP). The transmission chain is the opposite: baseband signals are generated and up-converted in the DSP module, converted into analog waveforms, amplified, and bandpass filtered before passing through the circulator and antenna. (From [3], used with permission.)*

spectrum that is not being used by other radio systems at a given moment. In order to be able to implement this ideal solution, the radio should see and be aware of the entire spectrum and of the communications being used at a specific time.

The motivation behind the concept of SDR is not only the high flexibility to adapt the front end to simultaneously operate with any modulation, channel bandwidth, or carrier frequency, but also the possible cost savings that using a system based exclusively on digital technology could yield.

In this article, we first give a short overview of several architectures for SDR receiver front ends. Then, several possible architectures for transmitter front ends are described. We discuss methods that can be used to improve amplifier efficiency. Instrumentation currently available in the commercial market that allows the characterization of such types of transceivers is presented in the "Test of Software-Defined Radio Solutions" section. Finally, we summarize this work and identify the more probable solutions from our point of view.

Architectures for Software-Defined Radio Receivers

In this section, several front-end architectures that may be applied to SDR receivers are reviewed. This review is mainly based on [4] and [5].

The first configuration [Figure 2(a)] is the well-known superheterodyne receiver, where the signal received at the antenna is translated to baseband using two down-conversion mixers, bandpass filtered and amplified. The baseband signal is converted to the digital domain where it can be processed. Because of the first mixing process from RF to IF, it is mandatory to use an image-reject filter in front of the mixer. Currently, this architecture is being adopted mostly for higher-RF and millimeter-wave frequency designs [6], [7], such as point-to-point wireless links. In these applications, the solutions discussed in the following are not practical. Actually, superheterodyne receivers have a number of substantial problems when they are applied to SDR applications. Generally, a number of fabrication technologies are used, making full on-chip integration difficult. Also, they are usually designed to a specific channel (in a particular wireless standard). This prevents the expansion of the receiving band for use with signals having various modulation formats and occupied bandwidths. Therefore, the superheterodyne configuration is not attractive for use in SDR receivers due to its complicated expansion for multiband reception.

Another approach is the zero-IF receiver [8], [9], shown in Figure 2(b), which is a simplified version of the superheterodyne architecture. The whole received RF band is selected by a bandpass filter and amplified by an LNA, as in the previous architecture. It is

then directly down converted to dc by a mixer and converted to the digital domain using an analog-to-digital converter (ADC). Compared to the heterodyne architecture, this has a clear reduction in the number of analog components and also allows the use of a filter having much less stringent specifications than the image-reject filter. As a result, this architecture can make use of a high level of integration, making it a common architecture for multiband receivers such as the one described in [9] and for complete transceiver architectures as in [10] and [11]. However, some of these components can be much more difficult to design due to the required performance of each. Also, the direct translation to dc can generate some issues, such as a dc offset [12]. Other issues are related to second-order intermodulation products that are generated around dc, and, since the mixer output is a baseband signal, it can be easily corrupted by the large flicker noise of the mixer [13]. Its advantages make this the most commonly used configuration in radio receivers currently.

A configuration similar to the zero-IF architecture is the low-IF receiver [14], in which the RF signal is mixed down to a nonzero low or moderate IF instead of going directly to dc. In this case, an RF bandpass filter is applied to the incoming signal, which is then amplified. The signal is converted to the digital domain with an ADC of relatively robust performance, which allows the use of DSP for digital filtering for channel-selection and also mitigate in-phase quadrature (I/Q) imbalances in quadrature demodulators. This architecture still allows a high level of integration and does not suffer from the problems of the zero-IF architecture because the desired

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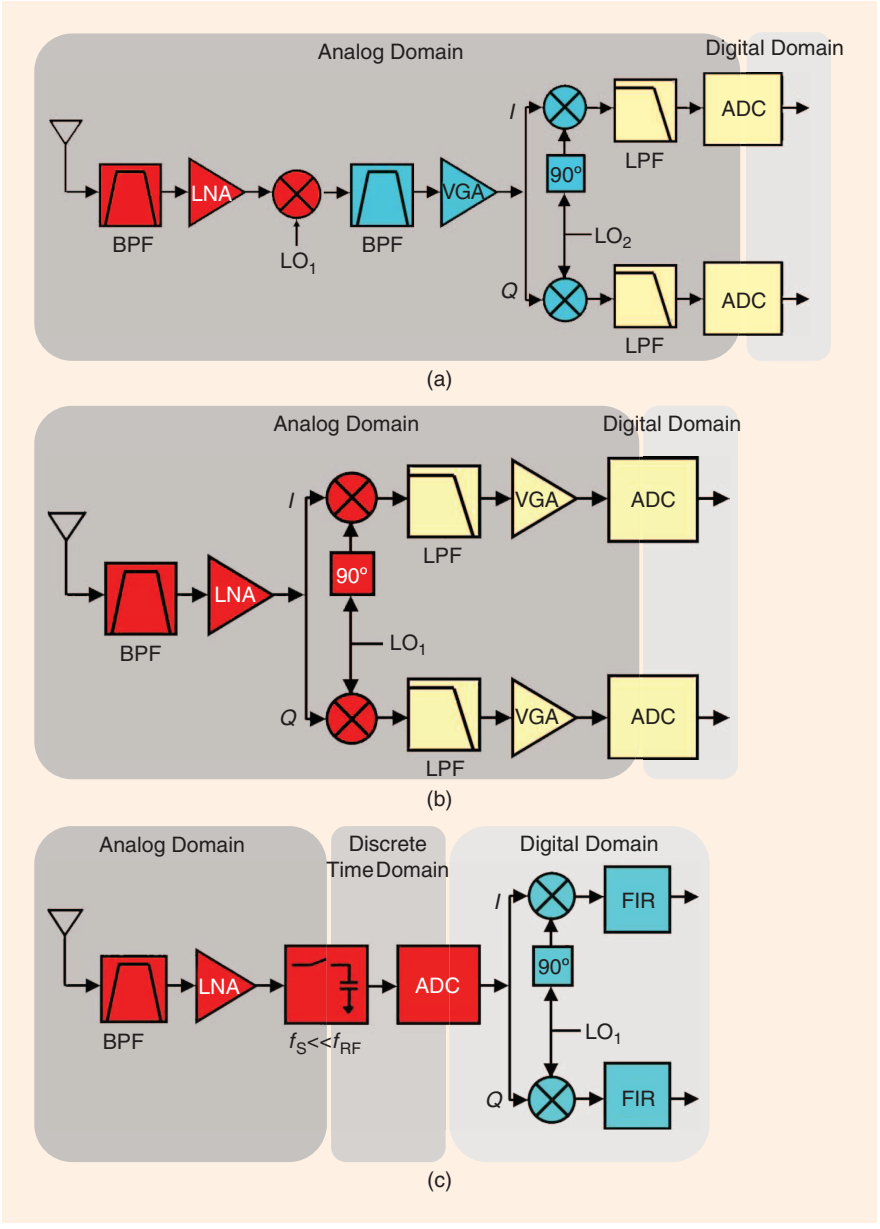

Figure 2. *(a) A superheterodyne receiver architecture where the RF signal is received, filtered, and amplified down-converted to an intermediate frequency where it is again filtered and amplified. Then the signal is converted through a quadrature demodulator to baseband and, in each path (I and Q), filtered, amplified, and converted to the digital domain. (b) A zero-IF architecture in which the RF signal is filtered, amplified, and directly down-converted to baseband by a quadrature demodulator. After that it is filtered, amplified and digitized. (c) A bandpass sampling receiver in which the signal is filtered, amplified, and sampled by a sample-and-hold circuit that is normally a part of the ADC. The signal is mixed-down to the first Nyquist zone, digitized by an ADC, and treated in the digital domain. ADC: analog-to-digital converter, BPF: bandpass filter, FIR: finite impulse response filter, I: in-phase component, LNA: low-noise amplifier, LO: local oscillator, LPF: low-pass filter, Q: quadrature component; VGA: variable gain amplifier.*

signal is not situated around dc. However, in this architecture, the image frequency problem is reintroduced and the ADC power consumption is increased because now a higher conversion rate is required.

Finally, an alternative to the previous solutions is the bandpass sampling receiver [15], [16], Figure 2(c). In this architecture, the received signal is filtered by an RF bandpass filter that can be a tunable filter or a bank of filters. It is amplified using a wideband LNA. The signal is sampled and converted to the digital domain by a high sampling rate ADC and digitally processed. This configuration is based on the fact that all energy from dc to the input analog bandwidth of the sample and hold circuit of the ADC will be folded back to the first Nyquist zone $[0, f_S/2]$ without any mixing down conversion needed. This architecture takes advantage of some properties of sample and hold circuits. As was described in [16], it is possible to pinpoint the resulting intermediate frequency, f_{IF}, based on the relationship

$$\text{if} \quad \text{fix}\left(\frac{f_C}{f_S/2}\right) \quad \text{is} \quad \begin{cases} \text{even}, & f_{IF} = \text{rem}(f_c, f_s) \\ \text{odd}, & f_{IF} = f_s - \text{rem}(f_c, f_s) \end{cases}, \quad (1)$$

where f_C is the carrier frequency, f_S is the sampling frequency, $\text{fix}(a)$is the truncated portion of argument a, and $\text{rem}(a,b)$ is the remainder after division of a by b.

In this case, the RF bandpass signal filtering plays an important role because it must reduce all signal energy (essentially noise) outside the Nyquist zone of the desired frequency band that otherwise would be aliased. If not filtered, the signal energy (noise) outside the desired Nyquist zone is folded back to the first zone together with the desired signal, producing a degradation of the signal-to-noise ratio (SNR). This may be given by

$$SNR = 10*\log_{10}\left(\frac{S}{N_i + (n-1)*N_0}\right), \quad (2)$$

where S represents the desired-signal power, N_i and N_0 are in-band and out-of-band noise, respectively, and n is the number of aliased Nyquist zones.

The advantage of this configuration is that the sampling frequency needed and the subsequent processing rate are proportional to the information bandwidth, rather than to the carrier frequency. This reduces the number of components.

However, some critical requirements exist. For example, the analog input bandwidth of the sample and hold circuit (normally inside the ADC) must include the RF carrier, which is a serious problem, considering the sampling rate of modern ADCs. Clock jitter can also be a problem. Also, RF bandpass filtering is required to avoid overlap of signals.

Other architectures being proposed for use in SDR receivers involve use of direct RF sampling techniques based on discrete-time analog signal processing to receive the signal, such as the ones developed in [17] and [18]. These methods are still in a very immature stage but should be further studied due to their potential efficiency in implementing reconfigurable receivers.

Architectures for Software-Defined Radio Transmitters

The Front End

In this section, we discuss several transmitter architectures that have potential application to SDR systems. As we know, a transmitter is not only the PA but a variety of other circuit components collectively known as the front end. The design of the PA is one of the most challenging aspects of transmitter design, having a high impact on the coverage, the product cost and the power consumption of a wireless system. Here we begin with a consideration of the complete transmitter architecture and, in a following section, discuss the PA as it relates to SDR. This review is mainly based on [19].

The first architecture [Figure 3(a)] is the common superheterodyne transmitter, which is the dual of the superheterodyne receiver presented in Figure 2(a). The signal is created in the digital domain and then converted to the analog domain using simple digital-to-analog converters (DACs). The signal is modulated at an intermediate frequency, where it is amplified and filtered to eliminate harmonics that were generated during modulation. Finally, the signal is up-converted to RF using a local oscillator (LO_2), filtered to remove unwanted image sidebands, amplified by an RF PA and applied to the transmit antenna. The I/Q modulator works at IF, which means hardware components are easier to design than they would be for an RF-based modulator. Finally, the overall gain can be controlled at IF where it is easier to build high-quality variable gain amplifiers. However, such an architecture has a significant number of problems, as in the receiver's case. Therefore, this architecture is mostly adopted for microwave point-to-point wireless links as, for example, in backhaul communications [6], [7] and of course in the above-mentioned field of radio transmitters. The amount of circuitry and low integration level, as well as the required linearity of the PA and the difficulty to implement multimode operation generally prevent the use of superheterodyne transmitters in SDR applications.

Figure 3(b) shows a block diagram of a direct-conversion transmitter [20], [21] that is a simplified

version of the superheterodyne front end. As in the last case, two DACs are used to convert the baseband digital I and Q signals to the analog domain. The low-pass filters that follow eliminate Nyquist images and improve the noise floor. These signals are directly modulated at RF by the use of a high-performance I/Q modulator. After that, the signal is filtered by a bandpass filter centered at the desired output frequency and is amplified by a PA.

In a frequency-agile system, the signal chain must be designed so that carrier frequencies can be synthesized over a defined range that will require a broadband post-modulator or a tunable post-modulator filtering to attenuate out-of-band noise. Thus, due to a phenomenon known as *injection pulling* [22], the strong signal at the output of the PA may couple to the LO_2. As a result, the frequency of the LO_2 can be pulled away from the desired value.

Even though this architecture reduces the amount of circuitry required and easily allows high-level integration, it carries some disadvantages such as possible carrier leakage and phase gain mismatch. Gain control may need to be carried out at RF and this architecture also requires a PA with good linearity. With careful design, these transmitters can be employed in SDR applications, and, with the development of integrated technologies, we have witnessed a fast migration from the superheterodyne architecture to direct-conversion transmitters.

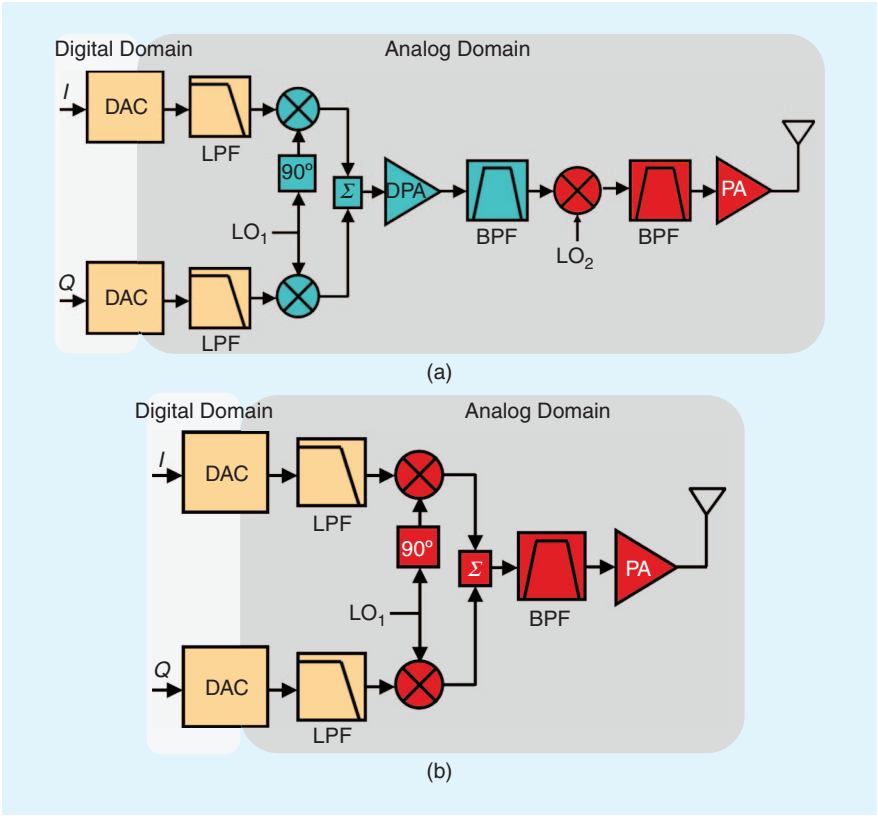

Figure 3. *(a) A superheterodyne transmitter in which the I/Q digital signal is converted to the analog domain, low-pass filtered, and modulated at an intermediate frequency. Then the signal is amplified, filtered, and up-converted to RF where it is filtered again and amplified before being transmitted. (b) A direct conversion architecture where the I/Q digital signal is passed to the analog domain by a DAC, filtered, and then directly modulated at the desired RF frequency. After this, the RF signal is filtered and amplified by a power amplifier. BPF: bandpass filter, DAC: digital-to-analog converter, DPA: driver power amplifier, I: in-phase component, LO: local oscillator, LPF:low-pass filter, PA: power amplifier, Q: quadrature component.*

The Power Amplifier Section

In the previous architectures, the RF PAs (PA block) used are class A, AB, or B, which demonstrate the highest efficiency when operated in the compression region, or are class D, E, and F operated in switching mode [23]. The latter, highly efficient PAs operate in a strongly nonlinear mode. As a result, they can only amplify constant-envelope modulated signals such as those used in the global system for mobile communications (GSM) access format. Modulation types such as quadrature amplitude modulation (QAM) that are used in new access formats such as wideband code division multiple access (W-CDMA) and orthogonal frequency-division multiplexing (OFDM), have high peak-to-average power ratios (PAPRs). The standard way to avoid compression of PAs is to operate them in "back-off" mode, that is, to reduce the input power until the PA is not driven into compression. Unfortunately, this lowers efficiency significantly, especially for high PAPR signals. Several linearization techniques, for example, feedback, feed-forward, or digital predistortion, [23], [24], have been proposed and evaluated, but these are not yet widely used in fully integrated PAs.

The problem of transmitting a high PAPR signal efficiently has been thoroughly investigated over the years. To increase efficiency, a technique proposed some years ago, the Kahn technique [25], is now being studied for use in new transmitter architectures.

Envelope elimination and restoration (EER), proposed by Kahn, is one method to linearize highly nonlinear, highly efficient transmitters. In these systems, the supply voltage of the output RF PA is dynamically

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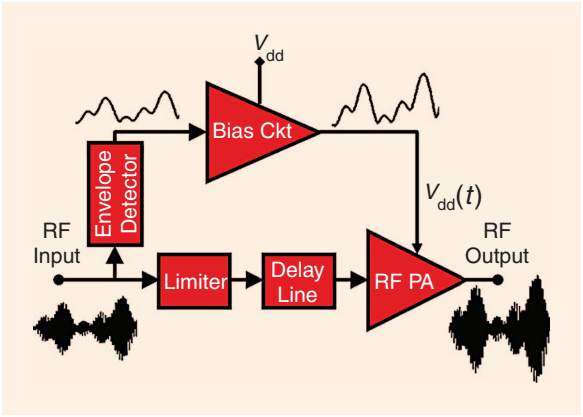

Figure 4. *Block diagram of a Kahn amplifier section in which the RF input signal is split into two branches. One branch is a delayed and constant-envelope RF carrier with phase information (implemented by a limiter and a delay line). The other branch carries the amplitude of the signal envelope to be amplified (Bias Ckt) and then applied to the drain voltage of the RF power amplifier.*

adjusted to restore the amplitude onto a phase-modulated representation of the signal. Figure 4 shows the traditional EER architecture. Although it is a very appealing concept, the actual implementation is very challenging. The challenge arises mainly from the design of a perfect delay line, an accurate limiting stage, an improved bias circuitry that could allow high PAPR and high bandwidths, and the bandwidth that the switched/saturated RF PA should cover to amplify the phase-modulated signal [30].

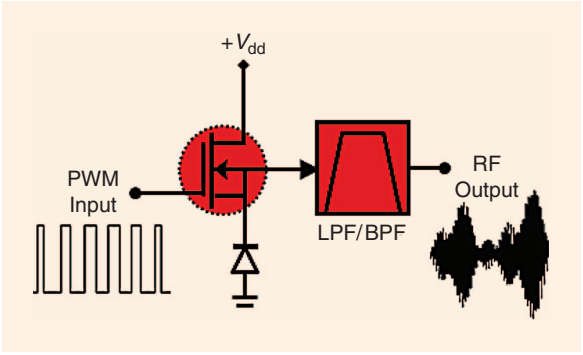

Figure 5. *Simplified circuit of a class-S power amplifier with a digitally generated pulse-width-modulated signal applied at its input. This circuit will generate a baseband signal or an RF signal at the output after the low- or bandpass filtering.*

For these reasons, in modern realizations, with the enormous improvements in DSP capabilities, it has been advantageous to implement the envelope detector, the limiter, and the delay line (time delay) digitally. Such a digital version of an EER transmitter is used in the polar transmitter, which will be explained later.

A visionary solution uses pulse-width modulation to create the so-called all-digital transmitter that will be described next. This all-digital approach is important because of the implementation of novel SDR configurations that will enable cognitive approaches. This approach also enables a low dc power consumption because it allows the use of very-high-efficiency transmitters, such as the class-S PA shown in Figure 5.

Furthermore, as the speed of digital signal processors advances, algorithms in which the DSP provides signals at RF can be envisioned (particularly for switching amplifiers in which the inputs are digital pulse-width modulated signals and the outputs are RF modulated signals) in order to develop the all-digital transmitter.

As shown in Figure 5, the class-S amplifier [26] can be a pure switching amplifier followed by a low-pass filter (to create an envelope signal) or a bandpass filter (to create an RF signal). This amplifier ideally will consume no dc power because the output voltage and the current are equal to zero alternately and, as a result, the efficiency achieved will be 100% in the ideal case. In reality, the class-S amplifier will consume some power in the signal transitions. This is because in real devices, interconnecting components and parasitic capacitance will produce some losses, and finite switching times will occur. The input pulse-width-modulated signal can be generated by a digital signal processor, eliminating the need for a wideband DAC and potentially saving cost.

Unfortunately, if one looks at real-world configurations, it is not possible, yet, to design a high-efficiency class-S amplifier to operate at very high frequencies. Nevertheless, some contributions are appearing in the field [27]. Similar approaches are being tried with sigma-delta modulators [28], [29].

Because of this, switching amplifiers that are being widely used in new configurations are based on envelope elimination and recovery in a polar transmitter configuration [30], [31] in which the envelope information is modulated. As a result, the required bandwidth is much smaller since it is a baseband signal that is being amplified. This allows the use of high-efficiency class-S amplifiers, Figure 6.

If we look at the circuit of Figure 6, the class-S amplifier only amplifies the envelope of the input signal (detected in the digital domain by the digital signal processor, DSP). In this case, the class-S amplifier is only used to vary the bias voltage, $V_{DD}(t)$, of the RF high-power amplifier. In the phase path, a constant-envelope

phase-modulated signal is generated in the DSP and then up-converted to RF and applied to the RF PA. This RF PA is always saturated, providing high efficiency. Nonetheless, the major concern of such schemes is the time alignment between the baseband envelope path and the RF path. This can be compensated in the digital domain by use of DSP.

Other architectures being proposed include amplifier sections based on the Doherty [32], [33] and outphasing [34] techniques. The Doherty scheme combines two PAs (a carrier PA biased in class-B and a peak PA biased in class-C) of equal capacity through quarter-wave-length lines or networks. In modern implementations, DSP can be used to improve the performance of the Doherty amplifier by controlling the drive and bias to the two PAs. For ideal class-B amplifiers the average efficiency can be as high as 70% for high PAPR signals.

The outphasing design, also known as linear amplification using nonlinear components (LINC), produces an amplitude-modulated signal by combining the outputs of two PAs driven with signals of different time-varying phases. Using ideal class-B amplifiers, the average efficiency now can be around 50% for the same large PAPR signals as in the previous case. More details about these designs can be found in [19].

With regard to SDRs, both the Doherty and outphasing techniques can be of high interest for future exploration. This is due to the fact that the improvements in the particular PA section efficiency will lead to higher efficiencies in the entire transmitter. Also, this transmitter architecture holds the promise of operating correctly for several multistandard and multiband signals.

Test of Software-Defined Radio Solutions

After introducing candidate architectures for both receivers and transmitters used in SDR front ends, we next address another important theme: the test and measurement of SDR systems. Key to this discussion is the concept of a mixed-domain measurement technique, because the SDR system always has one input in the analog domain and the other in the digital logic domain. In the SDR concept, the main idea is to push the ADC/DAC as close as possible to the antenna, as shown in Figure 1. As a result, fewer signals will exist in the analog domain, and the measurement of digital signals takes on a level of importance not found in traditional analog-RF system characterization.

For ideal class-B amplifiers the average efficiency can be as high as 70% for high PAPR signals.

Hardware

The instrumentation industry [35]–[37] has developed various instruments suitable for SDR characterization, such as mixed-signal oscilloscopes that are capable of operating in the analog and digital domains at same time. This allows time synchronization of both analog and digital signals in a single instrument. However, mixed-signal oscilloscopes only provide asynchronous sampling. This means that, like a traditional sampling oscilloscope, the mixed-signal oscilloscope uses its internal clock to sample data. As discussed in [38] and [39], when testing SDR devices (including ADCs), the correct evaluation of phase and amplitude transfer functions requires coherent sampling between the input, output, and clock signals. If these signals are asynchronously sampled, then spectral leakage may occur that can completely degrade any amplitude and phase information from the SDR. The spectral leakage arises due to the fact that when performing the necessary Fourier transform (DFT or FFT), the two signals do not share a common time domain grid, and thus they become uncorrelated to each other.

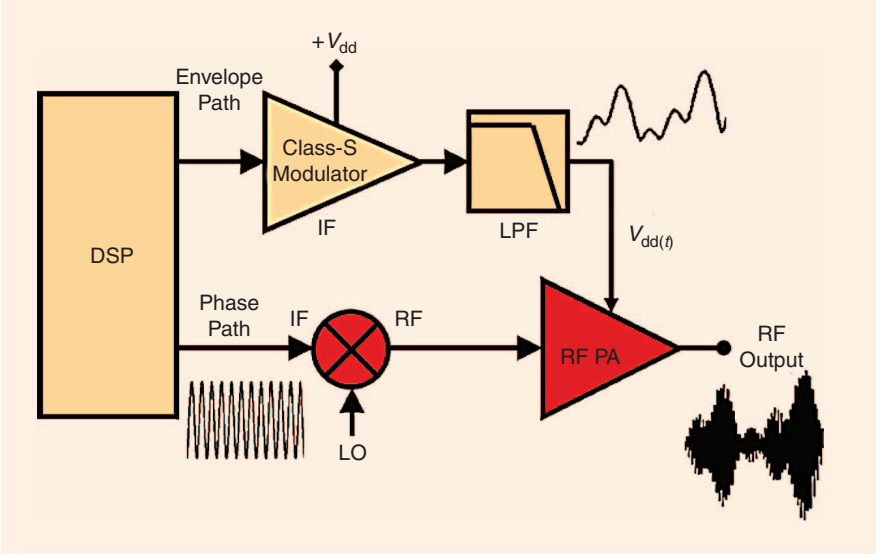

Figure 6. *Block diagram of a polar transmitter. The signal is generated by a DSP and divided into envelope amplitude and constant-envelope phase-modulated components. The pulse-width-modulated envelope signal is amplified by a class-S modulator, then low-pass filtered to produce the analog signal envelope and supplied to the bias of the RF power amplifier. The constant-envelope phase-modulated component is up-converted to RF with a mixer and amplified by the RF power amplifier.*

In a frequency-agile system, the signal chain must be designed so that carrier frequencies can be synthesized over a defined range.

Other potential problems with the mixed-signal oscilloscope include, for instance, the memory size necessary to obtain a behavioral model. Because these instruments normally use very high sampling rates, a huge number of points is required to be able to capture the slow/medium symbol rates of commonly used modulated signals. Thus, these types of instruments are not able to characterize a complete SDR front end in its entirety.

Other approaches also proposed by the instrumentation industry combine several instruments, including logic analyzers, oscilloscopes, vector signal analyzers, or real-time signal analyzers [40]–[42]. For testing an SDR transmitter configuration, these instruments can be used in an arrangement similar to the one shown in Figure 7. With the use of reference signals, trigger signals, and markers, one can acquire synchronized measurements between digital and analog domains and between time and frequency domains. Typical measurements that may be used to evaluate the transmission or reception chains in SDRs with these systems are the progression of error vector magnitude (EVM) and adjacent-channel power ratio (ACPR) throughout the signal chain.

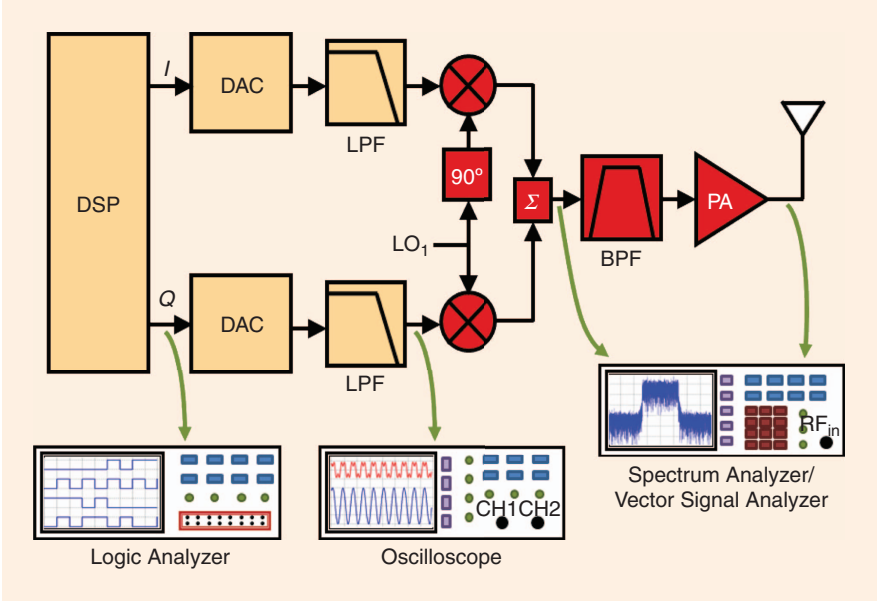

Figure 7. *Instrumentation employed in testing a software defined radio transmitter where several instruments are combined. A logic analyzer acquires the digital logic bits at the output of the digital signal processing (DSP) section, an oscilloscope analyzes the analog signal after the digital-to-analog conversion (DAC) and low-pass filter (LPF) reconstruction, and a spectrum analyzer or a vector signal analyzer obtains the analog RF signal right after the quadrature modulator or also after amplification.*

In [39], the authors discussed the issues of signal timing and synchronization requirements and proposed some solutions, for example, embedding a trigger signal in the test excitation. Some important problems still have to be addressed, such as a calibration procedure for mixed-signal instrumentation. The analog channel in a mixed-signal instrument should ideally measure the reflection coefficient at the input port. Directional couplers should be used to provide a wave-based, impedance-mismatch-corrected characterization of the RF signals incident on the device under test (DUT). With this information, it would be possible to relate the analog input with the digital output in order to find a transfer function or even the complete behavioral model for the SDR system. It is possible to construct such instrumentation using off-the-shelf components and algorithms, for example, the mismatch-correction algorithms discussed in [43]. However, a complete measurement set-up is not currently available commercially.

With this mixed-signal instrumentation, it will be possible to measure figures of merit that are native to analog front ends but also figures of merit that are native to digital communication signals.

Figures of Merit

One common technique to assess the overall performance of a digitally based radio is the bit error rate (BER) test. This test measures the quality of the signal transmission and reception in terms of erroneous data bits over the total bits sent. However, it is a rather limited test because it does not provide much information on the sources of bit errors.

However, if an arrangement similar to the one shown in Figure 7 is used for testing an SDR system, signals in the different domains are acquired simultaneously by the different instruments. This enables the test engineer to pinpoint the possible sources of imperfections throughout the entire signal chain.

In this regard, a second commonly used figure of merit is EVM, which provides insight into potential transmitter and receiver problems [40], [42] because the effects of both magnitude and phase errors on each of the digitally transmitted symbols are measured. EVM essentially measures the overall signal-to-noise-and-distortion ratio, quantifying

signal impairments due to nonlinear distortion, as well as system noise. Contrary to other figures of merit, EVM evaluates the impact on the signal quality in terms of the real transmitted symbols.

A metric that is typically used in transmitter testing quantifies the amount of spectral regrowth in the adjacent channels. Adjacent channel power ratio [ACPR, sometimes called adjacent channel level ratio (ACLR)], is often specified using out-of-band masks that define the maximum allowable transmitted power in an adjacent channel. ACPR usually arises from spectral regrowth due to nonlinear distortion.

ACPR can also be applied to the alternate channels (the channels adjacent to those adjacent to the bandpass signal). ACPR provides a functional test to assess the performance of the entire radio network, because it allows an engineer to evaluate the interference that the nonlinearities in the radio system will impose on other close-by channels.

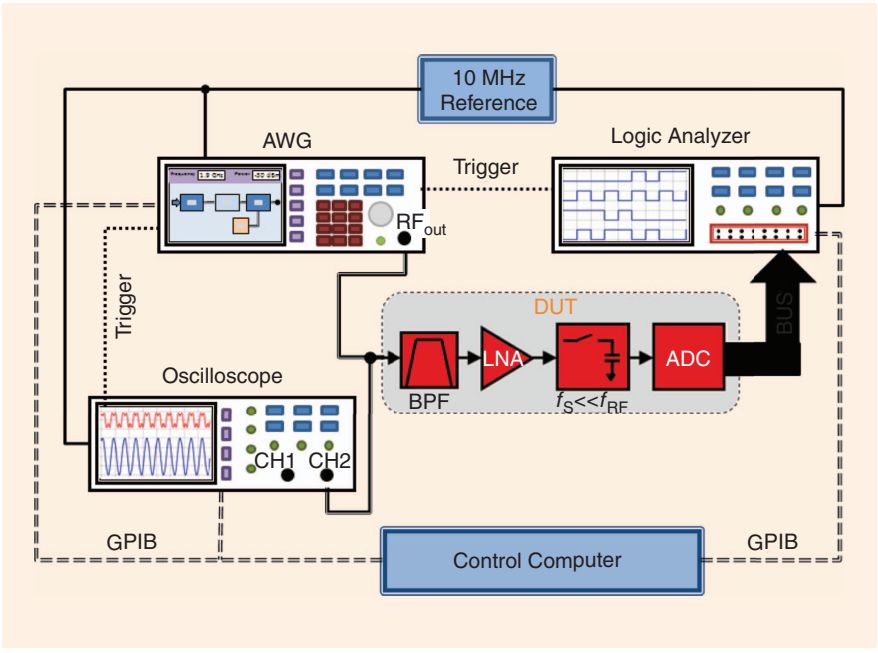

Figure 8. *Laboratory implementation of the instrumentation proposed in [39] for testing SDR front ends. The device under test (DUT) is excited by an arbitrary waveform generator, and an oscilloscope is used to sample the analog signal input to the DUT. A logic analyzer is used to sample the DUT's digital output signal. Reference and trigger signals synchronize the input and output measurements. The instrumentation is controlled by a computer using general purpose interface bus (GPIB) connections.*

For SDR test, as with many radio architectures, the excitation signal to be used during test will affect measured performance of the radio system. The effect of the test signal on radio performance is normally examined through the inherent statistics of the excitation, either using the probability density function (PDF) or the complementary cumulative distribution function (CCDF). The signal's PAPR value is also often used as a figure of merit [44]–[48].

These figures of merit, common to both traditional radio systems and SDRs, are discussed and explained in more detail in "Metrics for Wireless System Test." In the following example, we illustrate the mixed-domain methods that must be used to measure these figures of merit in SDR systems.

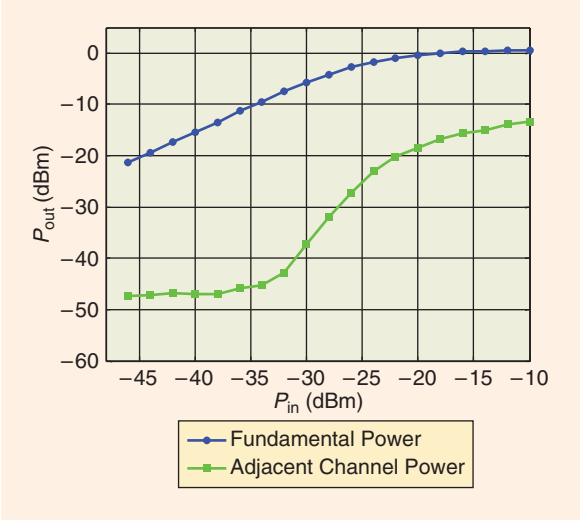

Figure 9. *Measured results at the output of the SDR front end with WiMAX excitation.*

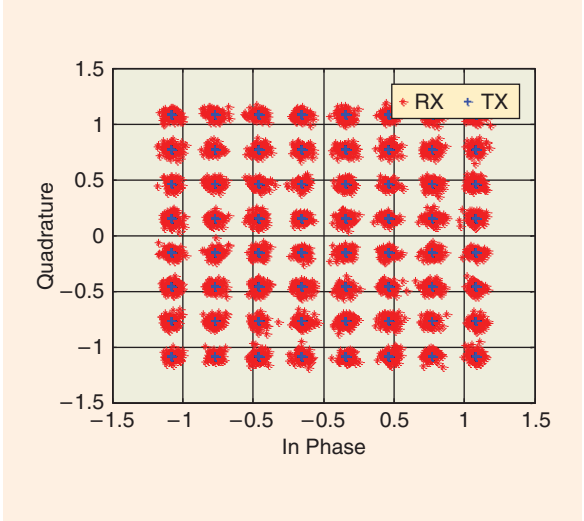

Figure 10. *Constellation diagram comparing the input and output WiMAX signals using 64-QAM modulation.*

Metrics for Wireless System Test

Here we will give a brief description of several figures of merit that were identified throughout the article.

Probability Density Function

In probability theory, a probability density function (PDF) is a function that represents the probability that a random variable X will take on a value less than the number x. Normally, the PDF is determined after a large number of measurements have been performed, which determine the likelihood of all possible values of x. It is a nonnegative function with unit area

$$\text{pdf}(x) = P[a < X \leq b] = \int_a^b f(x)dx, \tag{S1}$$

where a and b represent the limits wherein the probability of X will be assessed.

Complementary Cumulative Distribution Function

The complementary cumulative distribution function (CCDF) curve is closely related to the PDF because it is obtained by means of CCDF = 1 − CDF. The CDF is the cumulative distribution function that is obtained directly from the PDF's statistics as

$$\text{cdf}(x) = \int_{-\infty}^{a} \text{pdf}(x)dx. \tag{S2}$$

A CCDF curve shows how much time a signal spends at or above a certain power level. It is normally expressed in decibels above the average power.

Peak-to-Average Power Ratio

Peak-to-average power ratio (PAPR) is a relationship between the maximum value of the peak power and the average power of a given signal and is a measure of great interest in wireless communications. The evaluation of the impact of PAPR on communications systems is mainly made through the analysis of CCDF curves, where we define a certain percentage in the CCDF curve to pinpoint the PAPR value

$$\text{PAPR} = \frac{\max\limits_{0 \leq n \leq \text{NT}} |x(t)|^2}{\frac{1}{\text{NT}}\int_0^{\text{NT}} |x(t)|^2 dt}, \tag{S3}$$

where NT represents the total number of samples (time interval) that will be considered to determine the PAPR value.

Adjacent Channel Power Ratio

Adjacent channel power ratio (ACPR) is a measure of the amount of distortion that a wireless system generates in the adjacent-frequency channel relative to the power in the main channel. It is usually defined as the ratio of the average power in the adjacent-frequency channel (or offset channel) to the average power in the transmitted-frequency channel as

$$\text{ACPR}_{up} = \frac{\int_{F_1}^{F_2} S(w)\,dw}{\int_{U_1}^{U_2} S(w)\,dw}, \tag{S4}$$

where F_1 and F_2 represent the boundaries of the frequency spectrum, $S(w)$, of the fundamental signal, and U_1 and U_2 are the boundaries of the frequency spectrum of the upper-adjacent channel.

There are two ways of measuring ACPR, as defined in wireless standards, one that considers the ratio between the entire fundamental channel over the entire adjacent channel. The second approach (more popular because it is easier to measure) is to find the ratio of the output power either across the entire main band or in a smaller bandwidth around the center of carrier to the power in the adjacent channel with the same smaller bandwidth.

Bit Error Rate

Bit error rate (BER) represents the ratio of the number of erroneous data bits received to the total number of data bits transmitted. BER is normally given as a percentage, where 0% represents the case where no erroneous bits were detected at the receiver

$$\text{BER} = \frac{N^{\text{o}}\,\text{Erroneous Bits}}{\text{Total Bits Sent}}. \tag{S5}$$

This measurement can be performed in the digital domain by a software function implemented by the test engineer, but also using well-known BER testers that input a known data stream into the transmitter input and compare it with the data bits coming from the receiver's output.

Error Vector Magnitude

Error vector magnitude (EVM) is a measure of modulation and demodulation accuracy, as well as channel impairments. It may be used to quantify the performance of a digital radio transmitter or receiver. A signal sent by a transmitter or received by a receiver will suffer from various imperfections in both the hardware and software implementations that will cause the k modulated-signal constellation points, $Z_c(k)$, to deviate from their ideal locations, $S(k)$. Informally, EVM is a measure of how far the points are from the ideal locations, where, for N transmitted symbols, we have

$$\text{EVM} = \sqrt{\frac{1}{N}\sum_{k=1}^{N} |Z_c(k) - S(k)|^2}. \tag{S6}$$

Measurement Example

To illustrate the measurement of an SDR receiver, we used a mixed-domain measurement set-up such as the one presented in [39] (similar to that presented in Figure 7), as shown in Figure 8. The arbitrary waveform generator simulated the transmitted digitally modulated RF signal, and the receiver was simulated using the components shown in the block diagram. This DUT was excited with a single-user WiMAX signal in frequency-division-duplex mode with a bandwidth of 3 MHz and a modulation type of 64 QAM (3/4) [49].

Figure 9 presents the measured results at the output of the SDR receiver using the logic analyzer. This figure shows the total power averaged over the excitation band of frequencies and the total power in the upper adjacent channel arising from nonlinear distortion. This figure illustrates the mixed-mode nature of SDR testing: The analog output figure of merit ACPR has been reconstructed from the digital output and analog input signals.

We have also evaluated the performance of the DUT at a given input power in terms of EVM. The received digital WiMAX signal was demodulated and corrected in terms of gain and phase delay, and the constellation diagram shown in Figure 10 was obtained. An EVM value of approximately 5.05% was obtained in this particular measurement.

The characterization of the SDR components was only possible due to the fact that we have used a mixed-mode instrument, which allows the simultaneous characterization of the analog and digital waveforms.

Summary and Conclusions

In this article, we have presented a review of both receivers and transmitters that may be used in SDR front ends. We discussed advantages and disadvantages of each. As we saw, a well-designed architecture for a multiband multimode receiver should optimally share available hardware resources and make use of tunable and software-programmable devices. Not every receiver architecture has this feature. In that sense, in our opinion, the SDR receiver front-end will be based either on the zero/low-IF architecture or on the bandpass sampling design when it is more mature.

For the transmitter, the EER technique and its adaptations are promising choices for use in SDR applications because their efficiency is largely independent of PAPR. Thus, they may be readily applied to multistandard and multiband operation [50]. Such SDR and CR transmitter architectures will require not only highly efficient PAs but also wideband PAs [51]. The SDR community is moving from analog to digital approaches for signal transmission, and, thus, the demand for increased switching speed in RF PAs is becoming more evident and more stringent, leading in the future to class-S-based transmitters.

A well-designed architecture for a multiband multimode receiver should optimally share available hardware resources and make use of tunable and software-programmable devices.

Concerning the measurement instrumentation used to characterize SDR systems, we illustrated why mixed-domain instrumentation is essential for characterization of SDRs. We described why some improvements will have to be made in order to develop a synchronous instrument that will characterize SDR front ends rapidly, automatically, and with impedance-mismatch correction. Such an instrument would ideally provide information such as EVM for different types of modulation and adjacent channel power ratio for different technologies and would be able to test multistandard multiband radio configurations. We anticipate seeing these types of instruments on the market as SDR technology becomes more mature.

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[J2] – Wideband Behavioral Model for Nonlinear Operation of Bandpass Sampling Receivers

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Wideband Behavioral Model for Nonlinear Operation of Bandpass Sampling Receivers

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***Abstract*—In this paper, a new behavioral model for bandpass sampling receivers (BPSRs) is presented. The new model describes the wideband behavior of the BPSR and addresses specifically its nonlinear behavior, either in-band distortion, but also intermodulation and harmonic generation.**

The proposed model allows the selection of different memory taps for each nonlinear mixing cluster. This model capability simplifies the mathematical description of each cluster, being possible to describe the nonlinear behavior of the BPSR using low-complexity operators. An original model parameter-extraction procedure that works in parallel for each cluster of nonlinearities will also be presented.

Moreover, the presented behavioral model and respective parameter-extraction performances will be assessed by using several different excitations when applied in different Nyquist zones of the used BPSR.

***Index Terms*—Bandpass sampling receivers (BPSRs), behavioral modeling, parameter extraction, software-defined radio (SDR).**

I. Introduction

BANDPASS sampling receivers (BPSRs) are one of the proposed architectures for future cognitive radio (CR) approaches.

In this paper, a very wideband behavioral model strategy for this type of architecture will be presented based upon the Volterra-series description. The proposed model allows the identification of different memory taps, depending on the type of nonlinear mechanism that arises from the receiver, which is a step forward in the correct understanding of this type of wireless system. With these models, RF engineers would be more supported in their designs and give rise to better radio solutions [1]. Actually, the future concepts of CR, proposed by Mitola and Maguire [2], will demand a huge receiving spectral bandwidth combined with very different power levels, i.e., high dynamic ranges.

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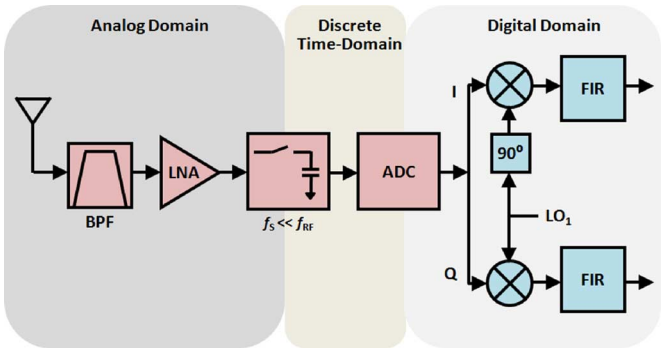


Fig. 1. Bandpass sampling receiver architecture. From [16].

By its very definition, a CR is a radio that is able to automatically adapt itself to the air interface by optimizing the carrier frequency, modulation, and choice of radio standard to minimize interference and maintain communication in a given scenario.

In that way, these CR approaches will be definitely based in the software-defined radio (SDR) architectures that are being evaluated at this moment by the scientific community. As was summarized in [3], there are a reduced number of solutions to construct the referred spectrum sensing capable CR radio. One of those is the BPSR [4], [5], which, due to the constant advancements achieved in analog-to-digital converter (ADC) technology, is becoming a much more feasible and practical solution (Fig. 1).

The key component of this architecture is the ADC (pipeline design) that normally contains a sample-and-hold circuit, which, in theory, will down convert the incoming signal as a mixer module, followed by the quantizing scheme based on a pipeline approach [6]. A brief analysis of the scientific community works shows that several models to represent the nonlinear behavior of pipelined ADCs already exists, mainly based on Volterra series approaches [7], [8].

The work presented in [7] uses Volterra operators to describe the nonlinear behavior of ADCs, and it is supported in a time-domain extraction scheme that allows the characterization of all dynamic effects, but it lacks the operation of the device over its different Nyquist zones (NZs). On the other hand, the model of [8] being based on a frequency-domain extraction approach, easily conducts to a complexity ill conditioned or even an unworkable problem due to the exponential increase in the number of Volterra kernels that need to be determined. Other pipeline ADC models are available, but do not address ADC behavioral information, and are mainly based on time-domain simulations [9]. Moreover, the simulation of such a huge and complex architecture (entire BPSR) is quite computer intensive, mainly

when the objective is to simulate RF signals modulated with high bandwidth excitations.

Thus, the main motivation of this paper is to propose a new wideband behavioral model for a BPSR covering the RF/IF and the baseband frequency responses in the first and over several different NZs. This work was begun in [10] where an initial approach to this problem was followed.

In order to achieve this goal, this paper is organized in the following way; firstly, some introductory concepts about the BPSR architecture are given. In Section III, a new behavioral model scheme will then be proposed, which can be used in other applications due to its flexibility. In Section IV, we will explain the necessary parameter-extraction procedure, including the experimental setup used and a triggering format to synchronize all the measured signals. Section V illustrates the application of the proposed behavioral model and the respective parameter extraction for a multisine excitation signal. Afterwards, in Section VI, the addressed behavioral model is further validated in different NZs using a common wireless signal as excitation. Finally, some conclusions will be drawn summarizing the obtained results.

II. Receiver Operation in Different NZs

The first step in order to model this new receiver scheme will be to study and understand the theory and proposed approaches behind the BPSR.

In the BPSR [4], [5] (Fig. 1), the incoming signal is initially filtered by an RF bandpass filter (BPF) that can be a tunable filter or a bank of filters, and then it is amplified using a wideband low-noise amplifier (LNA). The signal is then converted to the digital domain by a high sampling rate ADC and digitally processed. Digital signal-processing techniques can be used in order to alleviate some mismatches of the analog front-end.

Moreover, this architecture is a close approximation to the initial idea of Mitola [1] for an ideal SDR radio because it pushes the ADC closer to the antenna and in that sense provides an increased flexibility.

Nevertheless, the ADC typically presents sampling rates lower than the RF signal carrier frequency. BPSR allows the implementation of an approach that allows all of the energy from dc to the input analog bandwidth of the ADC to be folded back to the first NZ $[0, f_S/2]$. This process occurs without any mixing down-conversion because a sampling circuit is somehow replacing the mixer module. Actually this is one of the most interesting components of this architecture because it allows an RF signal of a higher frequency to be sampled by a much lower clock frequency.

This process can be observed in Fig. 2(a) and (b), in which we can see that all the input signals present in the allowable bandwidth of the sampling circuit are folded back to the first NZ [see Fig. 2(b)]. As can be seen, the signals are down-converted and fall over each other if no filtering is used previously. This folding process occurs for all the available signals at the input of the circuit but also for any nonlinearity that may be generated previously (e.g., in the LNA) or even in the particular sampling circuit.

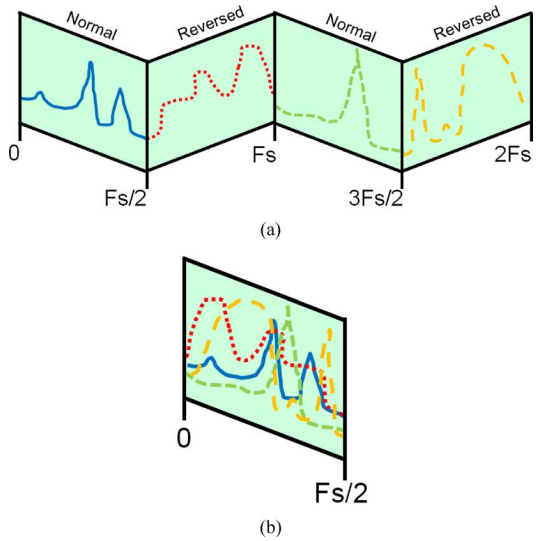


Fig. 2. Process of folding that occurs in the sample-and-hold circuit. (a) Entire input spectrum bandwidth. (b) Output from the circuit in which all the signals are folded back to the first NZ.

Regarding the resultant folded frequencies, f_{fold}, it is possible to pinpoint them based on the following relationship [11]:

$$\text{if} \quad \text{fix}\left(\frac{f_C}{f_S/2}\right) \text{ is } \begin{cases} \text{even}, & f_{\text{fold}} = \text{rem}(f_C, f_S) \\ \text{odd}, & f_{\text{fold}} = f_S - \text{rem}(f_C, f_S) \end{cases} \tag{1}$$

where f_C is the carrier frequency, f_S is the sampling frequency, $\text{fix}(a)$ is the truncated portion of argument a, and $\text{rem}(a, b)$ is the remainder after division of a by b.

Thus, in order to better understand the operation of the explained BPSR in different NZs, let us assume that the BPSR, as shown in Fig. 1, is sampled by a clock of 90 MHz and excited first by a signal excitation present in the first NZ (e.g., 11.5 MHz) and then excited by a signal excitation situated in the second NZ (e.g., 69 MHz). For instance, if we consider a model truncated at the third-order nonlinearity, for the first excitation frequency and taking into account the frequency folding phenomena, the fundamental and respective harmonics will fall in the first NZ. However, the same will not happen for the second excitation frequency, where the baseband will fall on the first NZ, the fundamental and second harmonic will fall in the second and fourth NZs, respectively, and are folded back in the reversed way, obtained with (1). Regarding the third harmonic it will fall in the fifth NZ and is folded back in the normal mode.

In that sense, any model that may be used to describe the behavior of such an architecture should have in mind that the operation over a huge bandwidth has to be covered and accompanied by different dynamic effects, which can be represented by different memory taps in the nonlinear model.

III. Proposed Wideband Behavioral Model

As was seen in Section II, the correct description of the BPSR nonlinear behavior requires that it must be wideband and it must depend on the NZ where the signal is being sampled.

Moreover, the nonlinear signal generation can impose spectral components appearing at the first NZ case of the low-frequency baseband generation, (typically an even-order nonlinear product) or very high-frequency components appearing at higher NZs that are further folded back to the main ADC bandwidth.

This will impose that the dynamic response of the BPSR will have delays of highly different orders, some at the RF time frame, and others at the baseband time frame.

The selected behavioral model mathematical description that was chosen for describing the nonlinear behavior of the BPSR was based on a Volterra-series approach [12] due to its good performance in this type of nonlinear scenarios.

A Volterra series is a combination of linear convolution and a nonlinear power series that provides a general way to model a nonlinear system with memory. In that sense, it can be employed to describe the relationship between the input and output of the entire BPSR presenting nonlinearities and memory effects. This relationship can be written as

$$y(t) = \sum_{n=0}^{\infty} \int_{-\infty}^{\infty} \cdots \int_{-\infty}^{\infty} h_n(\tau_1, \ldots, \tau_n)\, x_{\text{in}}(t-\tau_1) \cdots x_{\text{in}}(t-\tau_n)\, d\tau_1 \cdots d\tau_n \quad (2)$$

where $x_{\text{in}}(t)$ and $y(t)$ are the input and output signal waveforms, respectively, and $h_n(\tau_1, \ldots, \tau_n)$ is the nth-order Volterra kernel.

Despite the applicability of such an RF time-domain Volterra series model, one very important drawback is the complicated model structure, which leads to an exponential increase in the number of coefficients with the degree of nonlinearities and memory length considered.

It can be seen that sometimes the overall system description can behave very differently since, for instance, the even-order coefficients can generate signals at very high frequencies (e.g., the second harmonic) and at the baseband frequency near dc, this will impose that the Volterra approach as presented in (2) cannot be used[1] since it uses the same descriptor for the second harmonic as for the baseband responses. This was actually the main problem observed in the work presented in [10] since when a good approximation was achieved at higher frequencies, it had some problems in the lower frequencies and vice versa. That was really due to the fact that a similar amount of memory taps were used for all the nonlinear descriptors (kernels) because of the applied extraction procedure.

Thus, in order to minimize this problem, we propose to apply this Volterra-series model with a low-pass equivalent format [13], where each nonlinear mixing cluster is first selected and converted individually to its complex envelope; thus, the Volterra low-pass equivalent behavioral model will then be applied individually to each low-pass cluster, considering obviously the nonlinearity that has generated it. This procedure can actually be seen as a model extraction based on the envelope harmonic-balance procedure, where each cluster is actually addressed individually [14]. In Fig. 3, we exemplify this low-pass equivalent conversion for a third-order degree nonlinear scenario.

[1]At least for practical approaches, since the number of coefficients will rise very fast.

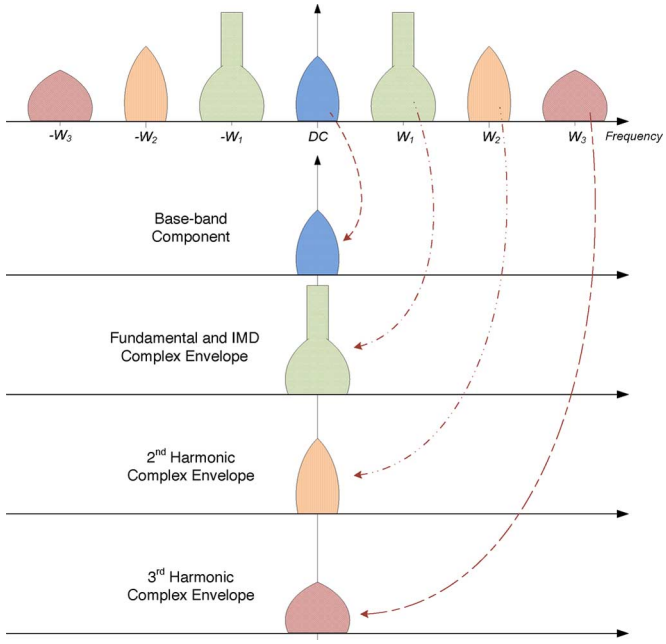


Fig. 3. Conversion to the low-pass equivalent of each cluster.

After this approach, the Volterra model will be a collection of different models for each cluster that were extracted individually, as illustrated in Fig. 4. Mathematically this is nothing more than to have the same Volterra operator, but now applied to the complex envelope signal, so the input will be the complex envelope of $x(t)$ and the output will be a collection of output complex envelopes corresponding to each low-pass cluster.

The baseband and second harmonic arise from a second-order multiplication

$$\tilde{y}_{\text{BB}}(k) = \tilde{h}_0 + \sum_{q_1=0}^{Q_{A1}} \sum_{q_2=q_1}^{Q_{A2}} \tilde{h}_{2,\text{BB}}(q_1, q_2) \cdot \tilde{x}(k-q_1) \cdot \tilde{x}^*(k-q_2) \quad (3)$$

$$\tilde{y}_{2\text{Harm}}(k) = \sum_{q_1=0}^{Q_{C1}} \sum_{q_2=q_1}^{Q_{C2}} \tilde{h}_{2,2\text{Harm}}(q_1, q_2) \cdot \tilde{x}(k-q_1) \cdot \tilde{x}(k-q_2) \quad (4)$$

where h_0 is the dc value of the output and $h_{2,\text{BB}}$ and $h_{2,2\text{Harm}}$ are the second-order Volterra kernels for the baseband and second harmonic responses, respectively. The character $\sim$ means that it is a complex signal or value, and the symbol $*$ symbolizes the complex conjugate. Notice the different memory lengths utilized on the baseband and second harmonic components that are represented by Q_{A1}/Q_{A2} and Q_{C1}/Q_{C2}, respectively.

On the other hand, the in-band linear signal and intermodulation distortion arise from the combination of a third-order

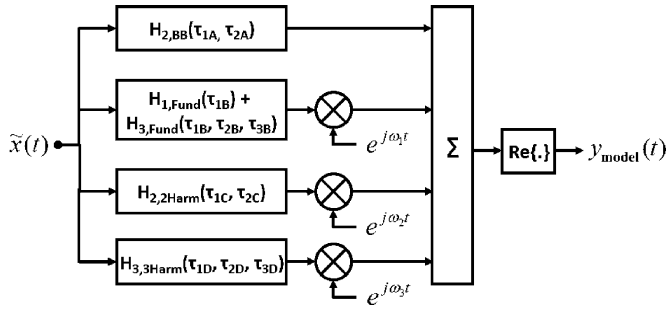


Fig. 4. Proposed design for the wideband behavioral model.

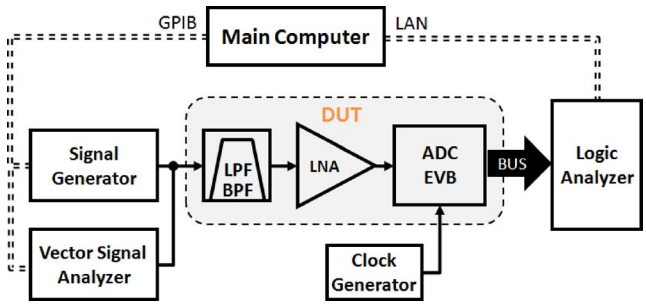


Fig. 5. Experimental test bench. From [10].

degree polynomial with a first-order contribution

$$\tilde{y}_{\text{Fund}}(k) = \sum_{q_1=0}^{Q_{B1}} \tilde{h}_{1,\text{Fund}}(q_1) \cdot \tilde{x}(k-q_1) + \sum_{q_1=0}^{Q_{B1}} \sum_{q_2=q_1}^{Q_{B2}} \sum_{q_3=q_2}^{Q_{B3}} \tilde{h}_{3,\text{Fund}}(q_1,q_2,q_3) \cdot \tilde{x}(k-q_1) \cdot \tilde{x}(k-q_2) \cdot \tilde{x}^*(k-q_3). \quad (5)$$

Finally, the third harmonic arises from a third-order degree polynomial

$$\tilde{y}_{3\text{Harm}}(k) = \sum_{q_1=0}^{Q_{D1}} \sum_{q_2=q_1}^{Q_{D2}} \sum_{q_3=q_2}^{Q_{D3}} \tilde{h}_{3,3\text{Harm}}(q_1,q_2,q_3) \cdot \tilde{x}(k-q_1) \cdot \tilde{x}(k-q_2) \cdot \tilde{x}(k-q_3). \quad (6)$$

If higher orders are needed, then more Volterra kernels should be calculated. It should be noticed that, in each cluster, we should include all the possible contributions. For instance, if a fifth-order polynomial is expected, then the third harmonic will arise from a polynomial that is the combination of a third-order coefficient with the fifth-order coefficient.

Afterwards, as sketched in Fig. 4, the output signal is up-converted to the corresponding cluster center frequency and all the selected components are sum together.

Again, it should be stressed that, in each cluster, we can use the nonlinear order and memory depth that we want, and thus, separate clearly different approaches.

IV. Parameter-Extraction Procedure

A simple BPSR was designed (Fig. 1) using laboratory components, mainly for demonstrative purposes. For that we used several BPFs to select the desired NZ to be modeled: in this case, two different NZs were tested. This was followed by a commercially available wideband LNA (0.5–1000 MHz) with a 1-dB compression point of +9 dBm, an approximate gain of 24 dB, and a noise figure of nearly 6 dB. We used a commercially available 12-bit pipeline ADC that has a linear input range of approximately +10 dBm with an analog input bandwidth of 750 MHz (−3-dB bandwidth of the sample-and-hold circuit). The ADC used a clock frequency of 90 MHz.

Considering this clock frequency, at the output of the DUT, we will have several NZs of 45 MHz $(f_s/2)$ of bandwidth for each one. Thus, we decided to use for our examples different excitations with different carrier frequencies of 11.5 MHz for the first NZ and 69 MHz for the second NZ.

In order to correctly characterize the constructed BPSR [device-under-test (DUT)], we have then implemented the setup presented in Fig. 5. This laboratory setup is based in the mixed-mode test bench proposed in [15], and as was exemplified in [16], it is dedicated to mixed mode characterization (SDR front ends).

As we can observe in Fig. 5, the analog input is sampled by a vector signal analyzer (VSA), which already gives the desired complex envelope signal to be used in the behavioral model extraction. The output is sampled using a logic analyzer (LA), being a digital representation of the analog signal. Also, these instruments should use the same sampling frequency or a multiple value, of the one that will be applied to the DUT as a way to maintain synchronization between the input and output signals.

Although, it is not shown in the figure, we have locked all the instruments to a 10-MHz reference and used trigger signals between the instruments. It is also important to note that all of the measurements were done using excitation frequencies according to the coherent sampling [17] in order to reduce any spectral leakage that could appear.

However, in this laboratory measurement setup, we do not have synchronized samplers between the different domains (analog and digital). Thus, in the performed measurements, we have used a triggering pulse embedded in the input signal followed by the waveform excitation of interest (see Fig. 6) [15]. In this way, all the measurements will be corrected accordingly to that trigger signal and thus will be synchronized.

After this procedure, the samples that include the trigger signal and the first samples of the signal are deleted in order to eliminate any transient arising from the change of the trigger sequence to the waveform itself.

As we know, the output of this DUT is a digital word of a certain number of bits (N) that must be converted to an equivalent voltage signal in order to be used in the extraction and validation procedures.

Nevertheless, when the obtained measurements were analyzed, we observed that these measured output signals are highly corrupted by noise (instrumentation noise and noise generated in the DUT components). We notice that these noise levels are close to the distortion that we would like to model and also are not stable, which will make the parameter extraction impractical or provide misleading results.

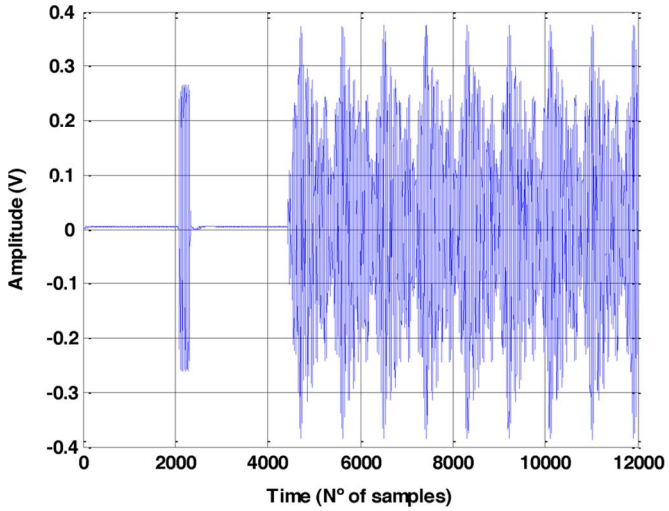


Fig. 6. Example of an excitation waveform including the triggering sequence initial pulse.

Thus, we have pursued a new approach that consists in the following steps.

Step 1) Apply a fast Fourier transform (FFT) to the output RF time-domain signals.

Step 2) Select only the desired frequency bins [10], [18] taking into account the nonlinearity order considered and construct a noise-free signal, only with the selected frequency components, for each one of the clusters decided to be extracted.

Step 3) Afterwards, apply an inverse fast Fourier transform (IFFT) in order to obtain a cleaner (without undesired frequency components and out-of-band noise) time-domain signal for each cluster.

Step 4) Calculate the complex envelopes (e.g., using the Hilbert transform) for each cluster of the rearranged output signals.

Step 5) Apply the low-pass equivalent Volterra-series model [see (3)–(6)] to these new output signals also using the measured input complex envelope and obtain the desired low-pass complex Volterra kernels.

Step 6) Up-convert each output complex signal to the corresponding cluster center frequency, depending on the resultant frequency from (1), and finally assess the model performance.

The previous steps for the extraction process can be generalized as shown in the flowchart diagram (Fig. 7).

As was previously mentioned, in Step 5), we are able to decide the nonlinear orders and memory taps that are more convenient for each cluster. This way the overall number of required parameters to match the output signals can be reduced by using this separate processing.

Another point that should be mentioned here is the fact that when the input signal falls in an even-order NZ, the output signal at the output of the DUT will appear rotated (reversed) (Fig. 2). In that sense, before we are able to apply all the steps of the proposed approach, we should first rotate back the signal in the frequency domain [between Steps 2) and 3)] and then apply the next proposed steps.

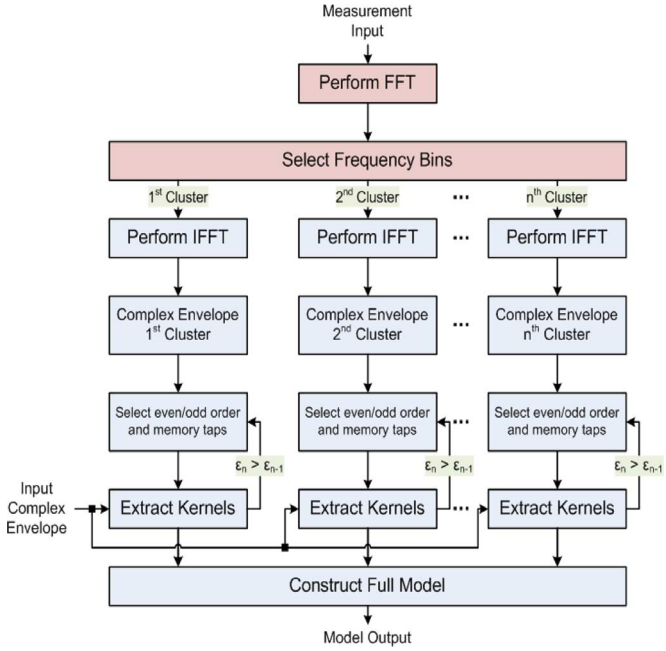


Fig. 7. Flow diagram of the kernels extraction procedure.

In order to reduce even more the impact of the measurement noise, we have taken several independent measurements for the output signals and then averaged them diminishing in that way the noise level significance [19].

Thus, considering that the input signal is sufficiently rich, i.e., one that presents a high variability and that the output of the Volterra series model is linear with respect to its parameters, the several low-pass complex Volterra kernels can be determined using a least squares technique, which is expressed by

$$H = (\mathbf{X}^T\mathbf{X})^{-1}\mathbf{X}^T Y \tag{7}$$

where $\mathbf{X}$ and Y are the input complex signal matrix and the output signal vector, respectively, and H is the vector of complex kernels that we are looking for. Thus, this least squares extraction has to be performed for each one of the clusters selected.

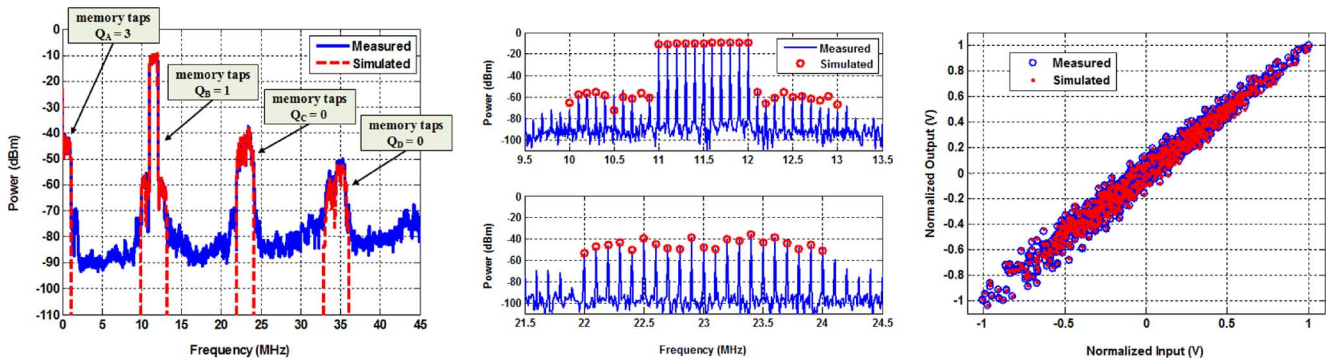
For instance, if we want to determine the complex parameters for the baseband cluster considering a memory length of Q taps, the input signal matrix $(\mathbf{X})$ should be composed by (8), shown at the bottom of the following page, and Y, the complex output at baseband frequencies, is obtained as

$$Y = [\,\tilde{y}_{\mathrm{BB}}(0) \quad \cdots \quad \tilde{y}_{\mathrm{BB}}(n) \quad \cdots \quad \tilde{y}_{\mathrm{BB}}(N)\,]^T \tag{9}$$

where Q represents the memory length and N is the number of samples captured for the input complex envelope signal and for the output signals.

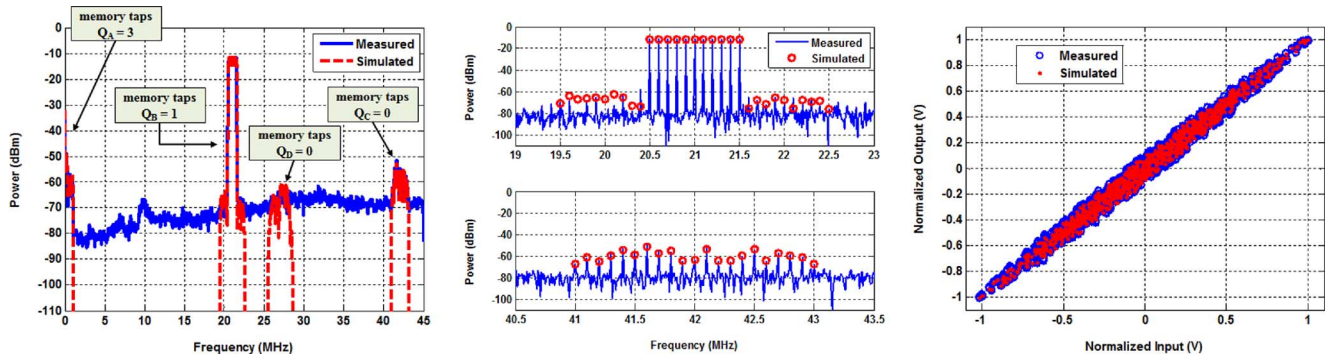
Thus, H can be then calculated using (7). This result has the advantage of notational simplicity and general applicability. H is actually composed by the following Volterra operators:

$$H = [\,\tilde{h}_0 \quad \tilde{h}_{2,BB}(0,0) \quad \tilde{h}_{2,BB}(0,q) \quad \cdots \quad \tilde{h}_{2,BB}(Q,Q)\,]^T. \tag{10}$$



(a) (b) (c)

Fig. 8. Measured and simulated results for the multisine excitation centered at 11.5 MHz (first NZ). (a) Entire subsample bandwidth (smoothed). (b) Carrier band and second harmonic band (zoomed in). (c) AM/AM characteristic.



(a) (b) (c)

Fig. 9. Measured and simulated results for the multisine excitation centered at 69 MHz (second NZ). (a) Entire subsample bandwidth (smoothed). (b) Carrier band and second harmonic band (zoomed in). (c) AM/AM characteristic.

Afterwards, we execute the design depicted in Fig. 4 in order to first construct the response for each individual cluster and then the final response of the behavioral model. Finally, each cluster is up-converted to the respective frequency obtained with the help of (1).

As was noted in the wideband behavioral model presented in Section III, in the Sections V and VI, we will assume that our behavioral model is truncated at the third-order nonlinearity. In terms of memory length, we have considered the number of taps that gives the lowest error between the measured and simulated signals for each cluster of nonlinearities independently.

We would like to emphasize that great care should be taken when choosing the carrier frequencies, signal bandwidth, etc. due to the folding process that happens in this DUT. This is very important because we do not want, at least until the third-order nonlinearity, that the signal falls in overlapping frequency bins where this model extraction will no longer be valid.

TABLE I
MEASURED AND SIMULATED POWERS FOR THE MULTISINE EXCITATION

	1st NZ (f_c = 11.5 MHz)		2nd NZ (f_c = 69 MHz)	
	Meas. (dBm)	Model (dBm)	Meas. (dBm)	Model (dBm)
Base-band	-32.7	-33.1	-44.1	-44.7
Fundamental	0.19	0.21	-1.49	-1.51
IMD_3 (Lower)	-48.5	-49.0	-56.5	-56.6
IMD_3 (Higher)	-50.6	-49.8	-58.6	-59.6
2nd Harmonic	-9.8	-9.8	-44.0	-44.5
3rd Harmonic	-40.2	-42.6	-52.6	-50.8

$$\mathbf{X} = \begin{bmatrix} 1 & \tilde{x}(0)\tilde{x}^*(0) & \tilde{x}(0)\tilde{x}^*(-q) & \cdots & \tilde{x}(-Q)\tilde{x}^*(-Q) \\ \vdots & \vdots & \vdots & & \vdots \\ 1 & \tilde{x}(n)\tilde{x}^*(n) & \tilde{x}(n)\tilde{x}^*(-q) & \cdots & \tilde{x}(n-Q)\tilde{x}^*(n-Q) \\ \vdots & \vdots & \vdots & & \vdots \\ 1 & \tilde{x}(N)\tilde{x}^*(N) & \tilde{x}(N)\tilde{x}^*(N-q) & \cdots & \tilde{x}(N-Q)\tilde{x}^*(N-Q) \end{bmatrix} \tag{8}$$

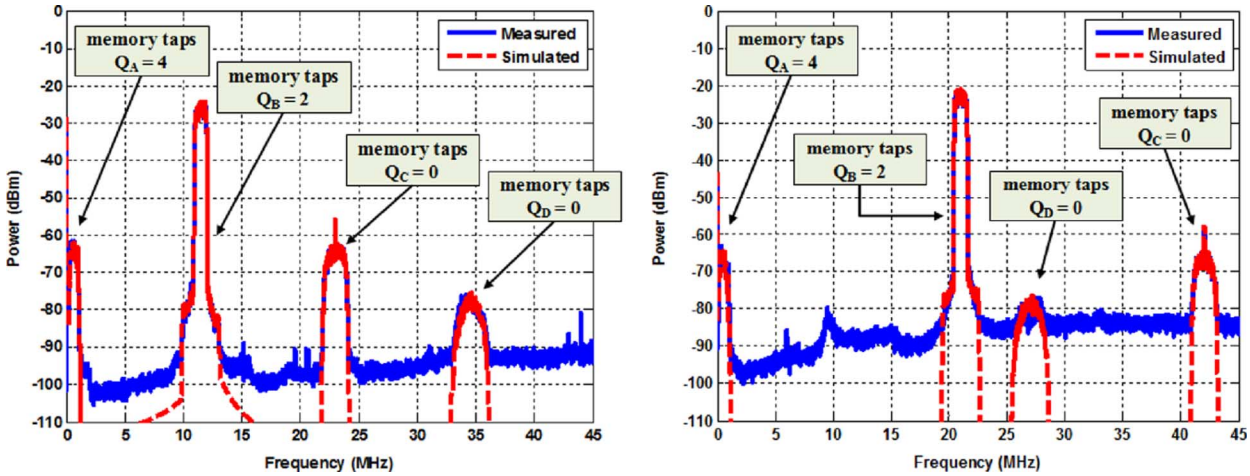


Fig. 10. Entire bandwidth (smoothed) of measured and simulated outputs for a QPSK signal centered at: (*left*) 11.5 MHz and (*right*) 69 MHz.

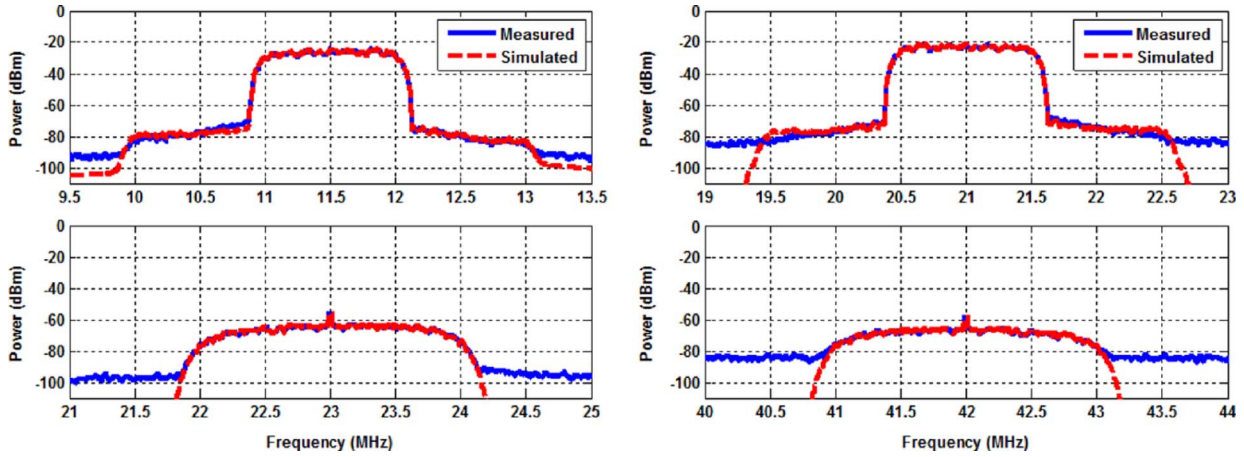


Fig. 11. Spectrum of measured and simulated carrier band and second harmonic band for a QPSK signal at: (*left*)11.5 MHz and (*right*) 69 MHz.

V. Model Validation With a Multisine Signal

The first action to evaluate the performance of the proposed behavioral model was to excite the DUT with a multisine signal with 11 tones carrying random phases in a bandwidth of 1 MHz, which creates a peak-to-average power ratio (PAPR) of around 6.4 dB. We have used the laboratory setup shown in Fig. 5 to perform several measurements. Using the captured input (complex envelope) and output waveforms, we then carry out the extraction of the necessary parameters. Afterwards, in order to assess the accuracy of the complete behavioral model, we used measurements from another multisine with similar statistical and spectral properties.

We then applied the steps explained in Section IV and merged the equations associated to each specific cluster (3)–(6) into a final complete model output, as shown in the following expression:

$$y(k) = \mathrm{Re}\{\tilde{y}_{\mathrm{BB}}(k) + \tilde{y}_{\mathrm{Fund}}(k)\cdot e^{jw_1 t} + \tilde{y}_{2\mathrm{Harm}}(k)\cdot e^{jw_2 t} + \tilde{y}_{3\mathrm{Harm}}(k)\cdot e^{jw_3 t}\}. \quad (11)$$

The obtained results are shown in Figs. 8 and 9 for the two different NZs evaluated. Looking at the figures, we can roughly say that the behavioral model and the described parameter extraction is estimating the unknown parameters well and producing very similar results for the two different NZs excited. Moreover, in Figs. 8 and 9(a), it is possible to observe the different memory depths (taps) in each particular nonlinear cluster necessary to achieve the obtained results.

In order to be more precise, we have verified the integrated power measured in the fundamental signal, lower and upper third-order intermodulation distortions, baseband component,

TABLE II
Measured and Simulated Powers for the QPSK Excitation

	1st NZ (f_c = 11.5 MHz)		2nd NZ (f_c = 69 MHz)	
	Meas. (dBm)	Model (dBm)	Meas. (dBm)	Model (dBm)
Base-band	-41.7	-42.9	-44.6	-45.4
Fundamental	-3.01	-3.02	0.40	0.38
Adj. Ch. (Lower)	-53.3	-54.6	-52.7	-52.5
Adj. Ch. (Upper)	-55.9	-56.0	-50.3	-51.2
2nd Harmonic	-38.5	-38.5	-40.8	-40.9
3rd Harmonic	-51.6	-52.2	-52.8	-53.0

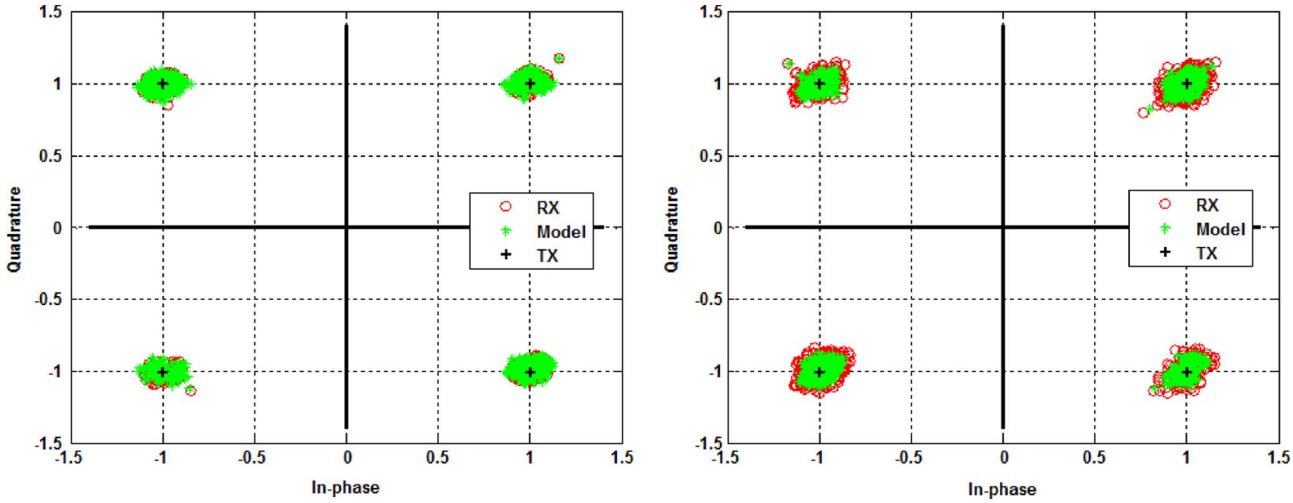


Fig. 12. Normalized constellation diagrams for the QPSK signal centered at: (*left*) 11.5 MHz and (*right*) 69 MHz.

and second and third harmonics. These results are exposed in Table I for the two NZs for both the measurements and the model. Clearly, the behavioral model follows the measurements quite well. Only in the third harmonic powers can we detect a perceptible difference (around 2 dB) that is mainly due to the proximity to the noise floor where the parameter extraction starts to become noise corrupted (even though we take out the out-of-band noise we will always have the in-band noise contribution).

It is also interesting to see that the two NZs present different AM/AM curves and that our model is accompanying the measured behavior, including the dynamics.

Finally, another commonly used figure of merit to characterize the performance of models will be used to compare the quality of our extracted model. This figure is called the normalized mean squared error (NMSE) [20]. Wherein we compared the obtained output from the behavioral model with the complete measured output signal (with all the other out-of-band noise and distortion) and the achieved values were -32.4 dB for the first NZ and -31.8 dB for the second NZ. We emphasize these results due to the fact that we are measuring at the output of the DUT a large bandwidth of 45 MHz shared by the two NZs being evaluated. All these results give a first confirmation about the strength of the proposed behavioral model.

VI. Model Validation With a Quadrature Phase-Shift Keying (QPSK) Signal

In order to corroborate the validity of the proposed model for a BPSR, we have applied an RF QPSK modulated signal with a symbol rate of 1 Msymb/s filtered with a square-root raised cosine (RRC) filter with a roll-off factor of $\alpha = 2.22$, which determined a signal PAPR of approximately 5.4 dB.

After that, we follow a similar approach as in the case of the multisine signal, and utilized part of the captured input complex envelope and output signals to carry out the extraction of the essential parameters. The remaining part of the samples was used to compare the behavioral model output with the measurement results. The same laboratory implementation (Fig. 5) was utilized and once again performed a large number of measurements to be able to then average and reduce the noise-level contribution.

A. Frequency-Domain Results

The obtained measured results compared with the ones achieved by the proposed behavioral model are shown in Figs. 10 and 11. Analyzing these figures, we can affirm that the behavioral model produces very good results for the two NZ signals, approximating well all the most important components of the QPSK signal. Also, it can be seen in Fig. 9 that the different memory lengths in each nonlinear cluster needed to obtain the presented results for both NZs tested.

Once again we have measured the integrated powers present in the fundamental signal, lower and upper adjacent channels, baseband component, and second and third harmonics. These results are shown in Table II for the two NZs evaluated. There it can be observed that our behavioral model is matching the performance of the DUT's measurements very well.

Contrary to the multisine case here, the model prediction of the third harmonic was acceptable, which, in our opinion, is due to the fact that the possible error that could appear there is spread along the entire third harmonic bandwidth. In that way, the noise impact on this error prediction is not so perceptible as it were in the multisine signal.

Moreover, we have again expressed the modeling error in terms of NMSE and the comparison between the complete measured output signals and the presented behavioral model results reached NMSE values of -33.0 dB for the first NZ excitation and -32.9 dB for the second NZ excitation.

As can be noted in the multisine outcomes, in these results, we can observe an increase in the noise floor of the second NZ when compared to the first NZ, which can be explained by a higher bandwidth of the filter used for this NZ, but also due to the impact of the sampling clock jitter.

In fact, the effects of clock jitter, that are less important for low-frequency purposes, are magnified when the ADC (or, to be more specific, sample-and-hold circuit) samples higher frequency or higher slew-rate signals. Such signals are found in

TABLE III
MEASURED AND SIMULATED EVM VALUES FOR THE QPSK EXCITATION

	1st NZ (f_c = 11.5 MHz)		2nd NZ (f_c = 69 MHz)	
	Meas.	Model	Meas.	Model
EVM *rms*	4.23 %	4.97 %	6.85 %	5.2 %
EVM peak at Symbol	16.39 % (703)	16.15 % (703)	22.13 % (898)	19.24 % (898)

bandpass sampling applications. The effect on the signal-to-noise ratio (SNR) is demonstrated by the equation [21]

$$\mathrm{SNR} = 20 * \log_{10}\left(\frac{1}{2\pi \cdot f \cdot t_j}\right) \tag{12}$$

where f is the carrier frequency of the signal and t_j represents the clock aperture jitter.

Thus, if we look to the previous equation, it is possible to state that the SNR is reduced if we use a clock signal with worse aperture time jitter, but it is also degraded with the increase in the carrier frequency, as was seen in these measurements.

B. Symbol Evaluation Results

At this point, we implemented a digital version of a QPSK demodulator in order to obtain the symbol information (around 1000 symbols) from the previously generated QPSK signal when it passes through the DUT in two different NZs.

Here, we would like to demonstrate that our proposed model also predicts the behavior of the slow symbol rate signal well enough when compared to the sampling frequency used, which carries the useful information.

Fig. 12 illustrates the normalized constellation diagrams for each NZ addressed and we can verify once again the very good performance of the proposed behavioral model and the respective parameter-extraction procedure. These assumptions are confirmed by the values presented in Table III, where a good matching in terms of root mean square (rms) error vector magnitude (EVM) and also in the peak EVM is observed.

VII. CONCLUSION

This paper has proposed and explained the concept of a new wideband behavioral model for BPSRs. It is accompanied by an innovative parameter-extraction procedure that is able to solve the problem of the BPSR folding process.

The proposed behavioral model and the respective parameter extraction was clearly validated by using two different excitations—multisine (deterministic) and QPSK (statistical) signals—when they were applied in two different NZs.

The presented parameter extraction allows a reduction in the number of required parameters to approximate the measured and simulated output signals by using separate processing for each cluster selected.

Contrary to what was been obtained with the previous behavioral model format [10], in this paper, we were able to much more precisely match the entire behavior of the DUT (huge differences in the baseband component that were nicely predicted here).

Moreover, the proposed model format is much more flexible and easily extended to higher NZs, which may present other nonlinearities and memory length considerations.

As well, this new behavioral model scheme has the freedom to be simply expanded to other fields with quite different applications that demand large bandwidth characterization.

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[J3] – Improving Dynamic Range of SDR Receivers for Multi-Carrier Wireless Systems

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Improving Dynamic Range of SDR Receivers for Multi-Carrier Wireless Systems

Pedro M. Cruz, *Student Member, IEEE*, Nuno Borges Carvalho, *Senior Member, IEEE*

***Abstract*— This paper presents a novel architecture to increase the instantaneous dynamic range of multi-carrier wideband digital receivers. This topology will see applicability in the high dynamic range front-ends for software defined radio and cognitive radio solutions.**

It will be proved that for multiband signals presenting a specific statistical pattern the now presented technique can increase the dynamic range of SDR receivers.

The theory will be evaluated using simulations and measurements of a real SDR RF front end receiver, when using multiband communication signals. Moreover, the proposed approach will also be compared with existing alternatives.

***Index Terms*—Dynamic range, multi-carrier, wideband receiver, software-defined radio.**

I. Introduction

HIGH dynamic range is a very important figure of merit when dealing with multi-carrier wideband digital receivers. In fact, the future RF architectures for software-defined radio (SDR) and especially cognitive radio (CR) will move fast to multi-carrier/multi-standard wideband front ends, which imply high dynamic ranges for its components in order to cope with very different power levels at the same time.

In this respect, in [1] Mitola has proposed that the receiving unit for an SDR should have a very wide bandwidth analog-to-digital converter (ADC) to gather and convert all the signals from analog to digital, and that ADC should have a wide dynamic range associated, since it may receive low power signals combined with high power ones, and considering that if the radio has to receive several different signals they should not combine with each other.

Also, the emergence of RF mixed signal circuits as the SDR and its subsequent step up to CR approaches [2] have opened a new field of research in order to find a feasible transceiver architecture to be utilized.

In these SDR/CR scenarios the incoming signal can comprise several different modulations conjugated with orthogonal frequency division multiplexing (OFDM) which can have very high peak-to-average power ratios (PAPR), and thus if the receiving unit is not designed accounting with these drawbacks, in the end it will degrade completely the quality of the received signal. A helpful solution for that could be the use of the available peak reduction techniques. Nevertheless, specifically for the receiving unit those peak reduction techniques are not easy to be applied or not practical. Other useful approach is to find for special architectures that in some manner increase the receiving dynamic range without degrade the initial quality of the incoming signals.

In that respect, this topic has been attracting the interest of the scientific community as can be perceived by a significant number of issued patents [3-5].

The work in [3] is appointed to wideband receivers and relies on the application of varying gains/attenuations to the input signal and then feeds the scaled signals to conventional ADCs followed by a multiplexer that will output a higher number of bits than each single ADC.

The later works [4, 5] make use of programmable gain amplifiers or amplifiers with different gains to adjust the input signal before the conversion by two parallel ADCs, and then digital signal processing (DSP) is applied to select the correct digitized signal.

Nevertheless, in none of the previous works it is clear how much dynamic range will be added and the lack of possible implementation constraints is a rough shortcoming.

Additionally, these techniques rely on the use of active devices that will increase the overall DC power consumption and potentially inherent nonlinear distortion when in presence of high-power interferers.

Moreover, in [6] a newly technique to extend the dynamic range of the A/D conversion was proposed, which uses an analog signal splitter followed by two ADCs and digital reconstruction of the input signal. There, it is claimed an improvement in the dynamic range of around 6 dB confirmed by several simulations, but again, the proposed architecture is built with active devices that will pose the same restrictions of previous works.

Thus, the main motivation of this paper is to propose a novel architecture for instantaneous dynamic range extension in wideband digital receivers when subjected to wideband multi-carrier excitations. In fact, a first approach to this technique has started in [7] where a comparable architecture accompanied by a digital reconstruction procedure was validated by several simulations for a single-carrier application.

In order to achieve this goal, the paper is organized in the following way; firstly some introductory concepts about the digital receivers and the importance of dynamic range are

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given. Section III will summarize the most important existent techniques for receiver dynamic range enhancement. Then, in Section IV, a novel architecture to increase the dynamic range of digital receivers will be proposed, which is appropriate for multiband high PAPR signals handling. Section V illustrates firstly with simulations the performance in terms of dynamic range of the proposed architecture against other feasible techniques for single and multi-carrier applications. Afterwards, the addressed architecture is further validated by a measurement example of a multi-carrier excitation composed by a high-power signal interfering on a low-power QPSK modulated signal. Finally, some conclusions will be drawn summarizing the obtained results.

II. Dynamic Range in Wideband Digital Receivers

In order to start this discussion we will explain the concept of dynamic range and its importance in multi-carrier wideband digital receivers.

A digital receiver [8] offer several advantages over their analog version because once a signal is digitized, the following processing will be entirely done at the digital domain allowing highly flexible and adaptable designs. These types of receivers become even more attractive due to the constant advancements in ADCs and FPGA/DSPs speeds and capabilities.

In a digital receiver the input signal is down-converted into an intermediate frequency (IF), either by a normal mixing stage or by using wideband sampling circuits (bandpass sampling phenomena), and then the signal is converted to the digital domain by using a high sampling rate ADC.

One feasible implementation of such a type of multi-carrier digital receiver is the bandpass sampling receiver (BPSR), [9, 10], shown in Fig. 1, essentially when it is considered for IF sampling scenarios. Perhaps one of the least understood components in such IF sampling receivers is the ADC (including the wideband sampling circuit) because it digitizes several channels at same time and thus, its functional dynamic range will be a stringent requirement.

In addition, assuming that dynamic range of a certain radio receiver is essentially the range of signal levels over which it can operate, it is not always easy to compare one set with another because it can be quoted in a number of ways.

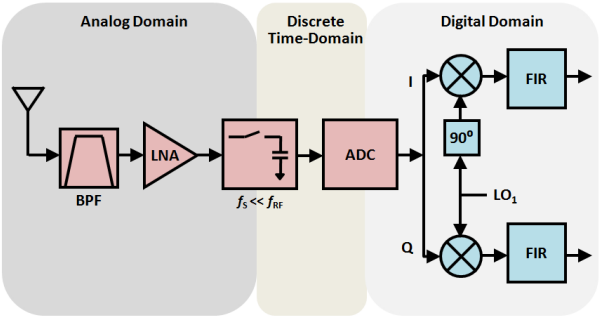

Fig. 1 – Band-pass sampling receiver architecture. (From [11], used with permission.)

Therefore, in order to clarify the concept of receiver dynamic range we will address two different cases, single signal dynamic range and instantaneous dynamic range.

The single signal dynamic range is understood as the ratio between the strongest signal power properly received without being clipped and the lowest signal power properly detected by the receiver (sensitivity level). Contrarily, instantaneous dynamic range is related to the power ratio of the maximum and minimum incoming signals that can be properly received at the same time. For instance, considering these definitions we may have a receiver with 60 dB of single signal dynamic range, but having only 20 dB of instantaneous dynamic range, as can be understood in Fig. 2.

Hence, the imperative ADC component has a fixed dynamic range that is delimited up and down by certain intrinsic characteristics.

Ideally, the low end of the range is governed by the signal-to-noise ratio (SNR) referenced to the ADC full-scale input, which is controlled by the inherent quantization error. It can be shown that this quantization error depends on the number of bits of the given ADC and the best case SNR can be calculated as:

$$\mathrm{SNR}_{\mathrm{dBFS}} = 6.02 * N + 1.76 \qquad (1)$$

where N is the number of bits of the ADC. Equation (1) is only valid if the noise is measured over the entire Nyquist bandwidth from DC to $f_s/2$. Moreover, if the signal bandwidth (BW) is less than $f_s/2$ then the achievable SNR may be increased and thus, a more correct expression for this condition is given by:

$$\mathrm{SNR}_{\mathrm{dBFS}} = 6.02 * N + 1.76 + 10 * \log_{10}\left(\frac{f_s}{2*BW}\right) \qquad (2)$$

The above equation reflects the condition called oversampling, where the sampling frequency is higher than twice the signal bandwidth.

Nonetheless, in a common receiver implementation, this low end limitation is managed most of the times either by the input noise floor or other associated effects such as the clock and internal timing jitter [12] mainly when it is operating at higher frequencies (IF sampling).

On the other hand, the high end is governed by its overload or strong signal handling performance. In the ADC component this is known as clipping distortion which occurs when the input signal exceeds the ADC full-scale range, and results in significant distortion (harmonic related or not) because the signal is rightly hard-clipped. This distortion is amplitude dependent and is of great importance in wideband multi-carrier digital receivers, due to the high PAPR of their signals and potential blockers in adjacent channels.

Taking into account what has been said, Fig. 2 presents a sketch that summarizes the limitations in terms of dynamic range and points where it can be improved, which is appointed by potential techniques to augment the high-side and low-side margins of the instantaneous dynamic range. Existent techniques to improve receiving dynamic range will be addressed in the next Section.

As a result, considering the situation of a single signal excitation it is possible to use an automatic gain control (AGC) circuit to follow the power variation of that signal. In a typical AGC device a feedback loop is used, wherein the output power level of this device is monitored and directly provides the regulation of the device gain itself, thereby maintaining its output power at a relatively constant level.

For example, in a common situation the AGC device may be configured to maintain the output power level between the limits of the ADC dynamic range as close as possible to its upper limit in order to maximize the attainable SNR.

Nevertheless, if we consider a receiver for SDR and CR, particularly one operating over multiple bands, it is likely to encounter signals with very different power levels, either by the conjunction of several desired high and low power signals or by the combination of strong interferences and weak received signals. Thus, in such a situation no AGC device can compensate for the varying signal strengths because reducing the gain to cope stronger signals will reduce the sensitivity to weaker ones. In some cases the received signal from one wireless standard can block another, for instance, when a Wi-Fi access point is nearby, yet one wish to receive a GSM signal having a much lower power [13].

Obviously, some sort of AGC (variable or stepped) will continue to be used in practical radios to prevent receiver overload but this should be managed in a careful way and accompanied by other instantaneous dynamic range enhancement techniques.

III. Techniques for Dynamic Range Improvement

As was seen in Section II it is very desirable to come up with techniques to extend the instantaneous dynamic range of ADCs. As a matter of fact, there are a few existing solutions to make such an improvement, which range from the addition of variable gain amplification preceding the ADC stage, non-uniform quantization based on compression and expanding the signal, averaging of several ADC outputs, as well as other practical alternatives such as, oversampling and interleaving followed by digital filtering. In the following we will briefly address the general operation of the referred solutions.

A. Variable Gain Amplifier plus Analog-to-Digital Converter

One of the possible solutions that is widely used and valid in every receiver architecture, is to employ a variable gain amplifier (VGA) jointly with a power detector circuit before the ADC stage to execute the abovementioned AGC function. This action will in principle place the incoming signal within the ADC limited dynamic range allowing the linear digitization of the received signal and maximizing the respective SNR value.

However, considering the case of a multi-carrier wideband digital receiver, we might have high power signals simultaneously conjugated with low power ones, which makes the VGA working strategy totally impractical.

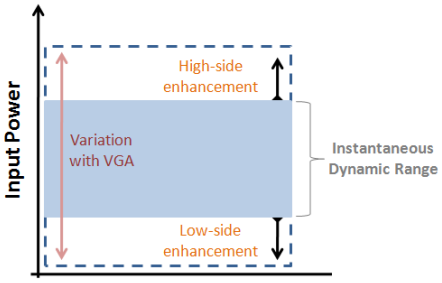

Fig. 2 – Illustration of limited instantaneous dynamic range and its potential improvements.

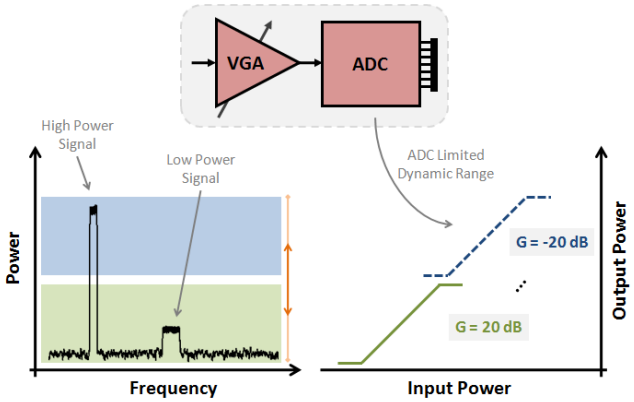

Fig. 3 – Explanation of the VGA plus ADC limitation when in a multi-carrier wideband scenario.

This happens because the VGA commonly controls the exact gain to apply in the current signal by measuring the integrated average power or peak power (diode detector) which will only focus on the high-power signal and could lead to the actual loss of the lowest signals.

On the other hand, if the VGA was capable to decide which signal to follow and focus on the low-power signal, it would increase its gain in order to receive the lower signal. However, in this situation, the high-power signal will completely saturate the upcoming device (ADC) and thus, generate a lot of distortion conducting to the loss of both signals.

Fig. 3 shows in detail that varying the gain of the VGA does not truly increase the effective dynamic range of a multi-carrier system, just move up and down the fixed ADC dynamic range.

Assuming that the dominant error is the ADC quantization, the VGA plus ADC will employ a constant error on the input signal despite its input power, as illustrated in Fig. 8 for a 4-bit (16 levels) quantization state.

B. Non-Uniform Quantization by Companding

A different approach that tries to overcome the limited ADC dynamic range issue is to perform non-uniform quantization on the input signal, [14], in order to concentrate the lower quantization levels in voltage regions with highest probability. In fact, observing the previous approach and especially Fig. 8, it can be detected that uniform quantization will be only optimal for uniformly distributed signals, which is not the experimented situation in actual wireless systems.

The works of Lloyd [15] and Max [16] are greatly recognized in the field of non-uniform quantization (also known as floating-point quantization), wherein an algorithm to determine the optimal (at a given time - require dynamic changes) non-uniform distribution of the quantization levels was proposed, which requires some knowledge about the distribution of the input signal. Although, the flexibility of this algorithm makes it seem attractive for SDR/CR applications, its implementation is unable to provide the required performance for wireless mobile applications.

One difficult yet feasible solution to design a non-uniform quantizer is to directly implement the partition and respective reconstruction levels in the conversion process, i.e., purposely construct a non-uniform ADC, as for example in [17].

A much easier and practical approach can be achieved by first passing the input signal through a nonlinear function ("compressor") followed a uniform quantizer and terminated by the inverse nonlinear function ("expander"), see Fig. 4.

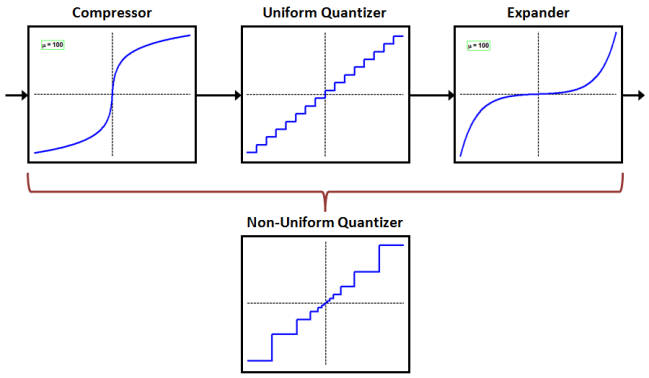

Fig. 4 – Diagram block implementation of the companding function.

The "compressor" and respective "expander" stages are represented by the following functions:

$$F(x) = sign(x)\frac{\log_{10}(1+\mu|x|)}{\log_{10}(1+\mu)} \qquad -1 \le x \le 1 \qquad (3)$$

$$F^{-1}(y) = sign(y)\frac{\left[10^{(\log_{10}(1+\mu).abs(y))}-1\right]}{\mu} \qquad -1 \le y \le 1 \qquad (4)$$

where x is the input signal at the "compressor", y is the input of the "expander", μ defines the degree of nonlinear compression, and *sign(a)* represents the signum function.

The complete process of these three consecutive stages is called "companding" and is the basis of μ-law and A-law algorithms [18], primarily used in the analog telecommunication systems to reduce the instantaneous dynamic range of audio signals. In a generic receiver implementation this approach may be realized by the use of a logarithmic amplifier (to perform the nonlinear gain curve) prior to the ADC device and then apply the inversion operation in the digital domain.

Once again, assuming that the ADC quantization is the dominant error, the "companding" approach performs a non-uniform quantization as shown in Fig. 8 using a 4-bit quantizer (center block of Fig. 4) and a μ value in the "compander" function (3) of one hundred. It is clear that the quantizing error affecting the input signal is smaller for low level values which allows the signal to be represented more accurately and presents a larger error for higher level signals leading to a coarsely representation. Moreover, this technique performs an enhancement in the low-side of the ADC instantaneous dynamic range, when compared to Fig. 2.

C. *Averaging Multiple Analog-to-Digital Converters*

Another well-recognized approach to augment the receiving dynamic range can be performed by, either parallelizing several ADCs and simply average the digital outputs or increasing (in multiples of two) the sampling rate of a single ADC and then, use each other sample to average [19]. Nevertheless, this second option is less desirable because faster ADCs may not yet be available and a faster sampling clock with low jitter is required.

In this implementation the signals are added directly, while the noise coming from each individual ADC if assumed to be uncorrelated will sum as the square root of the sum of the squares (root-sum-squares) which will improve the total SNR. The processing required to execute this functioning is commonly realized in a digital signal processor (e.g., FPGAs and ASICs).

Therefore, considering the case of two parallel ADCs having at the input a signal term (V_S) and a noise component (V_N) when applying this method it will result in a total output voltage that is given by:

$$V_T = V_{S\_ADC1} + V_{S\_ADC2} + \sqrt{V_{N\_ADC1}^2 + V_{N\_ADC2}^2} \qquad (5)$$

So, the signal has effectively been multiplied by two, while the noise part has been multiplied by $\sqrt{2}$, thereby increasing the achievable SNR by a factor of $2/\sqrt{2}$ or 3.01 dB. As well, if more ADCs are implemented in parallel we may get even more improvement in the SNR value, yielding around 6 dB using four equivalent ADCs, and so on.

Theoretically, the achievable enhancement is dictated by the number of used ADCs (N) as $10*\log_{10}(N)$ decibels.

Obviously, this finding will only be true if the root-sum-square of the non-correlated noise sources (thermal noise, clock jitter noise, etc.) is higher than the intrinsic ADC quantization noise. Thus, an improvement in the overall noise floor may be obtained but its effectiveness is highly dependent on the characteristics of its dominant noise sources. Nonetheless, this averaging technique is able to reduce the uncorrelated noise power but has no effect on distortions inherent to the specific ADC design, improving in that sense the SNR, but not the spurious free dynamic range.

Moreover, the accomplishment of a system like this requires a huge design effort and strictly careful processes on the prototyping, qualification and testing phases.

As in the case of the technique shown in Section III.B, this procedure enhances the low-side of the ADC instantaneous

dynamic range, as regards to what was presented in Fig. 2.

D. Other Feasible Techniques

Other proposed techniques include oversampling and interleaving of ADCs [20, 21].

As previously mention in Section II and pointed out in (2), sampling a certain signal with a rate higher than twice of its bandwidth can bring gains in terms of signal SNR.

Actually, the faster the signal is sampled the lower will be the noise floor, since having a constant total integrated noise it will spread out over more frequencies. However, the full effect of this process can only be achieved when the signal is decimated and filtered.

Moreover, using the last part of (2), it is possible to observe that each time the sampling rate doubles the effective noise floor will improve by an amount of 3 dB.

On the other hand, instead of increase the sampling of a single ADC we could interleave several ADCs, which equally allow the sample rate to be increased and obtain SNR improvements in the same fashion. In order to realize this, each ADC should be drove with clock signals properly phased. This fact may create implementation difficulties when compared to the averaging method, because in that case the clock signals can be derived directly from a common signal splitter, as apart the interleaved situation requires a more complicate circuit.

In addition, when time-interleaving ADCs it is common to obtain, in the reconstructed output, beyond the desired signals other non-harmonic distortion products known as offset and image spurs, [22], which are directly related to gain, phase and offset matching errors between channel-to-channel. Thus, a very tight channel matching condition is required when searching for high SNR values.

In summary, oversampling and time-interleaving represent non-direct methods to increase the receiving dynamic range. Also, these two techniques are more complex to implement than the averaging procedure described in Section III.C, but these should not be discarded due to their potential effectiveness in specific situations.

IV. Proposed Architecture for Dynamic Range Enhancement

This section is devoted to explain a novel technique to increase the instantaneous receiving dynamic range.

The proposed architecture is based on a passive coupling component (coupler) followed by two parallel paths of ADCs sampled with equally phased clocks and then, digital signal processing is applied to reconstruct the incoming signal. A block diagram for the proposed design is sketched in Fig. 5.

A quick look into a few scientific publications encounters similar strategies employed in different fields of applications such as, in power meters [23] and in successive detection logarithmic amplifiers [24].

The main idea of the proposed architecture is to pass, as much as possible, to the digital domain the required processing in the sampled waveforms to then digitally reconstruct the incoming information. In this way, the signal that comes from subsequent RF/IF front end components pass through a passive coupler that separate the signal into two different portions, the highest part goes to the output being feed to ADC_1 and a small part of the signal is coupled with a certain coupling ratio and goes to ADC_2. As can be seen in Fig. 5, the input signal is intentionally clipped in the upper ADC_1 in order to take full profit from the ADC_1 dynamic range. Afterwards, digital signal processing is used in the two digitized waveforms to reconstruct the incoming signal.

An important part of the proposed architecture rely on the capabilities provided by current digital processors to execute the digital reconstruction of the received signal, which is performed in a discrete-time sample-by-sample approach and its flowchart diagram is depicted in Fig. 6.

The digital processing unit has to read the two ADC buses and an over-range indicator bit (OVR bit). Then, this OVR bit is used to control whether the information from the two ADCs is used or not in the signal reconstruction procedure.

If it is inactive only the data from ADC_1 is considered from these specific time samples, but if it is active, the data from ADC_2 is compensated with gain and phase values obtained during a calibration period and used in conjunction with ADC_1 data to reconstruct the received signal.

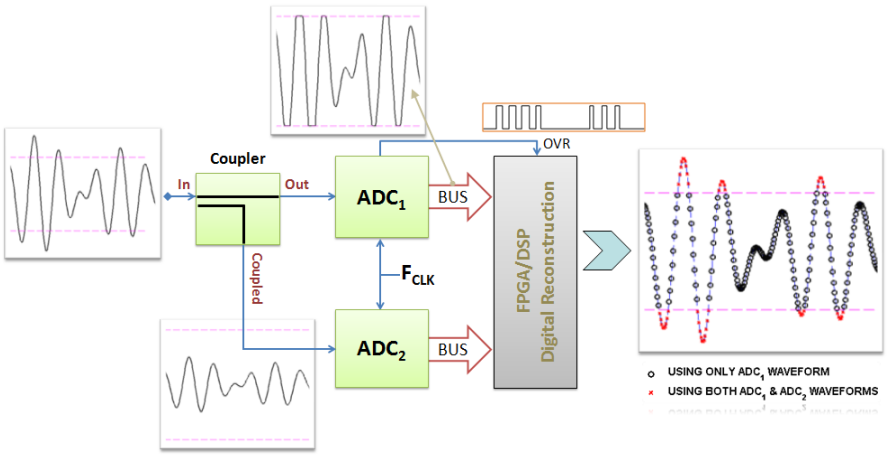

Fig. 5 – Proposed architecture to enhance the receiver instantaneous dynamic range with representative waveforms in relevant branches.

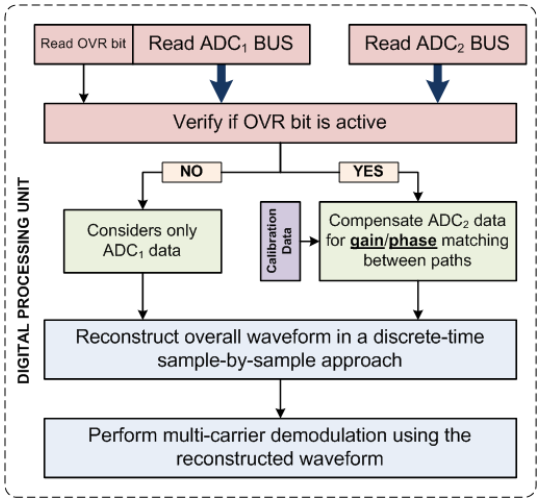

Fig. 6 – General flowchart diagram of the digital reconstruction procedure.

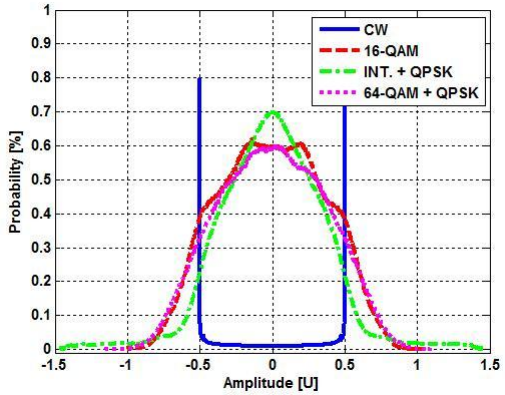

Fig. 7 – Probability density function of different signals.

As in the previous situations if it is assumed that the ADC quantization is the dominant error, the proposed design will work with two different constant quantization errors, as shown in Fig. 8 considering a 4-bit quantizer. Looking to that figure we can say that the improved performance of the proposed architecture is dependent on the statistics of the input signal, i.e., if the signal is mainly concentrated in the smaller values, then the minimum quantization error will be considered, while the large quantization error will be applied only to the high peaks of the input signal.

In that sense, Fig. 7 presents several probability density functions (PDF) for different wireless signals that will be considered in Section V. Over imposing these PDFs on the quantization patterns and respective errors depicted in Fig. 8, it can be stated that the proposed architecture when compared to the others is able to take advantage from the statistical distribution of the typical wireless input signals because they are mainly concentrated on the lower quantization part, except the constant envelope signals, as for instance a GSM signal.

Therefore, a correct evaluation of the input signal statistics mainly for wideband multi-carrier excitations [25] should be done in order to search for an optimal driving point that maximize the achievable dynamic range with the proposed architecture.

In summary, the instantaneous receiver dynamic range can be increased by the use of the proposed technique achieving improvements lower than the coupling ratio employed in the passive coupler. Also, contrarily to the techniques described along Section III, which focus on the low-side of the ADC dynamic range, the proposed technique is projected to enhance the high-side of the ADC instantaneous dynamic range. This functionality makes it suitable to receive high PAPR signals, typically in OFDM based systems, to resist to undesired strong interference signals, and to work on multiband multi-carrier scenarios.

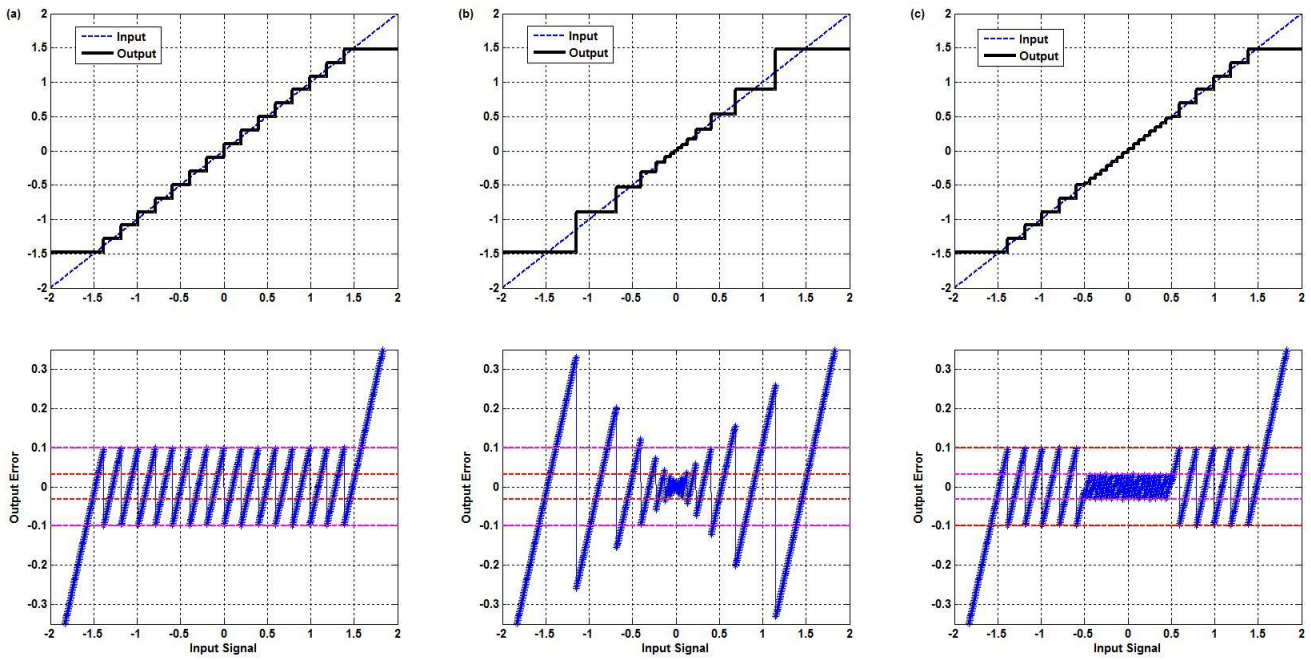

Fig. 8 – Different types of quantization (4-bit case) schemes produced by the different architectures: (a) VGA plus ADC, (b) companding, and (c) proposed.

V. Simulation and Measurement Results

In order to evaluate the performance of the proposed architecture compared to other existent designs several simulations were performed. After that, a measurement example based on the addressed simulations is presented in order to confirm the obtained results.

Three of the previously mentioned architectures were considered for performance evaluation, which includes the VGA plus ADC arrangement, the companding approach and the proposed technique.

As usual, all the architectures considered an AGC loop performed by an ideal VGA model before the exact design in order to allow the optimal driving point in each one and thus increase the adaptability of the evaluated systems.

Regarding the used simulation models they are based on MATLAB coding. The coupler model is constructed with S-parameters characterization obtained in a commercial vector network analyzer and then this data is used to replicate the overall transfer function in magnitude and phase for each port. In what concerns to the ADC model it represents the quantization and clipping behaviors and in this specific case an 8-bit ADC was considered to approximate the available commercial ADCs in the validating laboratory measurements. In addition, the ADC model considers a full-scale range of 2 Vpp, i.e., admits a maximum input power of +10 dBm (in a 50 Ω source) starting to clip after this value. The sampling clock frequency used was 90 MHz. No further specificities were embedded in the constructed models.

It is important to note that in the VGA plus ADC and companding situations the input signal is always drive in its optimum point and avoiding the clipping of any device (peak power after VGA always below +10 dBm). On the other hand, in the proposed architecture case the ADC_1 is always put into clipping even when operating with constant envelope signals. This can be executed because in the proposed design the full-scale limit after signal reconstruction is increased by the coupling ratio employed in the coupler component. Therefore, the new full-scale limit is situated around +20 dBm due to a 10 dB coupling ratio.

A. Single-Carrier Simulations

The first test to evaluate the performance of each architecture was to measure the attainable SNR when exciting it with a constant envelope sinusoidal excitation (CW) centered at 139 MHz (4^{th} Nyquist zone, NZ) being then bandpass sampled and appearing in the output at 41 MHz as illustrated in the upper part of Fig. 9.

This type of signal is exactly the worst case for the proposed architecture because its PDF is concentrated on the upper and lower limits, as shown in Fig. 7 by the curve labeled as "CW". Over imposing this curve in the quantization errors shown in Fig. 8 it can be seen that only a very small percentage of the signal passes through the lower quantization error with the proposed architecture.

The obtained results are presented in Table I.

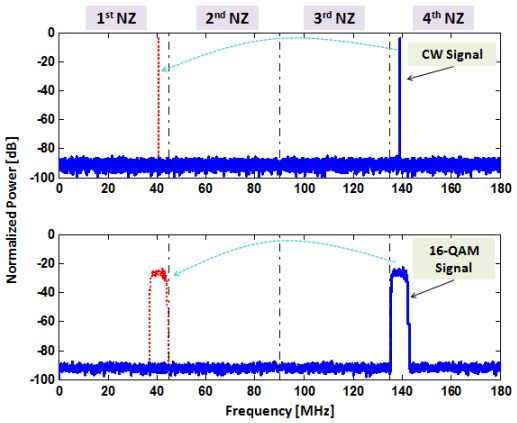

Fig. 9 – Input spectra for a single CW excitation (top) and a single 16-QAM modulated signal (bottom), before (solid line) and after the bandpass sampling procedure (dashed line).

TABLE I
SIMULATED SIGNAL-TO-NOISE RATIO VALUES FOR A CW EXCITATION

	VGA plus ADC	"Companding"	Proposed
SNR [dB]	48.9	39.1	49.9

TABLE II
SIMULATED ERROR VECTOR MAGNITUDE VALUES FOR A 16-QAM SIGNAL

Error Vector Magnitude	VGA plus ADC	"Companding"	Proposed
rms [%]	0.39	0.54	0.22
peak [%]	1.80	1.87	0.72

The second simulation experiment considered a 16-QAM modulated signal centered at the same carrier frequency of the previous CW signal. The 16-QAM signal carries a symbol rate of 6 Msymb/s and it is filtered with a square-root raised cosine (RRC) filter with a roll-off factor of $\alpha = 0.22$, which determines a signal PAPR of approximately 6.5 dB.

Because of the non-constant envelope of the 16-QAM modulated signal the driving points for each particular design has to be changed but this will be automatically handled by the VGA component.

The results presented in Table II show better error vector magnitude (EVM) values for the proposed architecture than the other approaches for both average and peak cases.

These results are completely in line with the ones obtained in the first simulation experiment.

Furthermore, in the two previous experiments a very low improvement was achieved mainly because of the VGA utilization, which brings the input signal to an optimum operating point. As well, the VGA application can be used to explain the worst performance observed in the companding design, which is supposed to greatly improve the achievable dynamic range when in single-carrier scenarios.

Even though, the proposed architecture is not intended for single-carrier excitations and constant envelope signals, the obtained performance is better than with the other evaluated techniques. This fact gives a first confirmation about the capabilities of the proposed architecture.

B. *Multi-Carrier Simulations*

A third evaluation procedure based on a multi-carrier excitation was accomplished, attempting to assess the impact of a high-power interferer in a low-power QPSK modulated signal. An illustrative input spectra is shown in Fig. 10.

In that way, the high-power interferer was executed by a multisine signal carrying random phases in a bandwidth of 2 MHz and centered at 109 MHz (3rd NZ) appearing in the output after bandpass sampling at 19 MHz. The low-power QPSK signal was kept at a carrier frequency of 139 MHz, transmitting a symbol rate of 5 Msymb/s and filtered by a RRC filter with a roll-off factor of $\alpha = 0.22$, determining a conjugated PAPR of approximately 9.2 dB.

Thus, in order to determine the truly dynamic range of each architecture the input power of the interferer was fixed at +10 dBm and the QPSK signal was swept between -20 dBc and -45 dBc, and then the resultant QPSK EVM was calculated.

The obtained results for the three evaluated architectures are shown in Fig. 11, in which it can be observed a great improvement in the instantaneous dynamic range by the proposed architecture. This means in other words that we still continue to properly demodulate a signal being received with a lower input power.

Moreover, it is also noted that the proposed architecture with two 8-bit ADCs is able to approximate the performance achieved in a VGA plus a 9-bit ADC design and thus, gaining almost one bit of instantaneous dynamic range.

As well, knowing that the companding architecture is focused in improving the SNR of low-power signals it is expectable that it performs, at least, better than the VGA plus ADC design, but what we see is that it is worse than the two other architectures. Despite that it can be explained by the VGA operation as previously stated, a better clarification for this finding is the fact that it is not intended for multi-carrier operation and thus, the strong interferer carry the low-power desired QPSK signal through a point where the quantization error is high leading to a higher error than the obtained with a uniform quantizer.

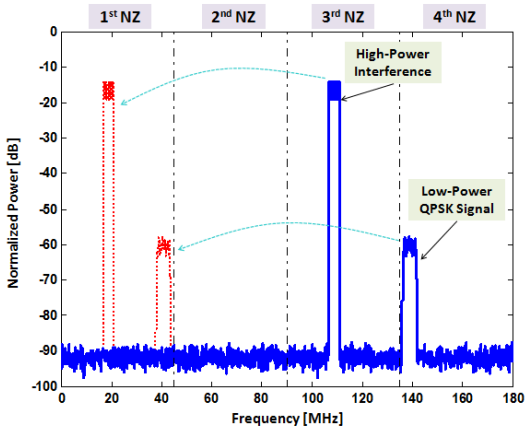

Fig. 10 – Input spectra of a multi-carrier signal composed by a high-power interferer and a low-power QPSK modulated signal, before (solid line) and after the bandpass sampling procedure (dashed line).

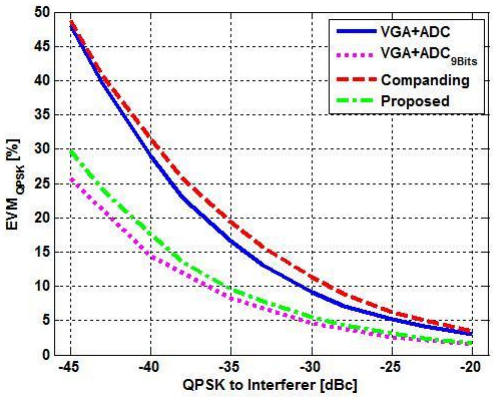

Fig. 11 – Simulated EVM values of a low-power QPSK signal being received simultaneously with a high-power interferer for the three architectures under evaluation.

Another test consisted in the computation of the EVM for two modulated signals having very different input powers and being received simultaneously. This multi-carrier excitation maintained the same carrier frequencies used in the previous tests and is composed by a high-power 64-QAM signal plus a low-power QPSK signal. The 64-QAM carries a symbol rate of 6 Msymb/s and the QPSK maintains the symbol rate of 5 Msymb/s being both filtered again by a RRC filter with the same roll-off factor, which has determined a combined PAPR of around 7.05 dB. The resultant PDF curve for this combination is shown in Fig. 7 with the label "64-QAM + QPSK", wherein it is obvious the similarity to a Gaussian-shaped distribution.

The obtained results for this multi-carrier combination of two modulated signals are presented in Table III. There it can be seen that the high-power 64-QAM signal is well demodulated in each architecture for all pairs of average input power tested, because this signal is always maintained in the optimal operating point getting in that way the highest SNR possible.

TABLE III
SIMULATED EVM VALUES FOR A MULTI-CARRIER EXCITATION COMPOSED BY A HIGH-POWER 64-QAM SIGNAL PLUS A LOW-POWER QPSK SIGNAL

	Average Input Power	VGA plus ADC	"Companding"	Proposed
64-QAM EVM [%]	+10 dBm	0.41	0.69	0.25
QPSK EVM [%]	-10 dBm [-20 dBc]	2.59	3.49	1.63
64-QAM EVM [%]	+10 dBm	0.54	0.49	0.34
QPSK EVM [%]	-20 dBm [-30 dBc]	8.11	11.20	5.24
64-QAM EVM [%]	+10 dBm	0.53	0.50	0.29
QPSK EVM [%]	-30 dBm [-40 dBc]	25.40	34.10	16.01

On the other hand, the low-power QPSK signal is masked by the available dynamic range due to the higher power 64-QAM signal, which is detectable in the increasing EVM values calculated for the QPSK signal.

Again the proposed architecture demonstrated better results than the two other designs for both EVM calculations and being the companding solution the worst case.

Based on the exposed simulation results we can affirm that an improvement of the instantaneous dynamic range can be achieved by the proposed architecture, which is also confirmed by the known direct relationship between EVM and SNR [26].

C. *Measurement Example*

Finally, in order to validate the proposed architecture for instantaneous dynamic range enhancement we have implemented two laboratory prototypes, one for the VGA plus ADC and another for the proposed architecture. We have decided to not implement a practical companding architecture mainly due to the weaker results obtained in the simulation experiments and also because it is a scheme quite difficult to be implemented, mainly in the process of calculating the exact inverse logarithmic function.

As happened in the simulation experiments a VGA device has also been used in the driving of the proposed architecture. Thus, in both cases a commercial stepped-gain VGA was employed being the gain parameter adjusted in order to drive each architecture to its optimal point.

To this VGA output was connected a commercial wideband (1-1000 MHz) directional coupler followed by two parallel 8-bit ADCs, which were properly clocked in phase using the same sinusoidal signal. Obviously, for the VGA plus ADC case it was just followed by a similar 8-bit ADC.

Then, from the previous simulation experiments we have chosen to validate the situation of a high-power signal interfering a low-power QPSK modulated signal. Therefore, signals with the same characteristics were generated and applied to both architectures under validation.

The laboratory setup implemented is shown in Fig. 12, in which we can identify two independent signal generators used because of the very different powers addressed for each specific signal.

Moreover, it is important to focus that great care should be taken on the signals generation in order to ensure a clean as possible multi-carrier signal at each architecture input.

The obtained measured results for the two evaluated architectures are shown in Fig. 13, wherein the achieved simulation performance is also plotted. Analyzing the figure we can observe that the obtained measurement results replicate very well the ones obtained in the simulations with just a bit degraded performance.

These deteriorated results are mainly because of higher laboratory instrument noise levels and non-ideal performance of ADCs not considered in the developed simulation models, likewise sampling clock jitter and small time misalignments between paths that adds phase mismatch and thus, further degrades the overall SNR.

Fig. 14 illustrates the constellation diagrams for the low-power QPSK signal measured for each architecture at different input powers, confirming the better performance of the proposed architecture compared to a VGA plus ADC design.

In general the conjunction of obtained results verifies the proper operation of the proposed architecture for dynamic range improvement under realistic signal environments.

VI. Conclusion

In this paper a novel architecture for instantaneous dynamic range is proposed and explained. By the use of this technique substantial improvements can be achieved when in rough scenarios, such as under strong interferences and multi-carrier operation, which are very common to SDR and CR environments.

The performance of the proposed architecture was compared to other designs by several simulation experiments and a measurement example.

It was proved that in the worst case, the proposed solution can present an increase of near 1-bit of resolution in conventional receivers. Moreover in real CR scenarios, where multi-carrier and multiband operation is the limiting factor due to dynamic range constraints, this technique can improve significantly the operation of the RF front ends.

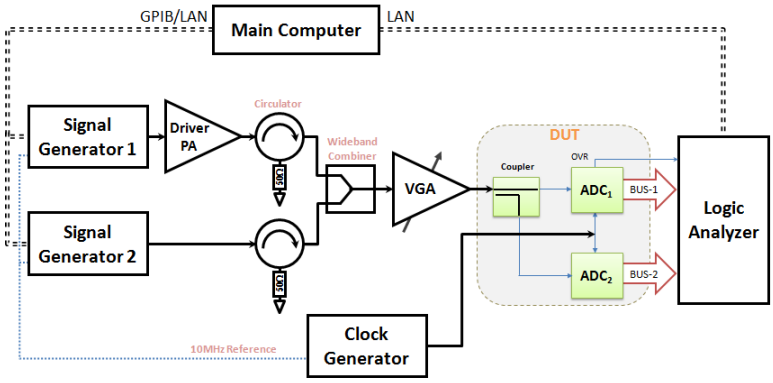

Fig. 12 – Laboratory setup used in the measurement validation example.

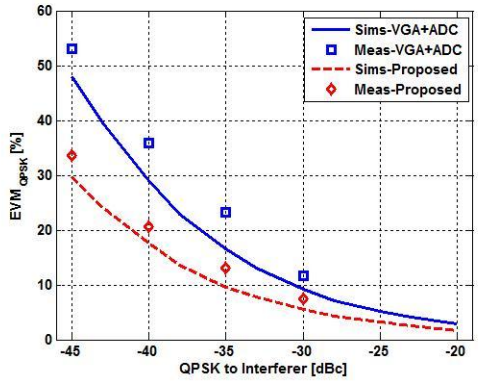

Fig. 13 – Measured EVM values of a low-power QPSK signal being received simultaneously with a high-power interferer for the VGA plus ADC and proposed cases.

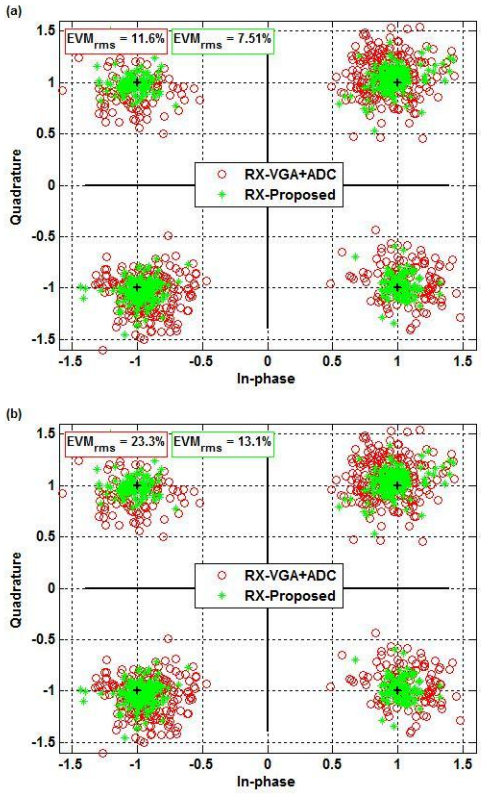

Fig. 14 – Constellation diagrams of the low-power QPSK signal for the VGA plus ADC and proposed architectures, when received at (a) -30dBc and (b) -35dBc to the interferer.

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Mr. Cruz was a finalist in the student paper competition of the IEEE MTT-S International Microwave Symposium 2008. He was recognized with the 3rd place in the GAAS Association PhD Student Fellowship for EuMIC 2009.

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He is a reviewer and author of more than 100 papers in several magazines and conferences and the chair of the IEEE MTT-11 Technical Committee and the chair of the URSI-Portugal Metrology group. Dr. Borges Carvalho is co-author of the book "Intermodulation Distortion in Microwave and Wireless Circuits" from Artech House, 2003.

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[C1] – PWM Bandwidth and Wireless System Peak-to-Minimum Power Ratio

Pedro M. Cruz and Nuno B. Carvalho

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PWM Bandwidth and Wireless System Peak-to-Minimum Power Ratio

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***Abstract*— This paper presents a relationship between peak-to-minimum power ratio, PMPR, and pulse-width-modulation, PWM, bandwidth, i.e., the digital PWM sampling frequency.**

It will be shown that in PWM modulators most important than PAPR is the PMPR figure of merit, since the required modulation bandwidth changes with this relationship considerably. Moreover a closed analysis will be done for well known modulated waveforms.

Furthermore, an H-bridge class-S modulator will be implemented in order to depict the impact of the different PWM waveform rates in its efficiency.

I. Introduction

Software-Defined-Radio (SDRs) will be the future of radio configurations, and the all digital transceivers are becoming a great source of innovative work either at Universities or Industry.

This all digital approach is important not only due to the implementation of novel SDR configurations, that will drove the radios to cognitive approaches, but also due to green environments since they will allow the use of very high efficiency transmitters, like for instance class-S power amplifiers, PA. Fig. 1 presents an example of one of these transmitters.

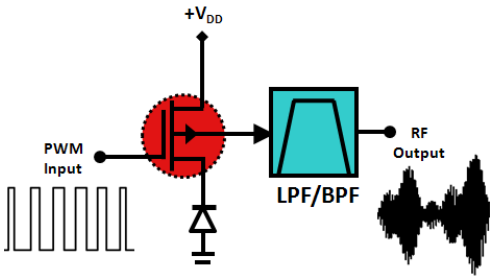

Fig. 1 – Simplified Circuit of a Class-S Power Amplifier.

As can be seen from the figure, the class-S amplifier [1] can be a pure switching amplifier followed by a low-pass filter (to create an envelope signal) or a band-pass filter (to create an RF modulated signal). Ideally, this amplifier will consume no DC power since the output voltage and the current are equal to zero alternatively and in that sense the achieved efficiency will be 100% (ideal case). In fact, it will consume some power in the signal transitions because in real devices some parasitic capacitances and interconnections components will produce some losses, and finite switching times.

The input pulse width modulated, PWM, signal of the class-S amplifier can be generated by the digital signal processor, DSP, eliminating the need for a wideband DAC and hence potentially saving costs.

Unfortunately, and if one look at the real world configurations it is not possible, yet, to design a high efficiency class-S amplifier to operate at very high frequencies. Nevertheless, some contributions are appearing in that field [2]. Similar approaches are being tried also with sigma delta modulators in order to have better signal-to-noise ratios [3].

Due to that, switching amplifiers are been used massively in new configurations based on envelope elimination and restoration (EER) or "polar" techniques [4, 5], in which the required bandwidth is much smaller allowing the design of high-efficient class-S amplifiers, Fig. 2.

If we look at circuit of Fig. 2 the class-S amplifier only has to deal with the envelope of the input signal which will vary the bias voltage, $V_{DD}(t)$, of the RF high power amplifier. In the phase path a constant-envelope phase modulated baseband/IF signal is generated in the DSP and then up-converted to RF and applied to the RF PA.

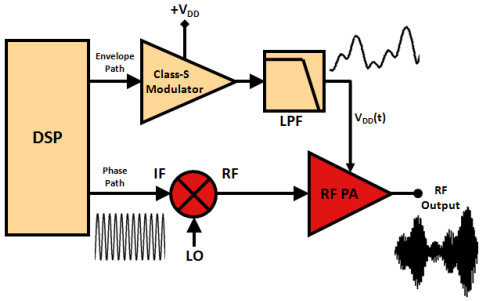

Fig. 2 – "Polar" Transmitter Circuit.

Nevertheless the SDR community is putting all efforts in this green path, by moving the concepts from analog to digital approaches, and thus the demands of the switching speed of RF PA are becoming more evident and more stringent.

Moreover the use of higher complex modulated waveforms, and in the future, of extremely higher complex waveforms, (as we expect to use in cognitive radios), will impose values of peak-to-average power ratio, PAPR, that are not available today, imposing sever restrictions to the electronics that should dealt with these new approaches.

In this paper we will address exactly this problem, by first revisit the concept and the need of using a new figure of merit for signal characterization called the peak-to-minimum power ratio, PMPR. Then, in section III, a relationship between the PMPR value and the pulse-width-modulator sampling frequency will be depicted. This will be followed by some simulation examples of the use of proposed formulation, in which is included an implementation of an H-bridge class-S modulator. Finally, some conclusions will be drawn.

II. Peak-to-Minimum Power Ratio Concept

The increase in bit-rate needs is pushing the modulation formats to a higher level of complexity, with 64- to 256-QAM been a usually used standard for wireless communications.

Moreover, the need for mobility and transmission rate is also imposing the use of OFDM with bandwidths so high as 70MHz for wireless communications case of LTE-Advanced, [6].

Due to this, the PAPR is increasing continuously, and thus degrading the dynamic range of ADC/DAC's and also forcing nonlinear behaviors in the power amplifier, PA.

PAPR can be defined as the relationship between peak power and average power, equation (1).

$$PAPR = \frac{\max_{0 \le t \le NT} |x(t)|^2}{1/NT \int_0^{NT} |x(t)|^2 \, dt} \quad (1)$$

On top of this the goal to achieve high efficiency and all digital transceivers, mainly due to the potential capabilities of SDR, are imposing new strategies for RF designs, mainly for the transmitter part of the SDR front-end.

One of those visionary solutions is to use pulse-width-modulation based in sigma-delta modulation or PWM techniques to create the so called all-digital transmitter [3, 7].

This approach is been pushed either at RF, which is a visionary solution at the moment, due to the fact that the frequency of operation is extremely high for a correct functioning of the amplifier, at least until the commutation speeds, of the class-D amplifier are not increased, or at the envelope frequency where the PWM is been used as a bias modulator to construct a high efficiency transmitter.

Nevertheless, PWM modulator bandwidth changes much with the level of quantization that is needed to represent quantitatively the input signal, which in this case is the signal to be transmitted.

The level of quantization, i.e., the PWM resolution increases as much as the relationship between the minimum and maximum value of the input signal swing varies. So, the typical PAPR is no longer the key figure of merit, but the relationship between the maximum and minimum starts to be a key figure of merit in complex signal characterization, as was stated previously by other authors [8].

Thus we can recall a new figure of merit called the peak-to-minimum power ratio, as:

$$PMPR = \frac{\max_{0 \le t \le NT} |x(t)|^2}{\min_{0 \le t \le NT} |x(t)|^2} \quad (2)$$

where $x(t)$ is the input signal and NT is the number of samples considered in the evaluation.

Thus, it is expected that for future PWM based power amplifiers, as class-S and so on, the figure of merit PMPR is a much interesting and useful quantity.

III. Relationship between PMPR and PWM Bandwidth

As was stated in the previous section the PMPR is a figure of merit that imposes a strong drawback on PWM modulators, this drawback is due to the relationship between PMPR and bandwidth needs, since a higher value of PMPR imposes a low value of quantization resolution, and thus of smaller PWM duty-cycles, which demands for increasing sampling frequencies. Thus the problem that we should resolve is on how much bandwidth we need for a specified PMPR.

In order to start this discussion, let us consider a constant envelope modulated signal as the case of a GSM signal. In this case if we want to modulate the RF signal with a PWM, the need for bandwidth mainly depends on the frequency of the RF carrier, and should be equal to more than the double of the Nyquist frequency, on the other hand if we want to modulate the envelope, then a single value is needed, so the PWM only have to characterize a constant DC value.

Nevertheless, if the signal presents a certain non-constant envelope, then the PWM modulator should start to consider a certain value of bandwidth that corresponds to the quantization resolution that we expect from the modulator.

This has driven the authors to propose a relationship between PMPR and PWM sampling frequency.

For instance, considering a non-constant envelope signal we can define that the reference voltage of the PWM (V_{REF}) should be equal to the maximum amplitude of the signal and the minimum should be represented by the ratio between the reference voltage and the respective available quantization levels (2^N) that is dependent on the number of bits (N).

Thus, knowing the PMPR value one can determine the minimum voltage levels that are able to represent this amplitude variation, equation (3).

$$PMPR = 10 * \log_{10}\left(\frac{|A_{max}|^2}{|A_{min}|^2}\right) = 10 * \log_{10}\left(\frac{|V_{REF}|^2}{\left|V_{REF}/2^N\right|^2}\right)$$

$$\Leftrightarrow PMPR = 20 * \log_{10}(2^N) \quad (3)$$

So, extracting from equation (3) the relationship between the maximum and the minimum amplitudes, we obtain:

$$\frac{A_{max}}{A_{min}} = 2^N = ceil\left(10^{\left(\frac{PMPR}{20}\right)}\right) \quad (4)$$

where ceil(.) represents the ceiling function.

In order to represent 2^N voltage levels in a PWM waveform one need, at least, a pulse width modulator that can provide at the output 2^N-1 different duty-cycles.

Finally, the PWM sampling frequency is obtained using equation (5).

$$f_{S,PWM} = f_{S,signal} * (2^N - 1) \quad (5)$$

So, it is clear that a higher value of the PMPR value imposes an increase in the required PWM sampling frequency. Next section will address this issue and present some simulation results that demonstrate this fact.

IV. Obtained Results for Typical Wireless Signals

In order to evaluate the concept described in last section, we have generated (using an R&S generator) several signals of well known wireless standards, as GSM, EDGE, W-CDMA and WiMAX.

Then, we extract the envelope of each signal and applied it to a digital PWM modulator that could be designed in a DSP. Table 1 present the main characteristics of the generated signals, as well as the oversampling ratio (OSR) that is required in the PWM modulator based in the previous proposed formulation. Fig. 3 shows the measured probability density function (PDF) of the envelope signals used.

TABLE I
Characteristics of the Generated Signals

Signal Type	PAPR [dB]	PMPR [dB]	PWM OSR	Modulation
GSM	0.03	0.07	1	GMSK
EDGE	3.52	15.54	5	8-PSK
WCDMA	4.01	29.52	29	π/4-QPSK
WiMAX	7.90	39.61	95	64-QAM

As can be seen from Fig. 3 the PDF of the each signal is significantly different. The envelope of the GSM signal is a constant value as we expected near 1 which is the normalized value for a constant envelope.

Since the other signals have a non-constant envelope, the relationship between the maximum and minimum value depends of the statistical distribution of each of them.

The WCDMA envelope signal presents an almost Gaussian behavior as expected and the WiMAX signal presents a different statistic that imposes the worst PMPR of them all, as was previously seen in Table 1. A curious PDF behavior can be seen in the EDGE signal, and it can be due to the type of modulation used.

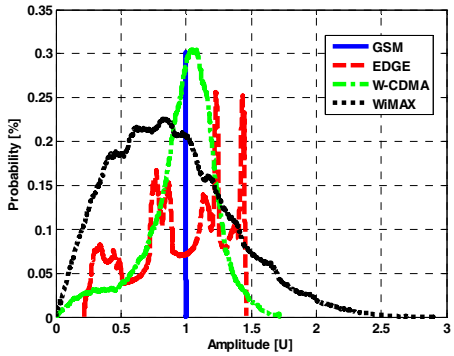

Fig. 3 – Measured statistics (PDF) of the signals used in the simulations.

Taking into account the provided values in Table 1 and using the equations (4) and (5) we can extrapolate the required sampling frequency (considering the PWM oversampling ratio) for the digital pulse-width-modulator.

We should be aware that these values are ideal, and we can select a smaller value if we can live with reduced SNR in the final recovered envelope signal.

As can be seen from Fig. 4, the error difference between the original envelope signal and the reconstructed envelope with the filtered (using a 4th-order Butterworth filter) PWM waveform was calculated when the sampling frequency of the PWM modulator is varied.

The error in GSM signal doesn't changes as was expected by its constant envelope with a value of one for the PWM oversampling ratio (OSR) presented in Table 1.

Regarding the other signals we can observe a reduction in this error with the increase of the PWM sampling frequency, till a limit of around -33dB for WCDMA and -34dB for WiMAX case, and a limit of -41dB for the EDGE signal.

The magenta squares represents the values required for the PWM oversampling ratio based on the formulation proposed in last section. As can be seen, the determined PWM OSR are enough to not cause a noticeable error between the original envelope and the reconstructed envelope. The reduced error of the GSM signal is due to the fact that it is a constant-envelope signal and the high value for the EDGE signal we believe that is due to the not common presented PDF.

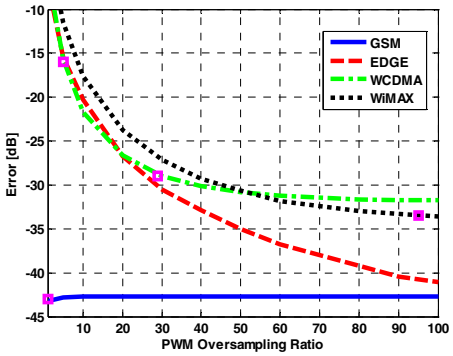

Fig. 4 – Simulated error between original envelope and reconstructed envelope of the PWM modulator.

V. Impact of PWM Signal on Class-S Modulator

Looking at Fig. 2, can be seen a class-S modulator employed in the envelope path. In order to evaluate the impact of different PWM waveform on the class-S amplifier, we have implemented a complementary voltage-switching H-bridge circuit that is shown in Fig. 5, [9]. This implementation was done in Agilent Advanced Design System (ADS) and we have used ADS models of a GaAs FET and a diode.

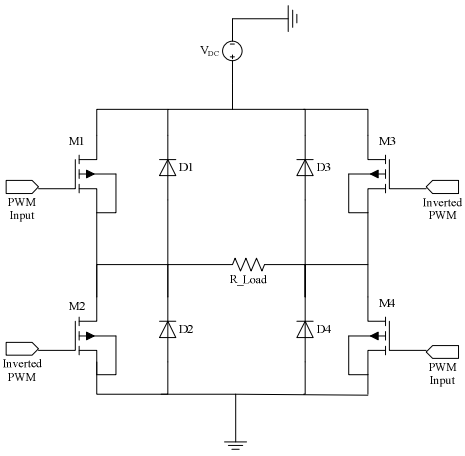

Fig. 5 – Circuit of an H-Bridge Class-S amplifier.

Regarding the circuit of Fig. 5 two complementary pulse voltage signals are driving the four FETs (M1 through M4). At any rising edge of the input signal (PWM Input), FETs M1 and M4 are turned on, while M2 and M3 are turned off. After a transient time, the amplifier output voltage is the DC supply voltage (V_{DC}) less the voltage drop across M1 and M4 in the triode region. The circuit stays in this state until the next rising edge of the second input signal arrives (Inverted PWM). Once this arrives, the circuit will change into another state and now M2 and M3 are turned on. In these two states the DC source power is converted to the RF load power by the current flowing through, either in M1 and M4 or M2 and M3.

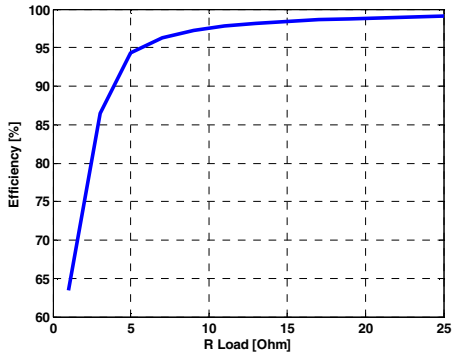

Fig. 6 – Simulated efficiency of the H-bridge amplifier for different load conditions.

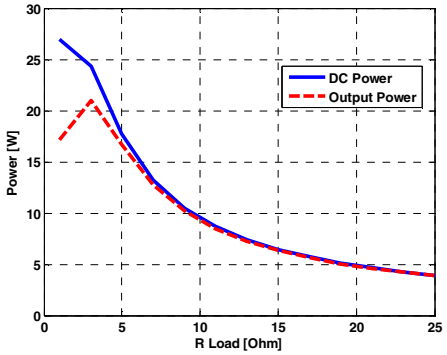

Fig. 7 – Simulated DC power consumption and output power of the H-bridge amplifier for different load conditions.

The performance of the H-bridge switching mode amplifier was observed for different load conditions. Looking at Figs. 6 and 7, we can observe that a load resistance of around 9Ω is a good compromise between output power and efficiency.

After that the previous PWM waveforms were applied to the H-bridge amplifier and the obtained results are shown in Table 2.

TABLE II
SIMULATED RESULTS FOR EACH PWM WAVEFORM

Signal Type	Output Power [W]	DC Power [W]	Efficiency [%]
GSM	10.213	10.501	97.257
EDGE	6.263	10.343	60.553
WCDMA	6.135	10.453	58.691
WiMAX	4.489	10.398	43.167

One can be leaded to think that if we design a high-efficiency envelope modulator it could work with that efficiency for various envelope signals, but this may be not true.

Regarding the presented results in Table 2, it is obvious that only constant envelope signals could work with almost 100% efficiency, as in the case of the GSM signal. However, with the introduction of new modulation formats and with the increase in the used bandwidth, the necessary sampling frequency also increases. When we try to modulate these envelope signals with a PWM modulator this sampling frequency will increase even more in the case that present high PMPR values, as was seen in the other simulated signals where the efficiency of the class-S modulator reduces with the increase in the required PWM sampling frequency.

VI. CONCLUSION

In this paper we recall the concept of PMPR to depict a new relationship between this value and the required bandwidth of a PWM modulating signal. We have made a direct relationship between these two important measures.

The results showed that as high the PMPR is, the higher is the value of PWM sampling frequency.

We should recall that the presented values are ideal, and that a reduction on bandwidth constraints can derive in reduced SNR at the output.

Moreover, as was mentioned above some approaches with sigma-delta modulation techniques, instead of PWM, are being addressed due to the reduced number of transitions produced that will lead to lower power consumptions.

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[C2] – Modeling Band-Pass Sampling Receivers Nonlinear Behavior in Different Nyquist Zones

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Modeling Band-Pass Sampling Receivers Nonlinear Behavior in Different Nyquist Zones

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***Abstract*— This paper presents a comprehensive behavioral model of a band-pass sampling receiver working throughout its input bandwidth. The key component of such architecture is the analog-to-digital converter, ADC, in which its input spectrum is normally divided in different Nyquist zones. Such a topology is appointed to be part of future demanding radio receivers for cognitive radio applications and spectrum sensing.**

An efficient model parameter extraction procedure will be addressed in order to obtain the required parameters for the proposed model when in presence of a huge amount of noise.

Furthermore, the presented behavioral model will be validated using real modulated signal excitations applied in different Nyquist zones of the used band-pass sampling receiver.

I. Introduction

Band-pass sampling receivers are one of the proposed architectures for future cognitive radio approaches.

In this paper some behavioral models for this type of architectures will be presented based on the Volterra series description. With these models RF engineers would be more supported in their designs and give rise to better radio solutions.

Actually we are facing an enormous development in the software-defined radio, SDR, field where a considerable number of solutions are being suggested. As was declared in [1] the ultimate goal for SDR architecture is to push the digitization as much as possible close to antenna. Nevertheless, the current ADC technology does not demonstrate the mature that is requested in such a solution. Additionally, the step up concept of cognitive radio, CR, also proposed by Mitola [2] will demand for a huge receiving spectral bandwidth combined with very different power levels, i.e., high dynamic ranges. By its very definition, a CR is a radio that is able to automatically adapt itself to the air interface by optimizing the carrier frequency, modulation, and choice of radio standard to minimize interference and maintain communication in a given scenario. In order to be able to implement this ideal solution, the radio should "see" and be aware of the entire spectrum and of the communications being used at a specific time and thus, be able to perform the wireless environment sensing.

In that way, these CR approaches will be definitely based in the SDR architectures that are being evaluated at this moment by the scientific community. As was summarized in [3] there are a reduced number of solutions to construct the referred spectrum sensing capable SDR radio. One of those is the band-pass sampling receiver [4, 5], BPSR, which due to the constant advancements achieved in the ADC technology is becoming a much more feasible and practical solution, Fig. 1.

The key component of this architecture is the pipeline ADC that normally contains a sample-and-hold (S/H) circuit, which in theory will down convert the incoming signal as a mixer module, followed by the quantizing scheme based on a pipeline approach, [6].

Nevertheless the simulation of such a huge and complex architecture is quite computer intensive, mainly when the objective is to simulate a RF signals modulated with high bandwidth signals.

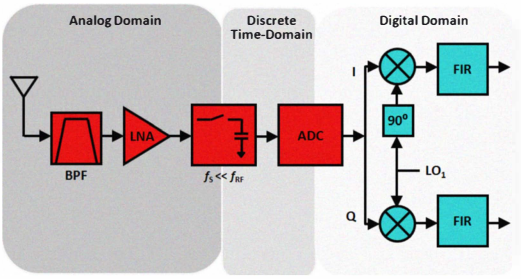

Fig. 1 – Band-pass sampling receiver architecture.

Thus the motivation of this paper is to propose a new behavioral model for a BPSR covering the RF and the base-band frequency responses.

Taking the properties of the sub-sampling phenomena that occurs in pipeline ADC's, several Nyquist zones, NZ, will be created and folded back to the first NZ.

The model should mimic either the linear operation, but also its non-ideal behaviors as the nonlinear effects but also noise arising from ADC quantization as well as jitter in the clock signal [3].

Thus, a model that is able to characterize the device in terms of nonlinear distortion, extra noise, for different NZ's is very welcome and appropriate.

In order to achieve such goal the paper is organized in the following way; firstly some introductory concepts about the BPSR architecture are given.

Then, in section III, a suitable behavioral model will be presented as well as the respective parameter extraction procedure. In section IV, we will illustrate and validate the addressed behavioral model for different NZ's operation of the BPSR using a common wireless signal as excitation. Finally, some conclusions will be drawn summarizing the obtained results.

II. Receiver Operation in Different Nyquist Zones

The first step in order to understand the complexity of these new schemes will be to study and understand the theory and proposed approaches behind the BPSR.

In BPSR [4, 5], Fig. 1, the incoming signal is filtered by an RF band-pass filter that can be a tunable filter or a bank of filters, and then it is amplified using a wideband LNA.

The signal is then converted to the digital domain by a high sampling rate ADC and digitally processed. Here we can take advantage of digital signal processing to alleviate some mismatches of the analog front-end.

Moreover, this architecture is a close approximation to the initial ideal of Mitola [1] for an ideal SDR radio because it pushes the ADC closer to the antenna and in that sense provides an increased flexibility.

Nevertheless, the ADC typically presents sampling rates lower than the RF signal bandwidth, so the BPSR presents an approach which allows that all energy from DC to the input analog bandwidth of the ADC will be folded back to the first NZ [0, f_S/2]. This process occurs without any mixing down-

conversion needed because a sampling circuit is replacing the mixer module. Actually this is one of the most interesting components of this architecture, because is due to it that an RF signal of a higher frequency can be sampled by a much lower clock frequency. This process can be observed in Fig. 2, for a two-tone input signal accompanied by the respective nonlinearities till the 3rd-order.

As can be seen the third-harmonics generated in the nonlinear device and that fall in the second NZ were folded back in an inverted way and fall very close the desired 2-tone input signal. It is possible to pinpoint the resulting folded frequencies, f_{fold}, based on the following relationship, [7]:

$$if \quad fix\left(\frac{f_C}{f_S/2}\right) \quad is \quad \begin{cases} even, & f_{fold} = rem(f_C, f_S) \\ odd, & f_{fold} = f_S - rem(f_C, f_S) \end{cases} \qquad (1)$$

where f_C is the carrier frequency, f_S is the sampling frequency, *fix(a)* is the truncated portion of argument *a*, and *rem*(*a*,*b*) is the remainder after division of *a* by *b*.

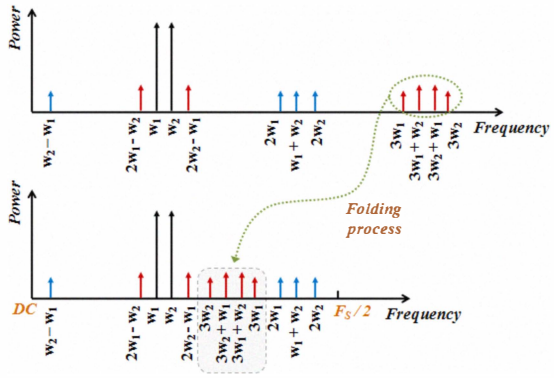

Fig. 2 – Process of folding that occurs in the sample-and-hold circuit.

Then, in order to better understand the operation of the explained BPSR in different NZ's, we have implemented a BPSR, Fig. 1, using laboratory components and also develop an experimental setup to characterize it.

We used several band-pass filters (BPF) to select the desired NZ to be modeled, in this case, two different NZ's were tested. This was followed by a commercially available wideband LNA (0.5 – 1000 MHz) with a 1-dB compression point of +9 dBm, an approximate gain of 24 dB, and a noise figure of nearly 6 dB. We used a commercially available 12-bit pipeline ADC that has a linear input range of approximately +10 dBm with an analog input bandwidth of 750 MHz and sampled with a clock frequency of 90 MHz. The setup used to characterize the device-under-test, DUT, is presented in Fig. 3 and is based in the test bench proposed in [8].

Considering the referred clock frequency at the output of the DUT we will have several NZ's of 45 MHz (f_s/2) of bandwidth for each one. In that sense we choose the carrier frequencies to be used of 11.5 MHz for the 1st NZ and 69 MHz for the 2nd NZ. Thus, as we plan to utilize a model truncated at third-order nonlinearity, for the first excitation frequency and taking into account the frequency folding phenomena, the fundamental and respective harmonics will fall in the 1st NZ. Nevertheless, the same will not happen for the second excitation frequency, since the fundamental and 2nd harmonics will fall in the 2nd and 4th NZ's, respectively, and are folded back in an reversed way, using equation (1). Regarding the 3rd harmonics they will fall in the 5th NZ and are folded back in the upright mode. In that sense, a great care should be taken when choosing the excitation frequencies for the behavioral model extraction.

It is also important to refer that all the measurements were done using excitation frequencies accordingly to the coherent sampling, in order to reduce any spectral leakage that could appear.

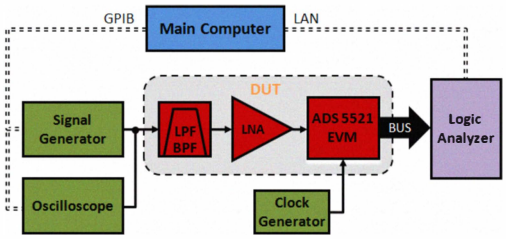

Fig. 3 – The Experimental Test Bench.

III. Behavioral Model and Parameter Extraction

This section is devoted to explain the behavioral model scheme proposed for the addressed architecture and the respective parameter extraction procedure.

Regarding that the objective is to compare the analog signal sampled at the input of the DUT with the respective digital output signal in order to extract a behavioral model, we have passed the measured output digital levels through an ideal digital-to-analog converter, expression (2), with the same number of bits (N) and same reference voltage (V_{REF}) of the used ADC.

$$V_{out} = V_{REF} * \sum_{i=1}^{N} \frac{b_i}{2^i} \qquad (2)$$

This procedure will create an equivalent output signal waveform that can be directly compared with the measured input signal. Then, in order to find a behavioral model to match this input and output measurements we have considered the Volterra series [9] approach. A Volterra series is a combination of linear convolution and a nonlinear power series that provides a general way to model a nonlinear system with memory. In that sense, it can be employed to describe the relationship between the input and output of the entire BPSR presenting nonlinearities and memory effects. This relationship can be written as,

$$y(t) = \sum_{n=0}^{\infty} \int_{-\infty}^{\infty} \cdots \int_{-\infty}^{\infty} h_n(\tau_1, \cdots, \tau_n) x_{in}(t-\tau_1) \cdots x_{in}(t-\tau_n) d\tau_1 \cdots d\tau_n \qquad (3)$$

where $x_{in}(t)$ and $y(t)$ are the input and output signal waveforms, respectively, and $h_n(\tau_1,\ldots,\tau_n)$ is the n^{th} order Volterra kernel.

Actually, we assumed that our Volterra series model will be truncated to the third-order nonlinearity and consider a single tap memory length to characterize the short-term memory effects, this was observed to be enough for our analysis. The chosen excitation that was selected for the parameters extraction is a multisine that should approximate the statistical behaviour of the environment where this device will be applied.

However, we observed that the measured output signals are highly corrupted by noise, which will made the parameter extraction impractical or providing misleading results.

Thus, we have pursued a new approach that consists in the following steps:

1. Apply a Fourier transform (FFT) to the input and output signals.
2. Select only the desired frequency bins [10] taking into account the nonlinearity order considered and construct a new signal with the selected frequency components.

3. Determine the gain of the entire BPSR considering only the fundamental signal frequency bins, which corresponds to calculate the underlying linear gain.
4. Afterwards, apply an inverse Fourier transform (IFFT) in order to obtain a cleaner (without undesired frequency components and noise) time-domain signal.
5. Apply a Volterra series model, expression (3), to these new input and output signals and obtain the desired Volterra kernels.

Moreover, taking advantage of this procedure we can also determine in the frequency-domain an error signal that will afterwards be added to the modeled output signal as an amount of additive Gaussian noise. In our case it includes noise coming from ADC quantization, clock timing jitter and thermal noise from LNA.

Thus, considering that the input signal, $x_{in}(t)$, is sufficiently rich, i.e., one that presents a high variability and that the output of the Volterra series model is linear with respect to its parameters the time-domain Volterra kernels can be determined using a least-squares technique, expressed by

$$\mathrm{H} = (\mathbf{X}^T\mathbf{X})^{-1}\mathbf{X}^T\mathrm{Y} \quad (4)$$

where $\mathbf{X}$ and Y are the input signal matrix and output signal vector, respectively, and H is the vector of kernels that we are looking for. This model is based on mixed time-frequency domain obtained signals. Actually, $\mathbf{X}$ the input signal matrix in the time-domain is obtained as:

$$\mathbf{X} = \begin{bmatrix} x(0) & \dots & x(0)x(0) & \dots & x(Q)x(Q)x(Q) \\ \vdots & & \vdots & & \\ x(N) & \dots & x(N)x(N) & \dots & x(N-Q)x(N-Q)x(N-Q) \end{bmatrix} \quad (5)$$

and Y the output signal matrix in time-domain is obtained as:

$$\mathrm{Y} = [y(0) \quad \dots \quad y(N)]^T \quad (6)$$

where Q represents the memory length and N is the number of samples of the input signal.

Thus, H can be then calculated using (4). This result has the advantage of notational simplicity and general applicability. H is actually composed by the following kernels:

$$\mathrm{H} = [h_1(0) \;\; h_1(Q) \;\; h_2(0,0) \;\; h_2(0,Q) \;\; \dots \;\; h_3(Q,Q,Q)]^T \quad (7)$$

As regard to the richness of the signal excitation we decide to excite the BPSR with a multisine signal with 11-tones with random phases that creates a peak-to-average power ratio, PAPR, of around 3.5 dB and a bandwidth of 1 MHz.

As was seen above we must have a great care in the procedure of choosing the carrier frequencies, signal bandwidth, etc. due to folding process that happens in this DUT, because we do not want, at least, till the 3rd-order nonlinearity that the signal fall in overlapping frequency bins where this model extraction will no longer be valid.

Finally, we apply the behavioral model proposed to the input and output measurements, extract the required parameters and compared the measured signals with the simulated ones using our behavioral model. The main obtained results are shown in Figs. 4 and 5 for the two different NZ's evaluated.

Looking at figures we can roughly say that the behavioral model and the described parameters extraction is estimating well the unknown parameters and producing very similar results for the two different NZ's excited. Other commonly used measure to characterize the performance of models is the normalized mean squared error [11], NMSE, and in this case we have obtained -31.80 dB and -29.49 dB for the 1st and 2nd NZ's, respectively. Also, the AM/AM curves (Figs. 4 and 5) confirms the assumptions about the validity of the behavioral model. It is also interesting to see from the AM/AM curves that the 2nd NZ presents more memory than the 1st NZ.

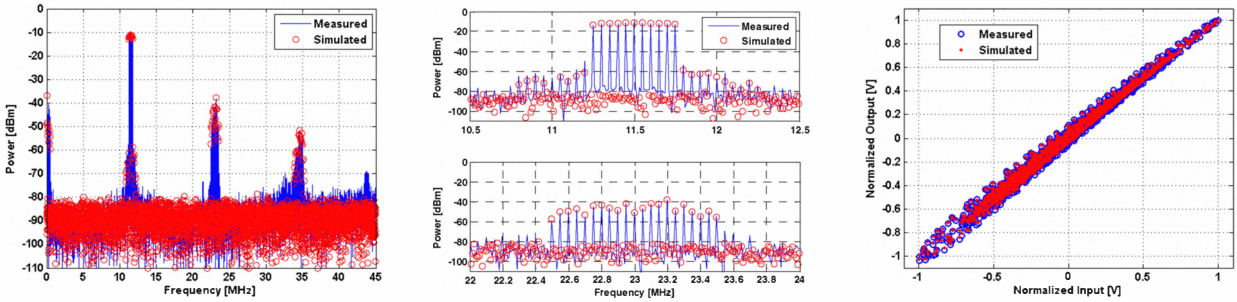

Fig. 4 – Measured and simulated results for the multisine excitation centered at 11.5 MHz (1st Nyquist zone): a) entire subsample bandwidth, b) carrier band and 2nd harmonic band, and c) AM/AM characteristic.

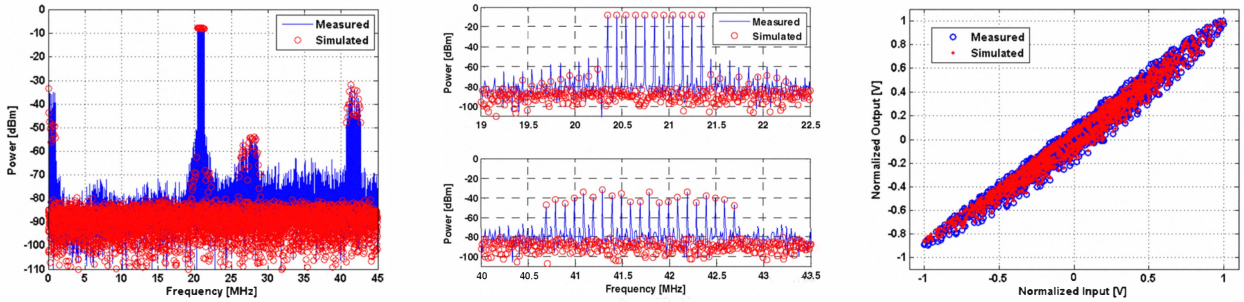

Fig. 5 – Measured and simulated results for the multisine excitation centered at 69 MHz (2nd Nyquist zone): a) entire subsample bandwidth, b) carrier band and 2nd harmonic band, and c) AM/AM characteristic.

IV. Validation Results

In order to corroborate the validity of the proposed model for a BPSR we have applied an RF quadrature-phase-shift-keying, QPSK, modulated signal with a bandwidth of 1 MHz, which present a PAPR of approximately 4.2 dB. We have used the same carrier frequencies as in the extraction procedure and also maintain the experimental test bench. After that, we compared the measured output results with the achieved by the proposed model, shown in Figs. 6 and 7.

Analyzing these figures we can again affirm that the behavioral model produces very good results for the two NZ's

signals, approximating well the fundamental signal, second and third harmonics, and lower and upper adjacent channels power. The base-band is not as good approximated, due probably to a bad selection of the type of memory we expect to gather with this model, mainly short-term memory.

Moreover, we can actually see an increase in the noise floor from one NZ to another, wherein our model also accompanies this behavior.

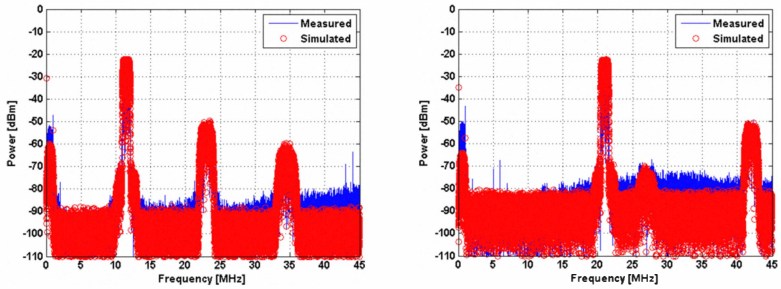

Fig. 6 – Entire spectrum bandwidth of measured and simulated outputs for a QPSK signal centered at 11.5 MHz (left) and 69 MHz (right).

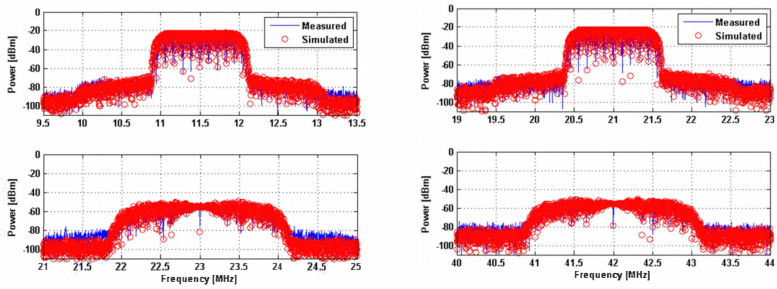

Fig. 7 – Spectrum of measured and simulated, carrier band and 2nd harmonic band for a QPSK signal at 11.5 MHz (left) and 69 MHz (right).

We have also expressed the modeling error in terms of integrated power in the fundamental, adjacent lower and upper channels, and 2nd and 3rd harmonics. These results are shown in Table I for the excitation in the 1st NZ and in Table II for the 2nd NZ. Observing the results we can state again that our model is approximating very well the behavior of the addressed BPSR in its entire bandwidth.

TABLE I
MEASURED AND SIMULATED OUTPUT POWERS FOR QPSK SIGNAL AT 11.5MHZ

	Carrier	ACP Low	ACP High	2nd Harmonic	3rd Harmonic
Meas. [dBm]	1.67	-49.44	-51.27	-27.90	-38.59
Model [dBm]	1.55	-51.80	-50.78	-27.05	-37.72

TABLE II
MEASURED AND SIMULATED OUTPUT POWERS FOR QPSK SIGNAL AT 69MHZ

	Carrier	ACP Low	ACP High	2nd Harmonic	3rd Harmonic
Meas. [dBm]	2.05	-50.88	-50.68	-26.69	-45.39
Model [dBm]	1.52	-49.38	-49.74	-27.65	-48.32

V. CONCLUSIONS

In this paper we have proposed and analyzed a new behavioral model for a BPSR when excited in two different NZ's. Since this model is based in input/output measurements and the parameter extraction is easy to implement for the nonlinear orders and memory lengths used here, it can be practically extended to higher orders.

We have also proposed a new approach to overcome with the noisy measurements using for that a mixed mode frequency-time strategy.

The model was also validated by a commonly used wireless modulated signal that confirms the functionality of the model and parameter extraction procedure.

It should also be stressed that this model is suitable for large bandwidth applications as was shown.

ACKNOWLEDGEMENT

We would like to acknowledge the financial support of this work within the project TACCS - Cognitive Radios Adaptable Wireless Transceivers, PTDC/EEA-TEL/099646/2008, and the FCT PhD grant (SFRH/BD/61527/2009) of the first author.

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[C3] – Multi-Carrier Wideband Nonlinear Behavioral Modeling for Cognitive Radio Receivers

Pedro M. Cruz and Nuno B. Carvalho

European Microwave Integrated Circuits Conference, Manchester, UK, pp. 414-417, Oct. 2011

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Multi-Carrier Wideband Nonlinear Behavioral Modeling for Cognitive Radio Receivers

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***Abstract*—This paper proposes a new multi-carrier wideband behavioral model scheme devoted to represent the non-ideal operation of multi-carrier nonlinear devices. This model is able to describe the operation under multi-carrier excitation of a nonlinear device, either the in-band but also the cross-modulation distortion between the input carriers.**

The proposed design is based on the Volterra series model and is able to attribute varying memory lengths to the different nonlinear clusters. In addition, a parameter extraction procedure that works in parallel for the several nonlinear clusters produced by the nonlinear device will be described.

Moreover, the presented wideband behavioral model will be validated using two multisine signals with different bandwidths when traversing a wideband nonlinear device, representing a cognitive radio receiver.

***Keywords*—Wideband behavioral modeling, multi-carrier, nonlinear systems, parameter extraction, software-defined radio.**

I. Introduction

Software-defined radios (SDR) are set to pave the way for the next generation of wideband communications. Due to the constant advent of new wireless communications standards, like the Universal Mobile Telecommunication System (UMTS), Worldwide Interoperability for Microwave Access (WiMAX), 3GPP Long Term Evolution (LTE), and so on, several issues have raised mainly by the difficulty of integration of those standards into a single radio device.

The appearance and recent development of SDR and cognitive radio (CR) technology will most probably overcome that issues and allow the implementation of a universal radio. As was stated by Mitola in [1] an SDR should be capable to digitally processing the received signals, which let the radio to be reconfigurable. Another important competence is the capability to operate in multi-mode and multi-standard scenarios that will demand for very wideband radio front ends, i.e., the radio architecture should be capable to operate under multi-carrier excitations, especially the wireless spectrum sensing radio stage of a CR approach.

The concept of CR also coined by Mitola in [2] will be certainly based in the SDR architectures, in which it should adapt itself to the transmission scenario by gathering information about all of the signals that are present in the air interface automatically.

Obviously, these assumptions will lead to a significant increase in the design complexity of the receiving and transmitting stages.

In that sense, modeling schemes for the components used in the radio front ends should also accompany those assumptions in order to allow wireless system design engineers to efficiently simulate their designs and give rise to better radio solutions. Therefore, these models are required to predict the operation over a very wide bandwidth and also to account for multi-carrier signal excitations.

Related to this subject, Gharaibeh and Steer [3, 4] have addressed the transmitter side multi-carrier nonlinear operation of power amplifiers based on a generalized statistical analysis.

Recently in [5] and later in [6] a wideband behavioral model for bandpass sampling receivers covering the RF and baseband frequency responses has been presented, which captures different memory effects, but it was only demonstrated for a single-carrier excitation.

Thus, the main goal of this paper is to propose a general behavioral model based on Volterra series for nonlinear devices, which is able to cover intermodulation and cross-modulation distortion mechanisms that appears in multi-carrier nonlinear devices.

In order to achieve such goal the paper is organized in the following way. Firstly some introductory concepts about multi-carrier communications and possible impairments are given. Then, in section III, a suitable behavioral model for multi-carrier operation of nonlinear devices based on Volterra series will be presented. In section IV, we will describe the used parameter extraction procedure and illustrate the performance of the proposed behavioral model under multi-carrier excitation. Finally, some conclusions will be drawn summarizing the obtained results.

II. Review of Multi-Carrier Communications

The first step in order to recognize the increased complexity of multi-carrier systems will be to understand the necessity of wideband and multi-carrier behavioral models to fully characterize the operation of wideband nonlinear components.

The interaction of multi-carrier signals when passed through nonlinear devices lead to a very complex problem due not only to self-distortion from each carrier but also due to the rather important phenomena of cross-modulation that will occur between those multiple carriers. That distortion mechanisms will manifest themselves as extra in-band and out-of-band alterations, which could completely degrade the

carrier signal-to-noise ratio and increase the adjacent channels interference. Other spurious components will appear at intermodulation frequencies that result in interference with other carriers within the operating bandwidth of the device.

Thus, in order to clearly comprehend these phenomenon's we will considered a simple static nonlinearity represented by a power series model truncated at the third-order degree,

$$y[x(t)] = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \qquad (1)$$

where $x(t)$ is the input signal, $y(t)$ is the output signal, and a_1, a_2, and a_3 are the power series coefficients.

Thus, considering that a multi-carrier signal passes through the previous nonlinear model, at the output, we will get several mixtures due to self- and cross-modulations. The mixing outcomes resulting from (1) are shown in Table I, which give us a brief idea about the complexity in terms of the number of mixtures and the wideband necessity for an appropriate behavioral modeling. In this example, two multi-carrier signals with different bandwidths and centered at different carrier frequencies were considered.

TABLE I
OBTAINED MIXTURES FROM THE MODEL IN (1) FOR TWO EXCITATION SIGNALS

First-Order (Linear Output)	Output Central Frequency (Bandwidth)
Linear signal output at ω_1	ω_1 (BW_1)
Linear signal output at ω_2	ω_2 (BW_2)
Second-Order Mixtures	
2nd-order self-modulation (ω_1 - ω_1)	DC ($2BW_1$)
2nd-order self-modulation (ω_2 - ω_2)	DC ($2BW_2$)
2nd-order cross-modulation lower	ω_2 - ω_1 (BW_2 + BW_1)
2nd-harmonic of ω_1	$2\omega_1$ ($2BW_1$)
2nd-harmonic of ω_2	$2\omega_2$ ($2BW_2$)
2nd-order cross-modulation higher	ω_1 + ω_2 (BW_1 + BW_2)
Third-Order Mixtures	
3rd-order cross-modulation ($2\omega_1$ - ω_2)	$2\omega_1$ - ω_2 ($2BW_1$ + BW_2)
3rd-order self-modulation (ω_1 + ω_1 - ω_1)	ω_1 ($3BW_1$)
3rd-order cross-modulation (ω_1 + ω_2 - ω_2)	ω_1 (BW_1 + $2BW_2$)
3rd-order self-modulation (ω_2 + ω_2 - ω_2)	ω_2 ($3BW_2$)
3rd-order cross-modulation (ω_2 + ω_1 - ω_1)	ω_2 (BW_2 + $2BW_1$)
3rd-order cross-modulation ($2\omega_2$ - ω_1)	$2\omega_2$ - ω_1 ($2BW_2$ + BW_1)
3rd-harmonic of ω_1	$3\omega_1$ ($3BW_1$)
3rd-order cross-modulation ($2\omega_1$ + ω_2)	$2\omega_1$ + ω_2 ($2BW_1$ + BW_2)
3rd-order cross-modulation ($2\omega_2$ + ω_1)	$2\omega_2$ + ω_1 ($2BW_2$ + BW_1)
3rd-harmonic of ω_2	$3\omega_2$ ($3BW_2$)

This simple nonlinear model, as expressed in (1), was then excited with two multisine signals centered at different carrier frequencies (ω_1 and ω_2) and with different bandwidths of 1 MHz and 2 MHz for the first and second multisine signal, respectively. In Fig. 1 can be observed the resultant smoothed spectra centered at carriers one and two when the other carrier (multisine signal) is switched on and off.

As can be seen, the action of switching on carrier two will cause a high impact on the in-band and out-of-band distortions in the region of carrier one. This happens because third-order cross-modulations will appear and completely deform the expected performance. It is also important to notice that spectral regrowth appearing at carrier one zone is broader when carrier two is on due to the respective higher bandwidth. Regarding the impact of 3rd-order cross-modulation in carrier two it is not so noticeable due to the lower bandwidth of carrier one but it will occur in the same fashion.

Thus, it is very welcome and appropriate to find suitable behavioral models capable of predict the behavior of nonlinear devices covering not only self-modulation distortion but also cross-modulations between two or more carriers.

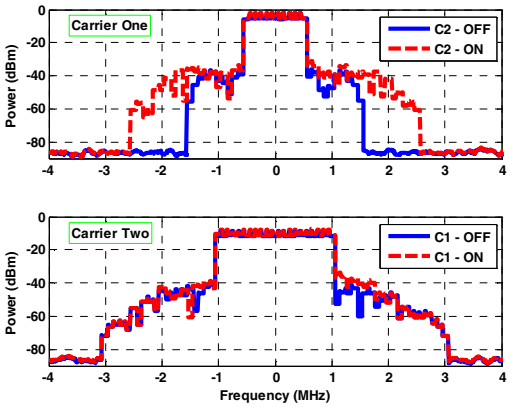

Fig. 1 – Obtained spectrum from the nonlinear model of (1) when excited by a multi-carrier signal: centered at carrier one zone (top), and centered at carrier two zone (bottom).

III. PROPOSED MULTI-CARRIER NONLINEAR BEHAVIORAL MODEL

This section is devoted to explain the proposed behavioral model scheme for the prediction of multi-carrier operation of general nonlinear systems. As was seen in the last section the correct description of a multi-carrier nonlinear component behavior requires that it must be wideband and it must depend on several input signals.

Moreover, looking to Table I we can state that nonlinear signal generation could force spectral components to appear at very different output frequencies. This fact will impose that the dynamic response of the nonlinear device might have delays of different orders and this should be also followed by the projected behavioral model.

In that way, in order to cover such a wideband nonlinear system (as multi-carrier devices) we have decided to treat each nonlinear cluster independently. In the next section it will be shown that this approach will facilitate the parameter extraction and possibly reduce the needed parameters for the entire model.

As was mentioned in the Introduction we have chosen the Volterra series [7] approach to find appropriate behavioral models for the wideband nonlinear components, due to its good performance in this type of mildly nonlinear scenarios. A Volterra series is a combination of linear convolution and a nonlinear power series that provides a general way to model a nonlinear system with fading memory and it can be written as,

$$y(t)=\sum_{n=0}^{\infty}\int_{-\infty}^{\infty}\cdots\int_{-\infty}^{\infty}h_n(\tau_1,\cdots,\tau_n)x_{in}(t-\tau_1)\cdots x_{in}(t-\tau_n)d\tau_1\cdots d\tau_n \quad (2)$$

where $x_{in}(t)$ and $y(t)$ are the input and output signals, respectively, and $h_n(\tau_1,\ldots,\tau_n)$ is the n^{th} order Volterra kernel.

As a way to make the proposed behavioral model practical we plan to apply the Volterra series model with a low-pass equivalent format [8], and then individually apply each low-pass model to the respective cluster. Therefore, the complete Volterra model will be a collection of different models for each cluster that are extracted individually.

The underlying concept of the proposed model is depicted in Fig. 2 for the nonlinear clusters associated to the carrier's one and two, lower and higher cross-modulations of second-order and third-order cross-modulations arising from $2\omega_1$-ω_2 and $2\omega_2$-ω_1. This proposed model could be extended to account for an augmented number of mixtures occurring in the multi-carrier nonlinear device but, obviously increasing the model complexity.

For example, the mathematical description to the signals centered at carrier one (and two) zone should account for several contributions such as: linear signal output; in- and out-of-band self-modulations; and in- and out-of-band cross-modulations:

$$\begin{aligned}\tilde{y}_{C_1}(k)=&\sum_{q_1=0}^{Q_{C1}}\tilde{h}_{1,C_1}(q_1)\cdot\tilde{x}_1(k-q_1) \quad +\\ &\sum_{q_1=0}^{Q_{C1}}\sum_{q_2=q_1}^{Q_{C2}}\sum_{q_3=q_2}^{Q_{C3}}\tilde{h}_{3,C_1}(q_1,q_2,q_3)\cdot\tilde{x}_1(k-q_1)\cdot\tilde{x}_1(k-q_2)\cdot\tilde{x}_1^{*}(k-q_3)\\ &\sum_{q_1=0}^{Q_{C1}}\sum_{q_2=q_1}^{Q_{C2}}\sum_{q_3=q_2}^{Q_{C3}}\tilde{h}_{3,CM_3}(q_1,q_2,q_3)\cdot\tilde{x}_1(k-q_1)\cdot\tilde{x}_2(k-q_2)\cdot\tilde{x}_2^{*}(k-q_3)\end{aligned} \quad (3)$$

where $h_{1,C1}$ is the linear signal kernel, $h_{3,C1}$ and $h_{3,CM3}$ are the third-order kernels for the self-modulation and cross-modulation responses, respectively. The character ~ means that it is a complex signal or value, and the symbol * represents the complex conjugate.

As well, the lower second-order cross-modulation arise from a second-order multiplication:

$$\tilde{y}_{CM_2L}(k)=\sum_{q_1=0}^{Q_{A1}}\sum_{q_2=q_1}^{Q_{A2}}\tilde{h}_{2,CM_2L}(q_1,q_2)\cdot\tilde{x}_2(k-q_1)\cdot\tilde{x}_1^{*}(k-q_2) \quad (4)$$

The remaining nonlinear components are obtained in a similar reasoning. Moreover, if higher orders are needed, then more Volterra kernels should be determined.

IV. Parameter Extraction Procedure and Measurements Validation

In this section we will start by explaining the parameter extraction procedure used in this work and then several measurements with a two-carrier excitation will be addressed in order to assess the model accuracy.

For the case study to be presented here, we have used as the device-under-test (DUT) a simple CR receiver, which has at the input a commercial wideband low-noise amplifier with a 1-dB compression point of +8 dBm, an approximate gain of 20 dB, and a noise figure of 3.8 dB.

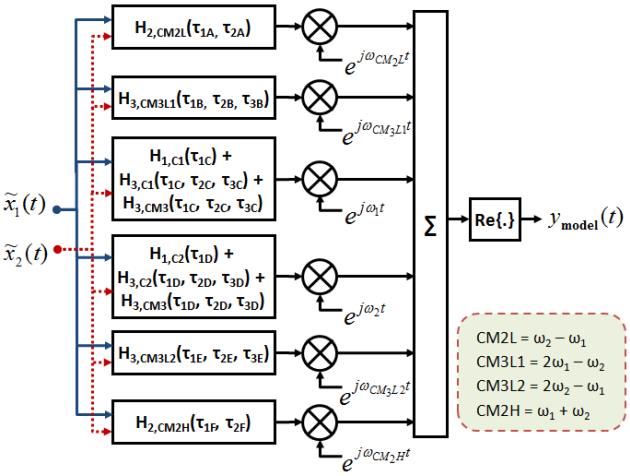

Fig. 2 – Proposed design for the wideband nonlinear behavioral model.

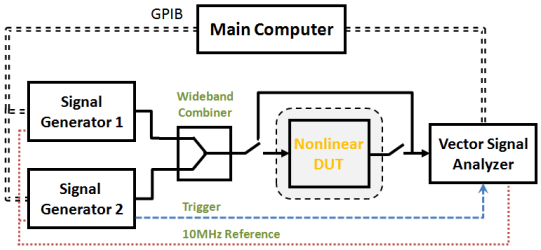

Fig. 3 – The experimental test bench used.

A. Parameter Extraction Procedure

To correctly characterize the nonlinear DUT and perform the necessary measurements we have used the set-up presented in Fig. 3. As can be observed two signal generators followed by a wideband combiner was used in order to produce the input signals, and a vector signal analyzer to acquire both the inputs and desired outputs to be modeled. With this approach we are already measuring the input complex envelopes and the selected output complex envelopes (carrier one; carrier two; 2nd-order cross-modulations; 3rd-order cross-modulations; etc.) to then apply the proposed low-pass behavioral model on each nonlinear cluster.

Then, in order to determine the required low-pass complex Volterra kernels we have utilized the same technique that was used in [5, 6], a least-squares extraction, expressed by

$$\mathrm{H}=(\mathbf{X}^T\mathbf{X})^{-1}\mathbf{X}^T\mathrm{Y} \quad (5)$$

where $\mathbf{X}$ and Y corresponds to the complex input signals and to each measured output nonlinear cluster, respectively.

Furthermore, great care should be taken when choosing the carrier frequencies, signal bandwidth, etc. because we must certify that each specific nonlinear cluster does not fall in overlapping frequency bands where this model extraction will no longer be valid. It should also be pointed out that a special care should be done when synchronizing all the signals, using instrumentation triggers.

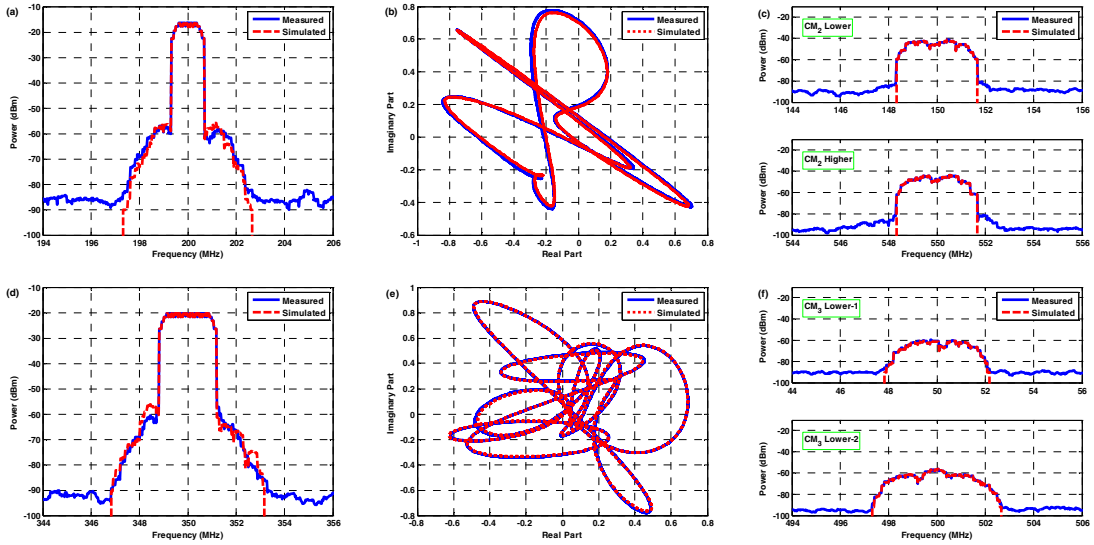

Fig. 4 – Measured and simulated results for the multi-carrier excitation: (a) spectrum of carrier 1, (b) time envelope of carrier 1, (c) spectrum of 2nd-order cross-modulations, (d) spectrum of carrier 2, (e) time envelope of carrier 2, and (f) spectrum of 3rd-order cross-modulations.

B. Measurements Validation

In order to evaluate the performance of the proposed behavioral model we have excited the DUT with two multisine signals, the first with 11-tones carrying random phases in a bandwidth of 1 MHz and the second composed by 21-tones with random phases in a bandwidth of 2 MHz. The selected carrier frequencies were 200 MHz and 350 MHz for the first and second excitations, respectively. We have set each carrier to an average input power of -24 dBm and performed several measurements with the set-up shown in Fig. 3.

The obtained results are shown in Fig. 4. There it can be roughly observed that the behavioral model and the described parameter extraction is estimating well the unknown parameters and producing similar results. We have also verified the integrated power in several important bands and the results are exposed in Table II.

Finally, we have calculated the normalized mean squared error (NMSE) for the two carriers and have achieved -32.4 dB for the first excitation and -27.5 dB for the second excitation executed in the time envelopes presented in Fig. 4 (b) and (e).

TABLE II
MEASURED AND SIMULATED OUTPUT POWERS FOR EACH CLUSTER

	Meas. [dBm]	**Model [dBm]**		**Meas. [dBm]**	**Model [dBm]**
Carrier 1	-6.17	-6.27	*CM_2 Lower*	-29.7	-29.7
Adj. Ch.-C_1 (Lower)	-48.0	-47.7			
Adj. Ch.-C_1 (Higher)	-48.8	-47.9	*CM_2 Higher*	-32.2	-32.1
Carrier 2	-7.24	-7.26	*CM_3 Lower-1*	-47.3	-47.5
Adj. Ch.-C_2 (Lower)	-50.7	-48.2			
Adj. Ch.-C_2 (Higher)	-49.9	-52.0	*CM_3 Lower-2*	-45.2	-45.2

V. CONCLUSIONS

In this paper we have proposed and analyzed a new behavioral model for multi-carrier nonlinear systems. This model is based in input/output measurements and was demonstrated and validated for a two-carrier scenario till a third-order degree nonlinearity, but it can be practically extended to higher nonlinear orders and number of excitations.

It should be emphasized that this model is suitable for large bandwidths as was shown. This is due to the specific structure of the parameter extraction based in a low-pass equivalent format that considers each nonlinear cluster separately.

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[C4] – Enhanced Architecture to Increase the Dynamic Range of SDR Receivers

Pedro M. Cruz and Nuno B. Carvalho

IEEE Radio and Wireless Symposium, Phoenix, AZ, pp. 331-334, Jan. 2011

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Enhanced Architecture to Increase the Dynamic Range of SDR Receivers

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***Abstract* — This paper proposes an architecture to increase the dynamic range of the analog to digital signal conversion. Preferably, such an architecture will witness more applicability in the wideband digital receivers for software-defined radio. It is based in passive circuitry followed by two analog-to-digital converters that acquire the incoming analog signal, and then digital signal processing is applied to reconstruct the signal.**

We will demonstrate clear improvements related to the case when only one analog-to-digital converter is used. Also, this architecture will be validated through several simulations, in which it will be subjected to common modulated signals that confirms the validity of such an architecture.

***Index Terms* — Analog-to-digital conversion, dynamic range, software-defined radio receivers.**

I. Introduction

The future RF architectures for software-defined radio (SDR) and cognitive radio (CR) areas should be able to receive any type of signal despite its bandwidth and dynamic range. In that sense the path is moving towards multi-norm, multi-standard radios that are capable of receiving a huge range of bandwidth combined with very different power levels, and thus high dynamic range approaches. In [1] Mitola has proposed that the receiving unit for an SDR should have a very wide bandwidth analog-to-digital converter (ADC) to gather and convert all the signals from analog to digital, and that ADC should have a strong dynamic range associated, since it may receive low power signals combined with high power ones, and considering that if the radio has to receive several different signals they should not combine with each other.

Also, the emergence of RF mixed signal circuits as the SDR and the next step up to CR approaches [2] have opened a new field of research in order to find a feasible transceiver architecture to be utilized. In these CR scenarios the incoming signal can comprise several different modulations conjugated with orthogonal frequency division multiplexing (OFDM) which can have very high peak-to-average power ratios (PAPR), and thus if the receiving unit is not designed accounting with these drawbacks, in the end it will degrade completely the quality of the received signal. An helpful solution for that could be the use of the available peak reduction techniques. Nevertheless, specifically for the receiving unit those peak reduction techniques are not easy to be applied or not practical.

Thus, in this paper our goal is to propose an architecture that increases the receiving dynamic range that should be easily reconfigured and adapted, and be able to detect both low power signals and high power ones (known signals or interferes).

Related to that, there are already several proposed architectures to deal with these aspects like, for example, the ones patented in [3, 4]. One of these works is appointed to be used in a wideband receiver and is based on the application of varying gains/attenuations to the input signal and then feeding the scaled signals to conventional ADCs followed by a multiplexer that will output a higher number of bits than each ADC. Nevertheless, it is not obvious how much the dynamic range will be improved. The other work make use of programmable gain amplifiers to adjust the signal power before it is converted by two parallel ADCs, and in a digital signal processor (DSP) the correct digitized signal is selected. Actually, this works is chosen to use in DSP-based acoustic devices but it can also be employed in wireless receivers. However, it is based in active devices that will increase the DC power consumption and potentially the nonlinear distortion when in presence of interferers. Moreover, in [5] it is proposed a new technique to extend the dynamic range of the A/D conversion based in an analog signal splitter followed by two ADCs in parallel and then digital signal processing. There it is claimed an improvement in the dynamic range of around 6 dB's confirmed by the simulations based on ideal device models. However, the proposed architecture is based in active devices that will pose the same restrictions of the previous work.

In this paper a new solution based on the attenuation of a specific branch followed by two parallel ADCs will be shown. Firstly, some details about the proposed architecture are given and possible employments in a complete receiver front end will be pointed out. Then, in Section III, the proposed architecture will be validated by several simulations in Matlab software. Moreover, its performance will be evaluated and compared with the performance of a simple ADC. In Section IV, we will present a complete validation of the proposed configuration subjecting two different modulated signals. Finally, some conclusions will be drawn.

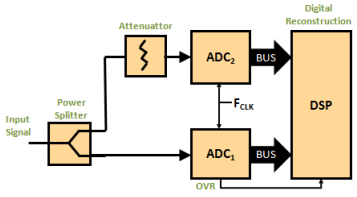


Fig. 1 – Proposed architecture to extend the dynamic range of the analog-to-digital conversion.

II. Details of the Proposed Architecture

This section is devoted to give more details about the proposed architecture to increase the dynamic range of the A/D conversion by using passive devices (a power splitter and an attenuator) followed by two ADCs in parallel and then a DSP/FPGA to perform the necessary treatments on the received digital bits.

The concept of the proposed architecture is depicted in Fig. 1. The core idea is to pass, as far as possible, to the digital domain any type of processing that may be applied in the incoming waveforms in order to overcome with the device's clipping behavior. In this case, for instance, the separation between small and large amplitude signals is made in the digital domain by using software functions.

Firstly, the input signal is separated into two equal parts by a power splitter. Then, one of the paths goes directly to one of the ADCs and it is digitized, and the other signal is attenuated and passed to the second ADC to be also digitized. Finally, a DSP will perform some tasks in order to reconstruct the signal. It is important to refer that the digital bits of the upper ADC are taken only when the signal exceeds the full-scale range of the lower ADC. This operation is signalized by the OVR (over-range indicator bit) that is a common output of an ADC, but other helpful techniques can be applied in software to define when to activate the second ADC outputs or when to put this ADC in a standby mode in order to diminish the DC power consumption.

The main tasks that have to be executed by the DSP are: first apply a digital gain (equal to the attenuation value imposed) to the digitized signal coming from ADC_2; calculates an error signal between this amplified version and the one received at ADC_1; finally reconstruct the signal by summing the ADC_1 output with the calculated error signal, which is executed for each time sample (of the clock used for the ADCs) that the input signal have activated the OVR bit of the ADC_1.

Observing the proposed architecture (from now on called configuration 2) it is obvious that it will demand for more devices than the normal implementation with only one ADC (from now on termed configuration 1). Even though, the complexity of the circuit as increased and the necessity of more processing capability, the potential improvements that can be obtained can be much valuable. Another constraint of the proposed architecture is the fact that using a power splitter will force, at least, a loss of 3 dB in the signal chain. However, this aspect can be easily solved by increasing the gain before this splitter (e.g. increasing the low-noise amplifier gain).

The advantages of this new proposed architecture are: it is able to extend the dynamic range of the A/D conversion in a value equal to the attenuator used (can be a variable attenuator with the obvious limits in the attenuation value); it is not so dependent on active analog devices that may originate several restrictions that turn the functionality of the receiver unpractical.

Moreover, the flexibility of such an architecture allow us to use it, for instance, in a band-pass sampling receiver [6, 7], Fig. 2, but also in other types of receivers without increasing so much the complexity of the front end, however our proposal is intended for wideband digital receivers to be used in SDR/CR applications.

III. Architecture Validation with CW Excitation

In this section we will evaluate the performance of the two previously mentioned configurations when subjected to a one-tone excitation. In order to be able to simulate both configurations we have constructed a model in Simulink for a pipelined ADC based on the premises presented in [8]. Our model accounts for quantization noise and clipping behaviors, and a 10-bit ADC was considered, which from theory could ideally achieve a maximum signal-to-noise ratio (SNR) of around 62 dBFS. Also, in this case, the ADCs used have a full-scale range of 1 Vpp, i.e., admits a maximum input power of +4 dBm (for a 50 Ω source) starting to clip after this value. The clock frequency used was equal to 90 MHz.

After that we have determined several figures of merit for the two configurations applying a -1 dBFS one-tone excitation and the results are presented in Table 1 and Fig. 3. These simulations have taken into consideration the ADC testing standard [9] and were performed accordingly to the coherent sampling theorem.

TABLE I
Obtained metrics for a -1 dBFS one-tone excitation signal

	Configuration 1	Configuration 2
Pout [dBm]	2.98	12.97
SNR [dBFS]	60.98	61.10
SINAD [dBFS]	60.95	61.04
SFDR [dBc]	87.93	84.51
THD [dBc]	83.85	79.67

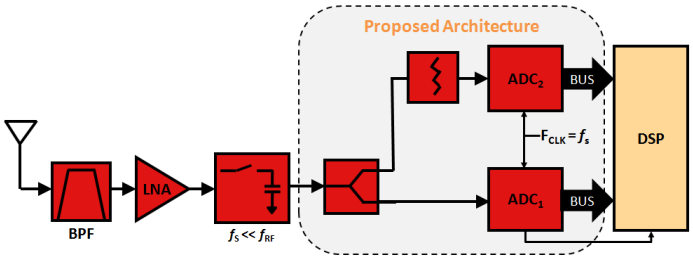


Fig. 2 – Proposed architecture to improve the dynamic range employed in a band-pass sampling receiver.

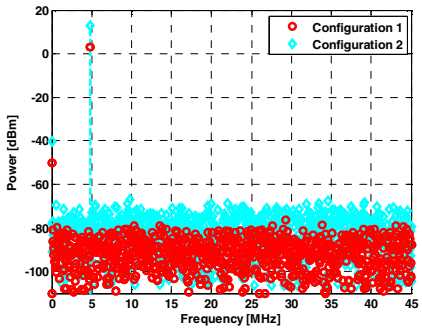


Fig. 3 – Simulated spectrum obtained with a -1 dBFS one-tone excitation signal for the two addressed configurations.

As can be seen from Fig. 3 the two depicted spectrums are quite similar with just an increase of about 10 dB (equal to the attenuator value used) in both signal frequency bin and noise floor for the case of configuration 2. Moreover, this is completely validated by the obtained values for each figure of merit shown in Table 1, wherein these results are almost equal to the configuration 1 except the maximum output power that has increased.

After that, using the same CW excitation we have swept the input signal power from -29 dBm to +17 dBm and measure the previously mentioned figures of merit. The obtained results are shown in Figs. 4 (a)-(c).

Once again the simulated results corroborate the previous assumptions about the proposed architecture demonstrating for each quantity an improvement of around 10 dB. Furthermore, we can observe that the main figures, such as, the signal-to-noise and distortion ratio (SINAD) and spurious-free dynamic range (SFDR) are almost equal in the linear range and kept at a very good performance above that level until its new full-scale limit. The high variation observed in the SNR and SINAD after the first clipping point (+4 dBm) is due to the fact that now we have a new full-scale limit (+14 dBm), i.e., if we plot these metrics in terms of dB to full-scale (dBFS) we will ideally obtain a constant level at 62 dBFS.

It is also very important to refer that in the presented results and in order to match the values of both configurations, the input power used for configuration 2 is 3 dB higher than the configuration 1 (to compensate the loss in the power splitter).

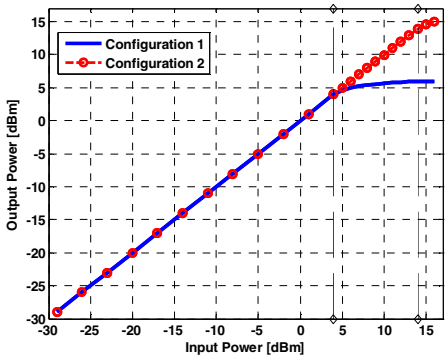
IV. Simulation Results for Modulated Signals

In order to corroborate the validity of the proposed architecture we have conducted several simulations with two different modulated signals such as quadrature-phase-shift-keying (QPSK) with a PAPR of around 4.96 dB and a 64-quadrature-amplitude-modulated (64-QAM) providing a PAPR of 6.49 dB. The obtained results for the two tested configurations are shown in Figs. 5 (a)-(d).

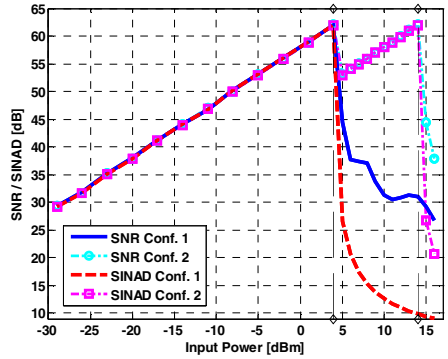
Fig. 5 (a) presents the output power in the fundamental and upper adjacent channels for a QPSK modulated signal centered at 10 MHz for the same clock frequency. As can be easily seen the configuration 2 only starts to clip 10 dB after the configuration 1. In Fig. 5 (b) we can observe an improvement in the error vector magnitude (EVM) for both modulations with an increase of 10 dB in the input power.

Finally, in Figs. 5 (c) and (d) are illustrated two constellation diagrams for a 64-QAM signal, in which we can state that for the configuration 1 we do not have any useful information contrary to the case of configuration 2 where we are able to correctly demodulate the received signal.

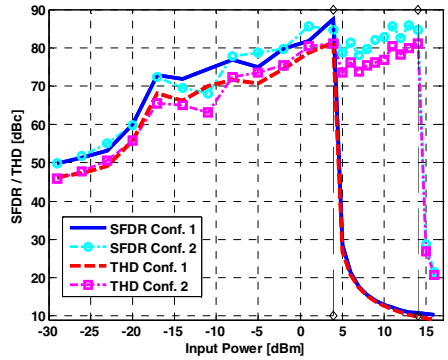
It is worth to mention that in each graph where the input signal power is varied we depict two more vertical black dashed lines (at +4 dBm and +14 dBm) to represent the full-scale limits of each configuration.



(a)



(b)



(c)

Fig. 4 – Obtained results for the two tested architectures with a one-tone excitation represented by several figures of merit: (a) Pin vs. Pout, (b) SNR and SINAD, and (c) SFDR and THD, (solid line – Configuration 1) (dashed-circle/square line – Configuration 2).

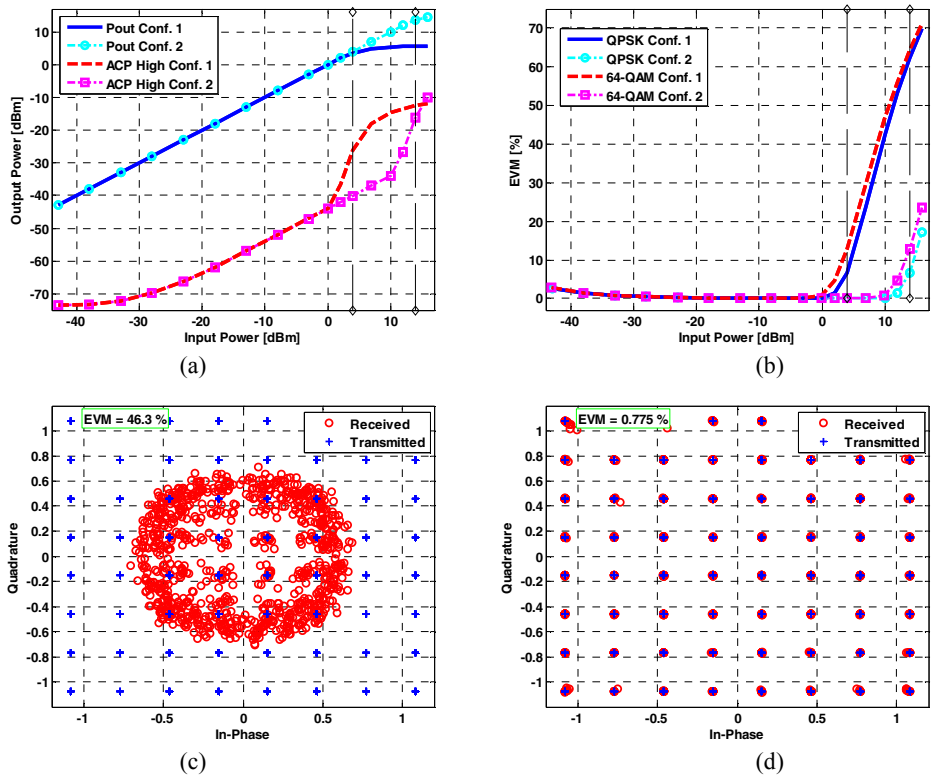


Fig. 5 – Obtained results for the two addressed configurations when subjected to different modulated signals: (a) output power and adjacent-channel power for a QPSK signal, (b) error vector magnitude vs. input power for the two modulations, (c) constellation diagram of a 64-QAM signal with an input power of +10 dBm applied to configuration 1, and (d) constellation diagram of a 64-QAM signal with an input power of +10 dBm applied to configuration 2.

V. Conclusion

In this paper we have proposed an advanced architecture to increase the dynamic range of the analog to digital conversion, which do not raise excessively the number of components to be used providing an augmented flexibility.

In fact, this new configuration could seen applicability in the wideband digital IF receivers (in which the received signal is demodulated in the digital domain) for the SDR and CR fields. This is because of the increased robustness of the new architecture has to circumvent, for example, interference problems of high power signals in lower ones.

We have validated the proposed configuration by using several figures of merit with a one-tone excitation signal. Moreover, we also performed simulations with two different modulated signals demonstrating obvious improvements.

The results showed that with this new configuration we are able to increase the dynamic range in 10 dB's, being this value controlled by the attenuator value used.

Acknowledgement

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[C5] – Evaluation of Second-Order Bandpass Sampling Receivers for Software Defined Radio

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Evaluation of Second-Order Bandpass Sampling Receivers for Software Defined Radio

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***Abstract*—This paper proposes a new design for second-order bandpass sampling receivers based on passive 90º hybrids and two parallel ADCs sampled with the same clock. Such a topology is suitable for wideband digital receivers appointed for software defined radio and spectrum sensing capable cognitive radios.**

The proposed architecture and digital compensation algorithm are a simple solution for the reception of a modulated signal under an adjacent stronger interference and for multiband multi-carrier modulated signal communication, due to its available bandwidth maximization. The results will be assessed in terms of spectrum representation and error vector magnitude evaluation.

Keywords-Bandpass sampling; cognitive radio; digital signal processing; second-order sampling; software defined radio

I. INTRODUCTION

Nowadays radio communications continue to see significant changes and improvements every day. Moreover, several ideas are being delineated and appoint to radio architectures approaching multiband and multi-carrier designs, such as LTE-Advanced with carrier aggregation [1].

It is now accepted that software defined radios (SDR) as proposed by Mitola in [2] will be the most probable solution for resolving the need of integration between wireless communication standards. Such a solution allows inexpensive, efficient interoperability between the available standards and frequency bands by a simple change in software algorithms. This SDR concept is also the basis for cognitive radio (CR) approaches [3], in which the underneath concept imposes strong changes in terms of both complexity and flexibility of operation due to its potential adaptation to the air interface.

All these considerations impose the use of analog-to-digital converters (ADC) and digital-to-analog converters (DAC), which became crucial components for this type of SDR/CR solutions. Thus, in order to capture such multiband multi-carrier signals, it will be necessary to design systems having large instantaneous dynamic range in conjunction with high receiving bandwidths.

However, increasing continuously the sampling rate of ADC/DACs should not be the solution for the high bandwidths because this will force a power consumption raise and thus, affect the overall system efficiency.

Much more interesting approaches are the use of second-order sampling [4] (also known as complex sampling) to augment the working bandwidth, associated to bandpass sampling [5] to sample signals at higher frequencies with lower sampling rates.

In that sense, the main goal of this paper is to present a new design that facilitates the implementation of second-order bandpass sampling receivers (BPSR) for SDR/CRs. The proposed design is able to receive multiband multi-carrier signals and is accompanied by digital compensation functions to further reduce unwanted image components.

In order to fulfill such an objective the paper is organized in the following way. Firstly a brief discussion about second-order BPSR implementations and concepts are given. Then, in section III, a new design that supports its operation in wideband 90º hybrids is described. In section IV, several measurement results are presented and its performance is illustrated in different scenarios. Finally, some conclusions will be drawn according to the obtained results.

II. DISCUSSION OF SECOND-ORDER BPSR DESIGNS

The first step in order to understand the operation of these novel schemes will be to study and understand the theory and proposed approaches behind the second-order BPSR, [6].

A general block diagram to implement this concept is presented in Fig. 1. The underneath idea is to separate the incoming signal into two paths having equal amplitude performance over the interesting frequency band and shifted by 90º in terms of phase description. This is known as the Hilbert transformation and has a frequency response as:

$$H(f) = \begin{cases} -j, & 0 \le f < f_A \\ +j, & -f_A \le f < 0 \end{cases} \quad (1)$$

Nevertheless for the microwave community this can be approximated by a broadband 90º phase shifter.

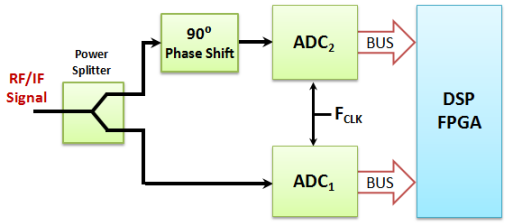

Fig. 1 – General block diagram of a second-order BPSR.

Ideally, with such an approach it is possible to completely eliminate any image signal created either in the sampling process or actually present at the input of the system. So, it is possible to make use of both positive and negative parts of the incoming spectra and thus, doubling the working bandwidth when compared to a single path, for instance, case of a first-order bandpass sampling receiver [7].

However, it is known that analog implementations are not perfect and suffer from several impairments. In that sense, when employing such a design in wideband receiver architectures, it is expected that the Hilbert transform requirements (equal amplitude and 90º phase balances) are not fulfilled. Considering the path without 90º phase shift as I-path and the one with 90º shift as Q-path, the I/Q imbalance of the system is defined as:

$$\begin{pmatrix} S_I'(t) \\ S_Q'(t) \end{pmatrix} = \begin{pmatrix} 1 & 0 \\ -g\sin(\varphi) & g\cos(\varphi) \end{pmatrix} \begin{pmatrix} S_I(t) \\ S_Q(t) \end{pmatrix} \quad (2)$$

where $S_I(t)$ and $S_Q(t)$ are the signals at the input, $S_I'(t)$ and $S_Q'(t)$ represent the signals after the system, and g and φ are amplitude and phase imbalances, respectively.

The created amplitude and phase imbalances will induce an imperfect image rejection and achieve a certain sideband suppression, which is given by:

$$Sideband\_Suppression(dBc) = 10\log_{10}\left(\frac{g^2 - 2g\cos(\varphi) + 1}{g^2 + 2g\cos(\varphi) + 1}\right) \quad (3)$$

In Fig. 2, it is illustrated the attainable sideband suppression when varying the gain error (g) and the phase error (φ).

Actually, this subject has been attracting the interest of scientific community, which have result in several works dedicated to different points ranging from the study of algorithms to determine optimum sampling frequencies [8] to the construction of digital compensation filters [9, 10].

For example, when employing a time-delay given by $\Delta T = 1/(4 * f_c)$, which represents a fixed 90º phase shift for a single frequency, it will imply a frequency response as described by:

$$H(f) = 1 + j.e^{-j.2\pi.f_c.\Delta T} \quad (4)$$

This procedure is able to totally eliminate any image signal only at a given frequency (f_c), which defines the time delay to employ between the I and Q paths either in the signal or clock paths. Then, as mentioned above, it is usual to perform digital compensation to correct the referred impairments being this based either on variable delay fixed interpolants [9] or fractional delay filters [10].

However, these techniques do not present yet practical and feasible FPGA/DSP implementations with acceptable performances for multiband multi-carrier operation within different input powers.

In summary, it can be said that such an architecture can be easily adopted for RF/microwave wideband digital receivers, as for example in low-IF receivers that initially translates the desired multiband signal to an intermediate frequency equal to the ADC sampling frequency or multiples of it (f_s, $2f_s$, etc.). Then, RF/IF bandpass filtering has to be executed by tunable filters or a bank of filters, to select the correct band (pairs of even and odd Nyquist zones, NZ's).

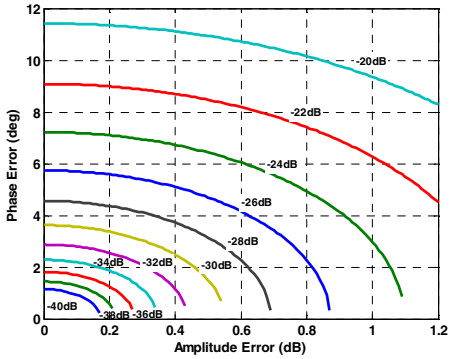

Fig. 2 – Sideband suppression dependence on phase and amplitude errors, as calculated by (3).

III. Proposed Design with Digital Compensation

Considering the conclusions from Section II, the study of implementation constraints for this second-order BPSR is fundamental to design a feasible multiband architecture.

In that sense, the proposed idea, in this paper, is based on the use of a 90º hybrid to approximate, in a limited but wide frequency range, the desired Hilbert transformation. To the authors knowledge it is the first time that a hybrid solution is used in conjunction with digital compensation to implement a complex BPSR. The block diagram is shown in Fig. 3.

Looking to Fig. 4 it is possible to observe that a simple commercial hybrid presents very interesting characteristics in terms of amplitude and phase imbalances (relatively constant over the band), which allows the execution of wideband Hilbert transformation with satisfactory sideband suppression.

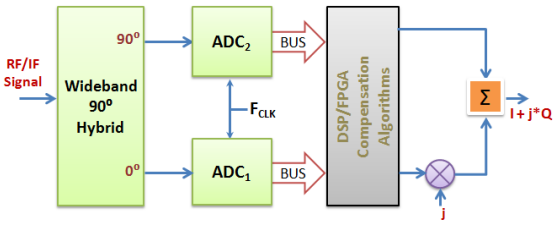

Fig. 3 – Block diagram of the proposed design for complex BPSR.

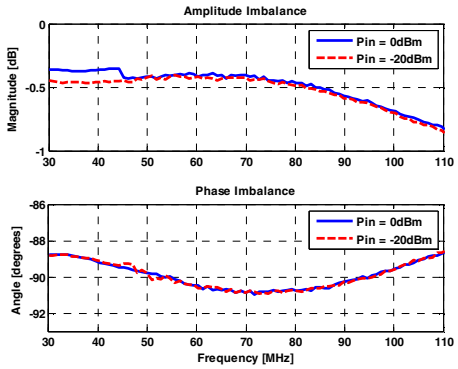

Fig. 4 – Performance of a commercial 90º hybrid within the band of interest measured in a commercial vector network analyzer.

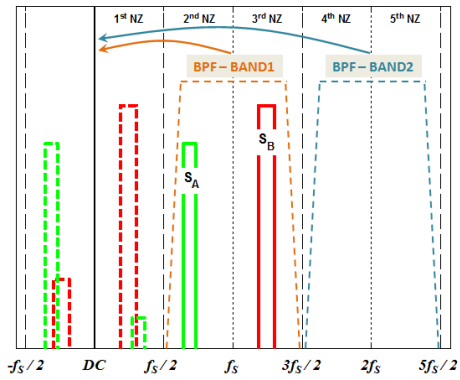

Fig. 5 – Frequency domain illustration of the working process for the proposed design.

Similarly to other receiving architectures the incoming signal has to be filtered and down-converted to reasonable IF frequencies. For example, Fig. 5 shows two signals (S_A and S_B) previously down-converted to the 2nd and 3rd NZ's respectively. Afterwards, the process of bandpass sampling will move it to the 1st NZ (positive and negative parts) and at same time create image components that are attenuated because of the used configuration. In this approach we observed that image attenuations in the range of 30-35 dB are obtained just by the use of a 90º hybrid.

In order to reduce even further these image components a simple compensation algorithm is implemented on the digital domain. At this point, the reverse matrix of (2) is directly applied on the previously received I and Q waveforms:

$$\begin{pmatrix} C_I(t) \\ C_Q(t) \end{pmatrix} = \frac{1}{\cos(\varphi)} \begin{pmatrix} \cos(\varphi) & 0 \\ \sin(\varphi) & 1/g \end{pmatrix} \begin{pmatrix} S_I'(t) \\ S_Q'(t) \end{pmatrix} \quad (5)$$

Then, these C_I and C_Q waveforms are combined to generate the final complex output $(C_I + j*C_Q)$.

As can be understood the used compensation scheme can only be optimal at a single frequency. This fact allow us to optimize its operation to reject the high power signal images when falling close by to low power ones, permitting an enhancement on the respective signal-to-noise ratio (SNR) important for signal demodulation.

Also, because of its simplicity, the proposed design demands a lower processing power from the FPGA/DSPs to obtain comparable image attenuations of existent architectures.

IV. Measurement Results

In order to validate the operation of the described complex BPSR architecture for the 2nd and 3rd NZ's (Band 1 in Fig. 5), a demonstrator has been implemented using laboratory components. This was accompanied by a careful development of an experimental setup to characterize it.

In the same way higher NZ's can be exploited for this second-order bandpass sampling operation, as represented in Fig. 5 by the 4th and 5th NZ's (Band 2).

After the filter (BPF) to select the desired band (35 MHz – 105 MHz) a commercial 90º hybrid (performances depicted in Fig. 4) was used. This was followed by a two-channel 10-bit pipeline ADC with a linear input range of approximately +10 dBm, an analog input bandwidth of 200 MHz and sampled with a clock frequency of 70 MHz. This value was chosen because of limitations on the laboratory components.

Then, several experiments were conducted in the proposed design. Firstly, the performance of the proposed architecture was evaluated when excited by two sinusoidal signals. The carrier frequencies chosen were 49 MHz and 88 MHz in order to fall in the 2nd and 3rd NZ's.

The second test attempts to assess the performance when it is excited by a QPSK signal with 1.75 Mbps of symbol rate and being interfered by a multisine signal with 4 MHz carrying random phases.

The last test consisted on the computation of the error vector magnitude (EVM) for two modulated signals being received simultaneously. In this situation we have used a 16-QAM signal centered at 88 MHz (which resulted in 18 MHz after bandpass sampling) carrying a symbol rate of 3.5 Mbps. The second channel has a QPSK signal with 1.75 Mbps and situated at 49 MHz (resulting in -21 MHz after bandpass sampling).

Looking to Fig. 6 (a)-(c), it can be noticed by the shown frequency domain spectra's a high rejection of the image signals in the several experiments conducted. Moreover, it should be stressed that the applied compensation scheme is able to further improve the image rejection obtained with the complex BPSR. As mentioned above, this compensation algorithm is focused on the lower power signal in a way to increase the associate SNR parameter, important aspect in the baseband signal demodulation.

Table I and Table II present the calculated EVM values for the different situations addressed when varying input powers of the input signals. There it can be observed that the proposed design is always better than a single path case. These results are partially illustrated in Fig. 6 (d)-(f).

Generally, the obtained results verify the proper operation of the proposed design for realistic signal environments.

TABLE I. Measured EVM results for a QPSK signal with a multisine interferer

Pin (MS)	Pin (QPSK)	EVM (Proposed)	EVM (Single Path)
0 dBm	0 dBm	1.52%	2.65%
0 dBm	-10 dBm	1.49%	2.78%
0 dBm	-20 dBm	1.88%	5.19%
5 dBm	-5 dBm	1.48%	2.66%
5 dBm	-15 dBm	2.67%	6.56%

TABLE II. Measured EVM results for multiband modulated signal reception using the proposed design

Pin (16-QAM)	Pin (QPSK)	EVM (16-QAM)	EVM (QPSK)
0 dBm	0 dBm	1.33%	1.77%
0 dBm	-10 dBm	2.46%	1.77%
0 dBm	-20 dBm	4.34%	2.01%
5 dBm	-5 dBm	1.59%	2.29%
5 dBm	-15 dBm	3.86%	5.91%

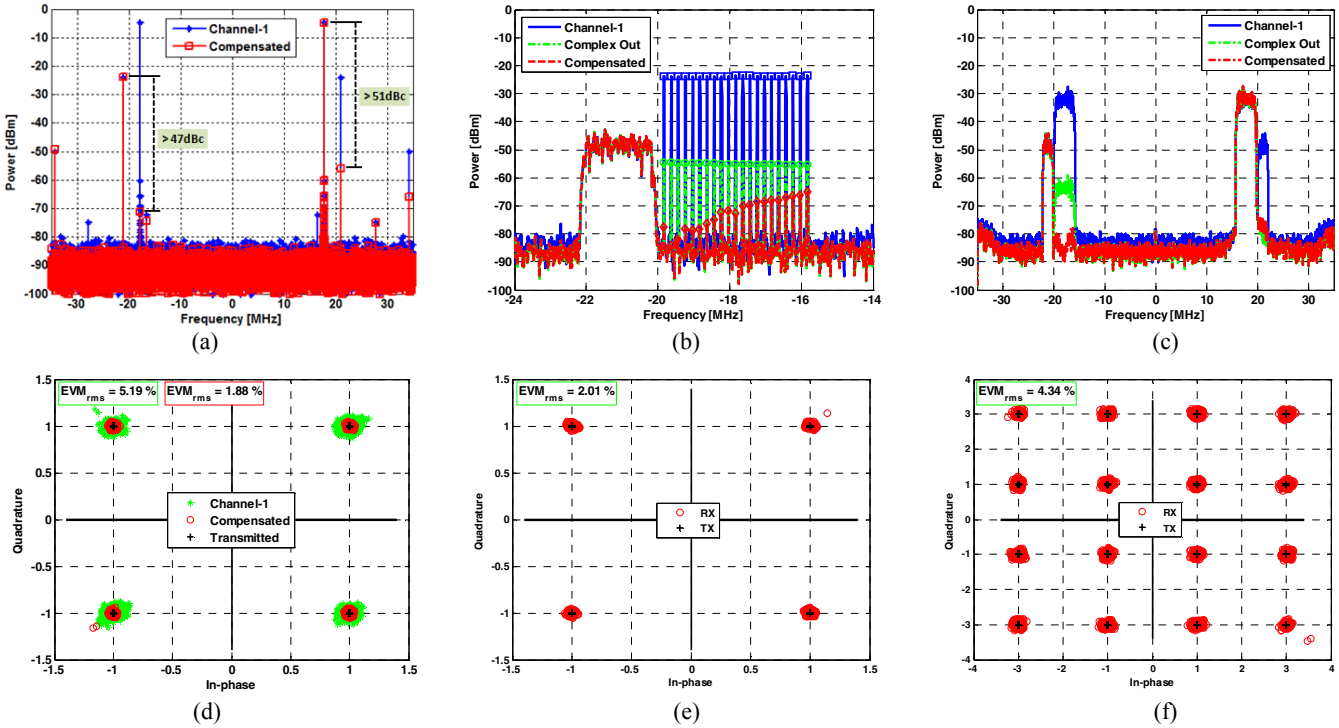

Fig. 6 – Frequency domain results for (a) two sinusoidal signals, (b) a QPSK interfered by a multisine and (c) multiband reception. Signal demodulation results of (d) QPSK signal under multisine interference for single path and proposed design, (e) and (f) QPSK and 16-QAM baseband I/Q information for a multiband reception system.

V. CONCLUSION

In this paper we have proposed a novel design for second-order BPSR based on a passive and wideband 90º hybrid that is able to double the working bandwidth. This will create room for potential improvement on the performance of current FPGA/DSPs. As well, reductions in the overall system power consumption will be expected.

This implementation is much straightforward than other approaches due to its easy analog part construction and because of the use of a single clock instead of two precisely delayed clocks.

Very promising results (focusing the high image rejection) were obtained by using a simple digital correction algorithm in order to make it easily implementable within FPGA solutions. Further developments could be then achieved in the digital compensation scheme to improve the image rejection for a wideband operation.

ACKNOWLEDGMENT

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Appendix B – Curriculum Vitae

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Curriculum Vitae

Pedro Miguel Cruz

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Email: pcruz@av.it.pt or pedrocruz82@gmail.com
Nationality: Portuguese
Date of Birth: 31/12/1982
Driving License: Category B
Marital Status: Single

ACADEMIC DEGREES

- **Ph.D. in Electrical Engineering, University of Aveiro, Portugal** 09/2008-Present
  Advisor: Prof. Nuno Borges Carvalho
  Degree Thesis: "Characterization and Modeling of Software Defined Radio Front-Ends"
- **M.Sc. in Electronics Engineering, University of Aveiro, Portugal** 09/2007-08/2008
  Grade: 14 (out of 20)
  Advisor: Prof. Nuno Borges Carvalho
  Degree Thesis: "Characterization of Systems for Software Defined Radio"
- **5 years Degree in Electronics Engineering, University of Aveiro, Portugal** 09/2000-07/2006
  Grade: 13 (out of 20)
  Final Project: "Project of Wideband Antennas for Terrestrial TV (Analogue and Digital) Reception" with a grade of 17 (out of 20)

OTHER COURSES

- **Advanced Studies in Electrical Engineering, University of Aveiro, Portugal** 09/2008-02/2010
  Grade: 17 (out of 20)
  Program: Ph.D. Curricular Component (60 ECTS)
- **IEEE 1st Annual International Measurement University, Trento, Italy** 08/2008
  Sponsor: IEEE Instrumentation & Measurement Society
  Certification: IEEE CEU program (3 credits)

PROFESSIONAL EXPERIENCE

- **Trainee/Software Developer, Portugal Telecom Inovação, Aveiro, Portugal** 09/2006-04/2007
  Activities: Developing and adjusting an indoor location system based in wireless devices (Wi-Fi)
  Supervisor: Eng. Teresa Soares

RESEARCH & TEACHING ACTIVITIES

VISITING RESEARCHER

- **Tampere University of Technology, Tampere, Finland** 08/2010-09/2010
  Host: Prof. Mikko E. Valkama, Department of Communications Engineering
  Sponsor: COST Action IC0803

RESEARCH PROJECTS

- **Cognitive Radios Adaptable Wireless Transceivers (TACCS)** 01/2010-12/2012
  Sponsor: Fundação para a Ciência e a Tecnologia (FCT), Portugal
  Position: Collaborator
- **High-Speed Point-to-Point Microwave Wireless Links (PANORAMA-Radio)** 01/2009-12/2010
  Sponsor: Quadro de Referência Estratégico Nacional (QREN), Portugal
  Position: Collaborator
- **Localization of People in Indoor Environments (LOPES)** 05/2007-08/2008
  Sponsor: Agência Nacional de Inovação (ADI), Portugal
  Position: Collaborator

TEACHING EXPERIENCE

- **Basic Informatics, University of Aveiro, Portugal** Fall 2010
  Program: Graduation in Management (1st cycle)
- **Basic Informatics, University of Aveiro, Portugal** Fall 2011
  Program: Graduation in Management (1st cycle)

STUDENT SUPERVISION

- **Analog-Digital Measurement System for Software–Defined Radios** 2010/2011
  Institution: University of Aveiro, Portugal
  Student: Diogo C. Ribeiro, M.Sc. student
  Role: Collaborator

SCIENTIFIC ACTIVITIES

AWARDS / DISTINCTIONS

- **Best Student Presentation Award, Belfast, United Kingdom** May 2012
  Sponsor: COST Action IC0803
  Work: "Evaluation of 2nd-Order Bandpass Sampling Receivers for Software Defined Radio"
- **Member of team distinguished with PLUG 2010 Award, Lisbon, Portugal** Nov. 2010
  Sponsor: Associação dos Operadores de Telecomunicações (APRITEL)
  Work: "Cognitive Radios"
- **Third place in GAAS Association PhD Student Fellowship, Rome, Italy** Sept. 2009
  Sponsor: Gallium Arsenide Application Symposium Association
  Work: "PWM Bandwidth and Wireless System Peak-to-Minimum Power Ratio"
- **Finalist in Student Paper Competition of IMS 2012, Atlanta, GA** June 2008
  Sponsor: IEEE Microwave Theory and Techniques Society
  Work: "Mixed Analog-Digital Instrumentation for Software-Defined Radio Characterization"

REVIEWER ACTIVITIES

- **IET Electronics Letters, (9 Reviews)** 2011-2012
- **IEEE Transactions on Circuits and Systems II, (1 Review)** 2012
- **XXVII Spanish Symposium of URSI 2012, (1 Review)** 2012
- **International Conference on Computer Convergence Technology 2011, (1 Review)** 2011

WORKSHOP SEMINARS

- **White Spaces Technological Needs** June 2012
  Authors: N.B. Carvalho, P.M. Cruz, N. Silva, A. Morgado, A. Oliveira, J.N. Vieira, J.P. Borrego
  Location: International Microwave Symposium 2012 Workshop, Montreal, Canada
- **Evaluation of 2nd-Order Bandpass Sampling Receivers for Software Defined Radio** May 2012
  Authors: P.M. Cruz, N.B. Carvalho, M.E. Valkama
  Location: 8th MC Meeting and Workshop of COST IC0803, Belfast, United Kingdom
- **Virtualized Instrumentation for Emergent Radio Technologies** Dec. 2011
  Authors: P.M. Cruz, D.C. Ribeiro, N.B. Carvalho
  Location: Workshop on White Spaces Technologies, Aveiro, Portugal
- **Characterization Challenges for SDR Radios** June 2011
  Authors: N.B. Carvalho, P.M. Cruz
  Location: International Microwave Symposium 2011 Workshop, Baltimore, MA
- **Time-Domain Simulator for a Bandpass Sampling Receiver** Nov. 2010
  Authors: P.M. Cruz, N.B. Carvalho, M.E. Valkama
  Location: 5th MC Meeting and Workshop of COST IC0803, Lausanne, Switzerland
- **Modeling Nonlinear Behavior of Bandpass Sampling Receivers** Feb. 2010
  Authors: P.M. Cruz, N.B. Carvalho
  Location: 4th MC Meeting and Workshop of COST IC0803, Aveiro, Portugal
- **Characterization of SDR Transceivers in Presence of Multisines** Sept. 2009
  Authors: N.B. Carvalho, P.M. Cruz
  Location: European Microwave Week 2009 Workshop, Rome, Italy
- **Characterization of Systems for Software Defined Radio** April 2009
  Authors: P.M. Cruz, N.B. Carvalho
  Location: 2nd MC Meeting and Workshop of COST IC0803, Brno, Czech Republic
- **Signal Clipping Strategies** Oct. 2008
  Authors: N.B. Carvalho, P.M. Cruz
  Location: European Microwave Week 2008 Workshop, Amsterdam, Netherlands
- **The Impact of Signal's PAPR on New Wireless Transmission Chains** June 2008
  Authors: N.B. Carvalho, P.M. Cruz, R. Ferreira
  Location: International Microwave Symposium 2008 Workshop, Atlanta, GA
- **Characterization of Mixed Domain Components for SDR Applications** June 2008
  Authors: N.B. Carvalho, P.M. Cruz, K.A. Remley, K.G. Gard
  Location: International Microwave Symposium 2008 Workshop, Atlanta, GA

LIST OF PUBLICATIONS

BOOKS & BOOK CHAPTERS

[BC1] P.M. Cruz and N.B. Carvalho, "Characterization of Software Defined and Cognitive Radio Front-Ends for Multi-mode Operation" – Chapter in *Microwave and Millimeter Wave Circuits and Systems: Emerging Design, Technologies and Applications*, Edited by A. Georgiadis, H. Rogier, L. Roselli, P. Arcioni, Wiley, November 2012. *(to be published)*

[BC2] P.M. Cruz, H.C. Gomes and N.B. Carvalho, "Receiver Front-End Architectures - Analysis and Evaluation" – Chapter in *Advanced Microwave and Millimeter Wave Technologies Semiconductor Devices Circuits and Systems*, Edited by Moumita Mukherjee, In-Tech, Austria, March 2010.

INTERNATIONAL JOURNALS WITH REFEREE

[J1] P.M. Cruz and N.B. Carvalho, "Wideband Behavioral Model for Nonlinear Operation of Bandpass Sampling Receivers", *IEEE Trans. Microwave Theory and Techniques*, vol. 59, no. 4, April 2011.

[J2] P.M. Cruz, N.B. Carvalho and K.A. Remley, "Designing and Testing Software-Defined Radios", *IEEE Microwave Magazine*, vol. 11, no. 4, June 2010.

INTERNATIONAL CONFERENCES WITH REFEREE

[C1] P.M. Cruz, N.B. Carvalho and M.E. Valkama, “Evaluation of Second-Order Bandpass Sampling Receivers for Software Defined Radio”, *European Microwave Integrated Circuits Conference*, Amsterdam, Netherlands, October 2012. (*to be published*)

[C2] D.C. Ribeiro, P.M. Cruz and N.B. Carvalho, “Corrected Mixed-Domain Measurements for Software Defined Radios”, *European Microwave Conference*, Amsterdam, Netherlands, October 2012. (*to be published*)

[C3] P.M. Cruz and N.B. Carvalho, “Multi-Carrier Wideband Nonlinear Behavioral Modeling for Cognitive Radio Receivers”, *European Microwave Integrated Circuits Conference*, Manchester, United Kingdom, October 2011.

[C4] P.M. Cruz and N.B. Carvalho, “Enhanced Architecture to Increase the Dynamic Range of SDR Receivers”, *IEEE Radio and Wireless Symposium*, Phoenix, AZ, January 2011.

[C5] P.M. Cruz and N.B. Carvalho, “Modeling Band-Pass Sampling Receivers Nonlinear Behavior in Different Nyquist Zones”, *IEEE MTT-S International Microwave Symposium*, Anaheim, CA, May 2010.

[C6] P.M. Cruz and N.B. Carvalho, “Architecture for Dynamic Range Extension of Analog-to-Digital Conversion”, *IEEE International Microwave Workshop Series on RF Front-ends for Software Defined and Cognitive Radio Solutions*, Aveiro, Portugal, February 2010.

[C7] P.M. Cruz and N.B. Carvalho, “PWM Bandwidth and Wireless System Peak-to-Minimum Power Ratio”, *European Microwave Integrated Circuits Conference*, Rome, Italy, September 2009.

[C8] P.M. Cruz and N.B. Carvalho, “PAPR Evaluation in Multi-Mode SDR Transceivers”, *European Microwave Conference*, Amsterdam, Netherlands, October 2008.

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[C10] P.M. Cruz, N.B. Carvalho and K.A. Remley, “Evaluation of Nonlinear Distortion in ADCs Using Multisines”, *IEEE MTT-S International Microwave Symposium Digest*, Atlanta, GA, June 2008.

NATIONAL CONFERENCES

[CN1] P.M. Cruz, N.B. Carvalho and M.E. Valkama, "On the Implementation of a Mixed Frequency-Time Simulator for Band-Pass Sampling Receivers", *Conference on Electronics, Telecommunications and Computers*, Lisboa, Portugal, November 2011.

[CN2] P.M. Cruz, D.C. Ribeiro and N.B. Carvalho, "Virtualized Instrumentation for Emergent Radio Technologies", *5th Congress of Portuguese Committee of URSI*, Lisboa, Portugal, November 2011.

[CN3] D.C. Ribeiro, P.M. Cruz and N.B. Carvalho, "Two-Tone Measurement Technique to apply on Mixed-Domain Instrumentation", *5th Congress of Portuguese Committee of URSI*, Lisboa, Portugal, November 2011.

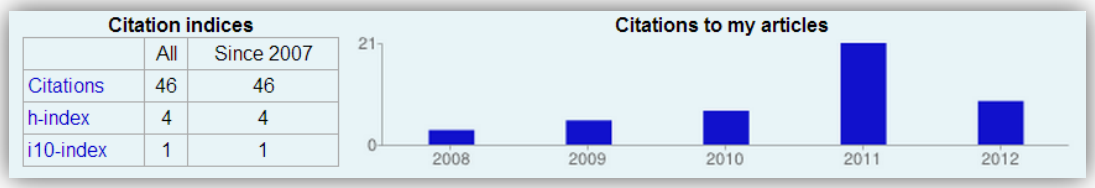
[CN4] P.M. Cruz and N.B. Carvalho, "Characterization of a SDR Front-End Receiver with Multisine Excitations", *7th Conference on Telecommunications – ConfTele 2009*, Santa Maria da Feira, Portugal, May 2009.

[CN5] P.M. Cruz and N.B. Carvalho, "Multi-Mode Receiver for Software Defined Radio", *2nd Congress of the Portuguese Committee of URSI*, Lisboa, Portugal, November 2008.

CITATIONS

Below is provided some information about the total number of citations that have been realized on the previous publications. Two of most important sources have been considered (Google Scholar and Researcher-ID).

- **Google Scholar (http://scholar.google.pt/citations?user=cCiMiEUAAAAJ)** October 2012



- **Researcher-ID (http://www.researcherid.com/rid/B-5892-2011)** October 2012