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System-Level Power Optimization for a $\Sigma\Delta$ D/A Converter for Hearing-Aid Application

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Abstract— This paper deals with a system-level optimization of a back-end of audio signal processing chain for hearing-aids, including a sigma-delta modulator digital-to-analog converter (DAC) and a Class D power amplifier. Compared to other state-of-the-art designs dealing with sigma-delta modulator design for audio applications we take the maximum gain of the modulator noise transfer function (NTF) as a design parameter. By increasing the maximum NTF gain the cutoff frequency of modulator loop filter is increased which lowers the in-band quantization noise but also lowers the maximum stable amplitude (MSA). This work presents an optimal compromise between these. Increased maximum NTF gain combined with a multi bit quantizer in the modulator allows lower oversampling ratio (OSR) and results in considerable power savings while the audio quality is kept unchanged. The proposed optimization impacts the entire hearing-aid audio back-end system resulting in less hardware and power consumption in the interpolation filter, in the sigma-delta modulator and reduced switching rate of the Class D output stage.

Keywords—Sigma-Delta modulator; Interpolation filter; Class D; Hearing aid; low voltage, low power

I. INTRODUCTION

High audio quality, longer operation time and small device size are parameters demanded in hearing-aids today. Optimum balance between the design parameters in every part of a hearing-aid device is therefore of vital importance, making the power consumption one of the crucial parameters for the design. This is also the case of the audio signal processing path, which requires digital-to-analog conversion and power amplification at the back-end to drive the speaker (see Fig.1). As part of the digital-to-analog conversion a digital sigma-delta ($\Sigma\Delta$) modulator with Class D output stage is usually used in

low-voltage low-power audio applications. This eliminates problems with device matching and reduced power efficiency experienced in case Class AB output stage is used [1, 2, 3]. The Class D output stage is usually implemented as an H-bridge (schematic in Fig.1 is simplified) and operates in switched mode. Compared to [1, 2, 3] that use Class AB power stage the Class D allows to perform all signal processing before the output filter in digital domain. Digital design provides the advantage of low-voltage low-power and cost effective implementation and scales down with integrated circuit (IC) technologies of today.

Due to the oversampling nature of the $\Sigma\Delta$ modulator an interpolation filter is needed prior to the modulator. When using a multi-bit $\Sigma\Delta$ modulator, digital pulse width modulation (DPWM) block that turns the $\Sigma\Delta$ signal into symmetrical 1 bit pulse width modulation, is needed.

This paper deals with the power optimization of the system in Fig. 1. Section II provides the design specifications for the $\Sigma\Delta$ modulator. In Section III, optimization approach is proposed. In Section IV $\Sigma\Delta$ modulator designs are compared as an example of the optimization approach. Finally, Section V concludes this work.

II. DESIGN AND FIGURE-OF-MERIT SPECIFICATIONS

A thorough discussion on hearing-aid audio back-end system specification and the $\Sigma\Delta$ modulator is provided in [4]. We assume ideal 16 bit quantization of the system input signal that has band-width (BW) of 10 kHz. This results in signal-to-quantization-noise ratio (SQNR) = 98 dB. The sampling frequency at the system input is $f_{s,in} = 22.05$ kHz. The input signal of the back-end is then up-sampled using an

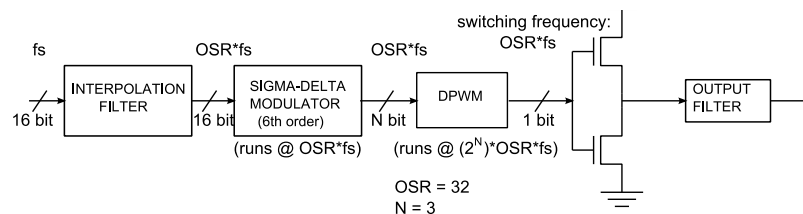


Figure 1. Simplified schematic of the back-end of audio signal processing chain: interpolation filter, $\Sigma\Delta$ modulator, Class-D output-stage and output filter.

interpolation filter [5] and passed to the $\Sigma\Delta$ modulator. The interpolation filter in state-of-the-art designs [1 - 3, 5 - 7] consists of multiple stages. Another requirement is the signal-to-noise-and-distortion ratio (SNDR) at the total output of the back-end of 90 dB. We designed the interpolation filter and the $\Sigma\Delta$ modulator to keep the quality of the audio signal at SNDR = 98 dB so that a margin of 8 dB is left for the performance reduction introduced by the output stage. MSA is also a crucial parameter, the lowest limit is -1.2 dBFS.

Note that we are dealing with a digital $\Sigma\Delta$ modulator in this work and we treat it as a digital filter. This allows us to judge the complexity and power savings using the FOM:

$$FOM = \sum_i b_i \cdot OSR_i \quad (1)$$

Where i is the number of adders in the $\Sigma\Delta$ modulator block, b_i is the number of bits used in individual adders and OSR_i is the oversampling used for the individual adders. In the case of the $\Sigma\Delta$ modulator block OSR_i is the same for all the adders. There are more precise figures of merit for sigma-delta modulators used in other works [2, 8]. However, these figures of merit can be used only after the design has been completed and possibly measured. The advantage of the figure of merit of Eq. 1 is that it allows us to compare different designs to each other early in the design process.

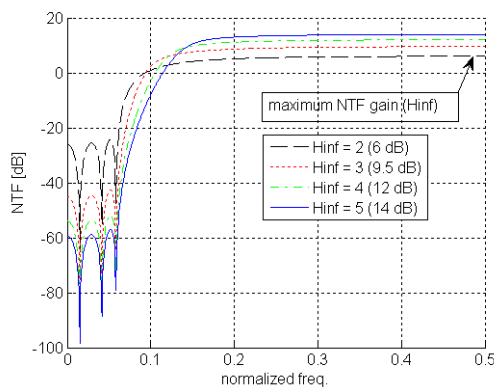


Figure 2. NTF of 6th order $\Sigma\Delta$ modulator with OSR = 8 and 5 bit quantizer. Maximum NTF gain H_{inf} as a parameter.

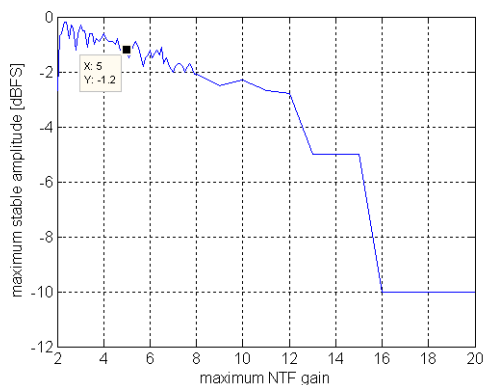


Figure 3. Maximum stable amplitude at $\Sigma\Delta$ modulator input as a function of max. NTF gain.

III. DESIGN OPTIMIZATION APPROACH

In this work we want to optimize the back-end of the audio signal processing chain in Fig. 1 [9] at system level with respect to power. With the Class D output stage being the main power consumer in the system due to the resistance in the output transistors, we aim to reduce its switching frequency. The switching frequency of the Class D stage is the same as the operating frequency of the $\Sigma\Delta$ modulator (see Fig. 1). Thus keeping the OSR of the $\Sigma\Delta$ modulator low helps to lower the power consumption of the Class D stage as well. We were not able to use the optimization approach of [9] where we trade higher modulator order for lower OSR while keeping the SQNR. With high modulator order (6th order, see Fig. 1) this increases the order even further. We tried to design a 12th order modulator with OSR=16 but experienced stability problems. To have a stable modulator with such high order it is needed to have high precision coefficients and integrator adders which results in worse modulator FOM. Such approach leads us away from optimum design. Thus the idea behind further optimization of the $\Sigma\Delta$ modulator and the entire back-end is to keep the modulator order, decrease the modulator OSR and increase the number of bits in its quantizer. To have lower power consumption in the Class-D output stage and have more bits in the quantizer of the $\Sigma\Delta$ modulator is reasonable tradeoff

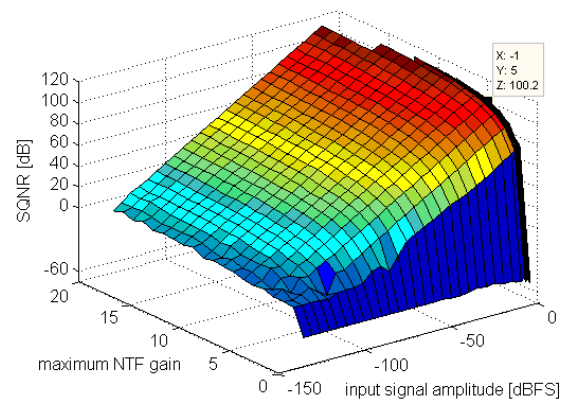


Figure 4. SQNR of the $\Sigma\Delta$ modulator output signal as a function of modulator input signal amplitude and max. NTF gain H_{inf} .

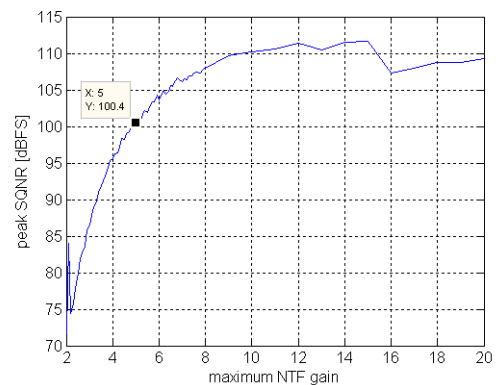


Figure 5. peak SQNR of the $\Sigma\Delta$ modulator output signal as a function of max. NTF gain.

since the $\Sigma\Delta$ modulator is completely digital and thus scales with technology. The same cannot be said about the Class-D output stage. In order not to increase the maximum system clock available given by the DPWM block (see Fig. 1), and at the same time decrease the OSR and keep the modulator at 6th order, combination of OSR = 8 and 5 bit quantizer is needed. However, 6th order modulator with OSR = 8 and 5 bit quantizer does not provide necessary peak SQNR = 98 dB at the output of the modulator, if maximum NTF gain $H_{inf} = 1.5$ is used, as recommended in [8]. As can be seen from the NTF plots in Fig.2, increase of H_{inf} above 1.5 pushes the cutoff frequency of the NTF up. This results in less in-band quantization noise and potentially gives better SQNR. At the same time increase of H_{inf} reduces the MSA which potentially gives worse SQNR (see Fig.3). These two effects contradict each other and need to be further investigated. Fig.4 and Fig.5 show that increase of H_{inf} above 5 allows us to reach peak-SQNR = 100 dB at the output of the modulator at maximum stable input amplitude (MSA) = -1.2 dBFS (Fig.3). Moreover, Fig.4 and Fig.5 show that further increase of H_{inf} reduces the in-band noise at the same rate as the MSA is reduced and results in a wide range where the SQNR is constant. Thus the highest H_{inf} is decided by the point where MSA reaches the limit of -1.2 dBFS (see Fig.3). Therefore our choice of $H_{inf} = 5$ is optimal for combination of $\Sigma\Delta$ modulator parameters of 6th order, OSR = 8 and 5 bit quantizer.

Performing the changes mentioned above allows us to reduce the operating frequency of the $\Sigma\Delta$ modulator and thus switching frequency of the Class D output stage by 87.5% compared to [4] and by 75% compared to the design of Fig. 1. This will result in considerable power savings. Moreover these changes will have a positive impact on the interpolation filter too as oversampling by 8 only is needed compared to oversampling by 64 in [3, 4, 6, 7] and by 32 in Fig. 1. This saves several stages in the interpolation filter operating at high frequency. Using the FOM of Eq.1 for interpolation filter of [4] and [9] we calculate FOM = 118 and FOM = 83 respectively. After the reduction of OSR down to 8 the FOM of the interpolation filter is 58. This is improvement of hardware/power saving by 49% in the interpolation filter compared to [4] and by 30% compared to [9]. With the maximum clock frequency of the DPWM block the same as in Fig. 1, and with power savings in the interpolation filter and in the Class D output stage, the only block of the back-end system that remains to be investigated to see whether or not this optimization approach is power efficient is the $\Sigma\Delta$ modulator. We discuss this in the next section.

IV. $\Sigma\Delta$ MODULATOR DESIGN AND COMPARISON

The modulator in this work is 6th order with OSR = 8, 5 bit quantizer and maximum NTF gain = 5. A model using fixed-point arithmetic was built and simulated in Matlab. The list of coefficients used for the modulator in current design can be seen in Tab. I. The FFT of the $\Sigma\Delta$ modulator fixed-point model's output signal can be seen in Fig. 6. A cascade of resonators with feedback (CRFB) $\Sigma\Delta$ modulator structure is used (see Fig. 7).

TABLE I. $\Sigma\Delta$ MODULATOR CURRENT DESIGN - COEFFICIENT LIST.

Coeff.	Value	Shift/Add	Adders
a ₁	1/8	2 ⁻³	0
a ₂	0.1718	2 ⁻³ +2 ⁻⁵ +2 ⁻⁷ +2 ⁻⁸	3
a ₃	0.2243	2 ⁻² -2 ⁻⁵ +2 ⁻⁸	2
a ₄	0.1604	2 ⁻³ +2 ⁻⁵ +2 ⁻⁸	2
a ₅	0.4992	2 ⁻¹	0
a ₆	0.1203	2 ⁻³ -2 ⁻⁷ +2 ⁻⁸	1
b ₁	1/8	2 ⁻³	0
c ₁	1/4	2 ⁻²	0
c ₂	1/2	2 ⁻¹	0
c ₃	1/2	2 ⁻¹	0
c ₄	2	2 ¹	0
c ₅	1/2	2 ⁻¹	0
c ₆	8	2 ³	0
g ₁	0.0351	2 ⁻⁵ +2 ⁻⁸ -2 ⁻¹¹	2
g ₂	0.1341	2 ⁻³ +2 ⁻⁷	1
g ₃	0.2652	2 ⁻² +2 ⁻⁷ +2 ⁻⁸	2

The fixed-point arithmetic model performs digital operations exactly as a VHLD design does. Thus the fixed-point arithmetic model can be directly used to judge the complexity of the $\Sigma\Delta$ modulator. Taking the Matlab fixed-point models and calculating the FOM according to Eq.1 gives data and FOM in Tab. II, clearly showing better (lower) FOM compared to the design of [4] and of Fig. 1 [9]. Expressing the current consumption of the back-end as sum of the currents needed in individual blocks we write:

$$I_{total} = I_{int} + I_{SDM} + I_{DPWM} + I_{dr} \quad (2)$$

Where I_{int} is the current needed in the interpolation filter (see Fig. 1), I_{SDM} is the current of the $\Sigma\Delta$ modulator, I_{DPWM} is the current of the DPWM block and I_{dr} is the current of the

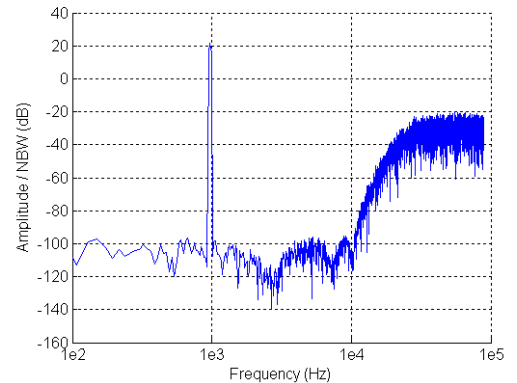


Figure 6. FFT spectrum of the $\Sigma\Delta$ modulators output signal. For the FFT Hann window was used. The FFT is 8192 points (NBW = 1.8311e-04)

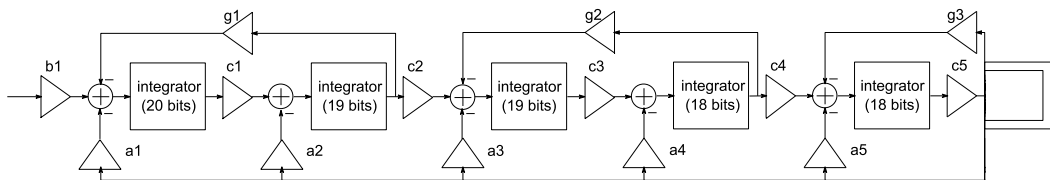


Figure 7. CRFB architecture of 6th order $\Sigma\Delta$ modulator with OSR = 8 and 5 bit quantizer.

Class D driver (power amplifier). In Section III we explained that using the proposed optimization I_{int} will be lowered by 30%, I_{dr} will be lowered by 75% and I_{DPWM} will remain the same compared to Fig. 1 [9]. Table II shows that I_{SDM} will be lowered by 60%. Thus in total there are considerable power savings achieved by the proposed optimization approach.

Table III. shows a comparison with other audio DAC designs for low-voltage low power applications. Exact comparison can not be performed as the FOM used in the reference works requires finished design. Moreover [1, 2, 3] use Class-AB power stage and require analog $\Sigma\Delta$ modulator which further complicates comparison at early design stage. Nevertheless trends of the low-voltage low power audio back-end designs can be seen in Table III. We note that one of the trends is to target SNDR = 90 dB [4, 6, 7] at the total output of the system. What most of the $\Sigma\Delta$ modulator reference designs have in common is the choice of system-level parameters of 3rd order and OSR around 64 with 3 bit quantizer [2, 3, 4, 6]. In case 1 bit quantizer is used a tradeoff is made and order of the modulator is increased from 3 to 4 to achieve the same audio quality [2, 7].

TABLE II. $\Sigma\Delta$ MODULATOR COMPARISON WITH THE DESIGN OF [4] AND [9].

	Order	Bit	OSR	H_{inf}	Adders	Pk. SQNR [dB]		FOM
						ideal	quantized	
[4]	3	3	64	1.5	12	106	98	193
[9]	6	3	32	1.5	22	105	98	192
This work	6	5	8	5	29	100	98	77

TABLE III. SYSTEM COMPARISON.

Design	Analog/Digital	Power Stage	BW [kHz]	OSR	Order	Bit	SNDR [dB]
[1]	Analog	Class AB	24	128	3	3	69
[3]	Analog	Class AB	20	64	3	3	82
[2]	Analog	Class AB	20	50	4	1	73
[4]	Digital	Class D	10	64	3	3	Target is 90
[6]	Digital	Class D	20	64	3	3	90
[7]	Digital	Class D	10	64	4	1	85

We note that a lower OSR directly reduces the operating frequency of the $\Sigma\Delta$ modulator, simplifies the interpolation filter and reduces the switching frequency of the Class D power amplifier. Thus designs with lower OSR, such as proposed in

this work, clearly consume less power. If, at the same time, the audio quality is kept unchanged the design is more efficient and has lower power consumption in total.

V. CONCLUSION

In this work we optimized the back-end path of the audio signal processing path with respect to power consumption. Lower OSR directly reduces the operating frequency of the $\Sigma\Delta$ modulator, simplifies the interpolation filter and reduces the switching frequency of the Class D power amplifier. If, at the same time, the audio quality is kept unchanged, the audio back-end is more efficient and clearly consumes less power. We trade lower OSR of the $\Sigma\Delta$ modulator for higher number of bits in its quantizer and higher maximum gain of the modulator NTF. Overall the power consumption of the entire back-end system is considerably reduced showing that trading lower OSR for higher number of bits in the quantizer and higher maximal NTF gain is an approach to be considered in low-voltage, low-power portable audio applications.

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