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Modeling, Simulation, and Validation of a Power SiC BJT

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Modeling, Simulation, and Validation of a Power SiC BJT

Tanya Gachovska, *Student Member, IEEE*, Jerry L. Hudgins, *Fellow, IEEE*, Angus Bryant, *Member, IEEE*, Enrico Santi, *Senior Member, IEEE*, H. Alan Mantooth, *Fellow, IEEE*, and Anant K. Agarwal, *Fellow, IEEE*

***Abstract*—This paper presents a physics-based model of a silicon carbide bipolar junction transistor and verification of its validity through experimental testing. The Fourier series solution is used to solve the ambipolar diffusion equation in the transistor collector region. The model is realized using MATLAB and Simulink. The experimental results of static operation and also the simulated and experimental results of switching waveforms are given.**

***Index Terms*—Silicon carbide (SiC) bipolar junction transistor (BJT), power semiconductor modeling.**

NOMENCLATURE

A	Device area (cm^2).
C_{J1} and C_{J2}	Capacitance of the depletion layers (F).
D	Ambipolar diffusivity (cm^2 s^{-1}).
D_p and D_p	Electron and hole diffusivities (cm^{2}s^{-1}).
ε	Dielectric permittivity of SiC (F/cm).
h_n	N^+ emitter recombination parameter (cm^4 s^{-1}).
h_p	P^+ emitter recombination parameter (cm^4 s^{-1}).
I_B	Base current (A).
I_C	Collector current (A).
I_{disp1} and I_{disp2}	Displacement currents at junctions J_1 and J_2 (A).
I_{L0}	Initial inductor current (A).
I_{n0}, I_{n1}, and I_{n2}	Electron currents at junctions J_0, J_1, and J_2 (A).
I_{p0}, I_{p1}, and I_{p2}	Hole currents at junctions J_0, J_1, and J_2 (A).
K_{FV}	Feedback constant.
L_L	Load inductance (H).
L_S	Stray inductance (H).
M	Number of terms of the Fourier series.
μ_n and μ_p	Electron and hole mobilities of SiC (cm^2 V^{-1} s^{-1}).
n_{B0} and n_{B1}	Electron concentrations at the two boundaries of the base region (cm^{-3}).
N_E	Emitter doping level (cm^{-3}).
N_C	Collector doping level (cm^{-3}).
n_i	Intrinsic carrier concentration of SiC (cm^{-3}).
N_N^-	N^- region doping concentration (cm^{-3}).
P_B	Doping concentration of the base (cm^{-3}).
$p(x, t)$	Excess carrier concentration in the drift region (cm^{-3}).
p_{x1} and p_{x2}	Excess carrier concentrations at the two boundaries of the drift region (cm^{-3}).
R_L	Load resistance (Ω).
R_S	Resistance of the wires (Ω).
Q_B	Total electron charge in the base (C).
τ	High-level carrier lifetime within the drift region (s).
τ_{BHL}	High-level lifetime in the P^+-base region (s).
τ_p	Minority lifetime in N^+ emitter (s).
q	Unit electron charge (1.6×10^{-19}C).
V_{BE}	Base–emitter voltage (V).
V_{CE}	Collector–emitter voltage (V).
V_{CSR}	Voltage across the carrier storage region (V).
V_{d1} and V_{d2}	Voltages across the N^-N^+ and N^-P^+ depletion layers (V).
V_{dc}	External dc voltage (V).
V_{J0}, V_{J1}, and V_{J2}	Voltages across junctions J_0, J_1, and J_2 (V).
v_{sat}	Saturation velocity of SiC (cm/s).
V_T	Thermal voltage—kT/q (T is the temperature (K) and k is the Boltzmann constant eV/K) (V).
W_B	Base width (cm).

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W_{d1} and W_{d2} — Widths of the N^-N^+ and N^-P^+ depletion layers (cm).
W_{N^-} — Drift region width (cm).
x_1 and x_2 — Boundary positions of the carrier storage region (cm).

I. Introduction

In recent years, silicon carbide (SiC) has been recognized as a potential candidate material to realize high-performance switches in the high-power, high-frequency, and high-temperature area due to its superior material properties such as wider bandgap, higher saturation velocity, higher electric field strength, and higher thermal conductivity compared to Si and GaAs.

The SiC Schottky diode was the first commercially available power switch [1]. The SiC power MOSFET has drawn a lot of attention due to the advantages of a unipolar device and ease of gate control. However, the poor reliability of MOS-channel mobility and the dielectric oxide, especially in high electric fields, has greatly hampered the development of the SiC MOSFET [2]. Bipolar devices such as the power bipolar junction transistor (BJT), gate turn-off thyristor (GTO), and insulated gate bipolar transistor (IGBT) provide further utilization of SiC material in high-power and high-temperature applications.

BJTs based on 4H-SiC have the advantages of no gate oxide and low on-state voltage in the lightly doped drift region due to double-sided high-level injection. The first 6H-SiC BJT with a blocking voltage of 50 V and a common-emitter current gain of 4–8 was fabricated in 1978 [3]. The first 4H-SiC BJT was reported to have a capability of open-base blocking voltage rated at 800 V and a common-emitter current gain (the ratio of the collector current to the base current) of 9 [4]. Recently, the 4H-SiC NPN BJT with a 6-kV open-base blocking voltage (V_{CEO}) and 28 mΩ cm^2 specific on-resistance has been reported with a corresponding common-emitter current gain of 3 [5].

In power electronics, SiC BJTs could be used as switches having two states: ON and OFF. These states are important in determining the efficiency and applicability of the BJT, while the transient processes between the two states have an important role in determining the energy losses, reliability, and performance of the circuit.

The objective of this study is modeling, simulation, and validation of the transient processes in a 4H-SiC BJT (1200 V-5 A SiC BJT, Cree, Durham, NC).

II. Modeling

Although SiC power BJTs have been fabricated and measured for several years, there are no physics-based models appropriate for circuit designers. The few models in the public domain have dealt with characterization of the current gain [6]. In this section, the development and implementation of a level-3 physics-based model [7] of a SiC BJT based on a Fourier series solution of the ADE equation using MATLAB and Simulink is presented.

The SiC BJT is simulated under inductive load switching condition. The circuit schematic is shown in Fig. 1. A freewheeling high-voltage SiC diode is employed in the simulation model. Table I provides the BJT parameters, as provided by the manufacturer, used in the simulation and Fig. 2 presents the structure of the SiC BJT. The carrier lifetimes were estimated based on experimental switching waveforms.

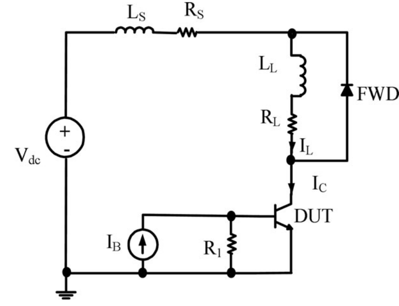

Fig. 1. Schematic of a switching test circuit used for experiments and simulation.

TABLE I
BJT Parameters

Parameters	Units	Definition	Value
A	cm^2	Active area of the device	0.01
W_{N^-}, W_B	μm	Thickness of N^- and P^+	40, 0.9
N_{N^-}, P_B, N_C	cm^{-3}	Doping of N^-, P^+, and N^+	1.1x10^{15}, 2x10^{17}, 1.2x10^{19}
τ_p, τ_n	μs	Minority lifetime in N^- and P^+	0.02, 0.155
μ_n, μ_p	cm^{2}V^{-1}s^{-1}	Electrons and hole mobility	900, 90

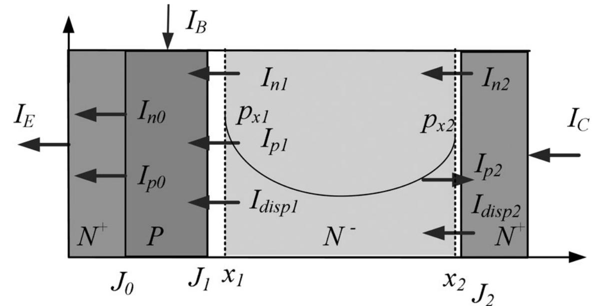

Fig. 2. Cross-sectional view of 4-kV 4H-SiC power BJT showing layer thicknesses (not to scale) and doping concentrations.

The circuit parameters listed in Table II are used for simulation of the SiC BJT under clamped inductive switching load.

The Fourier-series-based electrical model for power devices has been thoroughly introduced in [8]–[10]. The basic idea is to solve the ADE through a Fourier-series expansion.

The basic 1-D structure of the SiC BJT is illustrated in Fig. 3. The BJT is divided into four regions: the N^+ emitter, P-base, N^- drift region, and N^+ collector region. The external and internal electron and hole currents are indicated for each region.

A. N^+ Emitter Region

The N^+ emitter layer can be simply characterized as a hole sink. The hole current at junction J_0 is obtained by the equation

$$I_{p0} = qAh_n n_{B0} P_B. \tag{1}$$

TABLE II
CIRCUIT PARAMETERS FOR EXPERIMENTS AND SIMULATIONS

Parameters	Units	Value
V_{dc}	V	450
R_1	Ω	10^9
R_S/L_S	Ω/nH	1/330
R_L/L_L	Ω/mH	16/33

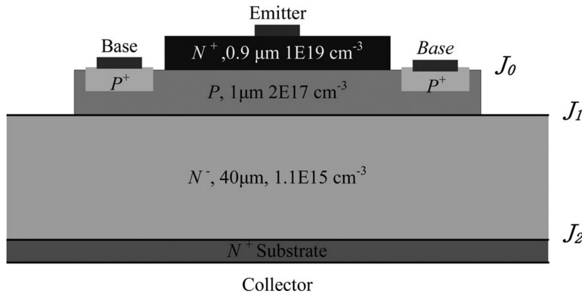

Fig. 3. 1-D cross section used for modeling the SiC BJT showing the hole and electron currents in each region.

The N^+ emitter recombination parameter h_n depends on emitter properties such as doping level N_E, hole diffusivity D_p, and hole minority lifetime τ_p

$$h_n = \frac{N_E}{n_i^2}\sqrt{\frac{D_p}{\tau_p}}. \tag{2}$$

The electron current component at junction J_0 is determined by

$$I_{n0} = I_C - I_{p0}. \tag{3}$$

The voltage drop across the junction J_0 is

$$V_{j0} = V_T \ln\left(\frac{n_{B0}(n_{B0}+P_B)}{n_i^2}\right). \tag{4}$$

B. P-Base Region

The P-base region is used to find the boundary current at junction J_1. The lumped charge method is used to model the charge behavior in the base region due to its moderate doping level and comparatively narrow base width. The injected carrier distribution in the base region during conduction is shown in Fig. 4.

Using the continuity equation for the base region, the injected minority carrier charge is described by the relation

$$\frac{dQ_B}{dt} + \frac{Q_B}{\tau_{\mathrm{BHL}}} = I_{n0} - I_{n1} = I_B + I_{p1} + I_{\mathrm{disp1}} - I_{p0} \tag{5}$$

where τ_{BHL} is the high-level lifetime in the P-base region.

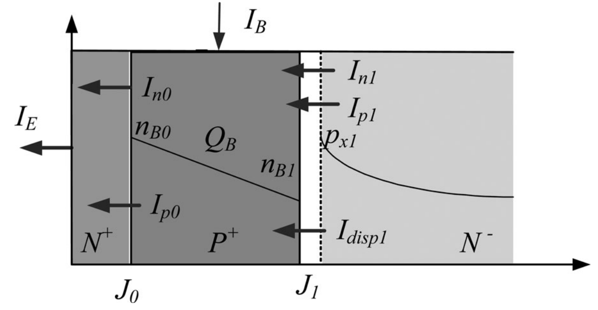

Fig. 4. Charge distribution and boundary current components in the P-base.

The total electron charge in the base is expressed as

$$Q_B = \frac{n_{B0}+n_{B1}}{2} qAW_B \tag{6}$$

where n_{B0} is the electron concentration at the base region boundary on the emitter side and W_B is the base width. The electron concentration at the base region boundary on the collector side, n_{B1}, is related to the excess carrier concentration p_{x1} by the doping concentration of the base P_B by the equation

$$n_{B1} = \frac{p_{x1}^2}{P_B}. \tag{7}$$

Since the diffusion length in the base region is much greater than the base width, the gradient of the electron concentration is approximately linear, giving the electron current at the base–collector junction, J_1, as

$$I_{n1} = qD_n A\frac{n_{B0}-n_{B1}}{W_B}. \tag{8}$$

The base–emitter voltage V_{BE} is calculated by the equation

$$V_{BE} = V_T \ln\left(\frac{n_{B0}P_B}{n_i^2} + 1\right). \tag{9}$$

C. N^- Drift Region (Collector)

The voltage drop in this region is calculated during the ON state. The injected excess carrier concentration is determined by the ADE. As for all power switches, high-level injection and quasi-neutral conditions exist. Under high-level injection conditions, the ADE describes the carrier dynamics in the majority of this region

$$D\frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{\tau} + \frac{\partial p(x,t)}{\partial t} \tag{10}$$

where D is the ambipolar diffusion coefficient, τ is the high-level carrier lifetime within the drift region, and $p(x, t)$ is the excess carrier concentration. The Fourier-series solution of the excess carrier distribution has been proposed in [11] as the solution of the second-order partial differential diffusion equation. It is converted into an infinite set of first-order linear differential equations [solutions in ([11])]

$$p(x,t) = p_0(t) + \sum_{k=1}^{\infty} p_k(t)\cos\left[\frac{k\pi(x-x_1)}{x_2-x_1}\right] \tag{11}$$

where

$$p_0(t) = \frac{1}{x_2 - x_1}\int_{x_1}^{x_2} p(x,t)dx$$
$$p_k(t) = \frac{2}{x_2 - x_1}\int_{x_1}^{x_2} p(x,t)\cos\left(\frac{k\pi(x-x_1)}{x_2-x_1}\right)dx. \quad (12)$$

The solution to the ADE is given by the following first-order differential equations as each of them refers to a harmonic $p_k(t)$ of the total minority carrier density $p(x,t)$:

for $k = 1, 2, 3 \ldots$

$$\frac{2D}{x_2 - x_1}\left[\left.\frac{\partial p(x,t)}{\partial x}\right|_{x_2}(-1)^k - \left.\frac{\partial p(x,t)}{\partial x}\right|_{x_1}\right]$$
$$= \frac{dp_k(t)}{dt} + \left[\frac{1}{\tau} + \frac{Dk^2\pi^2}{(x_2-x_1)^2}\right]p_k(t)$$
$$+ \frac{2}{x_2 - x_1}\left(\sum_{\substack{n=1\\n\neq k}}^{\infty}\frac{n^2}{n^2-k^2}\left[\frac{dx_1}{dt} - (-1)^{n+k}\frac{dx_2}{dt}\right]p_n(t)\right.$$
$$\left.+ \frac{p_k}{4}\left(\frac{dx_1}{dt} - \frac{dx_2}{dt}\right)\right)$$

for $k = 0$

$$\frac{D}{x_2 - x_1}\left[\left.\frac{\partial p(x,t)}{\partial x}\right|_{x_2} - \left.\frac{\partial p(x,t)}{\partial x}\right|_{x_1}\right] = \frac{dp_0(t)}{dt} + \frac{p_0(t)}{\tau}$$
$$+ \frac{1}{x_2 - x_1}\sum_{n=1}^{\infty}\left[\frac{dx_1}{dt} - (-1)^n\frac{dx_2}{dt}\right]p_n(t) \quad (13)$$

$$p_{x_1} = \sum_{k=1}^{n} p_k \quad \text{and} \quad p_{x_2} = \sum_{k=1}^{n}(-1)^k p_k.$$

The solution to the ADE is determined by using the boundary conditions at the edges of the charge storage region (CSR). The representation requires the width of the undepleted region and the hole and electron currents at the boundaries of the drift region, which give the gradients of the carrier concentrations at x_1 and x_2, respectively. The required boundary conditions are given in

$$\left.\frac{\partial p}{\partial x}\right|_{x_1} = \frac{1}{2q}\left(\frac{J_n}{D_n} + \frac{J_p}{D_p}\right)\bigg|_{x_1} \text{ and } \left.\frac{\partial p}{\partial x}\right|_{x_2}$$
$$= \frac{1}{2q}\left(\frac{J_n}{D_n} + \frac{J_p}{D_p}\right)\bigg|_{x_2}. \quad (14)$$

The displacement currents I_{disp1} and I_{disp2} are due to the changing depletion widths at junctions J_1 and J_2

$$I_{\mathrm{disp1}} = C_{J1}\frac{dV_{d1}}{dt} = \varepsilon A\frac{1}{W_{d1}}\frac{dV_{d1}}{dt}$$
$$I_{\mathrm{disp2}} = C_{J2}\frac{dV_{d2}}{dt} = \varepsilon A\frac{1}{W_{d2}}\frac{dV_{d2}}{dt}. \quad (15)$$

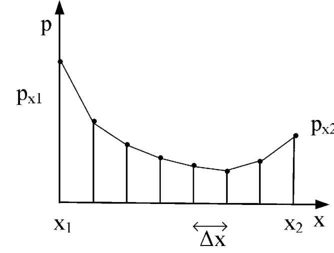

Fig. 5. Carrier distribution in the lightly doped region.

The voltages across the N^-N^+ and N^-P^+ depletion layers, V_{d1} and V_{d2}, are calculated by the following equations:

$$V_{d1} = \begin{cases} 0 & \text{if } p_{x1} > 0 \\ -K_{FV}p_{x1} & \text{otherwise} \end{cases}$$
$$V_{d2} = \begin{cases} 0 & \text{if } p_{x1} > 0 \\ -K_{FV}p_{x2} & \text{otherwise.} \end{cases} \quad (16)$$

The feedback constant K_{FV} is set to 10^{-12}, which gives good convergence and minimal error [12]. The associated depletion widths W_{d1} and W_{d2} are calculated using a step doping concentration change on each side of the junction

$$W_{d1} = \sqrt{\frac{2\varepsilon V_{d1}}{qN_{N^-} + (|I_c|/Av_{\mathrm{sat}})}}$$
$$W_{d2} = \sqrt{\frac{2\varepsilon V_{d2}}{qN_{N^-} + (|I_c|/Av_{\mathrm{sat}})}}. \quad (17)$$

The boundary positions x_1 and x_2 are calculated by

$$x_1 = W_{d1}$$
$$x_2 = W_{N^-} - W_{d2}. \quad (18)$$

The voltages at junctions J_1 and J_2 are

$$V_{j1} = 2V_T \ln\left(\frac{p1}{n_i}\right)$$
$$V_{j2} = V_T \ln\left(\frac{p_{x2}}{N_C}\right). \quad (19)$$

The voltage drop in the carrier storage region V_{CSR} is calculated based on the injected carrier concentration. The 1-D charge distribution in the lightly doped (carrier storage, CSR) region during the ON state is illustrated in Fig. 5.

The CSR is divided into equal width segments with the number of segments (M) being the same as the number of terms in the truncated Fourier series. The carrier distribution at every point is generated through the inverse Fourier transformation, while the carrier distribution between two points is a linear interpolation. Based on [11], the voltage drop in the region V_{CSR}

at any time is calculated by

$$V_{\mathrm{CSR}} \approx \frac{I_C}{qA(\mu_n+\mu_p)}\frac{x_2-x_1}{M-1}\sum_{K=0}^{M-1} \times\left[\frac{1}{p_{T(k)}-p_{T(k-1)}}\ln\left(\frac{p_{T(k)}}{p_{T(k-1)}}\right)\right] + V_T\left(\frac{\mu_n-\mu_p}{\mu_n+\mu_p}\right)\ln\left(\frac{p_{x2}}{p_{x1}}\right) \quad (20)$$

where the carrier distribution $p_{T(k)}$ is calculated as

$$p_{T(k)} = p\left(x_1+\frac{k(x_2-x_1)}{M-1}\right)+\frac{\mu_n N_B}{\mu_n+\mu_p}. \quad (21)$$

D. N^+ Collector Region

The N^+ collector region is similar to the N^+ emitter region as it is also a hole sink. The hole current at junction J_2 is obtained by the equation

$$I_{p2} = qAh_n p_{x2}^2. \quad (22)$$

The electron current at junction J_2 is

$$I_{n2} = I_c + I_{p2} - I_{\mathrm{disp2}}. \quad (23)$$

E. Voltage Drop

The voltage drop V_{CE} across the high-power SiC BJT is comprised of six components including voltages across junctions J_0, J_1 and pseudojunction J_2, the voltage across the two depletion regions V_{d1} and V_{d2}, and the voltage across the carrier storage region V_{CSR}

$$V_{CE} = V_{j0}+V_{j1}+V_{j2}+V_{d1}+V_{d2}+V_{\mathrm{CSR}}. \quad (24)$$

III. Realization in Simulink

The model of the high-power SiC BJT is implemented using MATLAB incorporated with Simulink. It is straightforward to couple Simulink to the numerical algorithm to solve differential equations [13]. The MATLAB program is used to input the basic parameters used by the Simulink program. The input parameters for the Simulink model are the device geometry parameters, the doping concentrations in each region (assumed to be uniform), charge carrier diffusion coefficients, and minority carrier lifetimes of different regions. SiC material parameters, such as hole and electron mobilities, dielectric permittivity, carrier saturation velocity, and the intrinsic carrier concentration (at 300 K), are also needed.

The implementation of the behavior of the BJT in Simulink requires use of a stiff solver due to the widely different time constants present in the model. Suitable solvers for simulation of power semiconductor devices are ode15s and ode23tb [14]. The configuration parameters chosen for the SiC BJT model are solver 23s (stiff/Mod. Rosenbrock); the maximum and minimum step sizes are, respectively, 10^{-6} and 10^{-120} s. The initial step size is set to "auto." The relative and absolute tolerances are set to be 10^{-3} and 10^{-5}, respectively. The simulation advanced options are set to use inline parameters, which means that the

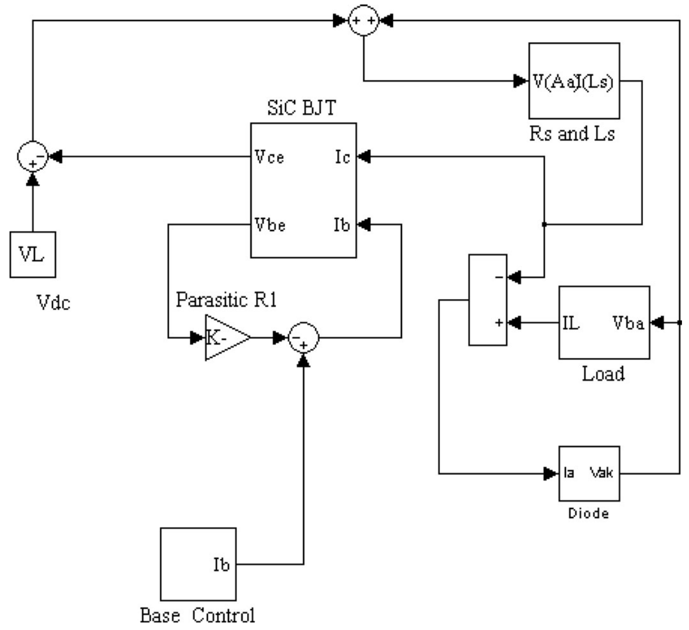

Fig. 6. Switching test circuit used for experiments of a SiC BJT (see Fig. 1) implemented on Simulink.

parameters are fixed during a simulation run. The zero-crossing control is set to be "disable all."

The electrical test circuit (see Fig. 1) of the SiC BJT under clamped inductive switching is realized in the MATLAB/Simulink environment. The diagram is presented in Fig. 6.

The high-power SiC BJT Simulink model is presented in Fig. 7. It has two inputs, collector and base currents, and two outputs, base–emitter and collector–emitter voltages. The BJT subsystem further contains embedded subsystems of the N^- drift region, the P-base, the N^+N^- pseudojunction, N^+ emitter, and a sum for the total voltage drop.

The N^+ emitter subsystem is used to calculate the voltage drop at junction J_0 using (4).

The P-base subsystem is used to calculate the current I_{n1}, voltage V_{BE}, and minority carrier concentration n_{B0} at junction J_0 by using (5)–(9).

The N^- drift region subsystem presented in Fig. 8 is the most important and complicated subsystem in the power BJT model. It consists of four subsystems: carrier storage region (CSR), feedback, drift region voltage drop, and displacement current.

The CSR subsystem provides the solution to the ADE, (10), by using the Fourier solution; (13); and the boundary conditions of (14). The feedback subsystem uses the output data from the CSR subsystem, the charge carrier densities p_{x1} and p_{x2}, as inputs. These carrier densities are used to determine V_{d1} and V_{d2} using (16). The boundary positions x_1 and x_2 are calculated using (17) and (18). They are input signals to the CSR subsystem, and also to the displacement current subsystem.

The value for the carrier densities p_{x1} and p_{x2} are limited to the minimum of n_i and used to calculate the junction voltage V_{j1} and V_{j2} using (19).

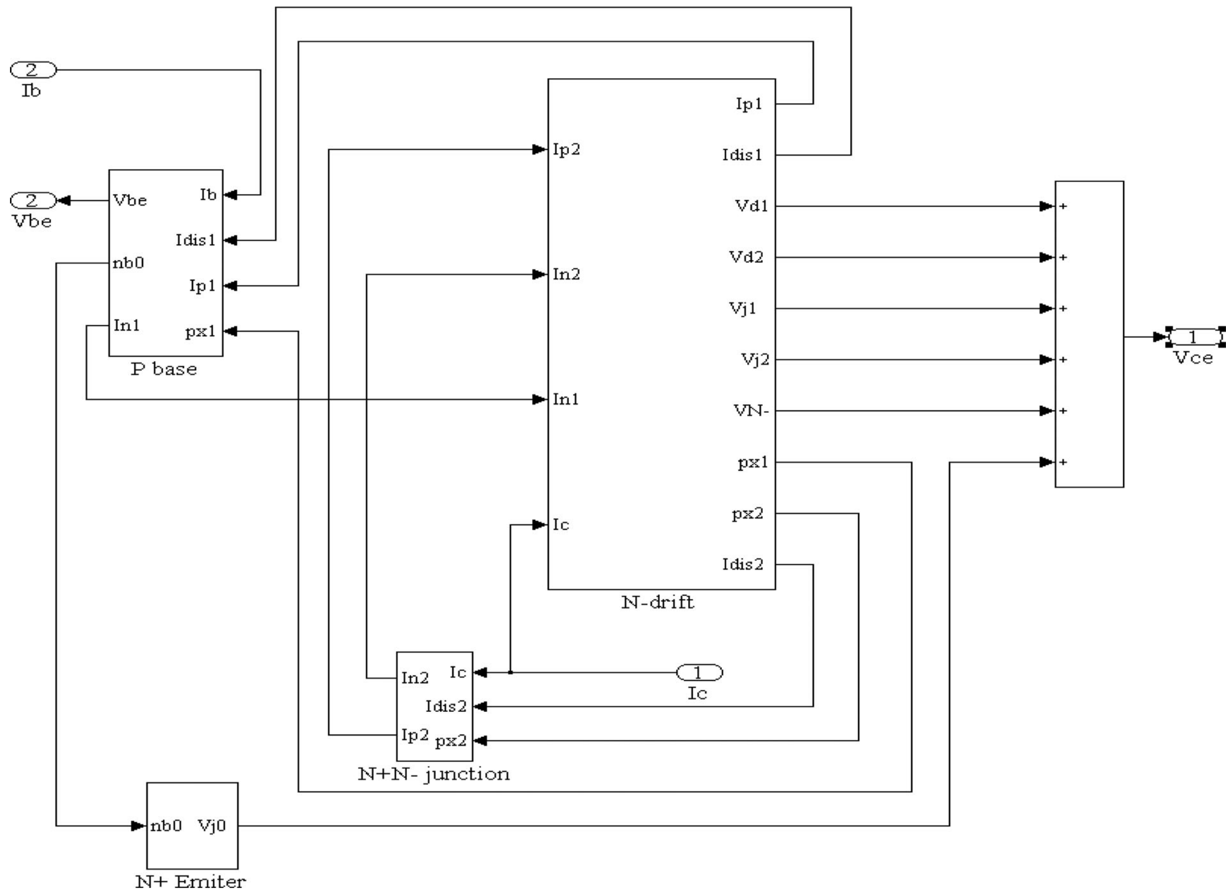

Fig. 7. SiC BJT subsystem implemented on Simulink.

The displacement current subsystem calculates the displacement currents at junctions J_1 and J_2 implementing (15). The drift region voltage drop subsystem uses the parameters of the other subsystems and calculates the voltage drop in the storage region using (20) and (21).

The N^+N^- junction subsystem calculates I_{n2} and I_{p2}; (22) and (23).

The total voltage V_{CE} is given as a sum the junction, the drift region, and the depletion layer voltages from (24).

IV. Measurement and Simulation Result of SiC BJT

To evaluate the behavior of the power semiconductor switches, two basic tests are usually employed: a static test and a dynamic test [15]. Generally, the static measurement is used to validate dc current and voltage characteristics while the dynamic test is used for measuring transient switching behavior.

The static measurement includes the *I–V* and *C–V* characteristics of semiconductor devices under dc conditions, breakdown voltage, and on-state voltage drop. The BJT dies used for the measurements are rated at 1200 V-5A. The *I–V* curves are measured with a curve tracer, Tektronix TEK 371A.

The measured common emitter *I–V* curves at room temperature for two different ranges of collector emitter voltage V_{CE} 0–2 V and 0–10 V are plotted in Fig. 9. The base current is increased from 0 to 90 mA in steps of 10 mA. Typically increasing the collector–emitter voltage when the transistors are operating in the active region results in a slight positive slope due to the Early effect. Instead, for the high-power SiC BJTs, it was observed that the collector current remained constant for low-base current values ($I_B < 50$ mA). For base currents higher than 50 mA, an increasing V_{CE} leads to a decrease in collector current. This is thought to be due to self-heating, which reduces the carrier mobility, and from increased effects due to surface states in these small-area devices [15]. The dc characteristics are only included as supplemental information for the reader. The core of the work was to extend previously developed Si IGBT models to SiC BJT for future converter designs. Therefore, modeling the switching operations is of prime importance.

The experimental and simulation results of the inductive switching tests on the SiC BJT at 450 V are presented in Fig. 10. It can be noticed that there is a small discrepancy between the experimental and simulation results during turn-on and turn-off. This discrepancy between the measured and simulated collector currents is probably caused by the differences in the freewheeling diode used in the model as compared to the experiments. The switching experiment was done using a high-voltage Schottky diode C3D20060, while during the simulation a power SiC PN^-N^+ diode model was used. The details of the diode model are given in [11] and [16]. The intent of using the pin diode structure was to verify the robustness of the device models

Fig. 8. N^{-} drift region subsystem of the SiC BJT model.

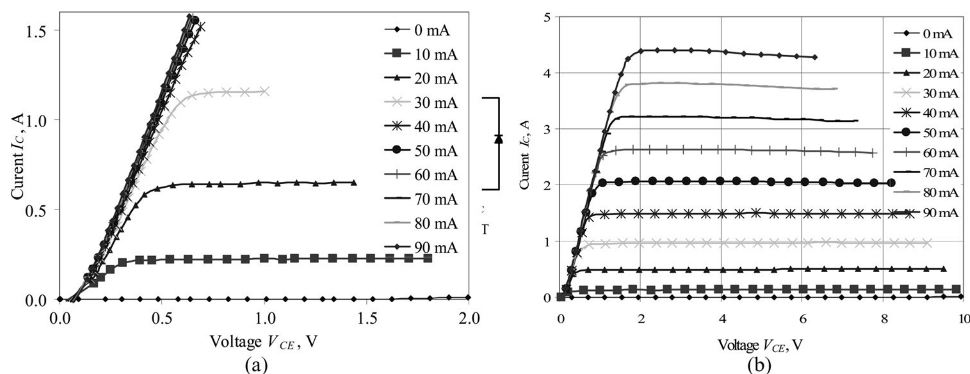

Fig. 9. Common-emitter *I–V* curve of SiC BJT at room temperature: (a) $V_{CE} = 0$–2 V; (b) $V_{CE} = 0$–10 V.

through convergence of the simulation to the correct results when using more than one power device. The focus in this study was on the BJT behavior, so only the diode recovery was important for a correct description of the BJT behavior. Hence, the recovery time of the modeled SiC $PN^{-}N^{+}$ diode was adjusted to match the reverse recovery behavior of the Schottky diode.

From the results of the switching tests, it can be noted that there was approximately a 40-ns rise-time during collector

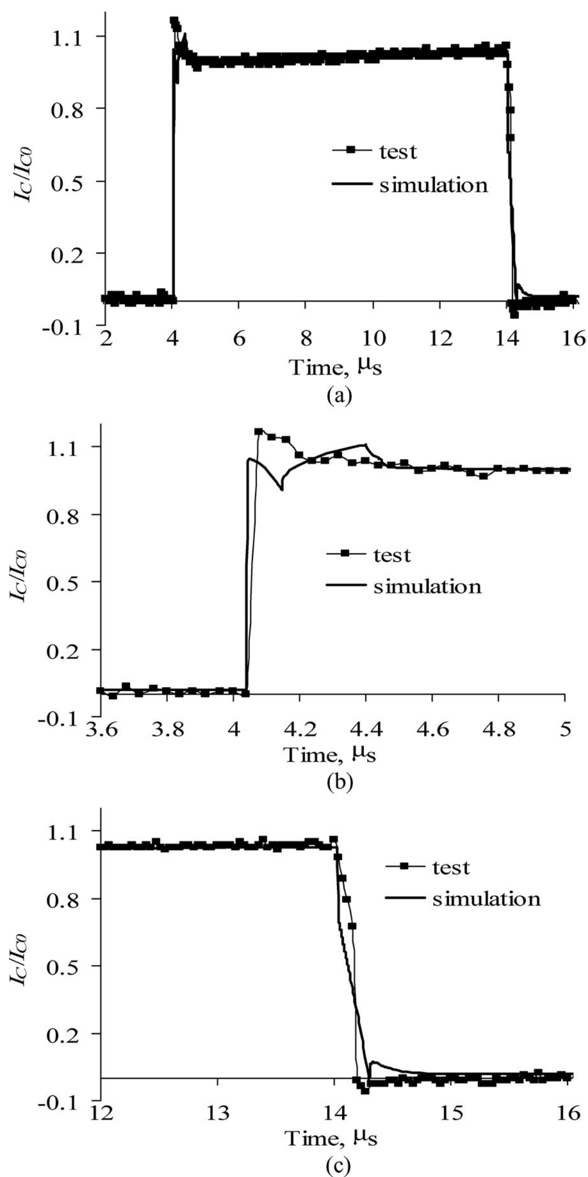

Fig. 10. Switching characteristics of the ratio of the collector current I_C/I_{C0} of SiC BJT at 450 V and $I_{C0} = 2.7$ A: (a) pulse; (b) turn-on; and (c) turn-off.

current turn-on and approximately a 200-ns fall-time during turn-off. Similar results are given in [17].

V. Conclusion

At the current density switched, 400 A/cm^2, the BJT exhibits about a 2-V forward collector–emitter drop. This is about 0.5 V larger than in a Si IGBT rated for the same breakdown. However, at higher breakdown ratings, the SiC BJT should exceed the Si IGBT performance in internal power loss and exhibit superior thermal behavior, both in junction temperature and thermal conductivity.

It should also be noted that the SiC BJT does not exhibit a quasi-saturation region as is typical in Si power bipolar transistors. It is yet to be determined if SiC BJTs exhibit second breakdown effects as their Si counterparts do. The devices tested seem robust and not prone to turn-off failure during inductive switching.

Further refinements in the Fourier modeling are underway and will be extended to other SiC bipolar structures such as a GTO.

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