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Stencil masks are key to charged particle projection lithography, in particular for ion projection lithography. To fulfill pattern printing requirements in the sub-70 nm regime, excellent thickness uniformity and thermal emissivity control are critical parameters for high quality stencil mask fabrication. We propose and demonstrate a technique based on infrared variable angle spectroscopic ellipsometry (IR-VASE) to measure these parameters with adequate accuracy and precision. The refractive index of the Si membrane was evaluated using a Sellmeier dispersion model combined with a Drude model. Because of its spectral range from 2 to 33 μm, the IR-VASE method is sensitive to the thickness of layers as well as to the concentration and profile of Si membrane doping. © *2000 American Vacuum Society.* [S0734-211X(00)08106-3]

I. INTRODUCTION

Silicon stencil masks can be applied to ion projection lithography (IPL), electron beam projection (PreVail), but might as well also be used for photon based lithographic techniques [157 nm, extreme ultraviolet (EUV)].[1] Charged particles or photons illuminate a stencil membrane mask with reduction printing to resist coated wafer substrates. Quantitative determination of the mechanical, electrical (conductivity), and thermal characteristics of stencil masks is a critical issue in the development of highly reliable mask technology. Thin silicon membranes like those used for this study were fabricated using the *pn* junction electrochemical etch stop (ECES) technique.[2,3]

The focus of this study is to demonstrate that the membrane thickness depends on the applied reverse bias on the *pn* junction during the ECES etching. We determined that by utilizing infrared variable angle spectroscopic ellipsometry (IR-VASE).[4]

II. *pn* JUNCTION ECES TECHNIQUES FOR SILICON MEMBRANE FABRICATION

To fabricate thin ($\sim$3 μm) membranes from ⟨100⟩ silicon wafers, aqueous alkali solutions like KOH or tetramethyl ammonium hydroxide (TMAH) are widely used. The etch mechanisms[5,6] are based on the oxidation of silicon in water and subsequent dissolution of silicon hydroxide from solid state silicon in an ambient with an excessive *p*H value by building silicon hydroxide complexes. The electrons injected into the conduction band of the silicon crystal during the oxidation steps reduce water molecules at the silicon and electrolyte interface by forming hydroxide ions and hydrogen gas.

$$\mathrm{Si} + 4\mathrm{OH}^- \longrightarrow \mathrm{SiO_2(OH)_2^{2-}} + 2\mathrm{H}^+ + 4e^-,$$

$$4\mathrm{H_2O} + 4e^- \longrightarrow 4\mathrm{OH}^- + 2\mathrm{H_2}.$$

The etch rates of crystalline silicon in alkali solution are different, depending on the crystal orientation. This anisotropic etch behavior is due to different oxidation states of silicon atoms at the surface in different crystal orientations.

Thus, the ECES is based on anodic passivation of silicon in an aqueous alkali solution. A positive potential of 0.5–0.8 V over the open circuit potential can passivate both *p*- and *n*-type silicon from etching. A sufficient anodic potential causes an accumulation of holes (h^+) at the silicon surface which increase oxidation states of silicon atoms at the interface between Si and electrolyte according to Ghandi.[7]

$$\mathrm{Si} + 2h^+ \rightarrow \mathrm{Si}^{2+}.$$

The Si atoms react with OH^- ions diffused into the surface to build $\mathrm{Si(OH)_2}$,

$$\mathrm{Si}^{2+} + 2\mathrm{OH}^- \rightarrow \mathrm{Si(OH)_2},$$

which change into $\mathrm{SiO_2}$ by splitting the hydrogen. The wafer surface is now covered with a very thin but dense $\mathrm{SiO_2}$ film which reduces the etch rate of silicon about two orders of magnitude. Using a reverse biased *pn* junction structure, the thin *n*-type Si region can be anodic passivated from the etch process while the *p*-Si substrate (due to a drop in potential at the *pn* junction) is insufficiently protected and will be etched off. A thin *n*-Si sheet with controlled thickness can be created conveniently by standard diffusion or ion implantation processes used in common integrated circuit (IC) production.

Specifically, the Si membranes used for the present study were fabricated with the ECES technique according to the following process steps [Fig. 1(a)]. The starting material was double side polished 100 mm *p*-type ⟨100⟩ Si wafers. Subse-

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quent to thermal oxidation and window fabrication in this layer on the front and back sides, phosphorus was implanted at the front side to achieve an *n*-type top layer after proper annealing. Using phosphorus diffusion the stress of the subsequent Si membrane can be controlled precisely because P provides tensile stress within the Si matrix. A metal layer was deposited onto the front side, forming electrical contact to the *n*-type layer. Using a newly designed electrochemical etch cell, which protects the front side totally from the aqueous alkali solution, membranes of about 4–7 μm were fabricated. As an example Fig. 1(b) shows a 100 mm Si wafer with 24 Si membrane fields.

For use as stencil masks the Si membrane must have a very homogeneous thickness—better than 1%.[8] For the case of ECES fabricated Si membranes the thickness depends on the *pn* junction space–charge region. This can be explained as follows with the assumptions (i) that near the *pn* junction ($x=0$) in the thermal equilibrium the charge density is zero outside of the transition region ($-x_{p_0}<x<x_{n_0}$) since bulk silicon is electrically neutral, (ii) that the minority electrons on the *p* side and the minority holes on the *n* side are neglected, and (iii) that the majority carrier concentrations are close to the doping concentrations near the edge of the transition region.[9] Therefore inside the transition region the charge density $\rho_0(x)$ is given by

$$\rho_0(x)\approx \begin{cases} -qN_a, & (-x_{p_0}\leqslant x\leqslant 0) \\ qN_d, & (0\leqslant x\leqslant x_{n_0}) \\ \text{with} \quad \rho_0(x)=0, & (x\leqslant -x_{p_0}\vee x_{n_0}\leqslant x), \end{cases} \tag{1}$$

where q is the electron charge, p_0, and n_0 the *p* and *n* charge-carrier concentrations and N_a and N_d the *p*-and *n*-side doping concentrations.

Finally the transition region is seen as completely depleted of mobile holes and electrons (the transition region at the *pn* junction $\equiv$ the depletion region).

By making the depletion approximation and dividing the *pn* junction into a depletion region sandwiched between bulk *p* and *n* regions, relatively simple solutions can be found, e.g., the depletion region width using Gauss's law:

$$\frac{dE}{dx}=\frac{\rho(x)}{\epsilon_s}, \tag{2}$$

where ϵ_s is the electric permittivity of Si($\epsilon_s=11.7\epsilon_0$).

The solution for the edge on the *p* side of the depletion region using the barrier potential $\phi_B=\phi_n-\phi_p$, where ϕ_n and ϕ_p are the potentials of the *n*- or *p*-bulk region in thermal equilibrium is

$$x_{p0}=\sqrt{\frac{2\epsilon_s\phi_B}{qN_a}\frac{N_d}{N_d+N_a}}. \tag{3}$$

It follows that the membrane thickness and stress depend only on the doping concentrations N_a for the *p* side and N_d for the *n* side. However the membrane thickness can be varied due to the barrier potential ϕ_B.

The etch stop during electrochemical etching can be controlled *in situ* by measuring the current I of the reverse biased ''*pn* diode'' versus time t (Fig. 2). As the back side of membrane approaches the space–charge region, more OH^- will be accelerated towards the membrane, resulting in an increased electrochemical reaction rate and subsequent increase in the current density. Thus, with a greater degree of coverage by the hydroxide, the SiO_2 passivation layer becomes thicker, causing the current to finally settle at a constant value. This indicates the end of the etch process. In this way well-controlled, repeatable thin silicon membranes can be produced in which the thickness variation depends on the bias voltage using the ECES technique.

III. EXPERIMENTAL SETUP: IR-VASE

To use these thin Si membranes for stencil masks, it is important to evaluate the thickness nondestructively. The samples were measured using a commercially available infrared variable angle spectroscopic ellipsometer.[10] The instrument consists of a Fourier-transform-based infrared spectrometer combined with a rotating-compensator variable angle ellipsometer. The compensator not only insures the accuracy of the ellipsometric angle Δ over its full 360° range it also provides a means by which to measure the amount of depolarization caused by the sample. For this study, data were acquired over the 2–30 μm (wave number of 330–5000 cm^{-1}) spectral range. The beam diameter is 8 mm at the sample, with a 3° angular spread. Data were taken with a resolution of 32 cm^{-1} at two or three incidence angles between 55° and 70°. This yielded ellipsometric data with reasonable sensitivity and signal-to-noise ratios.

Values for Ψ and Δ at each wavelength comprise the ellipsometric spectrum. This spectrum is an extremely sensitive function of the various layers and microstructure of a sample (for further information about ellipsometry, see Refs. 11 and 12). Unfortunately, for all but the simplest samples, this function cannot be inverted; therefore information must be extracted by optimizing the parameters of an appropriate optical model fit to the data. The numerical regression procedure used here (described by Herzinger *et al.*[11]) adjusts the various parameters until the mean square error between the calculated and measured ellipsometric values is minimized.

The optical properties of each silicon layer are defined by the classical Drude equation[12]

$$\epsilon_j=\text{offset}+\frac{A}{E_a^2-E^2}-\frac{1}{\rho_{\text{dc}_j}}\frac{4\pi\hbar^2}{(E^2\tau+i\hbar E)}, \tag{4a}$$

$$\rho_{\text{dc}_j}=\frac{m^*}{N_j e^2\tau}=\frac{1}{N_j e\mu}, \tag{4b}$$

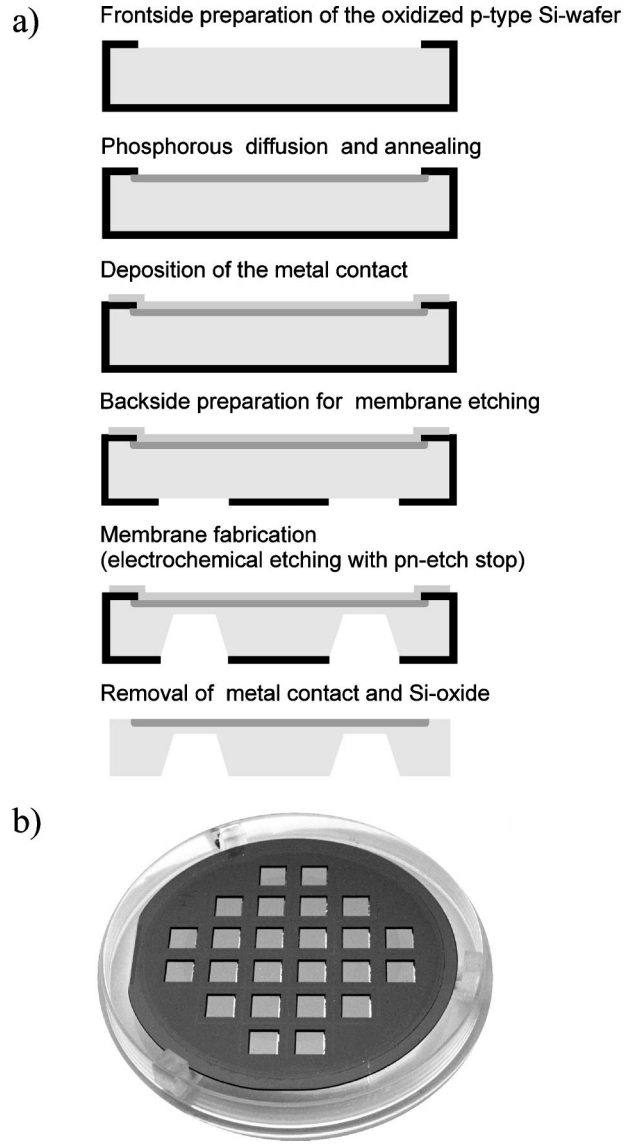

FIG. 1. (a) Process flow of *pn*-membrane production for open stencil masks using electrochemical etching with a *pn*-etch stop. (b) Sample with 24 mini-membranes (7×7 mm^2) on which membrane thickness was measured with IR-VASE.

where ϵ_j is the complex dielectric function of the jth layer, the offset, A, and E_a terms comprise a Sellmeier model for the residual dielectric response from the interband transitions, E is the energy of the incident photons, and τ is the mean scattering time of the free carriers. The quantity ρ_{dc_j} is the dc resistivity of the jth layer. It is inversely proportional to the electronic charge e, the carrier concentration N_j, and the carrier mobility $\mu=e\tau/m^*$, where m^* is the carrier effective mass. For this study, we assume that τ is independent of photon energy. Ultimately, we wish to determine N_j; unfortunately, N_j is not independent of mobility, since $1/\rho_{\mathrm{dc}_j}=e\mu N_j$. This is problematic because $\mu=e\tau/m^*$, and both m^* and τ are strong functions of doping in heavily doped samples. We use a method based on ASTM standard 723-88,[13] which yielded good results in a previous study.[4]

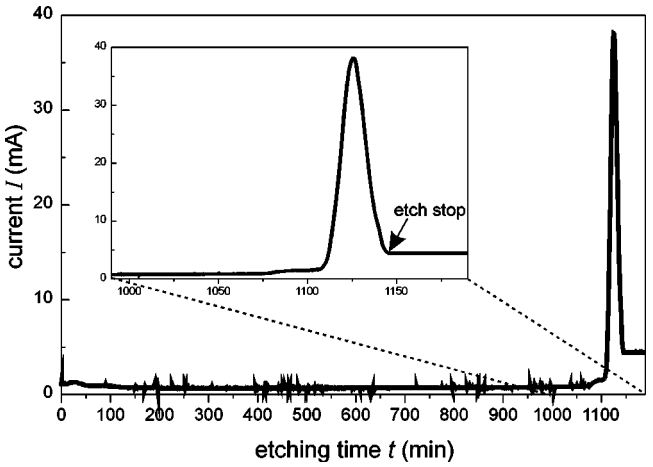

FIG. 2. Behavior of current I vs time t during the electrochemical etching and in particular during and shortly before the electrochemical etch stop.

This method converts silicon resistivities directly into carrier densities using empirical equations that were developed from a set of carefully characterized samples.

IR-VASE measurements were made on both the front and back of the *pn* membrane, because the highly doped region strongly absorbed infrared light. From the back side, IR light

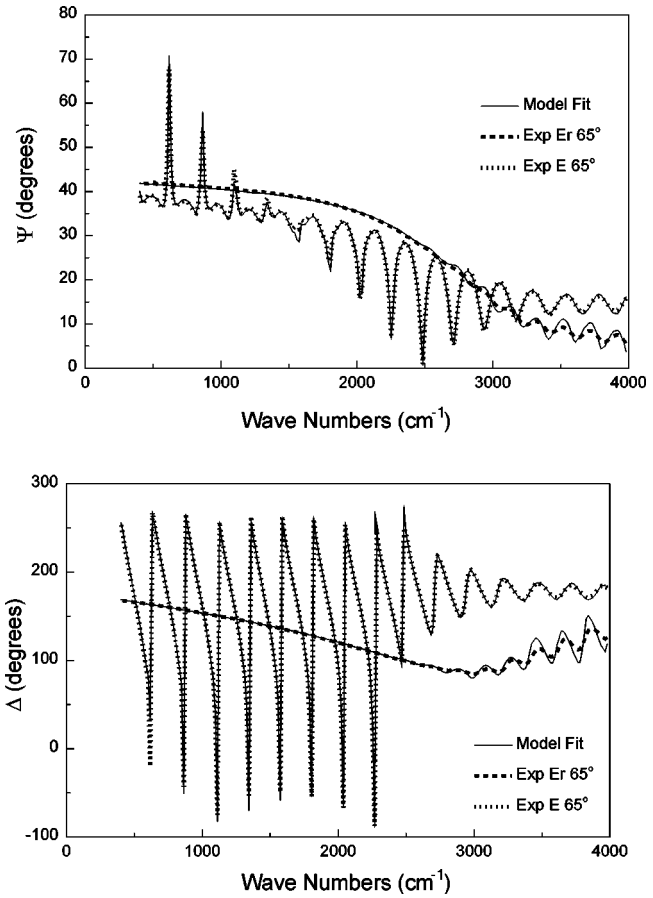

FIG. 3. Experimental data of ellipsometric angles Ψ and Δ measured with IR-VASE and the corresponding fits [Er: ellipsometry from the highly doped (reverse) side; E: ellipsometry from the back side].

TABLE I. Thickness of the regions of the *pn* membrane, which was etched with ECES using a bias voltage of 11 V and measured with IR-VASE.

Native oxide backside	0.005 μm
Silicon bulk region	5.00 μm
Silicon with free carriers	2.03 μm
Native oxide frontside	0.001 μm
Total thickness	7.036 μm

penetrates through 6 μm of low-doped Si and reflects from the highly doped front side region, producing strong interference oscillations (see data labeled ''E''). From the front side, IR light cannot penetrate beyond the highly doped region, resulting in no interference oscillations (see data labeled ''Er''). Simultaneous analysis of both data sets provides the best description (Fig. 3) of the membrane's IR optical response.

The result of the sample which was etched with a bias voltage of 11 V is shown in Table I using thicknesses determined from the data fit. The 90% confidence limit for the bulk and doped silicon layers was ± 0.03 μm.[10,11] The total sample thickness was 7.04 μm. The heavily doped region thickness of 2.03 μm compares favorably with estimates based on standard methods of IC technology. The free-carrier concentration depth profile for the same 11 V bias sample is shown in Fig. 4. The carrier concentration was derived using the empirical equation from Ref. 13.

IV. RESULTS

For these experiments, 100 mm⟨100⟩ Si wafers with defined *pn* junctions were wet chemical etched using ECES in a 30 wt% KOH solution at a temperature of 60 °C. To achieve a specific etch stop a dc bias voltage U was applied. By increasing this voltage U in the range between 2 and 11 V the membranes become thicker (a darker red color).

Comparison between the measurement results obtained and the theoretical thickness approximation presented above we found a dependency of the thickness of membrane d on the applied bias voltage U. That is shown in the experimentally determinated (black dots) and theoretically predicted (dashed line) thickness versus bias voltage diagram (Fig. 5). With the depth of the *n*-type dopant (phosphorus) d_n and Eq. (3) known we get the relationship for the effective membrane thickness as

$$d \propto d_n + \sqrt{\frac{2\epsilon_s}{qN_a}\frac{N_d}{N_d+N_a}U}. \tag{5}$$

Consequently we can determine, with the doping concentrations N_a for the p side and N_d for the n side, not only the thickness, but also the ''integral'' stress of the membrane with bias voltage U.

V. SUMMARY

It was shown that the thickness of thin Si membranes, realized with the electrochemical etch stop using *pn*-junction wafers, can be controlled by the bias voltage. With IR-VASE we were able to determine the thickness of such thin Si membranes that consisted of a highly doped n^+-type (phosphorus) region and a *p*-type (boron) region. Furthermore, the depth profile of the optical constants and of the concentration of the free carriers in membranes has been experimentally evaluated. From these values the thermal emissivity and thermal conductivity can be determined.

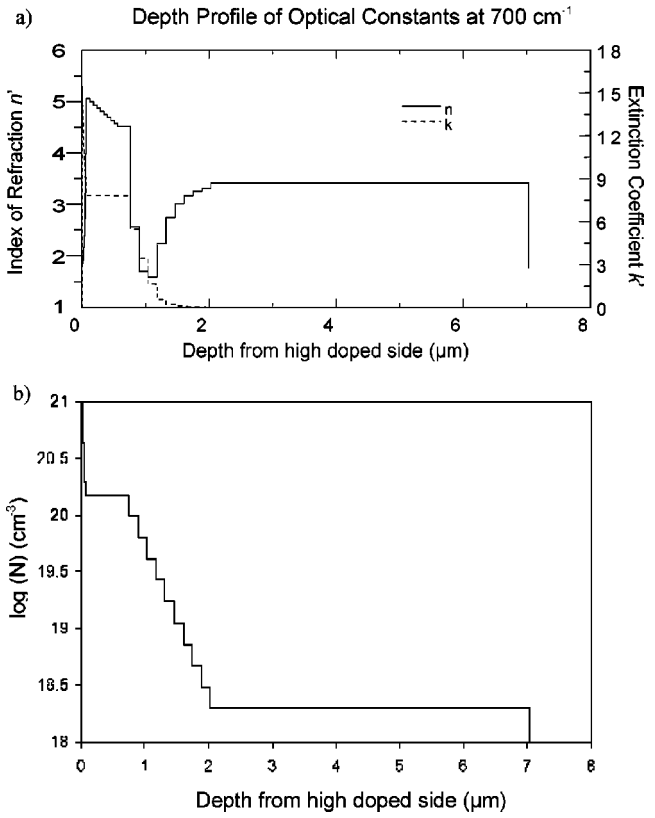

FIG. 4. (a) Depth profile of optical constants (refractive index n and extinction coefficient k) of the highly *n*-doped membrane side (IR-VASE) and (b) the resulting free carrier depth profile.

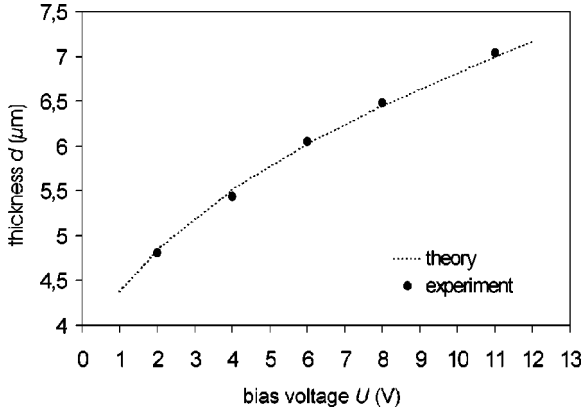

FIG. 5. Dependence of the total membrane thickness d on the bias voltage U for fabrication with ECES, experimentally determinated (black dots; with an accuracy of ± 0.03 μm, Refs. 10 and 11) and theoretically predicted (dashed line).

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