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Sharad C. Seth
University of Nebraska - Lincoln, seth@cse.unl.edu

Vishwani D. Agrawal
Bell Laboratories, Murray Hill, NJ

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SHARAD C. SETH, SENIOR MEMBER, IEEE, AND VISHWANI D. AGRAWAL, SENIOR MEMBER, IEEE

Abstract—**The results of production test on LSI wafers are analyzed to determine the parameters of the yield equation. Recognizing that a physical defect on a chip can produce several logical faults, the number of faults per defect is assumed to be a random variable with Poisson distribution. The analysis provides a relationship between the yield of the tested fraction of the chip area and the cumulative fault coverage of test patterns. The parameters of the yield equation are estimated by fitting this relation to the measured yield versus fault coverage data.**

I. Introduction

THE established approach to yield estimation of LSI chips is based upon an assumed defect-density distribution over a wafer. The yield equation, i.e., the yield versus chip area relationship, is expressed in terms of the parameters of this distribution which are estimated either from monitor wafers [1] or from a few carefully placed test chips on each wafer [2]-[4]. The monitors or test chips are designed to detect commonly known types of *physical defects*, such as opens and shorts in the layers of diffusion, polysilicon, and metal or the *parametric irregularities*. Once the distribution of defect-density is determined, the chip yield can be calculated. The parameters of yield equation not only vary from wafer-to-wafer or lot-to-lot but also undergo variations within a wafer. A continuous monitoring is, therefore, desirable.

In addition to parametric testing the wafer test also includes the functional testing of *all* the chips on the wafer. It was shown in [5] that the chip failure data thus obtained can be analyzed to estimate the *reject ratio*, that is, the fraction of bad chips passed as good by the tests. In this paper, we show that further use can be made of the same data in characterizing the yield equation. A compound model is introduced in which each physical defect is assumed to produce a random number of *logical faults*. The parameters of the model are derived from the functional test process. These test data reflect the effect of fault distribution over all the chips on a wafer instead of a few defect monitors.

II. Analysis

Let x be the random variable denoting the number of physical defects on a chip. Following Stapper [6] we will assume that x has a *negative binomial distribution* given by [7, p. 18]:

$$p_1(x) = \text{Prob(number of defects} = x)$$

$$= \binom{x + a - 1}{x} (Ab)^x (1 + Ab)^{-x-a} \tag{1}$$

where A is the chip area, and $a \geqslant 0$, and $b > 0$ are two parameters. Further, we assume that each physical defect can produce several faults, such as stuck-at-1's, stuck-at-0's, etc. Suppose a given chip has x defects and the ith defect causes k_i faults. Then the total number of faults on the chip is

$$n = \sum_{i=1}^{x} k_i.$$

We assume that the random variables k_i are independent and that their values occur with probabilities given by a Poisson distribution having mean c. Then the total number of faults in the presence of x defects will have a distribution which is the x-fold convolution of identical Poisson distributions. This is known to be a Poisson distribution also [8, p. 268] with mean cx. Thus

$$p_2(n|x) = \text{Prob(number of faults)} = n|x \text{ defects)}$$

$$= \frac{(cx)^n}{n!} e^{-cx}. \tag{2}$$

With the help of (1) and (2) we can express a *generalized distribution* [7, p. 21] for the number of faults on a chip:

$$p_3(n) = \text{Prob(number of faults} = n)$$

$$= \sum_{x=0}^{\infty} p_2(n/x) p_1(x). \tag{3}$$

Next, we will derive the probability generating function (p.g.f.) for $p_3(n)$ which is defined as

$$G_3(s) \triangleq \sum_{n=0}^{\infty} p_3(n)\, s^n \tag{4}$$

where s is the transformation variable (see [8, p. 264]. Substituting from (3), we get,

$$G_3(s) = \sum_{n=0}^{\infty} \sum_{x=0}^{\infty} p_2(n|x)\, p_1(x)\, s^n$$

$$= \sum_{x=0}^{\infty} p_1(x) \sum_{n=0}^{\infty} p_2(n|x)\, s^n.$$

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S. C. Seth is with the Department of Computer Science, University of Nebraska, Lincoln, NE 68588.

V. D. Agrawal is with Bell Laboratories, Murray Hill, NJ 07974.

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The inner summation in the last expression represents the p.g.f. of the Poisson distribution [7, p. 14] which is $e^{cx(s-1)}$. Therefore,

$$G_3(s) = \sum_{x=0}^{\infty} p_1(x)\, e^{cx(s-1)}$$

$$= \sum_{x=0}^{\infty} p_1(x)\, t^x \qquad \text{where} \quad t = e^{c(s-1)}$$

$$= G_1(t)$$

where G_1 represents the p.g.f. of the negative-binomial distribution p_1. This has the closed-form expression ([7, p. 17])

$$G_1(t) = (1 + Ab - Abt)^{-a}$$

which, upon substitution of the expression for t, yields the desired p.g.f. as

$$G_3(s) = [1 + Ab(1 - e^{c(s-1)})]^{-a}. \tag{5}$$

If f is the fault coverage expressed as a fraction of total faults, then $1 - f$ will be the probability of a randomly selected fault remaining undetected by the tests. When the chip has n faults, the probability of none of them being detected by the tests can be approximated as $(1 - f)^n$. This approximation is accurate under quite general conditions as shown in [9]. Now since n is a random variable with probability density $p_3(n)$, the apparent yield of chips that pass the tests will be

$$y + Y_{bg}(f) = \sum_{n=0}^{\infty} p_3(n)\,(1 - f)^n$$

where the left-hand side simply indicates that the apparent yield is composed of the true yield y and the yield $Y_{bg}(f)$ of bad chips tested as good. From the definition of probability generating function given by (4) the above expression is equivalent to $G_3(1 - f)$. Thus using (5), we get

$$y + Y_{bg}(f) = [1 + Ab(1 - e^{-cf})]^{-a}. \tag{6}$$

Obviously, for a complete fault coverage ($f = 1$), Y_{bg} is zero. Thus the yield is given by

$$y = [1 + Ab(1 - e^{-c})]^{-a}. \tag{7}$$

Reject ratio, which is defined as the fraction of bad chips among those that are tested good can be computed from (6) and (7) as follows:

$$r(f) = \frac{Y_{bg}(f)}{y + Y_{bg}(f)} = 1 - \left[\frac{1 + Ab(1 - e^{-c})}{1 + Ab(1 - e^{-cf})}\right]^{-a}. \tag{8}$$

Let $P(f)$ represent the fraction of chips rejected by test patterns with cummulative fault-coverage f, then,

$$P(f) = 1 - y - Y_{bg}(f) = 1 - [1 + Ab(1 - e^{-cf})]^{-a}. \tag{9}$$

III. Estimation of Parameters

The wafer test data for an LSI chip was analyzed. This chip contained approximately 2700 transistors. The chip-failure data was combined with the results from fault simulation to obtain a plot of the fraction $P(f)$ of failing chips versus the fault coverage f (see [5] for further details of this procedure.) The resultant data are shown as the points in Fig. 1. A weighted least squares procedure was used to estimate the parameters a, Ab, and c in (9) that best fit these data [10]. The results were as follows:

$$a = 0.748, \quad Ab = 1.770, \quad \text{and} \quad c = 2.777.$$

From (7) the yield for these values of the parameters is 48 percent which agrees closely with the expected yield for this chip. The reject ratio for the tests, which have a 90-percent fault coverage, is about one percent as computed from (8) (see Fig. 2). Also for a 0.1-percent reject ratio ($r = 0.001$), about 99-percent fault coverage will be required.

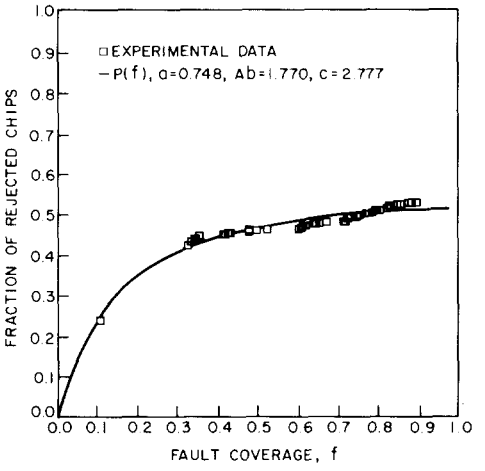

Fig. 1. Wafer-test data: Fraction of rejected chips as a function of fault coverage.

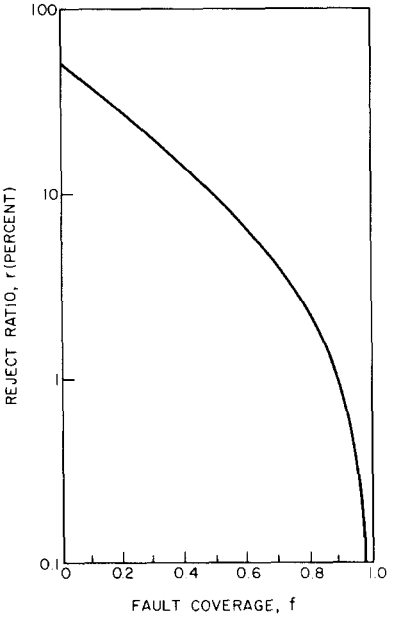

Fig. 2. Reject ratio versus fault coverage as computed from (8) using the estimated parameters $a = 0.748$, $Ab = 1.77$, and $c = 2.777$.

IV. Yield and Fault Coverage

Stapper's yield equation is written as [6]

$$y = [1 + A\bar{D}(\sigma/\mu)^2]^{-(\mu/\sigma)^2} \tag{10}$$

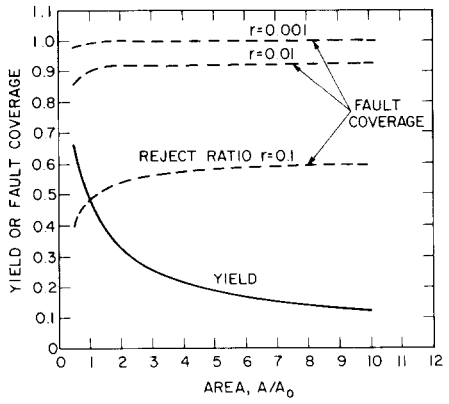

Fig. 3. *Yield Equation:* Yield versus area (solid curve) computed from the estimated parameters, $a = 0.748$, $A_0 b = 1.77$, $c = 2.777$. The normalizing area A_0 is the area of the chip of Fig. 1. The dashed curves are the computed fault coverages required for reject ratios of 10-, 1-, and 0.1-percent.

where $\bar{D}$ is the average defect density and σ/μ is the coefficient of variation of the defect density. A is the chip area. Comparing (10) and (7), we get

$$\sigma/\mu = \sqrt{1/a}$$

and

$$A\bar{D} = Ab(1 - e^{-c})\, a. \tag{11}$$

For the chip considered in the previous section, $\sigma/\mu = 1.16$ and $A\bar{D} = 1.93$. These values are of the same order as those given in [6]. Fig. 3 shows a yield versus area curve (solid line) as computed from these values. The normalizing area A_0 in this graph is the area of the chip whose test results were analyzed in the previous section.

For a given reject ratio r, (8) can be solved to give the required fault coverage,

$$f = -\frac{1}{c} \ln \left[1 + \frac{1 - (1 - r)^{1/a} \{1 + Ab(1 - e^{-c})\}}{Ab} \right]. \tag{12}$$

The fault coverages as computed from this formula are shown in Fig. 3 by dashed curves. It is interesting to note that as the area increases, for a given reject ratio, the required fault coverage converges to a fixed value. For example, a 1-percent reject ratio ($r = 0.01$) would require about 93-percent fault coverage. These results are, of course, valid for the chips that are fabricated in the same technology and design-style as the one from which the parameters were estimated. For finer features, one would expect the average number c of logical faults per physical defect to be larger and in that case equation (12) will give a lower fault coverage requirement for the same given reject ratio.

Normally, the yield equation is characterized by fitting (10) to the experimental data on yield versus area obtained from several chips of varying areas. In our analysis the characterization of the yield equation is accomplished from the data on just one type of chips. This is not surprising because the measured rejected fraction (or 1-yield), $P(f)$ given by (9), contains the effect of yield variation as the tested area of chip increases. To illustrate this we use (11) and rewrite (9) as

$$P(f) = 1 - [1 + A_f \bar{D}(\sigma/\mu)^2]^{-(\mu/\sigma)^2}$$

where A_f is the tested area given by

$$A_f = A \cdot \frac{1 - e^{-cf}}{1 - e^{-c}}.$$

Thus the $P(f)$ versus f relation can also be thought of as 1-yield versus tested area. Notice that A_f is a nonlinear function of f since in our model, a defect can cause several faults. The special case of a single fault per defect can be analyzed by assuming $c \ll 1$ so that the probability of more than one fault is very small. In this case $A_f = Af$ as has been discussed in [11].

V. Conclusion

Traditionally chip failure data has been used just to identify good chips from the bad ones. We have shown that such data, in combination with results from a fault simulator, can be used also to characterize important aspects of processing and testing. The yield equation derived in this paper is based on the distinction between physical defects and logical faults. The parameters of this equation are derived from the wafer-level test data.

Briefly, the advantages of the proposed approach are as follows:

(1) Since the yield equation is characterized at the functional test level, it is capable of taking the technology-dependent factors into account.

(2) No additional effort is required for data collection since the wafer-level tests for both yield characterization and production testing are the same.

(3) The results of analysis may be used differently for a new and mature process. For a new process the parameters of the yield equation may be monitored closely for an unexpected deviation from the norm and used to raise an alert in case of such a deviation. For a mature process, the yield equation could be used to estimate the yield and the required fault coverage of a future chip with a different area.

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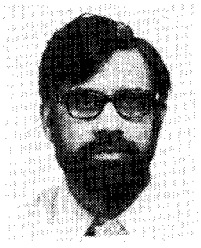

Sharad C. Seth (S'66-M'70-SM'82) received the B.E. degree in electronics and telecommunications from Jabalpur University, Jabalpur, India, in 1964, the M.Tech. degree in electrical engineering from the Indian Institute of Technology, Kanpur, India, in 1966, and the Ph.D. degree in electrical engineering from the University of Illinois, Urbana, in 1970.

Since 1970 he has been on the faculty of the Department of Computer Science, University of Nebraska, Lincoln, and is currently a Professor. He held visiting positions at the Indian Institute of Technology, Kanpur, India, during the years 1974-1975 and 1982-1983 and at Bell Laboratories, Murray Hill, NJ, during the summers of 1980 and 1982. His current research interests are in the areas of VLSI testing and design and reliability analysis of fault-tolerant systems.

Dr. Seth is a member of the ACM and the Computer Society of India.

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Vishwani D. Agrawal (S'68-M'70-SM'80) received the B.Sc. degree from Allahabad University, Allahabad, India, in 1960, the B.E. (honors) degree from Roorkee University, Roorkee, India, in 1964, the M.E. degree from the Indian Institute of Science, Bangalore, India, in 1966, and the Ph.D. degree from the University of Illinois, Urbana, Illinois, in 1971.

His experience includes teaching (1966-1967) in the Department of Electrical Engineering, Indian Institute of Technology, New Delhi, India; research (1967-1970) at the Antenna Laboratory, University of Illinois, Urbana; digital test technique development for Illiac IV Project (1970-1971) at the Automation Technology, Inc., Champaign, IL; electromagnetic pulse (EMP) experimentation (1971-1972) at E.G. and G., Inc., Albuquerque, NM; teaching and research (1972-1975) at the School of Radar Studies, Indian Institute of Technology, New Delhi, India; and spacecraft antenna design (1975-1978) at TRW Defense and Space Systems Group, Redondo Beach, CA. Since 1978, he has been working on computer-aided design and testing of LSI circuits at the Bell Laboratories, Murray Hill, NJ, where he is now the supervisor of Test Aids Group. He was co-recipient of the Best Applications Paper Award from the IEEE Antennas and Propogation Society in 1979, and his paper, coauthored with M. R. Mercer, has won him the Best Paper Award at the 1982 IEEE International Test Conference.

Dr. Agrawal is a fellow of the Institution of Electronics and Telecommunication Engineers (India).

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