AUTOMATED SYNTHESIS TOOL FOR DESIGN OPTIMIZATION OF POWER ELECTRONIC CONVERTERS

A Dissertation

by

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ABSTRACT

Designers of power electronic converters usually face the challenge of having multiple performance indices that must be simultaneously optimized, such as maximizing efficiency while minimizing mass or maximizing reliability while minimizing cost. The experienced engineer applies his or her judgment to reduce the number of *possible designs* to a manageable number of *feasible designs* for which to prototype and test; thus, the optimality of this design-space reduction is directly dependent upon the experience, and expertise and biases of the designer. The practitioner is familiar with tradeoff analysis; however, simple tradeoff studies can become difficult or even intractable if multiple metrics are considered. Hence a scientific and systematic approach is needed. In this dissertation, a multi-objective optimization framework is presented as a design tool.

Optimization of power electronic converters is certainly not a new subject. However, when limited to off-the-shelf components, the resulting system is really optimized only over the set of commercially available components, which may represent only a subset of the design space; the reachable space limited by available components and technologies. While this approach is suited to cost-reduce an existing design, it offers little insight into design possibilities for greenfield projects.

Instead, this work uses the Technology Characterization Methods (TCM) to broaden the reachable design space by considering fundamental component attributes. The result is the specification for the components that create the optimal design rather than an evaluation of an *apriori* selected set of candidate components. A unique outcome of this

approach is that new technology development vectors may emerge to develop optimized components for the optimized power converter. The approach presented in this work uses a mathematical descriptive language to abstract the characteristics and attributes of the components used in a power electronic converter in a way suitable for multi-objective and constrained optimization methods.

This dissertation will use Technology Characterization Methods (TCM) to bridge the gap between high-level performance attributes and low-level design attributes where direct relationship between these two does not currently exist. The loss and size models for inductors, capacitors, IGBTs, MOSFETs and heat sinks will be used to form objective functions for the multi-objective optimization problem. A single phase IGBT-based inverter is optimized for efficiency and volume based on the component models derived using TCM. Comparing the obtained designs to a design, which can be made from commercial off-the-shelf components, shows that converter design can be optimized beyond what is possible from using only off-the-shelf components. A module-integrated photovoltaic inverter is also optimized for efficiency, volume and reliability. An actual converter is constructed using commercial off-the-shelf components. The converter design is chosen as close as possible to a point obtained by optimization. Experimental results show that the converter modeling is accurate. A new approach for evaluation of efficiency in photovoltaic converter is also proposed and the front-end portion of a photovoltaic converter is optimized for this efficiency, as well as reliability and volume.

To my beloved parents and brother, for their continuous support and dedication

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1. INTRODUCTION

Electricity represents 40% of the total energy consumption worldwide [1] and the demand for the electrical power is only expected to increase [1]. Power electronic converters are integral to this growth as the digital economy and new load types necessitate point-of-use power conversion to almost arbitrary voltage and frequency. Thus, power electronics can be found through the electrical system as they enable efficient conversion generation, storage, and end-user applications. With technologies such as all electric aircraft [2] and electric vehicles gaining more attention, it is expected that the number of power electronic converters will continue to increase in the coming years [3]. Increasing numbers of digital devices will also increase the demand for power electronic converters; Cisco visual networking index forecast predicts that by year 2015 the number of digital devices connected to the network will be twice the world population [4]. At the same time, all electronics are expected to become *better, faster, cheaper* which required highly optimized designs. Therefore, effective design approaches are required in order to achieve high performance indices including size, weight, efficiency, cost, and reliability, to name a few.

Optimization of power electronic converters is certainly not a new subject. However, past efforts have been focused on the use of commercial off-the-shelf components in the design optimization. Thus, the resulting system was really optimized only over the set of available components which may in fact represent only a subset of the design space; a reachable space limited somewhat artificially by available components

and technologies. While this approach is suited for the engineer seeking to cost-reduce an existing design, it offers little insight into design possibilities for greenfield projects. Instead, this dissertation seeks to first broaden the reachable design space to identify a globally optimal design for some given objective, from which specifications for the individual components can be derived. A unique outcome of this approach is that new technology development vectors are expected to develop optimized components for the optimized power converter. The approach presented in this work uses a descriptive language to abstract the characteristics and attributes of the components used in a power electronic converter in a way suitable for multi-objective and constrained optimization methods. It should also be noted that in order to find a globally optimal point for a converter, the converter should be dealt with as a whole. Optimization of a subsection of a whole converter may result in missing on a truly optimal point for the converter. Therefore, this work only focuses on optimizing the entire power circuit of a power electronic converter.

1.1. Optimization problem

The *optimization* problem can be defined in a general form as [5]:

$$\begin{aligned} &\textit{Minimize} \quad f(x) \quad x \in \Omega \\ &\text{Subject to :} \quad g_i(x) \le 0 \quad i = 1...n \\ &\qquad\qquad\quad h_i(x) = 0 \quad j = 1...m \end{aligned} \tag{1-1}$$

where $f(x)$ is the objective function, $g_i(x)$ $i=1\ldots n$ and $h_j(x)$ $j=1\ldots n$ are equality and non-equality constraints respectively, and x is a vector of design variables in the space Ω. The optimization problem is usually defined as a minimization problem since *maximize* $f(x)$ is equivalent to *minimize* $-f(x)$ [5]. The goal of solving an optimization problem is to find

the best value for a performance index over a certain domain by changing a set of selected design variables.

The basic elements of an optimization problem are explained as follows.

- **Design variables** should define the object under optimization thoroughly. For example, if one wants to optimize a sedan car, design variables can be the engine horsepower, the dimensions and the material properties of the body and the frame, the transmission system part number and etc. The level of detail in design variables may vary from an optimization problem to the other. For example, instead of having the engine horsepower as a design variable, a designer may choose the dimensions of the crankshaft, cylinder, flywheel and other engine components as design variables.
- **Performance indices** are chosen by the designer depending on what they want to optimize in their design. In the car example, performance indices can be the maximum speed, fuel consumption in miles-per-gallon, the cost of the car, the durability/reliability of the car, etc. An **objective function** is used to calculate the performance indices from the design variables using principles of the operation of the device. For the car example, a set of mathematical equations which calculate maximum speed from the design variables such as engine horsepower and aerodynamics of the body can be an objective function.
- **Constraints** are limitations which mark certain sections of the design space as invalid. The reason for such limitations can vary from operational considerations to rules and regulations. For the car example, a very heavy engine cannot be

mounted on a weak frame and therefore, the weight of the engine and the strength of the frame are interdependent. Furthermore, environmental regulations may prevent the designer from using a certain type of engine with a certain type of exhaust system.

A minimizer is a point in the design space in which the objective function has the minimum value (locally or globally). A local minimizer for (1-1) is defined as the point $x^* \in \Omega$ if there exists $\varepsilon > 0$ such that $f(x) \geq f(x^*)$ for all $x \in \Omega \setminus \{x^*\}$ and $\|x - x^*\| < \varepsilon$. A global minimizer is defined as the point $x^* \in \Omega$ such that $f(x) \geq f(x^*)$ for all $x \in \Omega \setminus \{x^*\}$ [5]. An optimization algorithm is required to solve the optimization problem, and there are numerous well-known algorithms for this purpose. Section 3 Discuses candidate appropriate algorithms for the optimization of (1-1).

In the presence of multiple performance indices for a power electronic converter, it is often difficult to identify the "best" possible converter since the definition of "best" may be different based on designer's preference. In such a situation, one should use a multi-objective optimization.

The mathematical formulation of multi-objective optimization is as follows [6].

$$\begin{aligned} &\textit{Minimize} \quad F(x) = (f_1(x), f_2(x), \ldots, f_k(x)) \quad x \in \Omega \\ &\text{Subject to :} \quad g_i(x) \leq 0 \quad i = 1 \ldots n \\ &\qquad\qquad\quad h_i(x) = 0 \quad j = 1 \ldots m \end{aligned} \tag{1-2}$$

where $F(x)$ was a scalar function in the single-objective optimization problem (1-1), it is a k-dimensional vector of objective functions in the multi-objective optimization problem (1-2) and $g_i(x)$ and $h_i(x)$ are inequality and equality constraints respectively.

The ideal solution to the multi-objective optimization problem is a solution that has the best performance index on all of the dimensions. However, due to the existence of interdependencies and tradeoffs, such a solution is not likely to occur. In search for an optimum point, one might find a point x^* such that there is no other point x' in the feasible space that, by moving to x', reduces at least one objective function without increasing another [6]. This point is called *Pareto optimal*. If a point x' exists such that by moving from x' to x^* some of the objective functions improve while the others remain unchanged, then the point x^* is called *weak Pareto optimal.* A set of all Pareto optimal points is called a *Pareto frontier* or *Pareto front*. If a point x_1 is better than the point x_2 by some metric in all of the objective functions, it is said that x_1 *dominates* x_2. This concept will be further explored in section 4.

In this dissertation, instead of seeking a single design point as an optimal solution, the concept of a Pareto front will be explored. A Pareto front reveals the performance limits of a certain system and can be used by a designer in a decision making process based on a design objective.

1.2. A brief review of previous work

One common approach to the optimization problem is to restrict the optimization space to available components. A database is created containing the specifications of the components pre-selected by the designer, which is then evaluated typically using a search method. As it will be seen in detail in section 2, 51% of the surveyed papers in the literature (papers published in IEEE Journals and conferences in1995-2011), are limited to commercial off-the-shelf components, while in 18% of the papers a combination of

component-level analysis and component selection from a database are used. For instance, in the works of Dialynas and Zafiropoulos [7], Blaabjerg *et al.* [8, 9], Ejjabraoui *et al.* [10], Rigbers [11] and Yeung *et al.* [12], commercial off-the-shelf components were used for semiconductor switches. In the works of Busquets-Monge *et al.* [13-16] and Zhang Jun *et al.* [17-20], all of the components have been selected from commercial off-the-shelf products.

Another common trend observed in the literature is that in most of the papers a single component or a portion of the whole converter is the subject of the design optimization. This trend can be seen in 76% of the studied papers. For example, in the works of Bryant *et al.* [21-24], Pasterczyk *et al.* [25], Yuming *et al.* [26], and Wang *et al.* [27-30] , a combination of an IGBT and a diode, output filter of a single-phase inverter, the MOSFET in a DC-DC converter, and front end passive components in a voltage-source inverter are optimized, respectively. This approach might overlook some of the tradeoffs in the design, which, in turn, might result in suboptimal designs.

1.3. Thesis objective

It was explained in section 1.2 that the common approach in optimization of power electronic converters is to use a database of commercial off-the-shelf components. This approach, while useful in tweaking a product design, does not offer insight into a truly optimized converter, since constraining the selection set to commercial components limits the ability to find ultimate performance limits that may require advances in component technologies which will outperform the best in class of the existing available technologies. However, in order to find true performance limits of a power electronic converter, not

only the design space of the converter (with component part numbers as free variables) should be explored, but also the design space of the component technologies should be examined and inspected. Thus, a key outcome of the approach of this work is an understanding of R&D opportunities at the device level to support optimized converters.

Delving into the component technologies requires extensive mathematical modeling of the components, which is an essential part of this approach. The goal of mathematical modeling is to bridge the gap between low-level attributes of components and performance-level attributes of the converter. However, in some cases a direct relationship between these two types of attributes is not very easy to obtain for various reasons. In this dissertation, these reasons and an alternative approach (Technology Characterization Methods – TCM) to resolve this issue are also presented.

Figure 1-1 illustrates two different approaches towards the optimization and how they are linked. A top-down approach is essentially the breaking down of a system to gain insight into its components. In a top-down approach, the system is formulated without

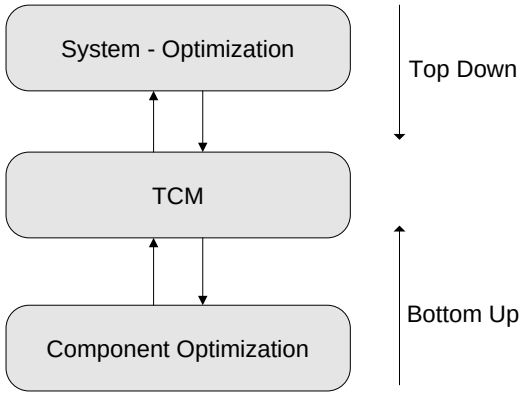


Figure 1-1. Relationship between system-level optimization and component-level optimization

getting much into details of the components. Each component is then studied in detail, until the entire system is reduced to base elements. A bottom up approach is putting smaller systems together to give rise to a grander system. The approach taken in this dissertation develops a direct link between low-level (bottom-up) and performance-level (top-down) attributes, which is not currently established.

The key contributions of this dissertation can be summarized as follows.

- The approach of this dissertation uses descriptive language (mathematical modeling) for the components in a power electronic converter, while the existing approach restricts the optimization space to available "catalog" components. Therefore, the approach presented in this dissertation identifies opportunities for component improvements. The approach of this dissertation, also, holistically considers the entire converter for multi-objective optimization.
- The approach of this dissertation develops a direct link between component-level and performance-level attributes. Technology Characterization Methods are used in order to establish this link wherever this link does not exist.

Portions of this dissertation have been published previously in [31-33].

1.4. Overview of optimization of power electronic converters

Power electronic converters are often optimized on an application-by-application basis. For example, in one design, efficiency and cost may be of importance with size and weight left unconstrained [25] while in another, efficiency and size be the most important

attributes [34]. In many cases, these objectives are not orthogonal but can be formulated in the context of either a multi-objective function, with weighting values given to each attribute [9], or a constrained optimization where one attribute is optimized subject to a constraint on another [35]. An example may be "highest efficiency subject to a maximum cost" as a constrained optimization, or identifying the cost/benefit for best price-performance tradeoff. These two approaches can generate different designs, depending on the desired outcome.

Like every other machine, power electronic converters are comprised of basic building blocks called components. Understanding these building blocks is essential to the optimization of power electronic converters. Different component categories are presented in below.

- **Power electronic switches** come in different types and ratings for different applications, and are the most important components in a converter. Diodes, Power MOSFETs, Insulated Gate Bipolar Transistors (IGBTs), Silicon-controlled rectifiers (SCRs) and Bipolar Junction Transistors are among the most popular ones. Power electronic switches contribute largely to power losses, thus, heat dissipation in the converters.
- **Magnetic components,** or transformers and inductors, contribute largely to the weight and volume and sometimes power loss of power electronic converters. Transformers are used for stepping up or down the voltage, providing electrical isolation, or as energy storage devices (in the case of a flyback converter). Inductors are used as energy storage devices and ripple or harmonic filters.

- **Capacitors** are usually used as ripple or harmonic filters. They come a variety of technologies such as electrolytic, plastic film, ceramic, tantalum, paper oil, etc. They contribute to the size and loss in the power electronic converters. Electrolytic capacitors are specifically known to be highly failure-prone components [31].
- **Thermal management components,** such as heat sinks and fans, are used to transfer heat generated by power loss away from the power electronic switches in order to keep their junction temperature below a maximum value. They contribute to the size and losses of the converters.
- **Gate drivers** are used to switch power switches on and off. Their contribution to power losses is mainly visible in the low-power applications while their contribution to the size of the converter is almost constant for switches of a certain rating in a specific application, and therefore, does not play a major role in the optimization.
- **Control** section of power electronic converters contributes little to the power losses of the converter, and usually is independent in terms of power losses and size from the power stage rating of the converter.

This dissertation will only take into account optimization of power train of power electronic converters in the presence of a known control scheme. In other words, this dissertation will focus on finding an optimum design for the power processing stage of the power electronic converter. Controls are excluded since the developmental roadmaps for digital devices such as DSPs and microcontrollers tend to increase functionality with reduced cost and can leverage economies of scale from other electronic market sectors.

1.5. Dissertation outline

In order to conduct the stated research objectives, the remainder of this dissertation is organized as follows.

In section 2, a literature review of optimization in power electronic converters is presented. Statistical analysis on different categories of papers published in IEEE journals and conferences is provided, and a complete survey of component modeling techniques in optimization of power electronic converters is performed.

In section 3, a review of optimization algorithms used throughout this dissertation is presented. Two different categories of search methods were introduced, and Particle Swarm Optimization, Genetic algorithm, PSO-aided random sampling and Non-dominated Sorting Genetic Algorithm –II (NSGA-II), which are used throughout this dissertation, are discussed in detail.

In section 4, the concept of Technology Characterization Methods (TCM) is introduced and the necessity of TCM in optimization of power electronic converters is discussed. TCM is applied to two different components (IGBT and heat sink), and the resulting models are used in efficiency-volume optimization of a single-phase inverter.

In section 5, a photovoltaic module-integrated inverter is optimized for efficiency, volume and reliability. A new technique to address the challenge of power decoupling is introduced, and multi-objective optimization is performed by means of a three-dimensional Pareto front. A prototype is also constructed in order to experimentally verify the modeling.

In section 6, a new approach to evaluate efficiency in photovoltaic converters is presented. This approach, which uses the actual recorded data of a photovoltaic module, is used as a performance index in the optimization of a flyback converter, and it is shown that the proposed approach provides a more accurate efficiency evaluation in comparison with the existing approach.

Section 7 is a summary of the relevant conclusions and possible extensions that can be drawn from the work presented in this dissertation.

2. OPTIMIZATION OF POWER ELECTRONIC CONVERTERS – A LITERATURE REVIEW

2.1. Introduction

This section presents results and analysis from a literature search of the publications written on the design optimization of the power stage of the power electronic circuits. Thus, the scope of the optimization considered in this section is limited to the publications related to design optimization of the power stage of the power electronic circuits, which explicitly excludes three other categories of optimization found in the literature:

- Incremental improvement to a specific performance index, which do not fall into a rigorous optimization problem.
- Optimization of the controller and control algorithm in which the performance indices are limited to the controller itself.
- Optimization of the performance indices of the whole converter (efficiency, cost, etc.) through changing controller parameters (i.e., controller tuning).

Thus, papers included in this study pertain to optimizing the whole or a part of the power stage of the power electronic circuit. The search methodology was as follows; a search with "Power Electronics" AND "Optimization" in IEEExplore website returned 3,686 papers in total. Other search terms were also examined. Table 2-I shows the number of papers retuned for different search terms.

Table 2-I. Number of papers retuned for different search terms

Search terms	Number of papers returned
Optimization AND Power Electronics	8,810
Optimization AND "Power Electronics"	3,686
Optimization AND Converter	2,912

The initial screening process focused on the optimization in power electronics and returned 363 papers. Out of these 363 papers, 305 papers (84%) were published in journals and conference proceedings of IEEE Power Electronic Society, and 58 papers were published in journals and conference proceedings of other IEEE societies. In the second screening process, the definition of optimization in (1-1) was used as the criteria and returned 104 papers in total in the time frame of 1995 to present, which all have been included in the reference section. These down-selected papers comprise the dataset for this survey which will explore the trends, similarities and differences in the techniques. Figure 2-1 shows the total number of the power stage design optimization papers per year, which shows a cyclical but increasing publication count, underscoring the increasing

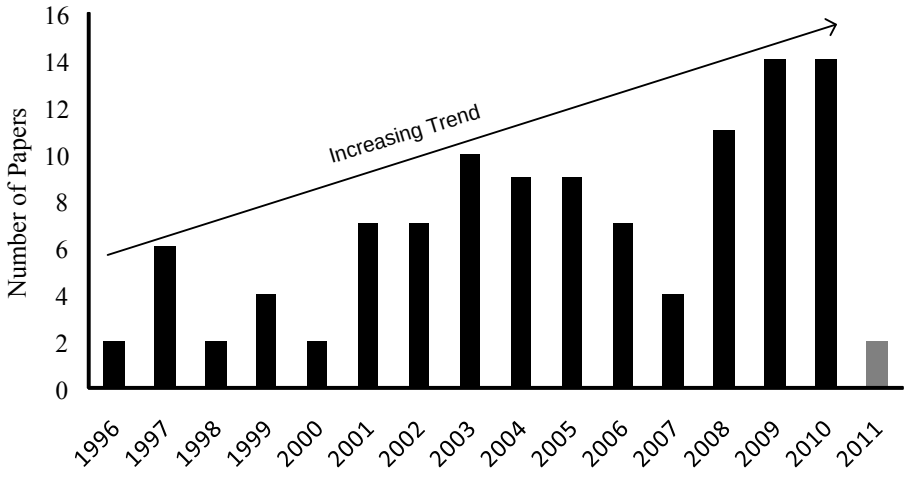


Figure 2-1. Number of power train design optimization papers per year

importance and interest in optimization.

In this section, first, statistical analysis of design optimization papers and critical analysis of relevant works in the literature will be presented. Due to the importance of component modeling, a survey on component modeling will also be presented.

2.2. Survey of the literature

While all of the papers falling into this group discuss a design optimization of a power electronic circuit to some extent, they fall into a variety of categories based on different aspects of the approach taken. This section groups the literature into the following five categories:

1. Optimization scope
2. Optimization objective
3. Optimization detail
4. Class of the converter
5. Optimization approach

2.2.1. Optimization scope

Papers have been categorized based on their design variables and whether their design variables are from a single component, multiple components (usually a portion of the circuit) or all of the components of the full circuit. Figure 2-2 shows the distribution of the papers based on this criterion.

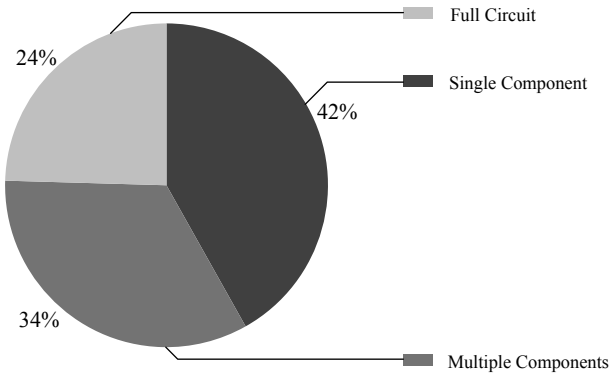


Figure 2-2. Distribution of papers based on the scope of the optimization

Those papers which have attempted to optimize the whole converter usually have a considerable portion dedicated to modeling of the entire circuit with design variables from all (or almost all) of the components.

2.2.2. Optimization objective

There are many common tradeoffs known in power electronic circuits, which may require multi-objective optimization. For instance, using iron-powder cores in inductors might decrease the volume of the inductor considerably, but, on the other hand, it might increase the core losses and therefore decrease the efficiency. However, a large group of papers has only a single objective in their cost function, which is usually based on the specific application of the converter. Figure 2-3 shows the number of papers with single, two or three or more optimization objectives.

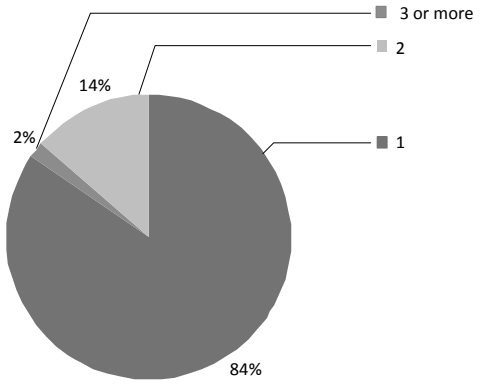


Figure 2-3. Distribution of papers based on number of optimization objectives

Analysis shows that most of the papers have efficiency as their optimization objective which indicates that energy efficiency is still the biggest design challenge. Figure 2-4 shows the distribution of the papers based on their objective. The efficiency is the energy efficiency of the converter, size is either volume or mass of the converter, cost is the value of money used to build the converter, harmonic content is the amplitude of voltage or current waveforms which are of frequencies other than the fundamental

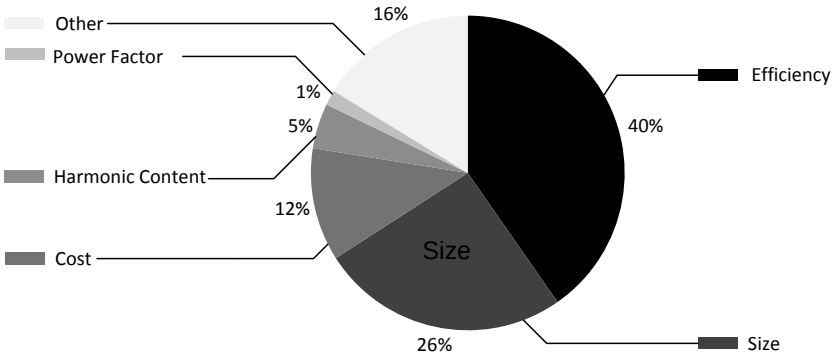


Figure 2-4. Distribution of the papers based on the objective function

frequency, and power factor is defined as the ratio of active power to the apparent power.

2.2.3. Optimization detail

The optimization literature examine different levels of modeling for different components. While transformers and inductors are designed and modeled in detail [25], capacitors and power electronic switches are usually selected from a catalog [25]. Figure 2-5 shows the distribution of the papers based on their modeling detail.

The papers that fall into the "gross specification" category simply have component values or their part numbers taken from a database as the optimization result, as would be done in an *ad hoc* component substitution approach. Papers in the "detailed" category attempt to model the individual components themselves. The output of such approaches includes design of the components and not just a selected value or a part number. Papers in the "Mixed" category have some of their components detailed-designed and some chosen from a database.

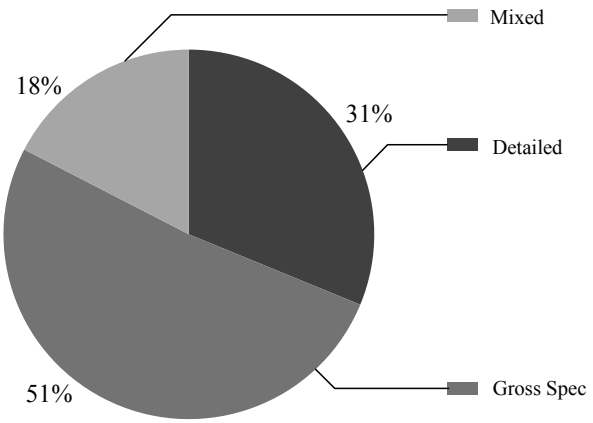


Figure 2-5. Distribution of papers based on level of modeling detail

2.2.4. Class of converter

Papers are also categorized based on the class of converter being optimized. Figure 2-6 shows the distribution of papers based the class of the converter. The converters were divided into classes based on their input and output voltage. DC-DC converters convert a DC input voltage to a DC output voltage with a different magnitude. AC-DC converters, or rectifiers, convert an AC voltage to a DC voltage, and DC-AC converters, or inverters, convert a DC voltage to an AC voltage. The "other" category includes the optimization literature in which a portion of the converter is optimized, and that portion is not specific to any of the three other classes.

2.2.5. Optimization approach

Two major groups of approaches can be taken toward solving the problem of optimization. The first group uses a gradient-based approach, which is usually based on a mathematical concept, to move towards the optimum point. The other approach uses either a blind search or non-gradient-based search method to achieve this goal, which is

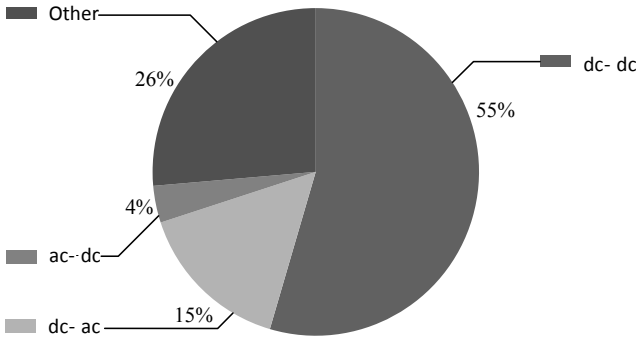


Figure 2-6. Distribution of papers based on the type of converter

easier to use in the optimization of power electronic converters since only the value of the objective function (and not any of its derivatives) is required. The popularity of non-gradient-based search methods have been on the rise in the past decade thanks to the dramatic increase in the processing speed of digital computers. Figure 2-7 shows the distribution of the papers based on the optimization approach.

Table 2-II summarizes the different categories along with citations to corresponding references.

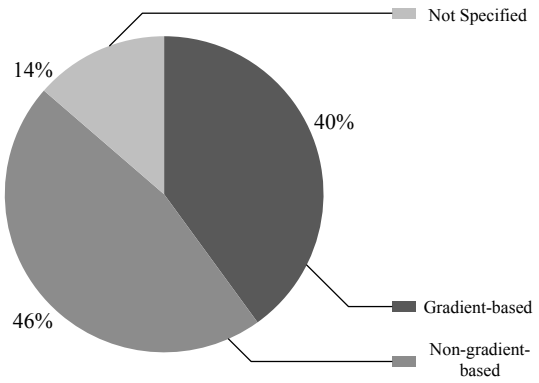


Figure 2-7. Distribution of papers based on the optimization approach

2.3. Critical analysis of the relevant literature

The focus of this dissertation is on component level optimization of the power train for power electronic converters. A brief review of relevant papers may be useful and will be presented in this section.

Table 2-II. Summary of different categories of papers in power electronic optimization

Category	References
Scope	
Full	[7-20, 30, 34-45]
Single component	[23, 46-89]
Multiple component	[21, 24-28, 90-120]
Number of objectives	
1	[7-9, 11-21, 23, 24, 26-28, 35-38, 41, 42, 44, 45, 47-53, 55-80, 82-87, 89-98, 100, 102-105, 107-109, 112-118, 120]
2	[10, 25, 34, 39, 40, 43, 46, 54, 81, 88, 101, 106, 110, 111, 119]
3 or more	[30, 99]
Modeling detail	
Mixed	[10, 13-16, 27, 28, 34-42, 45, 90, 120]
Detailed	[21, 24-26, 43, 47, 51-53, 56, 57, 59-65, 67-69, 71, 72, 74, 75, 77, 80-82, 87, 88, 106, 112]
Gross spec	[7-9, 11, 12, 17-20, 23, 30, 44, 48-50, 54, 55, 66, 70, 73, 76, 78, 79, 83-86, 89, 91-105, 107-111, 113-119, 121]
Class of converter	
dc-dc	[10, 12-21, 23, 24, 26, 34, 36-42, 44-46, 48-51, 56-59, 63, 65, 67, 69-73, 77-79, 81, 85, 89, 91, 94, 95, 99-102, 104, 108, 112, 113, 120]
dc-ac	[8, 9, 11, 25, 27, 28, 30, 43, 61, 66, 83, 84, 92, 93, 105, 106, 109]
ac-dc	[35, 47, 114, 119]
other	[7, 52-55, 60, 62, 64, 68, 74-76, 80, 82, 86-88, 90, 96-98, 103, 107, 110, 111, 115-118]
Optimization approach	
gradient-based	[13, 14, 25, 47, 49, 51, 53-57, 59, 61, 63, 66, 70-72, 75-82, 85, 88, 90, 94-97, 100-103, 105, 106, 110-112, 114]
non-gradient-based	[7, 10-12, 15-21, 23, 24, 26-28, 30, 43, 44, 50, 52, 58, 60, 62, 64, 65, 67-69, 73, 74, 86, 87, 89, 91-93, 96, 98, 99, 104, 107-109, 113, 115-120]
Not specified	[8, 9, 34-42, 45, 46, 83, 84]

Busquets-Monge *et al.* performed an optimization on a boost PFC converter, specifically on the boost inductor and EMI filter [13-16]. The cost of the converter was chosen as the objective function, and the EMI filter capacitance and inductance values, boost inductor parameters, switching frequency and the sink to ambient resistance of heat sink are taken as design variables, but capacitors and other components are selected from commercial off-the-shelf products, and semiconductor parts are pre-selected before the optimization. Zhang Jun *et al.* used Ant Colony Optimization for a typical power electronic converter [17-20]. Their work is significant because they performed a thorough optimization on all of the components; however, all of the components are chosen from commercial components and the focus is mostly on the optimization method.

A noteworthy work in this field was reported by Kolar *et al.* [42]. In this work, a boost PFC rectifier is optimized through detailed analysis of the components. Efficiency and power density were chosen as performance indices, and performance limits were explored using the Pareto front concept [122]. Component-level analysis has been done for all of the components, including the semiconductor switches and the capacitors. For MOSFETs, a figure of merit has been developed based on MOSFET chip area, and for capacitors, the energy density of electrolytic and film capacitors versus their voltage rating have been extracted. However, many of the models (e.g. switching losses) are only exclusive to the studied topology and cannot be used elsewhere.

In [7], a static transfer switch, which is a fast switch used to connect an alternative feeder to a load when the main feeder is lost, was optimized for reliability and cost. Standard reliability models (e.g. reliability of series or parallel components) were

deployed along with the commercial off-the-shelf component data. In the work of Blaabjerg and Pedersen [8, 9], efficiency of a voltage source inverter was optimized, but the focus was mostly on the semiconductor switching losses, and most of the other components were selected from commercial off-the-shelf components. Ejjabraoui *et al.* performed a thorough work on efficiency optimization of a DC-DC converter [10]; however, there was no component level analysis for the semiconductor switches, and they were chosen from off-the-shelf components. This also can be seen in works of Rigbers [11] and Yeung [12]. The former performed an efficiency optimization on an inverter while the latter focused on design of a switch-mode power supply with efficiency as the performance index to optimize.

Bryant *et al.* published a series of papers regarding efficiency optimization of a combination of an IGBT and a diode in a chopper cell [21-24]. The most important aspect of their work is considering device level parameters such as the drift region doping, the width of the die and high-level lifetime in optimization of the semiconductor components; however, they excluded the rest of the components in the converter. In the works of Pasterczyk *et al.* [25, 106], a PWM inverter was optimized for cost and efficiency. A detailed component level model was used for inductors and capacitors; however, power electronic switches were chosen from the off-the-shelf components. Takayama and Maksimovic presented a work in which power stage of a monolithic buck converter was optimized for efficiency [112]. Several dimensions of the monolithic buck converter were taken as design variables; however, the approach and the models can only be applied to a similar type of converter.

Wang *et al.* published a series of papers in power electronic optimization. In [27, 28], front end passive components were optimized for volume in a voltage-source inverter; the capacitors were chosen from off-the-shelf components; however, the inductors were designed in detail. In [29], an EMI filter was optimized for cost or size for a motor drive. Capacitors were chosen from catalog components while inductors were designed in detail. these three works were accumulated in [30], which presents optimization of a motor drive using genetic algorithms. Other than the magnetic parts, all of the other components were chosen from the off-the-shelf components. In the work of Yu et al [120], efficiency of a forward converter was optimized in three different load levels. The switching frequency and the design parameters of inductor and transformer (number of turns, core dimensions and etc.) were chosen as design variables but the other components were pre-selected.

2.4. Survey on component modeling

The evolution of digital computers made it possible to use advanced numerical and stochastic techniques for optimization of complex power electronic circuits. Advances in modeling techniques also resulted in more accurate models and therefore, a more accurate optimization. However, despite advances in modeling power electronic converters, only a limited class of models can be used for the optimization purpose due to the repetitive nature of optimization algorithms. Modern optimization algorithms, gradient-based or non-gradient-based, search for the optimal point moving from a candidate point to another, which makes it nearly impossible to use highly-accurate detailed models such as the ones obtained from Finite Element Analysis or similar techniques. Therefore,

modeling usually comes down to one or a set of algebraic (or in rare cases differential or integral) equations which are much easier to evaluate in a computation-intensive optimization problem. This section presents a study of the modeling approaches used in the design optimization of power electronic converters.

In the optimization problem defined in (1-1), objective function *f(x)* creates a mapping between the design variables and the design objective. This mapping is created using models of the components with regard to operation of the converter. For example, if energy efficiency of a converter is being considered as the design objective, loss models of individual components with regard to effective voltages and currents across the converter create a mapping between the design variables (e.g. component values) and the efficiency. Component models may also be used in defining constraints. For example, in order to check if a certain LC filter complies with IEEE 519 [123] or any other harmonic standard, a detailed model of the inductor, which takes AC resistance of the inductor winding for each harmonic frequency, is required. The optimization problem is then solved using either a gradient-based (e.g. Newton's method, Gradient Descent method or sequential quadratic programming, etc. [5]) or non-gradient-based (Simulated Annealing, Genetic Algorithm, Particle Swarm Optimization, etc. [124-126]) method. These methods *search* for an optimal point by means of an iterative approach, which involves evaluating the objective function one or more times in every iteration.

Similar to any other form of modeling, in power electronics, there is usually a tradeoff between the accuracy of the model and the number of the variables considered. Dynamics of the system are usually simplified (or entirely ignored) in order to develop a

reduced-order and hence, faster way of modeling A model derived from finite element analysis, for example, takes into account a fine mesh inside of each different material in the component as well as a large number of material properties. Such highly-accurate models may not be useful for the purpose of the optimization, since they are computation-intensive and time consuming. Therefore, optimization problems usually use simpler techniques, which involve mostly algebraic or simple differential or integral equations. Finding and categorizing such models is the subject of this section. A wide variety of techniques might be used in order to find a reduced order model for the optimization. For instance, Steinmetz equation is derived from curve fitting to a data series given by test measurements; Dowell equation is derived from solving diffusion equation in 1-D (and ignoring the 3-D nature of the problem), and considering a fixed forward voltage drop for a power diode simply ignores the slight variation in the voltage drop which can be calculated by using device physics equations.

Models can be studied based on the performance index which the model is used to calculate. In the next subsections, the following aspects of models are discussed:

2.4.1. Loss Mechanisms – Different phenomena that contribute to losses in power electronic circuits and approaches to model those phenomena.

2.4.2. Size modeling – Calculating weight and/or volume of the converter from a set of design variables.

2.4.3. Cost modeling – Different factors which are considered to affect the cost of the converter

2.4.1. Loss mechanisms

2.4.1.1. Core losses in inductors and transformers

Inductors and transformers are very common components in power electronic circuits and contribute to the power losses especially in high frequency converters. There are two mechanisms for the core losses: eddy current losses and hysteresis losses. While these losses are well studied under single frequency sinusoidal magnetic fields [127], the models and results are not generally applicable to switching power supplies. Due to the nonlinear nature of hysteresis losses, it is not possible to apply superposition principle in case of a non-sinusoidal field. Therefore, methods other than those applicable to sinusoidal excitation are mostly used to calculate core losses in magnetic components.

2.4.1.1.1. Steinmetz equation

The Steinmetz equation is used to calculate core losses when the magnetic field is sinusoidal. The basic form of the Steinmetz equation is:

$$P_{Core} = K \cdot f^{\alpha} \cdot B^{\beta} \tag{2-1}$$

where P_{core} is the volumetric core loss, f is the frequency of sinusoidal excitation waveform, B is the peak flux density of the core α, β and K are coefficients specific to core geometry and usually determined by curve fitting to the data provided by the manufacturer. Once the Steinmetz parameters are identified, either given explicitly by the manufacturer or found from curve-fitting the manufacturer's data plots, it is straightforward to calculate the core losses. A main limitation is that this equation is only good for sinusoidal excitation voltage and can be used whenever applicable. In [39, 68,

77, 128], the basic form of Steinmetz equation is used to calculate core losses in a resonant converter. In [42], this equation is used to calculate core losses in the AC side of a boost PFC converter. In [67], this equation is used based on an approximation, which neglects high-frequency effects. In [99], this equation is used to calculate core losses in a DC-DC converter, and it is claimed that it is given in the core datasheet, which is no longer available in the provided web address and finally in [60], core losses in a high frequency transformer are calculated using this equation; however, the magnetic field waveform of the transformer is not specified. In [52], the Steinmetz equation is used to calculate core losses in a transformer. The flux density is calculated from core geometry and excitation in [129] and used in the equation.

2.4.1.1.2. Modifications to Steinmetz equation

In most typical power electronic circuits, the magnetic cores are exposed to non-sinusoidal magnetic fields. Thus the basic Steinmetz equation does not predict core losses accurately under non-sinusoidal excitation. In [35, 37, 38, 40, 41, 45, 121, 130], a modified form of the Steinmetz equation, which is developed in [131], is used. In this modified form, instead of using frequency, the time-rate of change of flux density (dB/dt) is used to calculate the core loss:

$$P_{Core} = K_1 \cdot \left|\frac{dB}{dt}\right|^{\alpha} \cdot (\Delta B)^{\beta-\alpha} \qquad (2\text{-}2)$$

where ΔB is the peak-to-peak flux density and K_1 is calculated so that the modified equation is consistent with the original Steinmetz equation for sinusoidal waveforms. In [11, 110, 111, 120], another form of the modified Steinmetz equation, which is introduced

by Albach *et al.* [132], was used. In this work, an equivalent frequency is derived for the arbitrary waveform, which is used with the original Steinmetz equation, and the effects of temperature are also considered. In [10, 101, 102], a generalization of the Steinmetz equation based on [133], which seeks to calculate core losses in discontinuous (DCM) and continuous (CCM) conduction mode for a buck converter, is used. In these calculations, core losses in DCM depend only on the frequency and the maximum flux density, while in CCM, they depend on frequency, maximum flux density and flux density changes.

Jieli *et al.* [63] also use a generalization of Steinmetz equation based on their own work [134]. In this generalization, time average of core losses over a period is calculated from equation below:

$$P_{Core} = \frac{1}{T}\int_0^T K_1 \cdot \left|\frac{dB}{dt}\right|^{\alpha} \cdot \left|B(t)\right|^{\beta-\alpha} dt \qquad (2\text{-}3)$$

where, K_1 is calculated such that (2-3) is consistent with the original Steinmetz equation (2-1) under sinusoidal excitation. In [65], a modified Steinmetz equation is used, which is introduced in [135]. In this modified equation, an equivalent frequency is derived for non-sinusoidal waveforms, which is basically an integral form of the piecewise linear equation presented in [132]. A quadratic term was also added to the original Steinmetz equation because of the geometry effects. In [43], an equation, which is used, which is introduced in [136]. This equation, called Natural Steinmetz Equation, uses the assumption that the core losses depend on flux density and its rate of change instead of the fundamental frequency:

$$P_{Core} = \left(\frac{\Delta B}{2}\right)^{\beta-\alpha} \cdot \frac{K_N}{T} \int_0^T \left|\frac{dB}{dt}\right|^{\alpha} dt \qquad (2\text{-}4)$$

K_N is calculated in a way that (2-4) is consistent with original Steinmetz equation for sinusoidal excitation. Another modified version of the Steinmetz equation was used in [27, 28]:

$$P_{Core} = \alpha \cdot k \cdot (\beta \cdot f)^m \cdot \Delta B^n \qquad (2\text{-}5)$$

Although this equation appears structurally similar to the original Steinmetz equation (2-1), it is claimed that coefficients α and β compensate for the non-sinusoidal excitation [27, 28]. Waveform Coefficient Steinmetz equation is introduced in [137], and as the name implies, losses are calculated by multiplying a factor to the original Steinmetz equation. The factor is calculated from the flux waveform. Table 2-III summarizes modifications to the Steinmetz equation.

2.4.1.2. Copper losses in windings

Copper losses are a considerable portion of the total losses of the magnetic components. Generally, power losses in a current conductor can be calculated by multiplying the resistance by the square of the current. However, the conductor current and the current flowing in the adjacent conductors create a magnetic field, which leads to eddy current flowing in the conductor and therefore, additional losses in the conductor. Additional losses due to the conductor current and current flowing in adjacent conductors are called skin and proximity effects respectively. These two losses are highly frequency dependent, and since high frequency waveforms are very common in power electronics, these effects must be considered if an accurate loss prediction is required. Due to the linear nature of

Table 2-III. Major modifications to Steinmetz equation

Designation	Additional Consideration	Formula
Modified Steinmetz equation[132, 135]	*dB/dt*	$f_{eq} = \frac{2}{\Delta B^2 \pi^2} \int_0^T (\frac{dB}{dt})^2 dt$ $P = k \cdot f_{eq}^{\ \alpha-1} \cdot \hat{B}^{\beta} \cdot f_r$
Generalized Steinmetz Equation[134]	*B(t)* and *dB(t)/dt*	$P(t) = K_1 \cdot \left\|\frac{dB}{dt}\right\|^{\alpha} \cdot \left\|B(t)\right\|^{\beta-\alpha}$ $P = \frac{1}{T} \int_0^T P(t) \cdot dt$
Natural Steinmetz Equation[131, 136]	*dB(t)/dt*	$P_{Core} = \left(\frac{\Delta B}{2}\right)^{\beta-\alpha} \cdot \frac{K_N}{T} \int_0^T \left\|\frac{dB}{dt}\right\|^{\alpha} dt$
Waveform coefficient Steinmetz Equation [137]	A correction factor (Flux Waveform Coefficient)	$P = FWC \cdot K . f^{\alpha} \cdot B^{\beta}$ e.g. $FWC_{square} = \frac{\pi}{4}$

eddy current losses [127], superposition can be applied for calculation of the copper loss, unlike in the case of core losses. Different approaches taken in the optimization papers are reviewed below and also summarized in Table 2-IV.

2.4.1.2.1. Dowell equation

The Dowell equation is a generalized form of the solution for the diffusion equation of rectangular conductors adapted and applied to round conductors [127]. In this equation, instead of calculating losses directly, the "AC resistance" of the conductor is calculated. The ratio of this resistance to the DC resistance is given as:

Table 2-IV. Summary of copper losses

Reference(s)	Description
[43, 53, 60, 68, 77, 120]	Calculated from Dowell equation
[35, 37-41, 128, 130, 138]	Equivalent resistance calculated from current wave shape and Dowell equation
[80-82]	Equivalent frequency derived based on current wave shape. Resistance then calculated from Dowell equation
[11, 42, 48, 58, 63, 65, 67, 72, 73, 89, 92, 93, 95, 99]	Dc resistance used- high frequency effects neglected
[69]	Single-frequency resistance used- higher-frequency effects neglected
[10, 101, 102, 139]	Comprehensive analysis done for a flyback transformer
[52, 129]	Comprehensive analysis for a low profile transformer
[45, 110, 111, 140, 141]	Losses calculated from 2-D solution of diffusion equation
[27, 28, 62]	DC and eddy current losses calculated separately, superposition used for eddy current losses
[88, 142]	An analytical technique used- claimes to be faster than solving diffusion equation 2-D but with a good accuracy

$$F_R = \frac{R_{ac}}{R_{dc}} = A\left[\frac{\sinh 2A + \sin 2A}{\cosh 2A - \cos 2A} + \frac{2(N_l^{\,2} - 1)}{3} \cdot \frac{\sinh A - \sin A}{\cosh A + \cos A}\right] \tag{2-6}$$

where A is given:

$$A = \frac{\pi}{4}^{\frac{3}{4}} \cdot \frac{d}{\delta_\omega} \tag{2-7}$$

and d is the conductor diameter, δ_ω is the skin depth, and N_l is the number of layers in a multilayer winding. This equation is widely used in the literature along with the Fourier

analysis and superposition of the current waveform [43, 53, 60, 68, 77, 120]. In the case of a non-sinusoidal current, AC resistance should be calculated separately for each frequency in the frequency spectrum, which requires that the circuit be solved for each frequency separately. The total copper losses can be obtained using superposition principle, i.e. summing up losses of the circuits of each individual frequency. This approach, while accurate, increases the computing time and might be burdensome for an optimization algorithm.

Another approach, which is based on the Dowell equation, is to calculate the effective total resistance based on the current waveform. This approach is taken in [35, 37-41, 128, 130] based on an approach presented in [138], and, in this approach an effective resistance from the RMS current and its derivative is calculated. However, this equation is only useful when the current waveform and its derivative are known. In another approach, based on 1-D solution of diffusion equation, an equivalent frequency is calculated for a non-sinusoidal waveform [80-82]. Current derivatives are also required in this approach.

2.4.1.2.2. Equivalent resistance

In the Dowell equation, eddy current losses and therefore AC resistance are frequency dependent. However, some other papers model the copper losses by a single equivalent resistance. In [63], the DC resistance of the inductor was used, neglecting high frequency effects, reportedly because of low ripple current. In [42, 67] only DC resistance was used, stating explicitly that the high frequency effects are neglected. In [69], the transformer current waveform is considered to be sinusoidal (and confirmed by

measurement), and therefore, an equivalent resistance for sinusoidal waveform is used. In [59], an equivalent resistance is used to model both of the core losses and the copper losses, and the resistance is calculated from curve fitting. In [11, 48, 58, 65, 72, 73, 89, 92, 93, 95, 99] an equivalent resistance is used; however, no reason was specified for neglecting high frequency effects.

2.4.1.2.3. Other copper loss calculation methods

Although the Dowell equation and series resistance approximation are the most common approaches in the literature, other techniques have also been mentioned. In this section those techniques are reviewed.

Copper losses for a flyback transformer are calculated in [10, 101, 102] based on the detailed analysis given in [139]. Main loss mechanisms are studied in detail in [139] using an analytical approach. In [52], an equation for calculating power losses in low profile transformers is given but the comprehensive analysis is given in [129]. In [45], the copper losses are calculated using a 2-D solution of the diffusion equation presented in [141]. The approach of [141] is also used in [140] which gives the detailed loss analysis for [110, 111]. In [27, 28, 62], DC losses and eddy current losses are calculated separately and superposition is applied for eddy current, and finally in [88], an approach introduced in [142] is used, which is claimed to be more accurate than the 1-D solution to diffusion equation while being faster than solving the equation numerically.

2.4.1.3. Semiconductor losses

Calculating semiconductor losses depend on the type of the switch and the circuit. In power electronics, MOSFETs and IGBTs are used widely as primary switches while

diodes are mostly used for freewheeling and providing a return path for the current for one-directional MOSFETs and IGBTs. Losses in semiconductor switches are a considerable portion of the total losses of a power electronic converter, and therefore, precise loss modeling techniques are necessary for accurate loss calculation. Due to the complex nature of semiconductor materials and the large number of parameters involved, it is not always easy to model loss mechanisms based on the geometry or other device level characteristics of the switch. Therefore, most reviewed papers do not include these characteristics as design variables and instead, prefer to choose a switch from a database and hence, calculate losses from information provided in the datasheet. In [8-10, 12, 37-41, 48, 58, 63, 65, 69, 89, 92, 93, 95, 99, 120, 128, 130], at least one portion of semiconductor losses are calculated from the values provided by the datasheet and scaling with current and/or voltage.

2.4.1.3.1. MOSFET losses

MOSFET conduction losses are usually calculated using a simple on state equivalent resistance [10, 35, 37-42, 48, 58, 59, 63, 65, 69, 71, 72, 89, 95, 99, 112, 120, 128, 130]. In most of the papers, this resistance ($R_{ds,ON}$) is obtained from the datasheet and multiplied by RMS current square to calculate conduction losses [10, 37-41, 48, 58, 59, 63, 65, 69, 89, 95, 99, 120, 128, 130]. Some of the other papers attempt to calculate or scale $R_{ds,ON}$ based on some device-level characteristics or operational characteristics of the MOSFET. In [35], $R_{ds,ON}$ is obtained from the datasheet but is scaled with junction temperature of the MOSFET. In [65], $R_{ds,ON}$ is scaled with the maximum blocking voltage of MOSFET. In [42] $R_{ds,ON}$ is calculated from the MOSFET chip area. In [71, 72], $R_{ds,ON}$

is calculated from the MOSFET width, and in [112], $R_{ds,ON}$ is calculated from the MOSFET width and applied gate voltage. In [11, 45], $R_{ds,ON}$ is calculated from junction temperature and load current based on values extracted from the datasheet. A summary of calculating conduction losses for MOSFETs, excluding the ones purely extracted from the datasheet, is given in Table 2-V.

Table 2-V. Summary of conduction losses in MOSFETs (Excluding references calculating losses directly from datasheet values)

Reference(s)	Description
[35]	$R_{ds,ON}$ is scaled with junction temperature
[65]	$R_{ds,ON}$ is scaled with rated voltage
[42]	$R_{ds,ON}$ from MOSFET chip area
[71, 72]	$R_{ds,ON}$ from MOSFET die width
[112]	$R_{ds,ON}$ from MOSFET die width and applied gate voltage
[11, 45]	$R_{ds,ON}$ from Junction temperature and current extracted from datasheet

MOSFET switching losses depend highly on the type of the converter and its control strategy. In hard switched converters, the energy loss during one cycle is calculated using either the equivalent capacitance [42, 48, 51, 59, 71, 72, 89, 112] or rise and fall time of the MOSFET voltage and current [10, 58, 65, 92, 93, 95, 99]. In some other papers, turn-on and/or turn-off energy is directly used to calculate the switching losses [11, 63, 120] scaling them with voltage or current. Like $R_{ds,ON}$, MOSFET capacitance are taken from the datasheet in some papers [48, 59, 89] while in some others,

it is calculated or scaled from device level characteristics. In [51], capacitances change with width and length of each MOSFET; in [71, 72, 112], capacitances are calculated from width of the MOSFETs, and in [42] they are calculated from area of the MOSFET.

In soft switched converters, however, calculating switching losses cannot be done using the above-mentioned approaches. Therefore, a detailed loss analysis or empirical equations are required for these type of converters. In [35, 37-41, 45, 128, 130], empirical equations have been derived from measurement and curve fitting to express switching losses, and in [44], a model for a series-parallel resonant converter presented in [143] is used. a summary of methods for calculating MOSFET switching losses is presented in Table 2-VI.

2.4.1.3.2. IGBT losses

Unlike MOSFETs, IGBT forward voltage drop is not purely resistive. Different

Table 2-VI. Summary of MOSFET switching losses

Reference(s)	Description
[48, 59, 89]	From Capacitance values obtained from datasheet
[10, 58, 65, 73, 92, 93, 95, 99]	From rise time and fall time obtained from datasheet
[11, 63, 120]	Switching energy is scaled with voltage and current
[51]	Capacitance values scaled with length and width of MOSFET die
[71, 72, 112]	Capacitance values from width of MOSFET die
[42]	Capacitance values calculated from chip area
[35, 37-41, 45, 128, 130]	Empirical equation for soft-switched converters
[143]	Model for a series-parallel resonant converter

ways of modeling IGBT conduction losses in papers related to power electronic optimization can be summarized as follows. In [8, 9], forward voltage drop of the IGBT has a constant and a nonlinear term:

$$V_F = V_0 + r_0 \cdot I_L^{B_{con}} \quad (2\text{-}8)$$

where I_L is the IGBT current,V_0 is the fixed portion of forward voltage drop, B_{con} is a constant found from curve fitting and r_0 is called *dynamical resistance* is a function of gate drive voltage. A similar equation is used in [66] which is based on the model provided in [144], but details on finding the parameters are not given. Considering $B_{con}=1$ the second term in forward voltage drop becomes resistive, which is the base of the approach used in [43]. In this approach, fixed part of the forward voltage drop is derived based on the switching characteristics of the IGBT using a surface fitting approach and from available commercial samples. The resistive part is derived from the commercial samples using the maximum current of the IGBT.

A complete loss model for IGBT and diode is used in [21, 23, 24] which is based on the model presented in [22, 145, 146]. This model uses MATLAB/Simulink for modeling losses based on certain physical attributes of the IGBT such as active area and width of the IGBT die, doping level and high-level carrier lifetime. This model is good for an IGBT and a diode in a chopper cell; however, as explained in the paper, most power electronic circuits can be reduced to a chopper cell for the purpose of modeling and optimization. This model is able to calculate both conduction and switching losses. Linear interpolation is used in [30] to find turn-on and turn-off energy losses considering the effect of the gate resistance. Loss calculation for IGBTs is summarized in Table 2-VII.

Table 2-VII. Summary of loss calculation in IGBTs

Reference(s)	Description
[8, 9, 66, 144]	• Forward voltage drop: a fixed part and a nonlinear part • Nonlinear part is a function of gate resistance and load current • Switching losses from datasheet values and parasitic component values
[43]	• Conduction and switching losses inter-dependent • Dependence of fixed part of forward voltage drop to switching times. • Resistive part of forward voltage drop is a function of maximum current
[21-24, 145, 146]	• A comprehensive model using device-level parameters
[8, 9, 43, 92, 93]	• Switching losses from datasheet values
[25, 106]	• Switching energy from a nonlinear equation based on current.
[30]	• Switching losses from linear interpolation based on gate resistance

2.4.1.3.3. Diode

Diode conduction losses are usually calculated using a fixed forward voltage drop for the diode in on state which is usually extracted from the datasheet [35, 37-43, 58, 65, 69, 99, 128, 130]. In some of the papers, a resistive or nonlinear term is also added to this fixed voltage drop [10, 11, 45, 66]. Other approaches used are using Shockley equation for diode voltage drop instead of a fixed voltage [48] and a comprehensive loss analysis for IGBT and diode as explained in previous section [21, 23, 24]. Summary of diode losses is presented in Table 2-VIII.

Table 2-VIII. Summary of diode losses

Reference(s)	Description
[35, 37-43, 58, 65, 69, 99, 128, 130]	Fixed voltage drop from datasheet
[10, 11, 45, 66]	Fixed part and a resistive or nonlinear term
[48]	Shockley equation for diode voltage drop
[21-24, 145, 146]	A comprehensive model using device-level parameters

2.4.1.3.4. Gate drive losses

Even though gate drive losses usually contribute little to the total power losses, they might be of significance especially in a low power [71, 112] or high efficiency [35, 37, 38, 130] converter. Gate drive losses are almost exclusively calculated using the gate capacitance, gate voltage and frequency [37, 38, 71, 112, 130]. In [112] this capacitance is calculated from the geometry of a monolithic buck converter. Gate drive losses are also considered in [35] but the details are not given. Summary of gate drive loss calculation is given in Table 2-IX.

2.4.1.3.5. Capacitor losses

Capacitor losses are usually calculated considering an equivalent series resistance

Table 2-IX. Summary of gate drive losses

Reference(s)	Description
[37, 38, 71, 130]	From gate capacitance, gate voltage and frequency (from datasheet)
[112]	Gate capacitance is calculated from geometry for a monolithic buck converter

(ESR) for the capacitor [25, 35, 37-41, 43, 58, 68, 73, 89, 95, 106, 110, 111, 128]. This resistance represents the power losses in the capacitor which is due to some resistive losses because of the resistance of conducting material and also dielectric losses. If the former part is neglected, series resistance can be expressed as:

$$ESR = \frac{\tan \delta}{C \cdot \omega} \qquad (2\text{-}9)$$

where C is the capacitance, ω is the frequency in radians and $tan\ \delta$ is the loss angle which is nearly constant for a certain type of dielectric. In [35, 37-41, 68, 110, 111, 128] ESR due to the dielectric losses is calculated from the (2-9), while in [58, 73, 89, 95], no detail is given on how to calculate the ESR. In [25, 106] a resistance is added to the ESR to represent the losses due to resistivity of conducting parts which is calculated from capacitor geometry for a wound metalized film capacitor. A similar approach for the same type of capacitor with different set of equations is used in [43] which is based on the analysis presented in [147, 148]. A summary of capacitor loss calculation techniques is given in Table 2-X.

Table 2-X. Summary of capacitor losses

Reference(s)	Description
[35, 37-41, 68, 110, 111, 128]	• ESR calculated from *tan δ*
[25, 43, 106, 147, 148]	• ESR calculated from *tan δ* and capacitor geometry

2.4.2. Weight and volume modeling

2.4.2.1. Inductors and transformers

Inductors and transformers are usually custom designed in power electronic design, and therefore, their size (weight or volume) can be calculated from their geometry, which is a part of the design variable set. This approach is taken in [27, 28, 39-43, 45, 46, 53, 56, 57, 68, 77, 83, 84, 87, 97, 100, 110, 111, 128, 130]. In one paper, volume of the inductor is calculated from the area product of the inductor core which can be considered indirect calculation from geometry [45]. In [68, 110, 111] the volume of an integrated LC module is calculated from the core and the winding geometry.

The size of the magnetic components is calculated from other approaches if geometric parameters are not a part of the variable set. In [76, 91], Inductor volume is calculated from the stored energy, while in [76], it also depends on the inductance and maximum current. In [10, 90, 101, 102], the inductor volume is calculated from an empirical equation based on the inductance, maximum current and maximum flux density and in [99] inductor volume is directly extracted from a catalog of off-the-shelf components. A summary of size modeling for the magnetic components is given in Table 2-XI.

2.4.2.2. Capacitors

Unlike inductors, capacitors are not normally custom designed and therefore, their volume should be approximated, if not extracted directly from a catalog, which is the case in [10, 27, 28, 99, 130]. Other approaches include calculating capacitance volume from its

Table 2-XI. Summary of modeling size of magnetic components

Reference(s)	Description
[27, 28, 39-43, 45, 46, 53, 56, 57, 68, 77, 83, 84, 87, 97, 100, 110, 111, 128, 130]	From geometry
[68, 110, 111]	From geometry for an integrated LC module
[76, 91]	From stored energy
[10, 90, 101, 102]	From inductance, maximum current and maximum flux density
[99]	Directly from component catalog

stored energy [42, 76, 91] or from an empirical formula based on its capacitance obtained from a curve fit or given by the manufacturer [39-41, 83, 84, 90, 97, 100, 102, 128].

In some of the papers, however, capacitors are also custom designed and therefore, their volume is calculated from their geometry. In [56, 57] an integrated LC filter is designed and therefore, the total volume is calculated from the geometry of the components including the capacitor. A planar integrated passive module is designed in [110, 111] in which the total volume depend on geometry of the integrated components, i.e. capacitor and inductor, and in [43], volume of a film capacitor is calculated directly from its geometry. Capacitor modeling techniques are summarized in Table 2-XII.

2.4.2.3. Heat sink

Calculating heat sink size from analytical equations for heat dissipation is very complicated since heat sinks come in a wide variety of shapes which makes it difficult to

Table 2-XII. Summary of modeling size of capacitors

Reference(s)	Description
[10, 27, 28, 99, 130]	Size extracted directly from catalog
[42, 76, 91]	From stored energy
[39-41, 83, 84, 90, 97, 100, 102, 128]	Empirical equation based on capacitance
[56, 57]	From geometry for an integrated LC module
[110, 111]	From geometry for a planar integrated passive module
[43]	From geometry for a film capacitor

tie their thermal resistance to their weight or volume. Therefore, some estimation techniques are applied in power electronic optimization papers. In [10], heat sink volume is estimated from the required thermal resistance and in [101, 102] the size of the heat sink is somehow estimated but not explained. In [39-42, 128, 130], a concept called *CSPI* (Cooling System Performance Index), which is presented in [149], is used. *CSPI* is defined as follows:

$$CSPI = \frac{1}{R_{th,s-a} \cdot V_{CS}} \tag{2-10}$$

where $R_{th,s\text{-}a}$ is the surface-to-ambient thermal resistance and V_{CS} is the volume of the heat sink. According to [149], a higher *CSPI* means a higher power density for the converter in which the heat sink is used. Therefore, the approach in [39-42, 128, 130] is to use a heat sink with higher *CSPI*. Finding the volume of such a heat sink is then reduced to find the

surface-to-ambient thermal resistance required by semiconductor switches. Size modeling methods of heat sinks are listed in Table 2-XIII.

Table 2-XIII. Summary of size modeling for heat sinks

Reference(s)	Description
[10]	Estimated from thermal resistance
[39-42, 128, 130, 149]	A Cooling System Performance Index (CSPI) introduced for each heat sink. Optimization looks for higher CSPI

2.4.3. Cost modeling

Cost of the converter is an important objective function in many of the designs. In fact, high production costs may be a barrier for using some technologies which are desirable for certain applications. Due to the complexity of the pricing process in which economics is involved, most of the power electronic optimization papers either use the component cost (i.e. price) from catalogs or use a curve fit to find the cost from certain attributes of the components. In [7, 25, 99, 106], the price of commercial off-the-shelf components are used as their cost while in [98, 107, 117], the cost of resistor, inductor and capacitor is approximated from their resistance, inductance and capacitance respectively. In [13-16], cost of the components is approximated from the cost of actual off-the-shelf components; however, no detail is given on which attributes have been taken into account. In [81, 82, 88], cost of stranded wires is estimated from their diameter and number and in [45], cost of a semiconductor die is estimated from its surface area. A summary of cost modeling methods is presented in Table 2-XIV.

Table 2-XIV. Summary of cost modeling

Reference(s)	Description
[7, 25, 99, 106]	From price of off-the-shelf components
[98, 107, 117]	Cost of passive components is approximated from value
[81, 82, 88]	Cost of stranded wire estimated from strand diameter and number
[45]	Cost of a semiconductor chip is estimated from surface area

2.5. Conclusions from literature review

Based on what mentioned in previous subsections, some conclusions can be drawn about optimization of power electronic converters.

2.5.1. Design variables

Design variables are variables whose values can be freely varied by the designer to define a designed object. Magnetic components are usually custom-designed in power electronics and therefore, most papers of the literature have magnetic component properties, such as number of turns, core dimensions, air gap length and etc. in their design variables. However, with some exceptions, component level variables are not used in the case of semiconductor switches, capacitors and heat sinks due to the fact that they are not usually custom-designed. In other words, usually only design variables that can be changed in the power electronic lab environment are chosen as degrees of freedom. For semiconductor switches, due to the complex nature of semiconductors, little work has

been done that presents a relationship between device level characteristics of semiconductor devices and their circuit behavior. For instance, even though a tradeoff between IGBT speed and forward voltage drop has been known for many years, lack of an easy way to estimate IGBT losses from its device level attributes limits the research work to existing semiconductor devices. Modeling semiconductor devices with a deeper look into semiconductor physics will help the researchers to explore the whole design space of semiconductor devices and not only the commercial off-the-shelf components. Modeling heat sinks is also very important in calculating the total size of the converter but little attention has been paid to the cost and size modeling of heat sinks. This might be because of difficulty of modeling thermal conduction in heat sinks and incorporating such analysis into a power electronic design problem. However, due to the significance of heat sinks in total weight and volume of power converters, a descriptive modeling technique can be useful.

Capacitor losses are calculated from a very simple equation, (2-9), which only accounts for dielectric losses. Conduction losses due to the resistance of conducting part might be significant. Moreover, (2-9) is only valid when capacitor is carrying a sinusoidal current, and superposition cannot be applied due to the dielectric losses being nonlinear by nature. A solution to this problem will also be beneficial for power electronic design optimization.

2.5.2. Performance indices

Performance indices are characteristics of the device which the designer wants to optimize. Efficiency and size (or power density) are the most popular performance

indices; however, component level analysis is minimal when cost is chosen as the optimization objective. This may be due to the fact that analysis of cost depends on many economic factors and requires a multi-disciplinary research. Analysis on cost modeling techniques also show that most of the models for cost either use the inflated price or are very simplistic.

2.5.3. Constraints

Constraints are the limitations in the design which make certain designs invalid. There are generally two types of constraints in power electronic optimization. The purpose of the having the first group usually is to make sure that the devices operate in their safe or linear area. This group includes constraints on the junction temperature and maximum voltage and current of semiconductors, voltage rating of magnetic components and capacitors, maximum flux density in magnetic cores and etc. The second group represents standards which have to be met such as harmonic current levels, power factor for a rectifier and etc. boundaries set for variables define the design region and not treated as constraints.

3. OPTIMIZATION ALGORITHMS

An optimization algorithm or search method is used to find the local minimizer or search for a global minimizer for the problem (1-1) or find a set of equally good solutions to the problem (1-2) as a form of a Pareto front. There are many different types of optimization algorithms in the literature. This section will discuss of the search methods focusing more on the methods used in this dissertation.

The optimization algorithms are divided into two categories: gradient-based algorithms and non-gradient-based algorithms. Gradient-based algorithms are usually based on a mathematical concept, while non-gradient-based algorithms are based on a heuristic process. Since non-gradient-based algorithm optimization algorithms use the value of the objective function only, they are considered easier to formulate when the objective function is discontinuous or has integer variables. Therefore, in this dissertation, search methods such as Particle Swarm Optimization [125] and Genetic algorithm [124] are used. Since original form of Particle Swarm optimization can only be used for single-objective optimization, it is combined with a random sampling approach to make it suitable for multi-objective optimization. Since the original Genetic algorithm is also suitable for single-objective optimization only, a modified version of genetic algorithm called Non-Dominated Sorting Genetic algorithm - II (NSGA-II) is used.

The remainder of this section is organized as follows. In subsection 3.1, two categories of optimization algorithms will be introduced and the original forms of Genetic

algorithm and Particle Swarm Optimization will be introduced. In subsection 3.2, the PSO-aided random sampling and NSGA-II algorithm will be presented.

3.1. Single-objective optimization

There is a variety of search methods for a single-objective optimization problem. These search methods fall into two categories: gradient-based search methods which are based on a mathematical concept or non-gradient-based search methods which are usually based on a heuristic process.

One of the simplest forms of the gradient-based search methods is gradient steepest descent method. In this method, the next point is selected based on the gradient of the objective function at the current point. In other words, in step *k*, a search is conducted in the direction of $-\nabla f(x^k)$ which is the negative of the gradient of the objective function at point x^k. The basic idea for this method is that the objective function can be estimated by the first two terms of its Taylor series. This method (and other methods based on the gradient) needs the gradient of the objective function to be calculated. The minimize, which is found by this method, also hugely depends on the starting point [5].

In Newton's method, the Hessian matrix of the objective function is used to improve convergence with regard to the gradient method. In this method, in step *k*, the step p^k is calculated from:

$$p^k = x^{k+1} - x^k = -\nabla^2 f(x^k)^{-1} \cdot \nabla f(x^k) \qquad (3\text{-}1)$$

where $\nabla^2 f(x^k)$ is the Hessian of function *f* and for a function with *n* variables is defined as:

$$\nabla^2(x^k)=\begin{bmatrix} \frac{\partial^2 f}{\partial x_1^{\,2}} & \frac{\partial^2 f}{\partial x_1 \partial x_2} & \cdots & \frac{\partial^2 f}{\partial x_1 \partial x_n} \\ \frac{\partial^2 f}{\partial x_2 \partial x_1} & \frac{\partial^2 f}{\partial x_2^{\,2}} & \cdots & \frac{\partial^2 f}{\partial x_{21} \partial x_n} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{\partial^2 f}{\partial x_n \partial x_1} & \frac{\partial^2 f}{\partial x_n \partial x_2} & \cdots & \frac{\partial^2 f}{\partial x_n^{\,2}} \end{bmatrix} \qquad (3\text{-}2)$$

Newton's method has a faster convergence than gradient-based methods [5]. Newton's method is based on the three-term approximation of the Taylor series of function f. Both of gradient and Newton's method can only be used in unconstrained optimization.

For constrained optimization, however, *Lagrangian* function may be used to calculate the search directions. Lagrangian function is obtained from combining the objective function and constraints:

$$L(x,\lambda)=f(x)+\lambda^T g(x) \qquad (3\text{-}3)$$

where λ is a vector of scalar values called Lagrange multipliers. The step p^k is then calculated by:

$$p^k=\begin{bmatrix} x^{k+1} \\ \lambda^{k+1} \end{bmatrix}-\begin{bmatrix} x^k \\ \lambda^k \end{bmatrix}=-\nabla^2 L(x^k,\lambda^k)^{-1}\cdot\nabla L(x^k,\lambda^k) \qquad (3\text{-}4)$$

It can be shown that if $\nabla L(x^k,\lambda^k)=0$, which is true for the solution of the problem using (3-3) and (3-4), it implies that all of the constraints are met [5]. This method is called Sequential Quadratic Programming (SQP) and is essentially is the adaptation of Newton's method to the constrained optimization. Since SQP is used for constrained optimization, it can be used for power electronic optimization problems provided that the

Hessian matrix can be calculated. However, this matrix is impossible to calculate for problems with discontinuity and where integer variables are involved, which is usually the case in power electronic optimization problems. Moreover, like Newton's method, the solution found by the SQP depends largely on the starting point of the optimization. In order to explore the whole design region, one might run the SQP algorithm with different starting points, which may jeopardize the speed of the algorithm which is its major strength.

Non-gradient-based search methods take a different approach, which is better suited for problems with multiple minima and/or with discontinuous objective function and/or integer design variables [150]. These approaches try to iteratively improve the objective function using only the objective function value and not any of its derivatives. With introduction of digital computers, which resulted in tremendous reduction in computation cost, using these methods have become more popular. In subsections 3.1.1 and 3.1.2, two different non-gradient-based search methods used in this work will be introduced.

3.1.1. Genetic Algorithm (GA)

Genetic Algorithm is a non-gradient-based search method which mimics the natural evolution process. This algorithm became widely popular in 1970s through the works of John Holland and has been widely used in different applications ever since [150].

In genetic algorithm, a population of design points, called a *chromosome,* evolves iteration by iteration to move towards the best solution. The algorithm starts with

randomly generating the starting population in the design range. In each iteration, a subpopulation is chosen to *breed* a new generation. This process is called *selection*. Selection can be done in a variety of methods but usually involves some kind of fitness evaluation combined with a random process [124]. Alternatively, all of the chromosomes of a generation can be used to breed the new generation without selecting any specific ones.

Points from the pool of selected parents are then paired with one another to reproduce the new generation. Two genetic operators are involved in this process: crossover and mutation. Crossover operator combines the genes (i.e. design variables) of two parents. This is usually done by exchanging some of the genes of two parents by a certain probability pc. Mutation operator alters some of the genes of the resulted two offspring by a probability pm to mimic natural mutation. This latter process is necessary so that the algorithm can escape the local optima and continue searching for a global optimum point [124]. The algorithm goes on until a termination condition is met. Figure 3-1 shows a flowchart for genetic algorithm.

3.1.2. Particle Swarm Optimization (PSO)

Particle swarm optimization (PSO) was introduced by Kennedy and Eberhart in 1995 [125, 151, 152] and gained a rapid popularity as a fast optimization techniques for problems with complex objective functions. Like genetic algorithm, PSO attempts to find a global optimum by iteratively improving a solution. The concept behind PSO is biologically inspired by a group of animals such as a flock of birds or a school of fish searching for food and sharing information with each other [152].

The algorithm starts with selecting a set of random points in the design space. In each iteration, three sets of data are updated after evaluating the objective function for all of the points in the population (swarm).

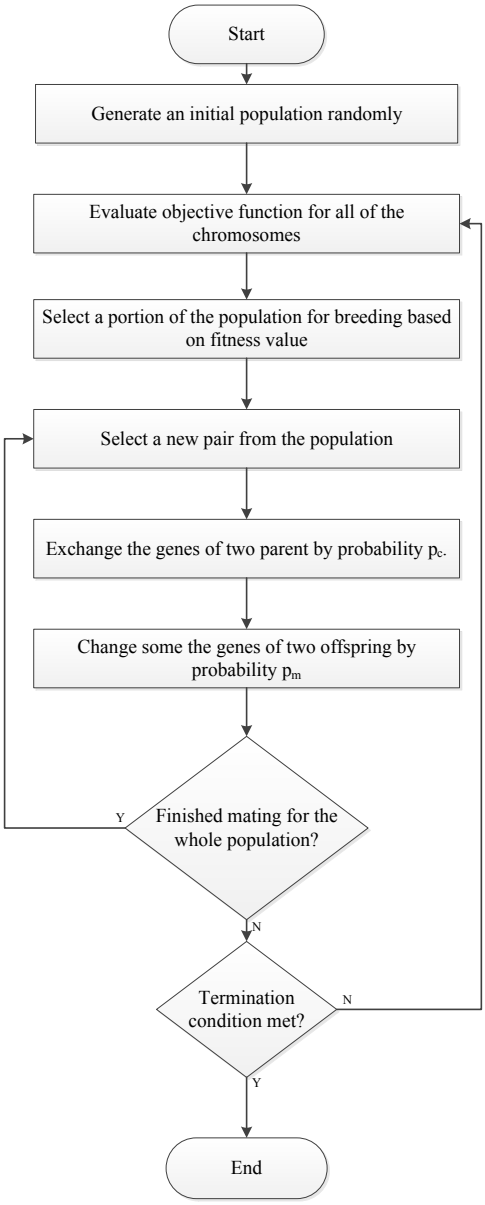


Figure 3-1. Flowchart of genetic algorithm

- **Best point found by each particle**: for each particle in the swarm, the best point ever found by this particle is recorded and updated in each iteration. This set of points is called *pbest*. In the first iteration, the best points are the current points.
- **Best point found by the entire swarm**: this point is called gbest and is the best point ever found by the entire swarm.
- **The velocity:** The velocity of the points is updated by the following equation:

$$V_{t+1,i} = V_{t,i} + C_1 \cdot r_1 \cdot (X_{t,i} - pbest_{t,i}) + C_2 \cdot r_2 \cdot (X_{t,i} - gbest_t) \qquad (3\text{-}5)$$

where $V_{t,i}$ is the previous velocity for particle i, $X_{t,i}$ is the current location of i^{th} member of swarm, r_1 and r_2 are random numbers with uniform distribution and C_1 and C_2 are user-defined constants. The velocity for each point is defined by displacement amount from the previous point and therefore,

$$X_{t+1} = X_t + V_{t+1} \qquad (3\text{-}6)$$

The algorithm is terminated by a user-defined termination function and *gbest* is reported as the optimum point. Figure 3-2 shows a flowchart of PSO.

3.2. Multi-objective optimization

The main difference between single-objective and multi-objective optimization is that in the case of multi-objective optimization, it is not possible to call a solution better than the other if neither is *dominated* by the other. In other words, in multi-objective optimization, there could exist a set of equally-good solutions and not just a single solution. Therefore, search methods such as PSO are not useful in their original form since they rely on the concepts of "better" and "best" in order to work.

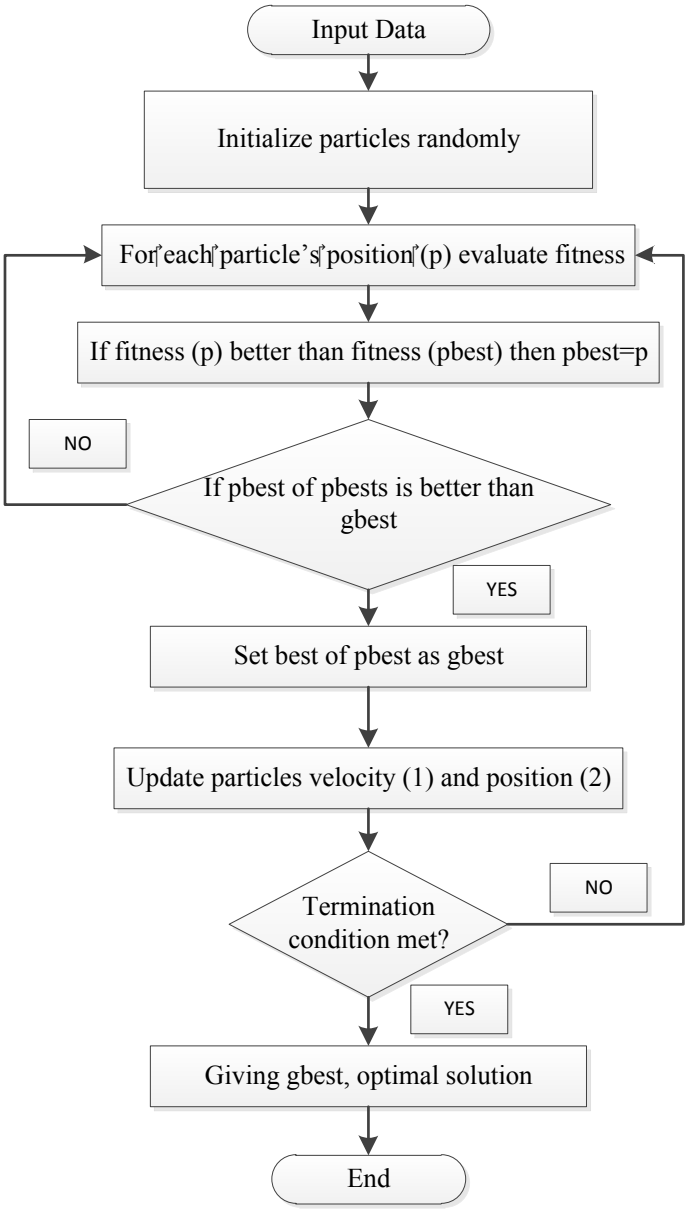


Figure 3-2. Flowchart of Particle Swarm Optimization

One way to make use of single-objective search methods is to assign weighting factors to each of the objective functions and use a single-objective search method to find a solution and then, change the weighting factor and perform the optimization again and

continue until finding enough points to describe a Pareto front. While this method is useful, it is difficult to assign weighting factors when the number of objectives is more than two.

A random sampling technique, which is essentially choosing *n* random points in the design region, can also be used to sample the design space uniformly to find the Pareto front. However, random sampling is a blind search approach and cannot be called an optimization or search algorithm. Moreover, it is not a computationally-efficient method. Therefore, in this work, a PSO-aided random sampling was used. In this search method, the non-dominated points found by random sampling were used as one of the starting points in the initial population of PSO. Normalized weighting factors for objective functions are then set according to the objective function values for the non-dominated starting point. PSO will attempt to push the Pareto front or, in other words, find the real performance limits of the converter. Figure 3-3 illustrates this process.

3.2.1. Non-dominated Sorting Genetic Algorithm-II (NSGA-II)

With rise in the popularity of non-gradient-based search methods, efforts have been made to create algorithms to solve multi-objective optimization problems [153]. In this work, a variation of Genetic algorithm called Non-dominated Sorting Genetic Algorithm – II (NSGA-II) was used. This method was created by Deb *et al.* [154] in 2002 and has been one of the most popular heuristic search methods for the multi-objective optimization.

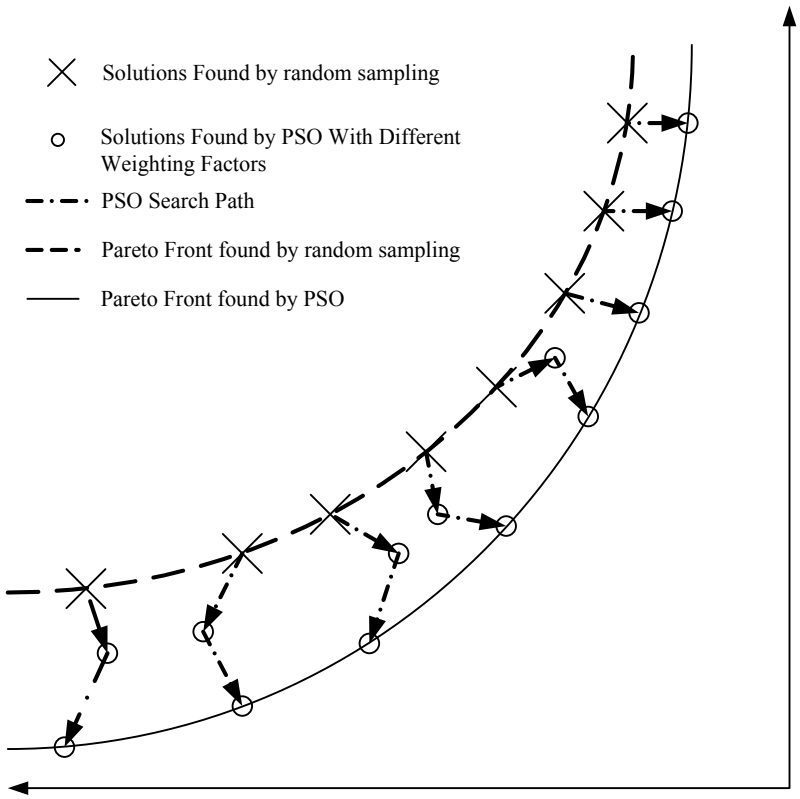


Figure 3-3. PSO-aided random sampling

A major problem in using algorithms such as Genetic Algorithm in Multi-objective optimization is that there is no easy way of declaring a solution better or worse than the other if none is dominated by the other. A multi-objective optimization algorithm, therefore, should find a Pareto front of candidate solution each of which can be considered equally good. The Pareto front should also be spread out throughout the objective function space and not be limited to a small area. The NSGA-II algorithm is used to find a Pareto front with such characteristics.

While NSGA-II uses Genetic Algorithm as its core, two new concepts are added to achieve a good multi-objective optimization. These two concepts are described below.

1. *Non-dominated Sorting:* It is mentioned that in a multi-objective space, no solution can be considered as a better solution than the other if none dominates the other. Non-dominated sorting uses a concept of *ranking* in order to assign a fitness value to each solution in order to facilitate the selection process in the Genetic algorithm. First introduced by [155], ranking concept is basically assigning a rank to each solution based on its domination status. At first, all of the non-dominated solutions are assigned rank 1 and then are temporarily removed from the solution pool. In the remaining solution pool, the non-dominated solutions are assigned rank 2 and this process goes on until no solution is left.

   In NSGA-II finding the rank for each solution (or non-dominated sorting) is done in a faster way which is exclusive to this algorithm. In this approach, all of the non-dominated solutions start with rank 0. Then two entities are calculated for each solution: domination count n_p which is the number of solutions which dominate solution p and S_p which is the number of solutions which p dominates. Now for each solution with n_p=0 each member of its S_p set (q) is visited and its domination count (n_q) is reduced by 1. If for any q, the domination count n_q becomes zero, they are put in another list Q which forms the second non-dominated front. This goes on until all of the fronts are identified and all solutions are assigned with a rank. Although creators of NSGA-II do not call this ranking, it is essentially the same concept as what described in [155]. Figure 3-4 shows the flowchart for non-dominated sorting.

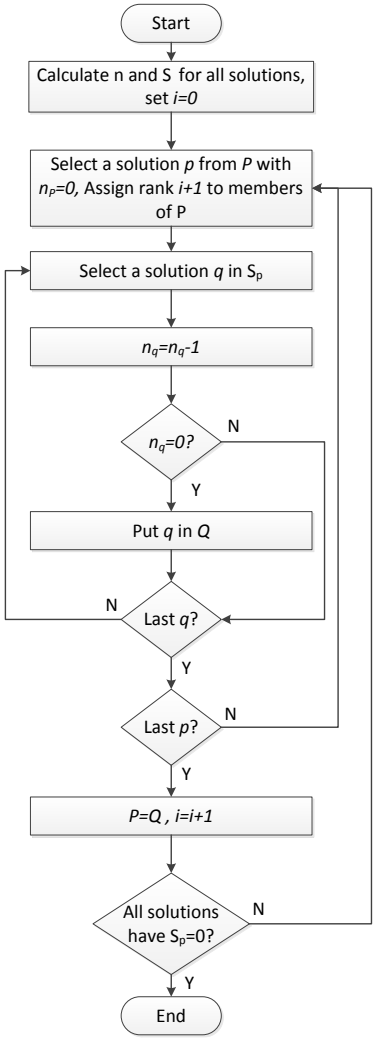


Figure 3-4. Flowchart of non-dominated sorting used in NSGA-II

2. *Crowding distance*: Crowding distance for each solution is defined as the average distance of two solutions on either side of the current solution. According to [154], crowding distance serves as an estimate for perimeter of the cuboid that is formed by two solutions around the current solution. The dashed rectangle in a two-objective problem in Figure 3-5 shows this concept.

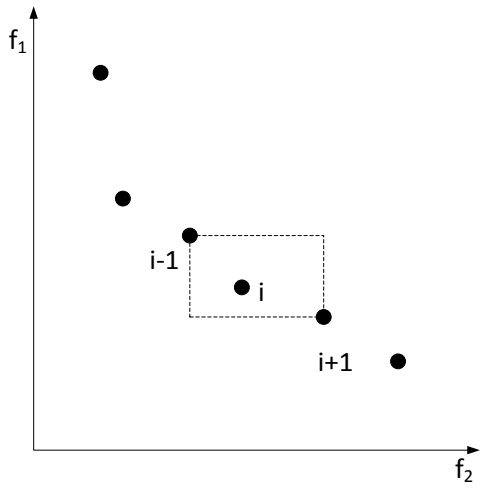


Figure 3-5. Concept of crowding distance [154]

In order to calculate crowding distance, solutions must be sorted along each objective separately for each sorted subpopulation. Take F_i as the i^{th} sorted subpopulation (i.e. with rank *i*). The distance d_{jk} is the distance between *j-1* and *j+1* solutions along objective *k*. for the solutions within F_i with smallest and largest objective function d_{jk} is defined as infinity. The crowding distance is then defined as:

$$d_j = \sum_{k=1}^{m} \frac{d_{jk}}{f_k^{\max} - f_k^{\min}} \qquad (3\text{-}7)$$

The calculation of crowding distance for each sorted subpopulation is illustrated in Figure 3-6.

Using two concepts of non-dominated sorting and crowding distance calculation, it is now possible to explain NSGA-II algorithm. In iteration *t*, parent population P_t and

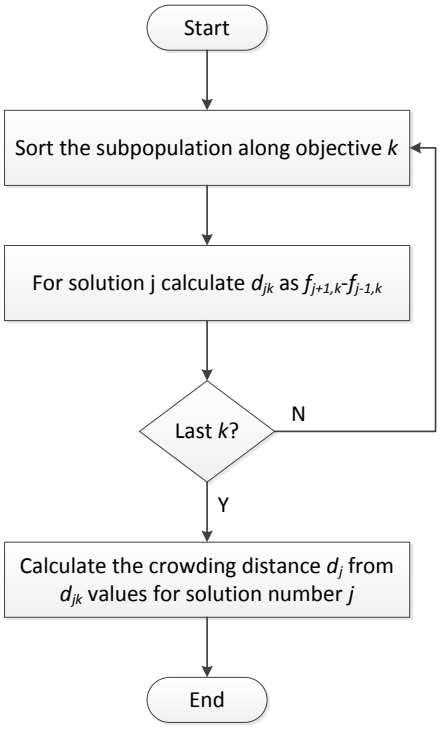


Figure 3-6. Flowchart for crowding distance calculation

offspring population Q_t , each with *N* solutions, are combined to form a bigger population with *2N* solutions. Non-dominated sorting is then performed to find solutions with similar ranks.

Selection process then is performed by selecting solutions with the lowest rank and then solutions with the next lowest rank. This process goes on until the number of solutions in the parent population exceeds *N*. Then, for the latest sorted subpopulation included in the parent population, only the solutions with a larger crowding distance are selected until parent population has exactly *N* solutions. Crossover and mutation operators are then performed to find the next offspring population. Figure 3-7 are shows the flowchart of NSGA-II algorithm.

NSGA-II algorithm is used in last section for multi-objective optimization of a flyback converter.

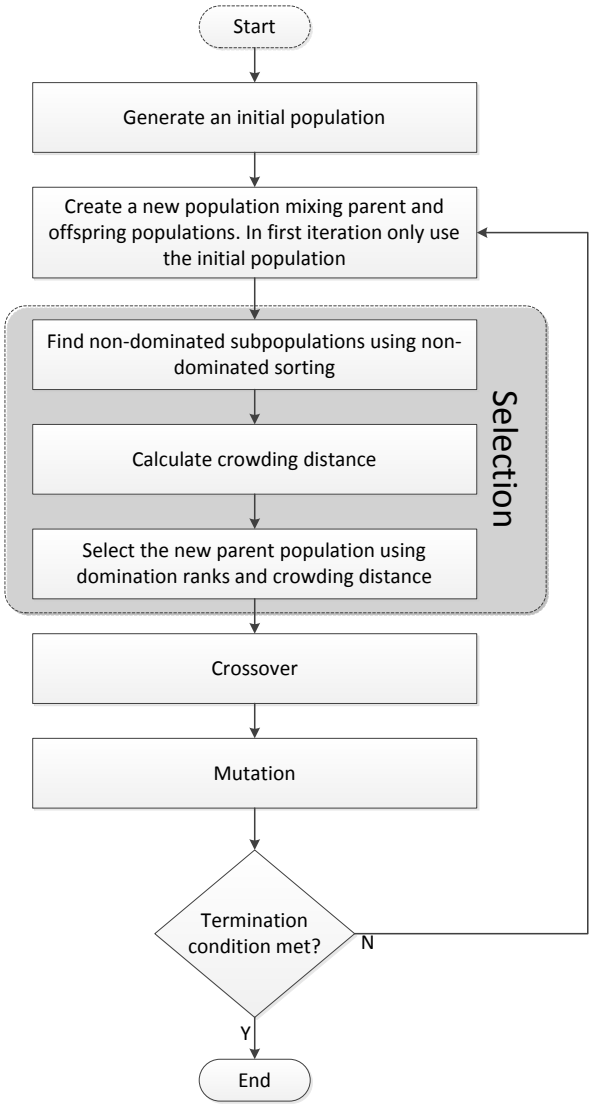


Figure 3-7. Flowchart of NSGA-II algorithm

3.3. Conclusion

Optimization algorithms are used to solve the single-objective or multi-objective optimization problems. In this section, the gradient-based and non-gradient-based optimization algorithms were introduced and the reason for choosing non-gradient-based optimization algorithms was explained. The original form of Particle Swarm Optimization and Genetic algorithm were explained in detail, and finally, PSO-aided random sampling and NSGA-II algorithms were introduced. The former is a combination of random sampling and Particle Swarm Optimization, and the latter is a modified form of Genetic algorithm. PSO-aided random sampling and NSGA-II algorithms are suitable for Multi-objective optimization and will be used in the remainder of this dissertation.

4. DECISION MAKING FRAMEWORK FOR POWER ELECTRONIC CONVERTERS

4.1. Technology Characterization Methods in component modeling

4.1.1. Technology Characterization Methods

The purpose of modeling is to create a mathematical relationship between the low-level attributes of the component, such as doping concentration of the semiconductor, which is of interest to the component designer and performance-level attributes, such as efficiency or switching speed, which is of interest to the power converter designer. Obtaining such a direct relationship is challenging because:

- **Variation of component complexity** – components such as semiconductor switches usually have a large number of design attributes, thus a high degree of freedom, whereas passive components such as inductors and capacitors can be fully characterized using a much smaller set of attributes and a small degree of freedom. Even relatively superficial technology appears simple, such as a heat sink, can be difficult to model due to the large number of degrees of freedom once a detailed model is considered.
- **Homologue** – functionally equivalent components may contain vastly different low-level design attributes. For example the integrated gate bipolar junction transistor (IGBT) may be considered functionally equivalent to the metal oxide semiconductor field effect transistor (MOSFET) even though their low-level attributes are very different, i.e. they can be used as voltage-controlled switches in converters.

- **Proprietary information** – technology details may be proprietary to the designer or the manufacturer. In this case, low-level modeling is challenging due to the lack of widespread knowledge of the technology or accessibility of design data.
- **Lack of data** – low-level data for a specific component technology simply does not exist, or is not comprehensive, as in the case of empirically derived correlations instead of derived from underlying fundamentals of physics.

Figure 4-1 illustrates how Technology Characterization Methods (TCM) can be used in the optimization [156, 157]. The Technology Characterization Method overcomes these challenges by creating a new type of model that captures the underlying component design attributes (low-level attributes) yet presents them in a way that a power converter designer can evaluate the *in-situ* performance attributes. Another advantage of such a modeling technique is that it makes it possible to evaluate components of the same

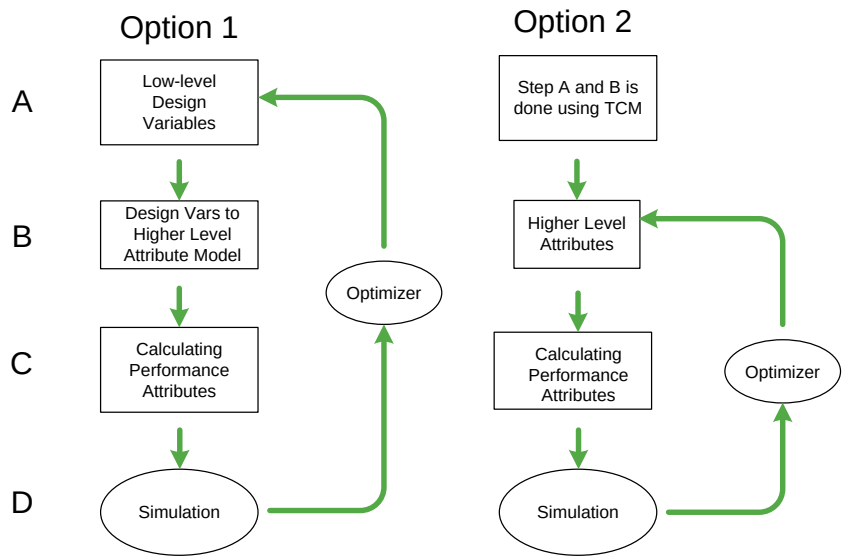


Figure 4-1. Describing Technology Characterization Methods and their usage in optimization

technology class but with slight differences in details using a single model. For example, within the technology class of the trench MOSFET, geometry has a significant effect on attributes such as the input capacitance and output capacitance. From the performance-attribute perspective, the shape of the trench matters only to the extent that it manifests as performance characteristics that affect losses.

Figure 4-2 illustrates two ways of applying Technology Characterization Methods to obtain models suitable for Pareto dominance [122] and nonlinear regression analysis [157]. As illustrated in Figure 4-2, eliminating design points that are dominated by other design points enables a more accurate dependence relationship to be identified. A sample dataset was created to demonstrate the difference between the goodness of fit before and after Pareto dominance analysis. After a quadratic polynomial fit was performed in

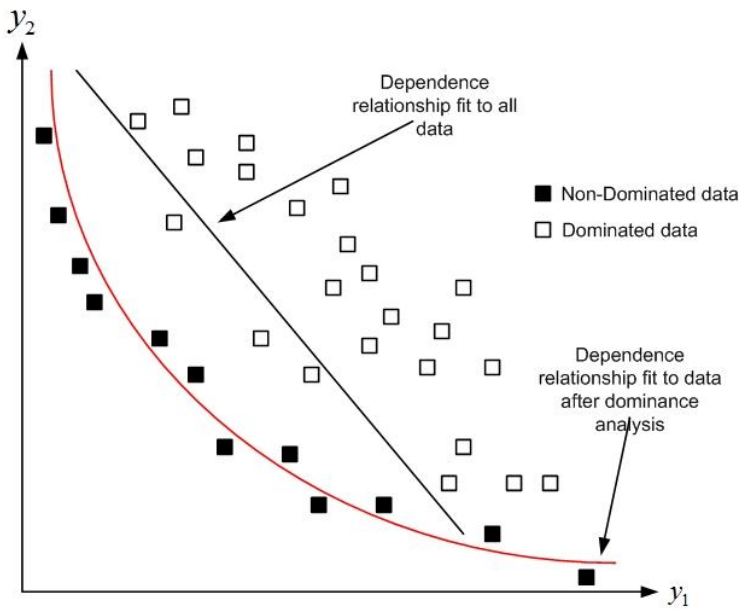


Figure 4-2. An illustration showing the difference between a dependence relationship fit to the full data set compared to the dependence relationship after dominance analysis

MATLAB, the R^2 value before Pareto dominance analysis was 0.3873 but it increased to 0.9464 after the dominance analysis was performed. The next section applies these techniques to semiconductor switches and heat sinks.

4.1.2. Semiconductor switches

Various types of semiconductor switches are used in power electronics and in different applications. One or more type of tradeoff usually exists in these switches. In 'bipolar' family of switches such as IGBTs and P-i-N diodes this tradeoff is between forward voltage drop and switching characteristics of the device (turn-on and turn-off behavior of IGBT and reverse recovery of the diode) [158, 159]. The existence of this tradeoff predicts that an optimal switching frequency must exist so that the total (switching+conduction) losses of a switching device are minimized.

In order to better understand tradeoffs in semiconductor devices, the relevant device models and operation should be explained. Many models have been suggested to calculate forward voltage drop of IGBTs. The simplest method, which will be used in here, is called rectifier-MOSFET model[158, 159]. This model sees the IGBT as a series connection of a diode an a MOSFET (Figure 4-3)

Using this model, it can be concluded that the forward voltage drop of the IGBT has two terms: an almost constant term due to the diode and a voltage drop across the MOSFET channel. Voltage drop across the rectifier part is given by [158]:

$$V_{F,P-i-iN} = \frac{2kT}{q}\ln\left[\frac{J_C W_N}{4qD_a n_i F\left(W_N / 2L_a\right)}\right] \qquad (4\text{-}1)$$

where function F is defined as:

$$F(x) = \frac{x \cdot \tanh(x)}{\sqrt{1 - 0.25\tanh^4 x}} e^{-\frac{qV_M}{2kT}} \qquad (4\text{-}2)$$

where q is the electron charge, T is the temperature, k is Boltzman constant (=1.38×10^{-23}),

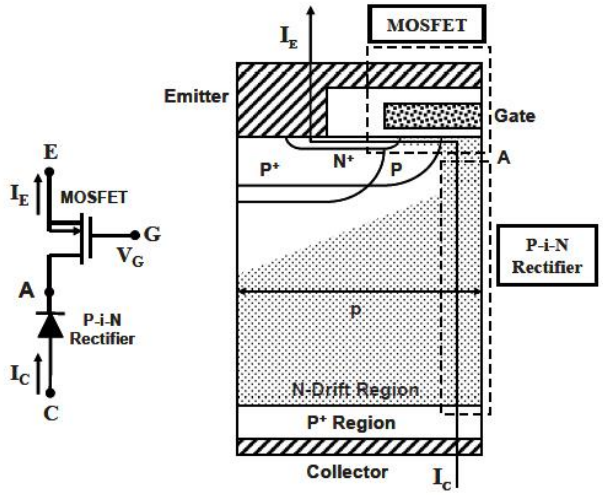


Figure 4-3. ON state equivalent circuit for IGBT [158]

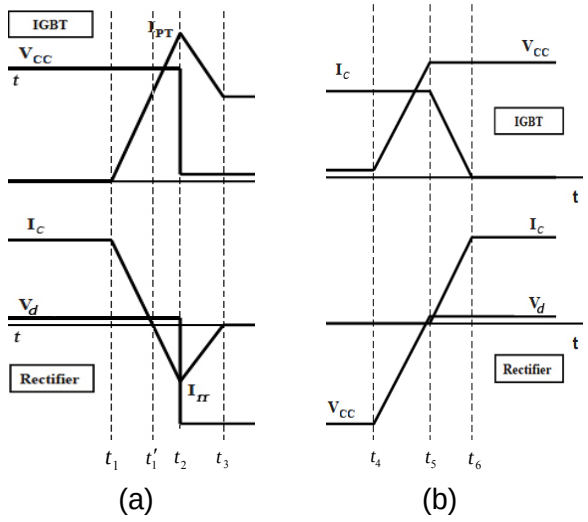


Figure 4-4. Example switching waveforms of the IGBT and anti-parallel diode (a) Turn on (b) Turn off [158]

J_C is the current density, W_N is the width of the drift region, n_i is intrinsic carrier concentration, D_a is ambipolar diffusion constant and V_M is related to the value *x* in *F(x)*. If *x* is smaller or equal to 2 then it is given by:

$$V_M = \frac{2kT}{q} x^2 \qquad (4\text{-}3)$$

Otherwise, it is given by:

$$V_M = \frac{3\pi kT}{8q} e^x \qquad (4\text{-}4)$$

L_a is called *diffusion length* and is given by:

$$L_a = \sqrt{D_a \tau_{HL}} \qquad (4\text{-}5)$$

where τ_{HL} is called *high-level lifetime*, which is a very important factor in forward voltage drop of IGBTs and also their switching behavior. The forward voltage drop due to the MOSFET channel is proportional to the current passing through the IGBT and therefore can be treated as a resistive term. Channel resistance of the MOSFET part can be calculated as follows:

$$R_{CH} = \frac{L_{CH}}{Z\mu_{ni} C_{ox} (V_G - V_{TH})} \qquad (4\text{-}6)$$

where L_{CH} is the channel length, μ_{ni} is inversion layer mobility, C_{ox} is capacitance of the oxide layer, V_{TH} is the threshold voltage, V_G is the gate voltage and Z in the thickness of the semiconductor die.

4.1.2.1. Carrier lifetime [158]

Under equilibrium conditions, there is a balance between the generation and recombination of electrons and holes in semiconductors. This equilibrium is disturbed by an external stimulus. When this external stimulus is removed, the excess carrier density in the semiconductor should decay for semiconductor to return to equilibrium state. This rate of recovery is governed by *minority carrier lifetime*.

Minority carrier lifetime depends of the level of injection of excess carriers. It has been observed that when the injection level is low, minority carrier lifetime becomes a constant value. This value is called *low-level lifetime*. On the other hand, when injection level increases, minority carrier lifetime reaches an upper bound value which is called *high-level lifetime*.

Lifetime of carriers in semiconductors depends on a variety of factors and calculating lifetime from physical properties such as doping concentration. is a very challenging task. However, lifetime control techniques such as injecting impurities and electron irradiation allow us to control lifetime of carriers, which is a very important factor especially in bipolar devices such as IGBTs and diodes.

4.1.2.2. Switching losses

Switching losses associated with an IGBT is divided into two parts: turn on losses and turn off losses. The turn on switching energy according to Fig. 3 can be calculated as follows:

$$E_{on} = \frac{I_{PT} \cdot V_{DC}}{2}(t_2 - t_1) + \frac{V_{ON} \cdot (I_{PT} - I_M)}{2}(t_3 - t_2) \qquad (4\text{-}7)$$

where:

$$I_{PT} = I_{rr} + I_C \tag{4-8}$$

is maximum reverse recovery current of diode and times t_1, t_2 and t_3 are properties of the diode. Therefore, the turn on switching energy losses are determined by the diode rather than the IGBT itself.

Turn-off switching behavior and losses depend highly on the type of the load (resistive or inductive load). Since in power electronic circuits there is always some form of inductance present, it is preferred that turn-off energy loss is calculated for inductive load. Figure 4-4 shows typical turn-off waveforms of the IGBT.

As it can be seen from Figure 4-4, in the first phase of turn-off, voltage rises to its maximum value while in the second phase, current falls to zero in a shape of a tail (which has been simplified in this figure as a line). The length of this current tail is a very important factor in calculating switching losses. Turn-off energy of the transistor can be calculated as follows:

$$E_{off} = \frac{I_M \cdot V_{DC}}{2}(t_5 - t_4) + \frac{V_{DC} \cdot I_M}{2}(t_6 - t_5) \tag{4-9}$$

The turn-off behavior of IGBT also depends on the type of the IGBT used. In asymmetric (or punch-through) IGBTs, since the width of the N-drift region is small, the current tail is shorter than that of symmetric (or non-punch-through) IGBTs in general. It is evident from (4-9) that turn-off energy of the IGBT is a factor of two important times in the turn-off process: turn-off delay time and fall time. These times are, in turn, determined

by carrier lifetime in N-drift and N-buffer regions for symmetric and asymmetric IGBTs. According to [158]:

$$t_6 - t_5 = \tau_{HL,N-Drift} \quad (4\text{-}10)$$

for a symmetric IGBT and

$$t_6 - t_5 = 2\tau_{LL,N-buffer} \quad (4\text{-}11)$$

for an asymmetric IGBT. Turn-off delay time also depends on carrier lifetime in N-drift and N-buffer regions according to [158].

The exact mathematical formulation of this tradeoff is very challenging due to the number of the parameters involved, some of which can only be determined via measurement. The formulation for the tradeoff is also slightly different in each different IGBT technology due to the differences in the structure. Therefore, statistical analysis is performed on a sample of 300 IGBTs from International Rectifiers, Fairchild Semiconductors and ST Microelectronics. The following are the outcomes of this process.

4.1.2.3. Channel resistance

It was seen that channel resistance in the IGBT is inversely proportional to the IGBT die thickness. It is also reported that the IGBT cross section area is normally a factor of its maximum current [158]. Since the width of the IGBT cell is almost constant, the cross section area is a factor of thickness of the die itself. Therefore, it would be expected that the channel resistance multiplied by maximum current should be nearly constant. In order to investigate this, channel resistance was calculated in those IGBTs whose datasheet had the forward voltage drop for two different currents in the same

temperature (73 total). Figure 4-5 shows the distribution of this quantity. The mean value of this quantity is 0.92 V. Since channel resistance has a small contribution to the forward voltage drop, this mean value will be used for different IGBTs. Thus, the channel

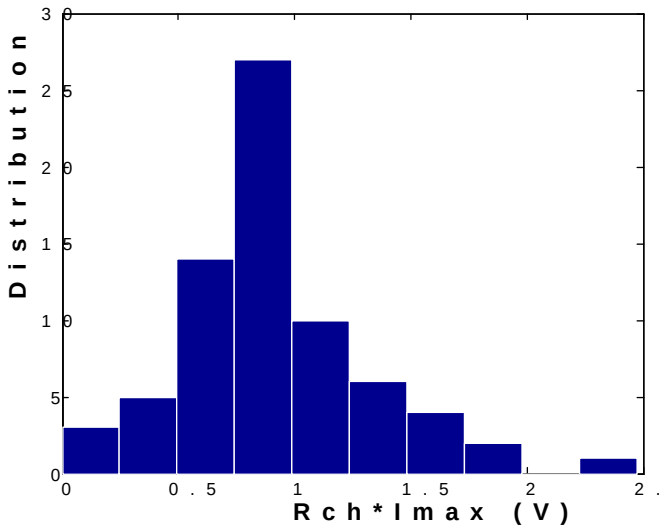


Figure 4-5. Distribution of $R_{CH} \times I_{\max}$

resistance will be obtained by multiplying this mean value to the maximum required current.

4.1.2.4. P-N voltage drop

A 3D space showing turn off delay time, fall time and fixed part of forward voltage drop (due to the P-i-N rectifier in the IGBT structure) is shown in Figure 4-6. A classical Pareto dominance analysis [122] was applied to the data in order to find the non-dominated IGBTs. It should be noted that even though all IGBTs do not have the same current ratings, parallel IGBTs can be used (effectively increasing the active area of the IGBT die) to increase the current rating while keeping switching performance. Therefore,

there is no restriction in terms of the current rating for the IGBTs and a selected IGBT with specific forward voltage drop and switching characteristics can be used in virtually any current rating.

A nonlinear regression was used to fit a model to the non-dominated data. The following model showed a good accuracy, i.e., high R^2 value.

$$V_{CE,ON} = C_1 + \frac{C_2}{C_3 \cdot t_d^{\,C_4} + C_5} + \frac{C_6}{C_7 \cdot t_f^{\,C_8} + C_9} \qquad (4\text{-}12)$$

where delay time and fall time are both in nanoseconds. Using the surface fitting tool of MATLAB, the values for C_1-C_9 were found for the best fit and along with R^2 value for the fit are listed in Table 4-I. Figure 4-7 also shows the surface fitted to the data of Figure 4-6.

Table 4-I. Coefficients for (4-12)

Coefficient	Value
C_1	0.3633
C_2	0.87
C_3	1.311×10^{-9}
C_4	4.137
C_5	0.773
C_6	1.134
C_7	0.2153
C_8	0.7072
C_9	0.4302
R^2	**0.9334**
R^2 when all data considered	**0.3742**

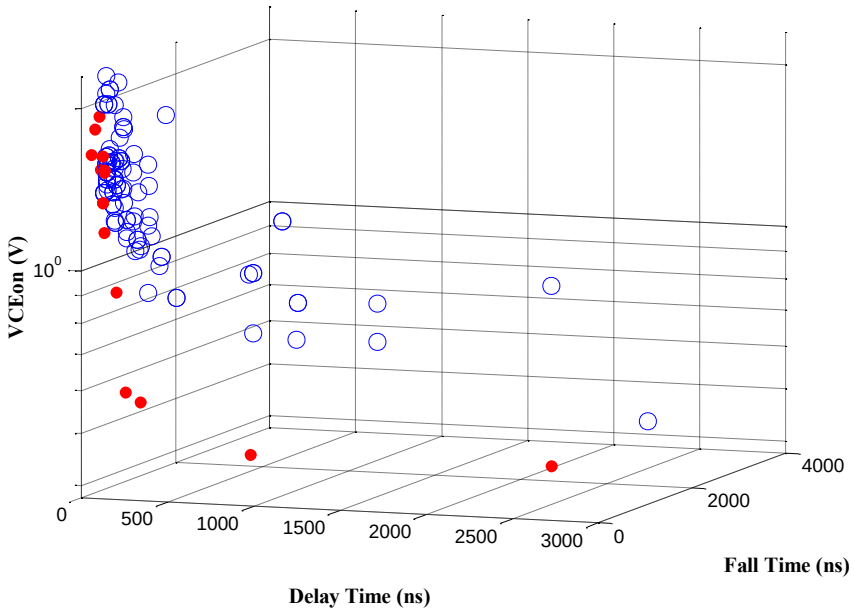


Figure 4-6. 3D plot of $V_{CE,ON}$ vs. delay time and fall time. Red points show the non-dominated data. The rest of the data are shown in blue circles.

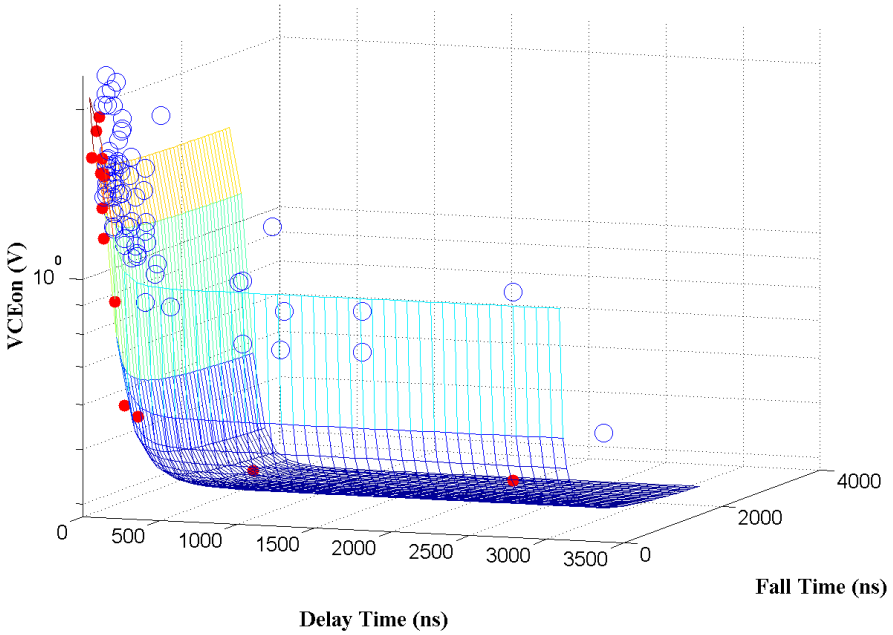


Figure 4-7. Surface fitted to the points in Figure 4-6.

4.1.3. Heat sinks

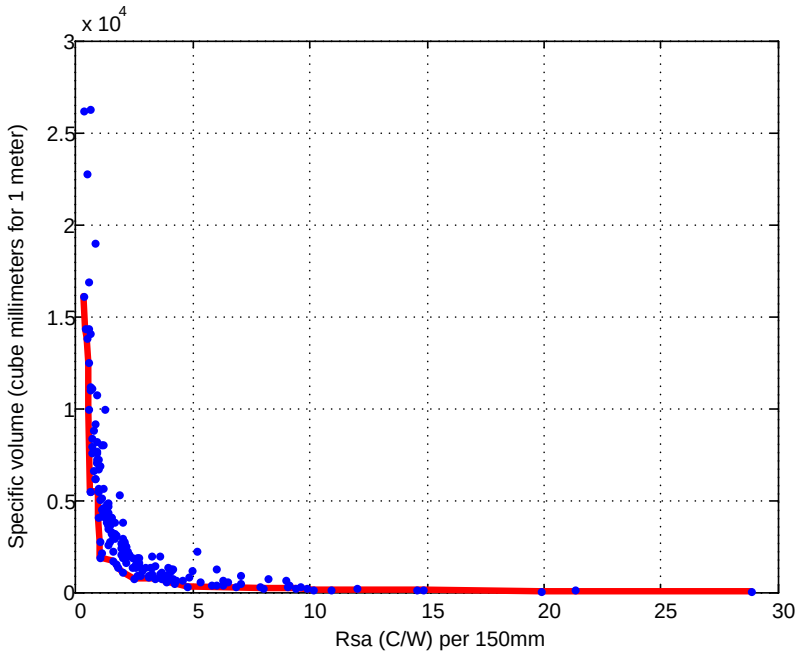
Heat sinks contribute significantly to the volume and therefore, power density of the power electronic converters. Modeling heat sinks in terms of their geometry is difficult and requires a vast knowledge on fluid mechanics and many free variables to consider. Therefore, in this paper a nonlinear regression is performed on 175 extruded heat sinks from Aavid Thermalloy [160] to find the specific volume of the heat sink from its surface-to-ambient thermal resistance. The process begins with specifying each heat sink as a point on a $R_{s\text{-}a}$-V space. Dominated designs are then eliminated from the set of components and then a nonlinear regression is performed to find the best function which fits the data points. The best fit was found using the function below:

$$Vol_{specific} = 2421 * R_{sa}^{-1.657} + 209.9 \qquad (4\text{-}13)$$

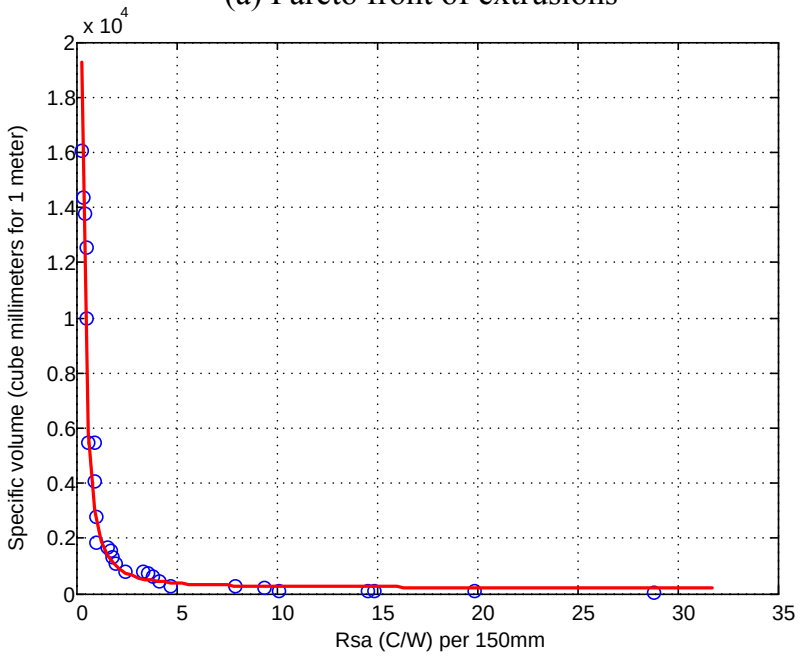
where R_{sa} is the thermal resistance for 150mm and $Vol_{specific}$ is in mm^3 for 1 meter of the extrusion. Figure 4-8 demonstrates each step of this process.

4.2. Example: Efficiency-volume optimization of an inverter

Power electronic converters, particularly those proposed for use in renewable energy systems, contain a wide variety of topologies each with different operating conditions on the basic components. This example begins by selecting a topology, which represents a common single-phase, renewable energy inverter. The output H-bridge, with a coupling LC filter and IGBT switches, is shown in Figure 4-9 and is used to develop the methodology and approach, which can later be applied to other topologies.



(a) Pareto front of extrusions



(b) Nonlinear regression

Figure 4-8. (a) Extrusions with Pareto front (b) nonlinear regression with only points on the Pareto front

Constraints are enforced by required performance specifications such as voltage and power and performance specifications such as THD. In this section, losses and volume of the converter have been chosen as objective functions.

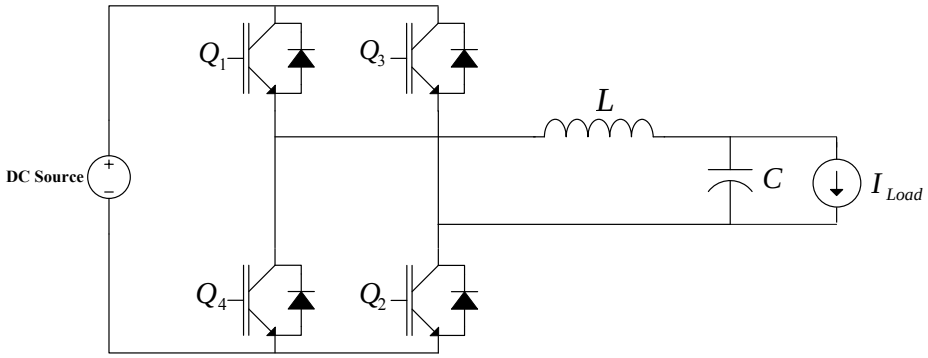


Figure 4-9. The power electronic converter considered for optimization

4.2.1. Sinusoidal PWM

Sinusoidal PWM is a well-known modulation scheme in the literature [161, 162]. In this modulation scheme, a sinusoidal waveform is used as carrier and a high frequency sawtooth or triangular wave as the modulator. Figure 4-10 shows typical waveforms for sinusoidal PWM with triangular modulation.

In order to calculate losses for each component, the current harmonic content should be known and therefore, knowledge of the voltage harmonic content of the PWM waveform is required. For the triangular modulation, which will be used throughout this dissertation, the harmonic content is as follows [161].

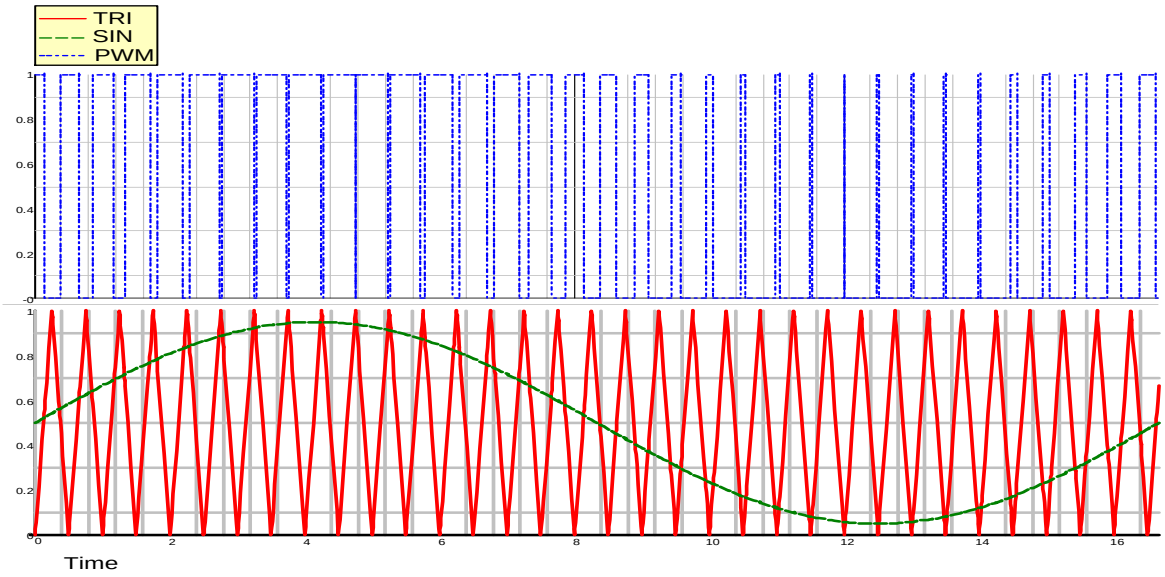


Figure 4-10. Waveforms for a sinusoidal PWM with triangular modulation

$$
\begin{aligned}
V_{PWM} &= M \cdot V_{dc} \cdot \cos(\omega_0 t + \theta_0) \\
&+ \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} \cdot J_0(m \cdot \frac{\pi}{2} \cdot M) \cdot \sin(m\frac{\pi}{2}) \cdot \cos(m[\omega_c t + \theta c]) \\
&+ \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n \neq m)}}^{\infty} \frac{1}{m} \cdot J_n(m \cdot \frac{\pi}{2} \cdot M) \cdot \sin([m+n]\frac{\pi}{2}) \\
&\cdot \cos(m[\omega_c t + \theta_c] + n[\omega_0 t + \theta_0])
\end{aligned}
\qquad (4\text{-}14)
$$

where M is called *modulation index* and is defined as the ratio of the carrier amplitude to the modulator amplitude; V_{dc} is the applied DC voltage; ω_0 and θ_0 are the carrier angular frequency and phase; ω_c and θ_c are the modulator angular frequency and phase and J_0 and J_n are zero-order and nth order Bessel functions of the first kind respectively. The first term of (4-14) is the fundamental component while the second and third terms are

switching frequency harmonics and sidebands respectively. Figure 4-11 Shows the harmonic content of sinusoidal-triangular PWM.

4.2.2. Modeling passive components

4.2.2.1. Capacitors

In Figure 4-9, the capacitor is in the output filter of the inverter and filters the AC current in the presence of AC voltage. In this application, polymer film capacitor technology is a good choice because of high volumetric efficiency and being able to serve in AC applications. Other capacitor technologies may be used for other applications, such as aluminum electrolytic capacitors which are popular choice for the internal dc bus in a multi-stage converter.

Equivalent Series Resistance of a capacitor contains two general terms: an ohmic

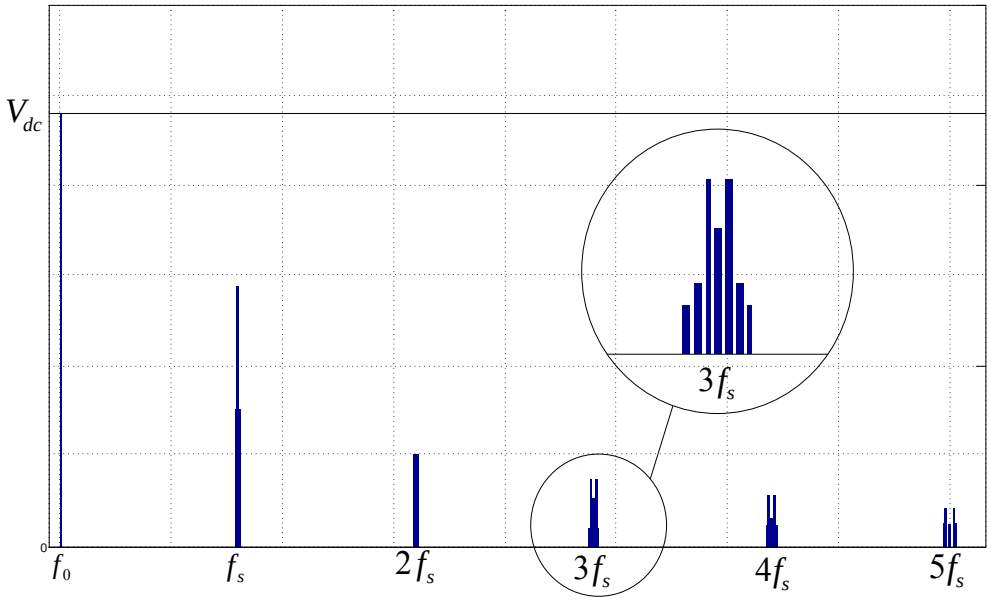


Figure 4-11. Harmonic content of sinusoidal-triangular PWM

term due to resistance of the metalized layer and metallic contacts and dielectric losses represented by *tan δ* divided by a factor of frequency as shown in (3-12) [25].

$$ESR = R_{\Omega} + \frac{\tan\delta}{C.\omega} \qquad (3\text{-}15)$$

Due to small thickness of metalized layer, high frequency effects such as skin effect are negligible [147]. Dielectric losses dominate in low frequencies while ohmic losses dominate in higher frequencies [163]. Since the converter of our interest is a PWM converter, it only carries waveforms of desired output frequency as well as PWM frequency spectrum which means that it does not carry almost any current in the frequency range between the desired output frequency and switching frequency. Therefore, superposition can be applied considering the fact that only one of the loss mechanisms dominate in frequencies of the spectrum. If resistive and dielectric losses are comparable in one of two frequency regions of interest, superposition can be applied as a first approximation [164]. The loss angle, *tan δ,* typically is around 0.02% for polypropylene. Resistance of a winding film based on the geometry is calculated from the equation below [147, 165]:

$$R_{\Omega} = \frac{2\rho w}{3l} \qquad (3\text{-}16)$$

where ρ is sheet resistivity in Ω/sq, w is the active winding width and l is the winding length. Using the equation above and applying superposition, losses for a metalized film capacitor can be calculated:

$$P_{Loss} = \sum_{n=1}^{\infty} ESR_n \cdot I_n^{\,2} \qquad (3\text{-}17)$$

where I_n is the current and ESR_n is the ESR for the n^{th} harmonic.

4.2.2.2. Inductors

In this section Natural Steinmetz equation ((2-4)) and Dowell equation ((2-6) and (2-7)) were used to calculate core losses and conductor copper losses respectively. Core loss calculation is done knowing the current flowing through the inductor and thus, the magnetic field in the core. Copper losses are calculated by using AC resistance for each frequency in the frequency spectrum.

4.2.2.3. IGBTs

Using the parameters described above, conduction and switching losses are calculated using the approach described in [166-168]. In order to simplify the calculations, diode properties are considered fixed. According to these references, conduction losses due to IGBT and Diode are as follows:

$$P_{IGBT} = (\frac{1}{8} + \frac{M\cos\theta}{3\pi})R_{CE}{I_{C,M}}^2 + (\frac{1}{2\pi} + \frac{M\cos\theta}{8})V_{CE,ON}I_{C,M} \quad (4\text{-}18)$$

where M is the modulation index; θ is the angle between fundamental component of voltage and current; $I_{C,M}$ is the maximum current; $V_{CE,ON}$ is the fixed part and R_{CE} is the resistive part of forward voltage drop. Considering a fixed forward voltage drop for the diode to remain consistent with what was assumed for the IGBT, the following equation is derived.

$$P_d = (\frac{1}{2\pi} - \frac{M\cos\theta}{8})V_d I_{C,M} \quad (4\text{-}19)$$

Switching losses can be calculated as follows:

$$P_{ON} = \frac{1}{8} V_{CC} t_r \frac{{I_{C,M}}^2}{I_{C,N}} F_S \qquad (4\text{-}20)$$

where P_{ON} is the turn on switching losses; t_r is the rise time of the IGBT and F_s is the switching frequency. It is assumed that the turn on properties of the IGBT is determined by the anti-parallel diode and a constant value (200 A/μs) for this rate of rise was taken into account. $I_{C,N}$ is the maximum current of the selected IGBT, which in this case, is equal to $I_{C,M}$ since the problem is an optimization problem. In other words, the maximum current in the IGBT is chosen to handle the maximum required current.

$$P_{OFF} = V_{CC} I_{C,M} t_f F_S \left(\frac{1}{3\pi} + \frac{1}{24} \frac{I_{C,M}}{I_{C,N}}\right) \qquad (4\text{-}21)$$

where P_{OFF} is the turn off switching losses and t_f is the summation of turn-off delay time and fall time.

Recovery losses (losses due to diode reverse recovery and excessive losses of the IGBT due to that phenomenon) are calculated as follows:

$$P_{rr} = F_S V_{dC} (0.184 I_{rr} t_{rr,N} + 0.288 I_{C,M} t_{rr,N}) \qquad (4\text{-}22)$$

where $t_{rr,N}$ is the reverse recovery time of the selected diode, I_{rr} is the peak recovery current and V_{dc} is DC bus voltage.

4.2.3. Weight and volume modeling

Due to the small size of semiconductors they contribute very little to the weight and volume of the system. Therefore, the main contribution comes from the capacitor, the inductor in the filter and the heat sink.

4.2.3.1. Inductor

To calculate the weight and volume of the inductor, the EE core geometry was chosen, since it is a popular topology in design of the magnetic components. Figure 4-12 shows different dimensions of the EE core. For magnetic core material, 70 different materials (Ferrite and Iron powder) from Ferroxcube [169], Magnetics inc.[170] and Micrometals [171] have been chosen as the material set.

Out of 6 dimensions shown in Figure 4-12, B, C and D were chosen as optimization variables and the rest can be calculated from the maximum flux density of the core. It is assumed that the core is designed in a way that for the maximum current it

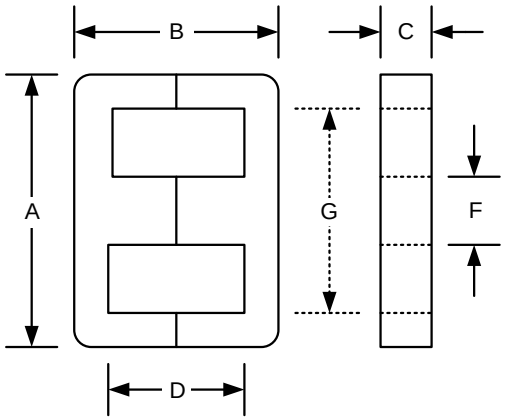


Figure 4-12. EE core dimensions.

operates in saturation flux density. Therefore, the required flux path length can be calculated as follows.

$$l_{flux} = (\frac{N \cdot I_{peak} \cdot \mu_0}{B_{sat}} - \frac{g}{\mu_0}) \cdot \mu_r \quad (4\text{-}23)$$

where N is the number of turns, I_{peak} is the peak current in the inductor, B_{sat} is the saturation flux density of the core, g is the length of eth air gap, μ_0 is the permeability of the air, and μ_r is the relative permeability of the core material. Since cross section of each leg of the EE core is constant throughout the leg, other dimensions in the EE core can then be calculated as follows.

$$A = l_{flux} - \frac{B}{2} + \frac{3C}{2} \quad (4\text{-}24)$$

$$F = B - D \quad (4\text{-}25)$$

$$G = A - F \quad (4\text{-}26)$$

Copper weight can also be calculated from wire gauge and number of turns, both of which are considered as design variables.

4.2.3.2. Capacitor

To calculate the weight and volume of the capacitor, capacitance, film thickness and film width are considered as design variables. The length of the capacitor film can be calculated from these variables. Capacitor film is typically wound on a former core whose diameter has a direct effect on the volume of the capacitor.

Calculations show that there is an optimal core diameter for each pair of film length and film thickness. Figure 4-13 shows variations in the total diameter of a capacitor

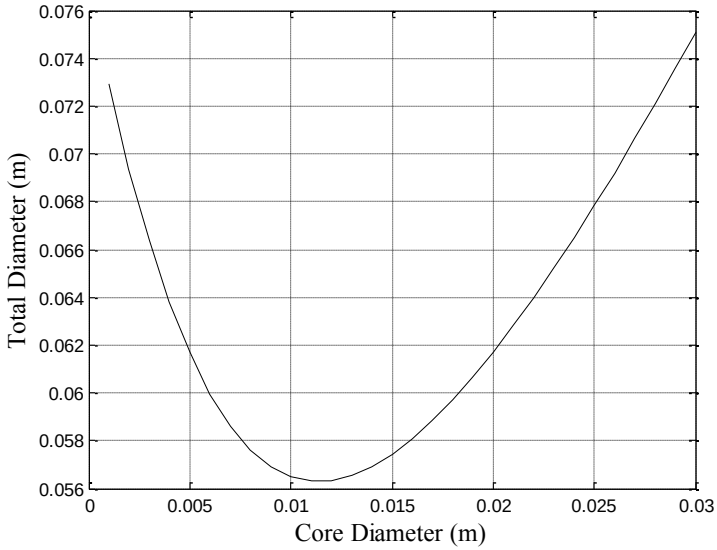


Figure 4-13. Total diameter versus core diameter for a capacitor winding

when core diameter changes. The film thickness and film length are 3μm and 246m respectively. This optimum radius can be calculated as follows:

$$R_{i,optimal} = 0.1385\sqrt{0.1728dl - 5.2832d^2} \qquad (4\text{-}27)$$

where d is the film thickness and l is the film length.

A survey on the weight of the capacitor modules produced by Cornell Dubilier [85] determined the specific mass of the capacitor to change between 1100 to 1300 kg/m^3. This is consistent with the fact that the specific mass of polypropylene is 946 kg/m^3 [172]. Therefore, a value of 1200 kg/m^3 was chosen for specific mass of the capacitor.

4.2.3.3. Heat sink

For the heat sink, volume is calculated using the thermal resistance for 150mm, (4-13) and required length for the extrusion to dissipate the heat resulted from losses in semiconductor switches.

4.2.4. Optimization and results

Two objective functions (converter losses and volume) considered for this optimization are as follows:

$$P_{Loss} = P_{ind} + P_{Cap} + P_{IGBT} + P_{diode} \quad (4\text{-}28)$$

$$Volume = V_{ind} + V_{Cap} + V_{Heat\,\mathrm{Sink}} \quad (4\text{-}29)$$

Table 4-II summarizes the optimization variables and their upper and lower bounds. Limits on individual harmonic levels and total harmonic distortion (THD) recommended by IEEE 519 [123] standard for individual harmonics and THD of the output current were enforced as constraints.

Table 4-II. Design variables

#	Variable	Description	Min	Max	Unit
1	a_w	Wire gauge	0.0062	26.92	mm^2
2	N	Number of turns	1	50	-
3	Cap	Capacitance	1nF	10mF	F
4	W_c	Film width	10	620	mm
5	d_c	Film thickness	3	10	µm
6	f_s	Switching Frequency	1	100	kHz
7	B	Core dimension	10	100	mm
8	C	Core dimension	10	100	mm
9	D	Core dimension	10	100	mm
10	G	Core air gap	0	1	mm
11	CI	Core material index	1	70	-
12	t_d	IGBT turn-off delay time	1	1000	ns
13	t_f	IGBT fall time	1	1000	Ns
14	R_{sa}	Heat sink thermal resistance for 150mm	0.32	28.83	W/°C

The specifications of the single phase inverter considered for this optimization are reported in Table 4-III. The resistance of the load is selected in a way that the output power of the inverter is 1kW. Such an inverter can be used as the DC-AC stage of a 1kW commercial solar inverter, such as the METEC 1kW inverter [173]. For simplicity and reducing the order of the problem, the specifications of the IGBT anti-parallel diode were fixed.

Random sampling [174] was performed for 723,500 number of iterations to obtain a Pareto front for the optimization which is shown in Figure 4-14. The figure reveals that it is possible to achieve very low losses or small volume One of the design points on the Pareto front (point A) has been fully described in Table 4-IV. The index 56 for the core material refers to Micrometals –M125 material [175].

Table 4-III. Specifications of the single phase inverter

Variable	Description	Value	Unit
V_{DC}	DC input voltage	$120\sqrt{2}$	V
R_{load}	Load Resistance	14.4	Ω
f_0	Fundamental Frequency	60	Hz
V_d	Diode voltage drop	1.2	V
$t_{rr,N}$	Diode reverse recovery time	50	ns
I_{rr}	Reverse recovery current	8	A
M	Modulation index	1	-
Θ	Phase shift	0	Degrees

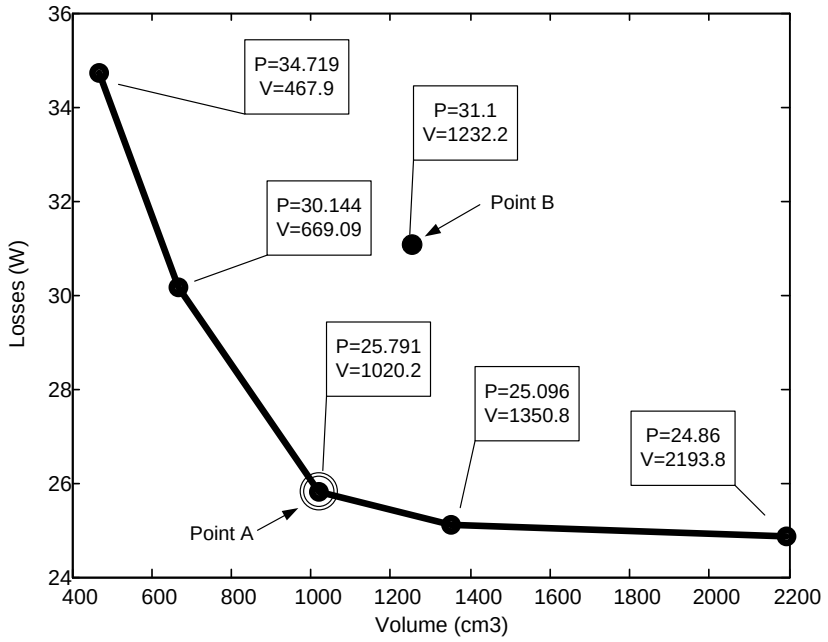


Figure 4-14. Pareto front showing the tradeoff between losses and volume (details of the point A is shown in Table 4-IV

The design reported in Table 4-IV may translate into a design which can be implemented by selecting commercial off-the-shelf components which have similar specifications. These commercial off-the-shelf components are reported in Table 4-V. Using the off-the-shelf components, the design is translated into point B in Figure 4-14. As can be seen in Figure 4-14, design B is dominated by points on the Pareto front, meaning it is feasible but not optimal. Therefore, the method presented in this work found that the converter design can be optimized beyond what is possible from using only off-the-shelf components. Output of this optimization provides specification sheet for component vendor.

Table 4-IV. Detail of point A on the Pareto front

Variable	Description	Value	Unit
d_w	Wire gauge	1.44	mm^2
N	Number of turns	15.14	-
Cap	Capacitance	60.44	μF
W_c	Film width	0.037	mm
d_c	Film thickness	6.08	μm
Vol_{cap}	Capacitance Volume	308	cm^3
f_s	Switching Frequency	7.8985	kHz
B	Core dimension	64.22	mm
C	Core dimension	42.39	mm
D	Core dimension	56.02	mm
G	Core air gap	9.73×10^{-4}	mm
CI	Core material index	58	-
Vol_{core}	Core volume	177.77	cm^3
t_d	IGBT turn-off delay time	844	ns
t_f	IGBT fall time	737	ns
$V_{CE,0}$	Forward voltage drop – fixed part	1.4096	V
R_{CH}	Channel Resistance	0.0513	Ω
R_{sa}	Thermal Resistance	22.88	W/ºC
$Vol_{spec,hs}$	Heat sink specific volume	223.43	1000 mm^3 for 1m length
V	Volume	1020.23	cm^3
P_{loss}	Losses	25.791	Watts

4.3. Conclusion

This section demonstrated the capabilities of characterization and abstraction methods in order to find a loss model for IGBTs and heat sinks without getting into a large degree of complexity. It also showed capabilities of multi-objective optimization using a descriptive language for the components to find a set of equally-good truly-

optimal solutions. In next section, a Module-Integrated inverter (MII) [176] is optimized for the efficiency, reliability and volume using this approach.

Table 4-V. Commercial off-the-shelf components that can be used to implement the design of Table 4-IV

IGBT		
Part number	IRG4BC10S	N/A
Turn-off delay time	630	ns
Fall time	710	ns
Forward voltage drop – fixed part	1.18	V
Channel Resistance	0.0617	Ω
Magnetic core		
Part number	Ferroxcube E 65/32/27	N/A
B	65.6	mm
C	27.4	mm
D	44.4	mm
Core volume	116.47	cm^3
Capacitor		
Part number	Cornell Dubilier 24FD3760-F	N/A
Capacitance	60	µF
Volume	253.68	cm^3
Heat sink		
Part number	Aavid Thermalloy 78260	N/A
Specific Thermal resistance (for 150mm)	21.31	W/ºC
Specific volume	120.75	1000 mm^3 for 1m length

5. PERFORMANCE LIMITS OF A RIPPLE PORT MODULE INTEGRATED INVERTER

In the past decade, use of photovoltaic (PV) energy has increased dramatically. Indeed, in the United States alone, PV installations have increased from 79 MW in 2005 to 878 MW in 2010, almost doubling every year since 2007, a trend expected to persist because of the global energy crisis and the climate change impact of fossil fuels [177]. Government programs such as the U.S. Department of Energy SunShot initiatives[178], aim to reduce the cost of PV by 75% by 2020 as well as increasing the installed capacity. To fulfill these ambitious goals, a holistic system view is required, which includes design and optimization of power conditioning.

Among the different designs for PV system power conditioning, Module Integrated Inverters (MII) are quickly becoming the main trend due to their improved energy harvest, lower installation costs, improved system efficiency, Plug-N-Power operation, and enhanced flexibility and modularity [179-181]. A module-integrated inverter is a PV inverter connected to a PV module. Unlike the centralized PV system, in which a PV inverter is connected to a large number of PV modules connected in series and parallel, or the multi-string PV system, in which strings of PV modules connected in series are connected to DC/DC converters and then the output of DC/DC converters is connected to a DC/AC inverter, module-integrated inverters enable better energy capture and benefit from lower installation costs and improved safety due to the omission of high-voltage DC cables. There are a few commercial MIIs available in the market, such as the

Enphase MII [19] or Solabridge Pantheon MII [101]. While efficiency and power density of a MII is of a great importance in its design, a major challenge is to improve the reliability of these converters, largely dominated by the lifetime of the decoupling capacitor [31, 182], also a challenge for the industry [183, 184] Decoupling capacitors, usually of the electrolytic type [180], are used to eliminate the double frequency ripple in single-phase AC power in order to prevent the pulsating current transfer to the PV module side and reduce energy harvest. Although criterion for minimum energy storage is now established [31, 182], the design tradeoffs to minimize the value of capacitance, which makes it possible to use more reliable film capacitors, has not been fully explored. In [31, 182], a ripple cancellation technique based on a ripple port is introduced. This double frequency cancellation technique is applied on the inverter side of a two-stage MII so that design and control of the DC-DC converter is independent of the DC-AC stage. In this section, a multi-objective design optimization is performed on the Ripple Port Module Integrated Inverter (RP-MII) with three different input stage DC-DC converters.

5.1. Photovoltaic energy conversion

Photovoltaic cells generate electrical energy on their terminals which depend on many factors such as solar irradiance and temperature. Models with various levels of detail are present in the literature. In one of the basic forms, a PV cell can be modeled by a current source anti-paralleled with a P-N diode (Figure 5-1). In this model, the terminal current of the PV cell can be calculated from:

$$I = I_{sc} - I_0(e^{\frac{qV_d}{nkT}} - 1) \tag{5-1}$$

where n is the number of cells in series, k is the Boltzmann constant ($=1.38065\times10^{-23}\ m^2kgs^{-2}$); q is the electron charge ($=1.60217\times10^{-19}\ couloumbs$); V_d is the diode voltage, T is the cell temperature; I_0 is called reverse saturation current and in some of the more advanced models [185, 186] it is also temperature dependent:

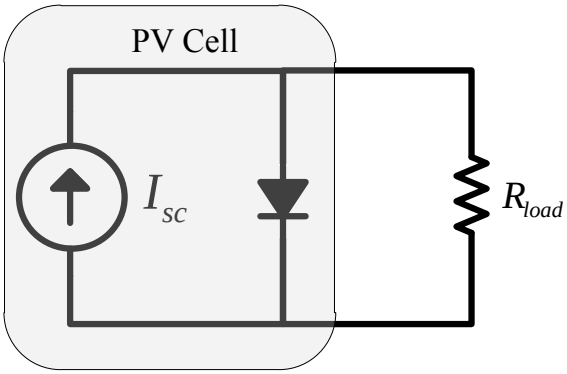


Figure 5-1. Basic model of a PV cell connected to the load

$$I_0 = I_{0,ref} \cdot (\frac{T}{T_{ref}})^3 \cdot e^{\frac{q \cdot V_g}{k}(\frac{1}{T} - \frac{1}{T_{ref}})} \quad (5\text{-}2)$$

where $I_{0,ref}$ is the saturation current in temperature T_{ref}, T is the temperature and V_g (=1.12V) is the silicon band gap voltage. I_{sc} is the short circuit current of the PV cell and a factor of solar irradiance and temperature [185, 186]:

$$I_{sc} = I_{sc,STC} \cdot \frac{G}{G_{STC}} + K_0(T - T_{ref}) \quad (5\text{-}3)$$

where $I_{sc,STC}$ is the short circuit current and G_{STC} is the solar irradiance both in standard test conditions. K_0 is the temperature coefficient and calculated as follows.

$$K_0 = \frac{I_{sc,T_{ref},1} - I_{sc,T_{ref},2}}{T_{ref,1} - T_{ref,2}} \quad (5\text{-}4)$$

where $I_{sc,T_{ref},1}$ and $I_{sc,T_{ref},2}$ are short circuit currents in temperatures $T_{ref,1}$ and $T_{ref,2}$. From equations (5-1) to (5-4), it is clear that the DC output characteristics of a PV cell depend significantly on its load and operating conditions. Therefore, in order to have a sinusoidal voltage with fixed amplitude from photovoltaic energy conversion, a power conditioning

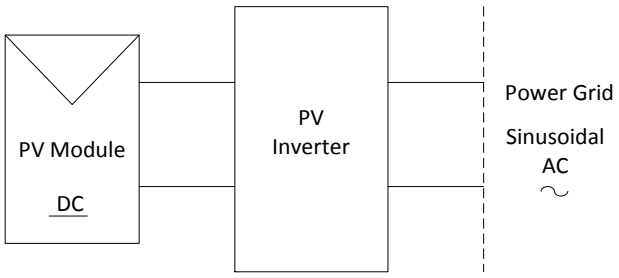


Figure 5-2. Photovoltaic inverter as the power conditioning unit

unit is required between the PV cell and the load or power grid. This power conditioning unit is a photovoltaic inverter. The diagram of a PV cell connected to the grid via a PV inverter is illustrated in Figure 5-2.

Dependency of voltage and current of the PV cells to each other also suggest that there should be a voltage and current combination, in which product of voltage and current or power generated by PV cell is maximized, known as Maximum Power Point

(MPP). MPP varies based on operating conditions (solar irradiance and temperature) [187]. The inverter must be able to adjust the voltage and current of the PV cells to extract maximum power from the PV cells; a process known as Maximum Power Point Tracking (MPPT) [187]. The slope of the power curve (Figure 5-3-b) in the maximum power point is zero, stated mathematically as follows.

$$\frac{dP}{dV} = 0 \tag{5-5}$$

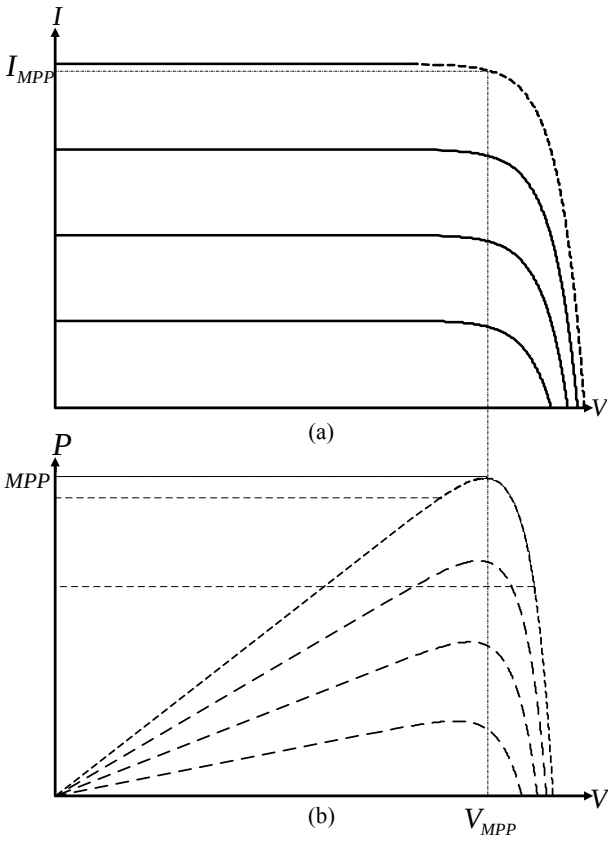


Figure 5-3. Maximum power point of a PV cell. Different traces are for different solar irradiance and PV module temperature

5.2. Photovoltaic inverters

Photovoltaic inverters come in a variety of designs based mainly on the architecture of the whole PV system [180]. In the past, a large number of PV modules, connected in series and parallel, were connected to a centralized high-power inverter. [180]. This architecture had many problems such as high-voltage DC cables between modules and inverter, loss of energy because of centralized MPPT and non-flexible design which restricted mass production opportunities. Presently, this architecture has been almost completely replaced by two relatively new technologies

A string of PV modules connected in series can be connected to an inverter. This technology, called the *String technology* [180], is a reduced version of centralized architecture, which still has the drawback of power loss due to centralized MPPT, though to a lower degree. However, when connected to the grid, input voltage of the inverter might be enough to avoid voltage amplification. Voltage amplification is otherwise required due to the grid voltage being higher than the voltage of a typical PV module. Multiple strings can also be used as what is called the *multi-string technology*, each with a converter capable of MPPT of their own but sharing a DC/AC inverter.

Another approach used is known as AC PV technology [180] or Module-Integrated Inverter [181]. In this technology, a PV module is coupled with an attached low-power inverter. Since there is only one module attached to the inverter, maximum power point of each module will be tracked separately and therefore will circumvent a mismatch due to centralization, which is the main advantage of this technology. AC PV technology also enables the plug-and-play capability of PV modules and inverters,

enabling easier utilization of solar energy. Figure 5-4 [180] reveals historical overview of PV inverters. Figure 5-5 Show a comparison between AC PV and centralized technologies.

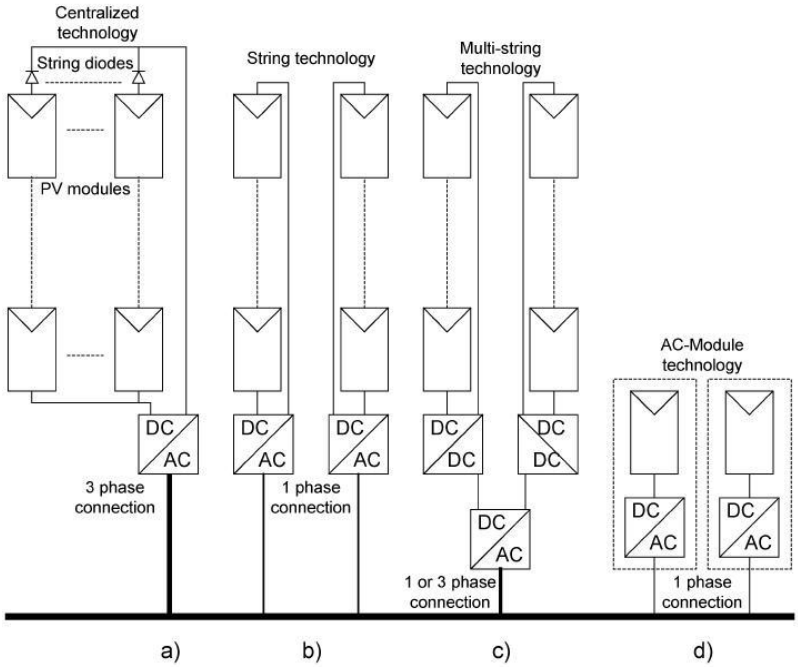


Figure 5-4. Historical overview of PV systems; (a) centralized structure (b) string technology (c) multi-string technology and (d) AC module technology [180]

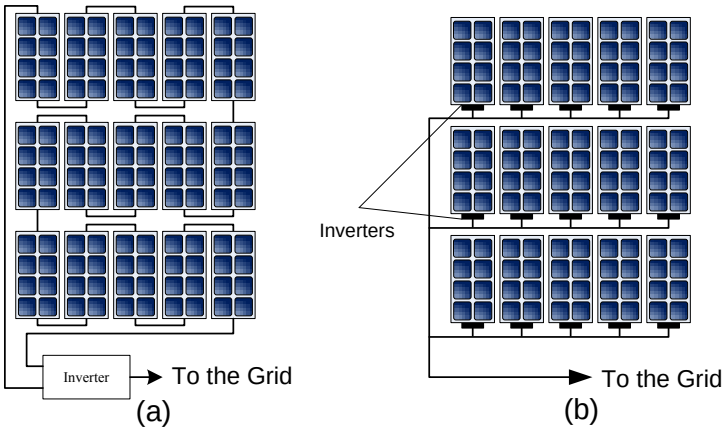


Figure 5-5. A comparison between (a) centralized and (b) AC PV and technologies

5.3. Module-Integrated Inverter (MII)

Many different topologies have been suggested for MIIs [181]. A PV inverter must have three specific characteristics: it should provide galvanic isolation, be able to perform MPPT, and it must embody a solution for power decoupling. Galvanic isolation is required to simplify grounding, safety and operation of PV modules; MPPT is required to ensure that the most possible energy is extracted from the modules, and decoupling is required to ensure the ripple in the PV module terminals is within the specifications.

Galvanic isolation is usually accomplished by means of a transformer, either high-frequency or line frequency [180]. Using a line-frequency transformer will enable the designer to administer the MPPT and conversion to AC in a single stage, and then use the transformer to amplify the output voltage to the required level. However, line-frequency transformers are bulky [187] and will affect the converter's power density. A high-frequency transformer will be deployed in between two conversion stages and is smaller in size. Figure 5-6 illustrates these two structures [181].

From the perspective of the DC link, there are three distinct types of MIIs in the literature: MII with a DC link, MII with a pseudo-DC link, and MII without a DC link [181]. In MII with a DC link, a front-end DC-DC converter usually performs the MPPT job and also provides isolation. The AC-DC inverter then converts the voltage to sinusoidal AC. The isolation condition requires that the DC-DC converter is of the isolated type, i.e., full-bridge, half bridge, push-pull, flyback, forward, etc. [188]. A bulk capacitor is usually connected in the DC bus to provide decoupling. A pseudo-DC link converter consists of a DC-DC converter which, instead of a constant DC, provides

rectified sinusoidal voltage at its output. This DC-DC converter also provides isolation. The second stage converts this rectified sinusoidal voltage to sinusoidal voltage by an unfolding circuit. An MII without a DC link converts DC to high-frequency AC, which is the input to the primary winding of the isolation transformer. The secondary winding is connected to an AC-link inverter, which directly converts the high frequency voltage to

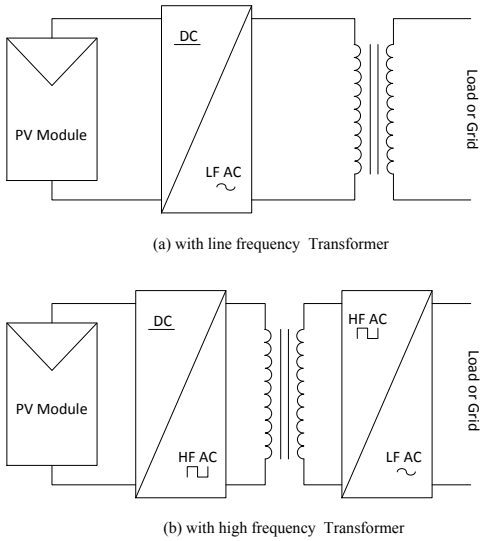


Figure 5-6. Using transformer for galvanic isolation with (a) low frequency and (b) high frequency transformer [181]

sinusoidal voltage. Figure 5-7 shows three different types of module-integrated inverter.

5.4. Power decoupling

Assuming that the voltage and current on the load or grid end of the inverter is purely sinusoidal, the voltage and current are of the form below:

$$V = V_m \cos(\omega t)$$
$$I = I_m \cos(\omega t + \varphi) \quad (5\text{-}6)$$

where V_m and I_m are the voltage and current amplitudes respectively and φ is the phase difference. The instantaneous power then will be of the following form:

$$P = V_m I_m \cos(\omega t)\cos(\omega t + \varphi) = \frac{V_m I_m \cos(\varphi)}{2} + \frac{V_m I_m}{2}\cos(2\omega t + \varphi) \\ = P_o + P_o \cos(2\omega t + \varphi) \tag{5-7}$$

As is witnessed from (5-7), instantaneous power has a constant term and a double frequency term with the same amplitude as the constant term. However, the power from PV module, assuming that it is operating at its maximum power, is given by:

$$P_{PV} = V_{MPP} \cdot I_{MPP} \tag{5-8}$$

and only has a constant term. If this difference in instantaneous power between the PV module and the grid is not addressed, the PV current will no longer be a constant DC

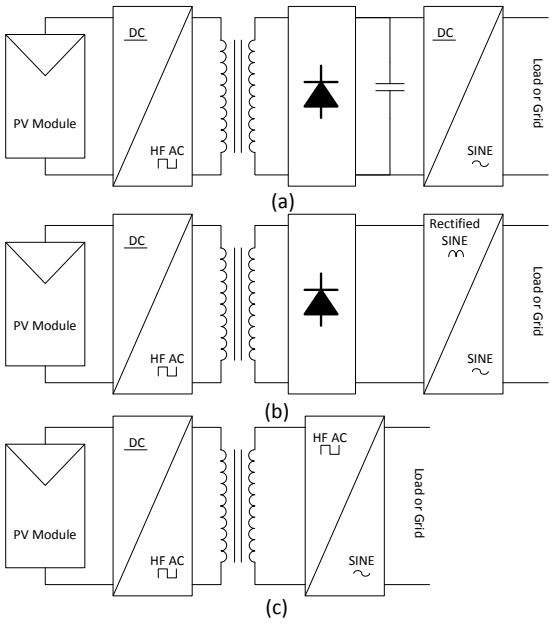


Figure 5-7. Three different types of PV inverters (a) with DC link (b) with pseudo-DC link and (c) without DC link [181]

value and therefore, PV will not operate in its maximum power point. This deviation from maximum power point is illustrated in Figure 5-8.

This power mismatch issue is usually resolved by means of a decoupling capacitor, which should be large enough to hold voltage ripple below a certain level. The size of this decoupling capacitor is given by [180]:

$$C = \frac{P_{PV}}{2 \cdot \omega \cdot V_{dc} \cdot \Delta V_{dc}} \tag{5-9}$$

where ω is the output frequency, V_{dc} is the DC bus voltage and ΔV_{dc} is the desired ripple.

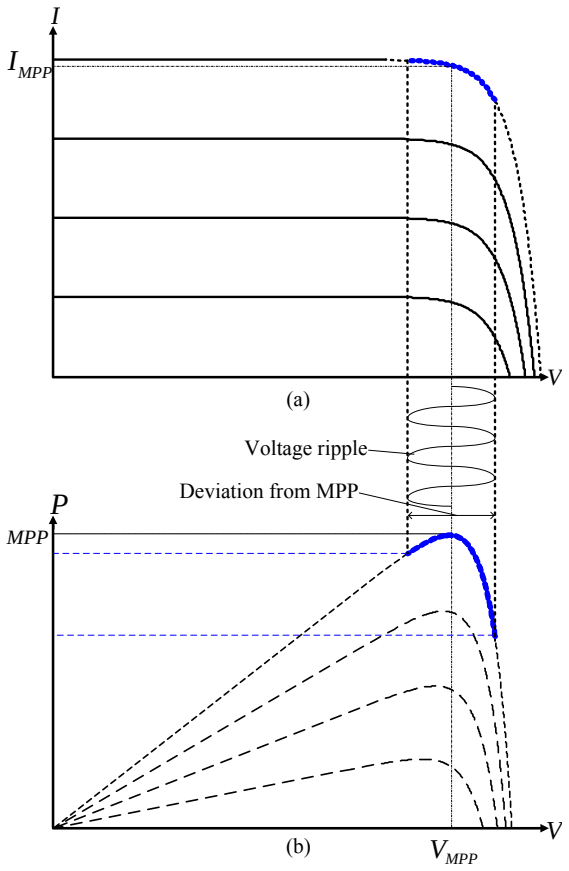


Figure 5-8. Deviation from maximum power point due to the current ripple in PV module.

For instance, for a 30V, 50W system, if the desired ripple is 5%, the required capacitor is 1,473μF. If the ripple is expressed as $\Delta V_{dc} = 2r \cdot V_{dc}$, the capacitor average stored energy can be computed as

$$W_c = \frac{1}{2r}\frac{P_o}{4\pi f} \tag{5-10}$$

where f is the line frequency. Since f is fixed, the stored energy is proportional to the output power. However, due to the double frequency ripple in the power, the minimum energy storage requirement can be calculated as follows.

$$W_S = \frac{P_o}{4\pi f} \tag{5-11}$$

The ratio of the actual capacitor energy (5-10) to the minimum need is $1/(2r)$. For example, for a 5% ripple, the capacitor stores 10 times as much energy as the minimum. A decrease in energy storage requirements may only be accomplished by allowing more voltage ripple, not desirable in PV applications.

Large capacitance in the system usually necessitates deployment of electrolytic capacitors. However, use of electrolytic capacitors creates a new challenge, since electrolytic capacitors are known to experience higher failure rates relative to other capacitor technologies [189-191]. Therefore, reliability of the entire system is dictated by electrolytic capacitors [31, 176, 182]. Thus, reliability of the system can be improved if the electrolytic capacitor is removed or replaced by a capacitor from a different technology (i.e., a film capacitor). Since electrolytic capacitors are known as major limitation for system lifetime, many attempts have been made to eliminate this double

frequency power; thus eliminating the necessity of the electrolytic capacitor [192-199]. In the following subsection, a new method for eliminating double frequency will be presented.

5.5. Double frequency cancellation using a ripple port

This work considers an active filter approach to eliminate the double frequency pulsating current from the DC source. The basic configuration of this method is illustrated in Figure 5-9. Control of the modulation index and phase of the ripple port converter enables adjustment of the instantaneous power in the ripple port such that it catalyzes a complete cancellation of the output power's double frequency component. It means that the power and therefore, current that the inverter and ripple port draw from the DC link does not embody any double frequency component and is purely DC. Therefore, a large decoupling capacitor is no longer a necessity and a smaller capacitor (C_{dc} in Figure 5-9) can be used to filter high-frequency contents of the current, not necessarily an aluminum electrolytic capacitor.

Assuming a pure sinusoidal voltage across the ripple port capacitor (C_{rp}), the capacitor voltage is given by:

$$v_c(t) = V_c \cos(\omega t + \theta) \tag{5-12}$$

where θ is modulation phase. The power across the capacitor can be calculated from:

$$\begin{aligned} P_c(t) &= V_c \cos(\omega t + \theta) \cdot C \frac{d}{dt}\left[V_c \cos(\omega t + \theta)\right] \\ &= -\omega C V_c^{\,2} \cos(\omega t + \theta)\sin(\omega t + \theta) \\ &= \frac{-\omega C V_c^{\,2}}{2}\sin(2\omega t + 2\theta) \end{aligned} \tag{5-13}$$

In order for this power to cancel out the double frequency component of the output inverter, the following is necessary:

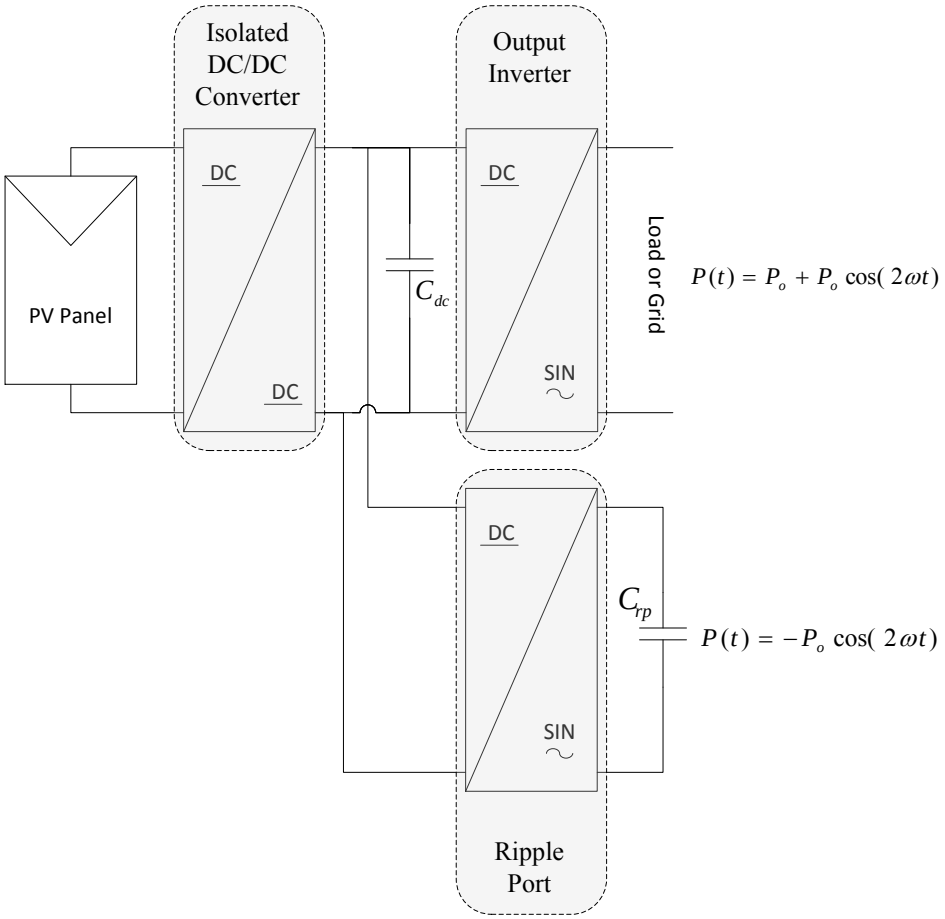


Figure 5-9. The basic configuration of double frequency cancellation using a ripple port

$$\frac{-\omega C V_c^{\,2}}{2}\sin(2\omega t + 2\theta) = P_o \cos(2\omega t + \varphi) \tag{5-14}$$

Using trigonometric identities, the following equations are derived [31].

$$C = \frac{2P_o}{\omega V_c^{\,2}} \tag{5-15}$$

$$\theta = -\frac{\pi}{4} + \frac{\varphi}{2} \qquad (5\text{-}16)$$

It is inferred from (5-15) that if peak capacitor voltage V_c is set to be large enough by design, the ripple port capacitor can be made arbitrarily small. Since the capacitor does not consume any active power, the ripple port does not consume any active power other than what is lost in the ripple port switches and the ESR of the capacitor.

5.5.1. Implementation

The ripple port active filter concept can be implemented by two H-bridges, each with 4 MOSFET switches and a sinusoidal-triangular PWM scheme. Though the capacitor is enough for double frequency power cancellation, switching voltage across the capacitor will create unacceptable high-frequency current spikes, possibly enabling large high-frequency current in the input current. These large spikes are likely to damage the power electronic switches. In order to resolve this issue, a small inductor is added in series with the capacitor to filter out some of high-frequency content. Figure 5-10 illustrates a basic diagram for double frequency cancellation with two MOSFET H-bridges. Figure 5-11 shows the simulation results for a 48V 110W system.

5.6. Exploring performance limits on a MII with ripple port concept

To demonstrate the capabilities of the approach proposed in this dissertation, a MII with the ripple port active filter concept was chosen as the design objective. Considering the three types of PV inverters mentioned in 5.2. and 5.3. , an inverter with a DC link is suitable to accommodate the inverter-ripple port concept. Adding the ripple port to the circuit in Figure 5-7 (a), large electrolytic capacitor at the DC link can be replaced by a

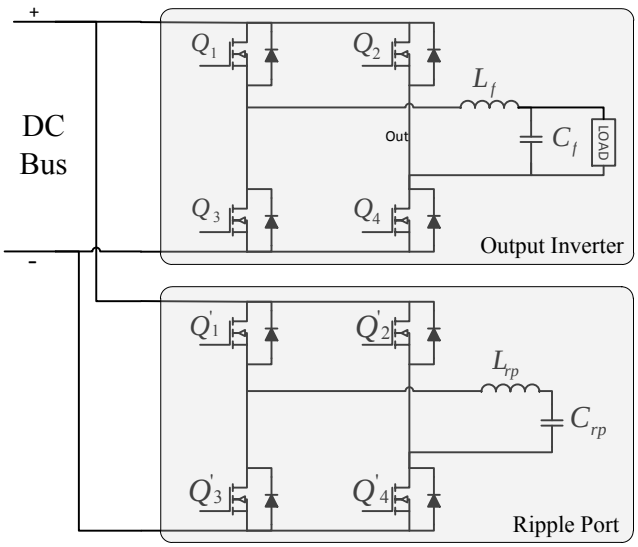


Figure 5-10. Inverter and ripple port H-bridges

smaller capacitor from a different technology. Among the different capacitor technologies, plastic metalized film capacitors have a long lifetime due to their graceful aging [189-191, 200-202]. Therefore, they are a particularly excellent choice to replace large electrolytic capacitor.

Three candidate topologies are chosen for the DC-DC stage of the module-integrated converter. Since galvanic isolation is often a safety requirement in PV inverters, flyback converter, push-pull converter and full-bridge converter are chosen as candidate topologies. This section will explore performance limits of these three candidate topologies used along with an output inverter and a ripple port. Figure 5-12 illustrates the schematic for ripple-port module integrated inverter (RP-MII).

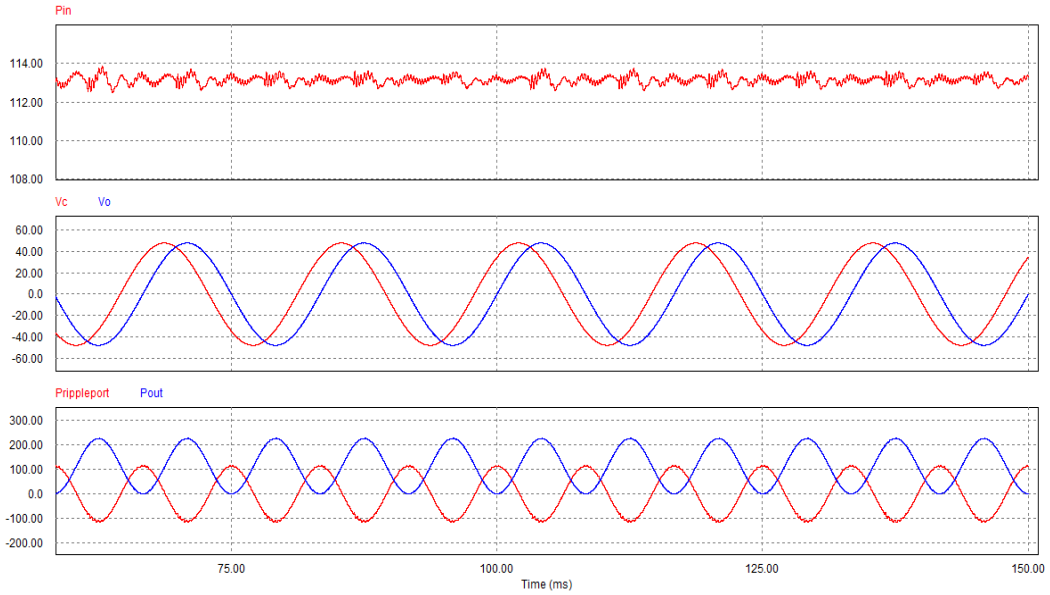


Figure 5-11. Simulation results for a 48V_{peak} 110W system

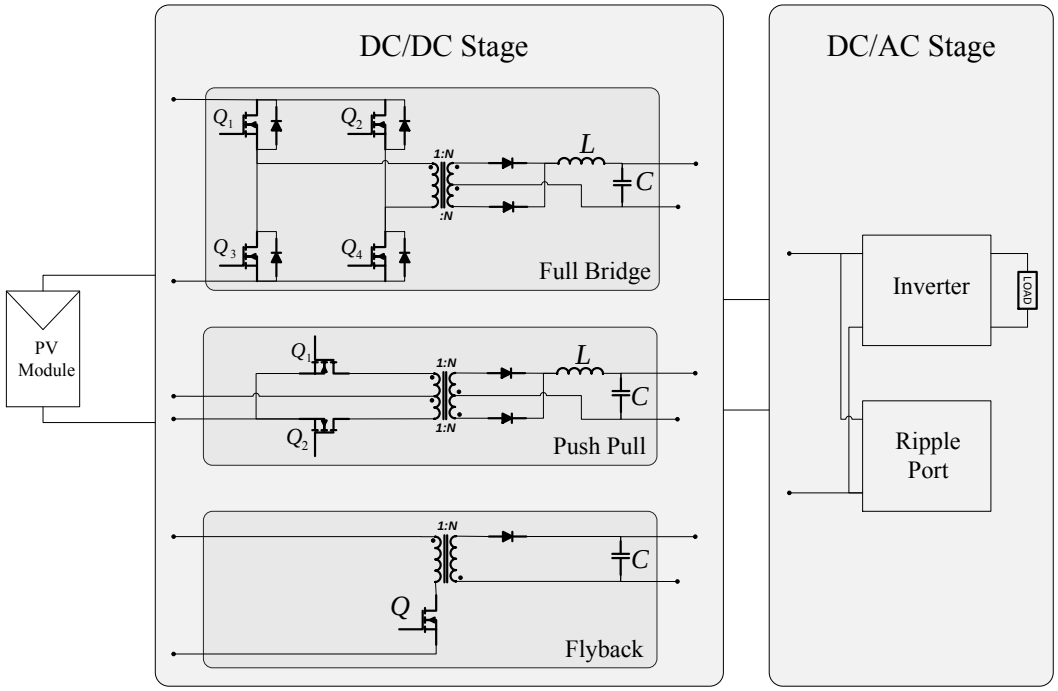


Figure 5-12. Candidate topologies for the dc/dc input converter of the RP-MII

5.6.1. Operation of the converter

5.6.1.1. Output inverter and ripple port

Both the output inverter and the ripple port are H-bridge inverters with sinusoidal-triangular modulation index, used also in ¶4.2. Instead of an LC filter for the output inverter, an LCL filter is considered Compared to LC filter, an LCL filter provides better harmonic filtering grid-tied applications [162].

Current flowing in the AC side of the converter can be calculated by applying the superposition principle, since harmonic content of the PWM voltage is known from (4-14):

$$I_{o,i} = \frac{V_{o,i}}{Z_{o,i}}$$
$$I_{rp,i} = \frac{V_{rp,i}}{Z_{rp,i}} \qquad (5\text{-}17)$$

where $V_{o,i}$ and $V_{rp,i}$ are amplitudes of i^{th} harmonic across output filter and ripple port components respectively and $Z_{o,i}$ and $Z_{rp,i}$ are impedances of output filter plus load and ripple port passive components for i^{th} harmonic, respectively.

Current on the DC side is also required to be calculated in order to check for low-frequency content to determine if ripple port is working properly. To achieve this calculation, the time-domain transfer function for the output inverter H-bridge can be formulated as below.

$$V_o = V_{dc} \times SWF_o \qquad (5\text{-}18)$$

where

$$SWF_o = A_0 \sin(\omega_0 t + \varphi_0) + A_1 \sin(\omega_1 t + \varphi_1) + ... + A_n \sin(\omega_n t + \varphi_n) \quad (5\text{-}19)$$

is the time domain transfer function and represents the amplitude for a frequency in the frequency spectrum of the output voltage. Since an infinite number of frequencies are present in the frequency spectrum of the PWM waveform, voltage harmonics smaller than 1% of the fundamental frequency component are ignored. Therefore, one can form a finite SWF_o. Values $A_0 ... A_n$ and $\varphi_0 ... \varphi_n$ for SWF_o can be constructed from (4-14).

Because there is no energy storage device in the H-bridge itself, the instantaneous power must be equal in either side of the H-bridge. Therefore:

$$V_{dc} I_{dc} = V_o I_o \quad (5\text{-}20)$$

From (5-18) and (5-20):

$$V_{dc} I_{dc} = V_{dc} \cdot SWF_o \cdot I_o \quad \rightarrow \quad I_{dc} = SWF_o \cdot I_o \quad (5\text{-}21)$$

Using trigonometric identities, amplitude and phase of bridge input current for each frequency of interest can be found. The frequency spectrum of the DC-side current is larger than that of the output current due to presence of sidebands. Since SWF_o and I_o should be multiplied term by term to obtain the harmonic content of DC-side current, products as in the following equation are possible.

$$\begin{aligned} & I_{o,i} SWF_{o,j} \sin(2\pi f_s t + \varphi_i) \sin(2\pi [f_s + 3 f_o] + \varphi_j) \\ & = \frac{A_i A_j}{2} \left[\cos(2\pi \cdot 3 f_o + \varphi_j - \varphi_i) - \cos(2\pi \cdot [2 f_s + 3 f_o] + \varphi_j + \varphi_i) \right] \end{aligned} \quad (5\text{-}22)$$

where f_s and f_o are switching and fundamental frequency, and $I_{o,i}$ and $SWF_{o,j}$ are amplitudes of the output current and the time-domain transfer function in f_s and $f_s + 3f_o$, respectively. As evidenced, this product contains some harmonic content in $3f_o$ while neither I_o nor SWF_o contains any harmonic content in that frequency. Such low-frequency content also requires limitation to keep the decoupling capacitor small. This restricts the amount of high-frequency content (switching frequency and sidebands) generated by the ripple port due to the capacitor switching. In other words, switching across the capacitor may create low-frequency content at the input current as well as high-frequency content, which should be limited in design.

5.6.1.2. Flyback converter

A schematic of a flyback converter is illustrated in Figure 5-13. In a flyback converter, the transformer is both an isolator and energy storage device and therefore, has different design considerations than other high-frequency transformers.

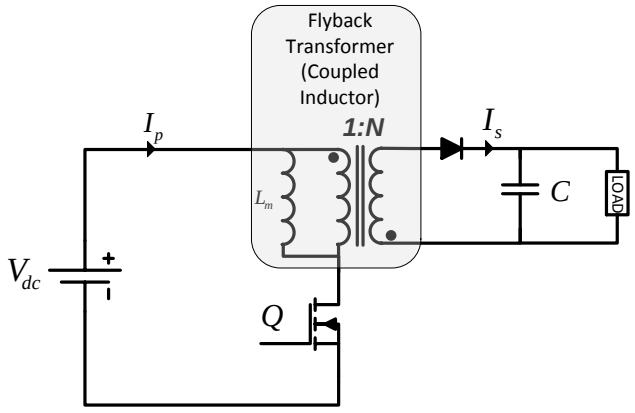


Figure 5-13. Schematic of a flyback converter

Figure 5-14 illustrates the primary and secondary current waveforms of flyback converter in continuous conduction mode. When the switch is closed, the current starts flowing in the primary winding of the transformer through the magnetizing inductance. Due to the polarity of transformer windings, no current passes through the secondary waveforms since the diode in the secondary is reverse-biased. When the switch is opened, the current lacks any path to flow in the primary; thus energy is transferred to the secondary, causing the diode to turn on and conduct the current to the load. Due to the nature of the flyback transformer, primary and secondary windings do not conduct any current simultaneously; therefore, the flyback transformer is often considered two coupled inductors rather than a transformer.

Volt-second balance across the transformer magnetizing inductance results in following relationship between input and output voltage [188].

$$V_o = V_{dc} \cdot N \cdot \frac{D}{1-D} - V_d \tag{5-23}$$

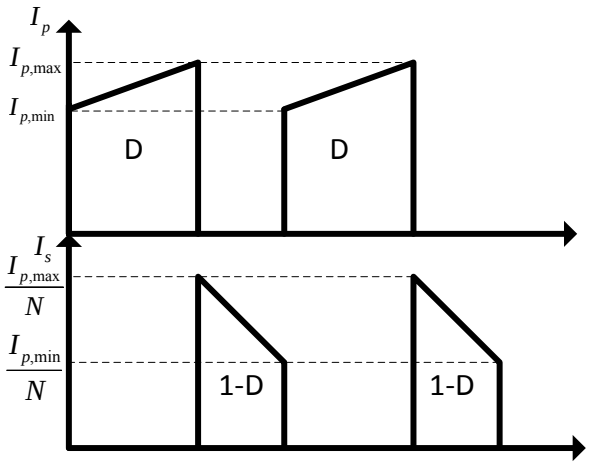


Figure 5-14. Primary and secondary current in a flyback converter (D is duty cycle)

where V_d is diode voltage drop and D is the duty ratio. In discontinuous conduction mode, however, the relationship between the input and output voltage is as given in (5-24). More advanced analysis of flyback converter can be found in [188].

$$V_o = V_{dc} \cdot N \cdot \frac{D}{\frac{2I_o.L_m}{V_{dc}.DT_s} - D} - V_d \qquad (5\text{-}24)$$

5.6.1.3. Full-bridge converter

Figure 5-15 illustrates the schematic of the full-bridge forward converter. Unlike the flyback converter, the full-bridge transformer is used only to provide isolation and stepping up the voltage rather than to store and release energy which is necessary in DC-DC converters. The inductor in the secondary side of the full-bridge converter is used as the energy storage component.

Figure 5-16 shows the basic waveforms of the full-bridge converter. The H-bridge creates a rectangular AC waveform with a duty cycle *D*, which is rectified at the secondary side of the transformer and connected to an LC filter similar to the LC filter in

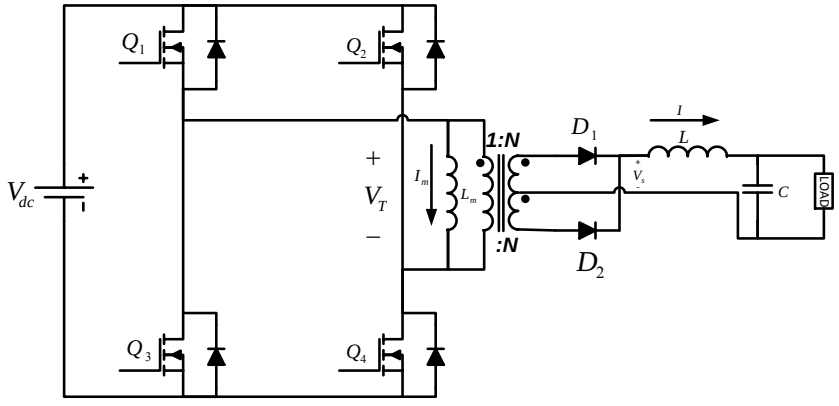


Figure 5-15. Schematic of full-bridge converter

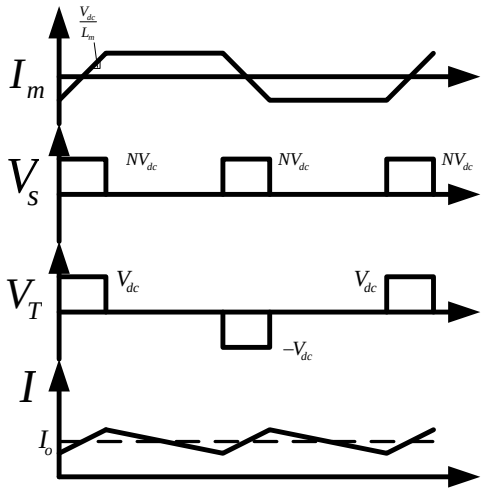


Figure 5-16. Basic waveforms of full-bridge converter

a buck converter. The output voltage to input voltage is, therefore, similar to the buck converter:

$$V_o = V_{dc} \cdot N \cdot D - 2V_d \tag{5-25}$$

where V_d is the voltage drop of the diodes on the secondary side.

5.6.1.4. Push-pull converter

The push-pull converter is also a buck-derived converter and operates similar to the full-bridge converter. Indeed, the secondary sides of push-pull and full-bridge converters are identical. Figure 5-17 illustrates the schematic of push-pull converter.

The push-pull converter operates similarly to the full-bridge converter, though the exception of having two switches instead of four, which is expected to lower

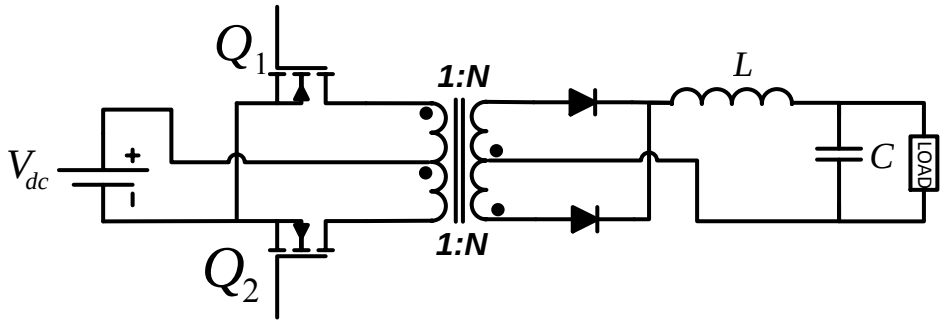


Figure 5-17. Schematic of push-pull converter

semiconductor losses. The push-pull transformer also contains a center-tapped winding in the primary.

5.6.2. Objective functions

Three performance indices were chosen in exploring performance limits. The volume of the converter or the sum of the volume of individual components, including inductors, transformers, capacitors, and the heat sink comprises one of the performance indices. Reliability was also chosen as a performance index and MIL 217 handbook [203] was selected to model the reliability. Reliability modeling will be explained more in the modeling section (section 5.6.4)

Efficiency was chosen as the final performance index. Since PV converters operate in different load conditions throughout a year, comparing single-point efficiency of converters might be misleading, since a converter with good full load efficiency might not have equivalently adequate efficiency in lighter loads. To address this drawback in the optimization, a weighted efficiency model [204] developed by California Energy

Commission (CEC) is employed. In this model, efficiency is calculated for various load levels and weighted efficiency is calculated from a weighted linear combination of these values. Equation (5-26) shows this calculation.

$$\eta_{wtd} = F_1\eta_5 + F_2\eta_{10} + F_3\eta_{20} + F_4\eta_{30} + F_5\eta_{50} + F_6\eta_{75} + F_7\eta_{100} \quad (5\text{-}26)$$

where η_5, η_{10}, etc. are the efficiency values for load levels of 5%, 10%, etc. and F_1-F_7 are the weighting factors. The values for weighting factors are presented in Table 5-I.

Table 5-I. Weighting factors for CEC weighted efficiency

Factor	Load level	Value	
		High insolation	Low insolation
F_1	5%	0.00	0.03
F_2	10%	0.04	0.06
F_3	20%	0.05	0.13
F_4	30%	0.12	0.10
F_5	50%	0.21	0.48
F_6	75%	0.53	0.00
F_7	100%	0.05	0.20

5.6.3. Approach

A three dimensional Pareto front for the entire converter is the best way to reveal the performance limits of the system; however, in order to reduce the complexity and computation time, it is assumed that the DC-DC stage and the inverter-ripple port stage

are decoupled from each other. This assumption is justified if the voltage ripple on the DC link is negligible. Since low-frequency ripple minimization is targeted in the design of the converter, only high-frequency ripple has to be kept low, which can be accomplished by a small high frequency filter capacitor. Therefore, a Pareto front for each stage of the converter (one for inverter and ripple port and one for each DC-DC topology, four in total) will be considered. In order to select the best option for the DC-DC converter, Pareto fronts of three DC-DC topologies will be compared. A design optimization program was written in MATLAB, called MII-MOO (module-integrated inverter multi-objective optimization) throughout the remainder of this dissertation.

5.6.4. Modeling

5.6.4.1. Design variables

Design variables from nearly all power stage components were chosen for each stage of the converter. Design variables for the full bridge and push-pull converters, flyback converter and output inverter-ripple port stage are listed in Table 5-II, Table 5-III and Table 5-IV respectively.

Among these design variables, switching frequency, transformer and inductor core and winding properties, capacitor dimensions and heat sink specific resistance are known, used and explicated in previous sections. Two new types of design variables are introduced: extra heat sink length and number of parallel MOSFETs. In the design process, heat sink extrusion length is specified based on selected thermal resistance and power dissipation of semiconductors so that the junction temperature does not exceed the maximum allowed value. However, extra length for the heat sink will keep the junction

Table 5-II. Design variable for full-bridge and push-pull converters

Component	Design variables
General	Switching frequency
Transformer	Core geometry, Core air gap length, core material, primary turns, primary conductor gauge, secondary turns, secondary conductor gauge
MOSFET	Number of parallel MOSFETs, Gate resistance
Heat Sink	Specific thermal resistance, extra heat sink length to reduce junction temperature
Filter Capacitor	Capacitor geometries (film width, film length and film thickness)
Filter Inductor	Core geometry, Core air gap length, core material, Number of turns, Conductor gauge

Table 5-III. Design variables for flyback converter

Component	Design variables
General	Switching frequency
Transformer	Core geometry, Core air gap length, core material, primary turns, primary conductor gauge, secondary turns, secondary conductor gauge
MOSFET	Number of parallel MOSFETs, Gate resistance
Heat Sink	Specific thermal resistance, extra heat sink length to reduce junction temperature
Filter Capacitor	Capacitor geometries (film width, film length and film thickness)

temperature lower still, rendering lower failure rate and higher reliability of the power MOSFET. Reliability modeling will be explained later in this section.

It is also known that the gate-to-source capacitance of thepower MOSFET (C_{GS}) is proportional and on-state drain-source resistance ($R_{ds,ON}$) is inversely proportional to the MOSFET die area [158]. This relationship can be written in mathematical form:

$$C_{GS} = K_1 \cdot A_{die}$$
$$R_{ds,ON} = K_2 \cdot \frac{1}{A_{die}} \quad (5\text{-}27)$$

Table 5-IV. Design variable for output and ripple port inverters

Component	Design variables
General	Switching frequency, modulation index and switching angle for both converters
Filter Inductors	Core geometry, Core air gap length, core material, number of turns, conductor gauge
MOSFET	Number of parallel MOSFETs, Gate resistance
Heat Sink	Specific thermal resistance, extra heat sink length to reduce junction temperature
Filter Capacitor	Capacitor geometries (film width, film length and film thickness)
Ripple port Inductor	Core geometry, Core air gap length, core material, Number of turns, Conductor gauge
Ripple port Capacitor	Capacitor geometries (film width, film length and film thickness)

where K_1 and K_1 are constant scalars. It will be revealed in the loss modeling section that larger C_{GS} results in slower turning on and off for the MOSFET and therefore, higher switching losses [205]. Conversely, larger $R_{ds,ON}$ results in higher conduction losses. Therefore, by adjusting chip area, it is possible to reach an optimum point in terms of losses for a certain operating condition.

If the effects of packaging on C_{GS} and $R_{ds,ON}$ are neglected, paralleling similar MOSFETs has the same effect as increasing the chip area [42]; therefore, the number of parallel MOSFETs was selected as a design variable.

5.6.4.2. Loss modeling

Loss modeling for passive components in inverter and ripple port circuits has been explained in ¶4.2.2. The same approach (Natural Steinmetz equation for the core losses,

Dowell equation for the copper losses and estimating the capacitor losses from (4-15), (4-16) and (4-17)) will also be employed in this section.

For inductors in the DC-DC converters and flyback transformer, the original Steinmetz equation is employed [188], since the variation of flux is only in one frequency (switching frequency) despite being non-sinusoidal.

$$P_{Core,DC} = K \cdot f_s^{\alpha} \cdot \Delta B^{\beta} \tag{5-28}$$

where ΔB is the variation in flux density due to current ripple. In push-pull and full-bridge transformers, however, the magnetizing current is AC and has a trapezoidal waveform (see Figure 5-16). Though the current and thus flux density are not of sinusoidal shape, the original Steinmetz equation is used to calculate the core losses, neglecting higher frequency effects. The accuracy of using original Steinmetz equation is justified since that minor B-H loops (Figure 5-18) are not present in the transformer core, because of the current waveform of Figure 5-16. Minor B-H loop is a nonlinear phenomenon which happens due to alternating flux reversal in magnetic cores, which in turn occurs when a high-frequency flux is added to a low-frequency fundamental flux component [206, 207]. Minor loops are highly nonlinear and difficult to model [208].

For copper losses in inductors and transformers of the DC-DC converters, the Dowell equation, along with the Fourier series of current, was used. Even though high-frequency effects may be negligible in low-ripple conditions, they might be considerable in discontinuous conduction mode; since the efficiency is evaluated for different load levels, high-frequency effects should be considered. Capacitor losses are calculated using

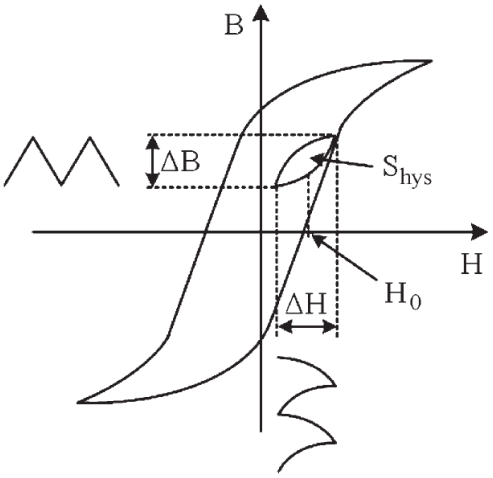


Figure 5-18. Illustration of minor B-H loops

ESR for switching frequency since current ripple, which only has a switching frequency component, passes through the capacitor.

Conduction losses of MOSFETs in the inverter and the ripple port H-bridges are calculated using the same approach as IGBT with the distinction being the lack of constant forward voltage drop. Indeed, drain-to-source resistance is the only loss mechanism. Therefore, conduction losses can be calculated from the equation below, also reported in [209].

$$P_{cond,AC} = (\frac{1}{8} + \frac{M\cos\theta}{3\pi})R_{ds,ON} I_{peak}{}^2 + (\frac{1}{2\pi} - \frac{M\cos\theta}{8})V_d I_{peak} \quad (5\text{-}29)$$

where M is the modulation index, θ is the phase delay of current with regard to voltage, V_d is diode voltage drop and I_{peak} is the peak current. Conduction losses in DC-DC converters can also be calculated from:

$$P_{cond,DC} = R_{ds,ON}(DI_{dc})^2 \quad (5\text{-}30)$$

where I_{dc} is the converter input current and D is the converter duty cycle. Calculating switching losses is more complex and requires an understanding of MOSFET switching process.

Figure 5-19 shows MOSFET switching waveforms and MOSFET capacitances [205]. As soon as the gate-source voltage becomes larger than the threshold voltage, the MOSFET begins to conduct current. When V_{GS} reaches $V_{plateau}$, current has reached its final level and V_{ds} starts to decrease. During voltage reduction, V_{GS} remains constant at $V_{plateau}$. There is a switching energy loss for each of the current and voltage rise and fall times, which accumulate to reflect the total switching energy loss. t_{ri}, t_{fu}, t_{fi},and t_{ru} are usually given in the datasheet for certain operating conditions. Calculating these times based on any given set of operating conditions will be explained as follows.

Current rise and fall times are mainly controlled by charging and discharging C_{GS} through gate resistance. For a given gate resistance, these times can be calculated via the

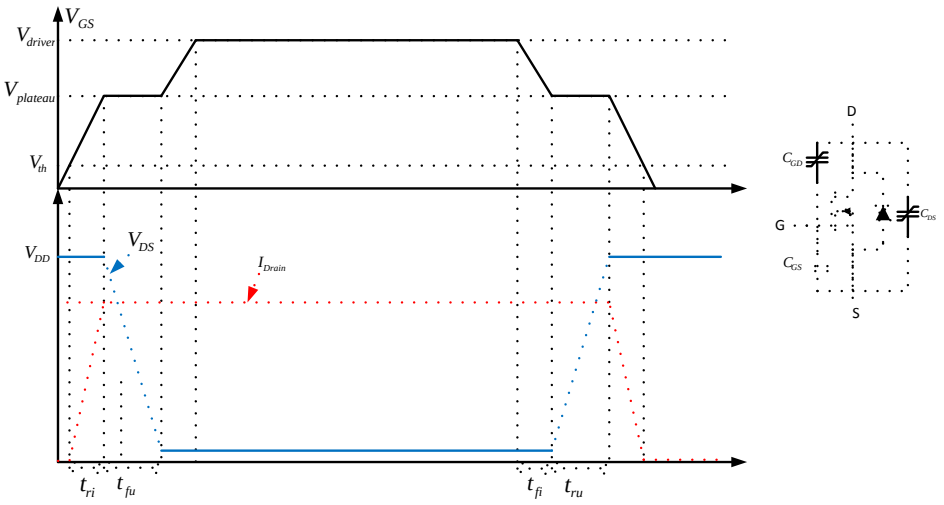


Figure 5-19. MOSFET capacitances and MOSFET switching waveforms

below equation:

$$t_{ri} = t_{ri,b} \cdot \frac{R_G}{R_{G,b}}$$
$$t_{fi} = t_{fi,b} \cdot \frac{R_G}{R_{G,b}} \quad (5\text{-}31)$$

where $t_{ri,b}$, $t_{fi,b}$, $R_{G,b}$ and R_G are datasheet rise time, datasheet fall time, datasheet gate resistance and current gate resistance respectively. Voltage fall and rise times are, however, more complicated to obtain since they are controlled by charging and discharging highly nonlinear gate-drain capacitance. Voltage fall and rise times are provided via the following.

$$t_{fu} = (V_{DD} - R_{ds,ON} I_D) \cdot R_G \cdot \frac{C_{GD}}{V_{driver} - V_{Plateau}}$$
$$t_{ru} = (V_{DD} - R_{ds,ON} I_D) \cdot R_G \cdot \frac{C_{GD}}{V_{Plateau}} \quad (5\text{-}32)$$

where V_{DD} is the off-stage voltage across MOSFET, and I_D is the drain current. C_{GD} is a highly nonlinear capacitor and changes as V_{ds} falls. Therefore, usually a median of this capacitance in high V_{ds} and low V_{ds} is considered in (5-32). A plot showing different values for C_{GD} is usually given in the datasheet. $V_{plateau}$ is given in the datasheet, but it depends on drain current and has to be adjusted for the drain current in specific application. According to [158]:

$$V_{plateau} - V_{th} \propto \sqrt{I_D} \quad (5\text{-}33)$$

Therefore, $V_{plateau}$ can be calculated from:

$$V_{plateau} = V_{th} + \sqrt{\frac{I_D}{I_{D,b}}} \cdot (V_{plateau,b} - V_{th}) \quad (5\text{-}34)$$

where $V_{plateau,b}$ and $I_{D,b}$ are datasheet value for $V_{plateau}$ and drain current in which $V_{plateau}$ is given respectively.

After calculating t_{ri}, t_{fu}, t_{fi},and t_{ru} switching energy losses can be calculated as follows:

$$E_{on} = V_{DD} \cdot I_D \cdot \frac{t_{ri} + t_{fu}}{2}$$
$$E_{off} = V_{DD} \cdot I_D \cdot \frac{t_{ru} + t_{fi}}{2} \quad (5\text{-}35)$$

Diodes also dissipate energy because of reverse recovery. Energy loss because of diode reverse recovery is calculated as follows:

$$E_{rr} = \frac{1}{4} \cdot Q_{rr} \cdot V_{DD} \quad (5\text{-}36)$$

where Q_{rr} is the reverse recovery charge. Q_{rr} is usually scaled based on drain current:

$$Q_{rr} = Q_{rr,b} \cdot \frac{I_D}{I_{D,b}} \quad (5\text{-}37)$$

where $Q_{rr,b}$ and $I_{D,b}$ are datasheet value for reverse recovery charge and the current in which it is measured, respectively.

For the DC-DC converters, equations (5-31) to (5-37) are easily employed, since the current switched by the MOSFETs is the same from one switching cycle to another. However, in two H-bridges where sinusoidal-triangular PWM is used, current varies throughout a cycle of sinusoidal waveform. Therefore, switching energies should be integrated over at least half of the fundamental period. Half of the period is enough since switching energies are only scaled with current magnitude, not with its direction.

Therefore, switching energies in the output inverter and ripple port will be calculated as follows.

$$E_{on} = \frac{1}{\pi}\int_0^{\pi} E_{on}(\theta)d\theta$$
$$E_{off} = \frac{1}{\pi}\int_0^{\pi} E_{off}(\theta)d\theta \quad (5\text{-}38)$$

These integrals can be calculated for a closed form answer for several mentioned switching energies such as,

$$E_{on,1}(\theta) = V_{DD}\cdot I_D \cdot \frac{t_{ri}}{2} = V_{DD}\cdot I_{D,m}\sin(\theta)\cdot t_{ri,b}\cdot\frac{R_G}{2R_{G,b}}$$
$$E_{on,1} = \frac{1}{\pi}\int_0^{\pi} E_{on,1}(\theta)d\theta = V_{DD}\cdot I_m \cdot t_{ri,b}\cdot\frac{R_G}{\pi R_{G,b}} \quad (5\text{-}39)$$

or,

$$E_{rr}(\theta) = \frac{1}{4}\cdot Q_{rr}\cdot V_{DD} = \frac{1}{4}Q_{rr,b}\cdot\frac{I_{D,m}\sin(\theta)}{I_{D,b}}\cdot V_{DD}$$
$$E_{rr} = \frac{1}{\pi}\int_0^{\pi} E_{rr}(\theta)d\theta = \frac{Q_{rr,b}\cdot I_{D,m}\cdot V_{DD}}{I_{D,b}\cdot 2\pi} \quad (5\text{-}40)$$

However, a closed form solution for several some of the switching energies is difficult to calculate. For example,

$$E_{on,2}(\theta) = V_{DD}\cdot I_D\cdot\frac{t_{fu}}{2} = \frac{1}{2}V_{DD}\cdot I_{D,m}\sin(\theta)$$
$$\times (V_{DD} - R_{ds,ON} I_{D,m}\sin(\theta))\cdot R_G$$
$$\times \frac{C_{GD}}{V_{driver} - V_{th} - \sqrt{\frac{\cdot I_{D,m}\sin(\theta)}{I_{D,b}}}\cdot(V_{plateau,b} - V_{th})} \quad (5\text{-}41)$$

$$E_{on,2} = \frac{1}{\pi}\int_0^{\pi} E_{on,2}(\theta)d\theta \quad (5\text{-}42)$$

Calculating a closed form solution for (5-42), if not impossible, proves certainly difficult. Therefore, this integration is performed numerically in the MII-MOO. Using the example of (5-39) to (5-42), off-state switching energies can also be derived. Finally, switching losses can be calculated from the following.

$$P_{sw} = (E_{om} + E_{off} + E_{rr}) \cdot f_s \tag{5-43}$$

where f_s is the switching frequency. Finally, driver losses can be calculated from equation below.

$$P_{driver} = \frac{1}{2} Q_g \cdot V_{driver} \cdot f_s \tag{5-44}$$

where Q_g is the total gate charge and can be found in the datasheet and V_{driver} is gate drive voltage.

5.6.4.3. Volume modeling

Volume modeling is achieved using the dimensions of the passive components and heat sink. Volume of the heat sink is estimated from (4-13), and volume of the film capacitors is also directly calculated from capacitor dimensions, as explained in 4.2.3. Since semiconductor switches contribute little to the volume of the converter, they were excluded from volume modeling.

EE cores were chosen for the inductors and transformers (see Figure 4-12). A study on 58 core geometries from Micrometals and Ferroxcube reveals a linear relationship between the different dimensions of their EE cores. These relationships were approximated using a curve fit as follows:

$$B(in) = 1.056A9(in) - 0.1392$$
$$C(in) = 0.2879A(in) + 0.06486 \quad (5\text{-}45)$$
$$D(in) = 0.7292B(in) - 0.0633$$

Using the above equations facilitates expression of the core volume with only one design variable. This is a form of "Reduced Order Modeling", which enables simplified models without loss of much accuracy, a process routinely done in magnetic devices due to complexity of detailed models [210]. Therefore, instead of using all of the dimensions as design variables, only dimension *A* was chosen.

5.6.4.4. Reliability modeling

Reliability modeling of electronic parts involves an extensive amount of physical testing under different stress levels. Currently, failure rates provided by MIL-217 handbook [203], are used most often for reliability modeling. According to [203], failure rate of components in electronic circuits depend on a variety of operational and environmental parameters. Table 5-V summarize failure rates for individual components.

In Table 5-V, λ_P is the failure rate of each component (failures per million hours), λ_b for each component is the base failure rate and π_T, π_A, π_Q, π_S, π_C and π_{CV} are the temperature factor, application factor , quality factor, stress factor, capacitance factor and capacitor voltage stress factor, respectively. π_E is known as environmental factor, set to unity in all calculations. Failure rate of the converter can be calculated adding the failure rate of individual components.

Table 5-V. Failure rates for individual components

Component	Failure rate
MOSFET	$\lambda_{P\_S} = n \cdot \lambda_{b\_S} \pi_T \pi_A \pi_Q \pi_E$ $\lambda_{b\_S} = 0.012$ $\pi_T = \exp\left(-1925\left(\frac{1}{T_m + 273} - \frac{1}{298}\right)\right)$ $\pi_A = 8\ (50\text{W} \le \text{P}_\text{r} < 250W)$ $\pi_Q = 5.5$
Diode	$\lambda_{P\_D} = n \cdot \lambda_{b\_D} \pi_T \pi_S \pi_C \pi_Q \pi_E$ $\lambda_{b\_D} = 0.025$ $\pi_S = \begin{cases} 0.054 & V_S < 0.3 \\ V_S^{2.43} & 0.3 < V_S < 1 \end{cases}$ $\pi_Q = 5.5$
Film Capacitor	$\lambda_{P\_C} = n \cdot \lambda_{b\_C} \pi_{CV} \pi_Q \pi_E$ $\lambda_{b\_C} = 0.00254 \cdot \left(\left(\frac{S}{0.5}\right)^3 + 1\right) \cdot \exp\left(5.09 \cdot \left(\frac{T_m + 273}{378}\right)^5\right)$ $\pi_{CV} = 0.34C^{0.18}$ $\pi_Q = 10$
Inductor and Transformer	$\lambda_{P\_I} = n \cdot \lambda_{b\_I} \pi_T \pi_Q \pi_E$ $\pi_T = \exp\left(\frac{-0.11}{8.617 \cdot 10^{-5}} \cdot \left(\frac{1}{T_m + 273} - \frac{1}{298}\right)\right)$ $\pi_Q = 3$

5.6.5. Constraints

In this subsection, constraints considered in RP-MII will be presented.

- **Maximum current of switches:** Current in the devices should not be more than the rating of the device. This is particularly important in the ripple port, where, if inductor is not large enough, high-frequency currents flow because of switching across the capacitor which may destroy the MOSFETs.
- **Maximum flux density of the cores:** Flux density should be maintained below the saturation level in magnetic cores for transformers and inductors. For the DC-DC converters, it is easy to calculate the maximum flux density from the maximum current. For inductors used in the AC side of inverter and ripple port, the maximum current is considered to be the sum of amplitude of all considered harmonics, since frequencies of interest are apart from each other by some orders of magnitude.
- **Low-frequency content of DC bus current:** To achieve replacement of bulk decoupling capacitor with a small capacitor, the MII-MOO has to gauge whether low-frequency content of DC bus current is below a certain level. This level was assessed as 10% of fundamental current
- **Harmonic content of inverter output current:** IEEE 519-1992 [123] was chosen as the benchmark for harmonic levels. In IEEE 519-1992, harmonic levels are evaluated with regard to the total demand current, not necessarily the fundamental frequency component. In this design example, full load current was chosen as total demand current.

- **Duty cycle of flyback converter:** High duty cycles in the flyback converter may lead to instabilities and difficulty in control [188]. Therefore, the duty cycle was limited to 80%.
- **DC bus high-frequency ripple:** This ripple was limited to 5% of the voltage. High-frequency ripple is attributable to switching in DC-DC stage or high-frequency current drawn from DC bus due to switching in the inverter and ripple port.

  Table 5-VI summarizes the operational constraints.

Table 5-VI. Operational constraints used in the optimization

Section	Constraint
Output Inverter	Filter inductors should not saturate The harmonic content of output converter should comply with IEEE 519
Ripple port Inverter	Inductor should not saturate
Combination of output and ripple port inverters	Low frequency content of input current (excluding 60Hz and including 120Hz) should be small (less than 10%)
Flyback converter	Flyback transformer should not saturate Duty cycle should be less than 90% - to address possible instability issues
DC Link Capacitor	Should be enough to filter high-frequency current generated by DC-DC converter, inverter and ripple port to keep DC ripple below 5%.

5.6.5.1. Results

A Pareto front for the output inverter and ripple port and three Pareto fronts for three different DC-DC topologies were obtained using the PSO-aided random sampling method. Figure 5-20, Figure 5-21, Figure 5-22 and Figure 5-23 illustrate the Pareto fronts

for the Pareto fronts found by MII-MOO. Figure 5-24 also reveals three Pareto fronts for three DC-DC converters in the same axis. Figure 5-20, Figure 5-21, Figure 5-22 and Figure 5-23, black points show the points which are found by MII-MOO. The meshed surface is drawn in order to visualize the Pareto fronts better. A designer can make tradeoffs within the set of Pareto-optimal designs for each section of the converter.

Figure 5-20 displays the Pareto front for the DC-AC side of the converter, i.e., the

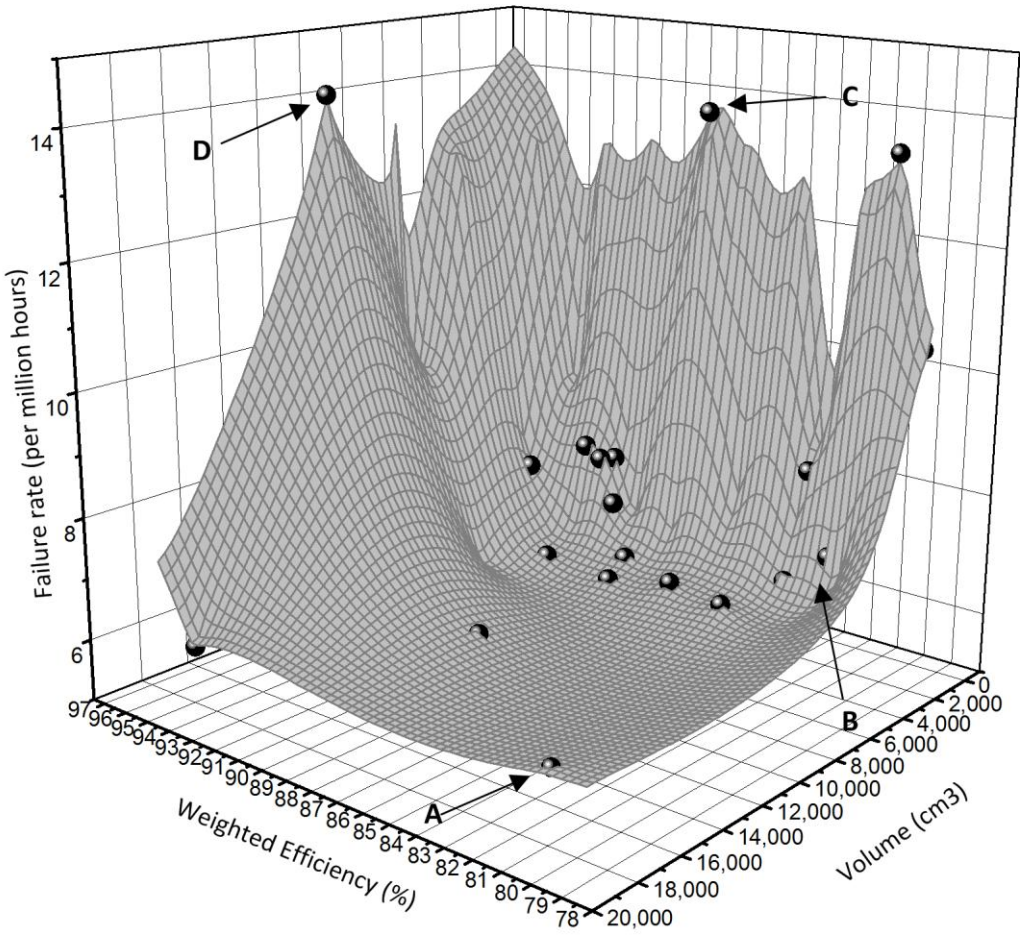


Figure 5-20. Pareto front for output inverter and ripple port from two angles (Black dots show the points found in optimization)

output inverter and the ripple port. This figure can be used by a designer to make tradeoff between the designs based on his/her preference. For instance, if the designer's preference is high reliability, he/she may choose point A as the design point; however, if efficiency is also prioritized, he/she may choose point B. Point C may be suitable if the volume of the converter is the main design objective; point D may be chosen if a higher efficiency is preferred, resulting in a low reliability and fairly large volume.

Figure 5-21, Figure 5-22, and Figure 5-23 show three Pareto fronts for flyback,

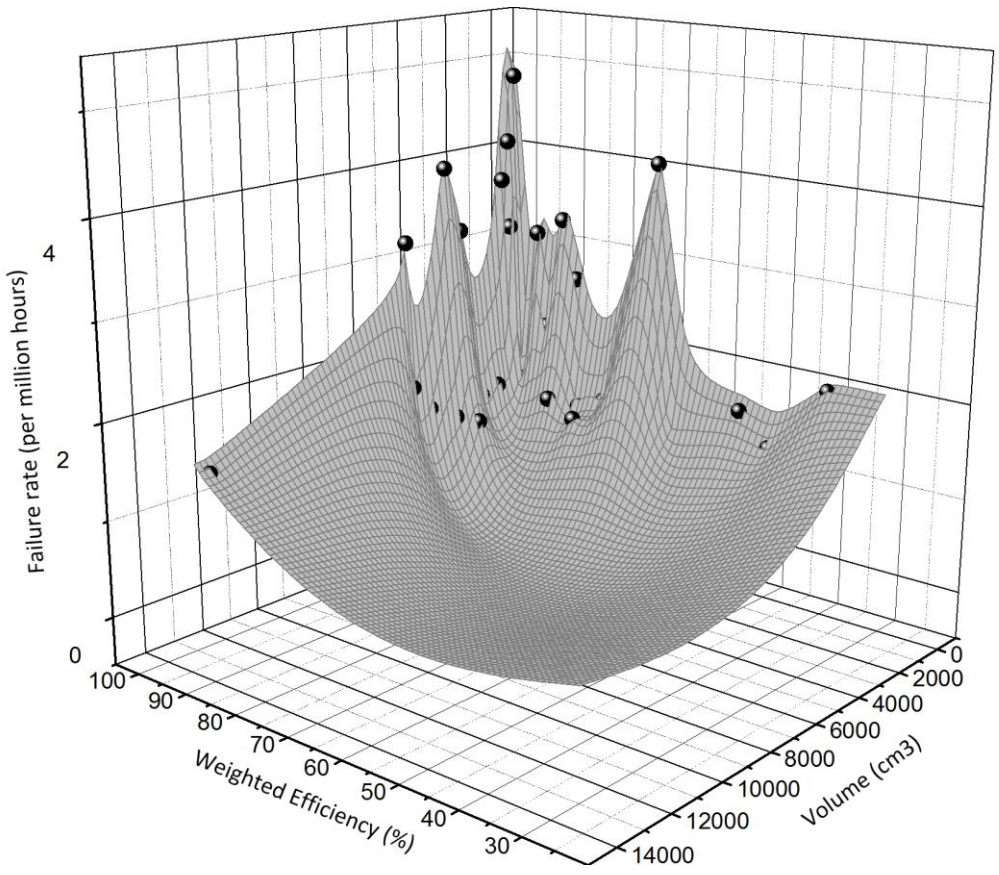


Figure 5-21. Pareto front for flyback converter from two angles (Black dots show the points found in optimization)

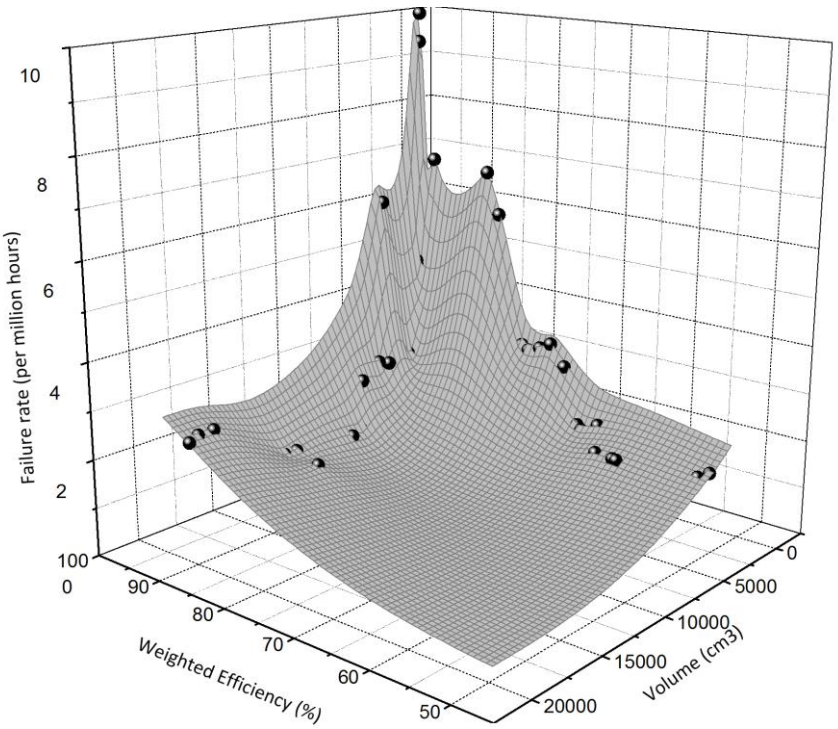


Figure 5-22. Pareto front for push-pull converter from two angles (Black dots show the points found in optimization)

push-pull and full-bridge converters, respectively. By drawing these three Pareto fronts on the same axis (Figure 5-24), one notice that the Pareto front of the flyback converter lies beneath that of push-pull and full-bridge converters. Therefore, every design on the Pareto front of the flyback converter dominates all of the designs of full-bridge and push-pull converters, which reveals that the flyback converter is a better choice for the DC-DC stage of the converter. It is also evident from Figure 5-21, Figure 5-22, and Figure 5-23 that superiority of the flyback converter is owed to its higher reliability, which is related to its lower component count.

After selecting flyback converter as the DC-DC stage topology, it is possible to make tradeoffs similar to those made for the output inverter and ripple port.

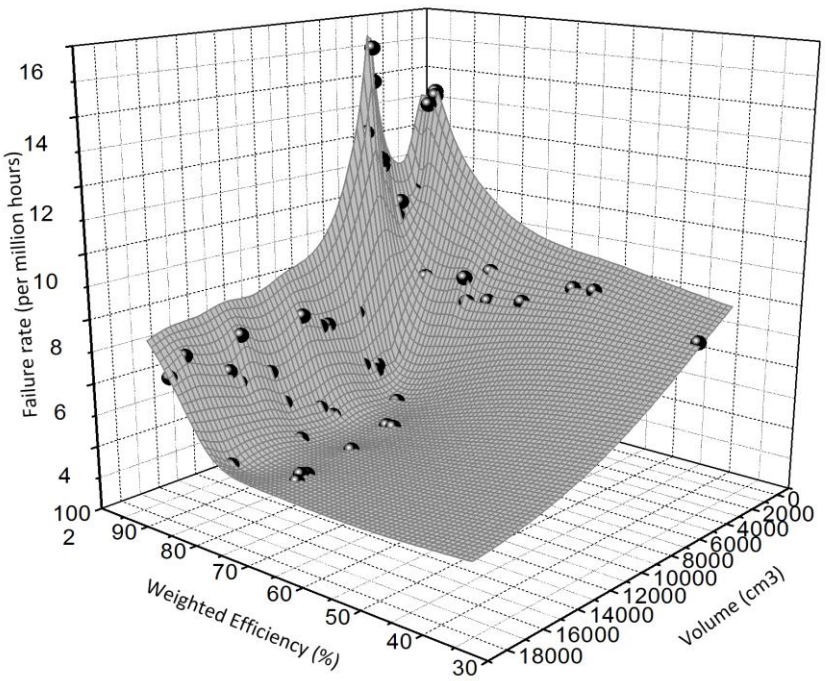


Figure 5-23. Pareto front for full-bridge converter from two angles (Black dots show the points found in optimization)

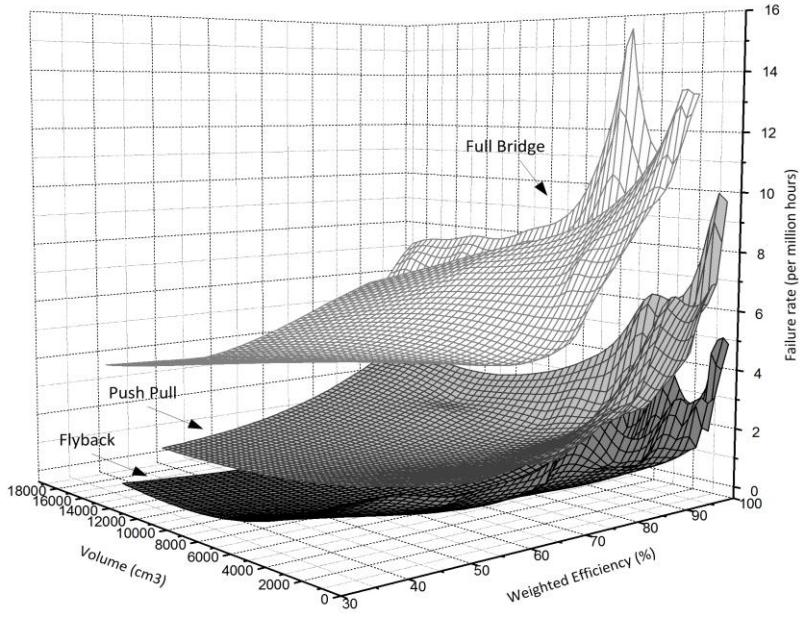


Figure 5-24. Comparison between the Pareto fronts for DC-DC converters

5.7. Experimental verification

In order to verify the results experimentally, I built a MII with a flyback input stage. I also chose the converter design as close as possible to a point on the Pareto fronts of the flyback converter and the output inverter plus ripple port. The verification's purpose is to reveal that the employed models are accurate when the corresponding components are built into an actual converter design. Table 5-VII shows the design variables for the output converter plus ripple port and Table 5-VIII reveals the design variables for the flyback converter.

Details about each of the components will be presented in following subsection.

Table 5-VII. Design variables for inverter and ripple port converters

Variable	Description	From optimization	Built	Unit	Reason for deviation
$f_{s,o}$	Output inverter switching frequency	24062.34	25000	Hz	Rounded
$f_{s,rp}$	Ripple Port Switching frequency	10535	10000	Hz	Rounded
$L_{f,1}$ Core Index	$L_{f,1}$ Core Material	12 (Ferroxcube 3F35)	4 (Ferroxcube 3C90)	-	Availability
N_{Lf1}	$L_{f,1}$ number of turns	198	100	-	Based on selected core
$Gauge_{Lf1}$	$L_{f,1}$ winding gauge	1.319	1.068	mm	Availability
A_{Lf1}	$L_{f,1}$ core dimension A[1]	65.16	93	mm	Availability
B_{Lf1}	$L_{f,1}$ core dimension B[1]	65.39	76	mm	Availability
C_{Lf1}	$L_{f,1}$ core dimension C[1]	20.38	16	mm	Availability
D_{Lf1}	$L_{f,1}$ core dimension D[1]	46.1	48	mm	Availability

Table 5-VII. Design variables for inverter and ripple port converters

Variable	Description	From optimization	Built	Unit	Reason for deviation
g_{Lf1}	$L_{f,1}$ core air gap	7.21	1	mm	Based on selected core
$L_{f,2}$ Core Index	$L_{f,2}$ Core Material	8 (Ferroxcube 3C94)	4 (Ferroxcube 3C90)	-	Availability
N_{Lf2}	$L_{f,2}$ number of turns	198	160	-	Based on selected core
$Gauge_{Lf2}$	$L_{f,2}$ winding gauge	1.118	1	mm	Based on selected core
A_{Lf2}	$L_{f,2}$ core dimension A[1]	65.82	93	mm	Availability
B_{Lf2}	$L_{f,2}$ core dimension B[1]	66.08	76	mm	Availability
C_{Lf2}	$L_{f,2}$ core dimension C[1]	20.57	16	mm	Availability
D_{Lf2}	$L_{f,2}$ core dimension D[1]	46.61	48	mm	Availability
g_{Lf2}	$L_{f,2}$ core air gap	3.851	2	mm	Availability
C_f	Filter capacitance	13.47	10	µF	Availability
$W_{C,f}$	Filter Capacitor film width	221.56	N/A	mm	N/A
$L_{C,f}$	Filter Capacitor film Length	9.61	N/A	m	N/A
$T_{C,f}$	Filter Capacitor film Thickness	6.16	N/A	µm	N/A
L_{rp} Core Index	L_{rp} Core Material	12 (Ferroxcube 3F35)	4 (Ferroxcube 3C90)	-	Availability
N_{rp}	L_{rp} number of turns	28	30	-	Based on selected core
$Gauge_{rp}$	L_{rp} winding gauge	1.08	1.5	mm	Availability
A_{rp}	L_{rp} core dimension A[1]	90.39	93	mm	Availability
B_{rp}	L_{rp} core dimension B[1]	92.05	76	mm	Availability

Table 5-VII. Design variables for inverter and ripple port converters

Variable	Description	From optimization	Built	Unit	Reason for deviation
C_{rp}	L_{rp} core dimension C[1]	27.64	16	mm	Availability
D_{rp}	L_{rp} core dimension D[1]	65.54	48	mm	Availability
g_{rp}	L_{rp} core air gap	8.5956	1.6	mm	Based on selected core
C_{rp}	Ripple port capacitance	43.5	40	µF	Availability
$W_{C,rp}$	Ripple port Capacitor film width	76.8912	N/A	mm	N/A
$L_{C,rp}$	Ripple port Capacitor film Length	45.21	N/A	m	N/A
$T_{C,rp}$	Ripple port Capacitor film Thickness	3.11	N/A	µm	N/A
$R_{g,o}$	Output converter gate resistance	10.2	22	Ω	For lower dv/dt transients
$R_{g,rp}$	Ripple port converter gate resistance	8.6	22	Ω	For lower dv/dt transients
N_{MOSFET}	Number of parallel MOSFETs	1.46	1	-	Rounded up
$R_{sa,spec}$	Heat sink to ambient specific thermal resistance (per 150mm)	0.41	3.23	ºC/W	Availability
L_{extra}	Extra length for heat sink (more than what's necessary)	545.34	244	mm	Availability

[1]. Please see section 10 for details

Table 5-VIII. Design variable for flyback converter

Variable	Description	From optimization	Built	Unit	Reason for deviation
$f_{s,fb}$	Switching frequency	58040.67	58000	Hz	Rounded

Table 5-VIII. Design variable for flyback converter

Variable	Description	From optimization	Built	Unit	Reason for deviation
TR core index	Transformer core material	46	4 (Ferroxcube 3C90)	-	Availability
N_p	Primary winding number of turns	15	10	-	Based on selected core
$gauge_p$	Primary winding wire gauge	2.7	2.05	mm	Availability
N_s	Secondary winding number of turns	31	20	-	Based on selected core
$gauge_s$	Secondary winding wire gauge	1.9	2.05	mm	Availability
A_{TR}	Transformer core dimension A[1]	103.89	93	mm	Availability
B_{TR}	Transformer core dimension B[1]	106.32	7.60E-02	mm	Availability
C_{TR}	Transformer core dimension C[1]	31.53	1.60E-02	mm	Availability
D_{TR}	Transformer core dimension D[1]	75.95	4.80E-02	mm	Availability
g_{TR}	Transformer core air gap	1.91	0.5	mm	Based on selected core
R_g	Gate resistance	1.85	33	Ω	For lower dv/dt transients
C_{DC}	Output Capacitor	17.79	20	µF	Availability
$W_{C,DC}$	DC Capacitor film width	35.72	N/A	mm	N/A
$L_{C,DC}$	DC Capacitor film Length	50.94	N/A	m	N/A
$T_{C,DC}$	DC Capacitor film Thickness	3.98	N/A	µm	N/A
N_{MOSFET}	Number of parallel MOSFETs	1.44	1	-	Rounded
$R_{sa,spec}$	Heat sink to ambient specific thermal resistance (per 150mm)	8.91	2	ºC/W	Availability
L_{extra}	Extra length for heat sink (more than what's necessary)	279	0	mm	Availability

[1]. Please see section 10 for details

5.7.1. Inductors and transformers

Inductors and transformers were designed almost completely by MII-MOO. Though the design was performed based on an EE core, availability issues necessitated, a set of UI cores built from Ferroxcube 3C90 material [211]. UI core was chosen because the magnetic circuit is similar to the magnetic circuit of an EE core. Figure 5-25 shows conversion of an EE core to a UI core.

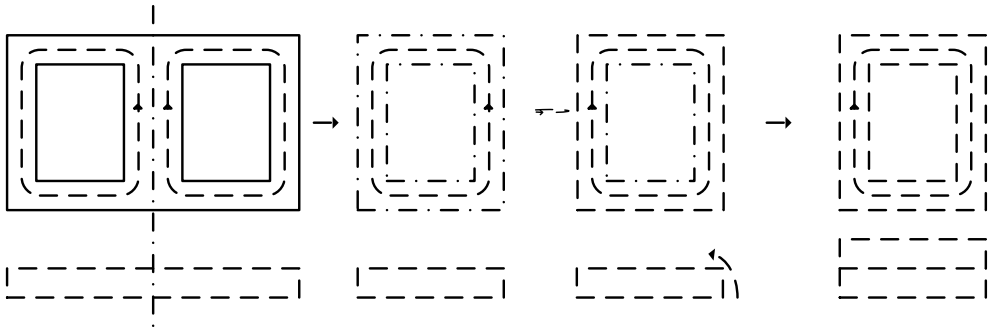


Figure 5-25. Relationship between a UI core and an EE core

The air gap in the magnetic core was created by putting pieces of paper in between the U and I parts of the core, or "shimming". The thickness of the stack of the paper was measured by a micrometer. Table 5-IX reflects values for predicted and measured

Table 5-IX. Predicted and measured inductance for inductors across the system

Inductance	Description	Designed	Measured	Unit
$L_{f,1}$	Filter inductance	6.29	5.6	mH
$L_{f,2}$	Filter inductance	10.54	10	mH
L_{rp}	Ripple port inductance	1.68	1.75	mH
$L_{m,TR}$	Flyback transformer magnetizing inductance	100	105	μH

inductance (measured by a PM6304 Philips LCR meter).

The flyback transformer also has a leakage inductance, which is important in the snubber design. This inductance was measured as 1.5 µH.

5.7.2. Capacitors

Capacitors are not usually custom-designed and therefore, it is difficult to find a capacitor with exactly the same specifications. Therefore, the ripple port capacitor was chosen from 10µF MKT capacitors from EPCOS [212]. Table 5-X shows volume of the actual capacitors compared to volume obtained from MII-MOO.

5.7.3. Heat sinks

The heat sinks were chosen based on the output of the optimization program and extrusion profiles available from Aavid Thermalloy. The initial intention was to use one heat sink for the output inverter and ripple port; however, two heat sinks were used due to EMI issues and because moving two converters away from each other proved necessary. Table 5-XI shows the chosen heat sinks for different parts of the converter. Expected specific volume of the converter is also reported in Table 5-XI. The difference between expected volume and actual volume of the heat sink is because the selected heat sinks are not on the Pareto fronts of the heat sink profiles (Figure 4-8).

Table 5-X. Volume of the designed capacitors and the actual ones which were used

Capacitance	Description	Designed	Actual	Unit
$C_{f,1}$	Filter Capacitance	34	18	cm^3
C_{rp}	Ripple port capacitance	121	72	cm^3
$C_{dc,flyback}$	Flyback DC capacitance	56	36	cm^3

Table 5-XI. Heat sinks used in different parts of the converter

Description	Part number	Specific thermal resistance (for 150mm)	Specific volume (1000 mm^3 for 1m length)	Expected specific Volume (1000 mm^3 for 1m length)
Output inverter heat sink	65250	3.23	989.9	556.9
Ripple port heat sink	65250	3.23	989.9	556.8
Flyback heat sink	62200	2	1920.24	977.59

5.7.4. MOSFET

To reduce switching losses, a MOSFET with low rise and fall time, which also has a relatively low on-state resistance, is required. After searching MOSFETs from different companies, a 9.9A 600V MOSFET (IPP60R199CP) by Infineon was selected. This MOSFET has an on-state resistance of 199 milliohms and rise and fall time of 5 and 5 nanoseconds in standard test conditions, respectively.

5.7.5. Control

A TI DSP microcontroller (TMS320F28335 floating point [213]) was utilized to generate gate signals for the converter. HCPL 3180 opto-driver from Avago technologies [214] was employed to drive the MOSFETs.

5.7.6. Flyback snubber circuit

In the flyback converter, when the switch is opened, energy stored in magnetizing inductance is transferred to the secondary; however, the current in leakage inductance has nowhere to go, and if a path is not provided for that current, it creates a significantly large voltage across the switch that, depending on the leakage inductance, may damage the switch. Therefore, a RCD clamp (using a resistor, a capacitor and a diode) is often used to clamp the voltage across the switch. Figure 5-26 shows the schematic of a flyback

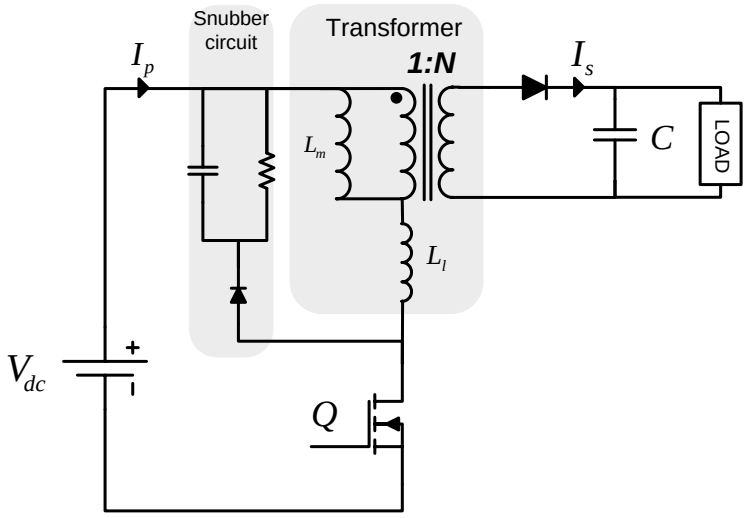


Figure 5-26. Flyback converter with a snubber circuit (RCD clamp)

converter with RCD clamp. Design of the flyback snubber, a necessary part of the circuit, was achieved according to the approach in [215] and the values for R and C are 5.5kΩ and 20nF respectively.

5.7.7. Results

The prototype was successfully tested for full power (200W) and load steps recommended by [204]. Figure 5-27 shows a photo of the setup, marking different sections. Figure 5-28 displays the waveforms for the output converter and ripple port in full load when the ripple port is operating. The traces in the figure are output current, output voltage, ripple port capacitor voltage, and input DC current from top to bottom respectively. The small box in the bottom left corner of the figure also reflects the RMS values for output current and voltage and the mean for the DC input current. Figure 5-29 shows the input current and its FFT when the ripple port is in the circuit. The traces are

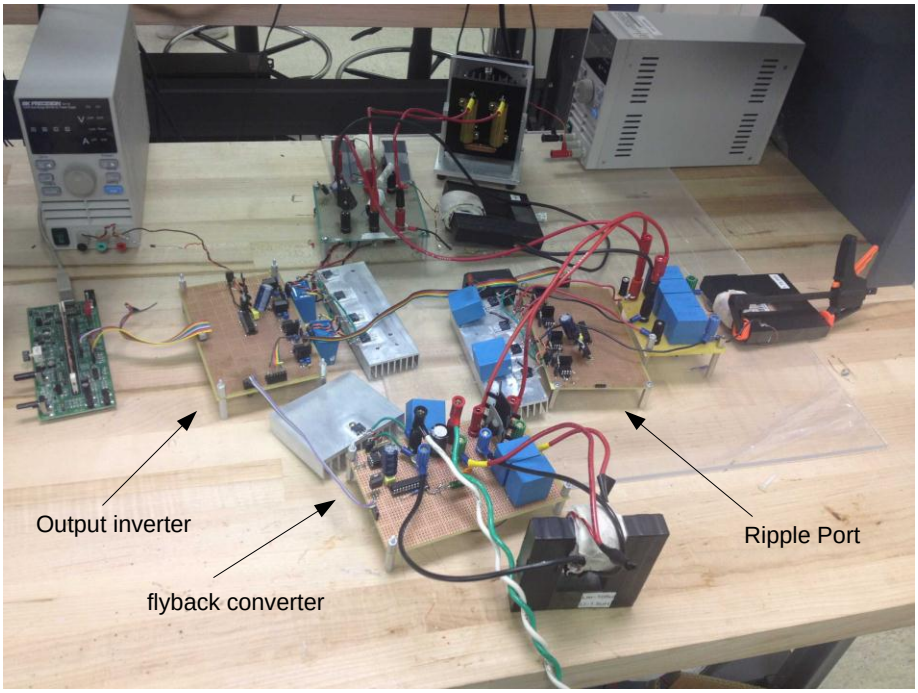


Figure 5-27. A photo of the experimental setup

FFT of the input current and the input current itself from top to bottom, respectively. Figure 5-28 shows a small value (less than 400mA) for peak-to-peak input current ripple.

Figure 5-30 shows the waveforms for the output inverter when the ripple port is not activated. The traces in the figure are output current, output voltage, ripple port capacitor voltage (which is zero since ripple port is not active), and input DC current from top to bottom respectively. Figure 5-31 shows the input current and its FFT when the ripple port is not activated. The traces are FFT of the input current and the input current itself from top to bottom, respectively. Figure 5-30 illustrates a peak-to-peak input current ripple of more than 2A. As rendered in Figure 5-31, without the ripple port, the second harmonic of the current is -2dB while in Figure 5-29, the second harmonic amplitude is

-40dB. Therefore, comparing Figure 5-29 to Figure 5-31provides evidence that the ripple port resulted in reduction of second harmonic current by -38dB.

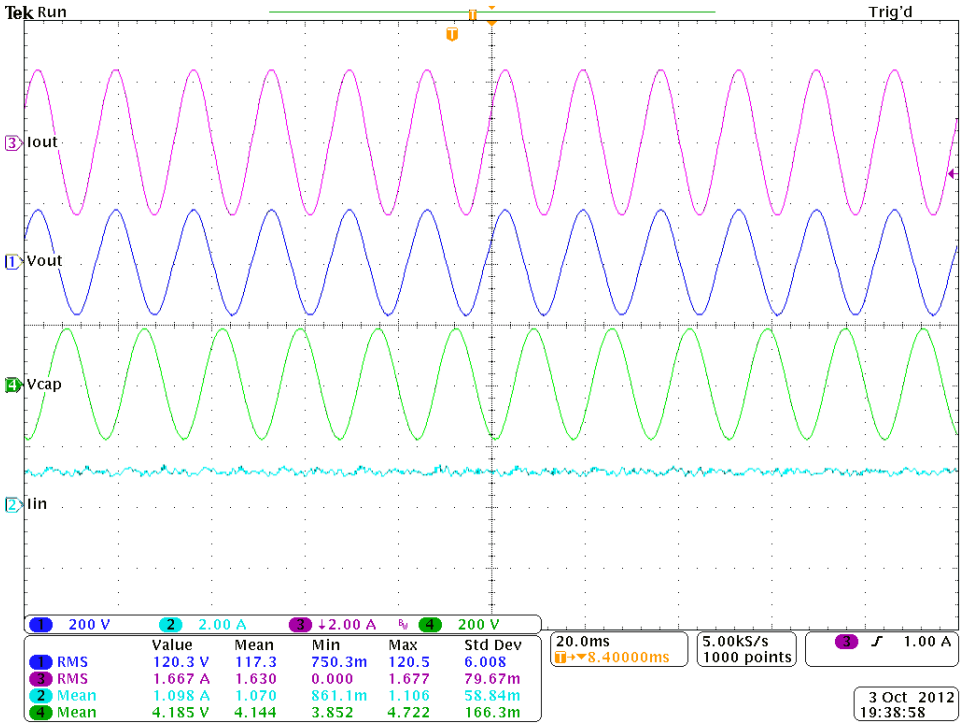


Figure 5-28. Voltages and currents of output inverter-ripple port converter in full load when ripple port is active (from top to bottom: Output current, output voltage, Voltage across ripple port capacitor and input current)

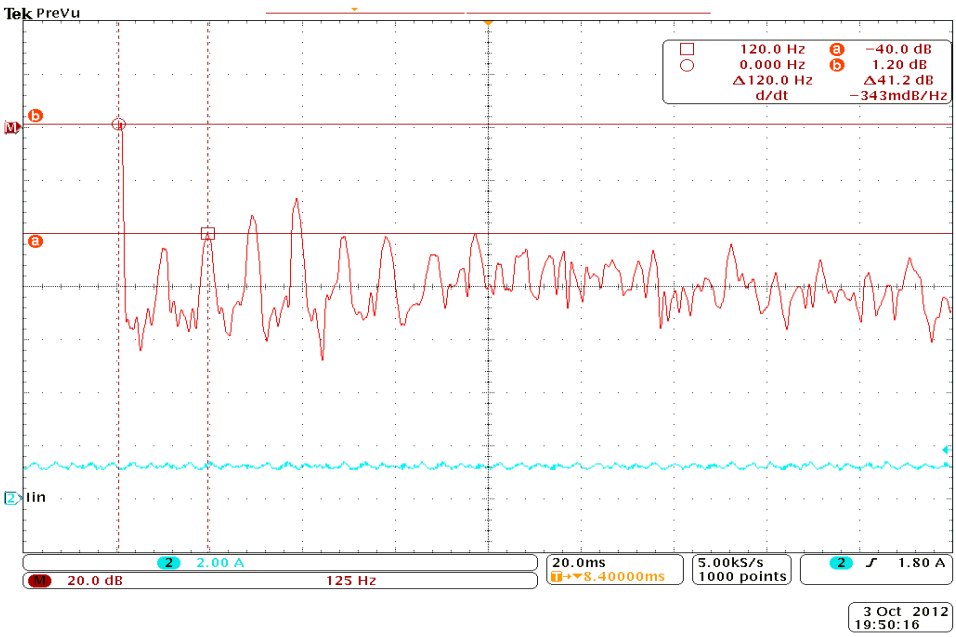


Figure 5-29. Input current and its FFT in full load (when ripple port is active)

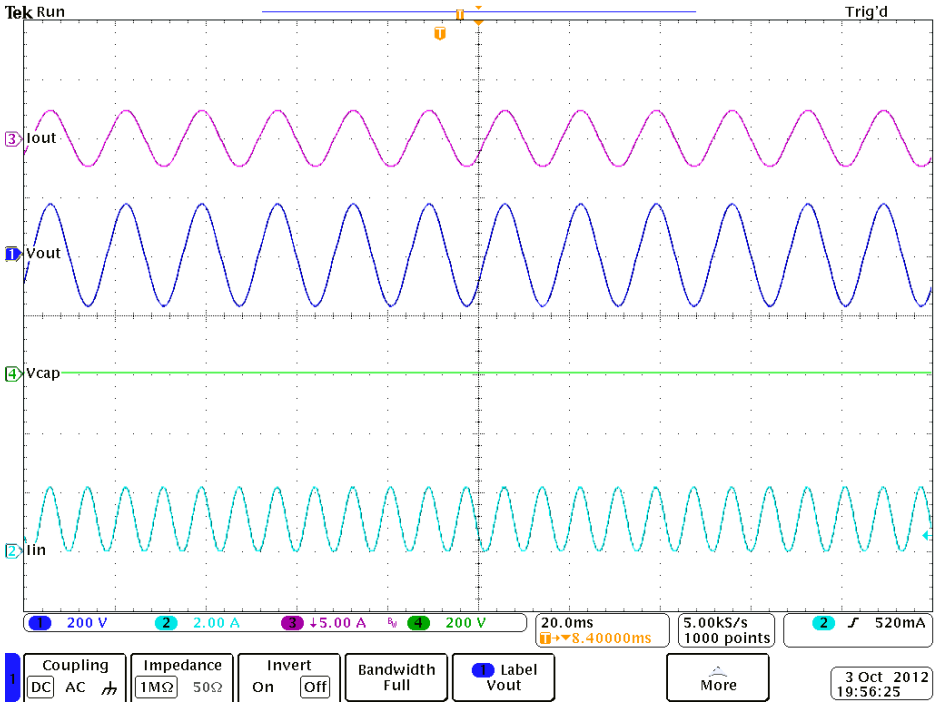


Figure 5-30. Voltages and currents of output inverter-ripple port in full load converter when ripple port is not active (from top to bottom: Output current, output voltage, Voltage across ripple port capacitor and input current)

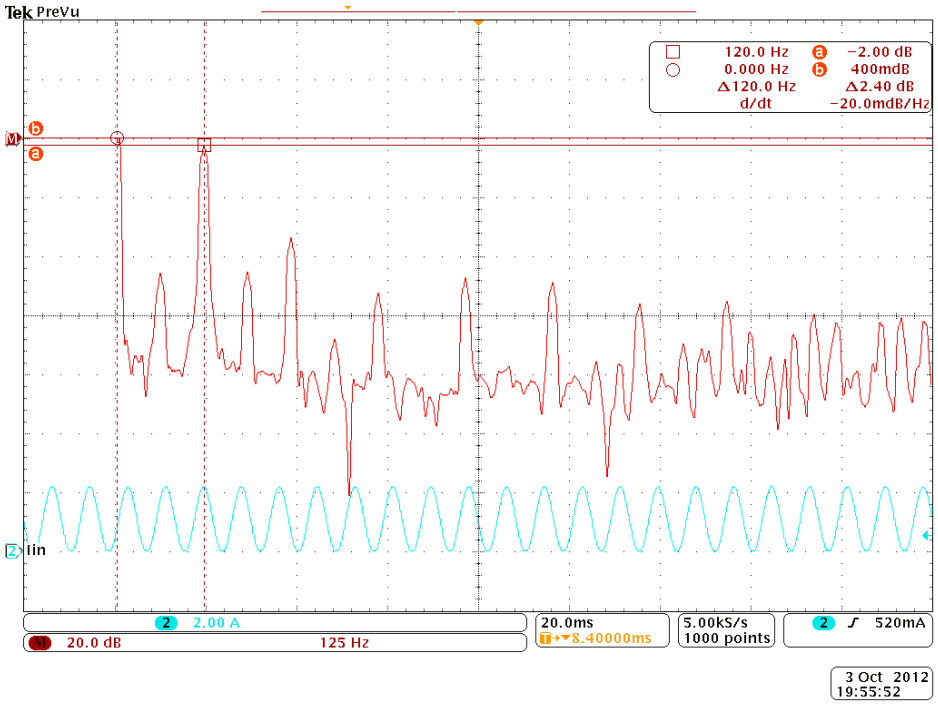


Figure 5-31. Input current and its FFT in full load whet ripple port is not active

Figure 5-32 shows the voltage and current waveforms of the flyback converter.

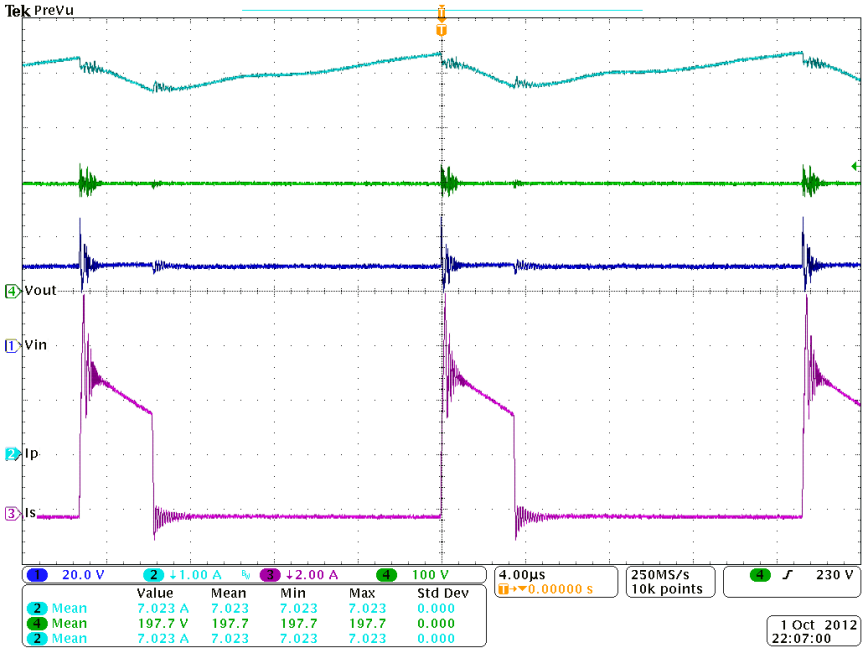


Figure 5-32. Voltage and currents of the flyback converter in full load (From top to bottom: Primary current, output voltage, input voltage and secondary current)

5.7.8. Power loss measurement

Power loss measurement was performed using a 4-channel Tektronix MSO 4034 oscilloscope equipped with two differential voltage probes and two current probes for the input and output voltages and currents.

Figure 5-33 and Figure 5-34 illustrate calculated vs. measured losses for flyback and output inverter plus ripple port converters, and Figure 5-35 and Figure 5-36 display the efficiency of the flyback and the output inverter plus ripple port, respectively. These figures reveal a reasonable conformity between measured and calculated losses in both stages. TCP0030 current probes have a 3% error [216], which is reflected in measuring both input and output current. Since losses are calculated from the equation below:

$$P_{loss} = V_{in} \cdot I_{in} - V_{out} \cdot I_{out} \tag{5-46}$$

The maximum error happens when I_{in} has +3% error and I_o has -3% error. On the other hand, the minimum error happens when I_{in} has -3% error and I_o has +3% error. The margins of error calculated from the mentioned approach are shown with dashed lines in Figure 5-33 and Figure 5-34. As illustrated, the measured losses are within the margins of error of the measurement setup.

5.7.9. Volume of the converter

Since magnetic components are designed thoroughly based on the core and winding dimension, it is expected that their volume is exactly the same as predicted. However, for the capacitors, this is not the case: The volume is different because commercial off-the-shelf products were deployed. The difference between estimated and actual volume for different capacitors was previously reported in Table 5-X.

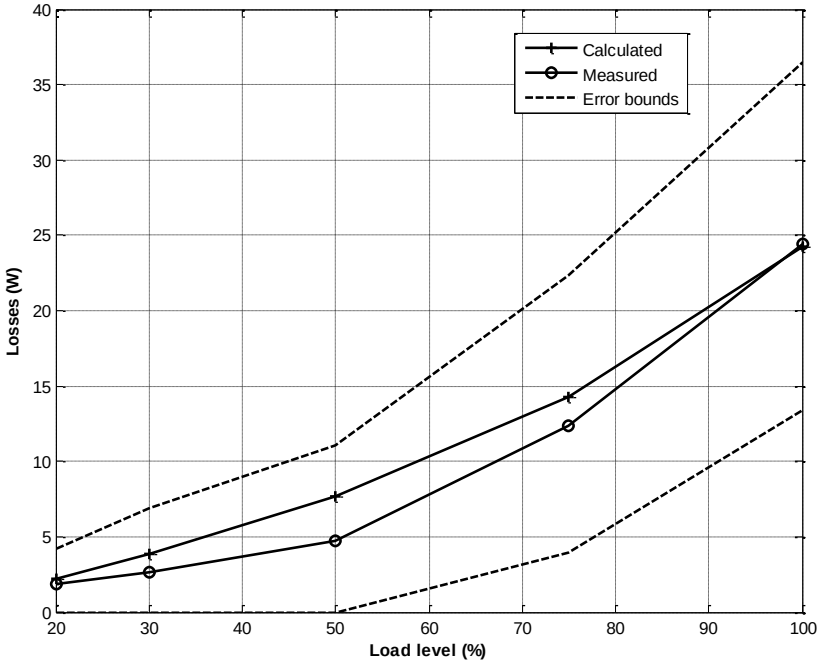


Figure 5-33. Calculated vs. measured losses for flyback converter

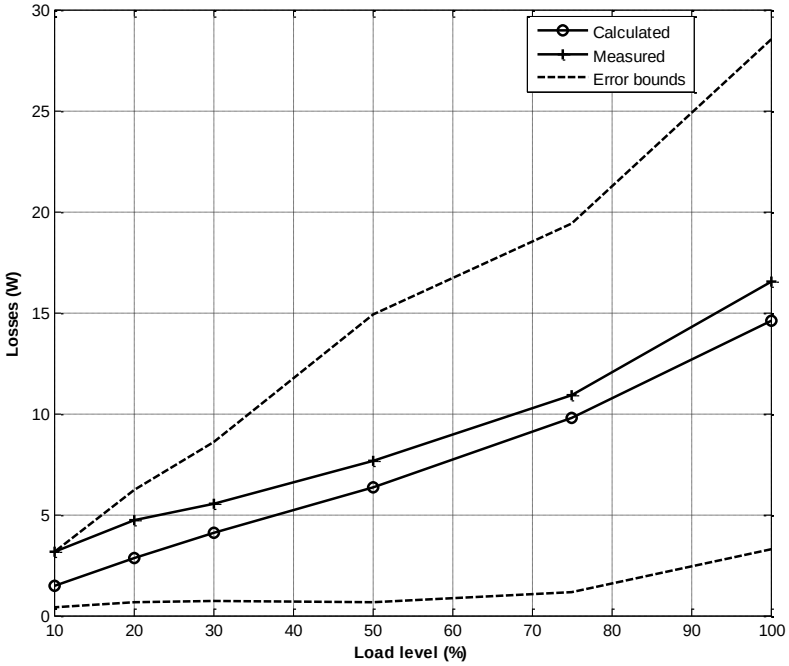


Figure 5-34. Calculated vs. measured losses for output inverter plus ripple port

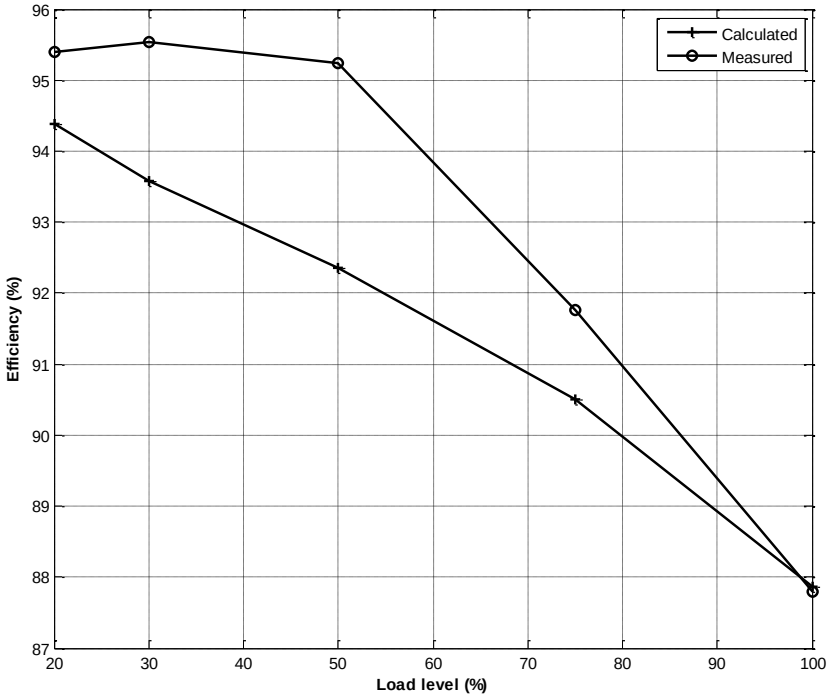


Figure 5-35. Calculated vs. measured efficiency for flyback converter

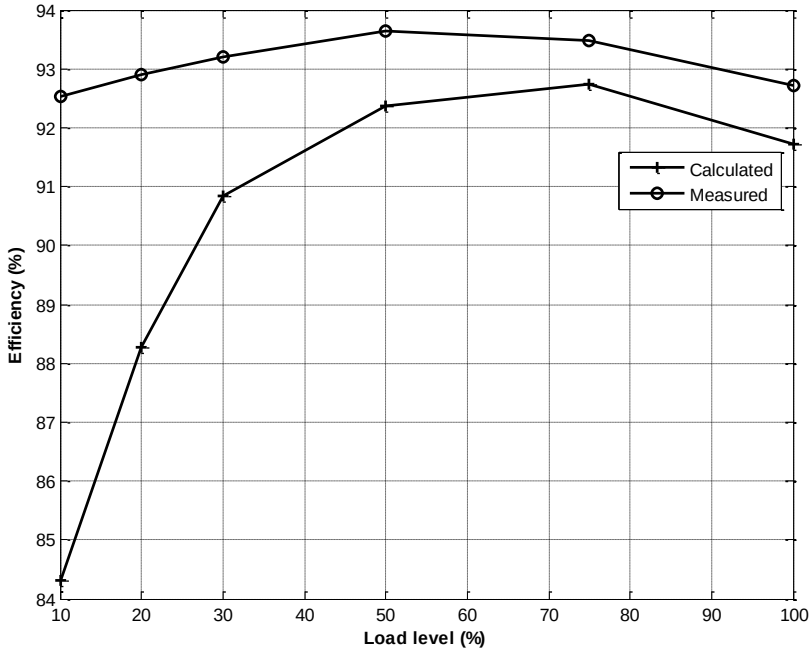


Figure 5-36. Calculated vs. measured efficiency for output inverter plus ripple port

For heat sinks, the volume was predicted from (4-13). The difference between the predicted and actual volume of the heat sink was reported in Table 5-XI. This difference can be justified as the selected heat sinks were not on the Pareto front of the heat sink profiles (Figure 4-8).

5.8. Conclusion

In this section a module-integrated inverter was optimized for efficiency, volume, and reliability, using the approach presented in section 4. First, concepts of PV inverters were introduced and a module-integrated converter was proposed to address the issues of power decoupling. Modeling and multi-objective optimization was performed and an experimental setup with parameters as close as possible to the output of the optimization program. The intention of having experimental results is to verify the modeling approach. The results reveal a close correlation between calculated and measured results.

6. OPTIMIZATION OF A PHOTOVOLTAIC CONVERTER BASED ON AN EFFICIENCY USAGE MODEL

Efficiency of a power electronic converter depends on a variety of factors including its load. Due to the load-dependency of efficiency and effects of other operating conditions, evaluating efficiency for a single point of a power electronic converter does not necessarily represent the true energy harvest of the converter. This phenomenon is more significant in power electronic converters deployed in photovoltaic applications, since these converters work in a broad spectrum of operating conditions depending on solar irradiance, temperature, wind speed, etc.[217] In this section, a PV converter is optimized based on a usage model, obtained from measurements on an actual PV module.

6.1. Efficiency and operating conditions

The fact that efficiency of power electronic converters depends on operating conditions has been understood for many years. Due to the nonlinear nature of losses in most of the components, the amount of energy loss changes with operating conditions, i.e., voltages and currents in the converter circuit. Some of the efficiency measurement guidelines have already accounted for this. For instance, 80 PLUS initiative has issued a test protocol that requires the power supply manufacturers to measure efficiency in different load levels [218]. Solar inverter manufacturers also usually provide an efficiency chart for different load levels. Figure 6-1 shows the efficiency of a Sunny Boy™ 4000-US inverter [219].

Efficiency dependency of a power electronic converter on operating conditions derives from the fact that energy losses in power electronic converters are usually nonlinear with respect to voltage and current. Moreover, in the presence of some fixed losses, such as gate drive losses, the efficiency becomes smaller in light load where these fixed losses dominate, since variable losses tends to scale with the current. Efficiency will rise as the load increases; however in higher loads where the load-dependent losses dominate, the efficiency drops again.

In photovoltaic converters, not only the amount of energy supplied by the PV module changes by solar irradiance and temperature, but also the input voltage and current of the PV converter is subject to change due to the maximum power point tracking. For example, the input current and voltage of a DC-DC converter connected to a PV module alters when the maximum power point of the module changes due to the

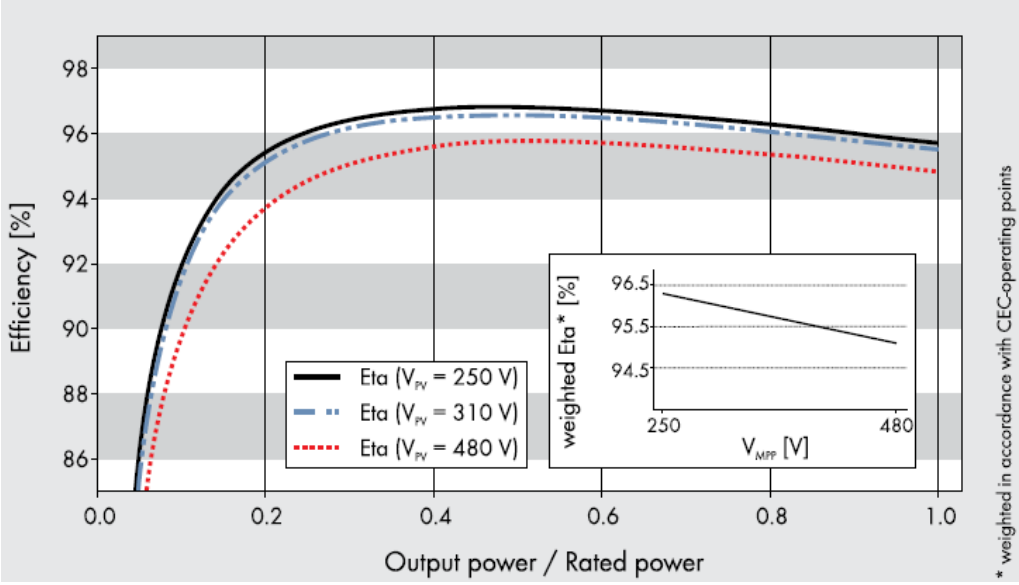


Figure 6-1. Efficiency plot of Sunny Boy 4000-US for various input voltages [219]

variation in solar irradiance and temperature. Therefore, an accurate efficiency evaluation of a PV converter should be performed considering not only the power delivered by the converter, but also voltages and current for which the converter operates. Due to the effects of operating conditions on efficiency, a converter, which is optimized for efficiency in a certain location, may not be optimal in another location. Considering the relatively high price of photovoltaic energy, it is important to extract as much energy as possible based on the place wherein the inverter is utilized. a truly optimized converter can be designed through use a descriptive language for the components and consideration of a proper usage model for the efficiency.

6.2. Usage models for PV converters

There are a few usage models in the literature for PV converters. California Energy Commission (CEC) has guidelines for measuring efficiency for grid-connected PV inverters [204]. In these guidelines, a weighted efficiency, a linear combination of efficiency in 6 different load levels, is employed, explained in section 5. The weighting factors under 'High Insolation' column are advised only by CEC while the weighting factors under 'Low Insolation' are also recommended by [220] and are used to calculate what is known as *European Efficiency*. CEC test guidelines also recommend three different DC voltage levels (V_{min}, V_{max} and V_{nom}) for the test procedure.

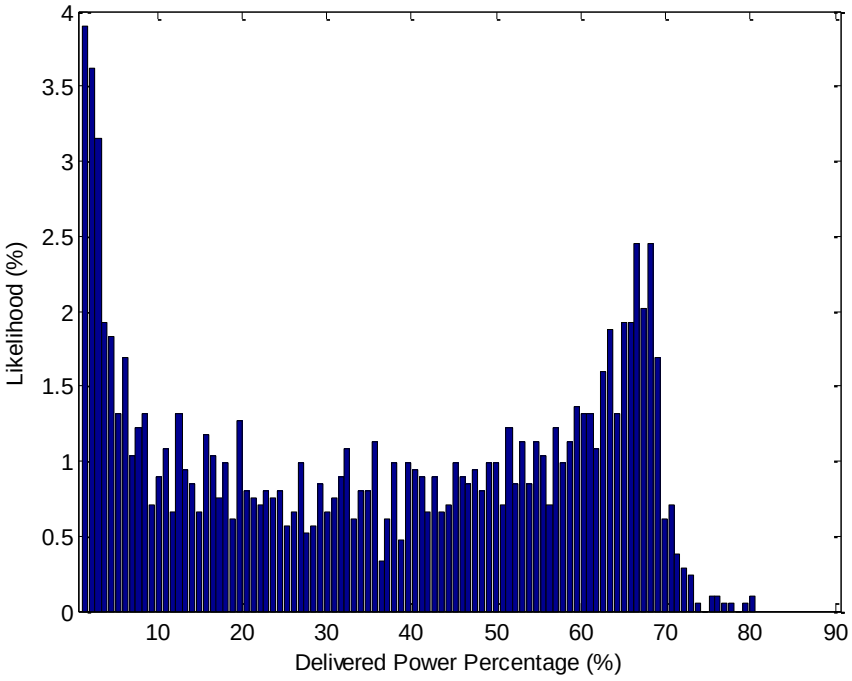
6.3. Problems with the PV converter usage models in design of PV converters

The current European and CEC usage models, while proving useful in providing testing procedures for PV inverters, might not be as useful in the design of PV converters. The drawbacks for these usage models are explained as follows.

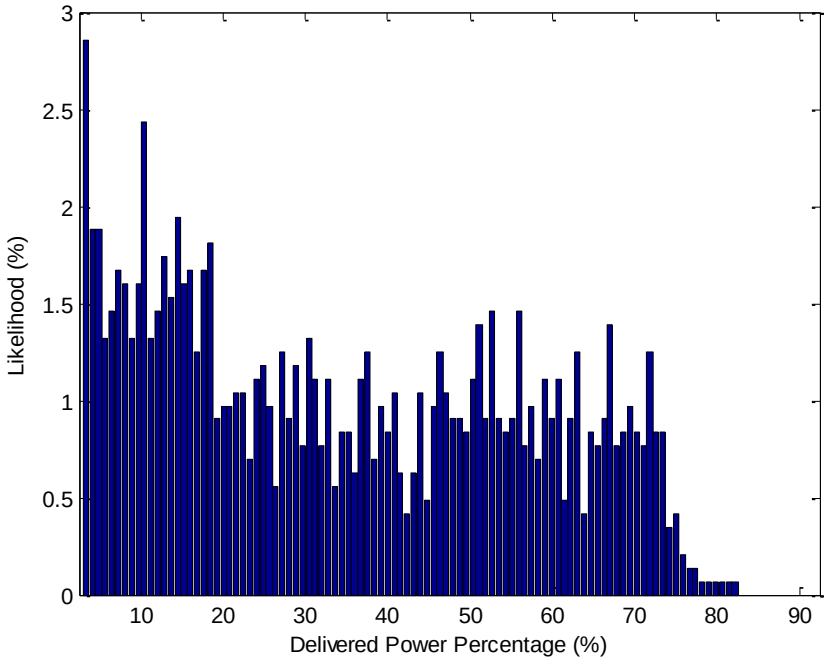
- The general weighting factors for high insolation and low insolation cases might not be accurate for all of the PV modules in different geographical locations. Alternatively, a model developed for California or Europe cannot be applied to places such as Middle Eastern countries or Texas where the climate is entirely different.

  Figure 6-2 illustrates the difference in distribution of the produced power for two PV modules, one in College Station, Texas, and the other in Ankara, Turkey, over the month of July. Figure 6-3 show the cumulative distribution function (CDF) of both PV modules vs. the CDF based on CEC weighting factors. Figure 6-4 illustrates the power distribution profile, binned only for CEC load levels, for both PV modules. All of the mentioned figures reveal differences in power distribution profiles with what suggested by CEC, which means that CEC weighted efficiency might be misleading.

- The efficiency testing procedure considers only three DC voltages for each inverter to be tested. However, averaging over these three DC voltages might lead to inaccurate efficiency since the likelihood of each DC voltage is not clear. In other words, instead of using actual usage data, potentially misleading inverter specifications are employed.



(a)



(b)

Figure 6-2. Comparison of power distribution profile for two PV systems (a) Ankara, Turkey and (b) College Station, Texas

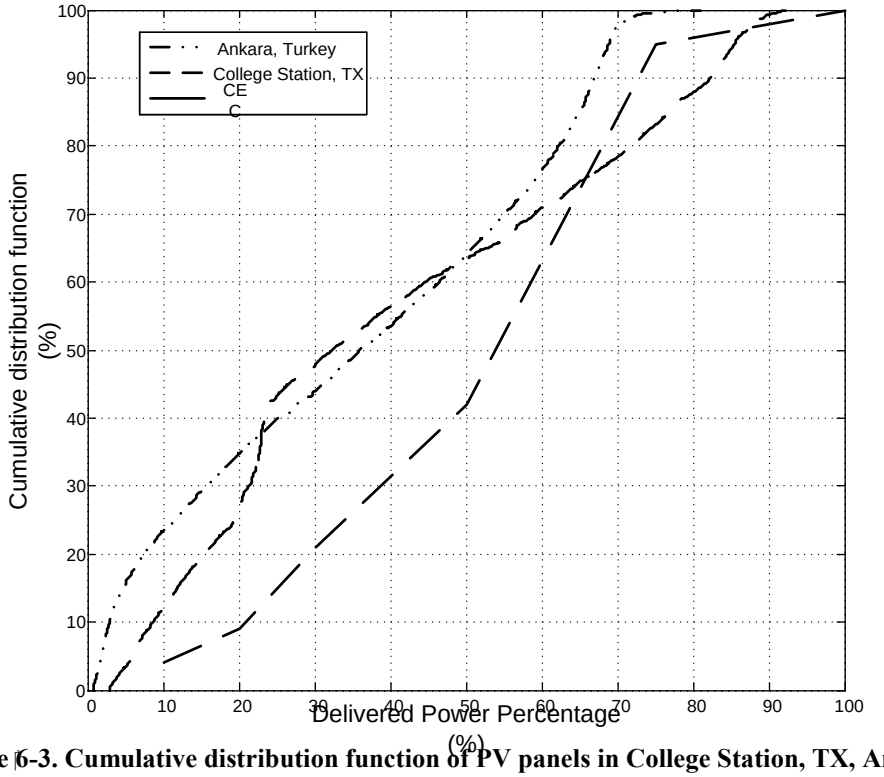


Figure 6-3. Cumulative distribution function of PV panels in College Station, TX, Ankara, Turkey, compared to what suggested by CEC

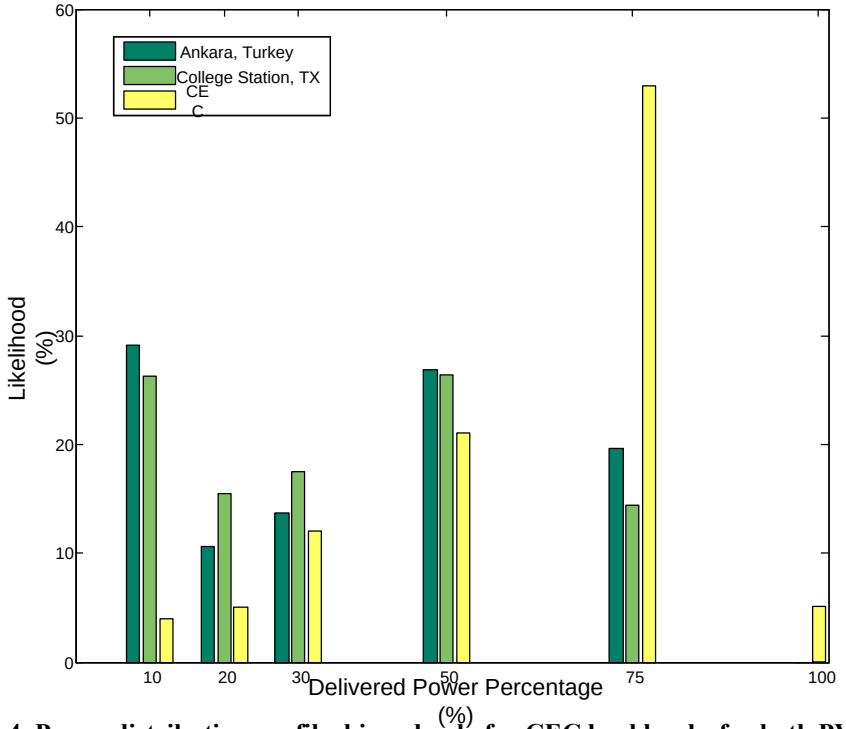


Figure 6-4. Power distribution profile, binned only for CEC load levels, for both PV modules

Alternatively, if the actual usage points are used to evaluate efficiency (or losses) and the obtained values are combined based on their likelihood, the resulted efficiency would prove more accurate. This dissertation utilizes this approach.

6.4. Multi-objective optimization of a PV converter based on usage model efficiency

As stated in the previous subsection, the efficiency of a PV converter depends not only on its load, but also on the characteristics of its input power, i.e., input voltage and current of the converter. Though PV modules may have a DC voltage from 0 to their V_{oc} (open circuit voltage), modern power electronic converters usually work at the maximum power point. In fact, modern PV converters extract 98%-100% of the available energy from the modules [221]. Therefore, throughout this chapter, it is assumed that the module always operates at the maximum power point.

In order to obtain a weighted efficiency based on a usage model, the following steps are taken:

1. Data is collected over a significant period of time. Only the data for the voltage and current for maximum power point need to be recorded. Figure 6-5 shows a scatter plot of maximum power point voltages and currents for a PV module installed in Ankara, Turkey recorded in 175 days.
2. The *v*-*i* space is then divided into several squares to find the distribution of the points. The number of *v*-*i* points within each square is divided by total number of data points and reported as probability of *v*-*i* maximum power point existing within that square. The squares with a small enough

likelihood (<1% for instance) are eliminated from the dataset and the remainder of the probabilities are normalized so that their summation is 100%. Figure 6-5 and Figure 6-6 show this process.

3. After the probability for each square is calculated, the center of mass of the points within each square is calculated. The center of mass will represent the corresponding square in the efficiency calculation. Table 6-I reveals upper and lower bounds for each square as well as the center of mass and probability.
4. The total efficiency of the converter is calculated using the probability of each of the squares from the equation below:

$$\eta_{weighted} = \sum_{n=1}^{N} P_n \eta_n, \text{N are regions where } P_k > 1\% \quad (6\text{-}1)$$

Table 6-I. The lower and upper bounds, the center of mass and probability of the squares in Figure 6-6

V_{lb}	V_{hb}	I_{lb}	I_{hb}	V_{avg}	I_{avg}	$P(\%)$
23.34	27.00	0.08	1.42	25.91	0.29	10.31
23.34	27.00	2.76	4.11	26.48	3.48	1.88
23.34	27.00	4.11	5.45	26.35	4.89	4.28
23.34	27.00	5.45	6.79	26.02	6.18	8.85
23.34	27.00	6.79	8.13	25.44	7.51	16.58
23.34	27.00	8.13	9.48	25.57	8.40	1.82
27.00	30.66	0.08	1.42	28.30	0.74	18.20
27.00	30.66	1.42	2.76	28.66	2.07	12.97
27.00	30.66	2.76	4.11	28.39	3.43	11.40
27.00	30.66	4.11	5.45	27.95	4.73	7.86
27.00	30.66	5.45	6.79	27.67	6.02	3.90
27.00	30.66	6.79	8.13	27.61	7.36	1.95
23.34	27.00	0.08	1.42	25.91	0.29	10.31

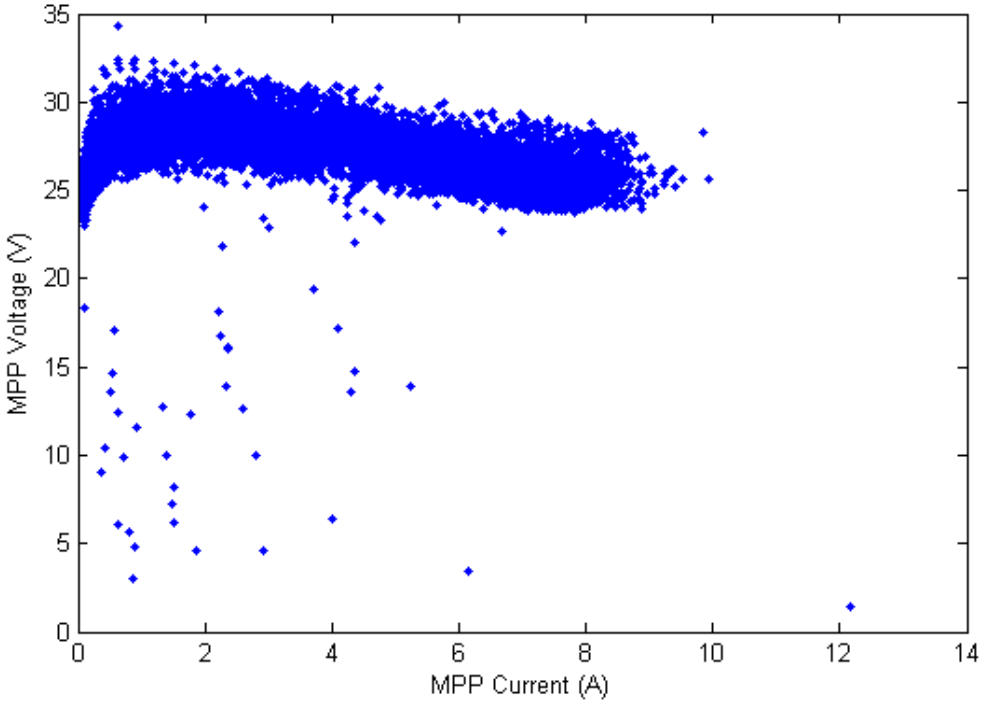


Figure 6-5. Scatter plot of MPP voltages and currents for a PV system in Ankara, Turkey

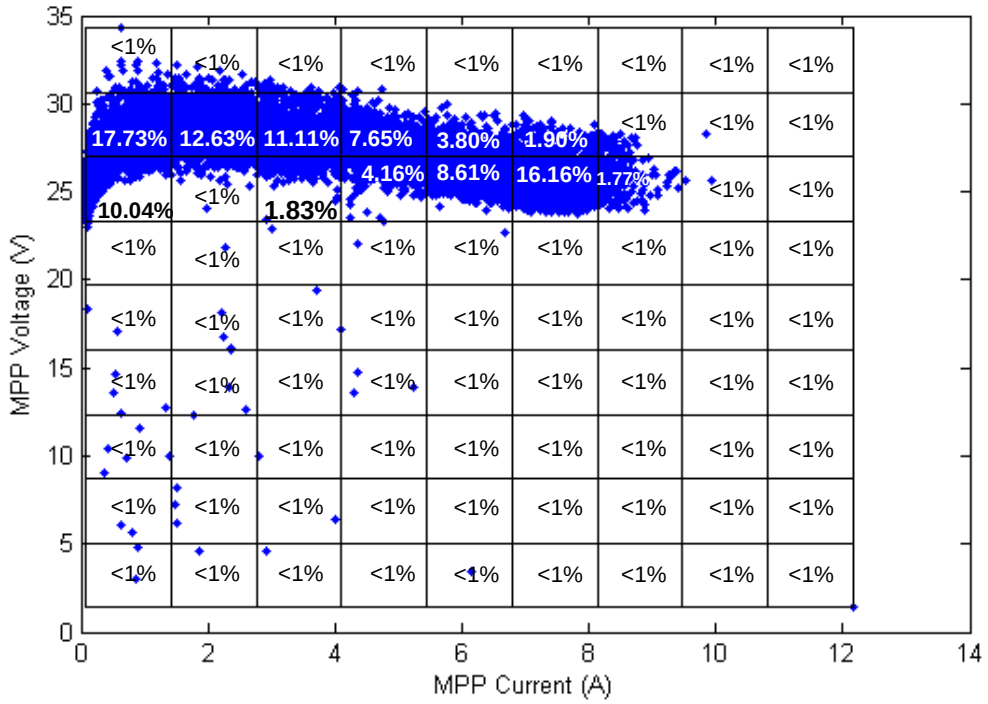


Figure 6-6. Finding the distribution of the points in the scatter plot

where η_i and P_i are efficiency and probability for ith square.

A flyback converter with a 200V output voltage was chosen to illustrate the differences between these two design approaches; one with the CEC weighted efficiency as the performance index and the other with the efficiency based on usage model as the performance index. Modeling and operation of a flyback converter was previously covered in section 5. and not repeated. The optimization objectives are the same as section 5. (efficiency, volume and failure rate); however, instead of using CEC weighting factors, voltages and currents with weighting factors of Table 6-I are employed. The multi-objective optimization problem was solved using the NSGA-II algorithm. A Pareto front of this optimization problem is demonstrated in Figure 6-7.

In order to reveal the difference between the proposed approach and CEC approach, weighted efficiency is calculated for the points on the Pareto front also using the CEC weighting factors. Figure 6-8 illustrate a comparison between these two weighted efficiencies for 50 arbitrary points on the Pareto front.

It is evident from Figure 6-8 that, though in many of the points on the Pareto front CEC weighted efficiency and usage model weighted efficiency are very close, in some of the points they can differ as much as 4.2%. Notably, in most of the cases CEC method shows a larger efficiency, which is misleading. Table 6-II offers statistical analysis performed on CEC weighted efficiency and usage model efficiency data for all of the 100 points on the Pareto front.

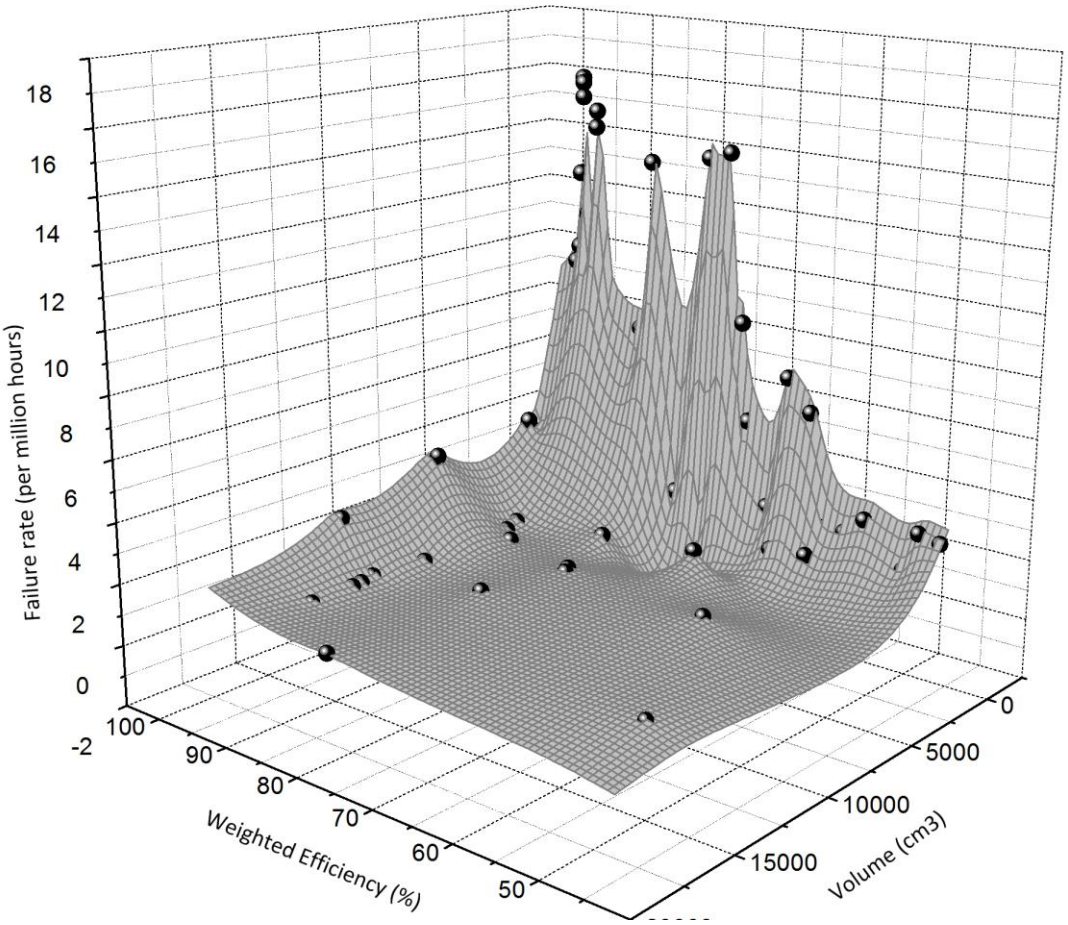


Figure 6-7. Pareto front for the flyback converter from two different angles with weighted efficiency calculated from the proposed usage model

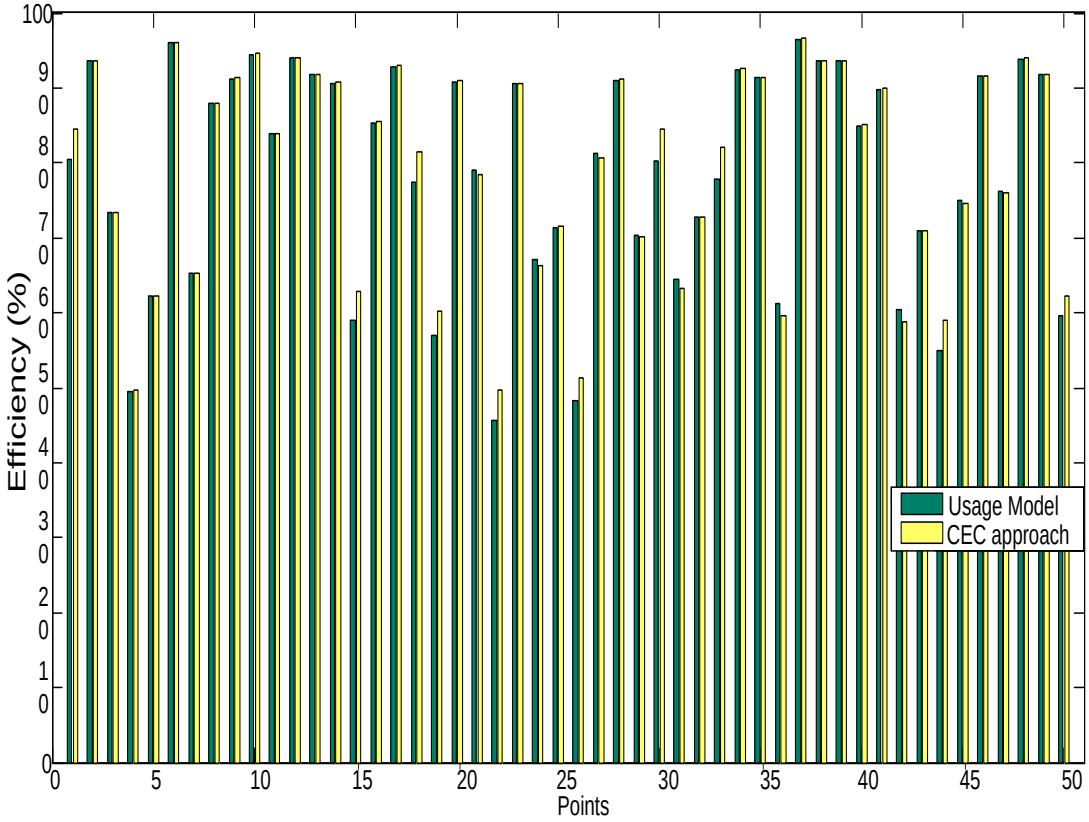


Figure 6-8. Comparison between weighted efficiency from proposed usage model and CEC approach

Table 6-II. Statistical analysis performed on CEC weighted efficiency and usage model efficiency data

Percentage of points in which CEC approach reports a larger efficiency	78%
Percentage of points in which CEC approach reports a smaller efficiency	22%
Mean value of $\eta_{CEC} - \eta_{usage}$	0.65%
Standard deviation of $\eta_{CEC} - \eta_{usage}$	1.65%

6.5. Conclusion

In this section, a usage model for the efficiency of photovoltaic converters was introduced. This method is based on the recording maximum power point voltage and current from an actual solar module and calculating the weighted efficiency based on the likelihood of a certain voltage-current combination. Due to the nature of the approach, the weighted efficiency calculated from this approach is a better performance index in comparison with that of California Energy Commission. Results reveal that two weighted efficiencies can be significantly different in some of the designs.

7. CONCLUSION AND FUTURE WORK

Optimization of power electronic converters has received considerable attention in the literature. However, most of the techniques have been constrained by considering only existing commercially-available components. While such an approach is suitable for the design of a commercial product, it proves inadequate; as this approach fails to consider which component attributes could offer a truly optimal design, even if these attributes are not yet available. This dissertation dealt with multi-objective design optimization of power electronic converters using a detailed mathematical approach, enabling the designer to go beyond the available commercial off-the-shelf components. Using this approach, one might find a truly optimal design point not limited by market availability.

In the first section, an overview of the optimization problem was explained; basic elements of an optimization problem were introduced; mathematical formulation of single-objective and multi-objective optimization was presented and challenges and specifics of optimization in power electronic converters were discussed.

In section 2, a literature review of the papers published in power electronics optimization was offered; an analysis of different approaches and methods to and for problem was presented. The remainder of section 2 dealt with a comprehensive review of modeling techniques for different components in power electronic converters. In section 3, a study of optimization algorithms employed in this work was presented and various algorithms used for single-objective or multi-objective optimization were introduced.

In section 4, Technology Characterization Methods and their utilization in power electronic converters were presented. Further, explained was how these methods can help to model tradeoffs in the optimization without the burden of intricate detail, especially in the case of power semiconductor devices and heat sinks. Models to address tradeoffs in IGBTs and heat sinks were derived and a single-phase inverter was then optimized for efficiency and volume based on those models.

In section 5, a module-integrated inverter was optimized for efficiency, volume, and reliability. The concept of double frequency power cancellation using an active filter, called a ripple port, was introduced; three candidate topologies for DC-DC stage of the MII were considered, and the multi-objective optimization was performed to elucidate performance limits of the candidate topologies as well as output inverter and ripple port. The flyback converter was selected based on the results, and an experimental design was constructed to verify the models.

In section 6, a usage model concept was presented to offer a better assessment of efficiency in various load levels in a PV converter. Recorded data of an actual PV module was used in order to derive the probability of combination of maximum power point voltages and currents. These data are then used for optimization of a flyback converter. Results reveal this approach offers a better assessment than that of California Energy Commission.

To pursue this work in the future, it is suggested that a more detailed analysis and modeling of semiconductor switches to identify other possibly overlooked tradeoffs is performed. Switches made from materials other than silicon (e.g. Silicon Carbide or

Gallium Nitride) can be studied, since they might have different characteristics than silicon-based devices. A multidisciplinary analysis can also be performed on heat sinks and other thermal management devices to obtain a more detailed model of such devices. Cost modeling of power electronic converters can be performed in more detail, taking into account economic considerations.

Although the proposed approach of this dissertation can be used for any type of power electronic converter regardless of the application, the focus this dissertation was mostly focused on power electronic converters for photovoltaic applications. In PV applications, especially in module-integrated inverters, efficiency, volume and reliability are of higher priority. In other power electronic applications, these priorities might not the same. For example, in a wearable power system, weight, reliability and cost of a converter might be the main design objectives while efficiency is of less importance. On the contrary, cost is of little priority in space applications while reliability of the converter is the most important design objective. Therefore, applying the method presented in this dissertation to converters from different applications might be useful in exploring performance limits of those converters.

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