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Limitations of the High-Low C-V Technique for MOS Interfaces With Large Time Constant Dispersion

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Limitations of the High–Low C–V Technique for MOS Interfaces With Large Time Constant Dispersion

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Abstract—We discuss the limitations of the high–low CV technique in evaluating the interface trap density (D_{IT}) in MOS samples with a large time constant dispersion, as occurs in silicon carbide (SiC). We show that the high–low technique can seriously underestimate D_{IT} for samples with large time constant dispersion, even if elevated temperatures are used to extend the range of validity.

Index Terms—AC conductance technique, interface states, interface traps, silicon carbide (SiC), wide-bandgap semiconductor.

I. INTRODUCTION

SILICON CARBIDE (SiC) MOS technology has made great progress since the first MOS devices were reported in the 1990s [1], but despite the progress, high interface trap density (D_{IT}) at the SiC/SiO$_2$ interface continues to be a concern for SiC MOSFETs. Even though silicon and SiC share the same native oxide, the properties of the interfaces are different. Yet, most techniques used to characterize the SiC MOS interface are borrowed directly from the silicon repertoire. The high–low CV method is one such technique.

Several reports in the literature stress the importance of interpreting SiC high–low data with care [2],[3]. D_{IT} data are valid only over the energy range where the high-frequency capacitance does not include any trap contribution and the low-frequency capacitance includes the contribution of all traps within a few kT of the Fermi level. The long response times of deep states make it hard to achieve true low-frequency conditions at room temperature when the Fermi level is deep in the bandgap. When the Fermi level is close to the majority carrier band, traps at the Fermi level respond quickly, making it hard to achieve true high-frequency conditions at those biases. Both high- and low-frequency conditions are simultaneously satisfied only over a narrow energy window, and the D_{IT} extracted from the high–low technique is only valid within this window.

In addition to the long response times of the interface states, the SiC/SiO$_2$ interface typically has a large time constant
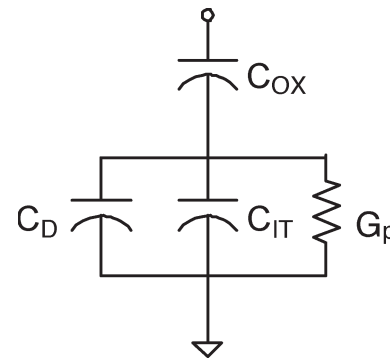
Fig. 1. Small-signal ac equivalent circuit of the MOS interface. C_{OX}, C_D, C_{IT}, and G_P are the oxide capacitance, depletion capacitance, interface trap capacitance, and interface trap conductance, respectively. C_{IT} and G_P are functions of frequency and surface potential, while C_D is a function of surface potential.

dispersion [2], [4], [5]. In silicon, the time constant dispersion is attributed to a variation in the density of fixed charges across the interface [6]. The time constant dispersion in SiC is typically two to three times larger than that in silicon, and its origin will be discussed in a separate paper [7]. In this paper, we focus on the effect of this time constant dispersion on data interpretation using the high–low CV technique.

II. THEORETICAL BACKGROUND

Fig. 1 shows the small-signal ac equivalent circuit of a MOS interface with interface states. In the high–low CV technique, the terminal capacitances C_{LF} and C_{HF} are measured as a function of gate voltage at two frequencies ω_{LF} and ω_{HF}. The interface state density D_{IT} at a given bias is calculated using [8], [9]

$$D_{\mathrm{IT}} = \frac{1}{q} \left(\frac{C_{\mathrm{ox}} C_{\mathrm{LF}}}{C_{\mathrm{ox}} - C_{\mathrm{LF}}} - \frac{C_{\mathrm{ox}} C_{\mathrm{HF}}}{C_{\mathrm{ox}} - C_{\mathrm{HF}}} \right). \qquad (1)$$

The surface-potential–gate-voltage (ϕ_s–V_G) relation of the sample is then used to correlate D_{IT} at a given bias with the position of the Fermi level in the bandgap at that bias. To calculate the ϕ_s–V_G relation of the sample, the high-frequency curve is treated as the ideal curve with no interface trap response, i.e., $C_{\mathrm{IT}}(\omega_{\mathrm{HF}}) = 0$. This makes the equivalent circuit at high frequency a series combination of C_{OX} and C_D. The surface potential is then calculated from the extracted C_D at each gate voltage. This method provides erroneous surface potential

data close to the majority band, since C_D has an interface trap capacitance contribution. This extra capacitance shifts the energy positioning of the D_{IT} points closer to the majority band. Another common technique uses the low-frequency CV curve to calculate the $\phi_s - V_G$ relation [10].

One of the most rigorous methods for evaluating the silicon MOS interface is the ac conductance technique [6]. This technique measures the equivalent parallel conductance G_p and capacitance $C_p = C_D + C_{IT}$ at several fixed gate voltages as a function of frequency. To model the frequency dependence of G_P and C_P, the theory assumes a random variation of fixed oxide charge across the interface, which produces a random variation in surface potential characterized by a Gaussian probability distribution. For a p-type sample biased in depletion, the interface state admittance can be written [6]

$$\frac{\langle Gp(\omega)\rangle}{\omega} = \frac{q}{2} \int_{-\infty}^{\infty} \frac{D_{IT}}{\omega\tau_p} \ln\left[1 + \omega^2\tau_p^2\right] P(u_s)du_s \qquad (2a)$$

$$\langle C_{IT}(\omega)\rangle = q \int_{-\infty}^{\infty} \frac{D_{IT}}{\omega\tau_p} \tan^{-1}(\omega\tau_p)P(u_s)du_s \qquad (2b)$$

where

$$\tau_p = \frac{1}{c_p N_A^-}\exp(u_s) \qquad (2c)$$

$$P(u_s) = \left(2\pi\sigma_{us}^2\right)^{-1/2}\exp\left[-\frac{(u_s - \langle u_s\rangle)^2}{2\sigma_{us}^2}\right]. \qquad (2d)$$

Here, u_s is the surface potential normalized to kT/q, τ_p is the time constant for hole capture by states at the Fermi level, c_p is the capture coefficient for holes, N_A^- is the ionized acceptor concentration, and σ_{us} is the standard deviation of surface potential or, in general, a measure of the time constant dispersion. The Gp/ω data obtained by measurement are fitted to (2) to extract the interface state parameters D_{IT} and c_p at the energy of the Fermi level at each gate voltage [4].

In 4H-SiC, the Gp/ω-versus-ω curves at each bias are broader than that in silicon [2], [4], [5], indicating a larger time constant dispersion. Fig. 2(a) shows the Gp/ω data (points) and the best fit using (2a) with a $\sigma_{us} = 4$. In contrast, for silicon σ_{us} is typically around two. The same broadening is also evident in the capacitance data [Fig. 2(b)]. As will be shown in the following, this broadening causes the high–low technique to underestimate D_{IT} in samples having a large time constant dispersion.

III. RESULTS AND DISCUSSION

To examine the accuracy of the high–low C–V technique in samples with large time constant dispersion, we assume a D_{IT}-versus-E distribution typical of 4H-SiC, and we simulate C–V curves at two frequencies: $\omega_{HF} = 2\pi \times 10^6$ rad/s (1 MHz) and $\omega_{LF} = \pi$ rad/s (0.5 Hz). The simulations are performed using the equivalent circuit in Fig. 1, with G_P and C_{IT} calculated using (2a)–(2d) and the C_D obtained using the "exact" MOS C–V theory [11]. We then regard these simulated curves as experimental data and perform the standard high–low analysis
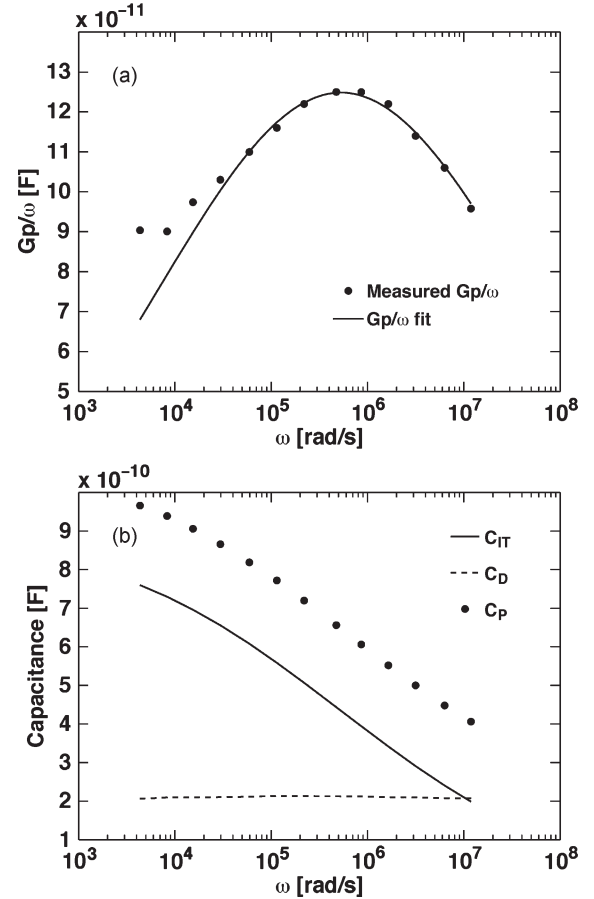

Fig. 2. (a) Measured Gp/ω curves on a 4H-SiC MOS capacitor biased in depletion. The sample was formed on a p-type SiC epilayer doped $\sim 2 \times 10^{16}$ cm^{-3} on a p$^+$ (0001) SiC substrate. The oxide was grown by pyrogenic oxidation at 1150 °C and annealed in nitric oxide at 1175 °C for 2 h. The sample was measured at room temperature in the dark using an HP 4284A LCR meter. The extracted parameters are $D_{IT} = 3.4 \times 10^{12}$ cm$^{-2} \cdot$ eV^{-1}, $\sigma_{us} = 4.0$, and $\tau_P = 4.9$ μs. The extracted parameters are used to generate a theoretical $C_{IT}(\omega)$ curve. (b) (Points) Measured $C_p(\omega)$, (solid line) calculated $C_{IT}(\omega)$, and (dashed line) extracted $C_D(\omega)$. The $C_{IT}(\omega)$ curve is generated using (2b) with the fitting parameters from the Gp/ω data. C_D is obtained by subtracting the calculated C_{IT} from the measured C_P. As expected, C_D is independent of frequency[4], confirming that all the interface trap capacitance has been removed.

to extract an "experimental" D_{IT} versus E. Finally, we compare the "experimental" D_{IT} to the D_{IT} originally assumed in the simulation. The simulations are performed for different σ_{US} values and at different temperatures to evaluate the range of accuracy of the high–low technique. For illustration purposes, these simulations are performed for p-type MOS capacitors, and the temperature dependence of the ionized acceptor concentration in 4H-SiC is explicitly included [11].

The dashed line in Fig. 3(a) shows the assumed D_{IT} distribution. This distribution is representative of the D_{IT} typically reported on p-type 4H-SiC [2], [4], [5]. The capture coefficient c_p is assumed constant throughout the bandgap. The results of simulated high–low measurements at room temperature are shown in Fig. 3(a). For a σ_{us} of four, typical of 4H-SiC [2], [3], [4], the extracted D_{IT} is underestimated at all energies. The reason for the error can be seen from Fig. 3(b), which shows the calculated $C_{IT}(\omega)$ at three bias points, labeled A, B, and C in Fig. 3(a). The extracted D_{IT} will only be accurate if C_{IT}/qD_{IT}
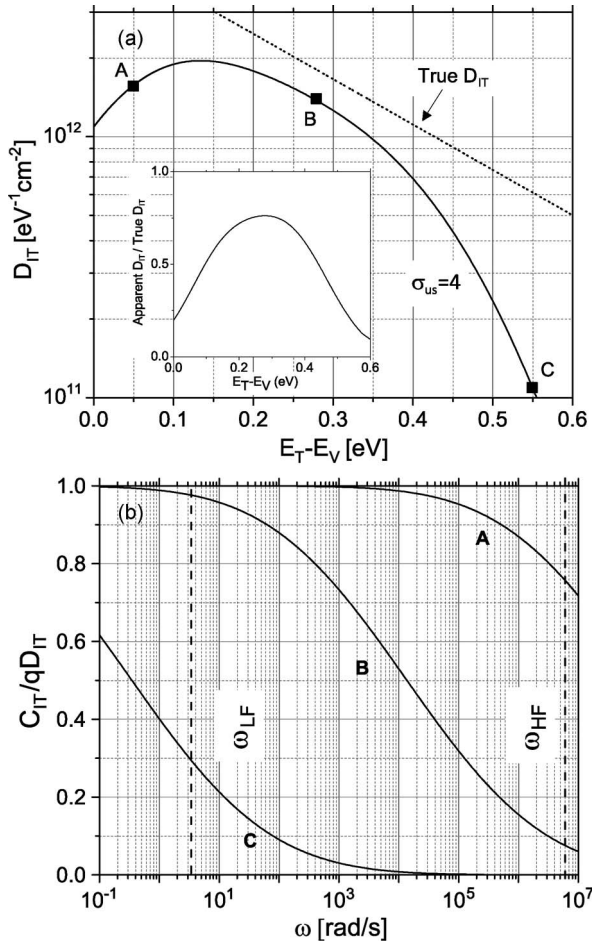
Fig. 3. (a) D_{IT} as a function of energy for the assumed D_{IT} distribution (dashed line) and deduced from the high–low technique for $\sigma_{us} = 4$. The relative accuracy of the deduced D_{IT} is shown in the inset. (b) C_{IT} versus frequency for $\sigma_{us} = 4$ at bias points A, B, and C in (a). The measured D_{IT} at points A, B, and C is proportional to the difference between the C_{IT} values at the low and high frequencies [the dashed lines in (b)] and is accurate only when the low-frequency normalized C_{IT} is equal to unity and the high-frequency normalized C_{IT} is zero. For samples with large time constant dispersion, these conditions may not be met for any bias point, as illustrated in part (b). All curves were simulated using a $c_P = 1 \times 10^{-11}$ cm^3/s, which is representative of many 4H-SiC samples [2], [4], [5].

is simultaneously unity at the low measurement frequency ω_{LF} and zero at the high measurement frequency ω_{HF}. This condition is clearly not met for bias points A or C. This is due to the large time constant dispersion for interface state response, which causes a very gradual transition from low- to high-frequency behavior. Using fixed measurement frequencies of $\omega_{HF} = 2\pi \times 10^6$ rad/s and $\omega_{LF} = \pi$ rad/s, there is only a narrow range of bias for which the high- and low-frequency requirements can be satisfied simultaneously.

High–low measurements on SiC are often performed at multiple temperatures to extend the energy range over which D_{IT} can be measured. Fig. 4 shows the simulated high–low measurements on a sample with $\sigma_{us} = 4$ and the D_{IT} distribution in Fig. 3(a), performed at several temperatures. The plotted points illustrate the way results are often reported in the literature, and an abrupt jump in D_{IT} is observed at the point where measurement temperature is changed. Measurements at a single temperature provide valid data over only a limited
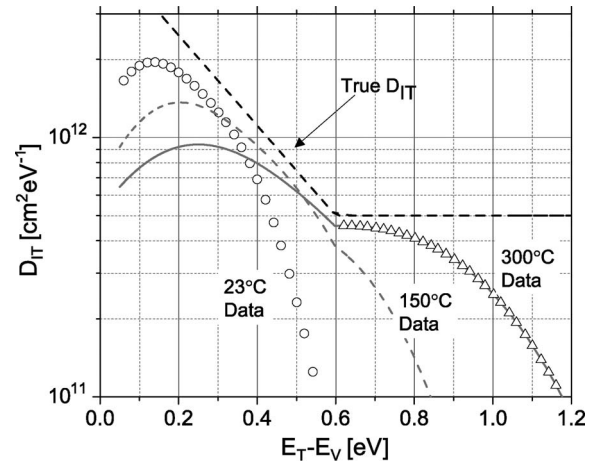

Fig. 4. Extracted D_{IT} versus energy for a $\sigma_{us} = 4$ sample at different temperatures. The points illustrate how data are often reported in the literature. To obtain a reliable estimate of D_{IT}, it is useful to make overlapping measurements at several temperatures and accept only the highest D_{IT} obtained at any given energy.
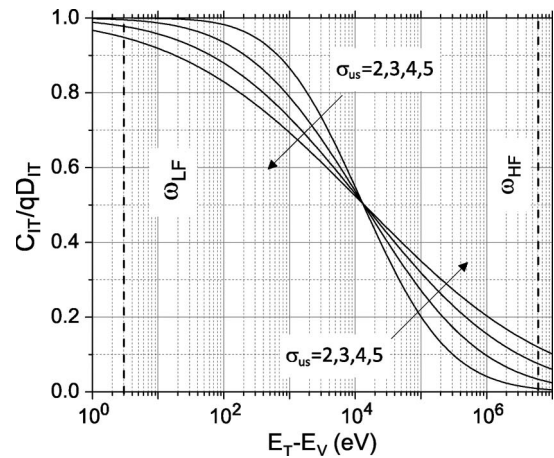

Fig. 5. Normalized C_{IT} as a function of frequency for different time constant dispersions. As σ_{us} increases, the curves become broader; more traps begin to respond at the high frequency ($2\pi \times 10^6$ rad/s), and fewer respond at the low frequency (π rad/s). This leads to an underestimation of D_{IT}.

energy range, but a fairly accurate picture can be obtained by combining data taken at several temperatures and accepting only the highest D_{IT} at any given energy. This is shown in Fig. 4 by extending the 300 °C data to lower energies (solid line) and adding additional data at 150 °C (dashed line).

Fig. 5 shows the C_{IT} versus ω for several values of σ_{US}. As σ_{US} increases, more states respond at the "high" frequency, and fewer states respond at the "low" frequency, increasing the error in D_{IT}. Note that the bias point in Fig. 5 is close to optimum, in that the capacitance transition occurs midway between ω_{HF} and ω_{LF}. As bias is varied, the capacitance transition moves to higher or lower frequencies, increasing the error, as illustrated in Fig. 3(b). When the high–low technique is performed at elevated temperatures, the range over which the high–low data are valid shifts toward midgap, as can be seen in Fig. 4. This is because the higher thermal energy reduces interface state response times.

In the high–low technique, there is no direct method to determine the range over which the data are valid, and this

is a major weakness of the technique. The ac conductance technique avoids this problem, since data are obtained over a range of frequencies, rather than at two discrete frequencies, and the entire $G_P(\omega)$ and $C_{IT}(\omega)$ curves are revealed. D_{IT} data are extracted only at those biases for which a clear conductance peak is observed versus frequency. This restricts the range of energies over which conductance data can be obtained. The conductance technique is *not inaccurate* outside this range, it simply provides *no data* for biases that are too close to the majority carrier band or too deep in the bandgap. (The energy range can be shifted closer to the band edge by measuring at low temperatures or deeper into the bandgap by measuring at high temperatures.) Unlike the high–low technique, the conductance technique makes no *a priori* assumptions regarding frequency response of the states. A comparison of the high–low and conductance techniques for the analysis of SiC MOS devices is given in [2].

Determination of surface potential is an important part of the data reduction process, since surface potential is used to calculate the bandgap energy of the interface states opposite the Fermi level. In the conductance technique, one can subtract the interface state capacitance $C_{IT}(\omega)$ from the measured parallel capacitance $C_P(\omega)$, leaving a frequency-independent depletion capacitance C_D, as illustrated in Fig. 2(b). This depletion capacitance is then used to determine the surface potential. In the high–low technique, C_D is inferred from the high-frequency capacitance under the assumption that none of the interface states can follow the signal. This assumption fails when the Fermi level is near the band edge. Consequently, C_D is overestimated, and the surface potential is thought to be closer to accumulation than it actually is. Like the D_{IT} errors discussed previously, there is no direct way to determine whether the energy position of states near the band edges is being determined correctly.

In this paper, we have considered a p-type sample, but our results apply equally to n-type samples. Our conclusions are relevant for any MOS interface with large time constant dispersion, such as MIS capacitors on III–V semiconductors.

IV. CONCLUSION

The high–low technique must be used with caution on samples with large time constant dispersion. This is particularly true of MOS interfaces on SiC and quite likely true for interfaces on III–V semiconductors as well. It is not possible to determine directly from the high–low data over what energy range the data are valid, compounding the problem. The ac conductance technique measures admittance over a range of frequencies and makes no *a priori* assumptions about the frequency response of the states. For this reason, it is the preferred technique in cases where large time constant dispersion is present.

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