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Impact of Strain on S/D tunneling in FinFETs: a MS-EMC study

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***Abstract*— As device dimensions are scaled down, the use of strained channels as performance booster becomes of special relevance. Moreover, the inclusion of quantum effects in the transport direction is imperative to predict the performance of future transistors. In particular, Source-to-Drain tunneling (S/D tunneling) is presented as a scaling limit in sub-10nm nodes. In this work, a Multi-Subband Ensemble Monte Carlo (MS-EMC) study of the impact of S/D tunneling in relaxed and biaxially strained channel FinFETs is presented.**

Keywords*— *Multi-Subband Ensemble Monte Carlo; direct Source-to-Drain tunneling; biaxial strain; FinFET

I. Introduction

The scaling down of conventional planar CMOS transistors presents challenges following the trend stipulated by Moore's Law. It is necessary to introduce new transistor architectures that overcome short channel effects [1-2]. FinFETs have been adopted with the potential for extending scaling virtually until the end of the roadmap. Simultaneously, strain engineering is one of the commonly used methods for performance enhancement. Moreover, this technology is considered by the International Roadmaps for Devices and Systems (IRDS) as one of the key factors to improve the device performance in sub-100nm nodes [3]. Accordingly, the study of strained FinFETs for contemporary and future CMOS technology generation remains of continuing interest.

In the corresponding simulation technologies, quantum effects in the transport direction start to play an important role when the channel length is reduced to few nanometers. Therefore, it becomes mandatory to implement the Source-to-Drain tunneling (S/D tunneling) mechanism in sub-10nm nodes [4-5] because it degrades the subthreshold behavior of future transistors. When an electron with total energy lower than the S/D barrier reaches it, there is a possibility of tunneling through the barrier instead of rebounding as classical dynamics predicts. Accordingly, the potential barrier shape and height are modified due to the presence of charge located under it. This phenomenon leads to an increase in the subthreshold current and consequently, to a reduction of the threshold voltage (V_{TH}).

The aim of this work is to perform a comprehensive study of the impact of S/D tunneling on strained FinFETs by means of Multi-Subband Ensemble Monte Carlo (MS-EMC) simulations. For this purpose, a detailed discussion of the S/D tunneling model included in our MS-EMC tool is provided, together with the details of the strain implementation, in Section II. The main findings are reported in Section III including a meticulous analysis of the electron distribution change in the subbands due to the strained channels. Finally, the main conclusions are summarized in Section IV.

II. Methodology

The simulation framework is based on a MS-EMC code which has been widely tested in different scenarios [6-7]. The simulator solves the Schrödinger equation in the confinement direction and the Boltzmann Transport Equation (BTE) in the transport plane (Fig. 1). The system is coupled by solving the Poisson equation in the whole 2D simulation domain. On the one side, arbitrary strain conditions can be considered locally in this code by tailoring the energy minima of each valley in order to reproduce uniaxial, biaxial, a combination of both, or non-uniform analytical strain mapping [8]. On the other side, the additional modules needed for taking into account the quantum effects are included as separated transport mechanisms without increasing the computational time, which is a noteworthy advantage of our code in comparison to purely quantum transport simulations. In addition to the S/D tunneling [9], others tunneling mechanisms such as band-to-band tunneling (BTBT) [10] and gate leakage mechanisms (GLM) [11] have been also incorporated in this MS-EMC tool. They can be activated or not depending on the simulation scenario, making possible their individual or simultaneous simulation [12].

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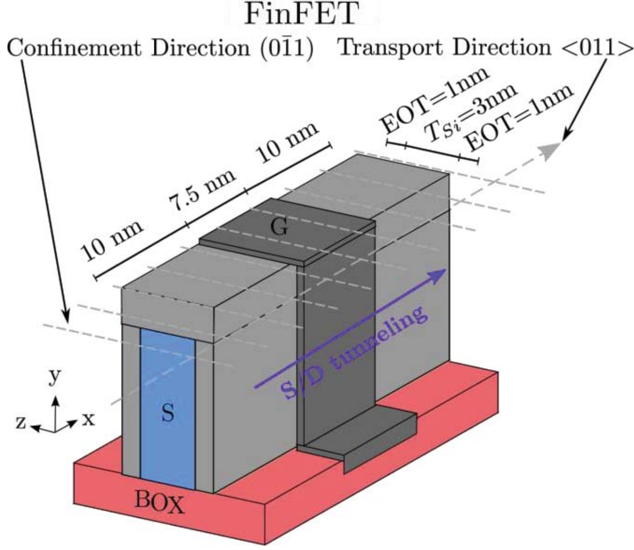

Fig. 1. FinFET structure herein analyzed with L_G=7.5nm and T_{Si}=3nm. 1D Schrödinger equation is solved for each grid point in the transport direction and BTE is solved by the MC method in the transport plane.

A. Description of the strain implementation

The MS-EMC simulator includes the possibility of taking into account strain effects on electrostatics and carrier transport. Our implementation follows the work presented in [13] where the valley splitting energy is considered. In this way, the changes in the nonparabolicity and the effective masses are neglected as second order effects. The numerical tool is can include molar fraction dependent biaxial strain induced by SiGe substrates, uniaxial strain (tensile and compressive) induced by technological stressors and a combination of both. As anticipated before, in order to reproduce real strain distributions in state-of-the-art devices, arbitrary strain conditions can be locally considered tailoring the energy minima of each valley obtained from both experimental and TCAD strain mapping results [8].

B. Description of the S/D tunneling model

S/D tunneling [9] is implemented as a stochastic mechanism evaluated for each superparticle at the end of the Monte Carlo free flight. If S/D tunneling is considered, an electron near the potential barrier with lower energy will be either reflected or transmitted through it. The WKB approximation [14] is used in order to estimate the tunneling probability. It mainly depends on the position of the carrier in the device, the transport effective mass, and the subband profile that determines the shape of the tunneling barrier:

$$T_{dt}(E) = exp\left\{-\frac{2}{\hbar}\int_a^b \sqrt{2m^* \ |E_{barrier}(x) - E|}\, dx\right\} \quad (1)$$

where a and b are the starting and ending points, E and m^* are the total energy in the transport plane and the electron transport effective mass, respectively. $E_{barrier}(x)$ represents the energy profile of the corresponding subband in the tunneling path. A rejection technique is used to determine whether the particle will tunnel or not. A uniform distributed random number r_{dt} is generated and compared to T_{dt}. If $r_{dt} > T_{dt}$, the electron will be reflected. Otherwise the electron will go through the barrier.

The last step in this model is to describe the tunneling path. A realistic process, in which the particles fly through the potential barrier during a certain period of time, has been considered because it has demonstrated a good description of the degradation in the subthreshold region similar to Non-Equilibrium Green's Function (NEGF) calculations [15]. The tunneling particle's motion inside the barrier obeys Newton's mechanics considering an inverted potential profile and ballistic transport.

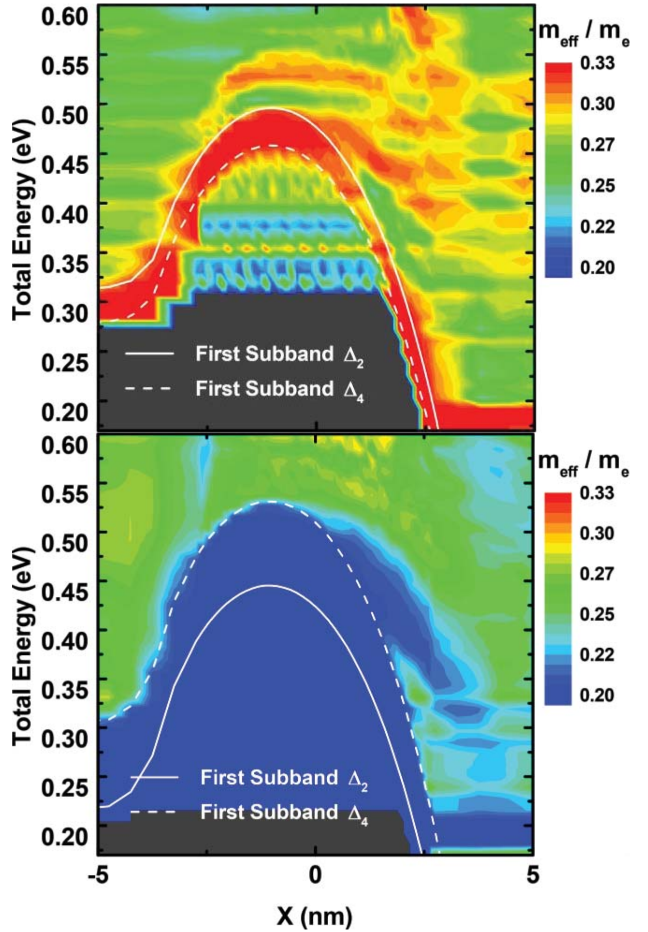

Fig. 2. Average effective mass of the electron distribution with the lower energy subband of the valley Δ_2 (solid) and of the valley Δ_4 (dashed) as a function of the total energy in the 7.5nm FinFET device including S/D tunneling for a simulation without strain (top) and with biaxial strain (bottom). V_{GS} = 0.1V and V_{DS} = 0.5V.

III. RESULTS AND DICUSSION

For the study of the impact of S/D tunneling in strained channels, a FinFET structure with biaxially strained channel (sSOI with a $Si_{0.8}Ge_{0.2}$ virtual substrate) has been chosen as shown in Fig. 1. In this study, the gate length ranges from L_G=5nm to L_G=20nm and the confinement and transport directions correspond to the (0-11) and <011>, respectively. The rest of the parameters remains unchanged: the Si thickness is 3nm, the Equivalent Oxide Thickness (EOT) of the gate insulator is 1nm, and the metal work function is 4.385eV. Abrupt doping profiles in the junctions between S/D and channel have been considered with $N_D=10^{20}cm^{-3}$.

Fig. 2 depicts the average transport effective mass distribution as a function of the total energy for the relaxed (top) and strained (bottom) devices including S/D tunneling for the 7.5nm gate length transistor. The average effective mass has been calculated as a function of the total population in each valley. The change in the fundamental subband from Δ_4 to Δ_2 leads to a decrease in the transport effective mass and, therefore, an enhancement of the tunneling probability even though the barrier is higher.

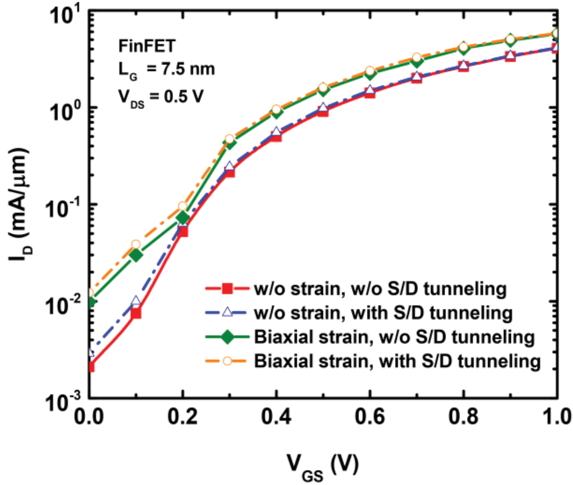

Fig. 3. I_D *vs*. V_{GS} in the 7.5nm FinFET device at V_{DS}=0.5V considering four different combinations: w/o strain and w/o S/D tunneling; w/o strain and with S/D tunneling; with biaxial strain and w/o S/D tunneling; and including both biaxial strain and S/D tunneling model.

As expected, the drain current increases in both the relaxed and strained cases (Fig. 3). However, the inclusion of S/D tunneling degrades the FinFET performance in the subthreshold region, whereas there is no noticeable impact at high V_G since thermionic emission is the dominant transport mechanism for that range of voltages.

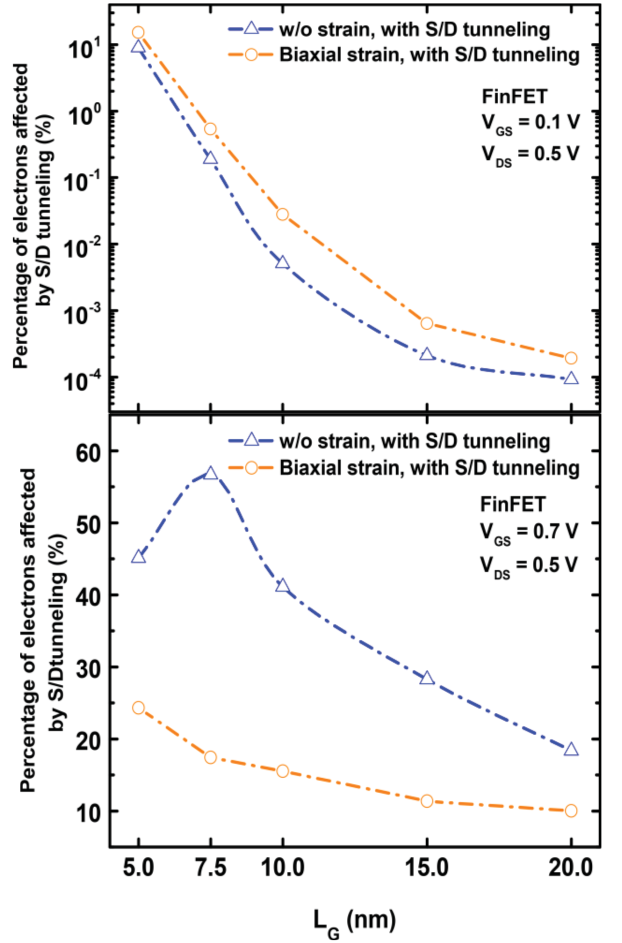

Fig. 4. Percentage of electrons affected by S/D tunneling as a function of L_G in the FinFET device at V_{DS}=0.5V for V_{GS} = 0.1V (top) and V_{GS} = 0.7V (bottom) obtained from a simulation w/o strain (triangles) and another with biaxial strain (circles).

The impact of strain in the tunneling process is illustrated in Fig. 4, where the percentage of electrons near the barrier affected by S/D tunneling is shown for different conditions. At low V_G, the smaller effective mass in the case of the strained devices enhances the tunneling process (Fig. 4 (top)). This is associated with the fact that both devices present similar barrier heights at low V_G and so the effective mass plays the main role in this case. As the gate voltage is increased, the situation is reversed: the relaxed device with smaller barrier has a higher percentage of electrons affected by S/D tunneling. These trends remain for different gate lengths as shown in Fig. 4. The difference in the subthreshold regime is reduced as the channel length is shortened. The disparities are more pronounced in strong inversion for all channel lengths where all relaxed devices exhibit more S/D tunneling.

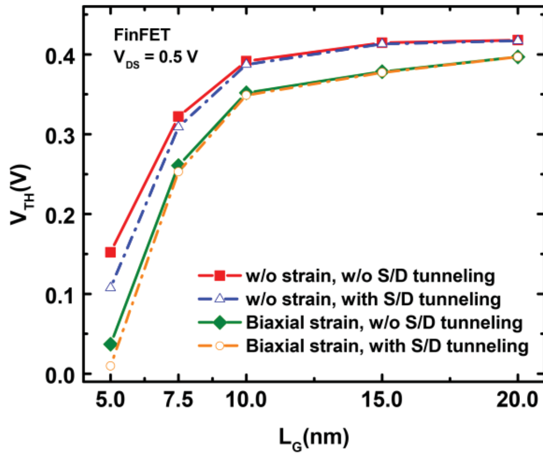

Fig. 5. Threshold voltage (V_{TH}) as a function of L_G in the FinFET device at V_{DS}=0.5V considering four different combinations: w/o strain and w/o S/D tunneling; w/o strain and with S/D tunneling; with biaxial strain and w/o S/D tunneling; and including both biaxial strain and S/D tunneling model.

Finally, Fig. 5 shows the threshold voltage (V_{TH}) behavior, which has been calculated according to the constant drain current method, for the four different scenarios as a function of the channel length. As expected, the V_{TH} is lower when S/D tunneling is considered due to the I_D increase. Moreover, the impact of the S/D tunneling on the V_{TH} increases as the L_G decreases, whereas it is almost negligible for devices with L_G >10nm. However, despite the number of particles that undesgoes S/D tunneling at low V_G is higher for the biaxial strained devices, the impact of this phenomenon on the V_{TH} is more pronounced for the relaxed devices.

IV. Conclusions

This work presents the impact of S/D tunneling in FinFETs considering relaxed and biaxial strained channels using a MS-EMC simulator. The biaxial strain has been locally included by tailoring the energy minima of each valley to reproduce the analytical strain mapping. The WKB approximation has been adopted for calculating the S/D tunneling probability. Moreover, the tunneling path assumption allows electrons to fly inside the potential barrier during a certain period of time following Newton's mechanics. We have demonstrated that the biaxial strain modifies the fundamental subband from Δ_4 to Δ_2 leading to a change of the S/D tunneling impact. The results show that, in subthreshold regime, the performance degradation induced by tunneling is more significant for the strained devices. This difference is reduced and even reversed as the gate bias increases.

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