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ALAM, A.E. <<http://orcid.org/0000-0001-8134-1429>>, CRANTON, Wayne <<http://orcid.org/0000-0002-0142-7810>> and DHARMADASA, I. <<http://orcid.org/0000-0001-7988-669X>>

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Electrodeposition of CdS thin-films from cadmium acetate and ammonium thiosulphate precursors

A. E. Alam¹ · W. M. Cranton¹ · I. M. Dharmadasa¹

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Abstract

Cadmium sulphide (CdS) thin-films have been electrodeposited using two electrode system to be used as the hole back diffusion barrier (hbdb) layer for graded bandgap solar cells with p-type windows. Cadmium acetate dihydrate [Cd(CH₃COO)₂·2H₂O] and ammonium thiosulphate [(NH₄)₂S₂O₃] have been used as the cadmium (Cd) and sulphur (S) precursors respectively. In this work, CdS layers have been grown on glass/FTO (fluorine doped tin oxide) substrates at cathodic potentials ranging from 1300 to 1460 mV in order to find the best growth voltage. N-type conductivity is observed for all the layers and band-gap ranged between ~2.36 and ~2.40 eV for as-deposited layers and ~2.31 and ~2.36 eV for air-annealed layers. X-ray diffraction (XRD) analysis revealed cubic/hexagonal mixed crystallinity for the as-grown layers which indicates a tendency of transiting towards hexagonal structure upon annealing. Compositional and morphological characteristics of the layers have been investigated with energy dispersive X-ray (EDX) and scanning electron microscopy (SEM) respectively.

1 Introduction

CdS/CdTe based solar cells, being one of the current market leaders for thin-film photovoltaics (PV), recorded 22.1% highest conversion efficiency, along with an ~18% module efficiency [1, 2]. The major growth techniques used for large area CdS/CdTe-based solar cell fabrication are, close spaced sublimation (CSS) [3], sputtering [4] and electrochemical deposition (ED) [5]. However, with respect to deposition process continuity, doping simplicity, self-purification, scalability, manufacturability, economic viability and Cd-containing waste reduction, electrodeposition (ED) is considered one of the leading techniques [6–11].

Our group has been working on CdTe-based thin-film PV research using all electrodeposited semiconductors following the graded bandgap (GBG) device structure. Graded bandgap solar cells, first conceptualised by Konagai and Takahashi [12], was later improved and next-generation multilayer graded bandgap solar cells were proposed and implemented by our group [11, 13–15]. Between the two proposed approaches of graded bandgap devices on n-type

and p-type window materials, cells fabricated on p-type windows have a potential of achieving high performance due to its possibility of producing higher open circuit voltage (V_{oc}). This was experimentally demonstrated by achieving $V_{oc} = 1.175$ mV with GaAs/AlGaAs system [16].

Our current efforts are focused on developing CdTe-based graded bandgap devices with p-type windows, using low-cost and scalable electro-plated materials. For multilayer GBG solar cells, apart from the regular window layer and absorber layer, improvements can be made by including an electron back-diffusion barrier (ebdb) layer and a hole back-diffusion barrier (hbdb) layer [17]. This will minimize the recombination of photo-generated and separated charge carriers caused by thermionic emission over the potential barrier [11, 17], as depicted in Fig. 1. A wide bandgap p-type CdTe:Mg material has already been developed and characterised by the group to be used as the possible p-window and reported in reference [18].

n-CdS is widely used as the window layer in electroplated graded bandgap solar cells developed with n-window approach. The most widely used cadmium (Cd) precursor is CdCl₂ in this case [19, 20]. But for electrodepositing CdS as a wide-bandgap hole back diffusion barrier (hbdb) layer, precursors should be chosen very carefully because, in this case the whole glass/FTO/p-window/CdTe absorber layer would require to be

✉ A. E. Alam
a.alam@shu.ac.uk

¹ Materials and Engineering Research Institute (MERI),
Sheffield Hallam University, Sheffield S1 1WB, UK

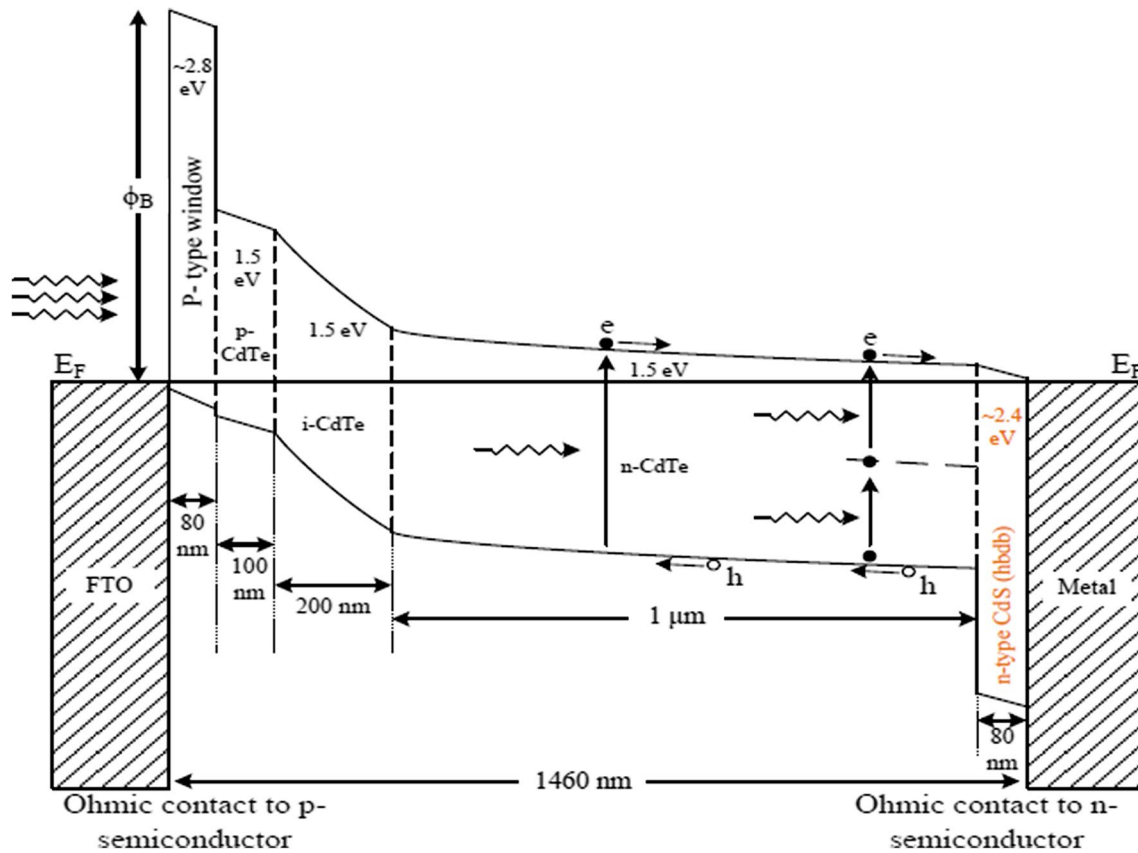


Fig. 1 Energy band diagram drawn to scale for a short-circuit multi-layer solar cell based on p-type window material ($p^+p-i-n-n^+$ structure). P^+ and n^+ layers act as electron back diffusion barrier (ebdb) layer, and hole back diffusion barrier (hdbb) layer respectively

submerged into the CdS electrolytic bath. Chlorine being a very strong corrosive agent and for having the strong hydrochloric acidity due to Cl^- and H^+ ions in the electrolyte, the underlying device structure can be dissolved [21]. Therefore, cadmium acetate $[Cd(CH_3COO)_2]$ precursor with weaker acidity has been used in this work.

Moreover, literature suggests sodium thiosulphate ($Na_2S_2O_3$) as the most widely used S precursor for CdS electrodeposition. But, this precursor tends to provide accumulation of sodium (Na), a p-type dopant in the CdS bath, which by incorporating through absorption or reaction may reduce the electrical conductivity of the CdS layer [22]. Hence, ammonium thiosulphate $[(NH_4)_2S_2O_3]$ has been used as the S precursor in this work.

This work focuses on growing ED CdS with the mixture of these precursors for the first time along with investigating through the growth potential and post-annealing characteristics. The aim is to grow n-CdS to be used as an hdbb layer suitable to be deposited on glass/TCO/p-window/CdTe-absorber layer for developing graded band-gap devices in future.

2 Experimental procedure

Cadmium sulphide (CdS) thin-film layers were grown from a 400 ml aqueous solution of 99% pure 0.3 M cadmium acetate dihydrate $[Cd(CH_3COO)_2 \cdot 2H_2O]$ and 99.5% pure 0.06 M ammonium thiosulphate $[(NH_4)_2S_2O_3]$ in de-ionised water. All these chemicals have been purchased from Sigma-Aldrich Ltd (UK). The pH and temperature of the solution has been kept constant at 3.00 ± 0.02 and $\sim 85^\circ C$ respectively. The pH has been adjusted using either nitric acid or ammonium hydroxide (NH_4OH). Two electrodeposition technique has been used for depositing the semiconductor materials on glass/TEC-7 Fluorine doped tin oxide (glass/FTO) substrates having sheet resistance of $\sim 7 \Omega/square$. High purity carbon rod has been used as the anode whereas, cathode (working electrode) has been prepared by attaching a glass/FTO substrate to a carbon rod using insulating polytetrafluoroethylene (PTFE) tape. Prior to electrodeposition, the substrates were cut into $3\text{ cm} \times 3\text{ cm}$ dimension and rinsed thoroughly with

de-ionized water after washing with soap solutions using cotton buds. The substrates were later dried with nitrogen gas. GillAC potentiostat from ACM Instruments is used as the power source for the 2-electrode ED system. The electrolytic solution was heated and stirred using a hot plate and magnetic stirrer. Moderate stirring rate has been applied to the bath throughout the electrodeposition process.

Cyclic voltammetry has been carried out to determine an estimated range of deposition potential where Cd and S co-deposition takes place. The deposited layers were investigated using energy dispersive X-ray (EDX) spectroscopy for compositional and material identification analysis and X-ray diffraction (XRD) for structural analysis and scanning electron microscopy (SEM) for morphological analysis. For characterising and optimising electrical and optical properties of the ED samples, photoelectrochemical (PEC) cell measurements and optical absorption using UV–Vis spectrophotometry have been carried out.

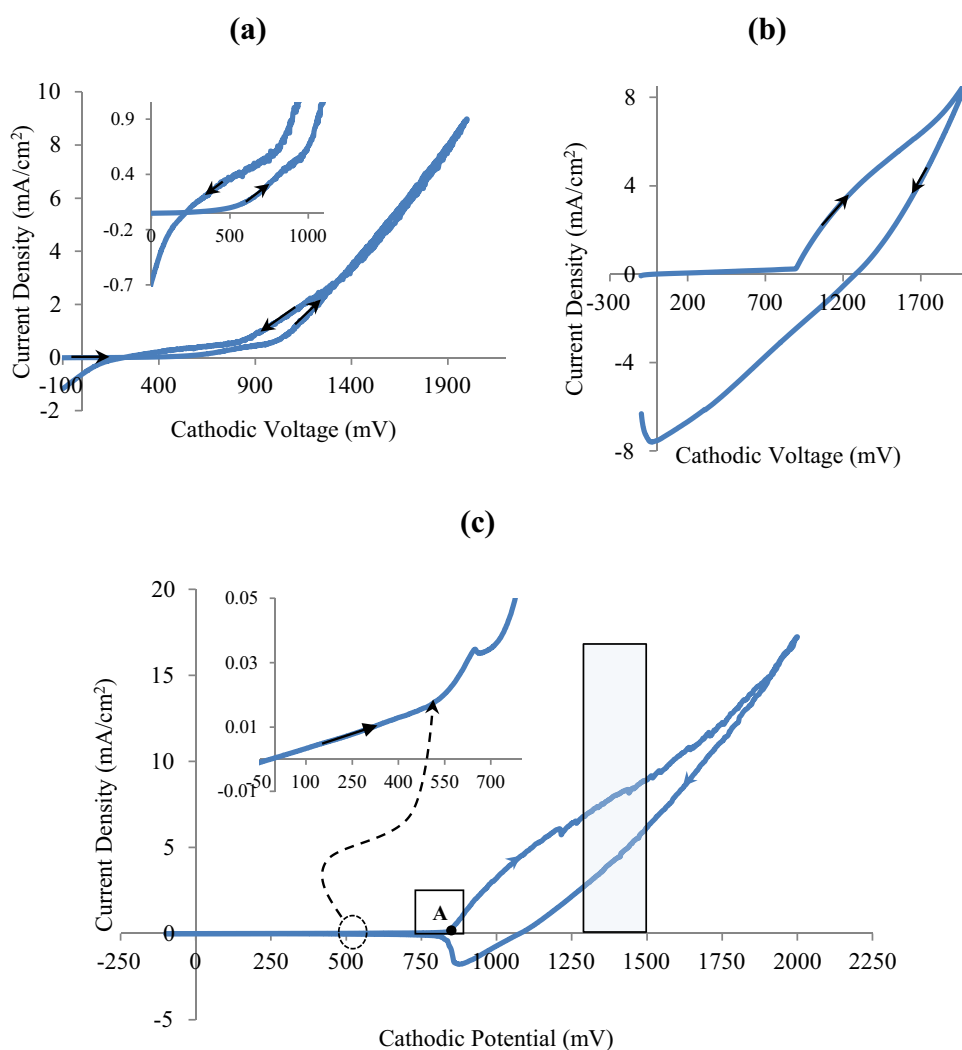
3 Results and discussion

3.1 Cyclic voltammetric Study

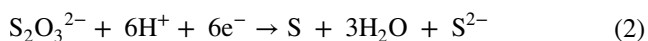
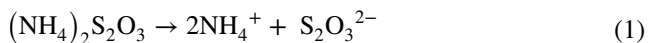
Cyclic voltammograms were separately recorded for electro-purified aqueous electrolytes containing 0.3 M $\text{Cd}(\text{CH}_3\text{COO})_2 \cdot 2\text{H}_2\text{O}$, 0.06 M $(\text{NH}_4)_2\text{S}_2\text{O}_3$ and a mixture of 0.3 M $\text{Cd}(\text{CH}_3\text{COO})_2 \cdot 2\text{H}_2\text{O}$ and 0.06 M $(\text{NH}_4)_2\text{S}_2\text{O}_3$. The pH and temperature of the solutions were adjusted to 3.00 ± 0.02 and $\sim 85^\circ\text{C}$ respectively. The cyclic sweep is recorded with a sweep rate of 3 mVs^{-1} within a cathodic potential range of 0.0 mV to 2000 mV. Figure 2 depicts a typical voltammogram data plotted with instructive symbols and legends.

Figure 2a depicts, due to the difference of redox potentials amongst the consisting ions, in the forward cycle of voltammogram sulphur (S) having a redox potential (E°) of +0.449 V (with reference to standard H_2 electrode), starts depositing at the beginning at ~ 500 mV. The

Fig. 2 Typical cyclic voltammogram of aqueous solution containing **a** 0.06 M $(\text{NH}_4)_2\text{S}_2\text{O}_3$, **b** 0.3 M $\text{Cd}(\text{CH}_3\text{COO})_2 \cdot 2\text{H}_2\text{O}$ [cadmium acetate dihydrate] and **c** mixture of 0.3 M $\text{Cd}(\text{CH}_3\text{COO})_2 \cdot 2\text{H}_2\text{O}$ and 0.06 M $(\text{NH}_4)_2\text{S}_2\text{O}_3$ in de-ionised water. pH and temperature of the solution were kept at 3.00 ± 0.02 and $\sim 85^\circ\text{C}$



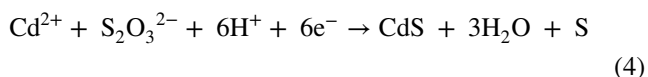
deposition takes place from the S precursor, according to the electro-chemical reaction Eqs. 1 and 2:



Later, Cd having an E° of -0.403 V (w.r.t. standard H_2 electrode) starts depositing at ~ 850 mV (Fig. 2b and point A in Fig. 2c) according to the electro-chemical reaction Eq. 3:



Hence, Fig. 2c shows the co-deposition of cadmium and sulphur begins hereafter and S-rich CdS starts to deposit from ~ 850 mV onward according to the reaction Eq. 4. As higher cathodic voltage is applied, Cd starts increasingly incorporating to the layer.



Therefore, it is estimated that near-stoichiometric CdS layer can be found within a range of ~ 1300 mV to ~ 1500 mV of growth potential. From 1500 mV onward, there is a relatively higher increment in current density, which indicates the possible dissociation of water.

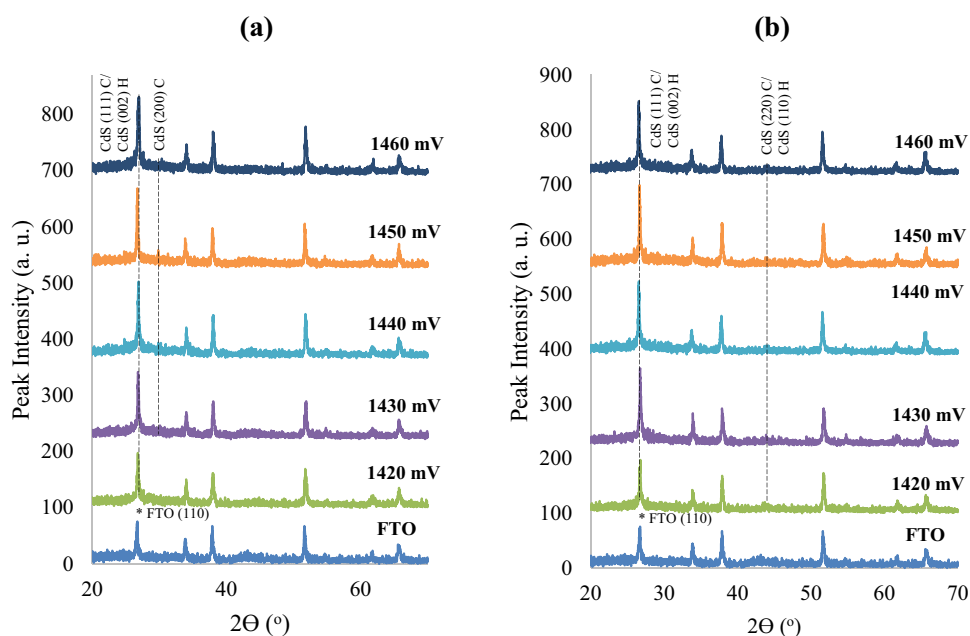
In the reverse cycle of Fig. 2c, the negative peak at ~ 850 mV reconfirms the dissolving of any elemental Cd as well as dissociation of CdS formed on the FTO surface.

3.2 X-ray diffraction (XRD) spectroscopic analysis

Aim of this analysis is to carry out the structural analysis of the deposited layers at different growth voltages. Philips

PW X'Pert Pro diffractometer has been used with Cu-K α monochromator having a wavelength of 1.54 \AA , where the source tension and current were kept as 40 kV and 40 mA respectively. XRD spectroscopy have been carried out on 5 as-deposited (AD) and heat-treated (HT) samples grown at 1420, 1430, 1440, 1450 and 1460 mV cathodic potential. In Fig. 3a, at $2\theta \approx 26.6^\circ$ and $\approx 30.1^\circ$ the as-deposited samples show XRD peaks corresponding to the diffraction from CdS (111) cubic/(002) hexagonal and CdS (200) cubic planes respectively. It is difficult to differentiate between CdS (111) C and (002) H plane because they coincide within 1%, therefore the XRD peak is often considered as resultant from mixed structures [23, 24]. Also, increment in the dominant peak intensity for AD CdS layers indicates the coinciding of CdS (111)C/(002)H peak with the underlying FTO (110) peak. After heat-treatment it is widely observed that CdS transforms phase from cubic/mixed to completely hexagonal CdS [20, 22]. In this work, the effect of annealing demonstrates a different trend of changes, indexing with the JCPDS reference files 89-0440 for cubic phase and 80-0006 for hexagonal phase. Figure 3b shows, after the heat treatment of the layers at 400°C for 20 min, whereas CdS (111) C/(002) H mixed phases still stay the preferred orientation at $2\theta \approx 26.6^\circ$, the slight (200) C peak disappears and CdS (110) H/(220) C mixed phase come into appearance at $2\theta \approx 43.9^\circ$. Though, this does not indicate a confirmed phase transition of the material from mixed to hexagonal, but shows a tendency towards achieving the hexagonal phase which is further supported by later experiments. For the dominant planes resulting from different growth voltages, the trend shows that peak intensity keeps gradually increasing upto 1450 mV and then goes down. Figure 4 depicts

Fig. 3 XRD patterns of CdS thin films grown at V_g range from 1420 to 1460 mV **a** for as-deposited and **b** after heat treatment for 20 min under 400°C in air



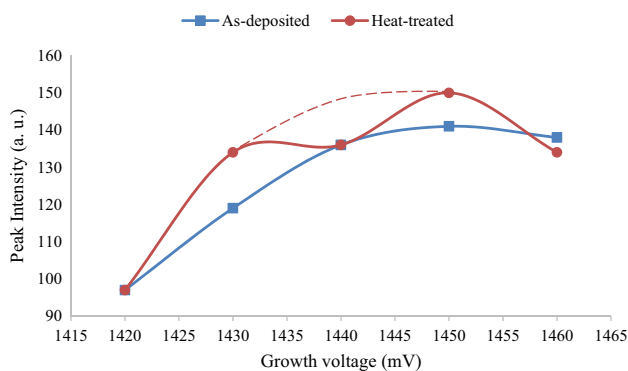


Fig. 4 Comparative analysis of dominant peak intensities for AD and HT layers grown at different cathodic voltages

this trend for both the as-deposited and heat-treated CdS samples. Along with the peak intensity, change of the CdS crystallite size due to growth voltage is shown in Table 1 for both the AD and HT samples. Crystallite size at the preferred orientation has been calculated using Scherrer’s formula given by Eq. (5).

$$D = \frac{0.94\lambda}{\beta \cos \theta} \tag{5}$$

where wavelength, $\lambda = 1.54 \text{ \AA}$, β = full width at half maximum (FWHM) of the diffraction peak in radian and θ = Bragg’s angle of incidence.

Table 1 shows that the as-deposited samples grown at 1450 mV has the largest crystallite size among the others. For HT samples, the trend carries on and all the HT samples show larger crystallite size than their as-deposited counterparts.

However, all CdS layers grown here on the TEC-7 glass/FTO substrates show overlaps of the dominant CdS plane with the dominant FTO (110) plane at $2\theta \approx 26.6^\circ$. Since,

the first batch of FTO substrates shown the preferred FTO orientation at $2\theta \approx 26.6^\circ$, for reconfirmation, another CdS layer has been deposited at the best apparent growth voltage (~ 1450 mV) on another batch of substrate having a different preferred orientation. Figure 5 shows that, CdS layers grown on a substrate having a preferred orientation elsewhere, also depicts a sharp peak intensity at $2\theta \approx 26.6^\circ$ for both as-deposited and heat-treated samples. The AD layer demonstrates cubic/hexagonal mixed phases at preferred orientation and (200) C peak at $2\theta \approx 30.1^\circ$. The HT sample still demonstrates mixed phases at preferred orientation, but (200) C peak disappears and another mixed peak appears at $2\theta \approx 43.9^\circ$ like the previous batch shown in Figs. 3 and 4. Alongside, there appears a slight peak at

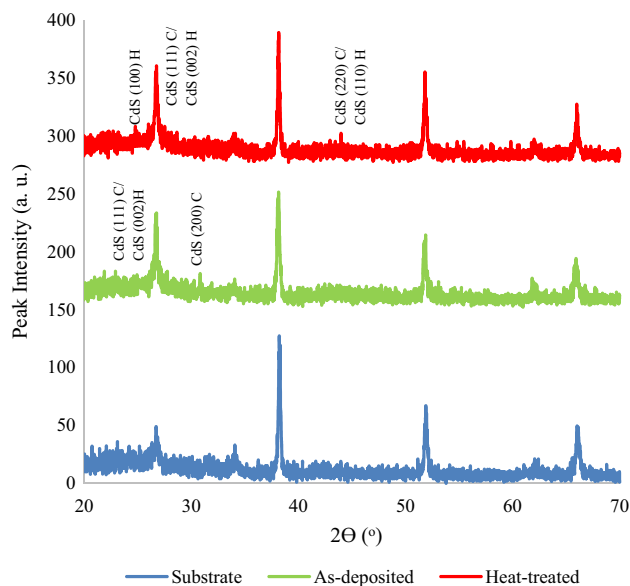


Fig. 5 XRD patterns of CdS layers grown on alternative substrate having different preferred orientation reconfirms the above results

Table 1 XRD analysis of as-deposited and heat treated CdS layers with the increasing Vg from 1420 to 1460 mV

Sample	Growth voltage, Vg (mV)	Peak position, 2θ ($^\circ$)	D-spacing (\AA)	FWHM ($^\circ$)	Crystallite size, D (nm)	Lattice strain (A. U.)	Plane of orientation (h k l)	Assignments
As-deposited	1420	26.753	3.33	0.265	32.20	0.0049	(111)/(002)	Cubic CdS/hexagonal CdS
	1430	26.702	3.33	0.245	34.82	0.0045		
	1440	26.535	3.36	0.227	37.57	0.0042		
	1450	26.652	3.34	0.210	40.62	0.0039		
	1460	26.536	3.35	0.340	25.08	0.0063		
Heat-treated	1420	26.769	3.33	0.238	35.85	0.0044	(111)/(002)	Cubic CdS/hexagonal CdS
	1430	26.769	3.33	0.228	37.42	0.0042		
	1440	26.769	3.33	0.208	41.02	0.0038		
	1450	26.645	3.34	0.195	43.75	0.0036		
	1460	26.903	3.31	0.200	42.68	0.0035		

$2\theta \approx 25.0^\circ$ for CdS (100) hexagonal phase. This further indicates a tendency for the layers towards achieve hexagonal phase upon heat-treatment, though having possibilities to have mixed phases present in the structure.

3.3 Energy dispersive X-ray (EDX) spectroscopy

EDX was carried out on the as-deposited and heat-treated CdS samples grown at 1430, 1440 and 1450 mV, using the compositional analysis software associated with the Quanta 650 SEM equipment, in order to obtain the chemical composition of the samples. The heat-treated samples were annealed at 400 °C for 20 min in air. Figure 6 shows the EDX spectra of the as-deposited and heat-treated sample grown at 1450 mV. Table 2 presents the atomic composition of as-dep and HT CdS grown at different voltages along with their changes in Cd/S ratio. It depicts that all the as-dep layers are S-rich in nature regardless the growth potential, whereas after heat treatment all of them shows slight comparative decrement in S percentage which resulted the HT sample grown at 1450 mV reaching stoichiometry. Despite having concerns about accuracy, EDX technique and this analysis give a qualitative idea about the composition of the CdS films and the near-stoichiometric growth potential for the process. This achievement of stoichiometry confirms the structural analysis using XRD and the achievement of highest crystallinity at 1450 mV. Any thin-film layer with only one phase tend to crystallise better during this growth process.

Table 2 Compositional analysis of as-deposited and heat-treated CdS layers at different growth voltage

Sample	Growth voltage, Vg (mV)	Atomic composition (%)		Cd/S ratio
		Cd	S	
As-deposited	1430	49.61	50.39	0.98
	1440	49.23	50.77	0.97
	1450	49.50	50.50	0.98
Heat-treated	1430	49.66	50.34	0.99
	1440	49.45	50.55	0.98
	1450	50.00	50.00	1.00

3.4 Photoelectrochemical cell (PEC) measurement

Photoelectrochemical cell measurements were carried out to determine the conduction type of the electrodeposited layers. The measurement is taken by dipping a glass/FTO/CdS layer along with another carbon electrode into an electrolyte prepared from 0.1 M Na₂S₂O₃ (sodium thiosulphate) aqueous solution. The voltage difference between the electrodes under dark (V_D) and illuminated (V_L) condition is measured to determine the conduction type of the semiconductor layer. This difference ($V_L - V_D$) represents the open circuit voltage of the solid/liquid junction and is commonly referred as the PEC signal. Polarity of the PEC signal indicates the conduction type. In this work, negative polarity of the PEC signal directs to n-type semiconductor and positive polarity directs to p-type semiconductor, whereas for metals, insulators and intrinsic semiconductors PEC signal is ideally zero. Figure 7

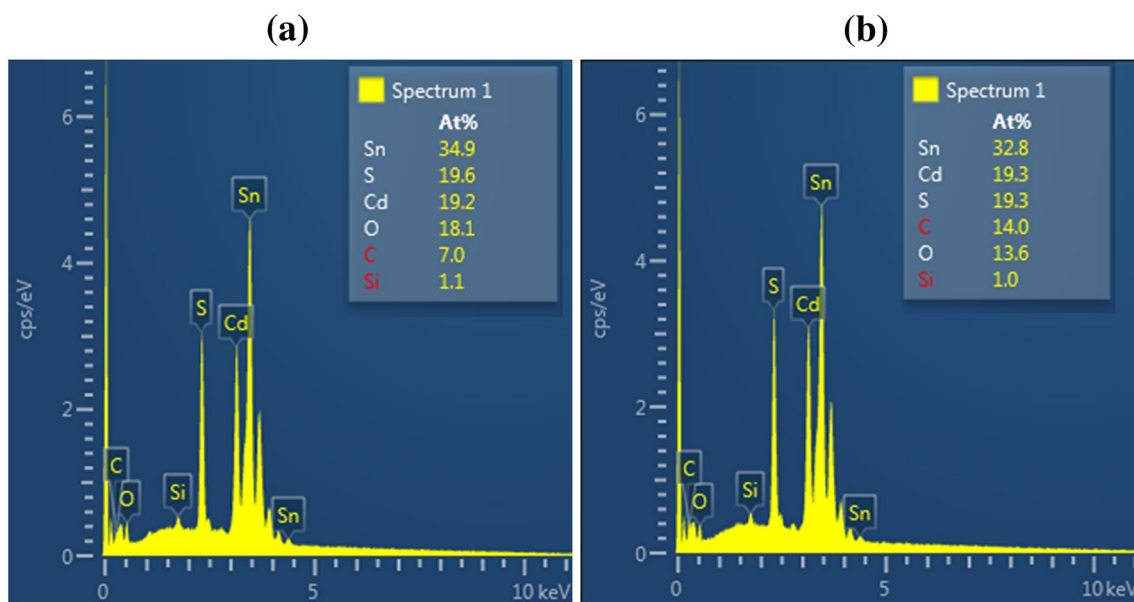


Fig. 6 EDX spectra of the **a** as-deposited and **b** heat-treated CdS films grown at 1450 mV

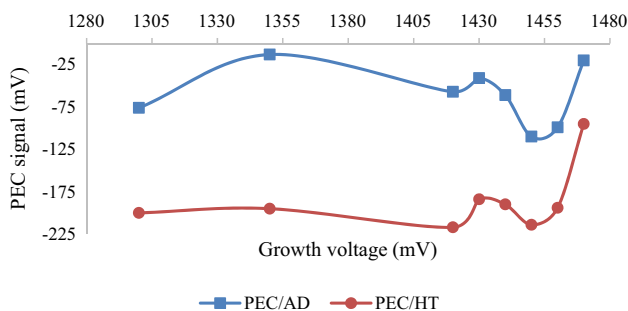


Fig. 7 PEC signal for AD and HT CdS samples

shows that all the CdS layers deposited at different cathodic potentials are n-type in conductivity as expected [19, 25]. HT samples show a stronger PEC signal compared to that of the AD samples. Strength of the PEC signal qualitatively indicates to the doping density and depletion region strength.

3.5 Optical absorption analysis

Optical absorption study has been carried out using Carry 50 scan UV–Vis spectrophotometer, for AD and HT CdS layers deposited at different growth voltages. The obtained absorption data within the wavelength of 300 nm to 1000 nm, have been used to plot an alternative Tauc plot, where square of absorbance (a^2) is plotted against photon energy ($h\nu$) [15, 26]. The intersection of extrapolated tangent line derived from the curve, gives the direct band-gap (E_g) of the studied semiconductor material.

According to Figs. 8a and 9, as-deposited CdS layers show direct band-gaps ranging between ~2.36 and

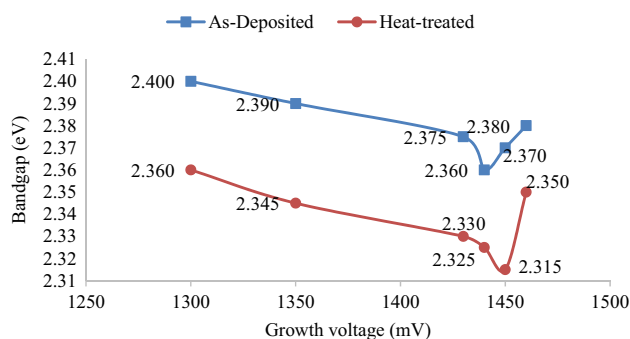
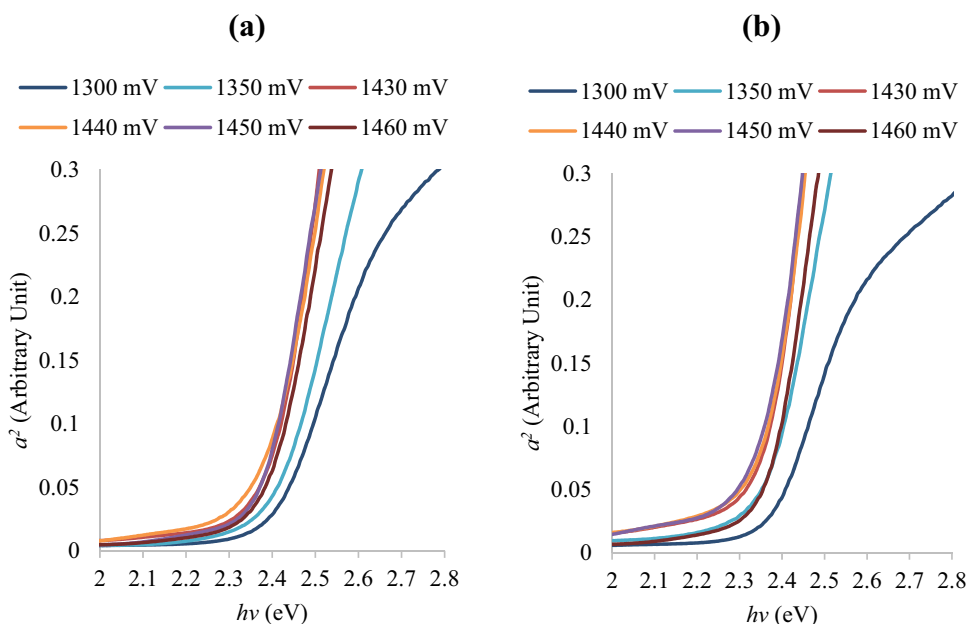


Fig. 9 Change of bandgap for CdS samples due to the change of growth potential

~2.40 eV, where the lowest band-gap value is observed at ~1450 mV of growth potential. Heat-treated CdS layers depict a similar trend as per Figs. 8b and 9, but after heat-treatment, band-gap decreases overall compared to that of the AD layers. Band-gaps of the HT layers range between ~2.31 and ~2.36 eV. The lowest band-gap value (~2.31 eV) for the heat-treated samples is found for the layer grown at 1450 mV which differs slightly from the previously measured E_g values (~2.42 eV) for electrodeposited CdS layers in the group [20, 22, 27]. This observation is supported by the visual appearance of the deposited layers as shown in Fig. 10. The CdS layers electrodeposited from these precursors demonstrate an orangish yellow appearance compared to the greenish yellow appearance of the previously electrodeposited CdS layers in our group [15, 20]. This indicates a possible shift in the typical absorption point of the layer from lower

Fig. 8 a^2 vs $h\nu$ plot for a as-deposited and b heat-treated (at 400 °C for 20 min in air) CdS samples



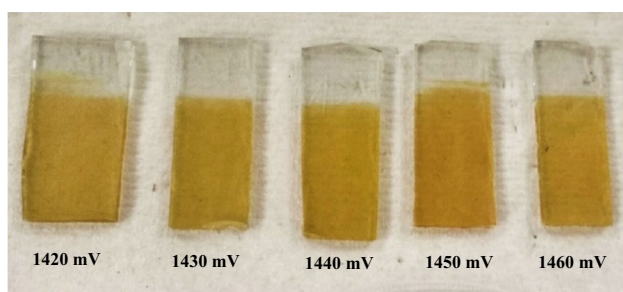


Fig. 10 Physical appearance of the as-deposited CdS layers grown at different cathodic voltages

wavelength towards higher wavelength, and vice-versa for the band-gap energy.

3.6 Scanning electron microscopy (SEM) analysis

In order to carry out the morphological characterisation of the CdS layers, SEM analysis has been done in the form of micrographs with Quanta 650 nano SEM instrument using 15.0 kV electron beam voltage and 32,000 \times of magnification. SEM images of glass/FTO/CdS substrates have been taken for both as-deposited and heat-treated samples grown at 1440 mV (Fig. 11a, b) and 1450 mV (Fig. 11c, d). In Fig. 11, at both growth voltages, regardless of heat-treatment, all the surfaces demonstrate agglomerations of CdS crystallites. From the SEM micrograph the size of the agglomerations are ranging approximately between \sim 200

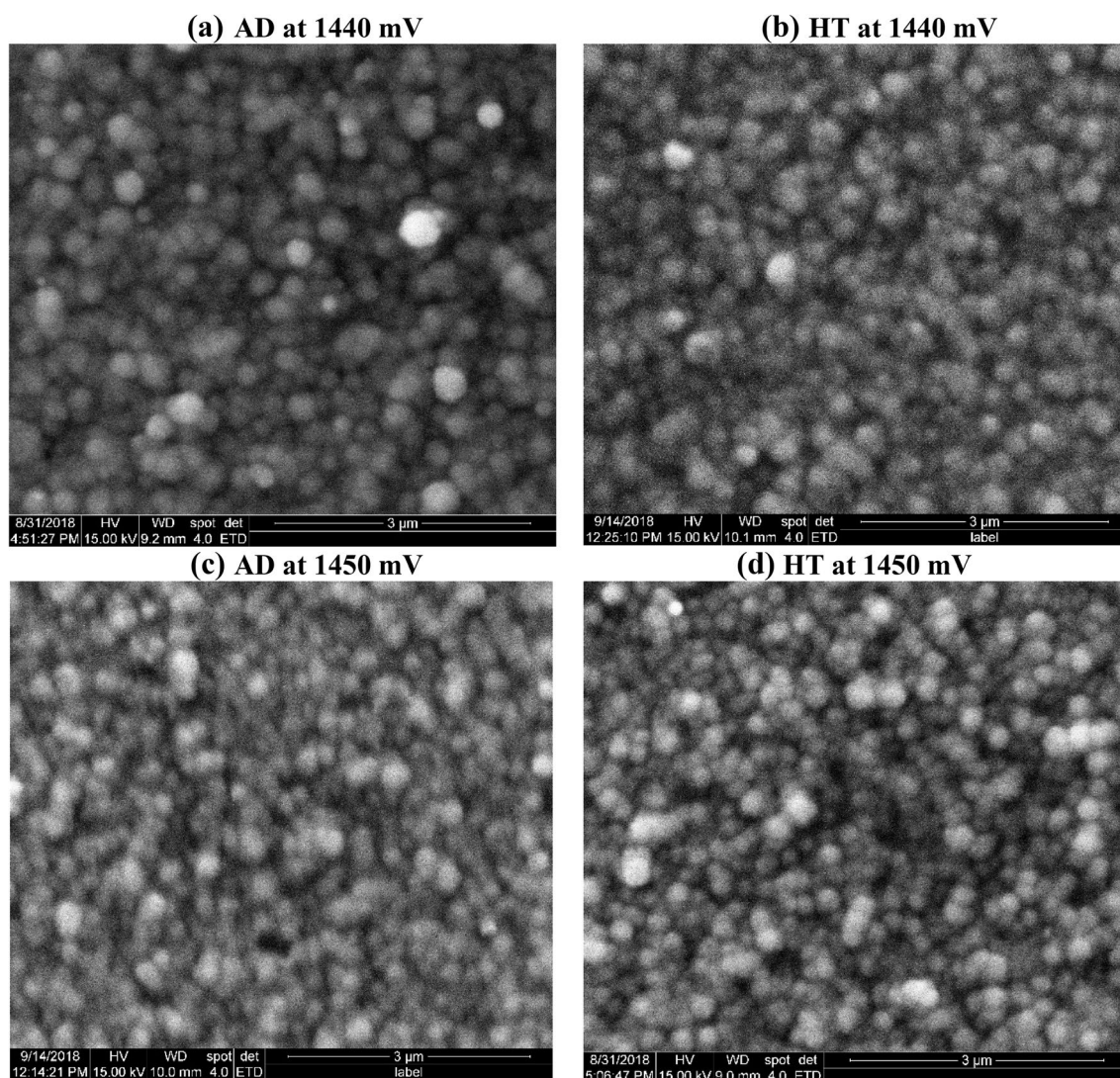


Fig. 11 Typical SEM images of CdS thin films grown at 1440 mV and 1450 mV **a, c** as-deposited and **b, d** heat-treated at 400 °C for 20 min in air

and ~300 nm. Therefore, individual CdS crystallites are not visible in the SEM image as calculated above in Table 1.

4 Conclusion

In this work, a low acidic precursor for Cd, and Na-free precursor for S were used for the electrolyte, so that CdS layers can be electrodeposited on top of CdTe absorber layers, in order to develop all-electrodeposited graded bandgap devices, starting from p-type wide-bandgap window materials. As the first step towards achieving this, CdS layers were deposited on glass/FTO substrate with the new precursors. The optimised growth voltage was 1450 mV for experimental conditions used in this work. As-deposited material consists of both cubic and hexagonal CdS, but demonstrates a tendency to transit towards hexagonal CdS after heat treatment at 400 °C for 20 min in air. All the layers grown are n-type in electrical conductivity. The only difference observed was the physical appearance of orangish colour instead of greenish yellow colour observed for CdS grown with other precursors. Accordingly, a lower bandgap energy of 2.31 eV was observed for the heat treated CdS layers. Incorporation of the layers in both graded bandgap devices based on n-type and p-type window layers are in progress.

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Compliance with ethical standards

Conflict of interest The authors declare no conflict of interest.

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