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Design optimization of the graded AlGaN/GaN HEMT device performance based on material and physical dimensions

N.A.F Othman[1], S. Rahman[1], S Wan Muhamad Hatta[1,2], N. Soin[1,2], B. Benbakhti[3], S.Duffy[3]
[1]Department of Electrical Engineering, Faculty of Engineering, University of Malaya, 50603, Malaysia
[2]Centre of Printable Electronics, University of Malaya, 50603, Malaysia
[3]School of Engineering, Liverpool John Moores University, L3 2AF United Kingdom

Abstract

Purpose - Design optimization of the traditional AlGaN/GaN HEMT device has been comprehensively conducted in achieving improved performance and current handling capability using the Synopsys' Sentaurus TCAD tool.

Design/Methodology/Approach - Varying material and physical considerations, specifically investigating the effects of graded barriers, spacer interlayer, material selection for the channel as well as study of the effects in the physical dimensions of the HEMT have been extensively carried out.

Findings- Critical figure-of-merits (FOMs) specifically the DC characteristics, 2DEG concentrations and mobility of the heterostructure device have been evaluated. Significant observations include enhancement of maximum current density by 63% while the electron concentration was found to propagate by 10^{20} cm^{-3} in the channel.

Originality/Value- This work aims to provide tactical optimization to traditional HFETs, rendering its application as power amplifiers, MMICs and RADAR, which requires low noise performance and very high RF design operations. Analysis in covering the breadth and complexity of heterostructure devices has been carefully executed through extensive TCAD modelling and the end structure obtained has been optimized to provide best performance.

Keywords Semiconductor device modelling; Device optimization; GaN HEMT; figures of merits; charge carrier mobility.

Paper Type Research Paper

I. Introduction

Gallium nitride (GaN) based heterostructure field effect transistor (HFET), or the high electron mobility transistor (HEMT) has become a very promising device for high-frequency (Synopsys Inc., 2014, Binder et al., 2018) and high-power application specifically in the microwave and radio frequency (RF) bands (Lenka et al., 2013, Sun et al., 2017). The implementation of the nitride-based material inside the buffer layer can lead to physical properties improvement such as higher band gap, high breakdown voltage and on-state current density, as well as strong polarization fields including both spontaneous and piezoelectric charges (Shrestha et al., 2014). End-use industries are widely opting GaN semiconductor devices owing to the excellent properties of the material including high temperature resistivity, low power consumption and high thermal conductivity and operability even at high temperature, thus augmenting their application in critical applications such as in the defense industry. The major figure-of-merits (FOMs) for heterostructure devices that need to be taken into consideration are the two dimensional electron gas (2DEG) concentration and mobility which are located between the aluminum gallium nitride (AlGaN) barrier and GaN buffer heterointerfaces. Recently, process optimization of heterostructures in achieving better device performance has progressed remarkably by taking into consideration of the quality of the material as well as design architectures of the GaN-based HFETs (Zhi-Yong et al., 2007, Das et al., 2014, Zhou et al., 2015, Brech et al., 1997). These designs are well associated with the performance of the 2DEG density and mobility performances. For instance, the rising amount of aluminum (Al) percentage inside the $Al_xGa_{1-x}N$ barrier (where x is the mole fraction) can improve the polarization effects (Ambacher et al., 2000, Köhler et al., 2010, Wang et al., 2006) which results in the increase of effective 2DEG density inside the channel layer. Furthermore, better 2DEG confinement can be achieved with higher Al content inside the barrier due to larger conduction band discontinuity since a larger barrier is produced (Zhi-Yong et al., 2007).However, in the perspective of surface morphology, the higher amount of Al in the barrier is related to the presence of strain inside the crystal arrangements by which too high Al percentage can cause the lattice mismatch to highly increase and interrupting the interface quality therefore reducing the device's mobility (Das et al., 2014, Arulkumaran et al., 2003, Miyoshi et al., 2005, Keller et al., 1999). Apparently, there is a limiting factor to the increment of Al mole fraction in $Al_xGa_{1-x}N$ barrier where the

Al percentage can only be increased up to 40% in order to improve the 2DEG concentration and mobility (Arulkumaran et al., 2003). Earlier works have shown that by altering the device's structure such as modifying barrier doping (Firoz and Chauhan, 2011), step-grading the structure layers (Yu et al., 2014, Das et al., 2014), as well as inserting interlayers in between the heterointerfaces (Roy et al., 2015, Shrestha et al., 2013, Brazzini et al., 2013), one can adjust the 2DEG concentration and also the device's mobility in the channel layer significantly. Besides that, design optimization in terms of physical dimensions are also vital in minimizing feature sizing without degrading their performances especially in switching speed and power consumptions (Binder et al., 2018). In this work, design optimization of the GaN-based heterostructure have been studied in order to improve the performance of the HFET device in terms of 2DEG concentrations and mobility such as step-grading the barrier layer of $Al_xGa_{1-x}N$ where *x* is the mole fraction of aluminum (Al), inserting the interlayer spacer at the heterointerfaces, as well as altering the material of the HFET channel. By employing these design combinations, a novel structure of GaN-based HEMT is proposed by which the results obtained for all three conditions is compared to the conventional AlGaN/GaN HEMT. The influences of these design considerations on carrier concentrations, mobility, velocities as well as the electric fields of the device are analyzed. Subsequently, the final structure of the GaN-based HEMT is optimized with the considerations of geometrical variations and the device's performance characteristics are investigated.

II. GAN BASED HFET DESIGN

A. HFET Structure

The device under study in this paper is a GaN-based HEMT. The epitaxial layers of the original conventional $Al_xGa_{1-x}N$/GaN HEMT device, where x = 0.25 are assumed to have grown in the [0001] Ga-face direction on a silicon (Si) substrate. The schematic cross sections of the conventional device are shown in Fig. 1(a). The epi-structure consists of a 10 nm AlN nucleation layer formation subsequent to the substrate and an undoped GaN buffer layer with a thickness of 2.0 µm is grown after. Then, a thin channel layer of 5 nm is defined inside the buffer layer, followed by the growth of a thin interfacial spacer layer of 2 nm. Finally, an 18 nm barrier layer of the device was deposited and followed by GaN capping layer as well as SiN passivation. There are three different designs that were considered in this study, where each design outperforms the previous as shown in Fig. 1. The first structure, namely Structure 1 is designed to have a step-graded $Al_xGa_{1-x}N$ barrier where x indicates the mole fraction of Al. The Al mole fraction for the step-graded $Al_xGa_{1-x}N$ barrier were set to be x = 0.5 for the first layer, x = 0.35 at the second layer and finally x = 0.2 with a thickness of 6 nm each (see Fig. 1(b)). Meanwhile, the design of the second structure, Structure 2 is the modification from the previous design where the AlGaN material for spacer region was replaced by the AlN material (see Fig. 1(c)). The final structure or Structure 3 is then compared to the two previous structures where the InGaN channel is implemented instead of a GaN channel in the conventional HFET structure (see Fig. 1(d)). The results obtained comparing these three designs were explained in detailed in Section III. The final structure is then simulated by taking into account of the geometrical considerations in terms of barrier layer thickness (t_b), gate length (L_g), and source-gate separation length (L_{sg}) in Section IV. The values for each parameter involved in the simulation are summarized in Table 1 including the default values used for the conventional HFET in this study.

B. Simulation Details

The 2D device simulations using the commercial software Sentaurus Synopsys TCAD is performed on the GaN-based HEMT. The gate contact is set to be Schottky type with a metal work function, Φ_{MG} of 4.4 eV. In this study, the electrical properties such as 2DEG concentration and mobility, electric fields as well as carrier velocity were extracted using the Sentaurus Visual. Drain bias, V_{ds} of 36 V was applied for all simulation conditions. Two levels of V_{gs} were applied for the DC output (I_d-V_d); V_{gs} = -2 V and V_{gs} = +2 V. During device simulation, required models have been incorporated for simulation precision such as mobility models, high-field saturation dependency as well as recombination mechanism, i.e. Shockley-Read-Hall process. To account for self-heating effect, the drift diffusion models were also integrated. Spontaneous and piezoelectric components were taken into account for the built-in polarization model which computes the formation of interface charges at the heterointerfaces due to the polarization divergence (Ambacher et al., 1999). The anistropic dielectric tensor is used concerning the reduction in polarization due to converse piezoelectricity (Ashok et al., 2009). Surface scattering roughness mechanism has also been taken into account during the simulation through the use of the constant mobility model and Lombardi model (Lombardi et al., 1988). In the simulation, surface charges are used to compensate the electron channel depletion caused by the negative polarization charges due to large polarization divergence at the cap surface (GaN/AlGaN) interfaces. In this

TABLE 1
PARAMETERS USED IN THE SIMULATED HFET (Synopsys Inc., 2014)

Parameters / Conditions	Conventional HFET	Proposed final design for HFET(Structure 3)
GaN cap thickness, t_c	3 nm	3 nm
GaN cap doping, N_c	$5x10^{18}$ cm^{-3}	$5x10^{18}$ cm^{-3}
AlGaN barrier layer	Ungraded – 25% Al	Graded (3 layers) – 50%, 35% and 25% Al
*AlGaN barrier thickness, t_{br}	18 nm	18 – 30 nm (stepsize 3 nm)
Interfacial spacer layer	AlGaN	AlN
Channel material	GaN	InGaN
Gate length, L_g	0.8 µm	0.8 µm
Source-gate separation, L_{sg}	1.0 µm	1.0 µm
Gate-drain separation, L_{gd}	3.0 µm	3.0 µm
*Spacer depth, t_{sp}	2 nm	2 – 5 nm (stepsize 1 nm)
Channel depth, t_{ch}	5 nm	5 nm
*Buffer thickness, t_{bf}	2 µm	2 – 3 nm (stepsize 0.5 nm)
AlGaN barrier doping	$2 x10^{18}$ cm^{-3}	
Spacer doping, N_s	$1 x10^{14}$ cm^{-3}	
Buffer doping, N_{bf}	$1x10^{15}cm^{-3}$	

*Note: Parameters used in geometrical variation analysis in Section IV

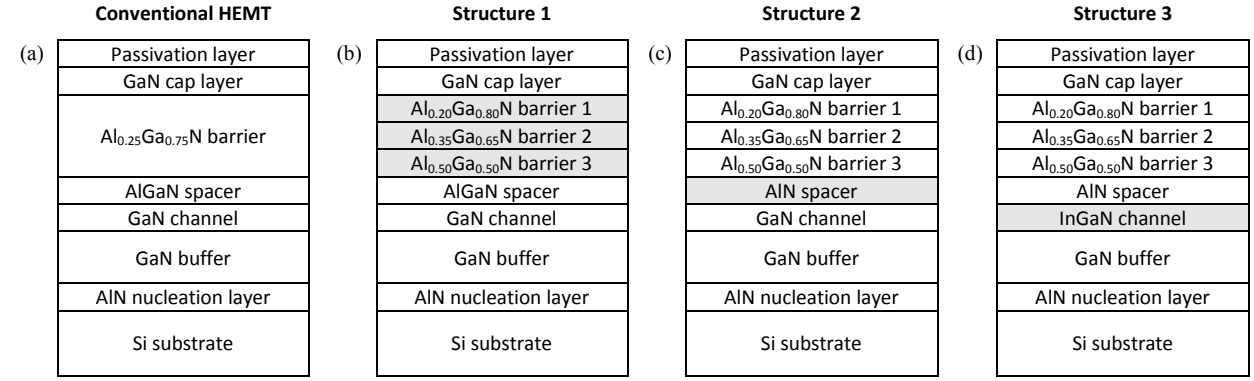

Fig.1: Schematic diagram of simulated GaN-based HFET showing (a) conventional $Al_xGa_{1-x}N$/GaN HFET; (b) graded $Al_xGa_{1-x}N$ barrier with AlGaN spacer and GaN channel – Structure 1; (c) graded $Al_xGa_{1-x}N$ barrier with AlN spacer and GaN channel – Structure 2 ($Al_xGa_{1-x}N$/AlN/GaN HFET); and (d) graded $Al_xGa_{1-x}N$ barrier with AlN spacer and InGaN channel – Structure 3 ($Al_xGa_{1-x}N$/AlN/InGaN HFET). For conventional device: x = 0.25; Structure 1-3: x_1 = 0.2, x_2 = 0.35, x_3 = 0.5.

work, the charges were compensated by deep, single-level trap states, with $N_{Tsurf} = 5x10^{13}$ cm^{-2} and $E_{Tsurf} - E_i = 0.4$ eV.

III. SIMULATED RESULTS AND DISCUSSIONS

Fig. 2 and Fig. 3 present the influence of barrier, spacer and channel layer process designs on DC output and transfer characteristics respectively. In this section, the impact of device design in terms of barrier will be discussed based on Fig. 2(a) in Section III-A, while Section III-B and III-C will focus on device design in terms of spacer and channel based on Fig. 2(b) and Fig. 2(c), respectively. At the end of this section, the optimized design of GaN-based HFET will be identified and is used for further study in Section IV.

A. Device Barrier Layer

For the first enhanced structure, Structure 1, a step-graded AlGaN barrier is used to improve the design performance. Fig. 2(a) compares the DC output characteristics at V_{gs} = -2V and V_{gs} = +2V for step-graded AlGaN barrier (Structure 1) (refer Fig. 1) with those of conventional GaN-based HFET. The I_d-V_d curves show improvement for the graded barrier with reduced Al mole fraction compared to conventional device. It is observed that the peak current density can achieve up to 3.3 /mm which increases by 63% compared to conventional HFET at V_{gs} = +2V. In addition, the transfer characteristics are illustrated in Fig. 3. From Fig. 3(a), the transfer characteristics depicts the increase in current density by 1.26 A/mm when the barrier is graded, with maximum drain current achieved is 3.3 A/mm. This observation correlates to earlier findings on AlGaN/GaN heterostructure electrical properties and is related to the presence of 2DEG in the channel (Zhi-Yong et al., 2007, Das et al., 2014). The 2DEG in the device barrier can be induced to increase which results in larger conduction-band discontinuity. This phenomenon will also enhance the piezoelectric (PE) polarization effect and thus improving 2DEG sheet density in the channel region. It has been observed in this work that the PE polarization density is enhanced as the Al content increases gradually in the proposed structure, compared to that in the conventional HFET which Al content in the barrier is consistent. Moreover, the polarization density is also affected by the lattice mismatch between Al and GaN compound, which leads to higher electron density at AlGaN/GaN interfaces (Ambacher et al., 1999). The adoption the step-grading AlGaN barrier structure can greatly overcome current collapse due to the screening of surface traps at the lower part of the widened channel (Zhou et al., 2015). Since the barrier is graded, there are large numbers of mobile electrons inside the barrier making the device immune to surface trapping effects, therefore results in smaller current collapse.

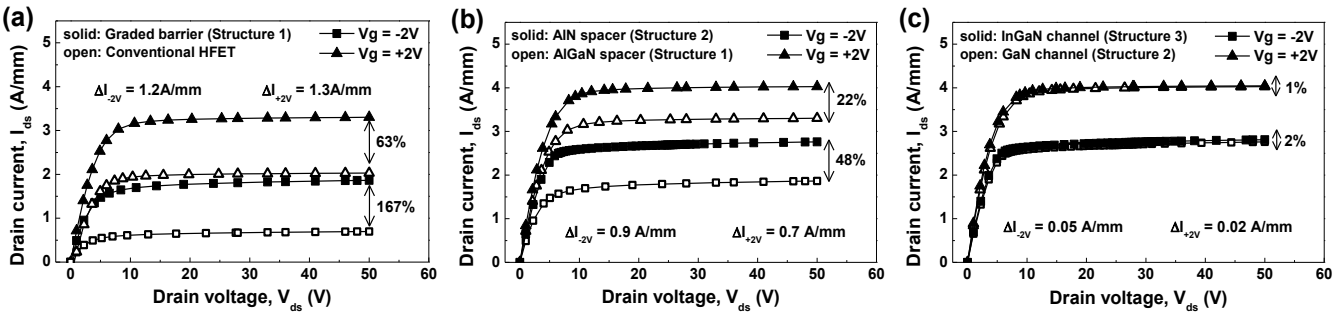

Fig. 2. I_{ds} – V_{ds} characteristics at V_{gs} = -2V and V_{gs} = +2V for (a) conventional and graded AlGaN barrier HFET (Structure 1); (b) AlN spacer HFET (Structure 2); and (c) InGaN channel HFET (Structure 3)

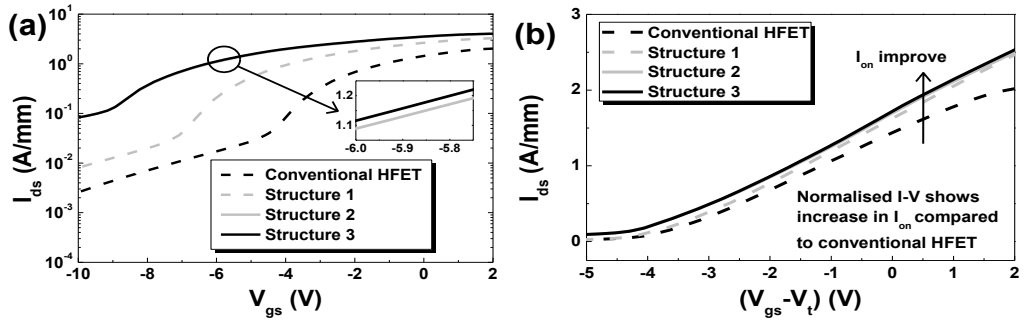

Fig. 3. (a) I_{ds} – V_{gs} characteristics at V_{ds} = 36V in logarithmic scale and (b) Graph of normalised I_{ds} versus (V_{gs}–V_t) curves for all structure

In addition, study of Fig. 4 has shown major improvement of 2DEG density at the channel region, by which the maximum magnitude can be achieved up to $1.66x10^{18}$ cm^{-3} for Structure 1 with graded barrier structure compared to the conventional HFET with density of $0.39x10^{3}$ cm^{-3}. However, extremely high content of Al inside the device barrier will eventually degrade the crystal quality of the interface, thus reducing electron mobility (Das et al., 2014). Fig. 5 depicts the comparison of the total current density in Structure 1, Structure 2 and the conventional HFET. From the figure, it is observed that the electron mobility is decreased particularly at the gate area for the graded barrier in Structure 1 compared to the conventional HFET. Earlier work (Lu et al., 2003, Miyoshi et al., 2004) has shown the dependence of electron mobility on the Al content in the barrier in which the carrier mobility reduces as the Al mole fractions increase. Apparently, reduction in mobility is caused by the differences in scattering factors when the barrier is graded. These are observed when the percentage of Al dopant inside each barrier is decreased. Apart from that, the total current density is greater for the graded barrier structure particularly at the source, gate and drain region. It is worth mentioning that the leakage is potentially higher for the graded barrier structure by observing the total current density due to higher electric field (Rezali et al., 2016) at the AlGaN/GaN interface as shown in Fig. 6. The peak electric field for Structure 1 according to Fig. 6(b) is 9.22 $x10^{6}$ Vcm^{-1}, which is higher compared to conventional HFET at 4.87 x 10^{6} Vcm^{-1}. In high-electric field stress, it is possible that the density of electron traps under the gate-drain region, caused by the hot electron bombardment at the layer interfaces to increase. These traps can lead to the enhancement of the device by improving the trapping effects (Kim et al., 2003).

B. Device Spacer Layer

The use of AlN spacer layer at the interface of AlGaN barrier and GaN channel is studied. It is reported that the implementation of AlN can reduce the strain along the interface (Shrestha et al., 2013) while improving the lattice of AlGaN barrier layer. In this section, the insertion of AlN spacer layer at the AlGaN/GaN interfaces in Structure 2 is to improve the electron mobility from the previous structure.

TABLE 2
SIMULATED RESULTS OF DC CHARACTERISTICS FOR ALL HFET STRUCTURES

Structure	Figure of Merits (FOMs)			
	$\|V_{th}\|$ (V)	I_{on} (A/mm)	R_{on} (mΩ)	R_{out} (mΩ)
Conventional	3.509	1.944	2.588	616.2
Structure 1	6.208	3.288	2.294	226.8
Structure 2	8.368	4.014	2.219	40.19
Structure 3	8.415	4.035	2.202	38.69
p-GaN gate, DHFET (Binder et al., 2018)	-	-	<10.0	-
AlGaN/GaN CG-HEMT	-	-	9-11.5	-

The I_d-V_d curves (see Fig 2(b)) depict improvement as it increases significantly as compared to Structure 1. Study from Fig 2(b) shows the peak current density for graded barrier of Structure 2 can achieve up to 4.02 A/mm which increases by 22% compared to Structure 1 at V_{gs} = +2V. Similar trend is observed in the transfer characteristics in Fig. 3 which indicates improvement with the insertion of AlN spacer layer at the heterointerfaces. This is strongly related to the increment of mobility caused by the lowering of alloy scattering (Shrestha et al., 2013, Roy et al., 2015). The improvement in electron density and mobility is owed to the higher quantum well depth which in turn lowers the alloy scattering with the implementation of binary compound such as AlN (Jena et al., 2001). The AlN material is introduced as the interfacial layer is to enhance the mobility thus to indirectly increase electron concentration as well at low temperature. The concentration inside the channel layer is increased to $2.2x10^{18}$ cm^{-3} in Structure 2 and is shown in Fig. 4(b).

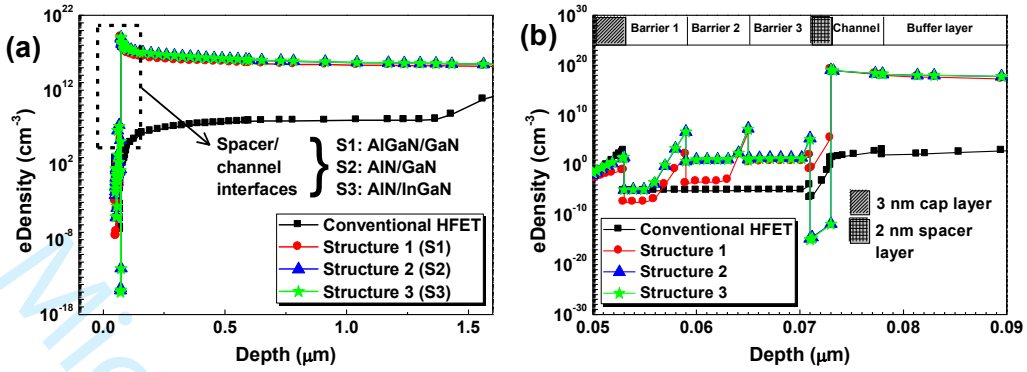

Fig. 4. (a) Electron density (cm^{-3}) for conventional HFET, as well as Structure 1-3 along device depth (μm). (b) Closer visual focusing on the density at the interfaces from the depth of 0.05 μm to 0.09 μm.

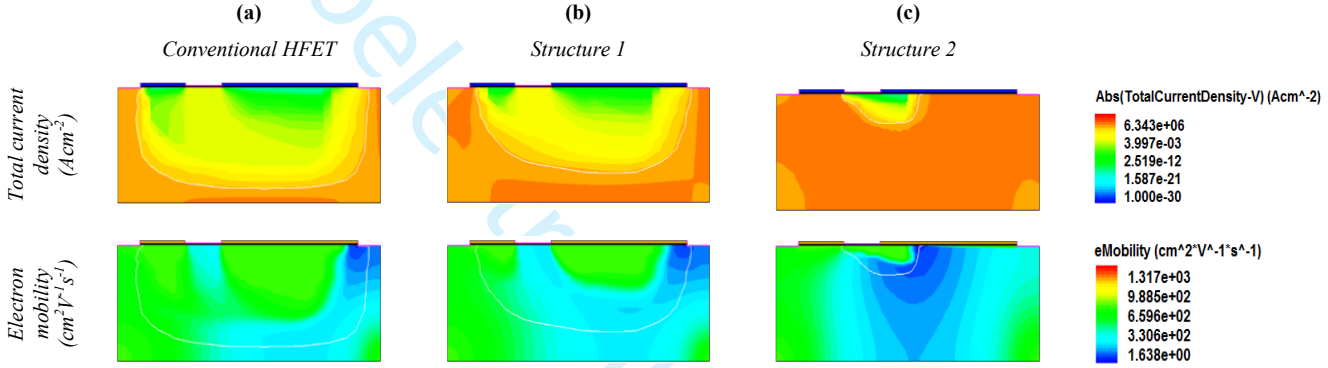

Fig. 5. Total current density and electron mobility for (a) conventional HFET; (b) Structure 1; and (c) Structure 2.

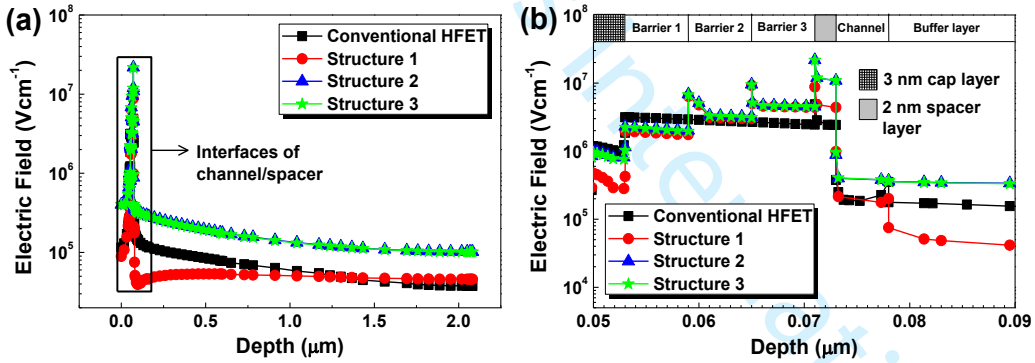

Fig. 6. (a) Electric field (Vcm^{-1}) for conventional HFET, as well as Structure 1-3 along device depth (μm). (b) Closer visual focusing on the field at the interfaces from the depth of 0.05 μm to 0.09 μm.

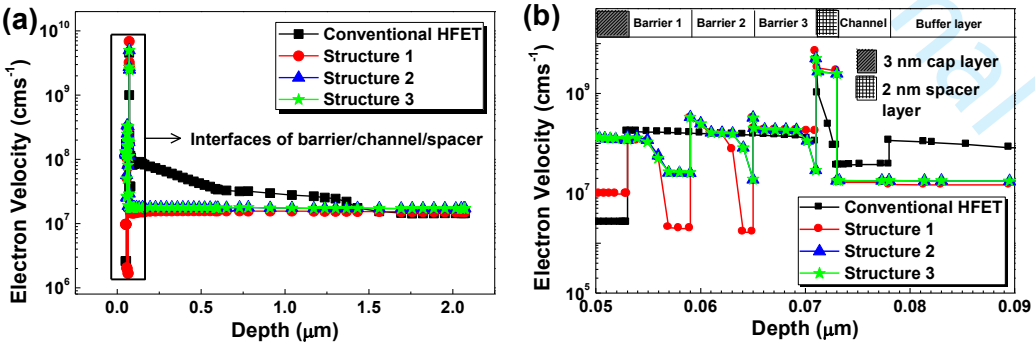

Fig. 7. (a) Electron velocity (cms^{-1}) for conventional HFET, as well as Structure 1-3 along device depth (μm). (b) Closer visual focusing on the velocity at the interfaces from the depth of 0.05 μm to 0.09 μm.

Apparently, AlN spacer layer gives an impact to the carrier transport, thus enhancing the carrier confinement (Shrestha et al., 2014). Analysing Fig. 4(b), the potential offset at the spacer/channel interfaces is improved with the insertion of AlN. This potential differences occurred owing to the polarization field (Keller et al., 2002) as shown in Eq. (1) (Lenka and Panda, 2011) where ΔE_c^2 and ΔE_c^1 are the effective conduction band offsets between the interfaces in Structure 2 and the Structure 1, respectively; N_{2D} is the sheet carrier concentration of Structure 2, ε_2 is dielectric constant, σ_2 is the polarization induced charge at the heterointerfaces of Structure 2, and t_b is the thickness of barrier. The effective Schottky barrier of the quaternary structure will also increase with the presence of AlN spacer barrier, which eventually reduces the device leakage (Brazzini et al., 2013).

$$\Delta E_c^2 - \Delta E_c^1 = \exp\left(\frac{\sigma_2 - N_{2D}}{\varepsilon_2}\right) t_b \qquad (1)$$

Fig. 5(c) suggests that with the insertion of AlN interfacial layer at the AlGaN/GaN heterointerfaces, the magnitude of electron mobility is improved particularly below the gate region. The electron mobility is observed to increase from 1102 $cm^2V^{-1}s^{-1}$ in Structure 1 to 1317 $cm^2V^{-1}s^{-1}$ in Structure 2. This raise in mobility is highly related to the reduction of alloy scattering with the presence of AlN as the spacer layer (Shrestha et al., 2014). The insertion of AlN spacer layer can also reduce the forward Schottky gate current (Nanjo et al., 2011) which can be attributed to the increased band discontinuity at the heterointerface due to enhanced polarization effects. This enables high gate voltage application for transistor operation. By combining the design structure of step-grading AlGaN barrier and insertion of AlN interfacial spacer layer at the heterointerfaces, the device performance has improved significantly. A high quality of AlGaN/AlN/GaN HFET with uniform structure is acquired with improved electron mobility as well as surface lattice arrangements as compared to the conventional structure. However, for graded structures, the total strain inside the barrier will decrease due to the reduction in lattice mismatch between AlGaN and AlN configurations, hence reducing lattice strain. Despite having low strain inside the layer, significant improvements can be observed in terms of 2DEG concentrations and electron mobility for the step-graded structure device incorporated with AlN spacer layer in between AlGaN and GaN interfaces. Fig. 5(c) indicates that there is sufficient reduction in the current density at below the gate region. Buffer leakages are expected to suppress apart from reduction in channel; this may also be due to reduction in electric field as shown in Fig. 6. Despite having higher electric field at the spacer/channel interfaces, Structure 2 has higher drop ranges of electric field compared to Structure 1. The electric field drops in about $9.8x10^6$ Vcm^{-1} at the spacer and channel interfaces for Structure 2 compared to Structure 1 with $3.38x10^6$ Vcm^{-1}. Fig. 7 illustrates the electron velocity of Structure 1-3 compared to the conventional HFET. It is quite promising for Structure 1 as the carrier have accelerated at the AlGaN/GaN interfaces compared to conventional design from 9.04 $x10^7$ cms^{-1} to 2.82 $x10^9$ cms^{-1}. However, the magnitude dropped to 1.66 $x10^7$ cms^{-1} in the channel region and to 1.49 $x10^7$ cms^{-1} in the buffer region.

This design improvement can lead to higher cut-off frequency and better RF improvement. On the contrary in Structure 2, the velocity is constant at the interface and is lower in the channel region compared to previous design although it increases towards the bottom of the buffer region from 1.46 $x10^7$ cms^{-1} to 1.72 $x10^7$ cms^{-1}.

C. Device Channel Layer

InGaN compound has been widely used as the channel material due to their lower band gap, which can enhance the high frequency characteristics and to prevent current collapse (Lenka et al., 2013, Zhang et al., 2016, Zhang et al., 2015). In this part, the structure design is improved, where the GaN channel is replaced to InGaN compound. It is observed that the output I-V characteristics for Structure 3 in Fig. 2(c) has shown slight improvement by which the current is increased by 2% at V_{gs} = -2V compared to the previous design (Structure 2). The inset of Fig. 3(a) illustrates the similar trend of transfer characteristics for Structure 3 compared to Structure 2. Narrower band gap in the InGaN channel device will increase the quantum well depth. Studying the carrier density behavior in Fig. 7, the results shows that the carrier density at the spacer/channel interface for Structure 3 is slightly higher compared to Structure 2. The implementation of the InGaN channel can improve the carrier confinement in the channel. This behavior is thus suggesting that InGaN channel devices are better in extinguishing the 1/f noise as well as radio frequency current collapse. InGaN is also well-known with their relatively low electron effective mass, hence leading to higher carrier velocity. It has been observed that the carrier transport in Structure 3 is higher compared to Structure 2, where the velocity is increased by $13.9x10^3$ cms^{-1}. This is expected due to the fact that carriers in InGaN are causing the velocity to increase, thus increasing the cut-off frequency for high performance devices. The interface between InGaN channel layer and GaN buffer layer will produce compressive strain in the channel. This will reduce the buffer leakage and can lead to improved 2DEG mobility. Table 2 shows the tabulated DC data for all structures simulated in this work. The results show that Structure 3 from this work has lower on-resistance (R_{on}) compared to other optimized designs in (Binder et al., 2018) and (Sun et al., 2017), respectively. The piezoelectric polarization in the InGaN layer is opposite to the AlGaN layer, which will result in the increase of the conduction band below the channel (Davydov, 2015, Park, 2003). Theoretically, high conduction band channel will results in higher band gap energy (Chow et al., 2017). In wide bandgap semiconductors, the breakdown voltage is improved and this will lead to the enhancement of buffer leakage current (Wang et al., 2017).

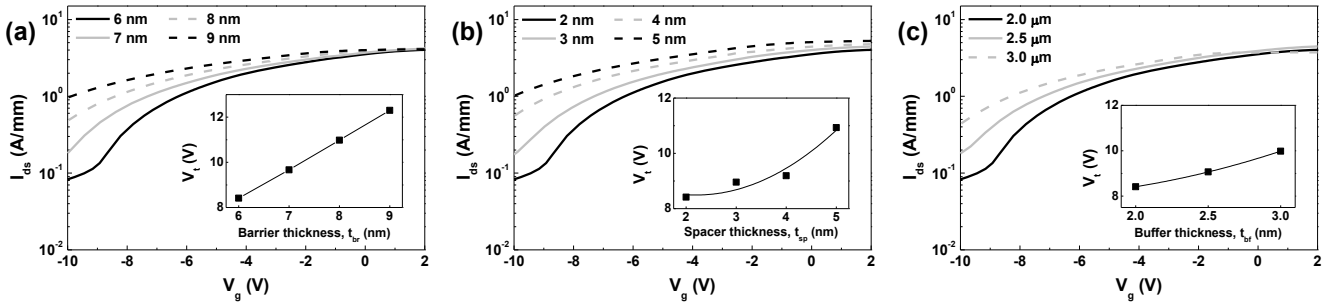

Fig. 8. Transfer characteristics at V_{ds} of 36V for various (a) barrier thickness, t_{br}; (b) spacer thickness, t_{sp}; and (c) buffer thickness, t_{bf} of the final structure (Structure 3). Inset: extracted V_t with respect to t_{br}, t_{sp}, and t_{bf}, respectively.

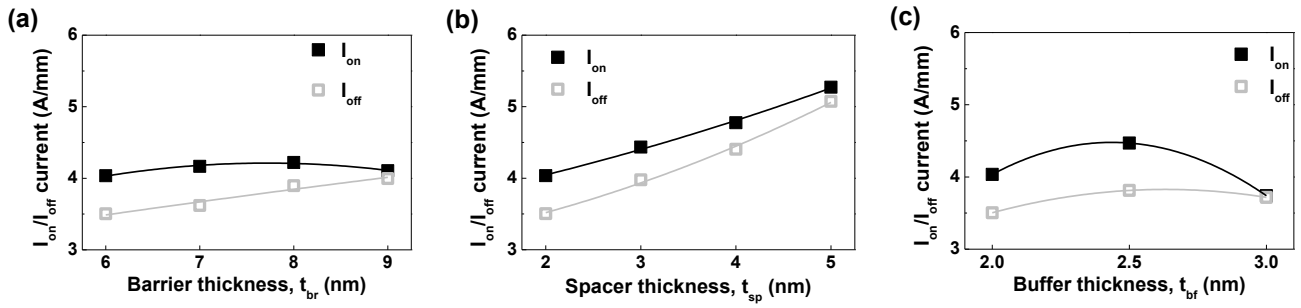

Fig. 9. I_{on} and I_{off} at V_{ds} = 36V with respect to t_{br}, t_{sp}, and t_{bf}

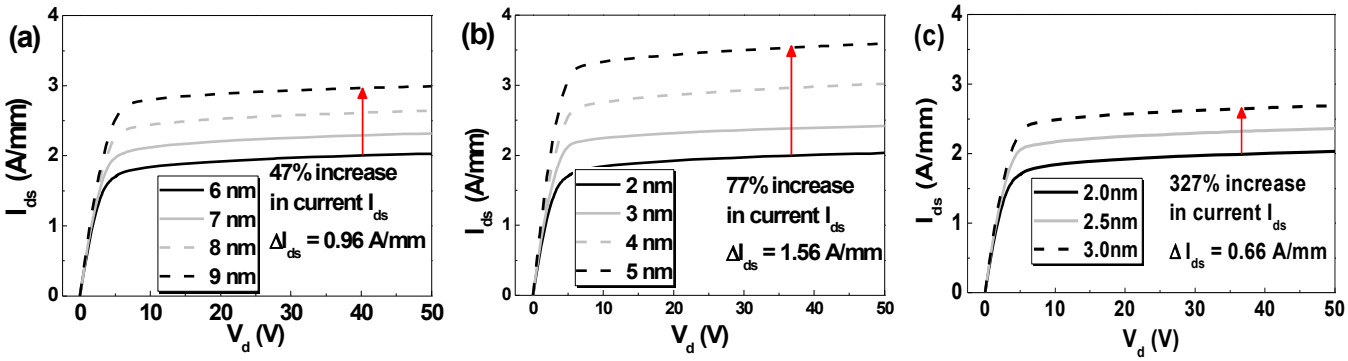

Fig. 10. Output characteristics at V_{gs} of 2V for various (a) barrier thickness, t_{br}; (b) spacer thickness, t_{sp}; and (c) buffer thickness, t_{bf} of the final structure

IV. GEOMETRIC DESIGN CONSIDERATION

The investigation is furthered by studying the impact of geometrical variation of the optimized design of HFET on I_d-V_g (see Fig. 8) and I_d-V_d (see Fig. 10). The impact of step-graded AlGaN barrier layer thickness (t_{br}), AlN interfacial spacer thickness (t_{sp}), and GaN buffer thickness (t_{bf}) variation is analyzed. For this section, the optimized design of Structure 3 is used as the device under test. Fig. 8 presents the scaling effects of t_{br}, t_{sp}, and t_{bf} on the transfer characteristics of the device. From I_d-V_g curves, it is observed in Fig. 8(a) that the on-current performance degrades as the barrier thickness decrease. Device barrier of 9 nm concedes 1 A/mm turn-on current which reduces to 0.1 A/mm when 6 nm barrier is employed. However, smaller thickness exhibits smaller threshold voltage, which can improve the switching speed of the device (Binder et al., 2018). V_{th} of 12.2 V and 8.2 V has been observed for 9 nm and 6 nm barrier layer indicating an almost linear variation. Similar trends are observed when the t_{sp} and t_{br} is varied in terms of threshold voltage, where each is varied from 2 nm to 5 nm and from 2 µm to 3 µm, respectively. However, spacer layer thickness revealed a non-linear variation with V_{th}. It can be noted that the rate of increase of V_{th} with t_{bf} is lower as compared with t_{br}. The DC output characteristics are illustrated in Fig. 10. For output characteristics, the current is enhanced by 77% when the thickness of AlN interfacial spacer layer is increased from 2 nm to 5 nm as shown in Fig. 10(b). This may suggest the device is significantly affected by the carriers in the spacer layer thus the increase in current. The buffer of the device on the other hand has less impact to the device performance as shown in the small change in the current level relative to the variation observed in the spacer. Note that from Fig. 11, the current density under the gate region is higher for 5 nm spacer

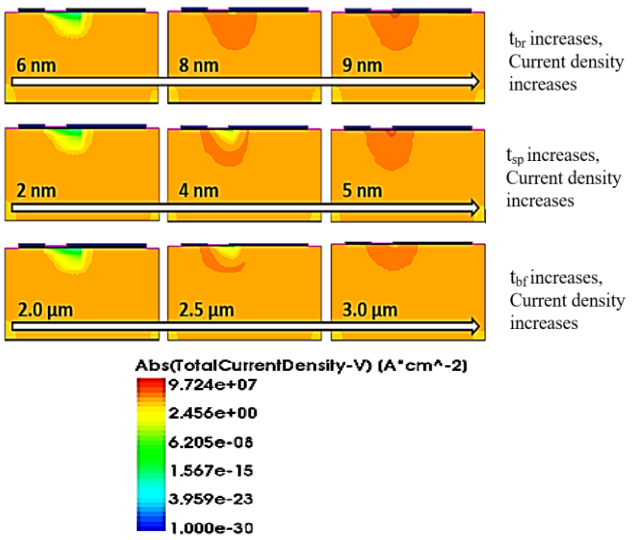

Fig. 11. Output characteristics at V_{gs} of 2V for various (a) barrier thickness, t_{br}; (b) spacer thickness, t_{sp}; and (c) buffer thickness, t_{bf} of the final structure

thickness, corresponding to the higher buffer leakage observed in Fig. 9(b). In higher thickness of AlN spacer layer, the conduction band off set is expected to increase, hence improving the 2DEG concentration level. In terms of buffer thickness, the 3 µm buffer thickness produces lower on current compared to 2 µm buffer thickness. However, by using the 2.5 µm thickness, the on current is enhanced despite the subsequent increase in the off current.

V. Conclusion

The specific electronic properties of an optimized design of a GaN-based HFET have been analyzed. The traditional AlGaN/GaN structure has been optimized in steps by scrutinizing the effects of barrier grading, concentration of mole fractions, spacer interlayer adoption and material selection of the channel. The electrical characteristics such as carrier densities, mobility and velocities are extracted. The optimized device design is studied for further geometrical variation impact. The final proposed structure consists of 1) step-graded barrier layer of three with equal thickness; 2) implementation of AlN as the interfacial spacer layer; and 3) replacing the conventional AlGaN channel with InGaN channel. This structure – AlGaN/AlN/InGaN, produces encouraging results in terms of mobility and 2DEG confinements. The threshold voltage, $|V_{th}|$ obtained for the AlGaN/AlN/InGaN HFET is 8.4V. The peak current achieved is 4.04A/mm with the on-state resistance of 2.2mΩ. The impact of geometrical variation shows that the drive current is improved by increasing the thickness of the barrier, and spacer layer despite having a trade-off to higher buffer leakage. On the contrary, reducing the thickness can lead to mobility enhancement, hence improving the device performance.

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