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Gerador de forma de onda arbitrária para SDR

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(Waveform Generator for Software Defined Radio)

Dissertação apresentada à Universidade de Aveiro para cumprimento dos requesitos necessários à obtenção do grau de Mestre em Engenharia Electrónica e Telecomunicações, realizada sob a orientação científica do Dr. Nuno Borges Carvalho, Professor associado com agregação do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro.

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Palavras-chave SDR, Software Defined Radio, Arbitrary Waveform Generator, Stimulus Signal

Resumo

Esta dissertação insere-se na área de electrónica de rádio frequência, mais concretamente na geração de sinal para caracterizar sistemas com a arquitectura Software Defined Radio (SDR).

Esta arquitectura tem como conceito a definição de um rádio completamente ajustável por software, através de conversão de blocos de domínio analgico para digital. Atendendo à importância que as novas tecnologias têm nos dias de hoje, os sistemas SDR aparecem como uma solução, uma vez que tendem a diminuir a parte de hardware, aproximando a conversão para o domínio digital cada vez mais próxima da antena.

Neste trabalho propõem-se duas implementações, um gerador CW (Continuous Wave) que tem como funções estimular um dispositivo sobre teste e ainda de actuar como oscilador local. A outra implementação assemelhando-se com a arquitectura de um gerador AWG (Arbitrary Waveform Generator) que terá como função originar dois tons para estimular um dispositivo sobre teste. A gama de frequências encontra-se entre os 40 e 1000 MHz.

Keywords SDR, Software Defined Radio, Arbitrary Waveform Generator, Stimulus Signal

Abstract

This dissertation is inserted into the area of radio frequency electronics, specifically in signal generation to characterize systems with Software Defined Radio (SDR) architecture.

This architecture has like a concept defining a radio completely adjustable by software, by converting blocks of the analog domain to the digital domain. This architecture has like a concept defining a radio completely adjustable by software, by converting blocks of the analog domain to the digital domain. Considering the importance that new technologies have nowadays, SDR systems appear as a solution since they tend to reduce the hardware part by approximating the conversion to the digital domain closer and closer to the antenna.

In this work, two implementations are proposed, one is a CW (Continuous Wave) generator which has the function to stimulate a device under test and also to act as a local oscillator. In the other implementation, that has a similar architecture of an AWG (Arbitrary Waveform Generator) generator has as function generating two tones to stimulate a device under test.

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List of Acronyms

1G First Generation

2G Second Generation

2.5G Second and Half Generation

3G Third Generation

4G Fourth Generation

ADC Analog-to-Digital Converter

ACPR Adjacent Channel Power Ratio

ADS Advanced Design System

AM Amplitude Modulation

AMPS Advanced Mobile Phone System

AWG Arbitrary Waveform Generator

BB Baseband

BPF Band-Pass Filter

BW Bandwidth

CCDF Complementary Cumulative Distribution Function

CDF Cumulative Distribution Function

CMOS Complementary Metal Oxide Semiconductor

CW Continuous Wave

DAC Digital-to-Analog Converter

DC Direct Current

DDS Direct Digital Synthesis

DET Departamento de Electrnica e Telecomunicações

DFT Discrete Fourier Transform

DIP Dual In-line Package

DSP Digital Signal Processor

DUT Device Under Test

ECL Emitter-Coupled Logic

EVM Evaluation Module

FFT Fast Fourier Transform

FM Frequency Modulation

FPGA Field Programmable Gate Array

GPRS General Packet Radio Service

GSM Global System for Mobile Communications

HP Hewlett-Packard

I/Q In Phase/Quadrature

IC Integrated Circuit

IF Intermediate Frequency

IMD Intermodulation Distortion

IP_3 Third-order Intercept Point

IT Instituto de Telecomunicações

LA Logic Analyzer

LAN Local Area Network

LLP Leadless Leadframe Package

LNA Low Noise Amplifier

LO Local Oscillator

LPF Low-Pass Filter

LSNA Large Signal Network Analyzer

LVCMOS Low-Voltage Complementary Metal Oxide Semiconductor

LTE Long Term Evolution

MDO Mixed Domain Oscilloscope

MSO Mixed Signal Oscilloscope

MSPS Mega-Samples Per Second

NBGN Narrow Band Gaussian Noise

NC No Connection

OCXO Oven Controlled Oscillator

PA Power Amplifier

PAPR Peak-to-Average Power Ratio

PCB Printed Circuit Board

pdf Probability Density Function

PECL Positive Emitter-Coupled Logic

PG Pattern Generator

PLL Phase-Locked Loop

PSD Power Spectral Density

QFN Quad-Flat No-leads

QoS Quality of Service

R&S Rohde & Schwarz

RF Radio Frequency

RBW Resolution Bandwidth

RL Return Loss

SDR Software Defined Radio

SMA Sub-Miniature version A

SMD Surface Mount Device

SMS Short Message Service

SPI Serial Peripheral Interface

SOIC Small-Outline Integrated Circuit

SSB Single Side-Band

TCXO Thermal Compensated Oscillator

TDD Time Division Duplex

TI Texas Instruments

TSSOP Thin-Shrink Small Outline Package

TTL Transistor Transistor Logic

UART Universal Asynchronous Receiver/Transmitter

UMTS Universal Mobile Telecommunications System

USB Universal Serial Bus

VBW Video Bandwidth

VCO Voltage Controlled Oscillator

VNA Vector Network Analyzer

VSA Vector Signal Analyzer

Chapter 1

Introduction

The history of radio communications started in the 1860s, when a Scottish physicist, James Clerk Maxwell, predicted the existence of radio waves. Then in 1886 Heinrich Rudolph Hertz, German physicist, verified that fast variations of electric current could be projected to the space in the form of radio waves. With these achievements, a lot of discoveries occurred and a disputed of who invented the radio (which in that time was named "wireless telegraphy") began. In 1895, Guglielmo Marconi, an Italian inventor, proved the possibility of radio communication by sending and receiving his first radio signal but one of Marconis contemporary, Nikola Tesla, Serbian-American inventor, two years earlier, in 1893, also has demonstrated the wireless telegraphy attested with two patents [3, 4], the Supreme Court overturned Marconi's patent in 1943 in favor of Tesla[1, 2].

After these achievements, a constant evolution of the wireless communications systems has began, first with the Amplitude-Modulated (AM) broadcast radios and later the Frequency-Modulated (FM) broadcast radios that have improved the quality of radio transmissions. All these results were important, but the biggest revolutionary technology to the wireless world was the cell phone. This technology started with the Advanced Mobile Phone System (AMPS) in 1980s and was recognized as first generation (1G) communication. In this generation (1G), the systems only allowed voice data transfer, the networks were only analog, so the system had big limitations. This Generation did not support any kind of encryption (safety problems), sound quality was poor and data rate was about 9.6 Kbps. Even with several problems, it did not stop the mobile phone market growth, from 30 to 50 percent annually and the number of subscribers in the world reached around 20 million by 1990 [5].

The second generation system (2G) appeared around 1990. The main idea was to solve the problem of 1G. These 2G systems are fully digital which brings advantages like safety, reliability and one important, efficient spectral usage. One of the second generation systems is the GSM (Global System for Mobile communications), which uses digital modulation to improve voice quality but the network still has limited data service. Also 2G brought the SMS (Short Message Service). In the late 1990s, an intermediary phase between the 2G and 3G appeared, 2.5G, which introduced the General packet radio service (GPRS) that allowed the packet-switched data capabilities to existing GSM networks [5].

The mobile technology 3G, third generation, has like a purpose supporting a wide band of services like audio, data and video. 3G cellular services also recognized as Universal Mobile Telecommunications System (UMTS), offers higher data rates and to Internet applications. This technology supports packet and circuit switched data transmission. UMTS delivers the

first possibility of global roaming, with possible access to the Internet from any place [5].

The present generation of mobile communications, 4G, fourth generation has been developed to improve the previous generation. A higher transmission rate (20 Mbps), higher bandwidth, better Quality of Service (QoS) are all guaranteed in comparison to 3G. Technologies like LTE (Long Term Evolution) and Mobile WiMAX were introduced in the market in 2006, but they have becoming known as 4G technologies. It is possible to conclude that 4G is a set of wireless standards, than can be efficiently realized using Software defined Radio (SDR) technology [5].

In 1995, J.Mitola introduced the concept of SDR. The idea proposed was to produce a radio that is fully adjustable by software, adapting the radio to several communication systems. Quoting Mr. Mitola, *"A software radio is a radio whose channel modulation waveforms are defined in software. That is, waveforms are generated as sampled digital signals, converted from digital to analog via a wideband DAC and then possibly upconverted from IF to RF. The receiver, similarly, employs a wideband ADC that captures all of the channels of the software radio node. The receiver then extracts, downconverts and demodulates the channel waveform using software on a general purpose processor"*. Resuming, the SDR has as main goal to push the ADC/DAC as close as possible to the antenna. This has like a result, fewer signals will exist on the Analog domain, and the measurement of digital signals takes on a level of significance not found in traditional analog RF system characterization [6].

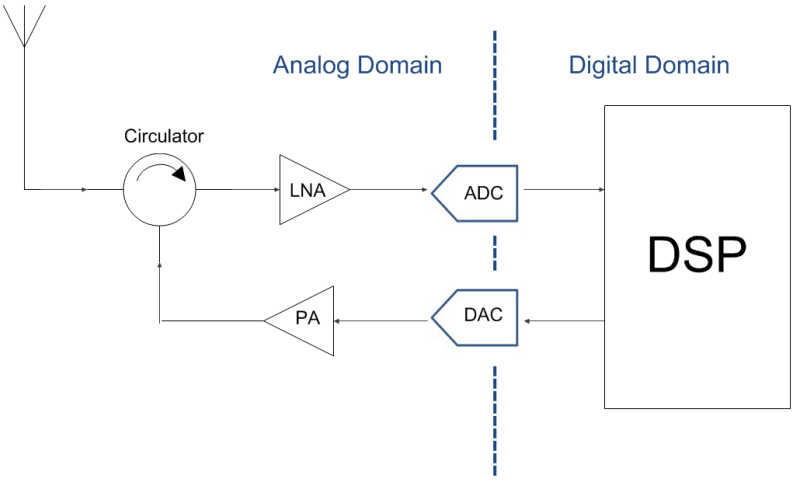

Figure 1.1: Ideal SDR Architecture

1.1 Motivation

Nowadays, wherever we are, whatever we do, we are always get in touch with current communication systems like mobile phone (a term that is becoming to disappear because of the growth of the smart phones), television, radio and principally internet. All these systems are becoming more wireless and digital, the importance of the digital domain is increasing but the analog domain stills necessary. However the wireless communication industry still has a lot of challenges to resolve to implement a global wireless network, where the SDR can also have an important role as a solution for the problems and challenges. For example the next

figure represents the results of study in 2011 that evaluate the adoption of SDR technologies in various markets.

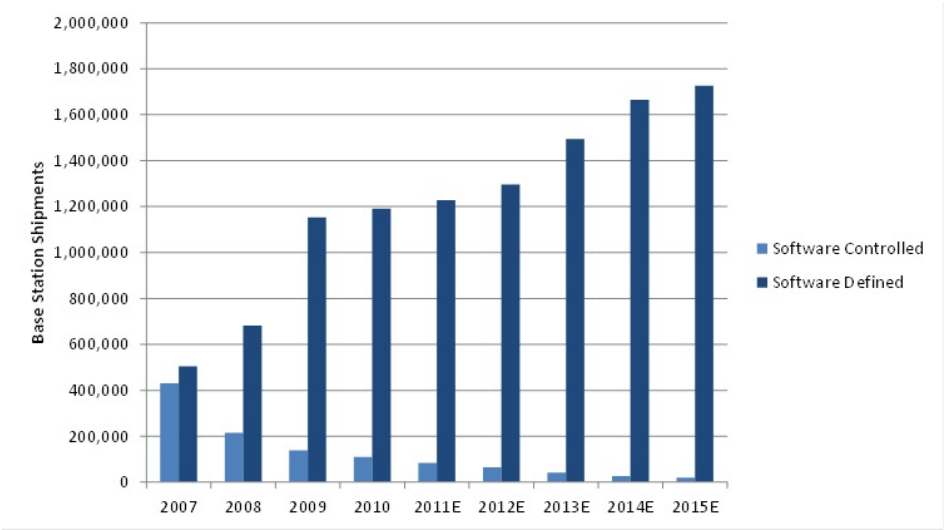

Figure 1.2: Adoption of SDR in various markets[7]

The typical SDR front end can execute different functions at distinctive times and the reconfiguration of the terminal can be done by software, for instance this ability facilitates the roaming from region to region. The reconfiguration by software makes a much easier and cost advantage (no need of a new hardware module). The key elements in SDR architectures are the ADC (Analog-to-Digital Converter) and DAC (Digital-to-Analog Converter), which can be considered as mixed-domain devices. The instrumentation industry has failed to characterize these kinds of components in a fast and simple way.

Having as a background the M.Sc. Diogo Ribeiro work [8], which is a solution to solve the problem described in the last paragraph, the objective of this dissertation is to build local a Continuous Wave (CW) Generator and an Arbitrary Waveform Generator (AWG), which can replace the external signals generators used in Diogo's thesis. The CW generator will act as stimulus signal for the DUT and as Local Oscillator in the IF stage. The AWG has to generate a two-tone signal to excite the DUT. The next section will provide more information about Diogo's work and the signals generators that are going to be replaced are present on figure 1.4.

To put the work to be developed in context with Diogo's work, the R&S SMU200A needs to be replaced by signal generators that have to produce:

- One tone signal(single sinusoid) and Two tone signal(two sinusoids);
- Output power close to 0 dBm;
- Frequency range, 40 MHz to 1000 MHz;
- Low cost implementation.

The R&S SMR40 needs to be replaced by signal generator that has to produce:

- One tone signal, single sinusoid;

- Output power close to 10 dBm;
- Frequency range, 40 MHz to 1000 MHz;
- Low cost implementation.

1.2 Analog-Digital Measurement System for Software-Defined Radios

The Analog-Digital Measurement System for Software-Defined Radios was projected developed by Diogo Ribeiro and supervised by Pedro Cruz and Nuno Borges Carvalho. This project had like a goal, a fast and simple way to test a SDR or a mixed-domain component which has been until today a gap from the instrumentation industry. More precisely, the idea was to built an instrument capable of doing the desired goal, characterize a mixed-domain component [8].

An instrument that is the close to the implemented one is the VNA, Vector Network Analyzer, which characterizes a component in frequency, only in the analog domain. So the architecture of the mixed-domain instrument is close to the VNA architecture (figure 1.3).

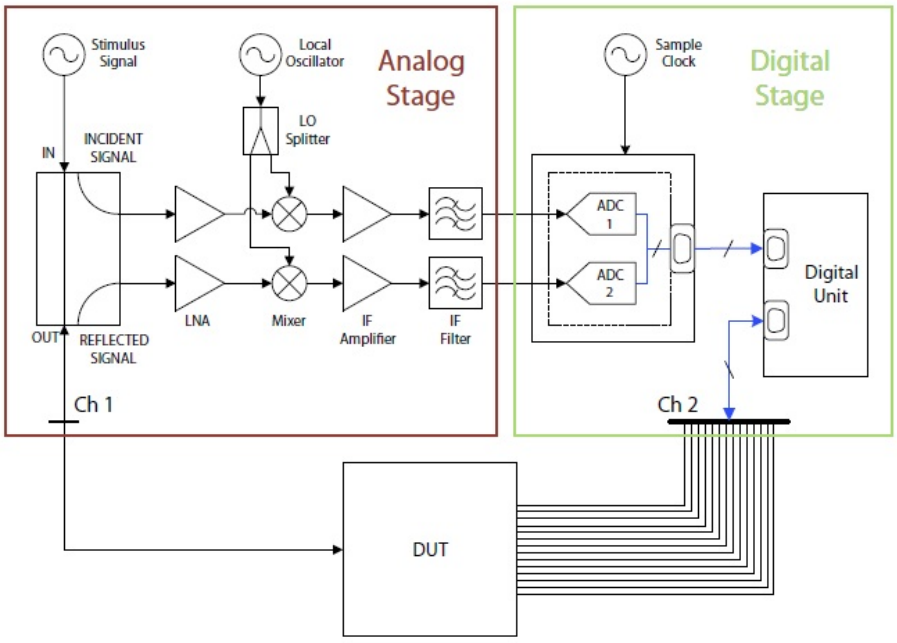

Figure 1.3: Mixed-Domain Instrument Architecture [8]

To characterize a mixed-domain component, for example an ADC (Analog-to-Digital Converter), where the port 1 is analog and the port 2 is digital, it is interesting to measure quantities like $S_{11}(\omega)$ and $S_{21}(\omega)$. The $S_{11}(\omega)$ represents the reflections on port 1, $S_{21}(\omega)$ the gain of the DUT. Other parameters like $S_{22}(\omega)$ and $S_{12}(\omega)$ are considered zero. [8]

The traditional VNA front-end architecture was implemented to the instrument's analog port and the Logic Analyzer like front-end to the digital port, the final system arrangement is presented in the next page.

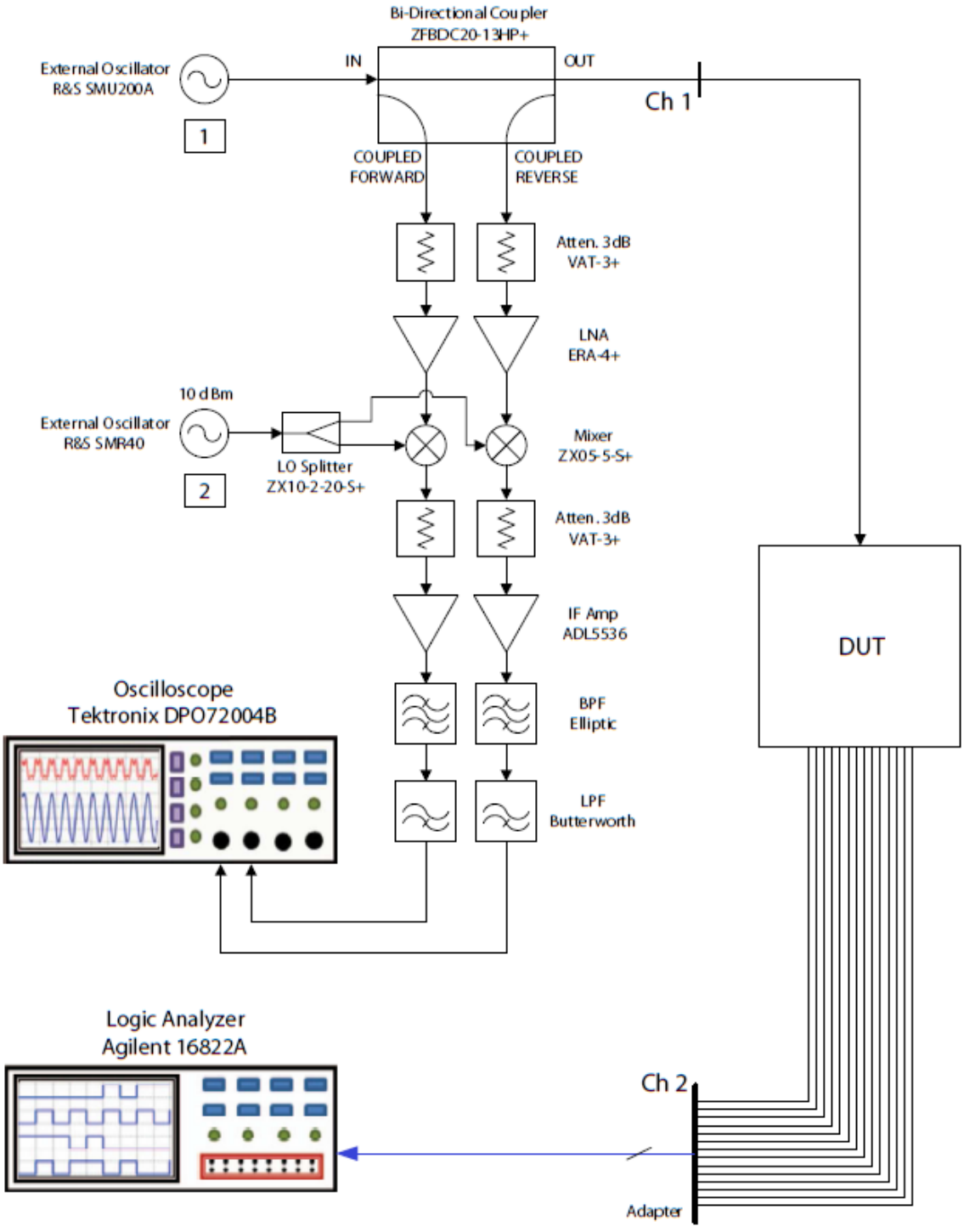

Figure 1.4: Final System Arrangement [8]

1.3 Document overview

This dissertation is organized into **six chapters**, where some chapters are divided in sections and subsections, which can be solutions or steps to accomplish the desired system. In the beginning of the chapters, a small explanation of the content of the section is described and at the end a conclusion.

In **Chapter 1** an introduction about the communications evolution is made from their initial times to the present times. After the introduction, the motivation for this master thesis is provided. To understand more why this project, a previous work is presented. **Chapter 2**, State of Art, presents an overview about the signal generators and the kinds of stimulus signals. The architectures of these machines are analyzed. Then, in **Chapter 3**, the CW Generator implementation is presented. There are two sections, with two solutions developed, each section refer to a solution. In **Chapter 4**, the Arbitrary Waveform Generator design and conception is obtainable. Here each sub-chapter refers to a block, in the block diagram available on figure number xx. All the problems and solutions are well presented in this chapter. Further, **Chapter 5** shows the results acquired with all system integrated. All the important measures are presented in the figures. At last, **Chapter 6** presents several conclusions and suggestions for future work.

Chapter 2

State of the art

In the previous chapter, the desired goals of this project were presented, implementation of Continuous Wave, which acts as local oscillator and stimulus and Arbitrary Waveform Generators that act as stimulus signal. Both generators will act as stimulus signals and these signals, for example, are used to produce the figures of merit present in every datasheet. The figures referred symbolize the electronic devices specifications and they are very important to the manufacturers. A particle example can be a power amplifier: gain, efficiency and non-linear distortion are all significant figures of merit. To accomplish these figures characterization procedures are used, the stimulus signal work as an input signal to excite the device under test [9].

The objective of this chapter is to get know-how to implement the desired goals of this project. In order to achieve the main objective, several background concepts about Signal Stimulus are introduced. Different kinds of these signals and how to generate them will be studied.

To start, the basic kind of stimulus signal will be studied, the one tone stimulus, which in this project will be the signal produced by the CW Generator. This kind of signal is useful in linear systems to obtain several figures of merit like noise figure and bandwidth for example. In these systems, the superposition laws are applicable, the extension of the figures of merit to other kinds of excitation is valid, so it is common that in linear systems the figures of merit are obtained by using one tone stimulus, than easily extrapolated to other forms of stimulus [9].

For non-linear systems the extrapolation is not easy, in some cases it is impossible, the reason is obvious, non-linear systems do not obey to the superposition laws. Thus, the one tone stimulus is not enough to get all the main characteristics of a non-linear device. A different kind of excitation is needed so a new section is introduced, two tone stimulus which typically, this stimulus is used to measure non-linear distortion [9].

As expected the chapter becomes more complex, as it goes forward, the multi-sine stimulus is addressed after the two tone excitation. Multi-sine is very important, in spectral and time domains. Some special cares need to be taken in order to produce multi-sine stimulus.

Before ending this chapter, new kinds of stimulus signals will be presented, chirp signals for example. Also, the concepts about AWG will be presented, this generators have an important role in generating mechanisms.

In the end of this chapter, there is a conclusion where the ideas to achieve the desired goals of the project will be present, in order to resume the study developed in this chapter

and to facilitate the future work of this project.

2.1 One Tone Stimulus

The one tone stimulus or in other way a single sinusoid is the orthogonal base for Fourier series evaluation. For this reason this kind of stimulus is the favorite form to measure the steady state and spectrum contents. Linear systems are typically well characterized by this kind of excitation. The input one tone stimulus is given by the following equation:

$$x(t) = A_i * cos\,(2\pi f t)$$

The next figures present the one tone signal in time domain and frequency domain.

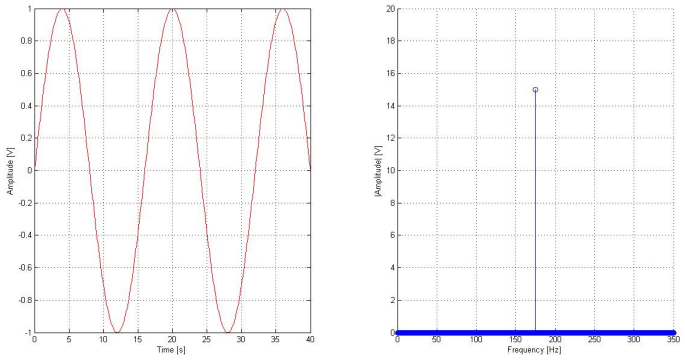

Figure 2.1: Single Sinusoid in time domain and frequency domain

This input has an amplitude A_i and a frequency f, usually denominated as fundamental frequency. In a linear system, the output will be at the same frequency, f, and because of being a linear system the output only changes in amplitude(A_o) and phase(θ), so it can be defined by

$$y(t) = A_o * cos\,(2\pi f t + \theta)$$

It is possible to extend this test to a nonlinear device under test but it becomes more complex. The A_o (output amplitude) will no longer be a scaled replica of the input level, A_i (input amplitude) and the relative phase, θ, will not only be determined by the frequency of the sinusoid. A_o and θ will nonlinearly vary with the stimulus signal level. The DUT will generate new components located at the harmonics of the input [9]. The following equation can represent in a convenient way the output of a nonlinear system, for a one tone excitation.

$$y(t) = \sum_{r=0}^{+\infty} A_{o_r}(2\pi f t, A_i) * cos\,[r \cdot 2\pi f t + \theta(2\pi f t, A_i)]$$

2.1.1 One Tone Generation Mechanisms

To generate one tone signals, different approaches can be done, since RF oscillators to direct digital synthesis (DDS) oscillator. These techniques will be further presented in this

chapter. There are several parameters that need to be considered to evaluate the quality of an RF sinusoid. The parameters of interest are phase noise, output power, frequency stability and others. Phase noise is a very important characteristic that determines the quality of an RF Signal, also it is very difficult parameter to control, a low value is fundamental for a good performance. Because of the importance of this parameter, a deeper explanation will be presented.

Phase Noise

It is always desired to place the total output power in the carrier, but that is unrealistic due to stochastic variation of the phase, thus dispersing the power to a finite frequency range. This power dispersion is named phase noise, and mathematically phase noised is treated as stochastic phase modulation of one of the side bands, i.e., SSB (single side-band phase noise). The SSB phase noise is measured in dBc/Hz units, thus implying that the measure in dB below the carrier magnitude is normalized to 1-Hz bandwidth [10].

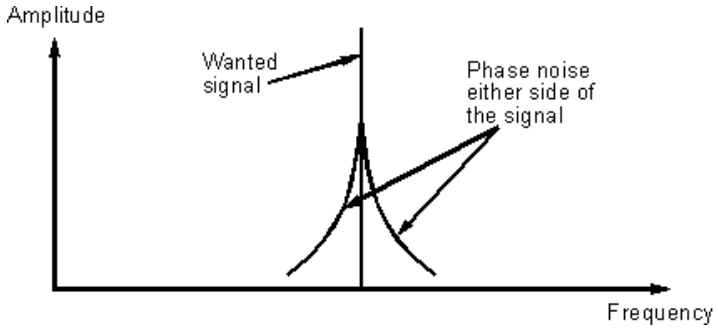

Figure 2.2: Phase Noise [11]

Usually in the datasheets, it is given the distance from the carrier for which the specification is valid, for example, -116 dBc/Hz, 20 KHz from carrier at 100 MHz.

In the next figure it is possible to observe the influence that phase noise can have. An interference signal is close the desired signal, the local oscillator has a high phase noise value, so the output desired signal can be corrupted by the interference signal.

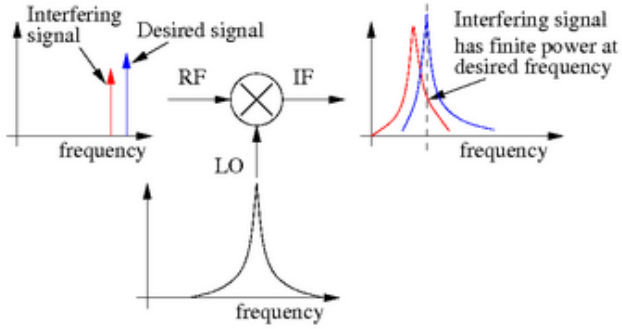

Figure 2.3: Phase Noise Interference Problem [12]

Returning to one tone generation mechanisms, a typical topology to generate one tone, is composed by three blocks, RF reference block, synthesizer block and output stage. To better understand, every block will be discussed individually.

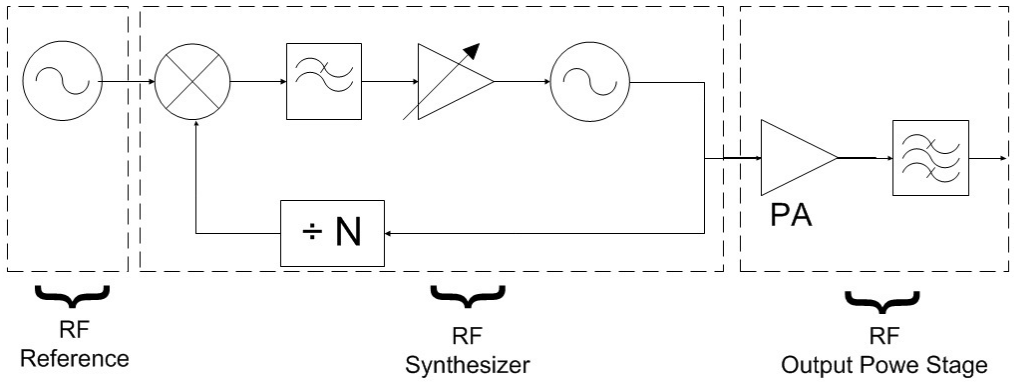

Figure 2.4: RF Generator Blocks

Reference Block

The first block of the chain is a simple reference signal, it can be made of a good oscillator, that typically it is produced by a quartz material, usually a crystal oscillator. These crystals are affected by parameters as aging, temperature and line voltage. Temperature is the parameter that affects more the degradation of the signal quality. To improve this characteristic, the crystal can be compensated in temperature by a Thermal Compensated Oscillator (TCXO) or by putting it in an oven or some similar controlled environment, in that situation it is named as Oven Controlled Oscillator (OCXO) [13].

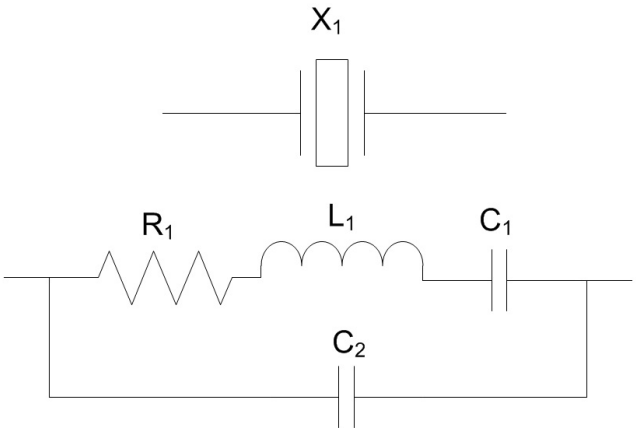

Figure 2.5: Typical Reference Crystal Oscillators

The Reference signal can also be external, for example coming from a signal generator. Usually in the back of the equipments is available a reference signal of 10 MHz that is useful to eliminate frequency deviation by providing this reference to all equipments used, for example signal generator and spectrum analyzer.

Synthesizer Block

The second block of the chain determines the output frequency and normally it is created by using a synthesizer. The most common synthesizers are based on the Phase Locked Loop (PLL) principle. The PLL are an easy way to create a synthesized sinusoidal oscillator, which the output frequency can be selected by using a digital keyword, usually done by digital dividers in the control loop.

The figure 2.6 presents a typical PLL configuration, the three main components are Phase detector (in fact it is a mixer), a Voltage Controlled Oscillator (VCO) and a frequency divider. The basic theory of operation is based on the fact that when the reference signal is mixed with the feedback signal it will create an output signal that will be filtered out by the low pass filter to eliminate the high frequency products, before being fed to the VCO. The low frequency voltage signal at the input of the VCO will put the VCO running at an RF frequency that will be further divided by the loop frequency divider. This process keeps going until the two signals at the mixer are at the same frequency and in phase which means that the output of the mixer will be a DC voltage. This voltage will then feed the VCO and thus the output will be maintained at a stable frequency, it is said that the PLL is locked. The filter bandwidth should be chosen in order to filter out any high value of frequency like previously said, but not as narrow band as possible, since in that case the PLL will not converge and will not lock for a high separation between frequencies. The value of the output frequency will then be determined using the loop frequency divider, where it is possible to choose a correct value for generating the RF frequency [14].

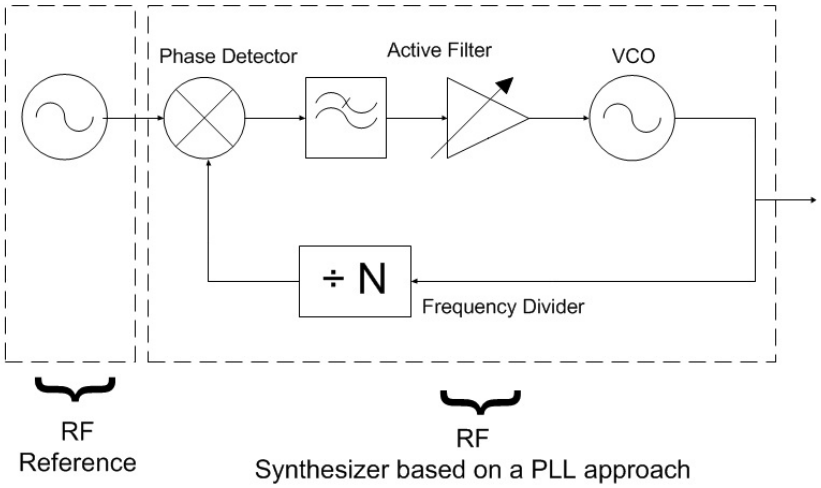

Figure 2.6: Ideal PLL Approach

For example, a reference signal 10 MHz, output signal 300 MHz. The frequency divider should be 300/10=30. This number is most of the time selected using a digital keyword, that is fed to the digital divider.

As said before, VCO is an important component or even can be the most important, it is the one which determines the output frequency. It can be produced from oscillators like Colpitts and Hartley. In these circuits, the oscillator frequency is in the most cases, controlled by changing the feedback loop using a capacitance that changes with voltage, a varicap for instance. To guarantee a good phase noise, special cares need to be taken [15].

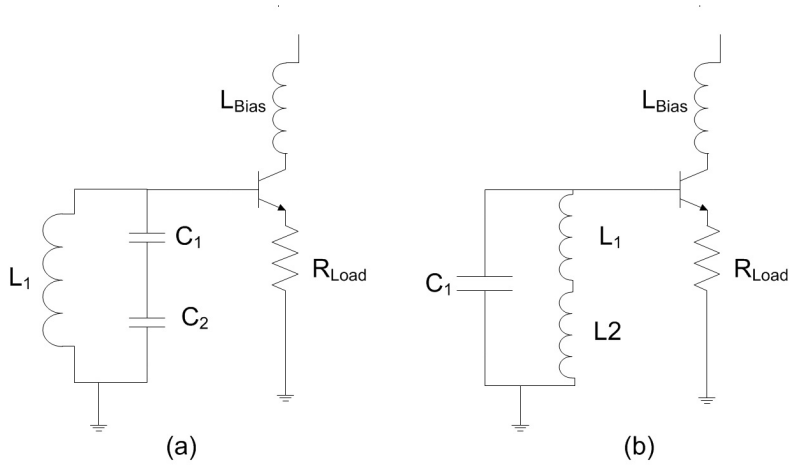

Figure 2.7: (a)Colpitts Configuration, (b)Hartley Configuration

Output Stage

This final block has like a purpose level up the signal and controls the output power. It can affect the signal since the output amplifier can operate in the nonlinear region, and so it will produce harmonics and spurious components that degrade the signal purity. This detail imposes that RF generators work at a value lesser than the maximum accessible. The modern kinds of these equipments present an uncal warning when reaching these points of operation [14].

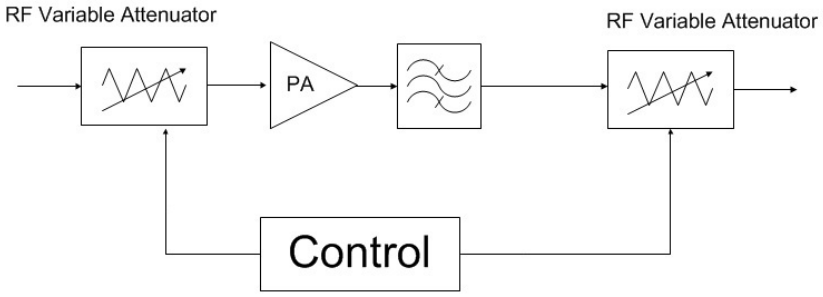

Figure 2.8: RF Output Stage

Direct Digital Synthesizer

An optional technique that is becoming more usage in RF signal generators is the Direct Digital Synthesizer, DDS. This technique enables very fine frequency increments to be achieved relatively easily. However the maximum limit of a DDS is normally much lower (commercially operate until 3 GHz at the moment) than the top frequencies required for the signal generator, so they are used in conjunction with phase locked loops to give the required frequency range [16].

To generate one tone signals a digital form of a sine wave is first uploaded by software to a memory (look-up table). This memory is then read by using a phase accumulator that will

traverse all the points with a pre-determined frequency. The read values will then be fed in a DAC (Digital to Analog Converter). Thus the frequency in this situation will be proportional to the speed at which the memory values are traversed. On the output it is necessary a band pass filter to assurance that the sine wave does not be similar to a DC stair case form, but that it is really a sine wave [16].

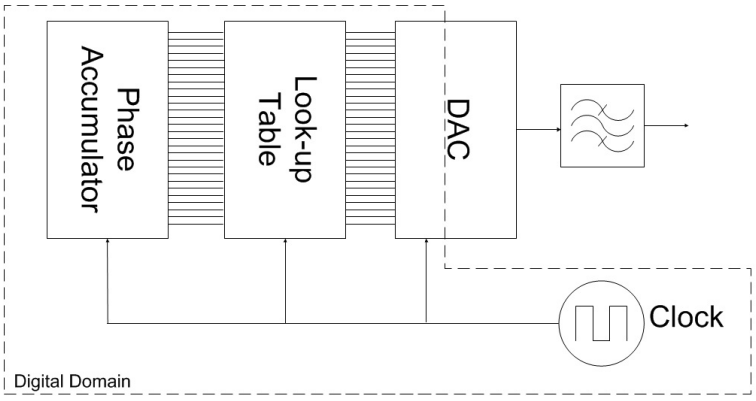

Figure 2.9: DDS Approach

2.2 Two Tone Stimulus

The previous characterization, one tone, is good enough to get most of all information of a linear. When nonlinear systems need to be characterized, this kind of characterization becomes poor, so a new signal is required. The two tone stimulus is a solution for this problem and it is an improved demonstration of true telecommunication signal excitations. The following equation describes the two tone signal:

$$x(t) = A_{i1}cos\left(2\pi f_1 t\right) + A_{i2}cos\left(2\pi f_2 t\right)$$

or

$$x(t) = A_{i1}cos\left(\omega_1 t\right) + A_{i2}cos\left(\omega_2 t\right)$$

where $\omega_x = 2\pi f_x$.

The two-tone signal is just a summation of two sinusoids that have different frequencies, the figure 2.10 presents an example of a two-tone signal in time domain and frequency domain.

In a nonlinear system stimulate by two-tone signal, it will product harmonics and other new components that appear close to the fundamental frequencies and close to the harmonics, named spectral regrowth, and close to DC named base-band components. [9] The output of a nonlinear device can be given by:

$$y(t) = \sum_{h=1}^{+\infty} A_{o_h} cos\left[\omega_{o_h} t + \theta_{o_h}\right]$$

where $\omega_h = m\omega_1 + n\omega_2$ and $m, n \in \mathbb{Z}$.

The output is composed by a lot of mixing terms, newly generated tones at $m\omega_1 + n\omega_2$.

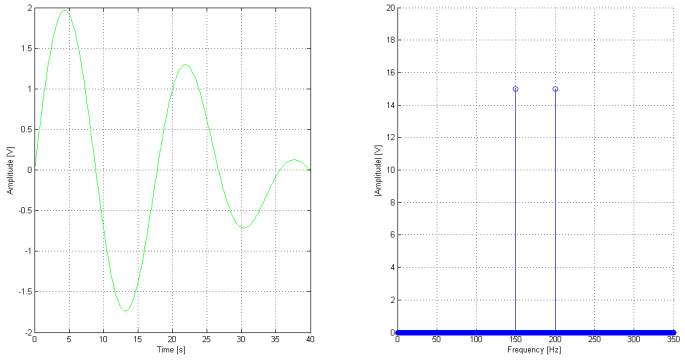

Figure 2.10: Example of Two Tone signal in time domain and frequency domain

2.2.1 Two Tone Generation Mechanisms

Like in the one tone mechanism, there are different ways to generate two tones. A simple method is to use two single sinusoid generators and combine them. The next figure illustrates this method.

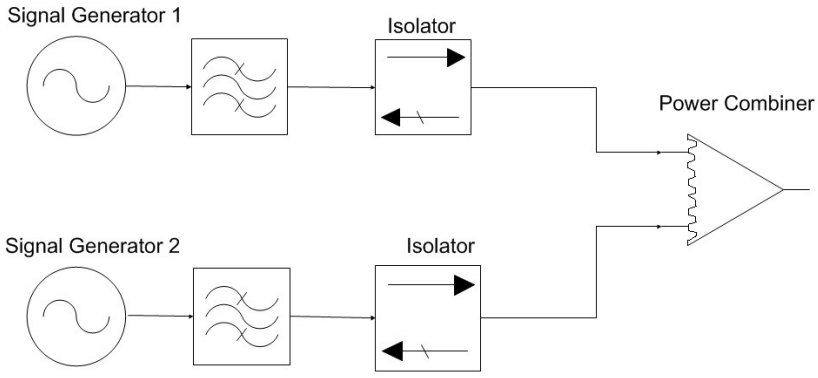

Figure 2.11: Example of Two-Tone signal setup

The RF Generators generate respectively each tone of the two tone equation, f_1 and f_2, i.e. RF Generator 1 is at f_1 and RF Generator 2 is at f_2. Then it is necessary to filter, to eliminate the harmonics produced by the generators in order to prevent interference. After the filter, an isolator needs to be place to reduce any signal that could possibly be reflected from the power combiner and consequently mix with the generated frequency, if some signal is reflected the measurement can be corrupted. Finally the signals are combined in the power combiner and the two-tone signal is created [9].

A DDS approach to generate two tones is also possible by using an Arbitrary Waveform Generator. The two tone signal will be loaded to a memory/look-up table and then is converted to the analog domain by a DAC. To up-convert the signal an IQ modulator is used. To better understand better how this generator works, an explanation will be done, but first let's take on count its architecture, the figure 2.12 presents the architecture of this kind of generators [17].

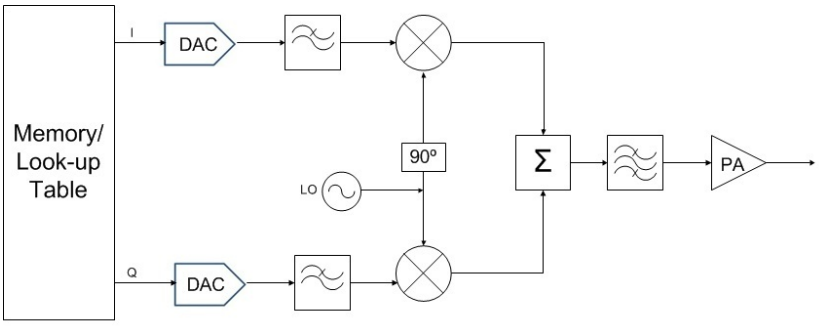

Figure 2.12: AWG Architecture

The generation mechanism begins with the base band signal, created in the digital domain, further can be stored in a memory or look-up table. An equation that represents the baseband signal is:

$$x(t) = x_I(t) + x_Q(t)$$

where $x_I(t)$ is the in-phase signal and $x_Q(t)$ is the quadrature signal.

The next step is to convert this signal to the analog domain, a DAC oppers this function. The DAC will also generate undesired components, image frequencies for example. To better understand this problem the next figure shows how an ideal DAC output from a sine wave has image frequencies, that need to disappear.

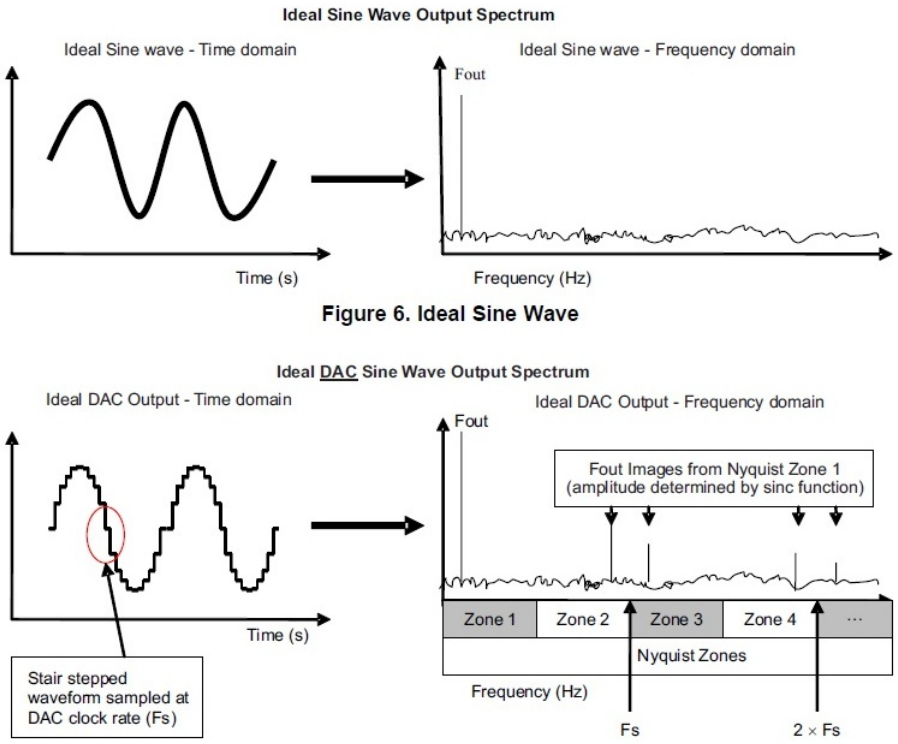

Figure 2.13: DAC conversion spectrum [18]

To eliminate those components a low pass filter is used. The filter shall has a cutoff frequency a little above the output fundamental frequency. The next stage is the up-conversion, an IQ Modulator is typically used in this stage.

One possibility to generate a two tone signal is to generate a single tone at base band that further will be up-converted to RF, generating a two-tone signal. For the base band signal the following equation can represent the signal.

$$\begin{aligned} x_{BB}(t) &= x_I(t) + x_Q(t) \\ &= A cos\left(\omega_{BB} t + \theta_{BB}\right) + jA cos\left(\omega_{BB} t + \theta_{BB} t\right) \end{aligned}$$

where $x_I(t)$ is the in phase signal and $x_Q(t)$ is the quadrature signal, A is the Amplitude of the tone, ω_{BB} is the base band signal frequency and θ_{BB} is the signal phase.

This signal will be fed to the IQ Modulator, to be up-converted to a frequency close to the frequency of the local oscillator.

$$\begin{aligned} x_{RF}(t) &= Re(x_{BB}(t)) e^{j\omega_{LO} t} \\ &= x_I(t) cos\left(\omega_{LO} t\right) + x_Q(t) sin\left(\omega_{LO} t\right) \\ &= A cos\left(\left(\omega_{LO} - \omega_{BB}\right) t - \theta_{BB}\right) + A cos\left(\left(\omega_{LO} + \omega_{BB}\right) t + \theta_{BB}\right) \end{aligned}$$

This last equation shows that the output signal will have components at $\omega_{LO} - \omega_{BB}$ and $\omega_{LO} + \omega_{BB}$, but because some DC component appears at the DAC output and also a non-ideal isolation, a spur signal will appear at ω_{LO}, which can degrade the signal. A possible solution to eliminate this spur signal is adding an offset frequency to the base band signal. This offset will lead the output to a four-tone signal, and the bandpass filter at the output of IQ Modulator, that has a first cutoff frequency little above the LO frequency, the final result will be a two tone signal. A con to this solution is the reduction of the frequency range [19].

Another problem can occur in this type of generator, if an output signal with high output power is desired. The two tone signal will be amplified by the PA, thus distortion can arise creating several spurious spectral components. To avoid this possible problem, the two tone signal shall be generated at a low output power and the PA shall operate in a linear region and has a high IP_3. This implementation also has cons, if the PA has a high noise pattern, the quality of the output signal is degraded.

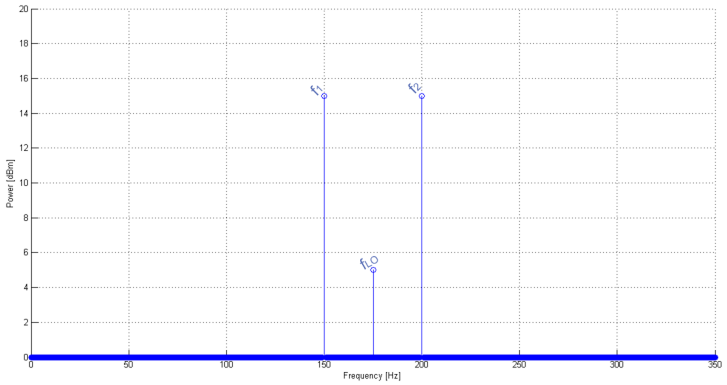

Figure 2.14: Spur at f_{LO}

2.3 Digitally Modulated Signals

With the evolution of the wireless systems, these kind of signals gain importance and now they are the most important type of excitation signals. It is possible to divide the digitally modulated signal in two areas, characterization and modeling RF components.

For characterization, the signals are generated according to the architecture presented on figure 2.12, the AWG architecture, using algorithms to generate the base band signals and then up-convert to RF. To modeling RF components, the quality of the signal in terms of state space to be covered is the most important problem to be resolved. Also the capability to identify the highest number of different system states combined with good periodic signals for measurements is important. To achieve these goals, the approach is to generate signals that are equals, as close as possible, the real telecommunication signals, several spectra excitations can be used, the Narrow Band Gaussian Noise (NBGN) is one of the most important. It is difficult to measure the real telecommunications signals using ordinary instrumentation and it is more difficult to generate those signals in a systematic measurement. For this last reason that is why some other kinds of signals are gaining importance in the instrumentation area, because they can be generated in an efficient way and the multi-sine is one of those signals [20].

2.3.1 The Multi-Sine

A fundamental kind of excitation signal for a correct gathering of the signal information is the multi-sine signal, because of the previous reason presented above. In a simple way, multi-sine is a sum of several tones (sine waves), which can be described by the following equation:

$$x(t) = \sum_{l=1}^{L} A_l cos\left(\omega_l t + \theta_l\right)$$

The L is the number of tones (sines) to be summed, ω_l is the radian frequency of each tone(sine) and θ_l is the phase of each tone (sine).

If ω_l has any frequency value, then it is a non-uniform multi-sine that can be periodic or not. To be a periodic signal, it is necessary to have an $\Delta\omega$ that is the maximum common divider of each of the frequencies. In other words, $\omega_l = k\Delta\omega$, where k is an integer. If the tones are generated in different generators, then it is necessary a phase synchronization between them, if the there is no synchronization the summation of ω_l will always create a non-periodic signal due to the phase deviation [9].

It is also possible to create tones equally spaced as in $\omega_l = \omega_0 + (q-1)\Delta\omega$, ω_0 is the position of the first tone and $\Delta\omega$ the constant frequency separation between them, in this case the multi-sine is said to be uniformly spaced. The period of this multi-sine is given by:

$$T_{MS} = \frac{1}{\Delta\omega}$$

Many considerations need to be done in first place, in order to extract some useful information. These signals can present different time domain waveforms, different amplitudes for each tone. The figure 2.15 represents examples of these waveforms. To describe these signals behaviours the amplitude probability density function was adopted, with this characterization each signal presents a different statistical values.

Because of the different statistical values that the multi-sine presents, a careful design of this kind of signal shall be taken, in order to characterize the nonlinear DUT [20].

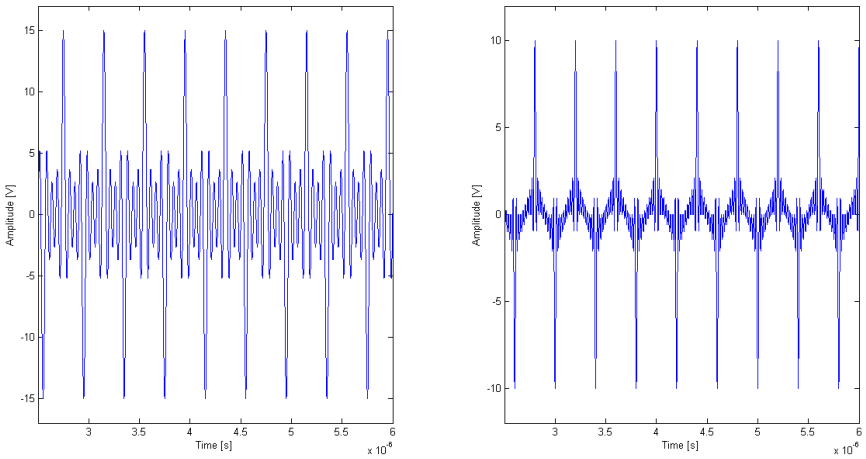

Figure 2.15: Example of Multi-sine Waveforms

Probability Density Function

The probability density function ($pdf(x)$) characterizes every random variable x. The pdf is established after a large number of measurements have been performed, which determine the likelihood of all possible values of x. If the random variable is discrete then it possesses a discrete pdf and if it is a continuous random variable, it possesses a continuous pdf [21].

Two important properties for $pdfs$:

- No event can have a negative probability;

$$pdf(x) \geq 0$$

- The probability that an x value exists somewhere over its range of values is certain.

$$\int_{-\infty}^{+\infty} pdf(x)dx = 1$$

The two properties must be satisfied by any pdf. Since the total area under the pdf is equal to 1, the probability of x existing over a finite range of possible values is always less than 1.

Several properties of the variable x can be extracted from the $xpdf$. One of them is the statistical average, given by the expected value equation.

$$E[x] = \int_{-\infty}^{+\infty} x \cdot pdf(x)dx$$

The random variable x in the previous equation can also be any function of x, $f(x)$, thus the expected value of $f(x)$ is:

$$E[f(x)] = \int_{-\infty}^{+\infty} f(x) \cdot pdf(x)dx$$

The expected value of x is typically called the moment of first order and is denoted as:

$$m_1 = \int_{-\infty}^{+\infty} x \cdot pdf(x)dx$$

Then, the moment of n^{th} order is defined as:

$$m_n = \int_{-\infty}^{+\infty} x^n \cdot pdf(x)dx$$

If the random variable is expressed in volts, the moment of first order will correspond to the average (mean or DC voltage) and the moment of second order corresponds to the average power.

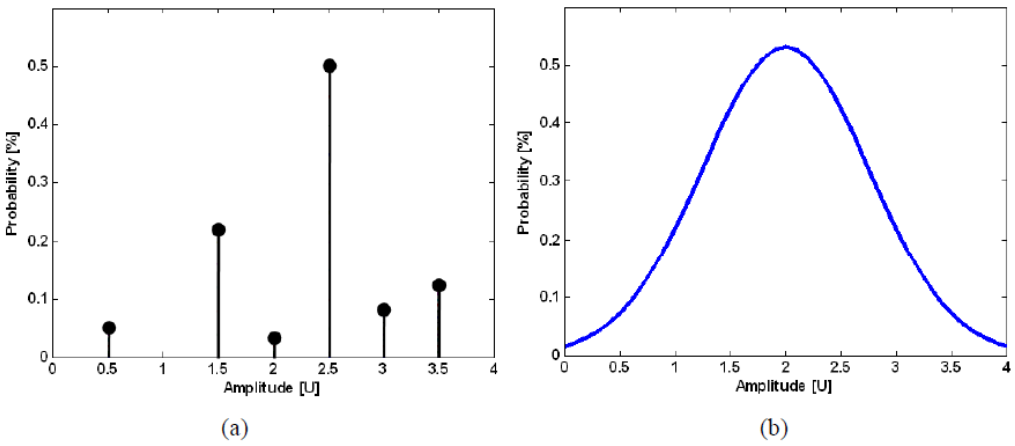

Figure 2.16: Simulated (a) discrete *pdf* and (b) continuous *pdf* [21]

2.3.1.1 Multi-Sine with Pre-determined Statistics

In nonlinear memoryless systems, the response to the stimulus signal value is instantaneous. Because of this aspect, it is possible to assume that the instantaneous output is completely determined by the stimulus signal amplitude. However the usual system's outputs as for instance output power, power spectral density (PSD), or Adjacent Channel Power Ratio (ACPR) have a statistical average value. The range of amplitude covered by the output is important but also the probability which these values are reached is essential, which makes it is more important to know, in average, the value weighted by the *pdf* than the instantaneous amplitude of the stimulus signal. For example, if the signal has very high instantaneous amplitude but a very low *pdf*, the output is irrelevant. In the datasheets, the manufacturers include information about *pdf*, or about the complementary cumulative distribution function, *ccdf*.

Complementary Cumulative Distribution Function

The Complementary Cumulative Distribution Function (*ccdf*) provides significant information about the signals used in real communications systems. For example it can show how much time the signal spends at or above a given power level. The Cumulative Distribution Function, *cdf* curves comes from the pdf, in mathematical way, it is represented by the integral of *pdf*.

$$cdf(x) = \int_{-\infty}^{a} pdf(x)dx$$

So the *ccdf* becomes from the complement of *cdf*, $ccdf = 1 - cdf$. As said before, *ccdf* can provide critical information, as for example, in the figure below, the variation of Peak-to-Average Power Ratio (PAPR) of a GSM signal using one and three channels. As can be seen, the complexity of the three GSM channels significantly degrades the overall signal [21].

To conclude, the *ccdf* are an important tool in design and test of system's components.

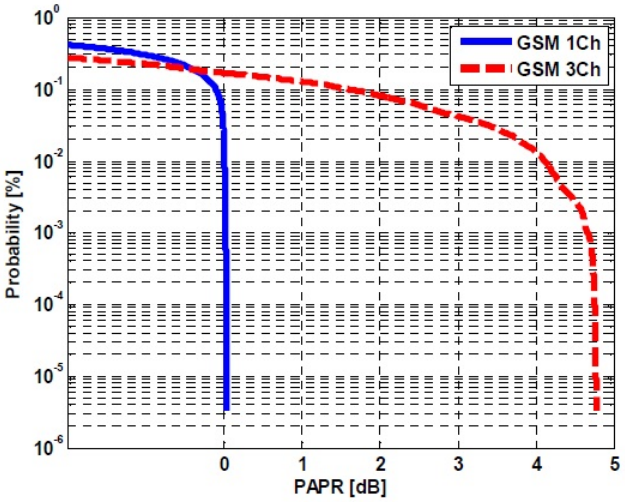

Figure 2.17: *ccdf* for a GSM signal with 1 Channel and 3 Channels[21]

2.3.1.2 Approximating the Multi-Sine *pdf*

Like previous said the *pdf* has an important role on design and verification bandpass systems so it is important to know how is the *pdf* behavior. There is one useful technique that permit to synthesize a desired multisine *pdf*, it consists on an algorithm with seven steps [20].

1) Synthesize a noisy signal with the specified pdf statistics pattern and reorder its instantaneous amplitude values in descending order. This creates the vector of pdf bins for the noise.

2) Synthesize an equal-amplitude multisine with the prescribed number and frequency position of tones.

3) Reorder its instantaneous amplitude values in descending order, recording the time samples where they stood. This creates the vector of pdf bins for the multisine

4) Substitute the amplitudes of the multisine vector of pdf bins by the one for the noise.

5) Restore these amplitudes in the original time samples of the multisine, creating a new multisine with the desired pdf.

6) Calculate the DFT of this signal, and level off the resulting tone amplitudes so that the total power is kept, maintaining the phases obtained. This represents the desired multisine we seek.

7) If the process of tone amplitude level-off has modified the multisine pdf to an unacceptable error, repeat the algorithm, using as the starting multisine the one synthesized with this technique, until an acceptably small error is reached.

To better understand this algorithm, figure 2.18 presents the figures of each step. Figure 2.18 (a) and figure 2.18(b) refer to the noisy signal in time and spectrum respectively. To finish step 1, figure 2.18(c) presents the sorting of signal amplitudes in ascending order. For step 2, figure 2.18(d) represents the time behavior of the generated multisine with equal-amplitude. On the next figure, 2.18(e), its spectrum is presented. The point 3 of the algorithm is presented on figure 2.18(f). The figure 2.18(g) reveals the spectrum after the amplitude change referred on points 4 and 5 of the algorithm. The last figure, 2.18(h), presents the multisine signal, after the algorithm realization.

2.3.1.3 Multi-Sine with Pre-determined High Order Statistics

In a memoryless nonlinearity, the first order statistics as an example the *pdf* and its associated moments are sufficient to describe the integrated value of distortion power. In nonlinear dynamic systems, the first order statistics is not sufficient because it is possible to generate multi-sines with similar *pdf* function but with different output spectral regrowth masks. For this reason another multi-sine design technique is necessary, in this case for dynamic nonlinear systems.

In these systems, the output does not change instantaneously with the input signal, so the statistical relations of the output shall include not only the static statistical behavior as the pdf but also higher order statistics. For polynomial description the output is given by

$$y(t) = \sum_{n=1}^{N} y_n(t)$$

where $y_n(t) = \int_{-\infty}^{+\infty} h_n(\tau_1, ..., \tau_n)x(t-\tau_1)...x(t-\tau_n)d\tau_1...d\tau_n$ and $h_n(\tau_1, ..., \tau_n)$ is nth order nonlinear operator.

The goal is to obtain the output Power Spectral Density (PSD) or the spectral mask of the output, $y_n(t)$ can be given by:

$$Y_{s,n}(w) = \int_{-\infty}^{+\infty} \{ \int_{-\infty}^{+\infty} ... \int_{-\infty}^{+\infty} h_n(\tau_1, ..., \tau_n) \left[\int_{-\infty}^{+\infty} X_s(\omega_1) e^{j\omega_1(t-\tau_1)} d\omega_1 \right] ... \left[\int_{-\infty}^{+\infty} X_s(\omega_n) e^{j\omega_n(t-\tau_n)} d\omega_n \right] d\tau_1 ... d\tau_n \} e^{-j\omega t} dt$$

$$= \int_{-\infty}^{+\infty} \{ \int_{-\infty}^{+\infty} ... \int_{-\infty}^{+\infty} \left[\int_{-\infty}^{+\infty} ... \int_{-\infty}^{+\infty} h_n(\tau_1, ..., \tau_n) e^{(j\omega_1\tau_1 + ... + j\omega_n\tau_n)} d\tau_1 d\tau_n \right] \left[X_s(\omega_1)...X_s(\omega_n) e^{j(\omega_1 + ... + \omega_n)t} \right] d\omega_1 ... d\omega_n \} e^{-j\omega t} dt$$

$$= \int_{-\infty}^{+\infty} \left[\int_{-\infty}^{+\infty} ... \int_{-\infty}^{+\infty} H_n(\omega_1, ..., \omega_n) X_s(\omega_1) ... X_s(\omega_n) e^{(\omega_1 + ... + \omega_n - \omega)t} d\omega_1 ... d\omega_n \right] dt$$

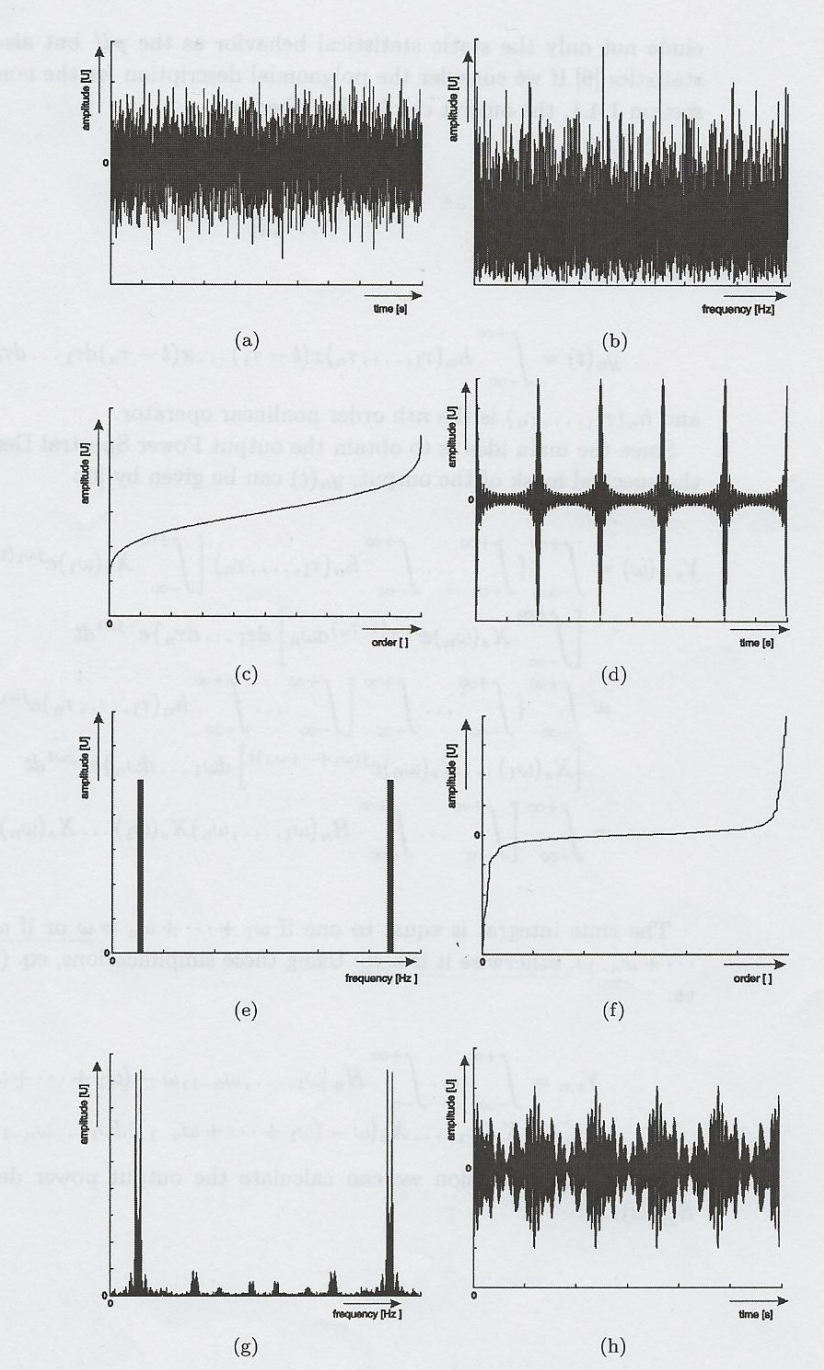

Figure 2.18: Algorithm phases

The time integral is equal to one if $\omega_1+...+\omega_n=\omega$ or if $\omega_n=\omega-(\omega_1+...\omega_{n-1})$, otherwise it is zero. Using these simplifications, the output is simplified to:

$$Y_{s,n}=\int_{-\infty}^{+\infty}...\int_{-\infty}^{+\infty}H_n[\omega_1,...,\omega_{n-1},\omega-(\omega_1+...+\omega_{n-1})]X_s(\omega_1)...$$
$$...X_s(\omega-(\omega_1+...+\omega_{n-1}))d\omega_1...d\omega_{n-1}$$

Using this expression, it is possible to calculate the output power density function, $S_{yy}(\omega)$, as:

$$S_{yy}(\omega)=\sum_{n_1=1}^{N}\sum_{n_2=1}^{N}\int_{-\infty}^{+\infty}...\int_{-\infty}^{+\infty}H_{n_1}[\omega_1,...,\omega-(\omega_1+...+\omega_{n_1-1})]$$
$$H_{n_2}[\upsilon_1,...,\upsilon-(\upsilon_1+...+\upsilon_{n_2-1})]^*$$
$$E\{X_s(\omega_1)...X_s(\omega-(\omega_1+...+\omega_{n_1-1}))X_s(\upsilon_1)^*...X_s(\upsilon-(\upsilon_1+...+\upsilon_{n_2-1}))^*\}$$
$$d\omega_1...d\omega_{n_1-1}d\upsilon_1...d\upsilon_{n_2-1}$$

In a third order nonlinearity, the output will be:

$$S_{yy}(\omega)=|H_1(\omega)|^2S_{xx}(\omega)+2Re\{\int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty}H_1(\omega)H_3(\omega_1,\omega_2,\omega-\omega_1-\omega_2)^*$$
$$E[X(\omega)X(\omega_1)^*X(\omega_2)^*X(\omega-\omega_1-\omega_2)^*]d\omega_1d\omega_2\}$$
$$+\int_{-\infty}^{+\infty}...\int_{-\infty}^{+\infty}H_3(\omega_1,\omega_2,\omega-\omega_1-\omega_2)H_3(\upsilon_1,\upsilon_2,\upsilon-\upsilon_1-\upsilon_2)^*$$
$$E[X(\omega_1)X(\omega_2)X(\omega-\omega_1-\omega_2)X(\upsilon_1)^*X(\upsilon_2)^*X(\upsilon-\upsilon_1-\upsilon_2)^*]d\omega_1d\omega_2d\upsilon_1d\upsilon_2$$

The $H_n(\omega_i,...,\omega_j)$ is the nonlinear frequency operator, it can be easily know because it only depends of the DUT nonlinear model. The value of the average $E[X(\omega_1)X(\omega_2)X(\omega-\omega_1-\omega_2)X(\upsilon_1)^*X(\upsilon_2)^*X(\upsilon-\upsilon_1-\upsilon_2)^*]$ should be equal for the multi-sine signal and for the real signal that is pretended to describe. Because of this reason, the signals should follow the next equation, for a third order nonlinearity:

$$S_{xxxx}(\omega_1,\omega_2,\omega_3)=E[X(\omega_1)X(\omega_2)X(\omega_3)^*X(\omega_1+\omega_2-\omega_3)^*]$$

The equation above is known as the signal's higher order statistics, because they represent an higher order extension of the first order PSD, $S_{xx}(\omega)$.

It is possible to conclude that the two signals, multi-sine $x(t)$ and real signal $x_r(t)$, are similar up to order n, they will present the same PSD, if they have close n th order spectra $S_{xx}(\omega)\approx S_{x_rx_r}(\omega), S_{xxxx}(\omega_1,\omega_2,\omega_3)\approx S_{x_rx_rx_rx_r}(\omega_1,\omega_2,\omega_3),...,S_{x...x}(\omega_1,...,\omega_{n-1})\approx S_{x_r...x_r}(\omega_1,...,\omega_{n-1})$.

This technique reveals a problem when it refers to the number of unknowns to be matched. As an example, if the noise is sampled as a $2k+1$ points and then is transformed by a DFT, $S_{xx}(\omega)$ only involves an average made over $2k+1$ points per realization. A second order analysis $S_{xxxx}(\omega_1,\omega_2,\omega_3)$ involves an average over $(2k+1)^3$ complex entities, for a third order $S_{xxxx}(\omega_1,\omega_2,\omega_3,\omega_4,\omega_5)$ an average of $(2k+1)^5$ so this design algorithm reveals an extremely heavy computational processing. If a multi-sine is implemented with a lower number of sines, this algorithm does not become so heavy, but the number of unknowns is limited, so as the

free states. The best approach is to consider a large number of sines in order to approximate the PSD in some selected bins. In the next figure this approach is presented, typically this is the implementation done in the lab.

To generate the multi-sine, it is simply done by optimizing the PSD of the multi-sine and the real signal in the interested bins. The optimization is done by recurring to the higher order statistics equations. As example, for a third order linearity, the errors can be minimizes according to the equation presented below.

$$\in_{4,b_1,b_2,b_3} = \sum_{m_1=\frac{(b_1-1)M}{B}+1}^{\frac{(b_1)M}{B}} \sum_{m_2=\frac{(b_2-1)M}{B}+1}^{\frac{(b_2)M}{B}} \sum_{m_3=\frac{(b_3-1)M}{B}+1}^{\frac{(b_3)M}{B}} \{A_{m_1} A_{m_2} A_{m_3} e^{[\phi_{m_1}\phi_{m_2}-\phi_{m_3}-\phi_{m_1+m_2-m_3}]}\}$$

$$\sum_{k_1=\frac{(b_1-1)M}{B}+1}^{\frac{(b_1)M}{B}} \sum_{k_2=\frac{(b_2-1)M}{B}+1}^{\frac{(b_2)M}{B}} \sum_{k_3=\frac{(b_3-1)M}{B}+1}^{\frac{(b_3)M}{B}} E[X(\omega_{k_1})X(\omega_{k_2})X(\omega_{k_3})^* X(\omega_{k_1}+\omega_{k_2}-\omega_{k_3})^*]$$

with $b_1, b_2, b_3 \in \{1, ..., B\}$

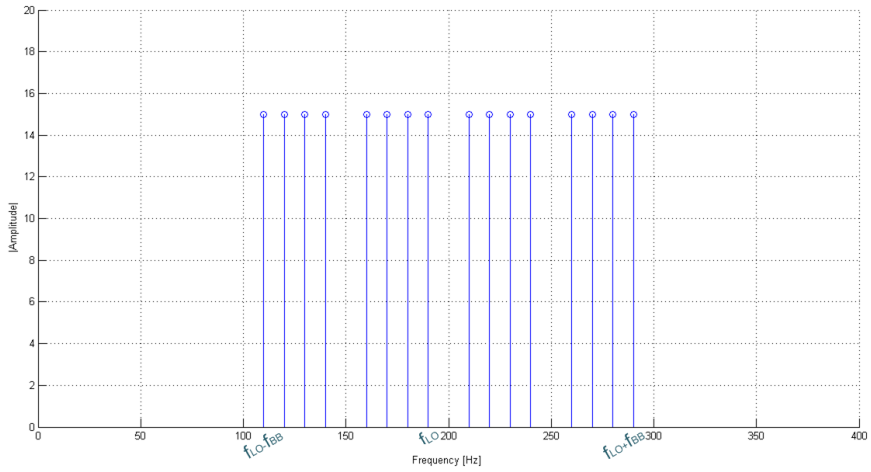

Figure 2.19: Frequency Bins

2.3.2 Multi-Sine Generation Mechanisms

Like in the two-tone case, to generate multi-sine several RF generators and power combiners can be used. This solution can have an extremely high cost, if a signal generator produces

one tone, to generate ten tones ten generators are necessary. Also it is very difficult to control the phase of each sine [9].

A better approach is by using an Arbitrary Waveform Generator, almost similar to the one presented in the figure 2.12. To start, the phase and amplitude of each sine needs to be determined, it can be done by a computer software using algorithms that were already presented in this work.

The algorithm's outputs is a set of amplitude and phases for each of the multi-sine bins, thus defining the digital version of the I and Q. This signal will be then uploaded to an AWG's memory before being converted to the analog domain through a DAC. The IQ modulator will up-convert the signal and finally the band-pass signal is amplified and presented on the output [20].

There are some problems that can occur, for example if the signal is wide-band, the non-idealities of the AWG can degrade the intended multi-sine presented on the output. Another problem is the phase arrangement developed in the algorithm, it can be entirely changed and so degrading the overall measurement. A solution to this problem is by using a feedback loop to synthesize the correct waveform at the input of the DUT [20].

2.4 Chirp Signals

Chirp signal is a signal that its frequency varies with time. The frequency varies in a certain range, (f_1 and f_2), which can vary in different ways, for example linear, exponential, quadratic or logarithmic [22].

If it varies linear, $f(t) = f_1 + kt$ (k is the chirp rate), the time domain function is given by:

$$x(t) = cos\left[2\pi(f_1 t + \frac{k}{2}t^2 + \theta_0)\right]$$

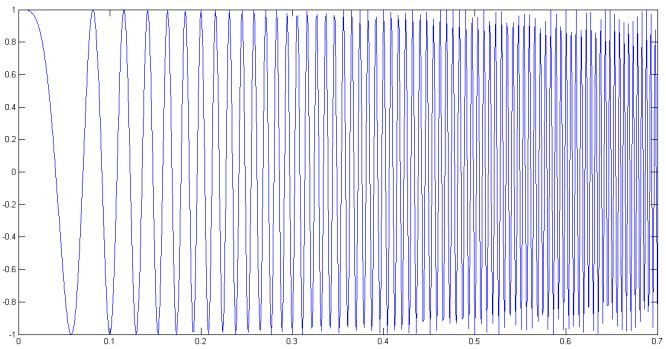

Figure 2.20: Linear Chirp Signal Time Domain

If it varies quadratic, $f(t) = f_1 + kt^2$ (k is the chirp rate), the time domain function is given by:

$$x(t) = cos\left[2\pi(f_1 t + \frac{k}{2}t^3 + \theta_0)\right]$$

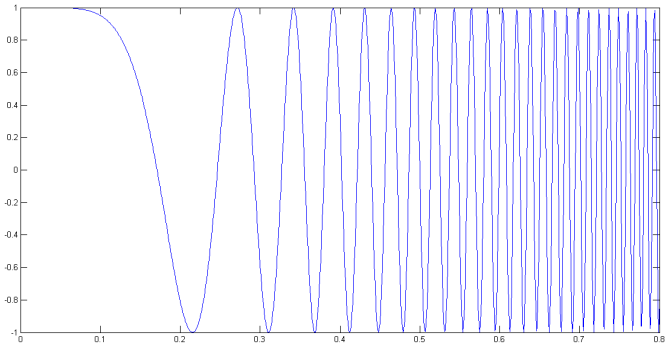

Figure 2.21: Quadratic Chirp Signal Time Domain

This kind of signal is gaining importance in RF/Microwave experiments because it mimics signals in TDD (Time Division Duplex) systems. For example a two-tone chirp signal, where the tone spacing is varying with time t, allows to acquire information about the nonlinear distortion and nonlinear distortion dynamics. The math equations, the time domain and the frequency domain figures are presented below [23].

$$x(t) = Acos\left[2\pi(f_c - \frac{\delta(t)}{2})t\right] + Acos\left[2\pi(f_c + \frac{\delta(t)}{2})t\right]$$

$$\delta(t) = \sum_{k=0}^{N} \rho_k rect(t - t_k)$$

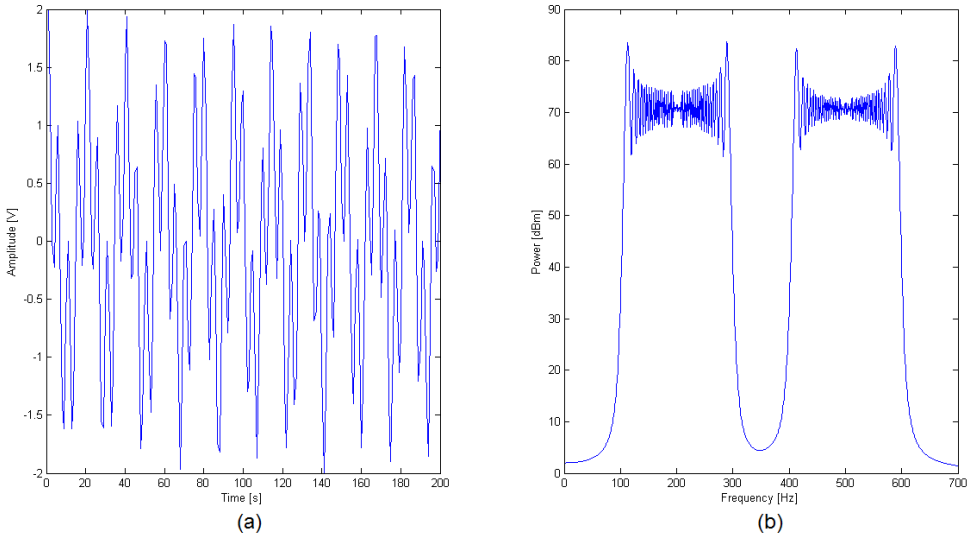

Figure 2.22: Two-Tone Chirp Signal(a) Time Domain (b)Frequency Domain

Usually to generate chirp signals, a DDS approach like the one presented on the figure 2.12. In the baseband signals should be two single tones, moving away from each other as the

time goes. With this configuration, the two-tones and the intermodulation products can be measured and characterized in one single measurement using a Vector Signal Analyzer (VSA) [23].

2.5 Pulsed Signals

A pulsed signal is a periodic signal that has two distinct states, on and off. The on state provides a stable signal with medium or high while and the off state has much reduced signal power, ideally there is no signal present in the off state [24].

Sometimes to characterize a DUT pulsed signals are used instead of CW signals. An example of pulsed signal applications is to measure the S-parameters of power amplifiers during the on-wafer phase. The pulsed signals with a proper duty cycle, the average power can be minimized in a significant part, maintaining the high peak power [25].

There are different types of pulsed signals, one typical is a single pulsed RF signal, figure 2.23. This periodic single pulse reduces the average power while maintaining the peak power by choosing a proper duty cycle. This imposes that the average power of the DUT is reduced to avoid the destruction of the DUT [25].

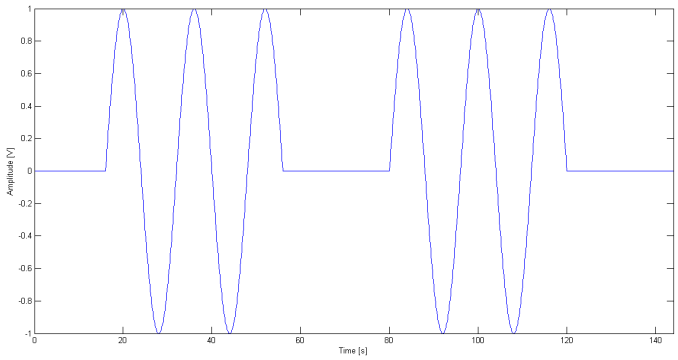

Figure 2.23: Single Pulsed Signal

Other kind of pulsed signals are the double pulses, commonly used in radar systems like weather radar and target tracking radar. The double pulse makes a double echo, which goes through signal processing efficiently and suppresses most of the noise and other interference signals, ensuring high measurement accuracy. The pulse trains, present on others radars systems, are a combination of different types of pulses, such as periodic or non-periodic, and modulation can be applied to each pulse [25].

In typical analog generators, the pulsed signal is generate by using a switch on the output that makes possible the two states of the pulsed signal, on state and off state. One advantage of these systems is the fact that they can generate very short signals (in the nanosecond range) and also they have a good on/off ratio. The biggest disadvantage is the fact that they do not change the pulse shape. Other kind of generating pulsed signals is the architecture that has already been studied in this chapter, the AWG architecture. The pulse's shapes can be generated in baseband signals and then up-convert by the IQ Modulator. With this architecture it is possible to implement different pulse forms, for example pulsed train is

possible to realize. The disadvantages are the bandwidth, more reduced and the on/off ratio is not so good in comparison to the previous mechanism [24, 25].

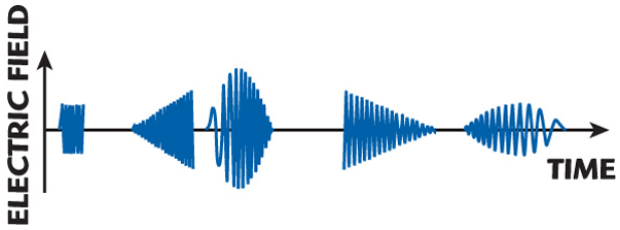

Figure 2.24: Pulsed Train Signal [24]

2.6 Conclusion

The study developed in this chapter present solutions to implement the desired generators. In the first section, One Tone Stimulus, approaches like PLL or DDS, need to be considered to realize the CW Generator. A parameter that also is necessary to take concern is the phase noise that degrades the quality of the signal.

The Two-Tone Stimulus, which belongs to the other objective in this thesis, presents an architecture that is becoming more used in RF Generators. The AWG approach is a powerful architecture, as it was possible to observe as this chapter advanced, different kind of signals are realized by this generator. One problem common in this type of generators is the LO harmonic that can be too high and thus degrades the signal quality.

Other signals like multi-sine, chirp and pulsed were studied in order to get more knowledge about the matter. Although they can be very useful to extract information of the DUT, because they mimic the real telecommunications signals, the Diogo's system is not ready to receive these kinds of signals, so for now, they stay out of the scope of this work.

Chapter 3

CW Generator

According to the desired goals, implementation of a CW generator and an Arbitrary Waveform Generator, this chapter presents the CW generator realization. This generator has like function to act like as one tone stimulus signal and to perform as a local oscillator in the system present on figure 1.4.

As described in the previous chapter, it is possible to implement a one tone signal by using RF synthesizers like a PLL. Develop a PLL is an interesting suggestion but can be very long and time is an important factor in this project. By observing the major companies of electronics products (Analog Devices, Texas Instruments, Mini-Circuits, Linear Technology and others), it is easy to find RF synthesizers with a PLL architecture. As said before, time is an important factor so the fast solution is to acquire an integrated circuit that can perform the desired purpose.

Some considerations are important to be done before choosing the component, first is the frequency range. Observing Diogo Ribeiro's system, it is possible to conclude that two local oscillators need to be realized. One will act in the down-conversion stage, convert to IF frequency, in this case this frequency is about 60 MHz and the other one LO will be needed in the stimulus signal generator, in the next chapter, all explanations due to this generator will be explained. So the stimulus signal frequency range is between 40 MHz and 1000 MHz, same as the LO needed in this stage. In the IF stage, the frequency range is adding 60 MHz to the stimulus signal, this is 100 MHz and 1060 MHz. Concluding the frequency requirement, an integrated circuit that operates in the region of 40 MHz to 1060 MHz is desired. The output power is also an important aspect to be considered; despite of the existence of large number of amplifiers or attenuators available in the desired band, the desired power is about 10 dBm in both stages, so a synthesizer with an output power close to 0 dBm is also desired. The impedance is as custom 50 ohm, also phase noise is an important characteristic, low values are pretended. In order to preserve the price of this project as low as possible, first place to search is the stock at Instituto de Telecomunicações (IT), if not available the component should cost as less as possible.

Summarizing the considerations about the RF synthesizer:

- Frequency range, 40 MHz to 1060 MHz;
- Output power close to 10 dBm;
- 50 Ω impedance;

- Low Cost.

After some researches, two integrated circuits were discovered, one from National Semiconductor LMX2541SQ2060E, and the other one from Analog Devices ADF4351. None of this integrated circuits are available at Instituto de Telecomunicações, so one of them needed to be acquired.

	$LMX2541SQ2060E$	$ADF4351$
$CostperUnit$	14.04	24.44
$EvalutionBoard$	394.57	175.00

Table 3.1: Cost in dollars of LMX2541SQ2060E and ADF4351

The ICs and theirs evaluation boards have an elevated cost so the option was to order free samples, and the first IC that arrives will be the one tested, since they have characteristics very similar. The first one to arrive was LMX2541.

3.1 1st Implementation

The LMX2541 is a low noise frequency synthesizer (normalized noise floor of -225 dBc/Hz) which has a high performance delta-sigma fractional N PLL, a VCO (fully integrated circuit) and an optional frequency divider. This PLL can also be configured to work with an external VCO. With a good reference oscillator (low phase noise), the LMX2541 generates a very stable, low noise signal. This integrated circuit is divided in a family of 6 devices (table 3.2) with different VCO frequency ranges (from 1990 MHz up to 4 GHz). By using the frequency divider(1 to 63), the LMX2541 can generate low frequencies as 31.6 MHz. Programming this device is by using microwire (subset of Serial Peripheral Interface). Supply voltage is 3.3V. The LMX2541's package is available in a 36 pin 6x6x0.8 mm Lead-Free Leadless Leadframe Package (LLP)[26].

Device	**VCOFrequency**	**UsingDividers**
$LMX2541SQ2060E$	$1990 - 2240$	$31.6 - 2240$
$LMX2541SQ2380E$	$2200 - 2530$	$34.9 - 2530$
$LMX2541SQ2690E$	$2490 - 2865$	$39.5 - 2865$
$LMX2541SQ3030E$	$2810 - 3230$	$44.6 - 3230$
$LMX2541SQ3320E$	$3130 - 3600$	$49.7 - 3600$
$LMX2541SQ3740E$	$3480 - 4000$	$55.2 - 4000$

Table 3.2: LMX2541 family frequency coverage, values in MHz [26]

As said before, the LMX2541SQ2060 was the IC obtained by order a free sample, in the table above it is possible to observe that another can perform in the desired frequency range. Taking care of other considerations, the output power is programmable, depending on the VCO constant values like VCO gain and VCO divider, but it should vary between 0 dBm and 3.5 dBm. A value not so far from the desired 10 dBm, but this issue will be taken care later. The reference input as the RF output presents a 50 ohm impedance as it was pretended. The

reference input presents a condition, the ideal case is to provide a 10 MHz sine wave single-ended, which is common to be available at the back of signal generators, spectrum analyzer and other devices. In LMX2541SQ2060E the reference signal should have a slew rate about 150 V/μs. With a 10 MHz single-ended sine wave it is not possible to achieve this slew rate, so according to the figure(also available on the appendix) presented in the LMX2541SQ2060E datasheet page 24, it is possible to choose a single-ended sine wave in other frequency, higher than 10 MHz.

To test this device, a printed circuit board was needed, so according to the datasheet of the IC and its evaluation board (figures available on appendix), one PCB was produced, as it is possible to observe in the figure below.

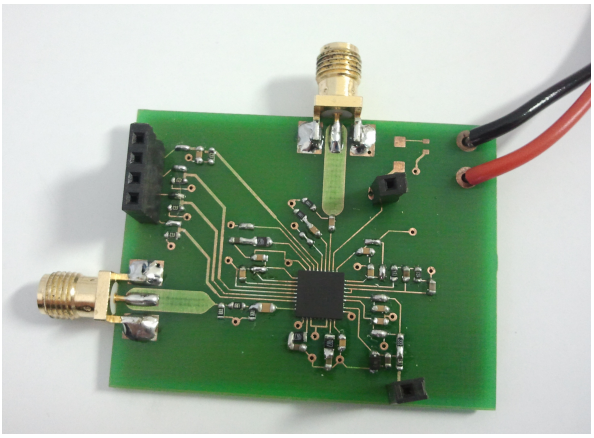

Figure 3.1: PCB of LMX2541SQ2060E

Also it is necessary to choose a microcontroller that is capable of programming the device, it should contain Microwire/SPI ability.

3.1.1 Programming the 1st Implementation

The first approach is to look for a microcontroller available at Instituto de Telecomunicações or at Departamento de Electrnica e Telecomunicações(DET)of Aveiro University, the microcontroller needs to have a SPI interface and output levels CMOS 3.3V [27]. The DET-PIC32 is a board developed at DET, which contains PIC32MX795F512H, a microcontroller from Microchip, a crystal of 8 MHz, a low voltage regulator and a development module(USB to serial UART interface) [28].

Some features of PIC32MX795F512H [28]:

- 32 bit microcontroller;
- 32 registers of 32 bits;
- 80 MHz maximum frequency;
- Operating voltage range of 2.3V to 3.6V;
- 512K Flash memory (plus an additional 12 KB of Boot Flash);
- 3 SPI modules.

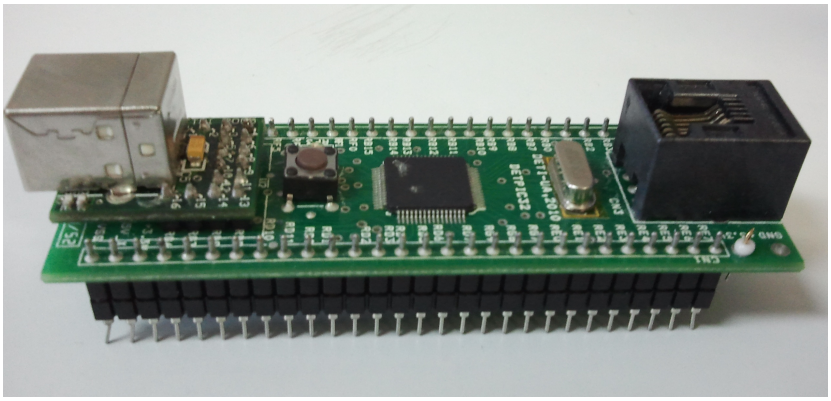

Figure 3.2: DETPIC32

Consulting the datasheet of LMX2541 [25], the section 2.01 presents the registers that needed to be programmed, 12 registers in a specific order (Register Map is available on Appendix). After choosing the correct registers values to program the device, the Serial Data Timing Diagram revealed a problem.

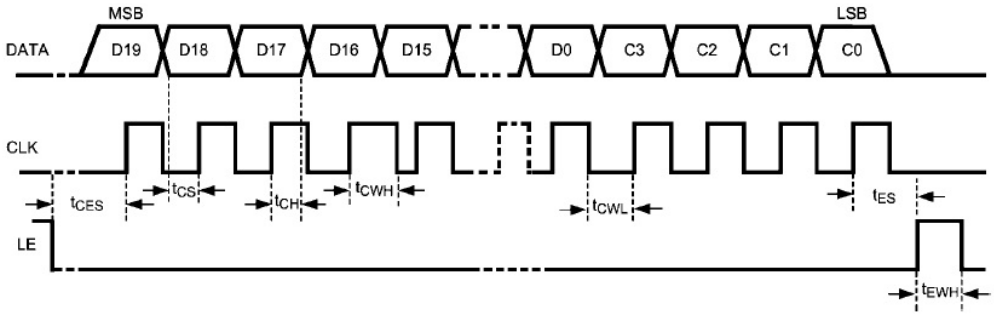

Figure 3.3: Serial Data Timing Diagram of LMX2541 [26]

As it possible to see, some time delays between the clock signal and data signal need to be done, t_{cs} and t_{ch} for example. To resolve this issue two inverters were placed to delay the clock signal, the chosen inverter was HEF4069UBF, available at stock of DET, it is a DIP package with 6 hex inverters incorporated, so can be easy placed on the breadboard [29].

3.1.2 Results of the 1st Implementation

With all requirements fulfilled, the LMX2541SQ2060E was tested. The reference signal was a 50 MHz single-ended sine wave with 0 dBm.

As it is possible to observe in the figure below, the spectrum reveals a problem. The local oscillator shall be a sinusoidal wave, a completely spectrum with one tone, but harmonics will always exist. As greater the value of the harmonics, more products will occur in the mixer.

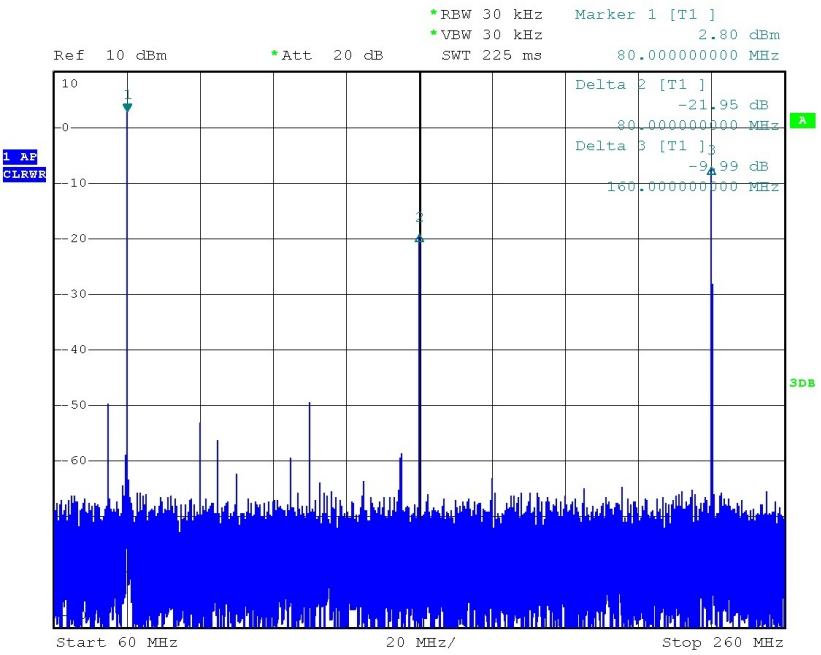

Figure 3.4: LMX2541 Spectrum, Output 80 MHz

This IC reveals harmonics with higher value. By analyzing the functional block diagram, the harmonics can be so high because the output of the VCO, a sine wave, is divided by a digital unit that approaches the sine wave to a square wave.

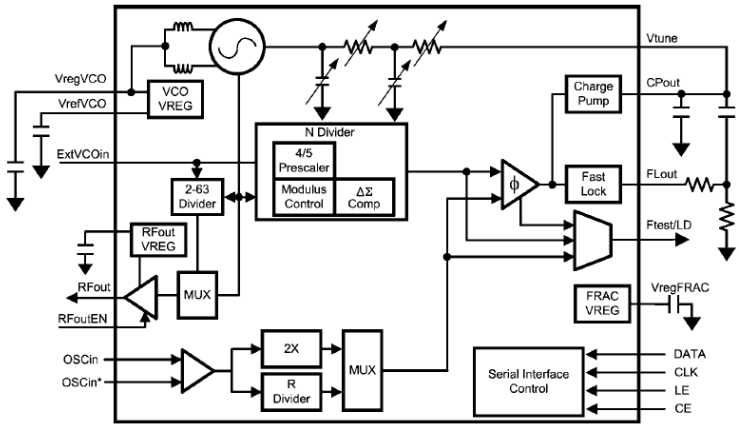

Figure 3.5: LMX2541 Functional Block Diagram [26]

Testing the output of 80 MHz, it is possible to observe in the oscilloscope (Tektronix DP03052, 500 MHz Bandwidth) that the signal has approximately square waveform.

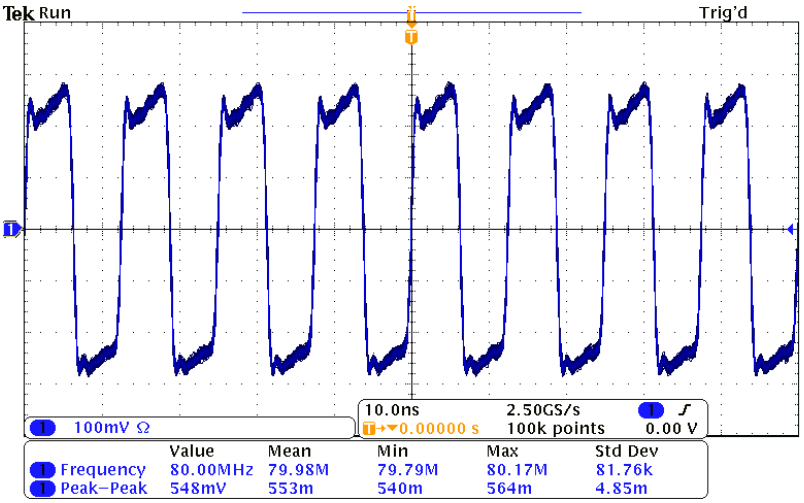

Figure 3.6: LMX2541 in time domain, Output 80 MHz

The fact of being a square, harmonics with high value, influences, when for example, the signal is applied as a local oscillator on a mixer, these high harmonics will create undesired products. One solution to suppress the harmonics is to apply filters and multipliers on the output, but because of the frequency range it demands a certain number of switches, this strategy is not too engineer. A different approach was decided to be realized.

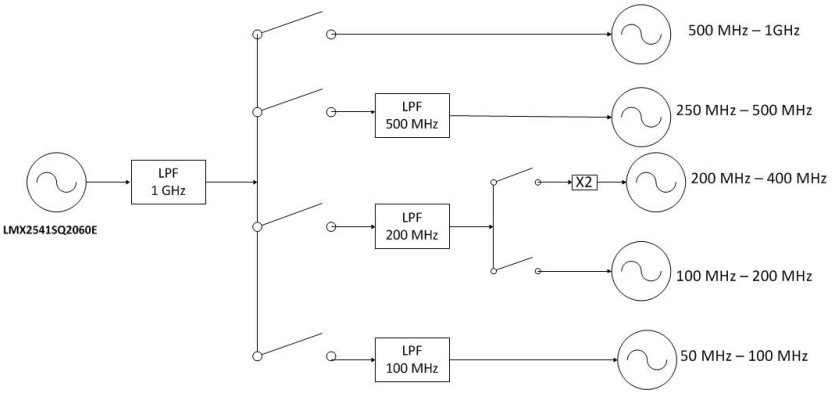

Figure 3.7: Example of solution to eliminate the harmonics in LMX2541

The ADF4351, refereed before, could be an option but taking considerations about the harmonics and block diagram presented on the datasheet it was concluded that the output is quite similar to the output of LMX2541SQ2060E, which reveals that is not useful for this project [30].

3.2 2nd Implementation

A previous research, presented in the beginning of this chapter, revealed that only two integrated circuits can perform in the desired frequency range, and the two ICs present the same problem, generation of square waves instead of sine waves. A new solution is necessary and an idea occurred. An old project developed in Instituto de Telecomunicações, named Panorama, used four RF synthesizers from LuffResearch, SLSM4 [31].

The SLSM4 is a frequency synthesizer from Luff Research, the tuning range is between 8500 MHz and 9500 MHz, with a frequency step of 500 Hz and the output power is about +10 dBm ± 1dB. Looking to the block diagram, this synthesizer presents a fractional N integrated circuit from Skyworks (SKY72302) that is a sophisticated phase-locked loop IC with a spur-free operation, 6.1 GHz operation. To program this device is by using Microwire(like in LMX2541). The supply voltage of SLSM4 is 5.2V. The reference input, shall be a 10 MHz with 0 dBm ± 3dB, in this component a single-ended sine wave can be used [32, 33].

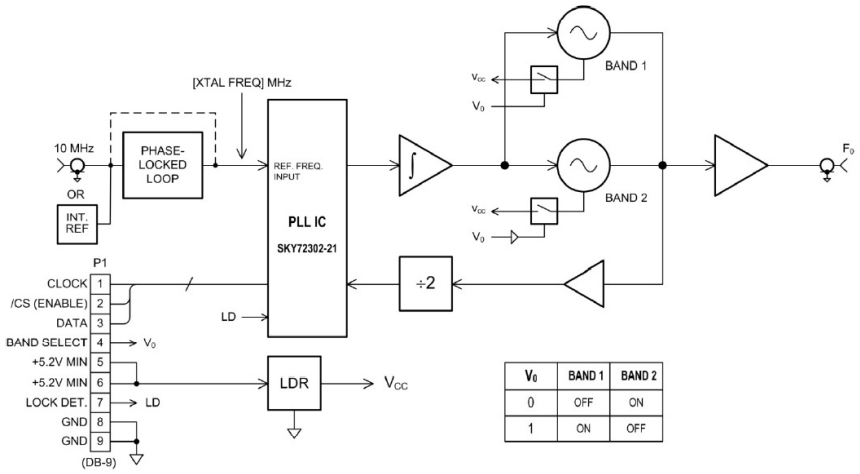

Figure 3.8: Block Diagram of SLSM4 [32]

The output frequency range is far from the desired but if two synthesizers were combined with a mixer like in the figure 3.5, one fixed with 8500 MHz and the other one changing, in the region of down conversion, the frequency range is between 0 Hz to 1000 MHz [32].

To test this solution only the mixer misses. Checking the IT's stock, there is one mixer that fits in the frequency range. The mixer in cause is ZMX-10G+ from Mini-Circuits. The IF port, which will be the output port, has a frequency limit of 2 GHz, acts like a low pass filter, which is useful to suppress harmonics if they exist and also eliminates the uppers products created by the mixer [34].

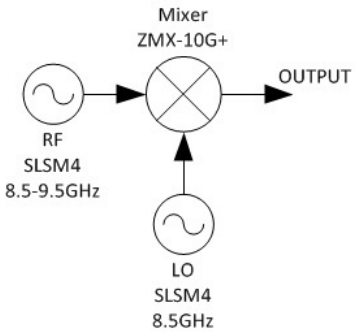

Figure 3.9: Solution applying SLSM4 and a mixer

3.2.1 Programming the 2nd Implementation

To programming this synthesizer, the data is sending by using SPI with 16 bits, so the previous microcontroller, DETPIC32, stills performing the data transfer requirements because it can provide SPI on 8, 16, 24 and 32 bits. In SLSM4, the data is transferred when CS signal is in a low state, so the DATA and CLOCK will be shared by the two components, and the CS will be individual for each SLSM4. The receivers levels are CMOS/TTL, the DETPIC32 provides LVCMOS 3.3V, so a level translation is needed. By consulting some notes about level translation, an integrated circuit was found that can performs the desirable translation [35]. The SN74LVCC3245A from Texas Instruments perform the desired translation, this IC has 8 inputs and 8 outputs, so it is more than the enough, one clock signal one data signal and three chip selects signals (explained later) [36].

About timing considerations, the maximum frequency of clock is 100 MHz, DETPIC32 can provide lower frequency value, so there is no problem for the clock signal. For the others signals it is necessary a delay, some HEF4069UBF were used, again, to realize the delay.

The figure below presents the PCB of SN74LVCC3245A, it is necessary to do a PCB because this IC is not provided in a DIP package so it cannot be placed directly in a bread board.

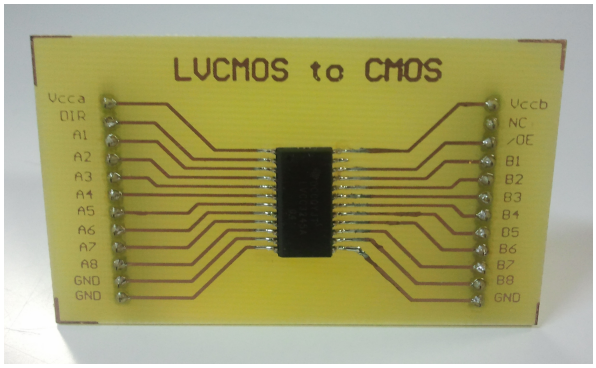

Figure 3.10: LVCMOS to CMOS

3.2.2 Results of the 2nd Implementation

With all considerations about programming done, it is time to test this solution. In the figure below the desired output is 80 MHz (to compare with the output of the previous solution), one SLSM4 fixed at 8500 MHz and the other fixed at 8580 MHz, reference signal sine wave 10 MHz 0 dBm, in both SLSM4.

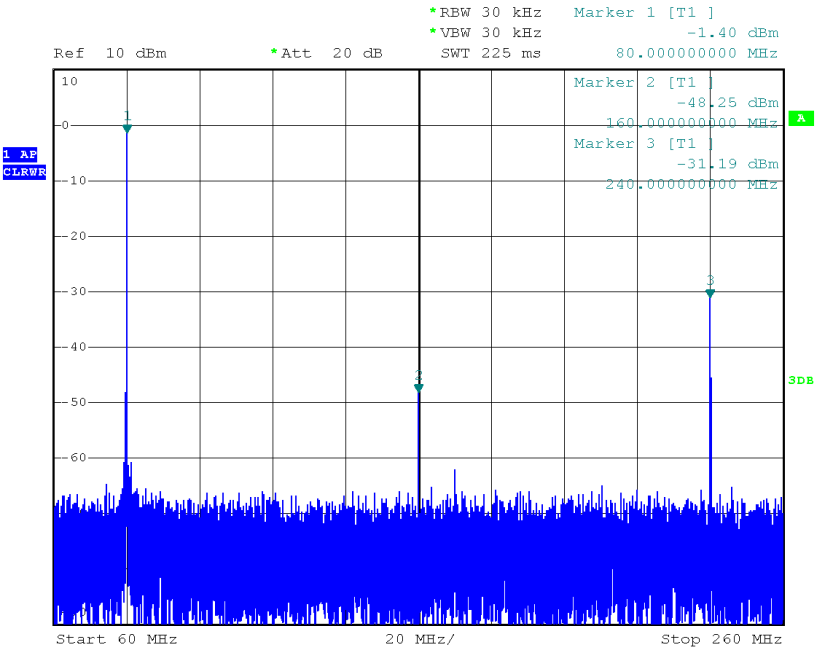

Figure 3.11: SLSM4 Spectrum, Output 80 MHz

The harmonics are very reduced in comparison to the LMX2541SQ2060E , -30 dB in relation to the 2nd harmonic and -20 dB to the third harmonic. The output power, -1.4 dBm stays a little lower than the expected but stills quite good.

Just to be sure that the output is a sine wave, using the oscilloscope previous referred, it is possible to obtain the output in time domain.

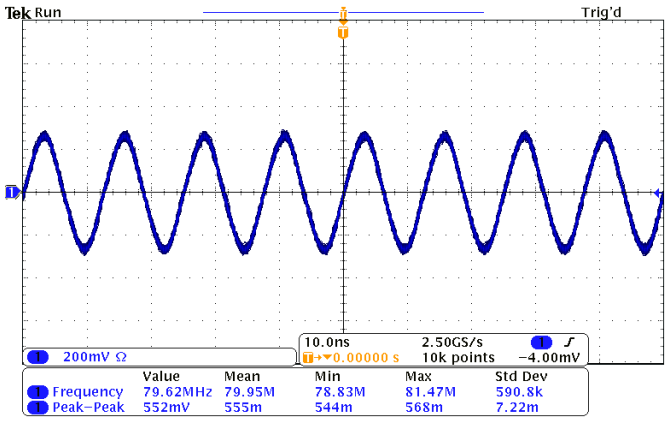

Figure 3.12: SLSM4 in Time Domain, Output 80 MHz

So the CW Generator needs to act as a local oscillator and as a stimulus signal. The final system arrangement for the CW generator is in the figure below. One SLSM4 will be fixed at 8.5 GHz, this 8.5GHz will enter in the two mixers, the others input ports of the mixers will receive a signal varying in 8.54GHz and 9.5GHz that permits to generate the signals presented on the output ports, one for act as stimulus signal the other as a local oscillator.

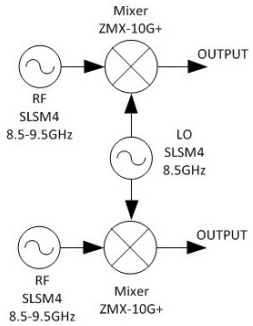

Figure 3.13: One tone and local oscillator mechanism

3.3 Conclusion

Two implementations were developed, LMX2541 and SLSM4. Each implementation has its pros and cons, and they will be analyzed in this section.

Starting with the first one, the problem is the output that revealed high harmonics components (square wave), that to eliminate implies to apply several filters, because the output frequency will change. Another con was the input, to apply a 10 MHz input signal, it needs to be a square wave because of the slew rate but by applying a sine to square wave converter it can be easily resolved. The output power was quite good, the IC fits in the frequency range and the PCB size was extremely good.

The second implementation, solve the problem two problems of the first implementation, low harmonic values on the output and a 10 MHz input signal. The output power is like in first, quite good. The cons are the frequency range and the size. The frequency range is 60 MHz less than the desired, this for the local oscillator, for the one tone stimulus, the frequency range was accomplished. About the size in comparison to the LMX2541SQ2060E is more superior, it is not the most gracious size but it works.

It is not easy to define which is the best solution, but because the objective of this CW Generator is to produce a single tone signal, the second implementation presents the best results. The harmonics generated in this section are low enough to excite the DUT and to produce products in a mixer when the signal is desired to operate as a local oscillator. The fact of IT has four SLSM4 available make this solution possible, if they were not available it would be impossible to implement this solution, as one SLSM4 cost about 1000 Euros.

Figure 3.14: CW Generator solutions

Chapter 4

Arbitrary Waveform Generator

The mixed-domain vector network analyzer is calibrated for one tone and two tone, so the stimulus signal generator needs to generate these two kinds of excitation signals. The previous chapter presented the one tone solution. This chapter is devoted to the Arbitrary Waveform Generator implementation that has to produce a two tone signal to stimulate the DUT.

Chapter two presented different architectures that can produce the desired signals. For two tone mechanism, the realization developed in the previous chapter can be used with a power combiner and an isolator, figure 2.11. This solution works but it is not so interesting and to implement it, two more SLSM4 are necessary, which is not available.

Another solution is desired and by consulting chapter two, it is possible to observe that the architecture of an arbitrary waveform generator is an interesting solution, creating band base signals in digital domain and then convert to the analog domain, to further be up-converted by using an IQ modulator.

Looking at the IT stock, a dual dac evaluation board from Texas Instruments is available, this DAC has a maximum 275 Msps, which is more than sufficient. The main problem is to generate the signals in the digital domain, but in the lab, there is a Logic Analyzer which has incorporated a Pattern Generator. The Logic Analyzer (LA) stays for a digital signal as the oscilloscope stays for an analog signal. The LA allows watching a digital signal in time. One of the mains differences between the two is the number of channels. While LAs have several channels, from 34 to hundreds of channels, an oscilloscope has only 2 or 4 channels, typically. Usually, included in the LA instrument is a Pattern Generator. It can generate digital signals. The LA that is available on the lab is the Agilent 16800. It has a Pattern Generator module that has 24 channels at 300 MHz clock, 48 channels at 180 MHz clock [37].

It was decided that the two tone mechanism solution will be similar to the AWG architecture, to take advantage of the LA. In the mixed-domain vector network analyzer, the LA is used to read the signals that come from the device under test (DUT), with this configuration the PG in the LA will produce the two tone stimulus signal.

All the blocks will be examined in this chapter, all in different sections and subsections. At each section the necessary results will be presented with the purpose to explain each signal transformation and procedure in this two tone generation mechanism.

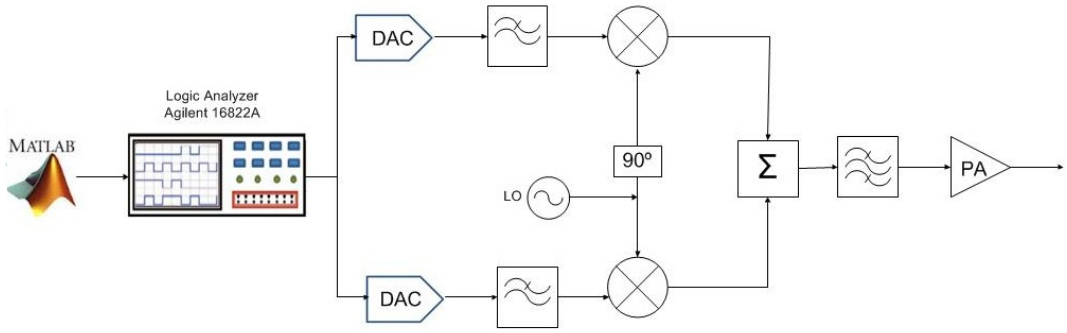

Figure 4.1: Block Diagram of two tone mechanism

Before presenting the AWG implementation, it is useful to define the main characteristics that this generator needs to realize.

Summarizing the considerations about the AWG:

- Two-tone generator;
- Frequency range, 40 MHz to 1060 MHz;
- Output power close to 0 dBm;
- 50 Ω output impedance;
- Low Cost.

Another consideration that could be done is the tone-spacing, but at this point of the project it is not so relevant, this matter will be treated further in this chapter.

4.1 Matlab to Logic Analyzer

Following the block diagram presented on figure 4.1, the first step is to make a connection between the Matlab and the Logic Analyzer. This connection is possible to be done by Local Area Network(LAN)- Ethernet, which is a wireless communication so it facilities the work to be done. According to the information provided in LA's manuals, the connection was done.

The Pattern Generator is organized in sequences that are list of test vectors. These vectors settle on the pattern output at each clock cycle, on the rising edge of the clock. There are two sequences, an init sequence (initialization sequence) and the main sequence. Init sequence is used to place the system in a known state, it is only executed once. The main sequence is used for the actual pattern generation that stimulates your system under test; this sequence loops if a start repetitive execution is performed. To create the vector, first it is necessary to create a signal in Matlab [38].

```
f = 5e6; %desired output frequency
fs = 120e6;   %sampling frequency
ts = 1/fs;
t = ts:ts:10/fcarrier;
partition = -1:2/4095:1;%12 bit scale
```

```
% Create CW signal
x2 = sin(2*pi*t*fcarrier);
Xin2 = x2/max(x2);
Xquant2 = quantiz(Xin2,partition);
```

The code is not complex, it generates the waveform according to the equation, in the example above it is a sine wave, this equation needs to take count the sampling frequency. Another concern that is necessary to be done is the number of bits. The DAC that was used (explained in the next section) receives 12 bits so it is necessary to convert the values to a 12 bit scale, but not using the full scale, because it corrupts the output spectrum of the DAC .

In chapter 2, when the two-tone case was studied, the I channel for the IQ Modulator shall be a cosine wave and for the Q channel shall be a sine wave, so in the LA one channel was programmed as a cosine wave and other channel with a sine wave.

After configuring the Pattern Generator, it is possible to save all the data configured. The full Matlab code is available on Appendix.

4.2 Details on Digital to Analog conversion

With the first block connection done, it is possible to move forward. This step is very important, it gets out of the digital domain and passes to the analog domain. To make this possible it is necessary to use a Digital to Analog Converter, and in the IT's stock there is one available.

The DAC5662 is a monolithic, dual-channel 12-bit, high-speed (the maximum data rate is 275 MSPS) with on-chip voltage reference. The DAC5662 EVM can accept +3.3 V CMOS logic level data inputs. The analog output from the DAC EVM is available via SMA connectors, voltage signal single-ended. The DAC5662 EVM default operation setting is with a single-ended input clock sent to the DAC5662. A 3 V_{pp}, 1.5V offset, 50 % duty cycle external square wave needs to be applied. This input represents a 50 Ω load to the source [39, 40].

The PG has two kinds of pods, data pods and clock pod, it will be discussed separately the two solutions.

The first and necessary consideration is the clock frequency provided by the Logic Analyzer, it cannot be more than 275 MHz (maximum frequency of the DAC). As previous said the LA can provide an internal clock that operates at minimum 1 MHz and maximum of 180 MHz (if it works in full channel) or a maximum of 300 MHz (if it operates in half channel). The internal clock of the LA is enough to be provided to DAC5662, so it is possible to use this DAC [41].

Data Pods

The Data cables from the LA puts out differential values in ECL logic levels and the DAC receives single +3.3 V CMOS logic levels. A level translation and conversion are needed.

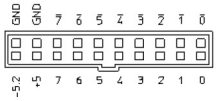

Figure 4.2: Data Cable Pinout [40]

The SN65LVDT348 is high-speed quadruple differential receiver, that can act as a level translator and it converts to single levels. [42] A printed circuit board was produced to resolve this problem.

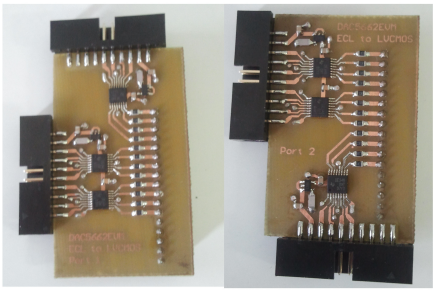

Figure 4.3: Data Pods

By connecting the data cable to the data pod, it is possible to observe the signals in the oscilloscope, in the figure below it is possible to check that the levels are now ready to be provided to the DAC5662.

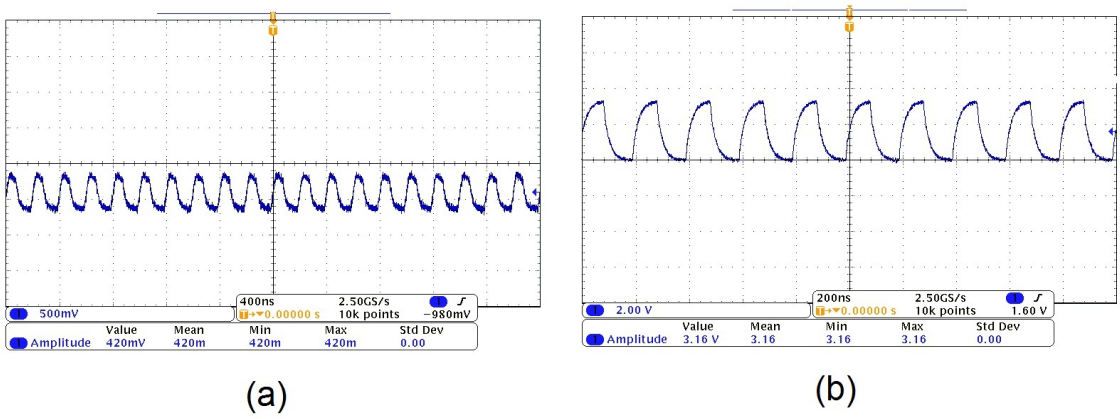

Figure 4.4: ECL to LVCMOS, Data Pod

The figure 4.4(a) presents the ECL levels, where the logic values are negative, typical the voltage correspond to the logic value "0" is -1.75 V and -0.9 V corresponds to the logic value "1". On figure 4.4(b), the same signal is translated to LVCMOS levels, where usually 0 V corresponds to logic level "0" and 3.3 V is voltage referent to logic level "1". The waveforms are not a perfect square waves, this can be due to the capacitance imposed by the probes of the oscilloscope [43].

Clock Pod

The clock pod problem is similar in terms of level translator, so to convert it, the same integrated circuit from TI was used. The CLK cable has a clock input, so the pod also has a clock input, the device to translate CMOS to differential LVECL was MAX9360 from Maxim [44].

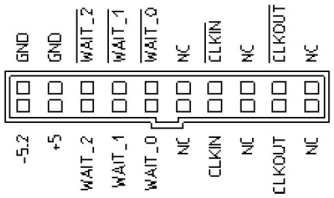

Figure 4.5: Clock Cable Pinout [40]

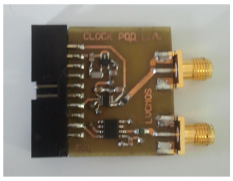

Figure 4.6: Clock Pod

As previous written, the clock port from DAC5662 has 50 ohm impedance. The output of the clock pod is not optimized for a 50 ohm signal. Using an oscilloscope with high bandwidth it is possible to observe the differences.

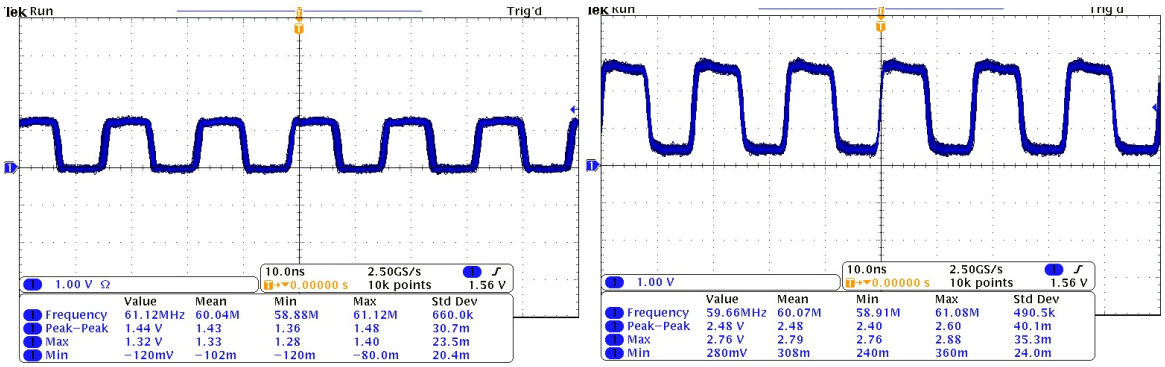

Figure 4.7: Clock Signal, on the left side the 50 ohm and right side the high impedance

The Clock coming from the pod is not useful to the DAC because the maximum level is only 1.32 V, this happens because the output of the developed data pod is not optimized for a 50 ohm impedance. To solve this problem, a several number of solutions are possible, some of them it will be presented here.

External clock applied on the DAC

An external clock can be applied to the DAC. In the RF Lab, there is one AWG (Agilent 33250A 80 MHz bandwidth) that can works as an external clock. Configuring this generator to a square wave of 60 MHz to test the DAC was done, the desired output is 6.5 MHz sine wave, the results were taken from the spectrum analyzer.

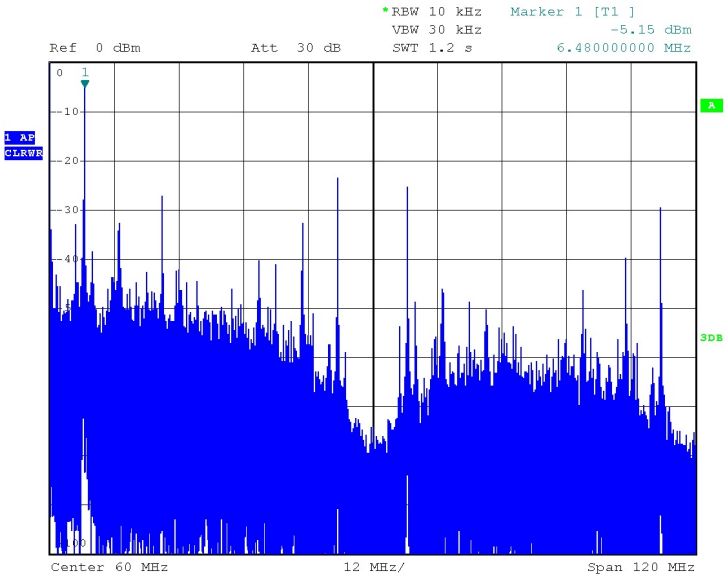

Figure 4.8: Spectrum of the DAC, external CLK signal

In the spectrum there is a lot of spurs and undesired components and a deviation from the desired frequency is also noticed. This can be due to the fact of the clock that originates the data, the LA clock, is not the same applied to the DAC. Also the clock signal that comes from the Agilent 33250A is not a perfect square wave, because the bandwidth of that generator is 80 MHz.

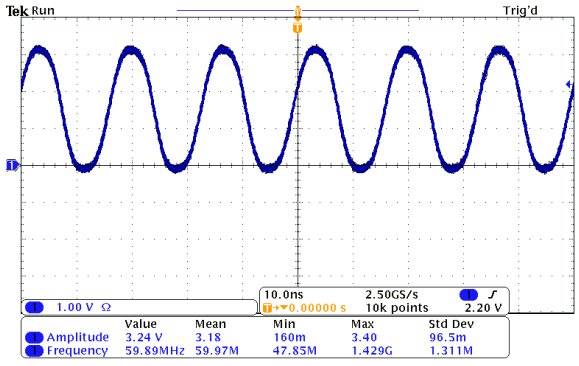

Figure 4.9: CLK signal from Agilent 33250A

This result is not useful but it proves that the LA is putting the values correctly in the DAC. To improve the spectrum, new approaches need to be done.

Amplifying the clock signal from the pod

In the previous solution, it is known that an external signal with determined levels can perform as clock of the DAC5662, so why not to amplify the clock signal from clock pod so that it can be on the same levels of the external clock. To amplify a square signal it is necessary a wide band amplifier, the maximum clock signal can be 180 MHz, so the fifth harmonic is at 900 MHz, the amplifier should have bandwidth higher than 900 MHz. In IT's stock, there is a wide band amplifier (DC to 4 GHz), ERA-4, from Mini-Circuits, gain of 14,2 dB at 1 GHz. An external attenuator of 3 dB was placed so that the signal has the same level as the one provided by the AWG [45].

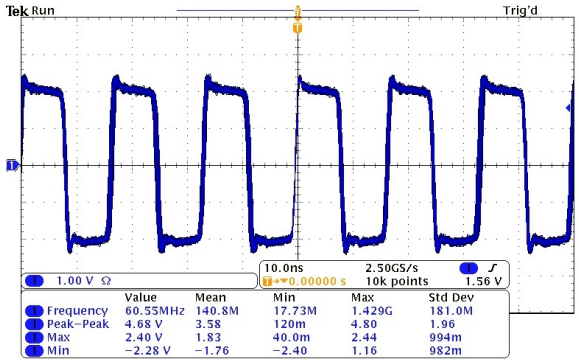

Figure 4.10: Amplified clock from the clock pod

With this configuration it is possible to increase the sampling frequency, various tests were done, here is the figure for a frequency of sampling 140 MHz, the desired output is 6.5 MHz sine wave.

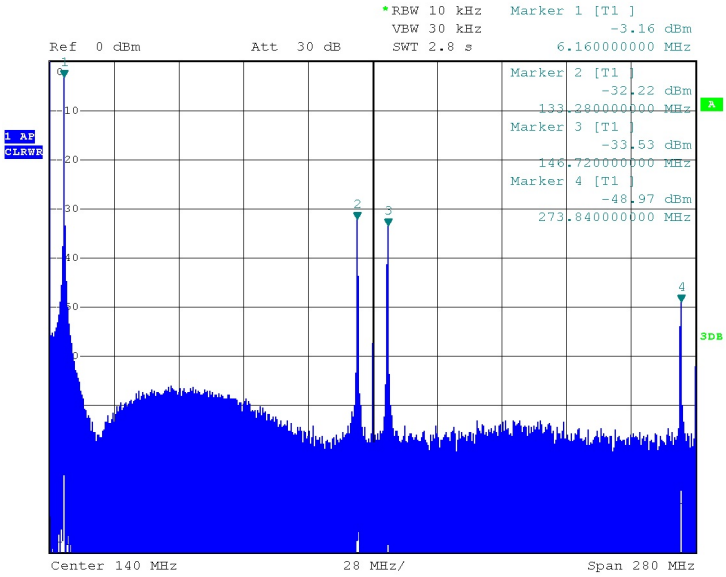

Figure 4.11: Spectrum of the DAC, Solution with ERA-4 ,fs = 140 MHz

The results are much better than the previous solution, the only spurs is the image

frequencies(fs-f;fs+f;2fs-f). There is still a deviation, but it will always exist because the clock from the logic is not directly applied. The cables, connectors, amplifier and the attenuator will delay the signal. This solution is a satisfactory but it is still possible to improve it. Adding a bias-tee, an RF component that adds a DC level to the RF signal, will put the signal between the recommended levels [46].

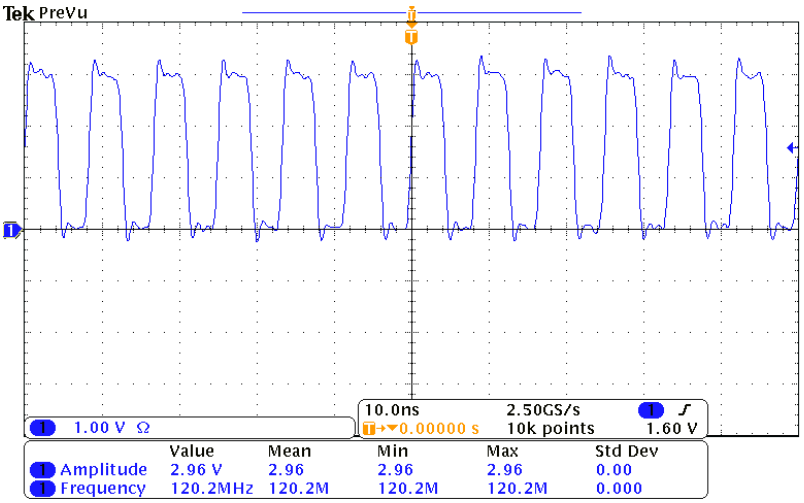

Figure 4.12: Clock Solution with ERA-4 and bias-tee

With the bias-tee, a DC offset was applied to the signal so the negative values disappeared and now the amplitude is close to 3 V as it is recommended on the datasheet. The next figure shows the output spectrum of the DAC when this Clock signal is applied.

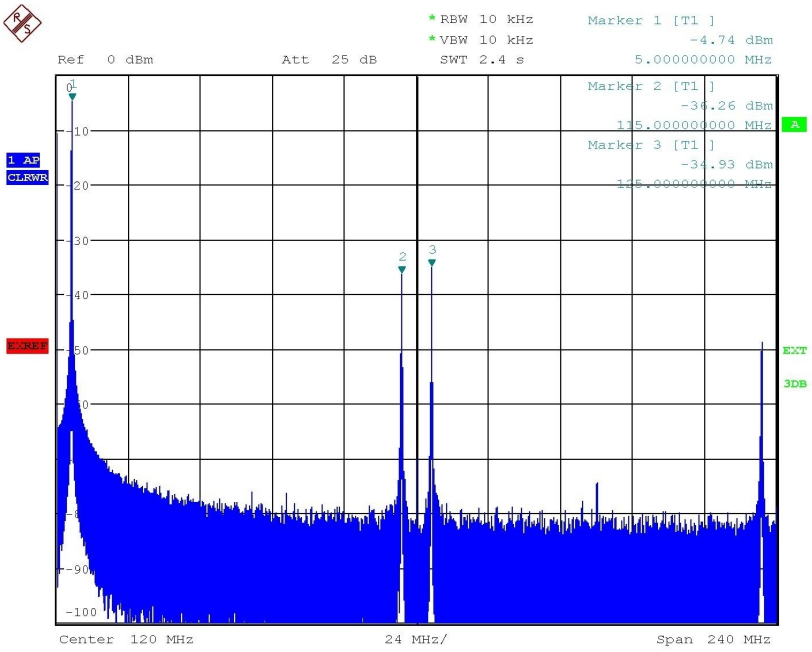

Figure 4.13: Spectrum of the DAC, Solution with ERA-4 and bias-tee, fs = 120 MHz

Comparing to the previous results, this one presents a better spectrum, low noise level, the frequency deviation still exists, due to some inevitable delays between the data signal and clock signal that come from the data pods and clock pod (with ERA-4 and the bias-tee). This solution is satisfactory but the DAC output presents a high phase noise in relation to the expected.

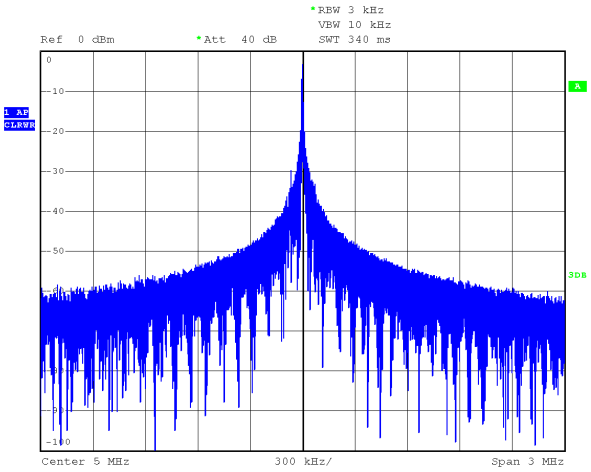

Figure 4.14: Phase Noise at DAC Output

To understand where this phase noise is coming the clock were analyzed in the spectrum analyzer.

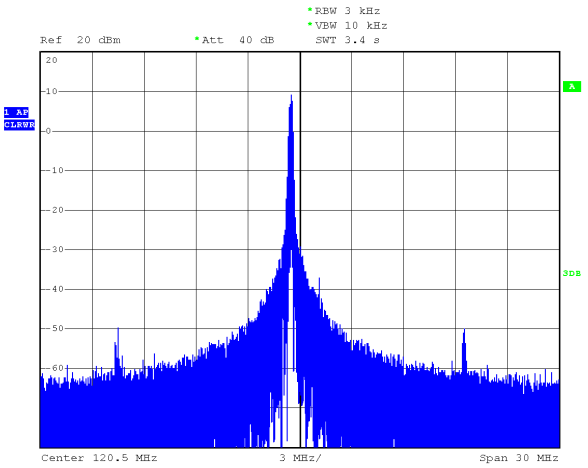

Figure 4.15: Spectrum of the Clock provided from the LA

The clock signal provided by the Logic Analyzer presents a poor quality, high phase noise value. This clock affects the DAC output, although the full spectrum being satisfactory there is still improvements to be done.

External clock applied on the Logic Analyzer

When IT purchased the Logic Analyzer, a clock pod was also acquired, this pod is connectible to the clock cable. At the output of the pod the data is available on PECL levels and the clock signal is not available on SMA connector, so this pod cannot be directly applied to the DAC5562 EVM.

Figure 4.16: Clock cable connected to a Clock pod

With this pod, it is possible to apply a clock signal as an input that can fed the LA. Also this pod makes the same clock available on the CLOCKOUT pin, so this one can fed the DAC. By configuring a scheme like in the next figure, it is possible to feed the LA and the DAC with the same clock signal.

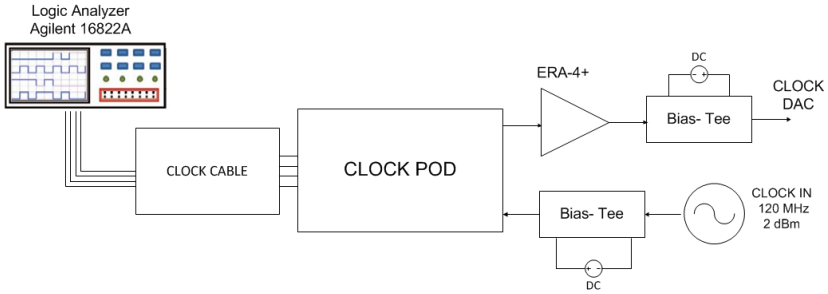

Figure 4.17: Clock Scheme to fed LA and DAC

The ERA-4+ and the two bias-tee are necessary to level up the signal to the desired levels for the input at the clock pod and for the input for the DAC port. To observe the differences of this configuration, the clock signal that feeds the DAC5562 EVM was measured in the Spectrum Analyzer and in the Oscilloscope.

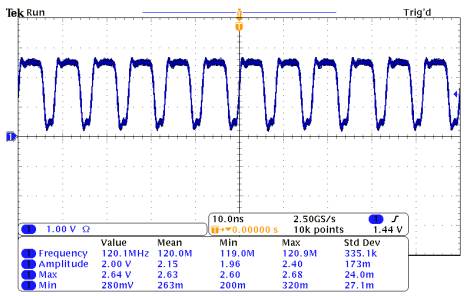

Figure 4.18: New Clock Time Domain

The input clock signal is a sine wave but the clock, transforms this waveform in a square as close as possible, as it is possible to observe in the figure above. The signal levels are enough for the DAC to interpret the signal as a clock signal.

In the frequency domain, to get a more concrete result, the figure was obtained with less span and centered at the fundamental frequency, 120 MHz.

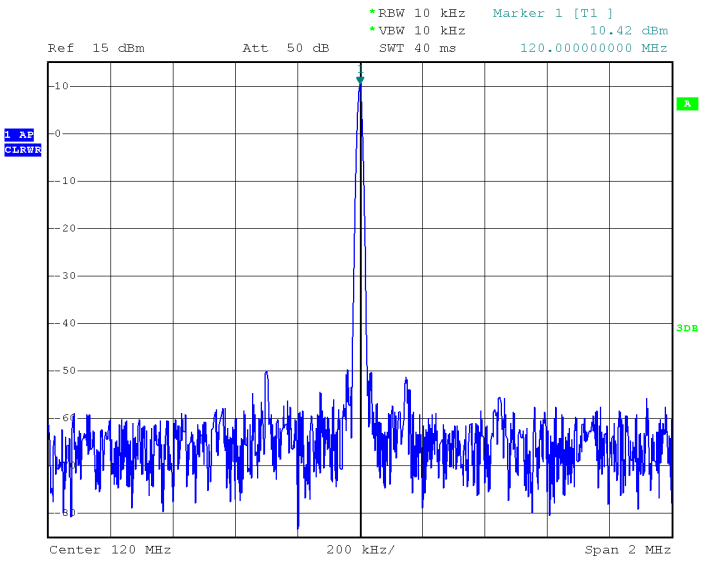

Figure 4.19: New Clock Spectrum

Observing the spectrum it is possible to conclude that the new clock signal presents a lower value of phase noise, the waveform is narrower than the previous one. With this clock applied to the DAC is expected that DAC output will present a low value of phase noise.

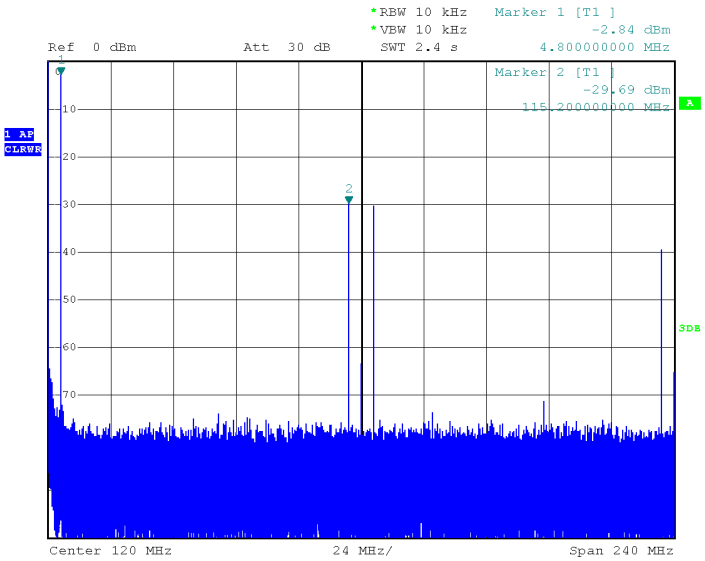

Figure 4.20: DAC output spectrum with new clock applied

The output spectrum present significant improvements about phase noise, the output presents narrow risks but to be more sure about this problem, another figure was taken with the Spectrum Analyzer at the desired output, 5 MHz, but this time, with less span, 3 MHz. The figure allows concluding that the output is almost perfect, phase noise has low values, a little deviation 6 kHz from the desired that is not relevant to continue this project. The output power also increased, 2 dB in relation to the previous solution, to resume the clock problem is completely with very good results. A disadvantage of this solution is the fact that demands some extra components, but all of them are available in IT's which makes no extra costs to this project.

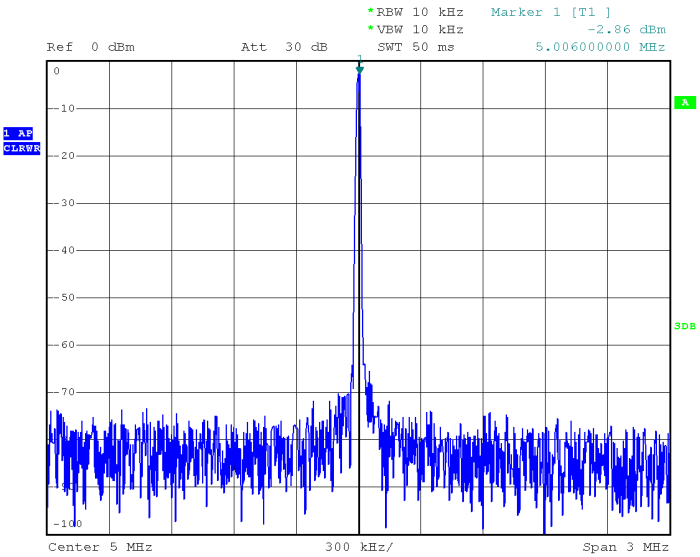

Figure 4.21: DAC output spectrum at 5 MHz, Span = 3 MHz

It is necessary to produce two signals, one for I channel and one for the Q channel. They have the same frequency so the spectrum shall be the same. In the figure below, the two outputs of the DAC in time domain is presented. As it was studied in the chapter 2, this output reveals a stair stepped. This happens because the image frequencies have significant values, to transform these waveform more sine, it is necessary to suppress these undesired components.

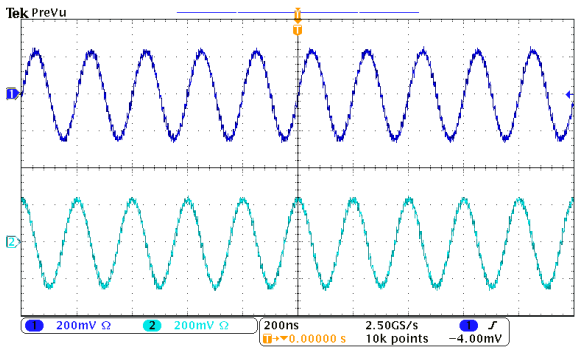

Figure 4.22: In time domain, the output of the DAC

4.3 Low Pass Filter

In the previous results, the DAC5562 output spectrum revealed the image frequencies components that always appeared on the output, making the output signal in time domain a stair stepped. A perfect sine wave is desired to be presented in the inputs of the IQ Modulator, so the image frequencies are undesired components. To eliminate these undesired spectrum's components, a Low Pass Filter was designed. The cut off frequency established was 10 MHz which implies that the base band signals will be at maximum 10 MHz. The filter was first projected on Advanced Design System, then the values of the capacitors and inductors were established according to the ones existing in IT's stock and the best simulation results on ADS.

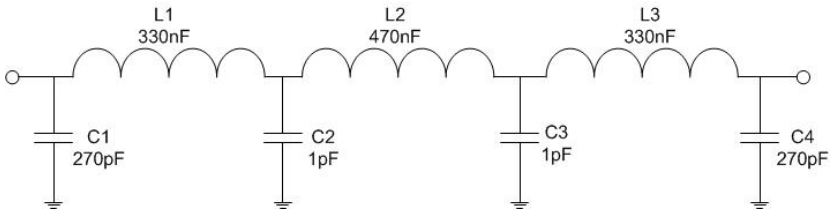

Figure 4.23: Schematic of the low pass filter

To measure the S-Parameters of this filter, the Network Analyzer used was HP8753D, which operates between 30 kHz and 3 GHz. Because the fact of S_{21} is equal to S_{12} and S_{11} is equal to S_{22}, only S_{21} and S_{11} are presented in the figures below.

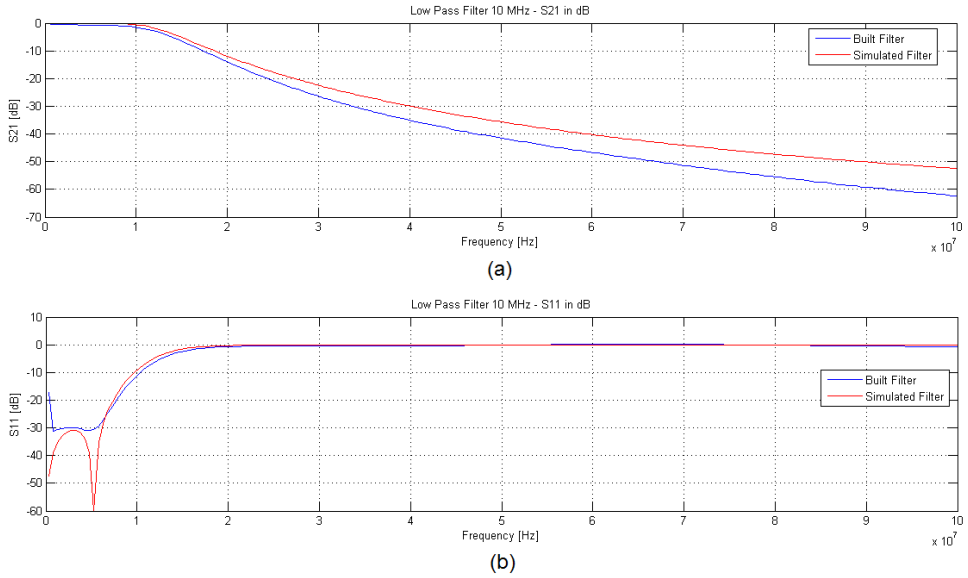

Figure 4.24: S_{21} (a) and S_{11} (b) of the low pass filter

According to the graphics, the results of the built filter are close to the simulated results on ADS. The difference can be due to the fact that on ADS, some parameters were omitted and the resistance value of the inductors considered was a lower value than the real. Although there is little differences, they are not significant to the desired performance of the filter.

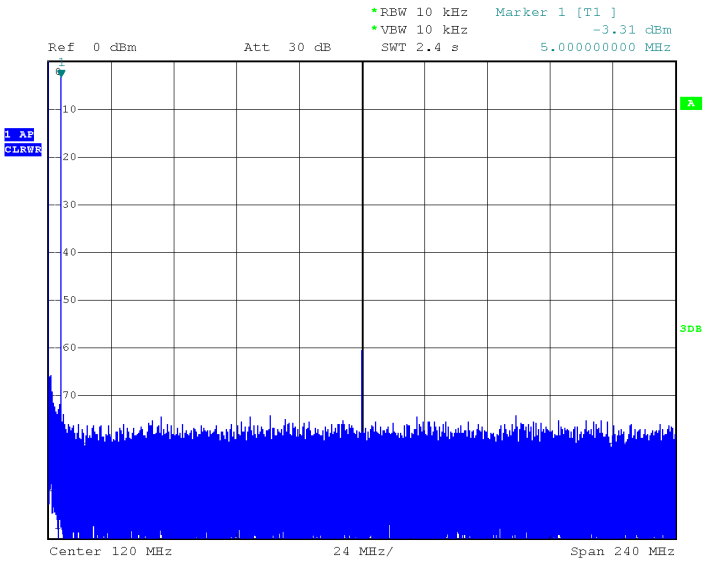

Figure 4.25: Spectrum of the DAC, when filter is applied on the output

The output spectrum reveals that the filter is working well. There is a little attenuation in the band pass but it was expected because the inductors present resistance values different from zero. The results are very satisfactory and observing in the oscilloscope, the waveforms are a perfect sine and cosine waves.

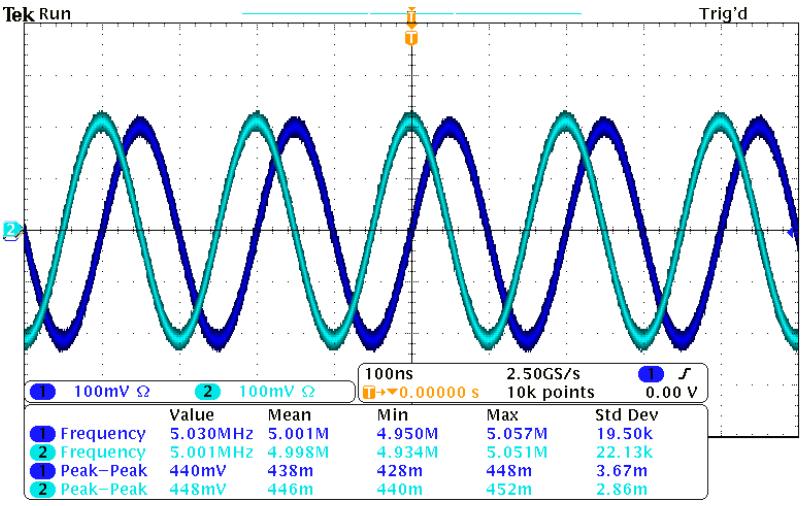

Figure 4.26: In time domain, the output of the DAC after filtering

Also in the figure above it is possible to observe that the waveforms present a 90 degrees phase difference, as one output represents the I (in-phase) signal and the other the Q (quadrature) signal.

4.4 IQ Modulator

The IQ Modulator is the component that will produce the two-tones and up-convert the frequency. This component typically has three inputs and one output. The inputs are the baseband signals, I and Q, and the local oscillator input. The desired IQ Modulator shall fulfill the next requirements.

- Frequency range, 40 MHz to 1000 MHz;
- Output power close to 0 dBm;
- 50 Ω LO input impedance;
- 50 Ω output impedance;
- Low Cost.

After doing some research, an IQ Modulator that fits in the frequency range is LTC5598 (5 MHz to 1600 MHz) from Linear Technology. This integrated circuit has a QFN package, which the PCB and soldering processes developed in DET does not guarantee that this IC works. A test was made, but the results were none. So to continue this project a PCB could be done outside of the University but that implies some extra costs that are not justifiable for this project. [47] A new research was done to find an IQ Modulator that does not present a QFN package, the new requirements are:

- Not a QFN Package or lower size;
- Frequency range close to 40 MHz to 1000 MHz;
- Output power close to 0 dBm;
- 50 Ω LO input impedance;
- 50 Ω output impedance;
- Low Cost.

The ADF8345 from Analog Devices was the component that does not present a QFN package and it works in a frequency range close to 40 MHz-1000 MHz. The AD8345 works in the region of 140 MHz to 1000 MHz and has 16-lead TSSOP package. The LO input is differential but it can be driven single-ended, which is desired in this project. The baseband inputs are driven differentially and should present a common level of 0.7 V, so a conversion single-ended to differential is necessary, these inputs presents a bandwidth of 80 MHz and high impedance. The output of ADF8345 presents 50 Ω impedance [48].

There are other characteristics to take count. The output power is close to 0 dBm if the supply voltage is 5 V and I and Q are 1.2 V_{pp} signals, if the supply voltage is 2.7 V and I and Q signals are 200 mV_{pp} the output power is close to -16 dBm. The LO leakage is about -40 dBm for but it can has a maximum value of -33 dBm when LO is about 800 MHz. The sideband rejection present values like -33 dBc and -48 dBc [48].

Before taking considerations about the output first it is necessary to guarantee that the inputs are in the correct specifications. The LO input, does not consist of a problem because

it can be driven single-ended, so the CW Generator or signal generator from the lab can be used to test the IQ Modulator. The baseband inputs need to be driven differentially and present high impedance so the next subsection presents the solution.

4.4.1 Single-ended to Differential conversion

The ADF8345's baseband inputs are driven differentially with a common level voltage of 0.7 V and an high impedance. The DAC5662 EVM in this project is responsible to produce the baseband signals, the DAC5662 is configured to produce the outputs on single-ended voltage signals and it presents a 50 Ω impedance. It stills possible to change the DAC EVM output, but it was decided to do not change the evaluation board, so a single-ended to differential conversion is necessary [48].

Using a transformer can resolve this problem but on the datasheet from AD8345, there is a suggested amplifier capable of convert single-ended to differential, the amplifier is AD8132. In the IQ datasheet a level of common voltage for I and Q signals is necessary, the AD8132 has one input for setting the common mode voltage. The input of the AD8132 can be optimized for 50 ohm impedance and the output for high impedance, so this amplifier fulfils the necessary requirements [49].

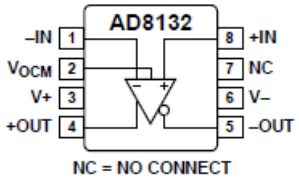

Figure 4.27: AD8132 Pinout

As it is necessary one for I signal and the other for the Q signal, two PCBs were produced. The size shall be small, as this component works as a converter.

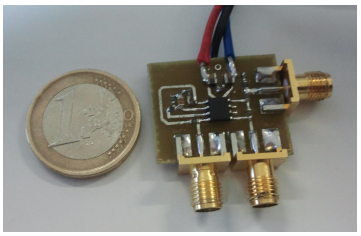

Figure 4.28: AD8132 PCB

Looking at the figure 4.22, the DAC outputs after filtering that will be the input of the AD8132, this signal presents 488 mV_{pp}, so the differential outputs will be around 244 mV_{pp}, which will lead the IQ Modulator to produce the outputs around -16 dBm. The figure in the next page presents the output waveforms, differential signal, of one AD8132.

The frequency of the signals is 5 MHz, which was the desired value. About the levels, they do not present the same level, a small difference that can affect the output power of the IQ Modulator. Although it is not present in the figure, the mean value value that represents the common voltage is about 0.7 V, the recommended common voltage.

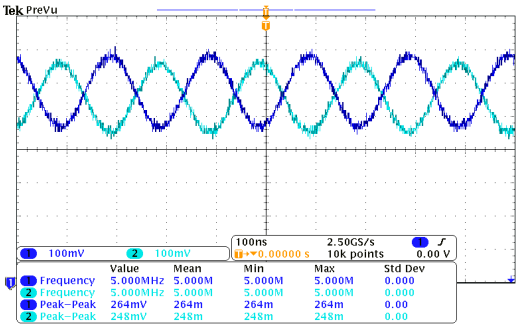

Figure 4.29: Output of AD8132

4.4.2 Results of IQ Modulator

With all inputs in the right configuration, the AD8345 can be tested, a PCB was developed to test this device. The size of this PCB is small which is good, as the size is one of the objectives of this project.

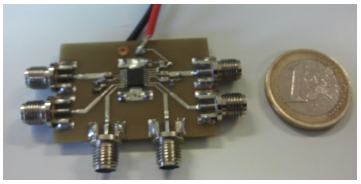

Figure 4.30: AD8345 PCB

With all connections done, the AD8345, can be tested, the inputs are 5 MHz signals with 244 mV_{pp}, the LO has a frequency of 500 MHz and a -2 dBm level. This LO signal comes from a signal generator that is available on the RF lab. At this point it is only necessary to test the equipment so it is not necessary to use the LO developed on chapter 3.

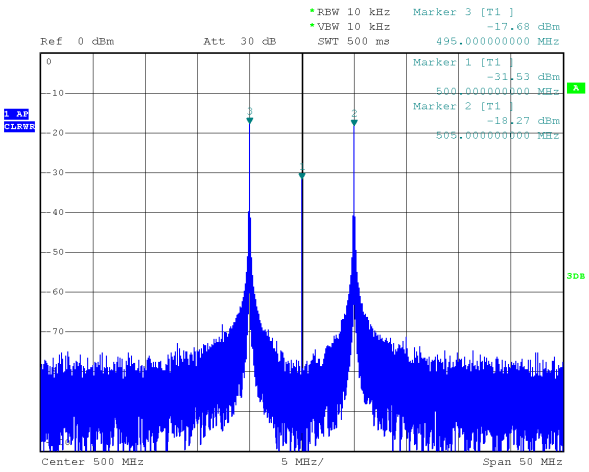

Figure 4.31: Output of AD8345

The levels of the output signal are close to the values expected (around -16 dBm), the small difference can be due to the reason previous presented, and the outputs of AD8132 do not present exactly the same level. The peak in the middle of the tones correspond to the LO leakage, about -31 dBm. In the datasheet the maximum value for LO leakage is about -33 dBm, a little inferior than in practice. This value damages the result, to reduce this leakage one solution can be generating a four-tone signal and then filtering with a high pass filter or a low pass filter to eliminate the LO Leakage and the downside band or upside band, like it was suggested in chapter 2 [48]. This solution works but it reduces a lot the frequency range, so it is out of question. To solve this problem another two approaches will be presented.

Applying a Power Combiner a Phase Splitter

The idea of this solution is to add the output signal from the IQ Modulator with a signal at the same frequency of local oscillator in the IQ Modulator but this signal has a 180 phase difference related to the one that fed the IQ Modulator. The next figure presents a suggested implementation of this approach.

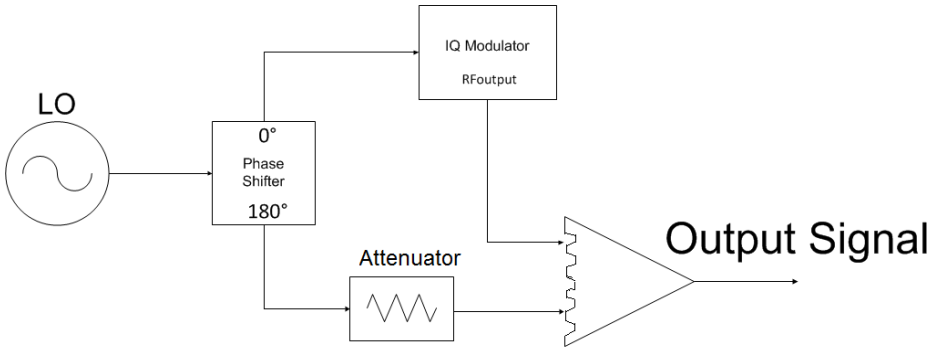

Figure 4.32: Solution to reduce LO leakage

This solution cannot work due to the fact that the signals are only guaranteed to present a 180 phase difference on the output of the phase shifter, at the input of the power combiner they cannot present that phase difference, which can lead to a sum instead of a subtraction.

Another problem of this implementation is the frequency range of the phase shifter, which normally has a very limited bandwidth. The phase-shifter can be replaced by another RF component a hybrid. The hybrids are splitters that divide the input signal in two signals with a phase difference typically of 90. In comparison to the power splitters the hybrids present less frequency range and less attenuation.

For this implementation, a hybrid like SYPJ-2-13+ from Mini-Circuits, that operates from 10 MHz to 1000 MHz and the outputs present a 180 phase difference can be useful. In the RF Lab stock it is not available any hybrid that works in the desired frequency range, so to implement this solution it is necessary to acquire a hybrid, the one referred from Mini-Circuits, but because of its price and time delivery, this solution is out of question [50].

Changing the Offset Voltage

By consulting [51, 52], the LO Leakage is a common problem in IQ Modulators. In both documents the same solution is implemented. This solution consists in varying the DC offset voltage of I and Q, a combination of these variations will lead to an optimal point where the LO Leakage is about -70/-80 dBm.

The process starts to vary one of the offsets, I or Q, in the figure below the I was the first to be varied so Q stays constant. The minimum LO Leakage, -40 dBm, for the first variation was found when the I offset was $200\mu V$. The next variation has I fixed at $200\mu V$ and Q varies, when Q is equal to $400\mu V$ the LO Leakage presents the minimum value for the second pass, around -50 dBm. A third pass is done by maintaining Q offset at $400\mu V$ and sweeping the I offset. At $150\mu V$ the LO Leakage presents its minimum value, around -75 dBm.

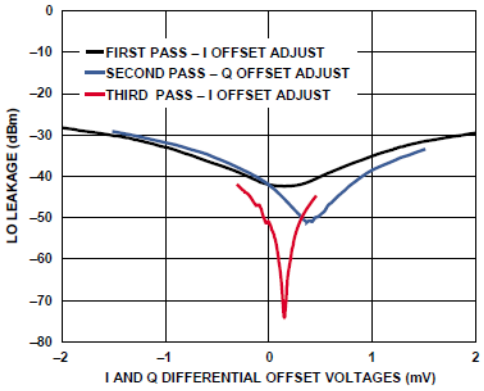

Figure 4.33: LO Leakage Compensation [52]

The offset voltages are applied on the DAC outputs, which typically include auxiliary ports to add this offset. The DAC5662 EVM does not include these ports and the outputs are configured to be driven in single-ended voltage signals, to put the outputs configured in differential signals it is necessary to remove components from the evaluation module but it was decided to do not change the EVM.

An offset voltage can be applied to the single-ended but as it is possible to observe on figure 4.33, these offset signals are very small signals, around 100 and $400\mu V$, at the IT's there is no power supply working in these ranges, so this solution cannot be tested.

4.5 Output Stage

The output stage typically in the IQ Modulators is composed by a band-pass filter and a power amplifier to level up the signal. The band-pass filter is used to eliminate the undesired components out of the band of interest produced by the IQ Modulator like spurs and harmonics. In this project the desired frequency range is between 40 MHz and 1000 MHz, the IQ Modulator operates between 140 MHz and 1000 MHz, a little less than the desired band. Because the IQ Modulator does not work out of band the filter is not necessary, but if the LTC5598, previous IQ Modulator that fits in the desired band, a BPF was necessary to be placed at its output, because that IC works between 5 MHz and 1600 MHz.

About the Power Amplifier, an ERA-4+ can be used, it fulfills the requirements but the problem of applying an amplifier is because of leveling up the LO Leakage too. To get the output power of the tones close to 0 dBm, the output can be amplified but the LO Leakage will also increase due to the amplifier. Another chance to set the output power of the tones close to 0 dBm is to place amplifiers after the filter to level up the signal to 2.4 V_{pp}, so the baseband inputs of IQ Modulator can be at 1.2 V_{pp} to place the output power of the IQ Modulator close to 0 dBm. With this last configuration the PA is not necessary because the signal is in the desired output power.

4.6 Conclusion

The work developed in this chapter was based in the block diagram presented on figure 4.1, that is an architecture very similar to the architectures used in the AWGs where typically a memory or look-up table is the first block of the diagram. The memory in the project was replaced by a Pattern Generator that is available in the LA Agilent 16822A, an instrument available in the RF Lab. This conclusion will analyze block by block until the end of the chain.

The programming of the PG by using Matlab was successful achieved, one aspect that can matters is the time that is spend to fill the vectors in the PG, it depends the number of samples, more samples more time to program the PG. This problem can be avoided by saving the configuration in Matlab, the configuration saves the values of the vectors so the time to load the values is much less than the time to program the vectors. With Matlab is possible to load the PG configurations so different kinds of waveforms can be saved in PG and be loaded almost instantaneously.

The next block, DAC is very important and the results in this area reflect the importance. The first operation realized in this block was the level translation of data levels, which was done successfully. Then the clock presents other problems, like level translation and phase noise. After some approaches, the last one revealed the best results, low phase noise and little frequency deviation. The con of the last clock solution is the need of an external oscillator in comparison to the previous implementations. The final output of the DAC presents an almost ideal spectrum.

To eliminate the frequency images, a filter was designed and built. The filter performance is very satisfactory, as it is possible the output of the filter in the frequency domain (figure 4.10) and in the time domain (figure 4.26), it eliminates the undesired component and presents a little attenuation in the desired pass band. At this point of the project the results are very successful.

After filtering, the IQ Modulator is the block that follows. Because the baseband inputs are driven differentially, a single-ended conversion was done by using an amplifier, AD8132. The output of the amplifier converts to differential but it presents some distortion. With all input requirements fulfill the IQ Modulator was tested, the output present a high LO leakage that stills need to be eliminated. Some solutions were proposed but, the components are not available to test them. Also the IQ Modulator needs to be replaced for another that fits in the entire frequency range, 40 MHz to 1000 MHz, the LTC5598 is one IQ Modulator that can perform the in desired range, but because its package is a QFN, a PCB needs to be made outside of the University which demands extra costs.

Chapter 5

Results

This chapter present the results with all systems integrated, CW Generator and AW Generator. Before analyzing the results of all system integrated, the CW generator results will be compared to one of the signal generators available on the lab, the R&S SMR40. The results of the AWG will be compared to one vector signal generator the R&S SMJ100A also available in the lab. Some extra results as the four-tone signal and eight-tone signal will be presented, the tones spacing is 1 MHz.

5.1 CW Generator results

In all figures the parameters of the Spectrum Analyzer are: Span 2 MHz, Ref Level 10 dBm, Att 20 dB, RBW 10 kHz and VBW 1 kHz.

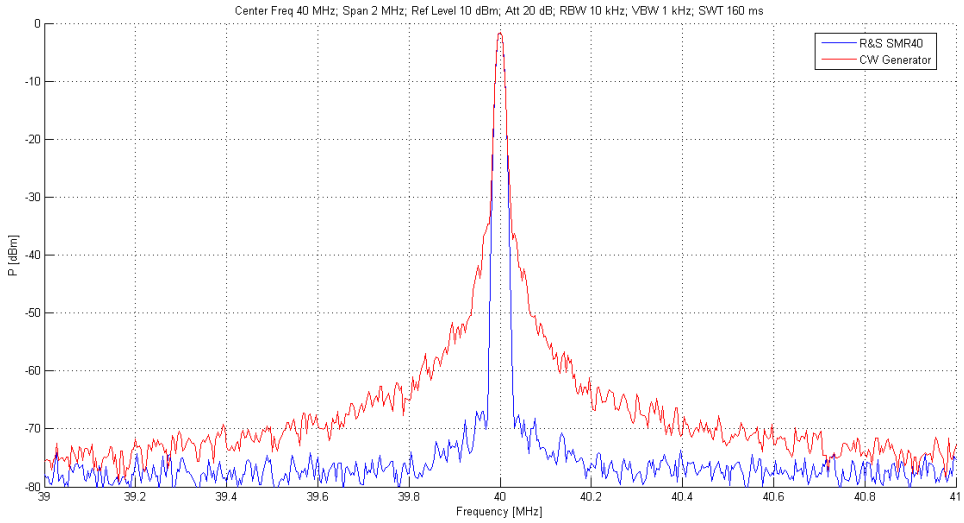

Figure 5.1: CW Generator vs R&S SMR40, 40 MHz

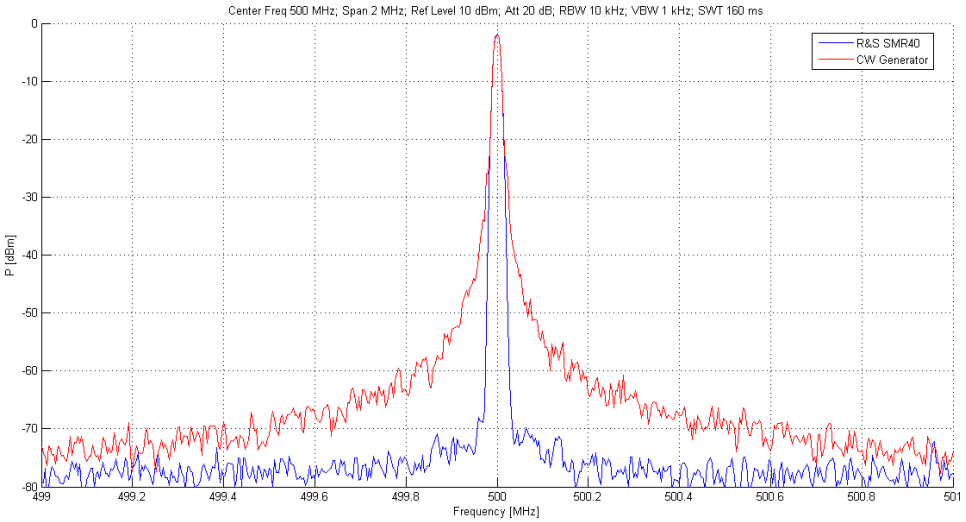

Figure 5.2: CW Generator vs R&S SMR40, 500 MHz

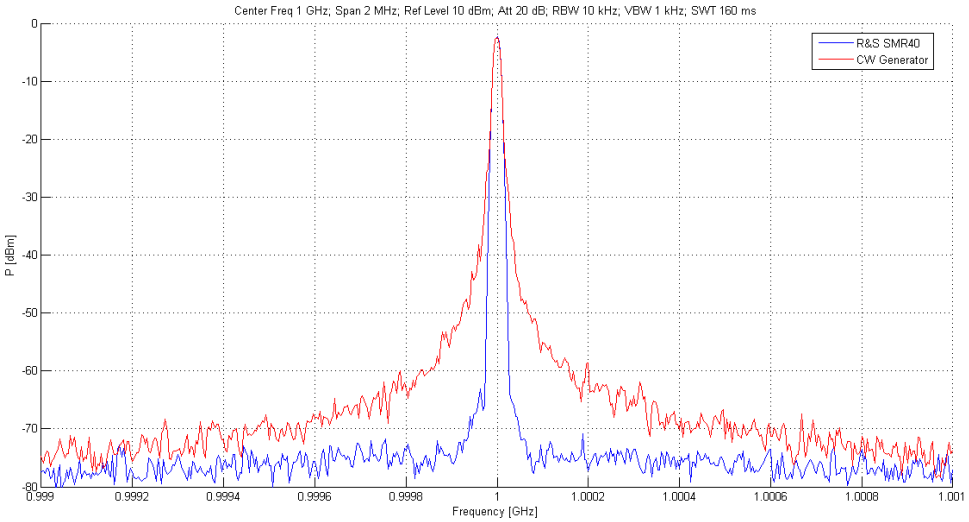

Figure 5.3: CW Generator vs R&S SMR40, 1 GHz

5.2 Arbitrary Waveform Generator results

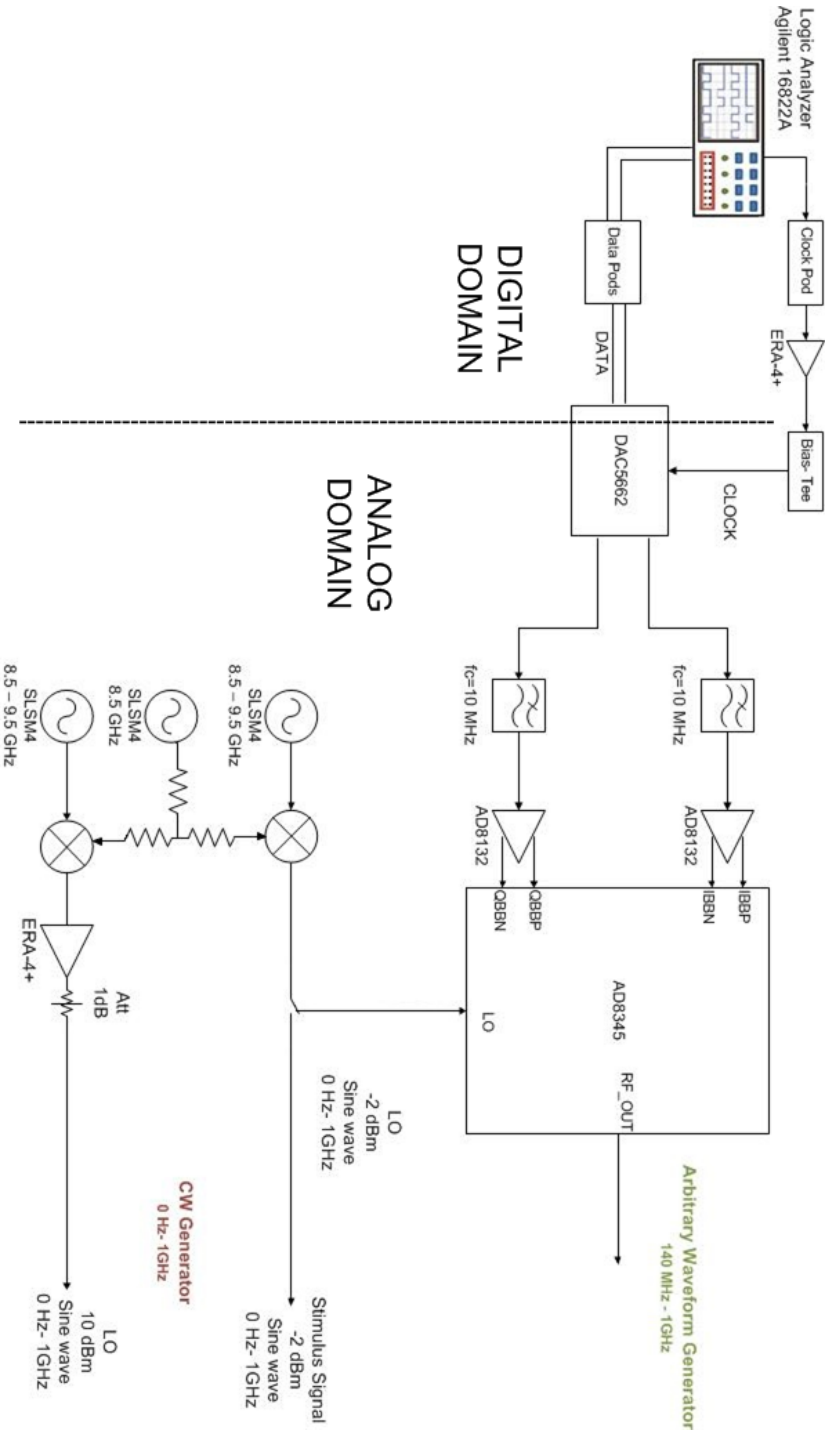

Figure 5.4: Final Arrangement I

In the next figures the parameters of the Spectrum Analyzer are: Span 50 MHz, Ref Level 0 dBm, Att 30 dB, RBW 10 kHz and VBW 10 kHz.

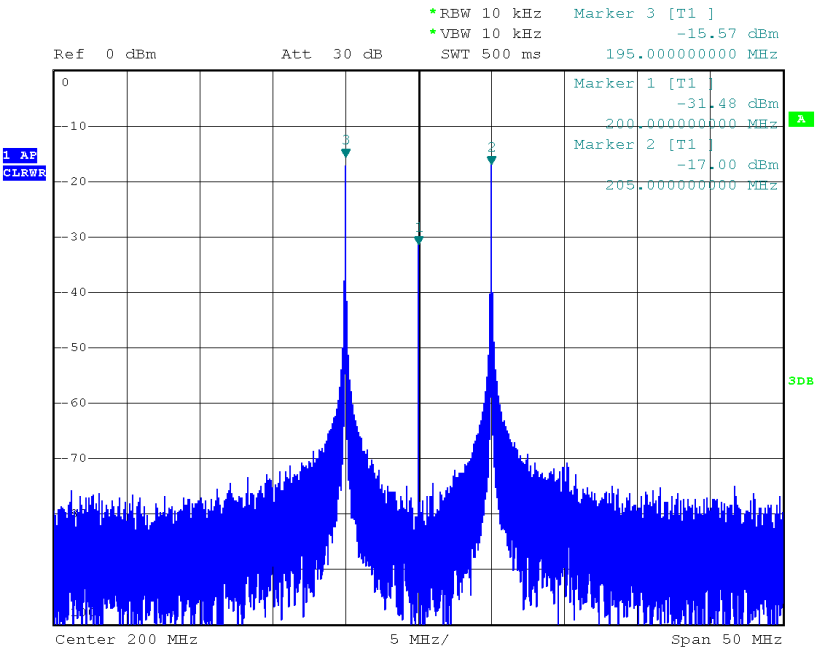

Figure 5.5: AWG output, $f_{lo} = 200$ MHz

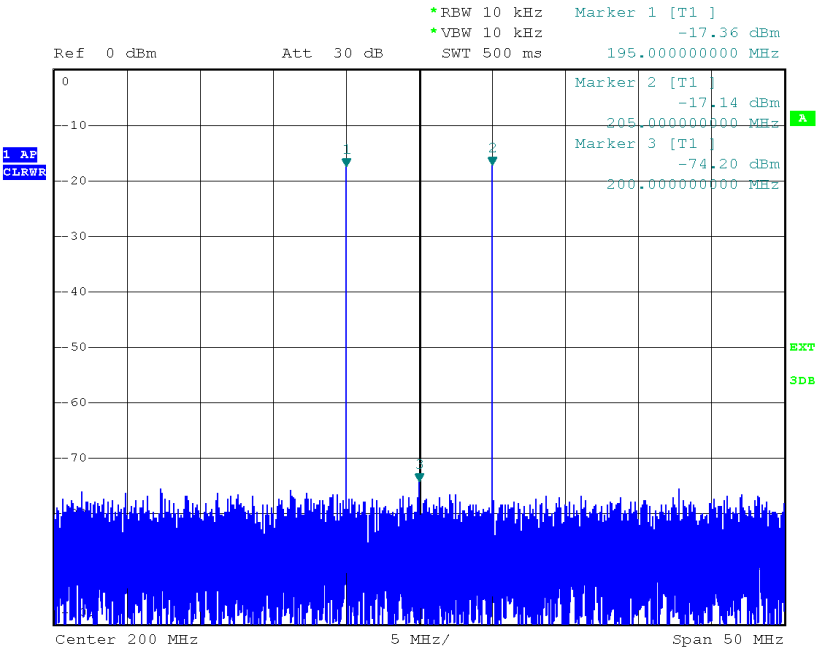

Figure 5.6: R&S SMJ100A output, $f_{lo} = 200$ MHz

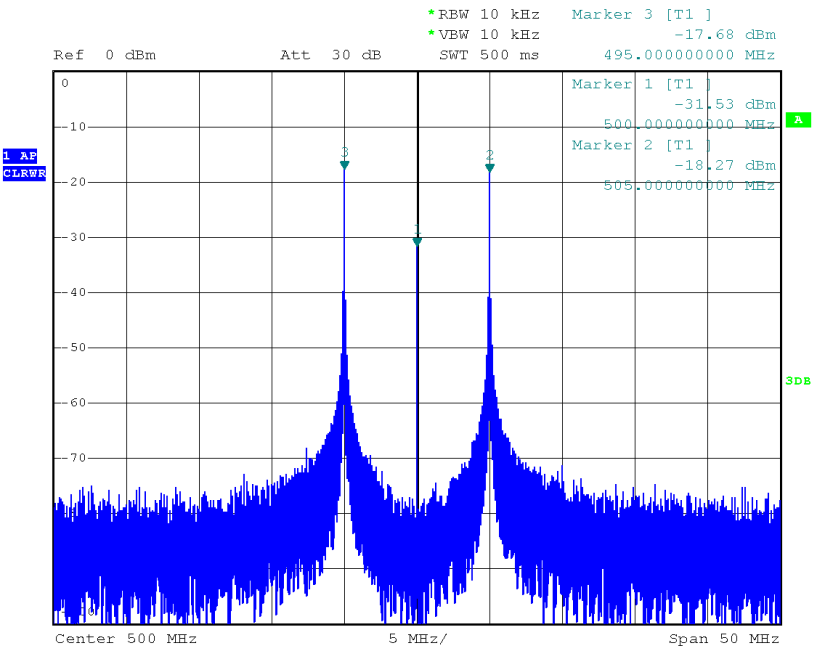

Figure 5.7: AWG output, $f_{lo} = 500$ MHz

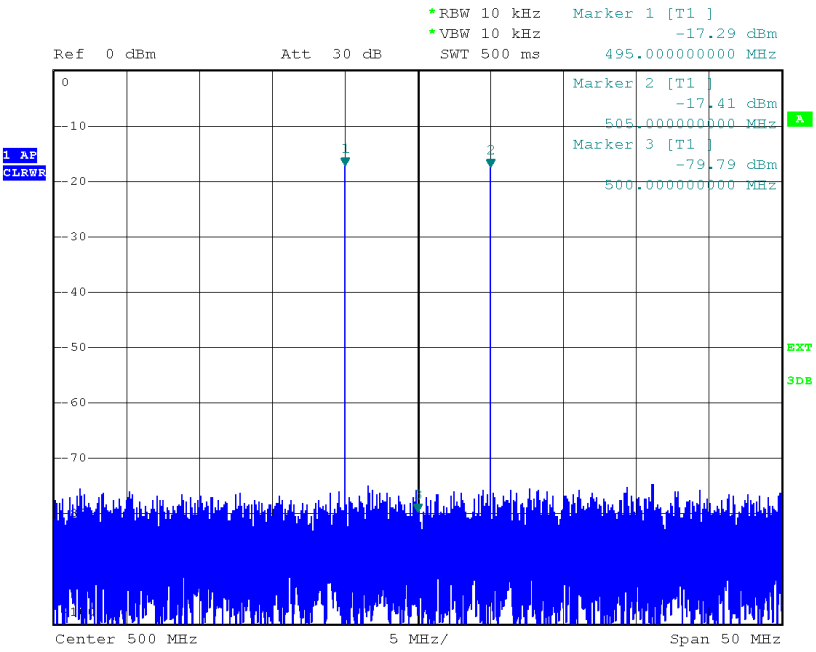

Figure 5.8: R&S SMJ100A output, $f_{lo} = 500$ MHz

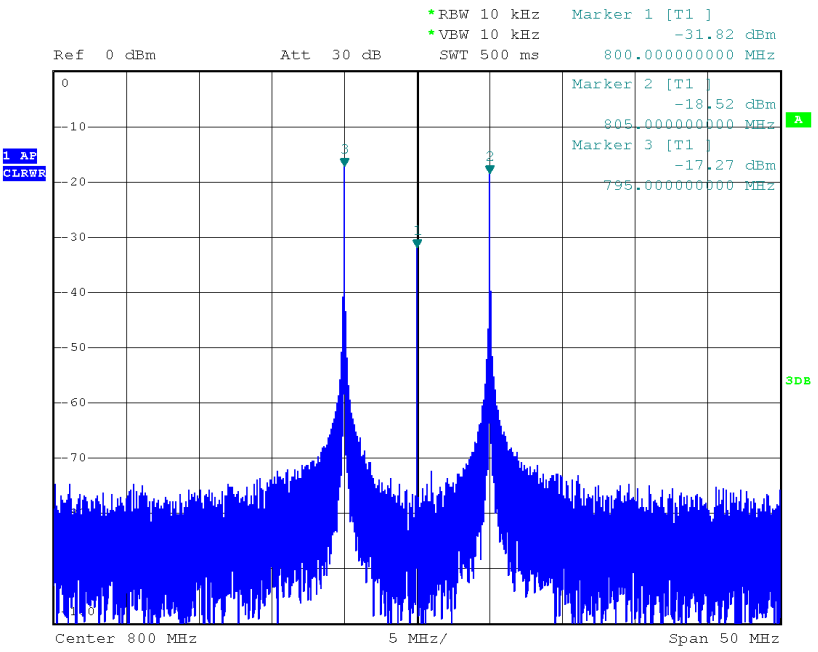

Figure 5.9: AWG output, $f_{lo} = 800$ MHz

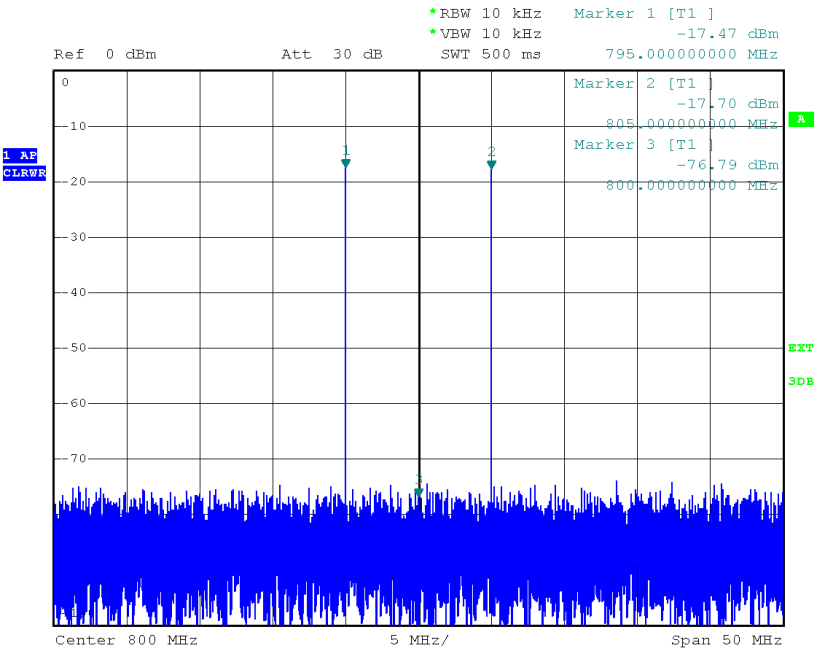

Figure 5.10: R&S SMJ100A output, $f_{lo} = 800$ MHz

Four-Tone Signal

On each DAC5562, the output:

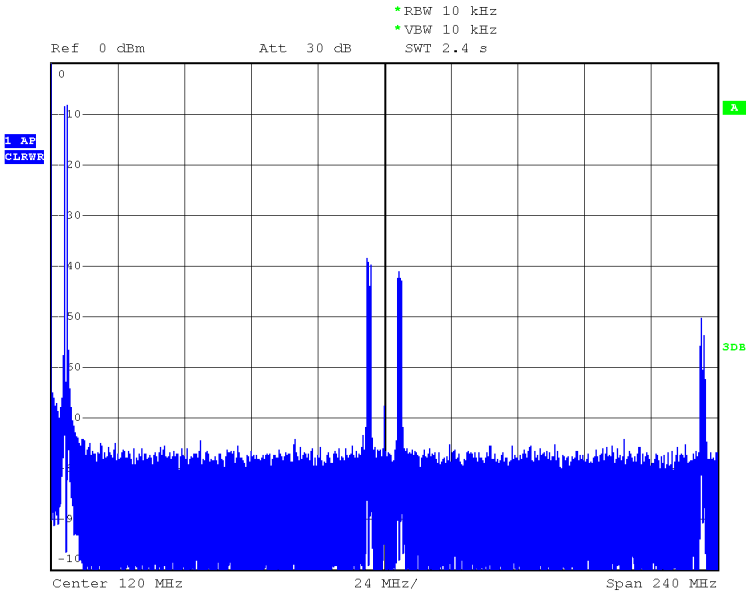

Figure 5.11: DAC output two tones, Span = 240 MHz

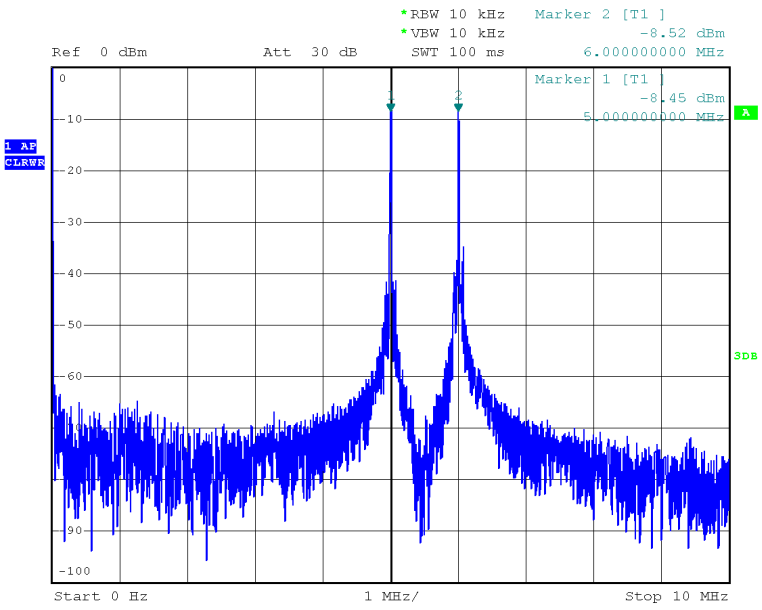

Figure 5.12: DAC output two tones, Span = 10 MHz

In the next figures the parameters of the Spectrum Analyzer are: Span 20 MHz, Ref Level 0 dBm, Att 30 dB, RBW 10 kHz and VBW 10 kHz.

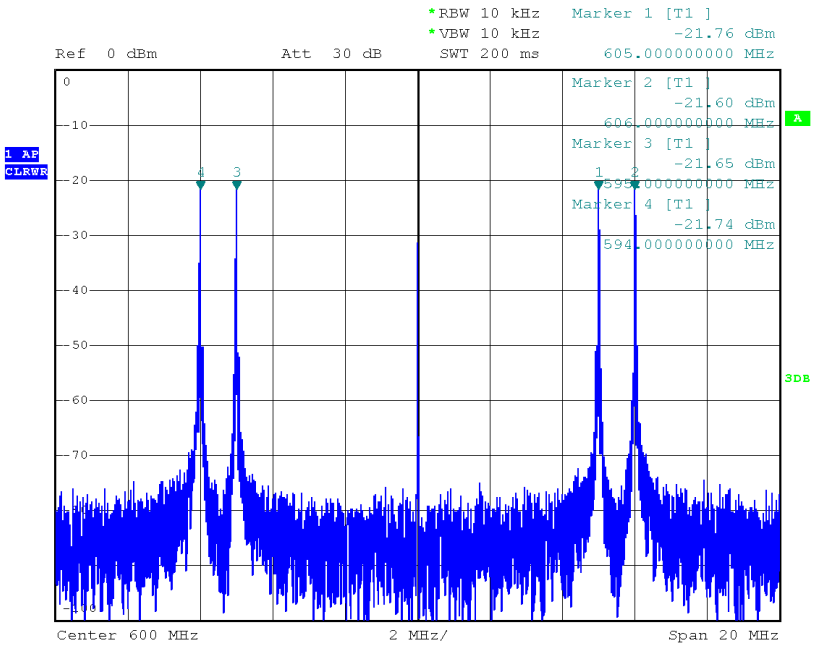

Figure 5.13: AWG output , $f_{lo} = 600$ MHz

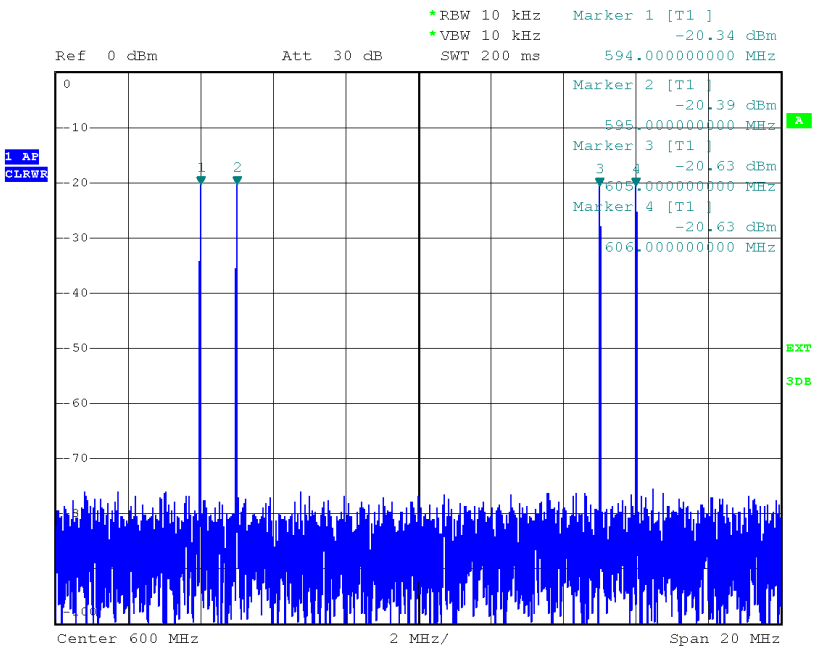

Figure 5.14: R&S SMJ100A output four-tone signal , $f_{lo} = 600$ MHz

5.3 Conclusion

By observing the CW results vs R&S SMR40, the main difference between the two signals is the phase noise, which in CW Generator developed is bigger. The phase noise of the implemented generator is two times the phase noise of SLSM4, the two input signals will be combined in the mixer. One aspect common in both generators, it is the fact that the output power decreases with the increasing of frequency. Other aspects that can be compared are the frequency range, frequency spacing and price but because of the big differences of these values it is not worthy to compare these properties.

The AWG tested was the system on figure 5.4, the results correspond to the expected, a considerable phase noise value and a high LO leakage. The results from R&S SMJ100A present a low phase noise value and a LO leakage of -59 dBc. The phase noise in the tones comes from the DAC5662 as it is possible to observe in figures 4.14 and 5.12. In both generators the output power does not vary much as long the frequency increases and the power of the lower side band, $f_{LO} - f_{BB}$, is a little superior than the power of the other tone $f_{LO} + f_{BB}$.

With the system present in the next page, figure 5.15, that provides an external clock to the LA, the phase noise on the AWG output will decrease, due to the clock that fed the DAC does not present a jitter like the previous one. The figures 5.17 and 5.19 represent the DAC outputs for two-tones and four-tones with the clock applied like in the system on the next page. The phase noise is much less so the output of the AWG shall present better performance. The LO leakage continues to be eliminated, some solutions were present but due to miss of components to test them, it was impossible to test them.

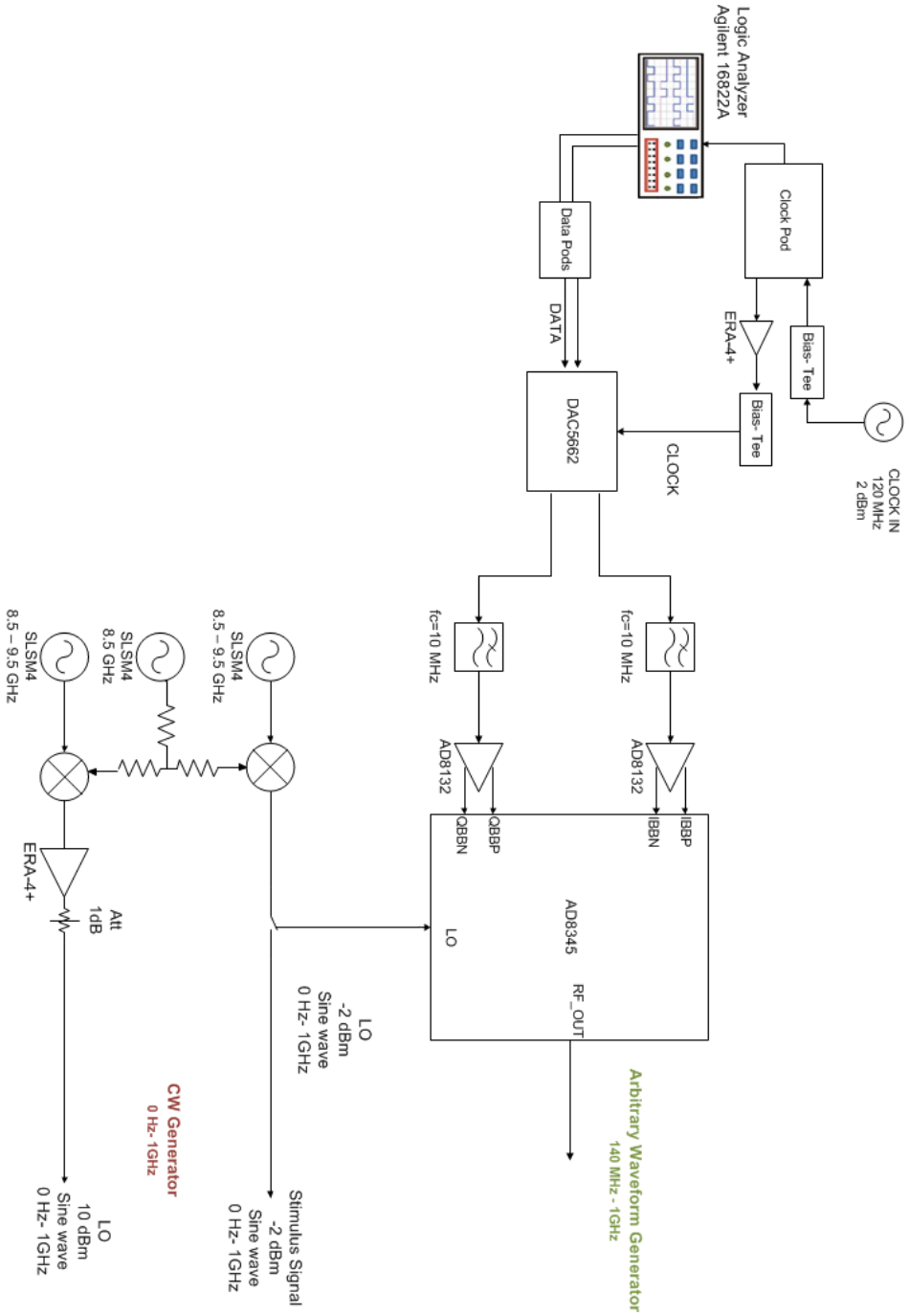

Figure 5.15: Final Arrangement II

Two-Tone Signal

On each DAC5562, the output:

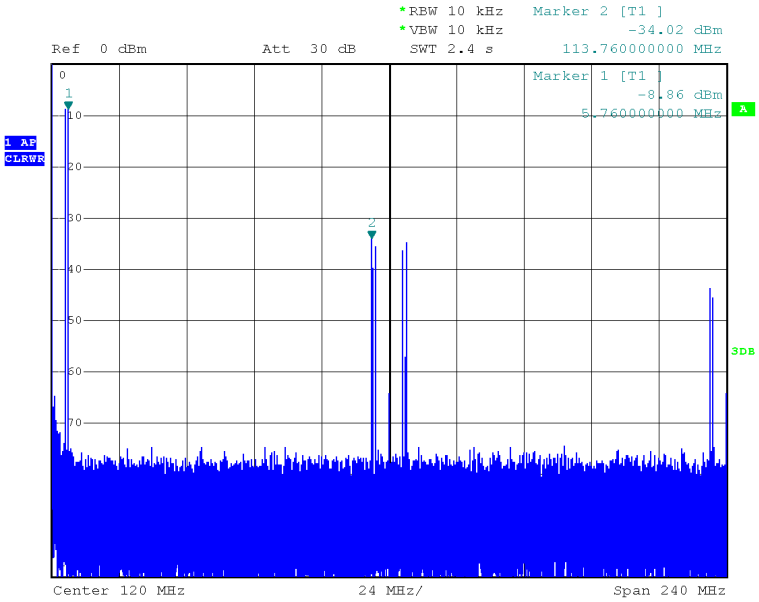

Figure 5.16: DAC output two tones, Span = 240 MHz

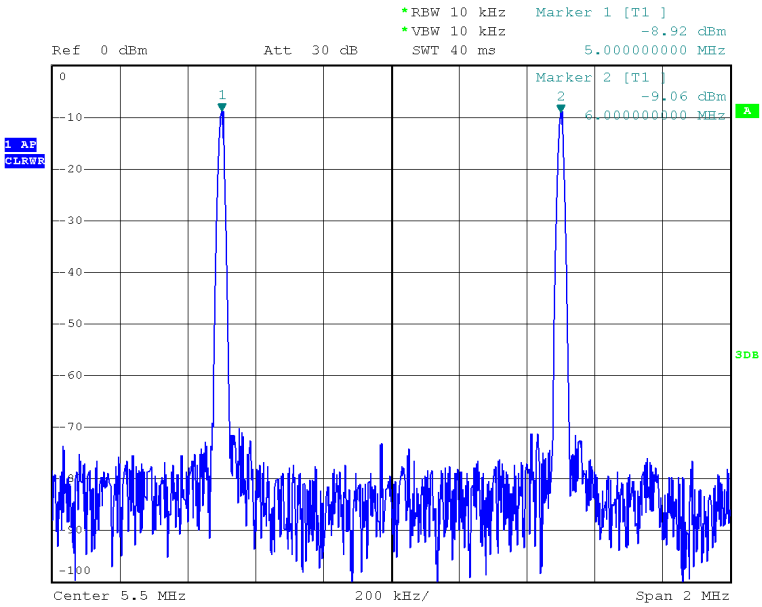

Figure 5.17: DAC output two tones, Span = 2 MHz

Four-Tone Signal

On each DAC5562, the output:

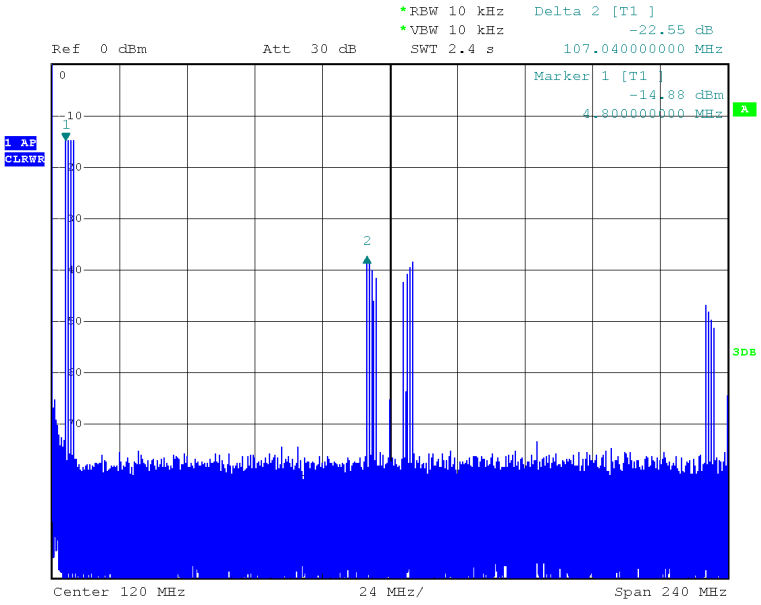

Figure 5.18: DAC output four tones, Span = 240 MHz

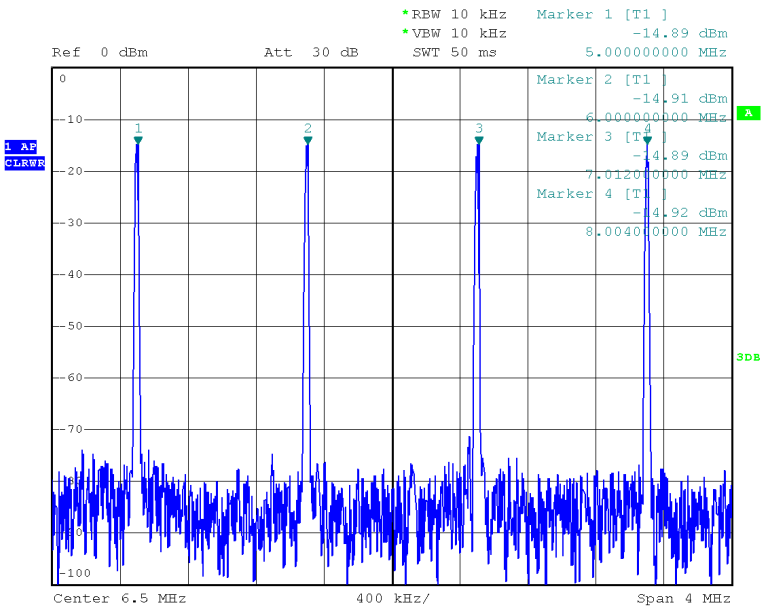

Figure 5.19: DAC output four tones, Span = 4 MHz

Chapter 6

Conclusion

In a global overview, the objectives were accomplished, development of a continuous wave and arbitrary waveform generators. The frequency range is a little less than the initial one desired, the IQ modulator used is the principal responsible for the reduction of the frequency range.

The CW generator that has two outputs, one act as a local oscillator for the mixed-domain measurement system and the other output act as Stimulus Signal for the previous referred system or also act as local oscillator for the IQ Modulator. Two implementations were done, because the output of the first one provided a square wave instead of a sine wave. The second implementation resolved the problem of the first one but for the output that needs to act as local oscillator for the measurement system, there is a loss of 60 MHz in the frequency. It is not a relevant loss, so the in general the performance is quite satisfactory. The size in comparison to the first implementation is a bigger but if it is compared to a normal signal generator is acceptable.

The developed Arbitrary Waveform Generator was an interesting implementation, because it took advantage of the Logic Analyzer available in the RF Laboratory. The LA is a powerful tool and having a Pattern Generator makes the LA more powerful. The AWG developed can be very useful for the RF Lab users, the cost of this implementation was almost zero and the results are very satisfactory. The frequency limitation is due to the IQ Modulator used.

To finish this thesis, some work that can be developed in the future, improvements and add-ons are suggested.

6.1 Future Work

The two generators are tools with a lot of potential and lot of improvements can be done. In CW Generator, some add-ons and improvements that can be done:

- Returning to LMX2541SQ2060E and implement a solution to suppress the harmonics, so the output can be a sine wave. This will lead to an increasing of the frequency range and a size reduction. The disadvantage will be a reduction of the frequency spacing;
- Development of a control board, that includes the DETPIC32, the four inverters used HEF4069UBF and the data converter SN74LVCC3245A;
- Looking in the market for some new RF synthesizers, which fit in the desired region.

The AWG also has a lot of improvement and add-ons to be done, some ideas are presented below:

- Increasing the number of tones to be generated;
- Generate more kinds of signals, for example chirp signals and pulsed signals;
- Change the IQ Modulator, for example to LTC5598, which increases the frequency range and reduces the LO leakage;
- Developing a GUI Interface, in Matlab for example, so a user can chose the type of signal to be displayed.

With all improvements, the entire system can be placed in the measurement system for mixed-domain devices, so that can be a closed box. Another option is to place the system developed in this thesis in a close box, similar to a signal generator.

Appendix

In this chapter, the PCBs developed, the Matlab Code for programming the Logic Analyzer and the C code to program the SLSM4 and LMX2541SQ2060E are provided. Also the S-parameters of the components more relevant in this project will be presented. The parameters were taken by using VNA Agilent PNA E8361C.

PCB Layouts

LMX2541SQ2060E

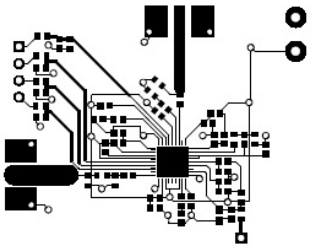

Figure 6.1: LMX2541SQ2060E PCB Layout

SN74LVCC3245A

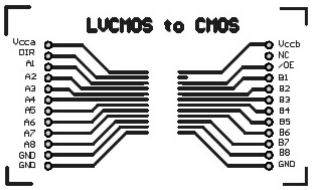

Figure 6.2: SN74LVCC3245A PCB Layout

Low Pass Filter 10 MHz

Figure 6.3: Low Pass Filter PCB Layout

AD8132

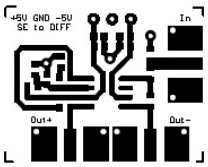

Figure 6.4: AD8132 PCB Layout

AD8345

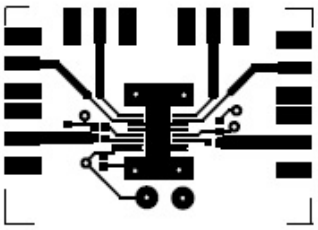

Figure 6.5: AD8345 PCB Layout

S-Parameters

Analog Domain Devices

LMX2541SQ2060E

Return Loss of the input port

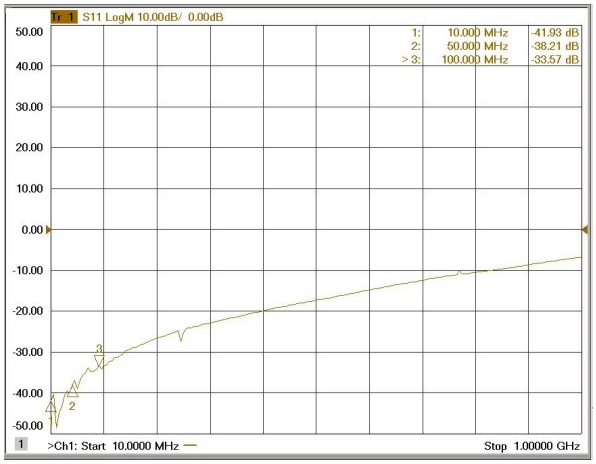

Figure 6.6: Return Loss of the input port of LMX2541SQ2060E

Return Loss of the output port

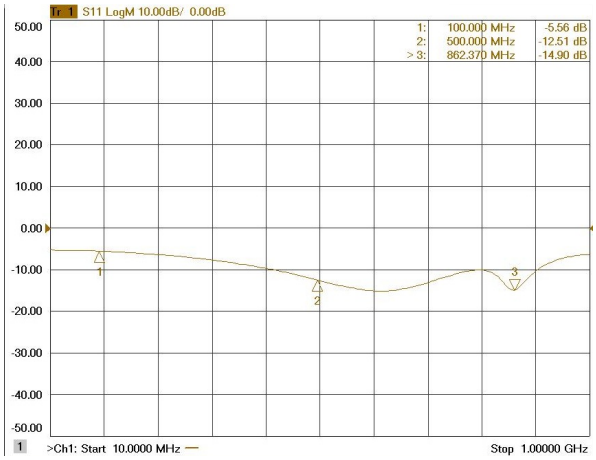

Figure 6.7: Return Loss of the output port of LMX2541SQ2060E

SlSM4

Return Loss of the input port

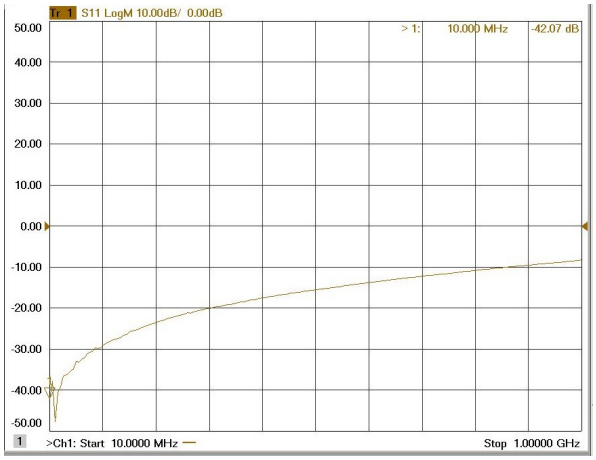

Figure 6.8: Return Loss of the input port of SLSM4

Return Loss of the output port

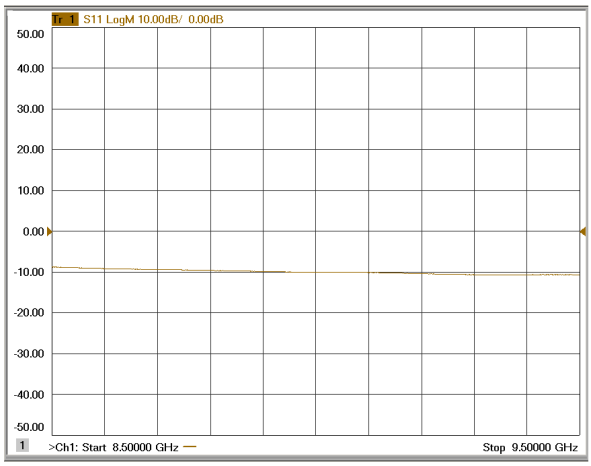

Figure 6.9: Return Loss of the input port of SLSM4

ERA-4+

S_{11}

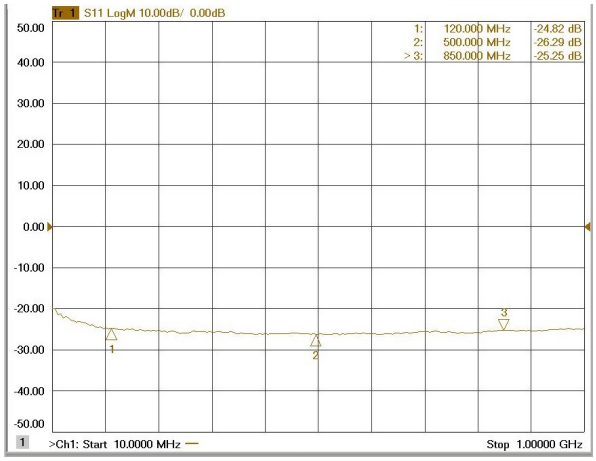

Figure 6.10: S_{11} of ERA-4

S_{21}

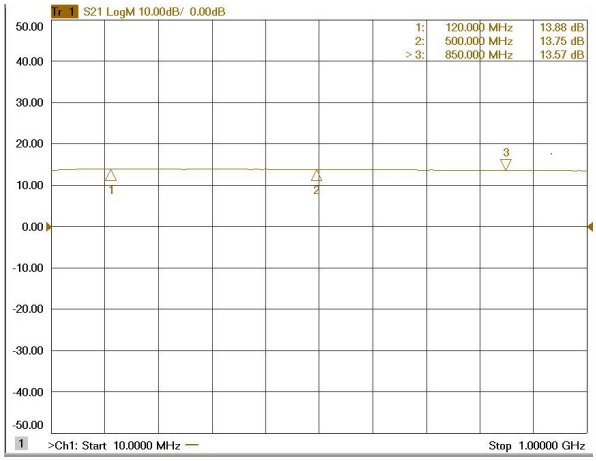

Figure 6.11: S_{21} of ERA-4

S_{12}

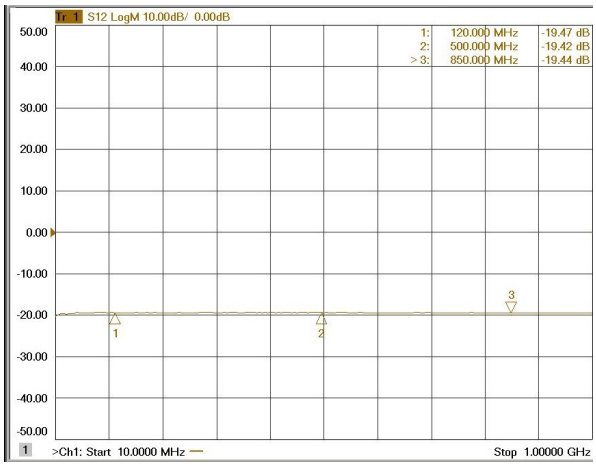

Figure 6.12: S_{12} of ERA-4

S_{22}

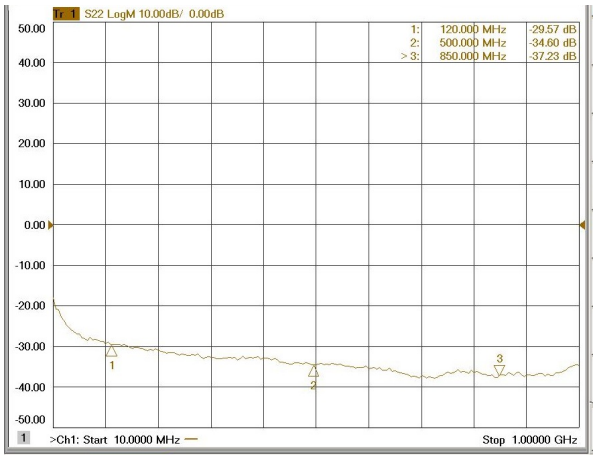

Figure 6.13: S_{22} of ERA-4

Bias-Tee

Return Loss of the RF port

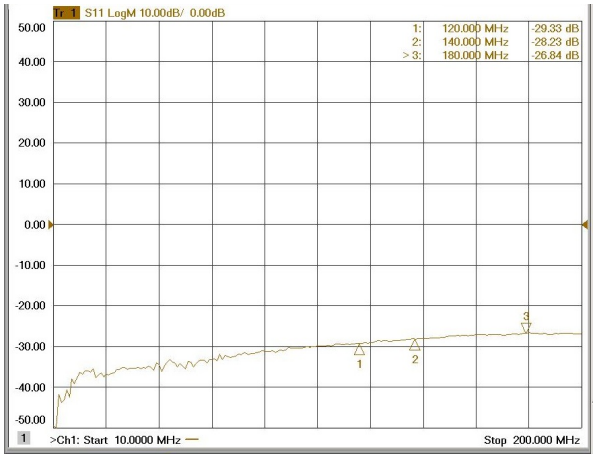

Figure 6.14: Return Loss of the RF port of Bias-Tee

Return Loss of the RF&DC port

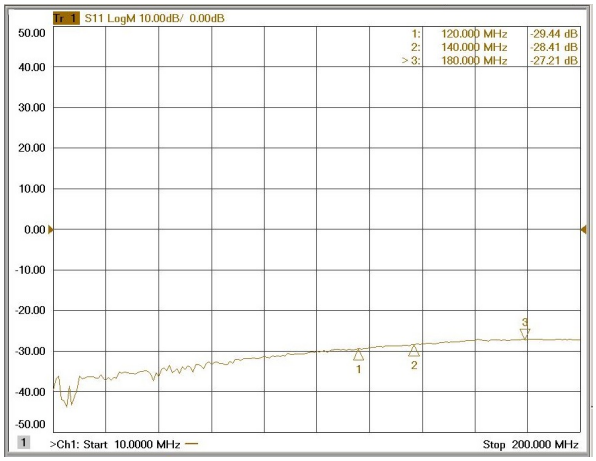

Figure 6.15: Return Loss of the RF&DC port of SLSM4

LPF 10 MHz

S_{11}

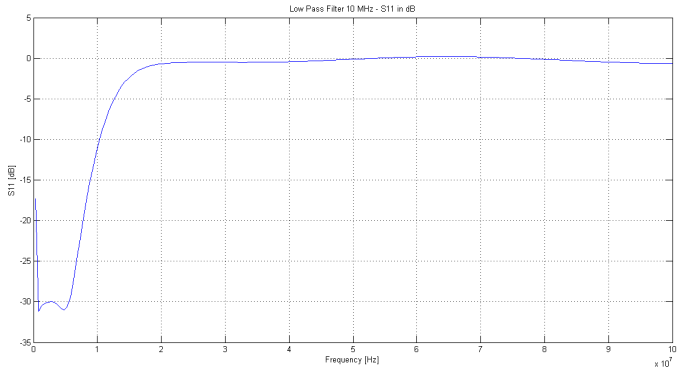

Figure 6.16: S_{11} of LPF

S_{21}

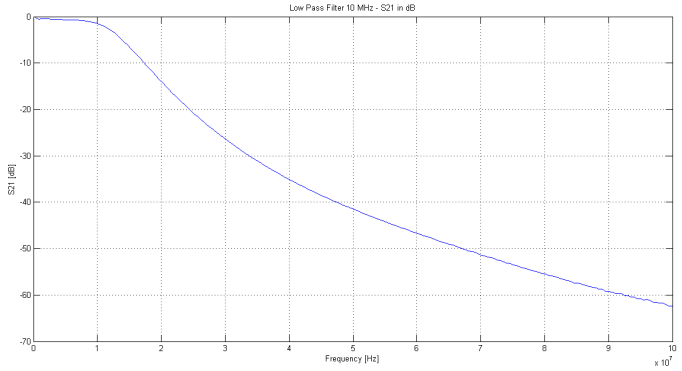

Figure 6.17: S_{21} of LPF

S_{12}

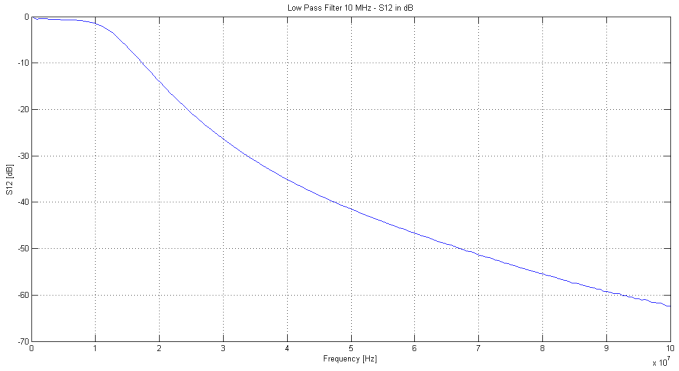

Figure 6.18: S_{12} of LPF

S_{22}

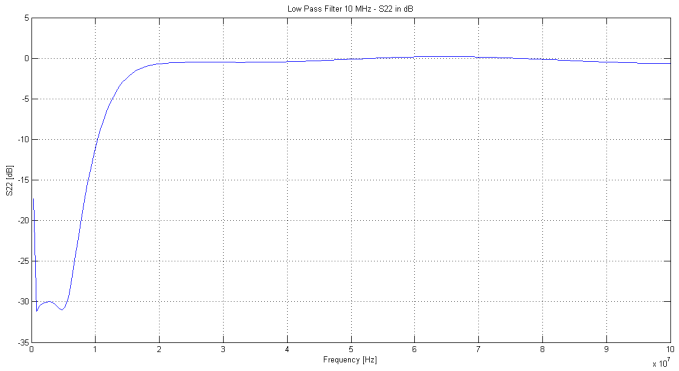

Figure 6.19: S_{22} of LPF

AD8132

Return Loss of the input port

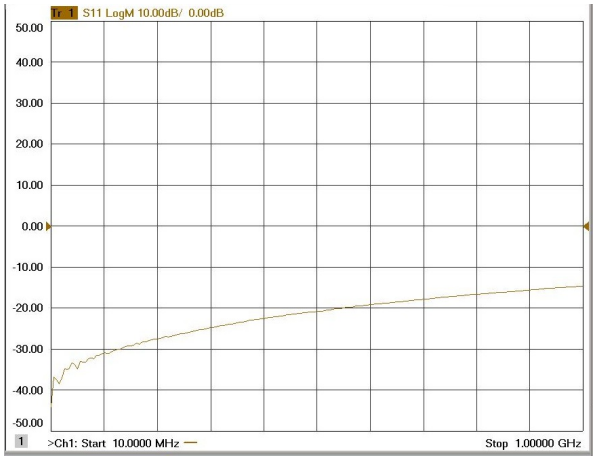

Figure 6.20: Return Loss of the input port of AD8132

AD8345

Return Loss of the LO port

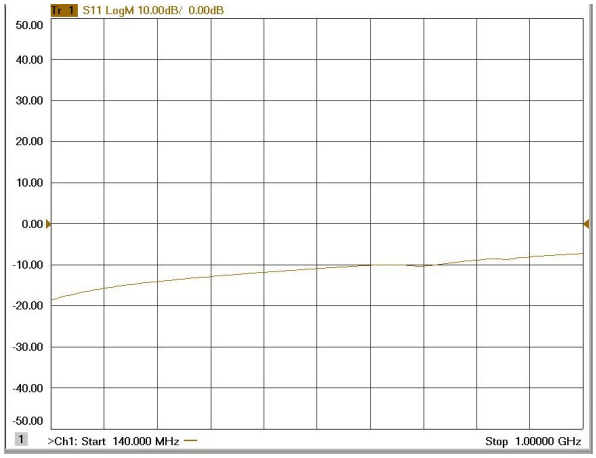

Figure 6.21: Return Loss of the LO port of AD8345

Return Loss of the RF_{out} port

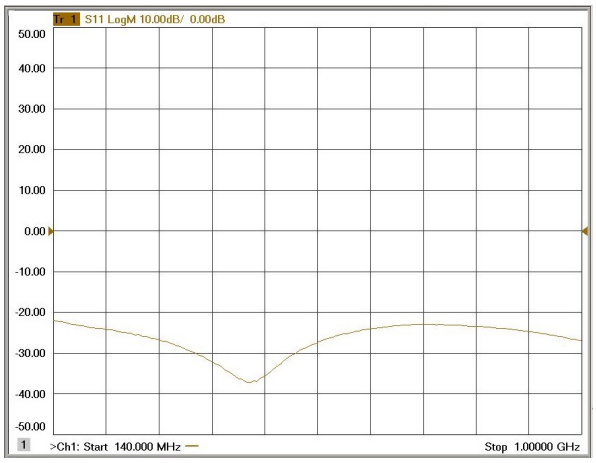

Figure 6.22: Return Loss of the RF_{out} port of AD8345

Mixed Domain Devices

DAC5562 EVM

Return Loss of the Clock port

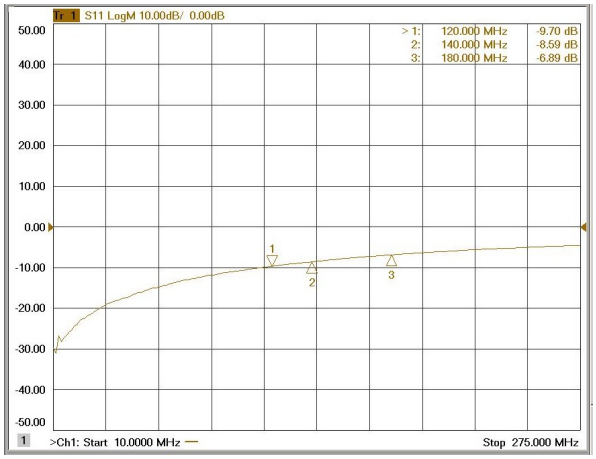

Figure 6.23: Return Loss of the Clock port of DAC5562

Return Loss of the Output ports

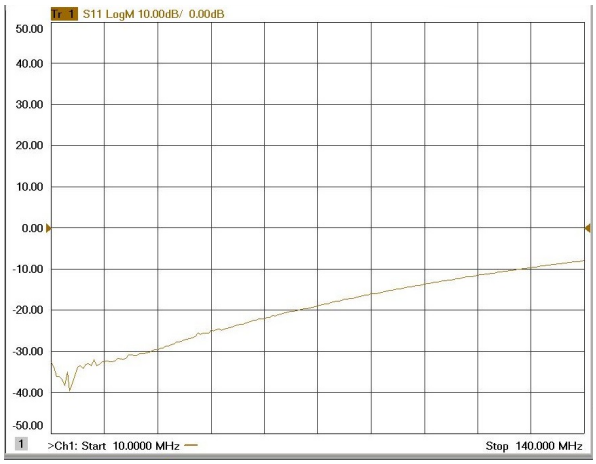

Figure 6.24: Return Loss of the Output ports of DAC5562

Matlab Code

The Matlab code presented below is referred to the communication established between Matlab and Logic Analyzer via Local Area Network (LAN) connection. This connection makes possible the programming of the vectors, in this example, they are programmed with a cosine wave and a sine wave, in bus number 1 and bus number 2, respectively.

```
close all; clear all; clc;

LA.ProgID = 'AgtLA.Connect';        % Assign Programmatic ID to a string
LA.IP = '192.168.70.24';            % IP of the remote logic analyzer

LA.LocalPath = 'D:\UsersFolder\FMartins';
%Local directory that gets the saved file
LA.RemotePath = 'C:\Documents and Settings\Administrator\MyDocuments
\AgilentTechnologies\LogicAnalyzer\Config Files\';
% Only needed with transfer option

%%%%%%%%%%%%%%%%%%%%Create a COM Object - Connect%%%%%%%%%%%%%%%%%%%%%%
try
    LA.hConnect = actxserver(LA.ProgID);
catch ME    % If there's an error creating the COM automation server...
    display ('Controlled abort while creating local COM object.');
    display (ME.message);
    error ('Controlled abort.');
end

try
    LA.hInst = get (LA.hConnect, 'Instrument', LA.IP);
catch ME    % If there's an error getting the Instrument interface...
    display ('Controlled abort while creating remote COM object.');
    display (ME.message);
    error ('Controlled abort.');
end
display ('All connections done');

%%%%%%%%%%%%%SET LA%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

LA.hInst.Stop   % In case analyzer modules are running, stop them.

%% Set the installed LA Modules

LA.hModules = LA.hInst.get('Modules');  % Get the Modules property

for i = 0:(LA.hModules.Count - 1)       % For each Module in the collection
    LA.hModule = LA.hModules.get('Item', int32(i));    % Get the module
```

```
    % The Item property requires an integer parameter.

    %If a pattern generator is detected... Get the pattgen object
    if (strcmp(LA.hModule.Type, 'Pattgen'))
        LA.hPattGen = LA.hModules.get ('Item', LA.hModule.Slot);
        %LA.hPattGen = LA.hModules.get ('Item', strPG);

    %If a 16911A analyzer module is detected, Choose the *last* 16911A module
    elseif (strcmp(LA.hModule.Model, '16911A'))
        LA.h16911A = get(LA.hModules, 'Item', LA.hModule.Slot);
    end
end

%%%%%%%%%%%%%%%%%%%%%%%%Vectors of PG%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

display ('Programming the PG...')

fs = 120e6;     %sampling frequency
df = 1e6;       %tones distance
ts = 1/fs;
fcarrier = 5e6; %first tone
Nt = 1;         %number of tones
t = ts:ts:(100/df);
partition = -1:2/4095:1;    %12 bit scale

x1 = 0;
for aa=1:Nt
    x1 = x1 + 1*exp(j*(2*pi*(fcarrier+(aa-1)*df)*t));
end

% I
Xin = real(x1)/max(real(x1));
Xquant = quantiz(Xin,partition);
k1 = 0.95*Xquant;

% Q
Xin2 = imag(x1)/max(imag(x1));
Xquant2 = quantiz(Xin2,partition);
k2 = 0.95*Xquant2;

for i = 1:length(t)
    vector = ['Vector "My Bus 1"=d' int2str(k1(i))];
    LA.hPattGen.InsertLine((i+3), vector);
end

for i = 1:length(t)
    vector = ['Vector "My Bus 2"=d' int2str(k2(i))];
```

```
    LA.hPattGen.InsertLine((i+3), vector);
end

display ('Press any key to run the PG in repetitive mode...')
pause
display ('Starting the PG in repetitive mode...')
LA.hPattGen.Run(int32(1));
disp('Done')
```

C Code

The C code used in this work was developed to program the two RF synthesizers used in this project, LMX2541 and SLSM4. The code was edited on vim, compiled on pcompile and transferred to DETPIC32 by using ldpic [27].

LMX2541SQ2060E - C Code

Example:

```
#include "pll.h"

void spi_init(void);
void pll_writeData(int);

int main(void)
{
spi_setClock(500000); //SPI CLOCK 500kHz
TRISE=0; //define E ports as output
int i=0;

spi_init(); //SPI ON
PORTE=0x05;  //LE OFF, CE ON
SPI2CONbits.ON = 1; //SPI OFF

//Write the registers
pll_writeData(0x00000017);
pll_writeData(0x000000CD);
pll_writeData(0x0000001C);
pll_writeData(0x28001409);
pll_writeData(0x0111CE58);
pll_writeData(0x001FFFE6);
pll_writeData(0xBF480025);
pll_writeData(0x11008324);
pll_writeData(0x01B91F03);
pll_writeData(0x04000642);
pll_writeData(0x00000021);
pll_writeData(0x00000500);

SPI2CONbits.ON = 0; //SPI OFF o saida
for(i=1; i<8; i++); //delay
TRISG=0; //define G ports as output
PORTG=0x00;  //CE and LE ON

while(1){}

return 0;
}
```

pll.c

```
#include "pll.h"
int i=0;

void spi_setClock(unsigned int clock_freq)
{
SPI2BRG = (F_CLK / (2 * clock_freq)) - 1;
}

void spi_init(void)
{
volatile char trash;
SPI2CONbits.ON = 0;
SPI2CONbits.FRMEN = 1; //FRAME MODE disabled
SPI2CONbits.CKP = 0; //idle as 0
SPI2CONbits.CKE = 0; //active transition from idle to active
SPI2CONbits.SMP = 0; //sample phase middle
SPI2CONbits.DISSDO = 0; //SDO ON
SPI2CONbits.MODE16 = 1; //data width = 16 bit
SPI2CONbits.ENHBUF = 1; //enhaced mode on
SPI2CONbits.MSSEN = 0; //disable slave select support
SPI2CONbits.MSTEN = 1; //enable master mode
SPI2BUF = 0x00; //cleans reception FIFO

while( !SPI2STATbits.SPIRBE ) //emptying FIFO
trash = SPI2BUF;

SPI2STATbits.SPIROV = 0;
}

void pll_writeData(int value)
{
SPI2BUF = value;
PORTE=0x02;   //activa /CS
while( SPI2STATbits.SPIBUSY ){}
PORTE=0x03;  //LE ON
}
```

SLSM4 - C Code

```
#include "pll.h"

void spi_init(void);
void pll_writeData(int);

int main(void)
```

```
{
TRISE=0; //define portos E como saida
PORTE=0x03;  // /CS=1, BAND 1
int i=0;
spi_setClock(900000); //SPI CLOCK 900kHz

spi_init();
SPI2CONbits.ON = 1; //SPI ON
for(i=1; i<850; i++); //delay
PORTE=0x03;  // /CS OFF

pll_writeData(0x0025); //Main divider register

for(i=1; i<850; i++); //delay

pll_writeData(0xAAAA); //Main dividend LSB register

for(i=1; i<850; i++); //delay

pll_writeData(0xAAAA); //Main dividend MSB register

PORTE=0x03;  // /CS OFF

SPI2CONbits.ON = 0; //SPI OFF
TRISG=0; //define portos G como saida
PORTG=0x00;  //DATA,SCLK OFF

while(1){}

return 0;
}
```

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