HIGH-POWER BI-DIRECTIONAL DC/DC CONVERTERS

WITH CONTROLLED DEVICE STRESSES

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SUMMARY

As research on renewable energy and the electrification of transportation accelerates, high-power bi-directional dc/dc converters are increasingly required in energy storage and PHEV/EV applications. In scaling the power levels of converters, mitigating a converter system's parasitic components is important to realize high efficiency and high-power density. Hence, this dissertation proposes developing a converter to use the converter system's parasitic components effectively.

The objective of the research is to develop a cost-effective high-power bi-directional dc/dc converter with low total-device ratings, reduced system parasitic effects, and a wide input/output range. Additional objectives of the research are to develop a small-signal model and control methods, and to present performance characterizations.

Device stresses in the proposed topology are controlled to maintain minimal levels by varying the duty ratio and phase-shift angle between the primary and the secondary bridges, which results in a low total-device rating, when compared to conventional bi-directional dc/dc topologies.

In the proposed topology, soft switching, which reduces power loss, can be realized under specific operating conditions. When the condition that causes minimal device stress is satisfied, zero-voltage switching (ZVS) can be obtained. In the research, ZVS capability is explored for a wide range of voltage conditions as well as for the minimal device-stress condition. The performance characterization includes verifying the soft-switching regions and power-loss estimation.

Another part of the thesis is the controller design of the converter. Small-signal models and feedback controllers are developed, and the controllers are experimentally validated.

Because in the isolated high-frequency converters, transformer saturation is an important issue, a method to prevent transformer saturation is proposed and experimentally validated.

CHAPTER 1

INTRODUCTION

Global-climate change and the depletion of fossil-fuel reserves are driving society's quest for a sustainable-energy infrastructure. Currently, societal interest seems to point in two directions. The first is to use existing energy infrastructure intelligently and efficiently. The second is to develop renewable-energy sources and integrate them into the existing energy infrastructure.

The past decade has seen a tremendous increase in renewable energy and the transit-electrification research. In both of these fields, power electronics is a key technology in linking energy sources to various loads and power systems. For example, many renewable energy and plug-in-hybrid/electric vehicles (PHEV/EV) require energy-storage systems in which dc/dc converters with bi-directional power-flow capability are essential components.

As there was little need for bi-directional high-power conversions in the past, most of the existing dc/dc converters are targeted at uni-directional and low (or medium) power applications. The growth of PHEV/EVs, renewable energy, and energy-storage applications is expected to accelerate the need for high power bi-directional dc/dc converters.

Currently envisioned for high-power bi-directional dc/dc converters are the following applications:

- Utility-scale energy storage
- DC grid with various energy sources
- Electric or plug-in-hybrid electric vehicle (EV/PHEV)

- Back-to-back ac/dc/dc/ac systems

Figure 1.1 shows a possible architecture of a PHEV-drive train. The arrows in Figure 1.1show the directions of the power flow. The energy-storage battery is charged and discharged depending on the drive train's power demand. In this architecture, the bi-directional dc/dc converter controls the direction and the magnitude of the power flow.

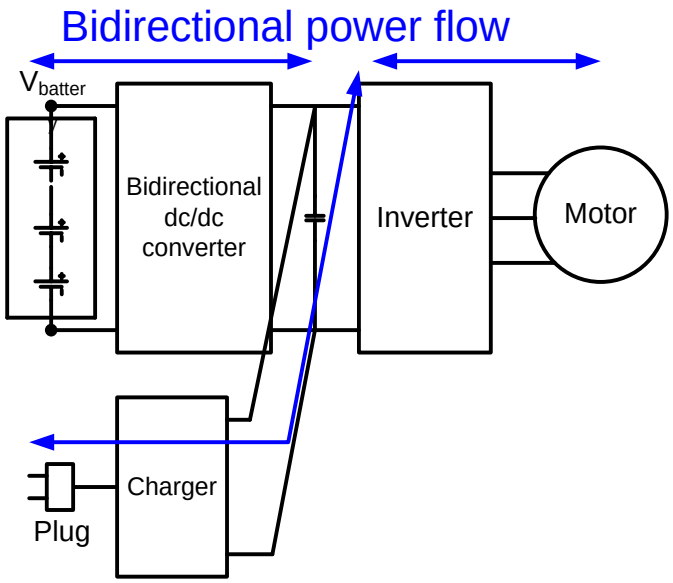


Figure 1.1. A dc/dc converter applied in a PHEV.

The bi-directional dc/dc converter controls the power to charge and discharge the battery. The output voltage of the battery charger can be converted to the $V_{battery}$ by the bi-directional dc/dc converter during the charging mode. When the battery is loaded, the bi-directional converter can supply power to the motor through the inverter, as shown in Figure 1.1.

Another possible application of a high-power bi-directional dc/dc converter is for the energy-storage system [1, 2] in a utility level, as shown in Figure 1.2. In the energy-

storage system in a utility scale, high-power density is a benefit derived from the usage of the isolated bi-directional dc/dc converter. Because the isolated bi-directional dc/dc converter is operated at a high-switching frequency, the volume of the isolation transformer can be reduced in comparison with that of a transformer designed for 60 Hz excitation.

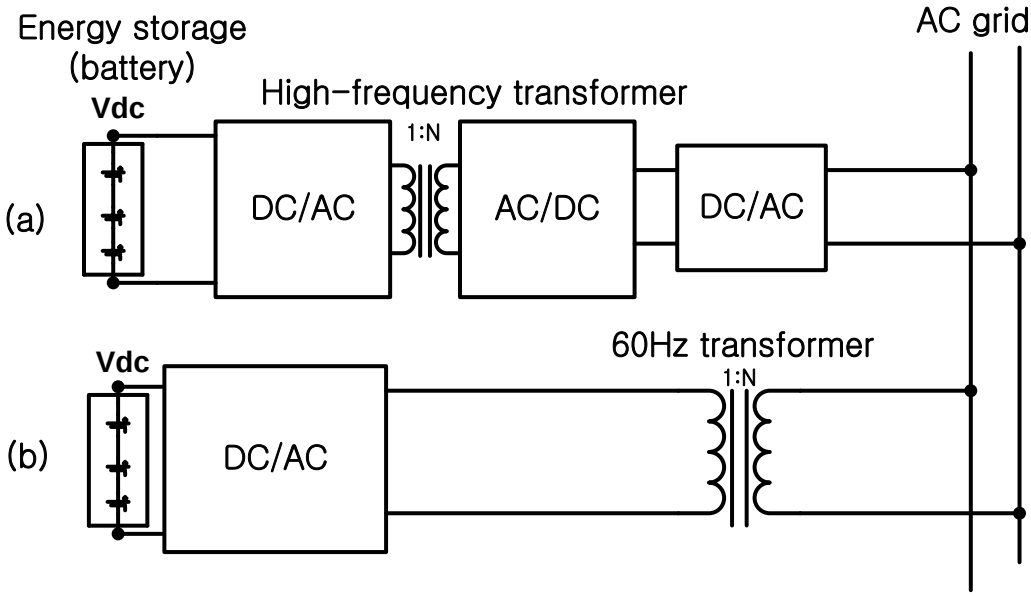


Figure 1.2. Energy-storage systems in a utility scale.
(a)With a bi-directional dc/dc converter,
(b) Without a bi-directional dc/dc converter.

Figure 1.2(b) shows an energy-storage system using a dc/ac inverter and an isolation transformer. In this architecture, the design of the isolation transformer is based on the line frequency of 60 Hz, which requires a large volume of the magnetic core.

Another application of a bi-directional dc/dc converter is for the dc grid with various energy sources. When multiple dc sources are connected to a bus, the bus voltage can experience large variations from variations in load power. A battery and a fuel cell are examples in which the bus voltage varies within a wide range.

Another possible application of bi-directional dc/dc converters is back-to-back ac/dc/dc/ac conversion using a bi-directional dc/dc converter and inverter/rectifier. An electronic transformer [2] was proposed using the back-to-back system.

The design of high-power dc/dc converters has several requirements, including high-power density, high efficiency, and low total-device rating, which is related to the manufacturing cost. The ratings of the switching devices and the capacitors make up a large portion of the manufacturing cost of the power converters. For this reason, the rating of the switching device should be considered in the design and selection of the power-converter topology.

As a general requirement for high-power dc/dc converters, the performance of the converter must meet the various conditions of the targeted applications. If the converter is to be used in energy-storage applications, the converter is expected to operate under wide variations in input and output conditions. The terminal voltage of the energy storage has large variations that depend on the load conditions. Another important issue in a high-power converter is how to deal with converter's parasitics. The converter's parasitic elements significantly influence the performance of high-power converters. The parasitic inductances generally cause many problems, limiting the power levels and efficiency.

The primary contribution of this thesis is that it develops a high-power bi-directional dc/dc converter (Dual-Active Bridge Buck-Boost (DAB^3) converter) with controlled device stresses for a wide input/output range.

The second contribution of the thesis is its characterization of the proposed converter. The thesis analyzes soft-switching capability, and develops parametric loss

estimation for the converter. Through these characterizations, the benefits that can be obtained in the DAB^3 concept are justified.

The third contribution of the thesis is a small-signal model of the topology. The DAB^3 converter can be controlled by two separate variables such as the duty ratio and the phase-shift angle. The transfer functions from the small-signal models are derived and analyzed in stability.

The fourth contribution in the thesis is development of the control method. The basic function of the controller for the proposed converter is to regulate the voltage outputs. With the basic controller, a method which prevents dc currents in the transformer is developed because the dc saturation of the isolation transformer is often observed in the dual-active switching mode. Finally, experiments are conducted to validate the proposed converter with feedback controllers which regulate the output voltages. Experiments are also performed to validate the method to prevent dc current in the transformer. The implementation of the digital-control algorithm is based on an FPGA (Field-Programmable-Gate Array), which is used to realize the low propagation delays in the control loop.

CHAPTER 2

BI-DIRECTIONAL HIGH-POWER DC/DC CONVERTERS

2.1. Introduction

In the design of high-power bi-directional dc/dc converters, the main trade-offs are between the power density and the power efficiency. Since the 1970s, the power density of the power-electronic converters has rapidly increased, owing to the advancement of the power-semiconductor technology. With the more advanced power semiconductors, a high(er)-switching frequency has been realized for switch-mode power-electronic converters. Hence, the volumes of the magnetic devices can be decreased.

In general, switch-mode dc/dc converters are composed of switching devices, magnetic components (inductors and transformers), capacitors, and heat-dissipation components, etc. Increasing the switching frequency can reduce the geometric dimensions of a magnetic component, such as an inductor and a transformer. However, operation of the power converter in a higher-switching frequency causes a higher-switching loss (lower power efficiency) in hard-switching conditions and may increase the volumes of heat-dissipation components.

Since a bi-directional dc/dc converter is a combination of two uni-directional dc/dc topologies, a discussion of the origin of problems can start with the uni-directional high-power dc/dc topologies. In the late 1970s, a high-power resonant-dc/dc converter was introduced for a traction motor by [3], as shown in Figure 2.1. In general, resonant-dc/dc converters have a very low-switching loss at a high-switching frequency since they

use zero-voltage (ZVS) and zero-current switching (ZCS) techniques. As a result, the volume of heat sinks and magnetic cores can be reduced in resonant dc/dc topologies, thereby reducing the manufacturing cost and increasing the power density. Furthermore, the transformer's leakage inductance ($L_{leakage}$) was effectively utilized in series-resonant converters (SRC).

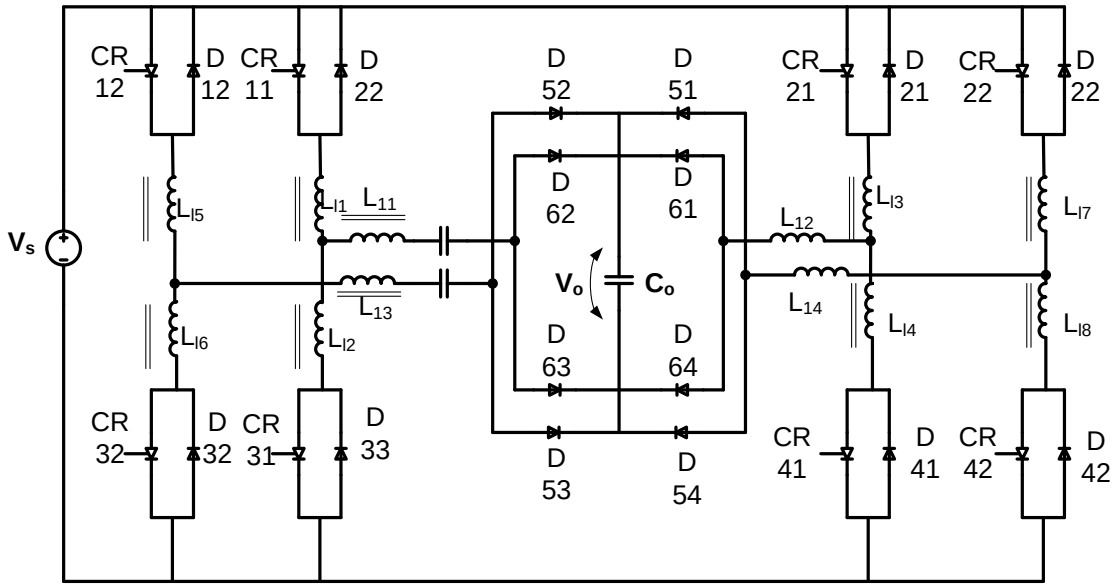


Figure 2.1. A simplified twin-bridge series-resonant converter presented in [3].

The main disadvantage of a series-resonant converter (SRC) is that the resonance between an inductor (L_r) and a capacitor (C_r) can cause very high-peak currents, resulting in high total-device ratings (TDR). The definition of a total-device rating (TDR) given by Equation (1) is the sum of the ratings of each device. In Equation (1), V_i^{peak}, I_i^{peak} and P_o denotes the peak voltage, the peak current of each device and the output power, respectively.

$$S_{total}\,(\text{TDR}) = \frac{\sum_{i=1}^{n}\left(V_i^{peak} \times I_i^{peak}\right)}{P_o}\ (\text{P.U.}) \quad \text{where, } P_o = \text{output power (W)} \qquad (1)$$

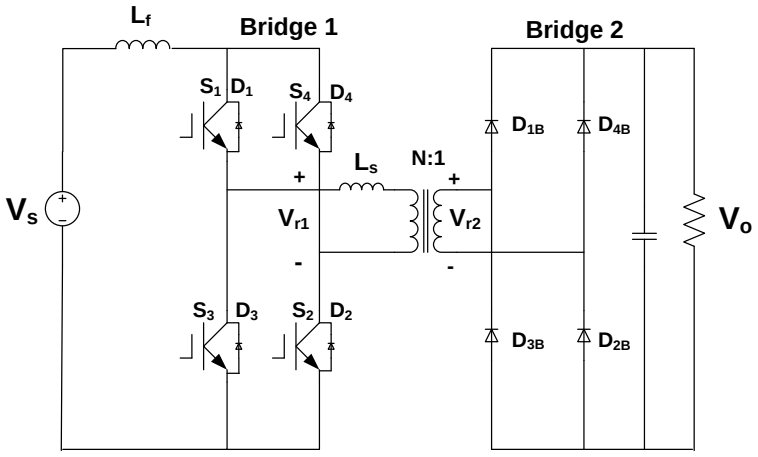
In general, the output power of an SRC topology can be controlled by varying the switching frequency or the duty ratio. For wide input/output ranges, the converter should be operated in a wide range of switching frequencies, which requires a complicated optimization in the circuit design.

2.2. Literature Survey

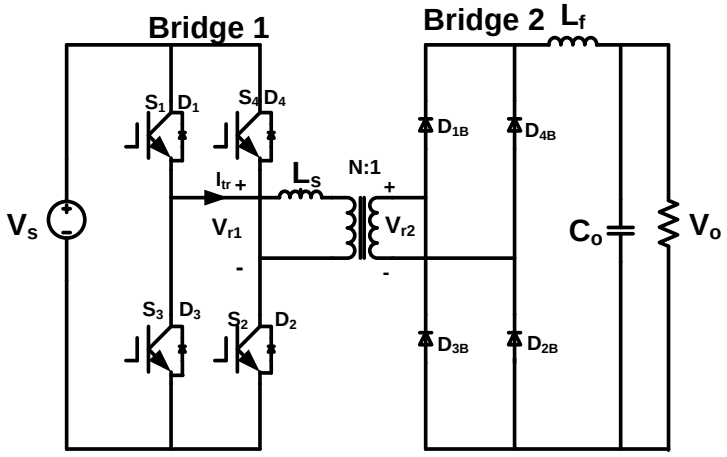
In the resonant-converter topology in Section 2.1, high-power density is achieved by increasing the switching frequency. Despite the benefits of high-power density, the major limitation of this topology is the high total-device ratings as resonant currents flow in the devices, and these resonant currents are responsible for the high conduction losses. Against the limitations of resonant topologies, the next generation of power converters was introduced [4-6]. These had low total-device ratings (TDR). After the resonant-dc/dc topology for high-power applications, full-bridge converters and a Dual-Active Bridge converter (DAB converter) were developed.

2.2.1. Full-bridge converters

Full-bridge topologies are introduced for uni-directional applications, and are widely used due to their reliability, simple structures and high efficiency. Many variations [4-9] of the full-bridge topologies have been introduced. Generally, full-bridge topologies are divided into two types – the voltage-fed and current-fed, as shown in Figure 2.2. The current-fed topology is composed of an H-bridge, a filter inductor and auxiliary circuits such as active/passive-clamp circuits to deal with high-voltage stresses on the source side. A diode bridge and a filter capacitor are located on the load side, and an isolation transformer is located between the H-bridge and the diode bridge.



(a) Current-fed type.



(b) Voltage-fed type.

Figure 2.2. Schematic of full-bridge converters.

Ideally, a full-bridge dc/dc topology should present low total-device ratings (TDRs) because a square-wave voltage drives an ideal transformer to power the load. However, the leakage inductance of the transformer increases device ratings. The leakage inductance of the isolation transformer causes high-voltage stresses across the switching devices because of the mismatch between the energy in the leakage inductance of the transformer and the filter inductor. For this reason, the current-fed full bridge converter requires auxiliary circuits such as active-or passive-clamp circuits to mitigate the voltage

stress. Furthermore, the active-clamp circuit also causes high-current peaks, a problem discussed in Section 2.2.2. A further impact of the leakage inductance is that it decreases the power throughput from the source to the load. Hence, more winding turns are required to transfer the rated load power. Hence, the current level on the source side increases, and the conduction loss on the source side increases as well.

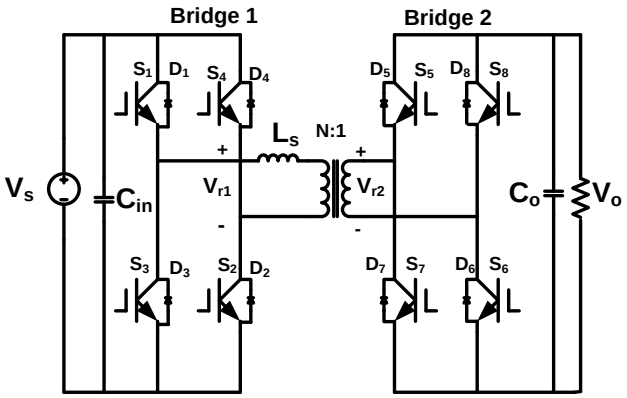
Reverse-recovery currents, parasitic capacitances of diodes and parasitic inductances in the power stage cause EMI problems. Hence, clamping circuits are required to reduce the EMI effects.

2.2.2. Converters using dual H-bridges

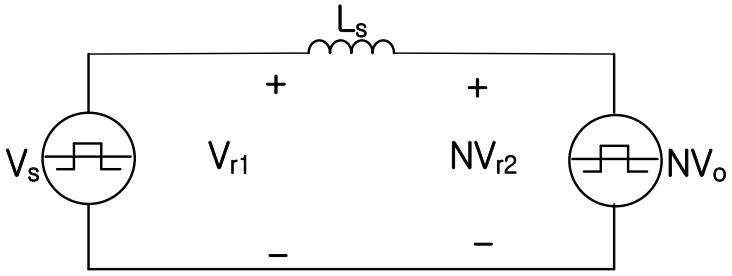
Since the introduction of the Dual-Active Bridge (DAB) converter [4, 10], many authors have proposed the DAB topology for many high-power applications [1, 2, 11-14] such as automotive and energy-storage systems.

In the DAB converter, the leakage inductance (L_s), which is shown in Figure 2.3 (a), is used as a main power-transfer element. Figure 2.3 (b) represents the simplified equivalent circuit of the DAB converter, which is described by the leakage inductance and two ac-voltage sources. The phase-shift between the two ac-voltage sources drives the current and power to the load. The ac-voltage sources can be generated by the modulation of the gating signals of two H-bridges. DAB offers a "minimal" topology, using two semiconductor bridges, two dc-side capacitors and an isolation transformer, as shown in Figure 2.3. Major parasitic elements of the system such as the leakage inductances of the isolation transformer, and the parasitic capacitances of the switching devices, are purposely used in the power transfer and in the switching transitions,

respectively. The parasitic elements (L_s and C_{pi}, i=1,2,…,8) make quasi-resonant transitions during the switch-turn-on and-off, which mitigates voltage spikes across the switching devices.



(a) Schematic.



(b) Equivalent circuit.

Figure 2.3. Dual-Active Bridge (DAB) converter.

System control is affected by switching both bridges in a square-wave mode, thereby realizing the power-flow control by varying the phase angle between the two square waves, as shown in Figure 2.4. The power equation is given by

$$P_o = \frac{NV_1V_2}{\pi\omega L_s}(-\emptyset^2 + \pi\emptyset) \quad \text{where, } \omega = 2\pi f_s. \tag{2}$$

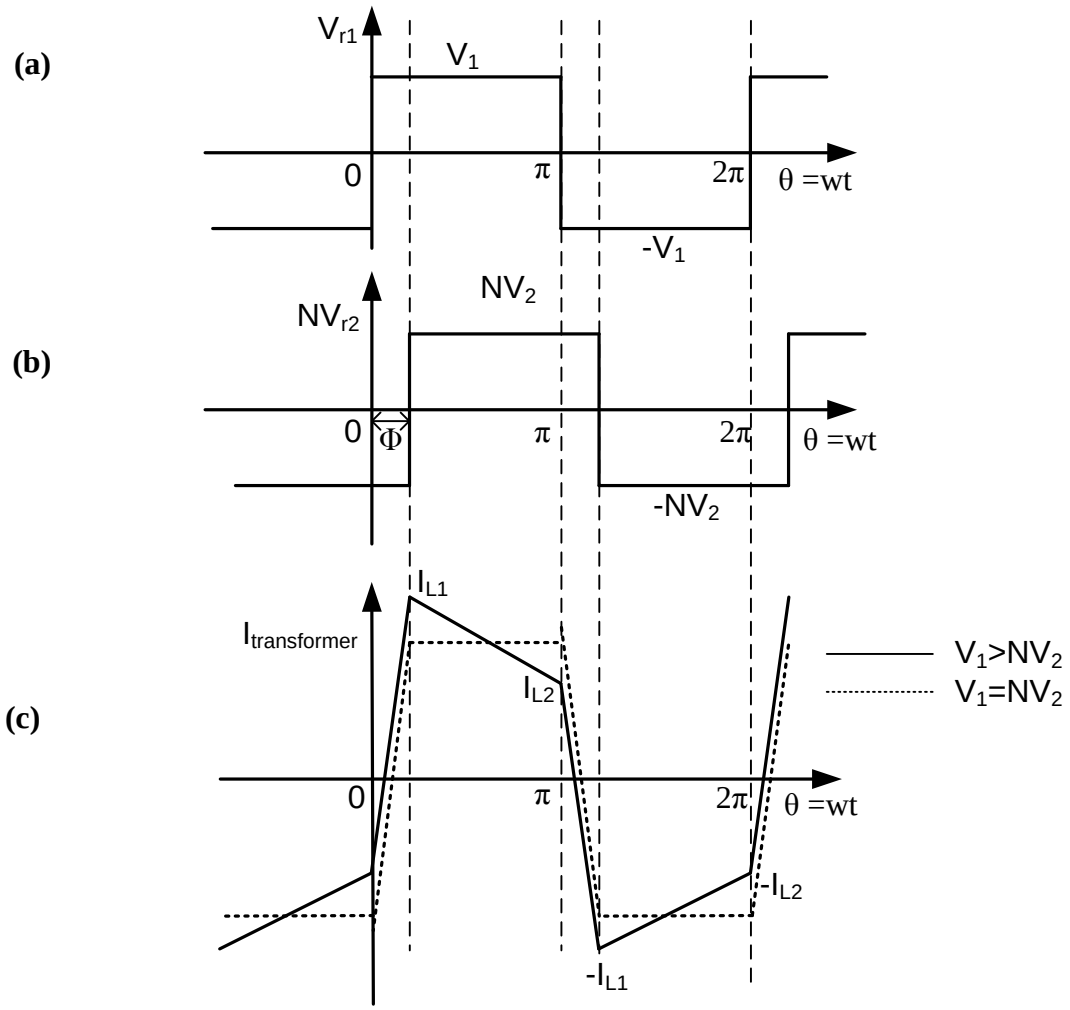


Figure 2.4. Important waveforms of DAB converter.
(a) Voltage waveforms V_{r1}, (b) Voltage waveforms NV_{r2},
(c) Transformer current.

In Equation (2), the output power is a function of the phase-shift angle (∅) , the source voltage (V_1=V_s), the output voltage (V_2) and the turn-ratio (N), the switching frequency (f_s), and the leakage inductance (L_s).

Under ideal operating conditions (i.e., when the input and reflected-output voltages are equal), the current stresses in the devices are minimized, as the transformer current has a flat top. In the ideal case, assuming sufficiently small-leakage inductance,

the minimum total-device rating (TDR) would be $8xP_o$ (P_o is the output power), as would be the case for an ideal voltage-source full-bridge dc/dc converter. Under more realistic conditions (i.e. when the input or output voltage varies over a wider range), the current stresses, and hence, the device ratings for the DAB converter, become very high. High-current stresses both increase the device losses dramatically and reduce the efficiency of the converter in such applications. As most applications will have some level of dc-bus variation, this has been a significant limitation of the DAB topology. Figure 2.4 shows the transformer voltage and current waveforms in Bridge 1 and Bridge 2. When V_1 does not equal NV_2, the slope of the transformer current becomes high as shown in Figure 2.4(c). The slope of the current on the primary side during $\emptyset < \theta < \pi - \emptyset$ depends on $\frac{di}{dt} = \frac{(V_1 - N \times V_2)}{L_s}$. As the difference, V_1-NV_2 becomes larger, the slope, $\frac{di}{dt}$ becomes higher for a constant value of L_s.

Modulation of switching signals has been proposed in [11, 15] to limit the level of peak currents in the DAB topology. The current and voltage waveforms of the isolation transformer are illustrated in Figure 2.5 under the conditions, $V_1 > NV_2$ and $V_1 < NV_2$, respectively. In the modulation schemes, the switching modulation generates positive and negative slopes either in trapezoidal or triangular waveforms. The objective of the modulation schemes is to limit the peak value of the transformer current when V_1 does not equal NV_2. Despite these schemes, the slope of the current depends on the voltage difference, V_1-NV_2, resulting in high-peak currents when applied to wide input/output voltage applications. As shown in Figure 2.5 (a) and (b), transformer currents reset to zero when zero voltage interval is applied to V_{r2}', which enables switching at the zero current levels in Bridge 2. However, a triangular modulation is available only when

V_1>>NV_2 is satisfied. Furthermore, these schemes require the computation of duty cycles, based on the output power, so that the computation complexity increases when compared with the conventional DAB and full- bridge converters.

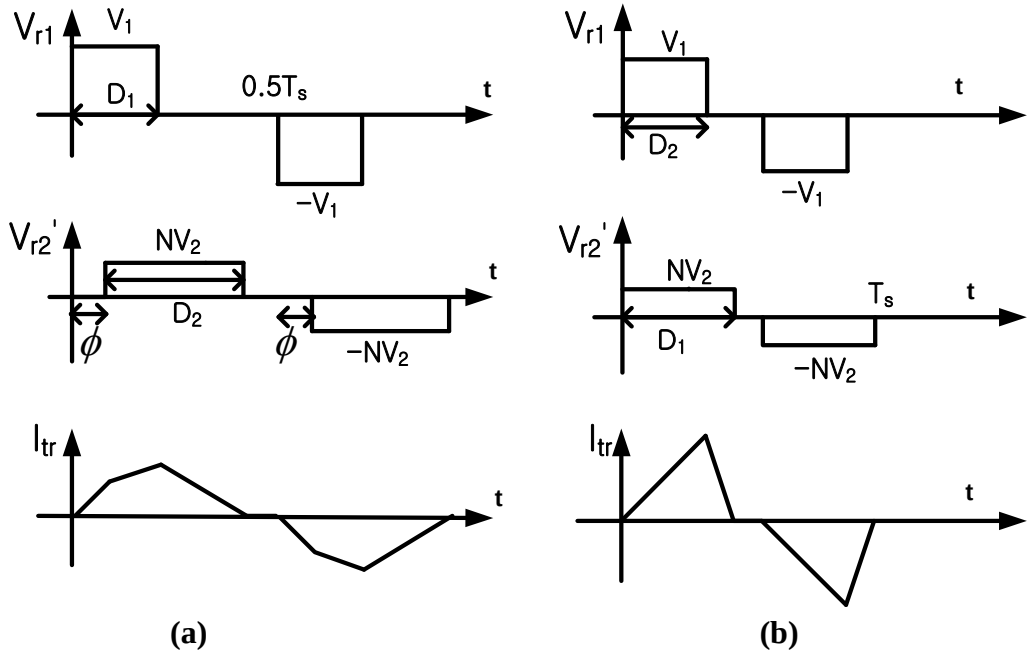


Figure 2.5. Key waveforms of modulation schemes (V_2'=NV_2)
(a) Trapezoidal method, (b) Triangular method

The ZVS range is extended in [16] for a wider range of input/output voltages in comparison with that of the original DAB converter. When V_1 is significantly larger than NV_2, the large $\frac{di}{dt}$ of the transformer current can cause I_{L1} or I_{L2} in Figure 2.4 to become negative in the original-DAB converter. In this condition, ZVS is not available and results in high-switching loss. Modulating the switching signals can extend the ZVS region, as shown in Figure 2.6. However, when this topology is applied to a wide-input/output range, the slope of the current can be high.

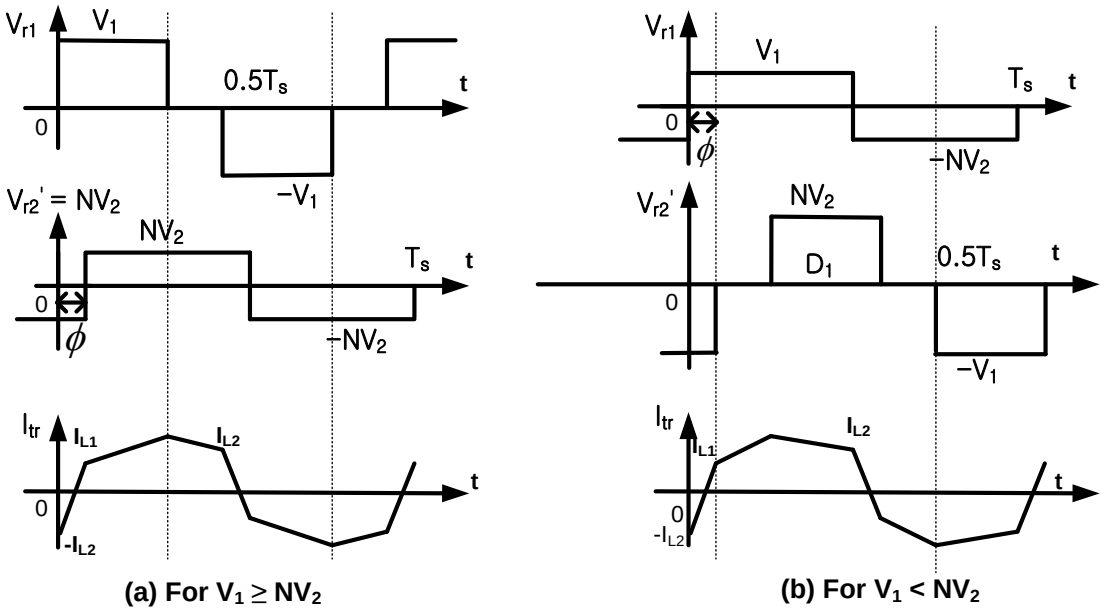
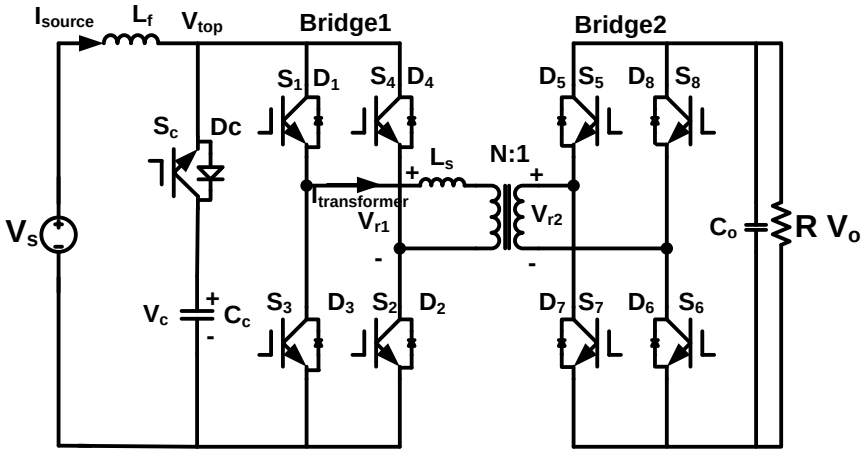
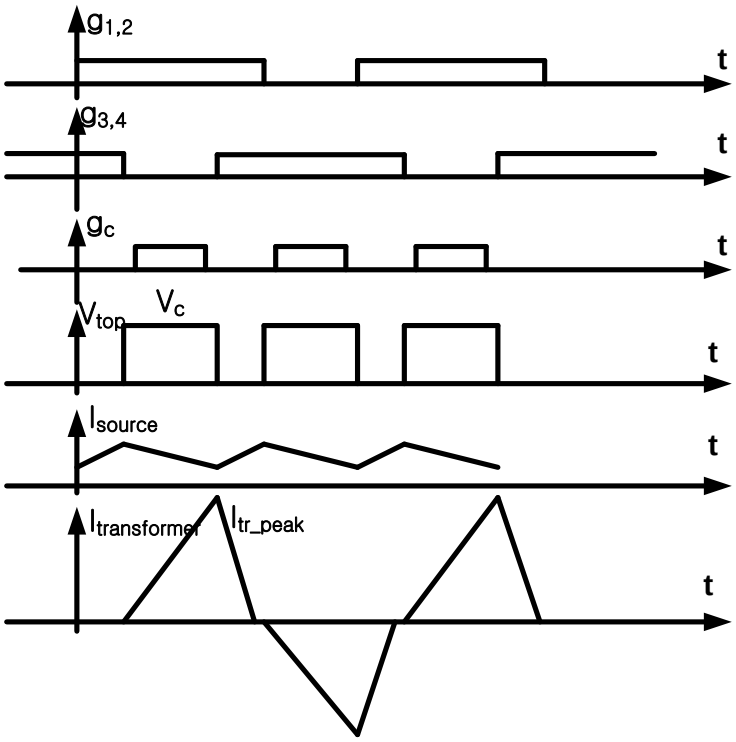


Figure 2.6. Extending ZVS region by switching-modulation schemes.

As a bi-directional power-flow is required in many applications, the uni-directional full-bridge topologies have been modified as shown in Figure 2.7. The topology has been introduced for an energy-storage application for fuel-cell systems [8, 17]. The uni-directional full-bridges, shown in Figure 2.2, are modified to achieve a bi-directional power flow. When the power flows from V_s to R, it is denoted as being in "boost mode". When the power flows in the opposite direction, it is denoted as being in "buck mode".



(a) Bi-directional full-bridge converter for the boost operation.



(b) Gating signals (g_1-g_4,g_c), top-node voltage in Bridge 1, filter-inductor(L_f) current and transformer-current waveform.

Figure 2.7. Bi-directional full-bridge converter.

In the boost mode, only the active switches in Bridge 1 are gated, while only anti-parallel diodes are used to rectify ac waveforms in Bridge 2. The operation of the converter is same as the actively-clamped current-fed full-bridge converter. The topology

looks similar to the proposed topology in the thesis. The main difference is that this topology in Figure 2.7 has single ended excitations. Switch S_c and a capacitor C_c composes an active clamper to mitigate the high-voltage spikes across the switching devices.

Figure 2.7 also shows important waveforms of the boost operation. The transformer current essentially has high peaks and resets to zero. The slope of the transformer current depends on the leakage inductance of the transformer, duty ratio, "D", and the voltage difference between the clamp-capacitor voltage, V_c and the output voltage, V_o'(=N×V_o). The peak current value, I_{tr_peak} can be represented by Equation (3).

$$I_{tr\_peak} = \frac{(V_c - NV_o)}{L_s} (D \times T_s) \quad (3)$$

Ideally, V_c and NV_o should be the same; however, when a diode bridge is used, the leakage inductance decreases the power throughput, which makes the voltage across the leakage inductance (=V_c-NV_o) a non-zero value. The peak current can become high, depending on L_s and the voltage difference, V_c -NV_o. This high peak current increases total-device rating (TDR).

In the past [18, 19], some variants have been introduced, using dual H-bridges and a duty-cycle control. In such topologies, some variants of clamp circuits (RCD or resonant) are used to increase efficiency; however, a larger number of devices are needed, which introduced higher costs and volumes. When high power and current applications are considered for wide input/output ranges, the topology in [18] has high conduction losses which are caused by high-circulation currents in the transformer. The

circulating current decreases the efficiency of the converter, which is the main disadvantage of this topology.

2.2.3. Dual-Active Half Bridge converters

A half-bridge topology is widely used for its low total-device ratings and reliability. However, the original half-bridge topology has limitations in the magnitude of the device currents when the source voltage varies widely.

Some authors have modified a half-bridge topology to obtain a bi-directional capability and to reduce current stresses over wide-input/output conditions. Among the modified topologies, the modified Dual-Active-Half Bridge (M-DAB) topology in Figure 2.8 seems to be a possible topology for high-power applications, since it effectively uses the parasitic components and has low a total-device rating for a wide source-voltage range.

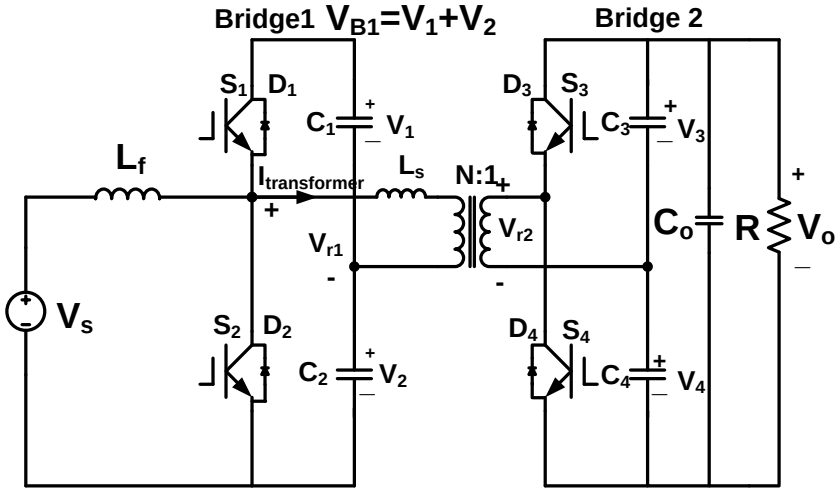


Figure 2.8. Schematic of the M-DAB topology.

The device ratings of this topology, which are estimated for the 50% duty ratio, are reported to be quite low from the literature in [20]. However, the authors did not

discuss the availability for high-power applications with wide input/output ranges. In [21], the topology was experimentally proven to have low device ratings for wide operating ranges.

In Figure 2.8, V_s represents a voltage source that has wide variations. V_o represents the dc-bus voltage, which is maintained at a relatively constant value. Voltage levels across the capacitors (C_1-C_4) are defined as V_1-V_4, respectively. During the time interval, $D \times T_s$, in Figure 2.9, the gating signal of the switch, S_2, is in the "on" state. The relationship between the source voltage V_s and V_{B1} ($=V_1+V_2$) is given by (4).

$$\frac{V_s}{(1-D)} = V_{B1} = V_1 + V_2 \tag{4}$$

During the operation of the converter, the duty ratio, D, controls the source-to-V_{B1} ratio, while the phase-shift angle (∅) between Bridge 1 and Bridge 2 controls the power to the output load. Figure 2.9 shows ideal waveforms of the M-DAB converter. It is seen that when the conditions $V_1=NV_3$ and $V_2=NV_4$ are satisfied, the current waveform is "flat-topped," resulting in minimal-current stresses. Tracking this condition by using a control strategy is the main objective, which presents low total-device ratings. Equations (5)-(7) show the transformer current peaks in the steady state and the power equation when the "flat top" condition is maintained. The power equation indicates that the output power can be regulated by controlling the phase-shift angle,∅, and the duty cycle, D, which, is controlled like a boost converter to maintain the voltage, V_{B1}, at the desired value.

$$I_0 = I_1 = \frac{D}{1-D}\frac{V_s \emptyset}{\omega L_s} \quad (5)$$

$$I_2 = I_3 = -\frac{V_s \emptyset}{\omega L_s} \quad (6)$$

$$P_{out} = \frac{1}{2\pi}\int_0^{2\pi} v_{ab}(\theta) \times i(\theta) = \frac{v_s^2 \times \emptyset}{4\pi \times 2\pi f_s \times L_s \times (1-D)} \times (4\pi D - \frac{\emptyset}{1-D}) \quad (7)$$

Where,

L_s = series ac inductance including the leakage inductance (H)

$\omega = 2\pi f_s$ (rad/sec)

f_s = switching frequency (H_z)

V_s = source voltage (V).

The phase-shift angle is controlled to transfer the required output power. In other words, the output voltage is controlled with the phase-shift angle. As the voltage (V_s) changes over the desired range (ex. 2:1), the duty cycle is varied to maintain a constant voltage, $V_{B1} = NV_o$. Again, the phase-shift angle is varied to maintain the output voltage. The advantage of this topology is the low total-device rating (TDR) when compared to the TDR of the DAB topology. The main disadvantage of this topology is the very high current ratings (A_{RMS}) of dc-energy-storage capacitors. This characteristic is inherent in a half-bridge topology.

Figure 2.10 (a) shows the current waveforms of the switching devices and the capacitors of Bridge 1. Figure 2.10 (b) illustrates the device currents (I_{s3}, I_{s4}, I_{c3}, I_{c4}) of

Bridge 2 indicating that the RMS values of the capacitor currents seem to be high. Using the waveforms in Figure 2.10 and Equation (7), the current-ripple ratings of the capacitors can be derived analytically, and the results are listed in Appendix A.

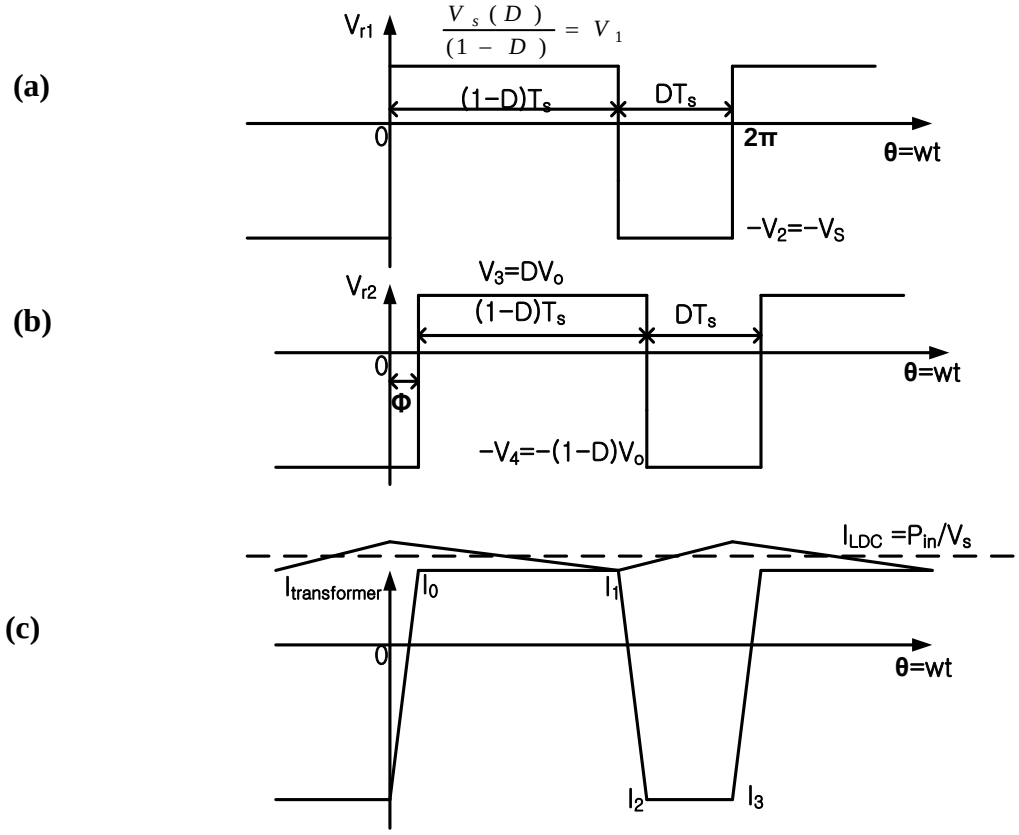


Figure 2.9. Important waveforms of the M-DAB converter.
(a) Voltage in the primary side (V_{r1}),
(b) Voltage in the secondary side, (V_{r2}),
(c) Transformer current.

The main advantage of the M-DAB converter is that it provides flat-top transformer currents for wide input/output ranges. When the TDR of M-DAB is compared with that of DAB, the difference is significant. A comparison of the TDRs is presented in

Table 1 indicates that the M-DAB topology shows a very small TDR when compared to that of the DAB, ideal PWM full-bridge, and bi-directional full-bridge topologies. An ideal PWM full-bridge has 8 p.u. of the TDR as an ideal value. However, the bi-directional configuration using this topology requires two converters. Hence, the resulting TDR will be a total of 16 (p.u.). Furthermore, the parasitic component, such as the leakage inductance, increases the device ratings. The bi-directional full-bridge topology has 26 p.u. as a total-device rating, which is obtained from the simulation. Since the leakage inductance of the transformer causes high-current peaks, this topology has a higher total-device rating than the M-DAB topology. As discussed, the M-DAB topology has disadvantages in the current-ripple ratings of the dc-energy-storage capacitors. This value is so large that it limits the use of this topology for high-power applications.

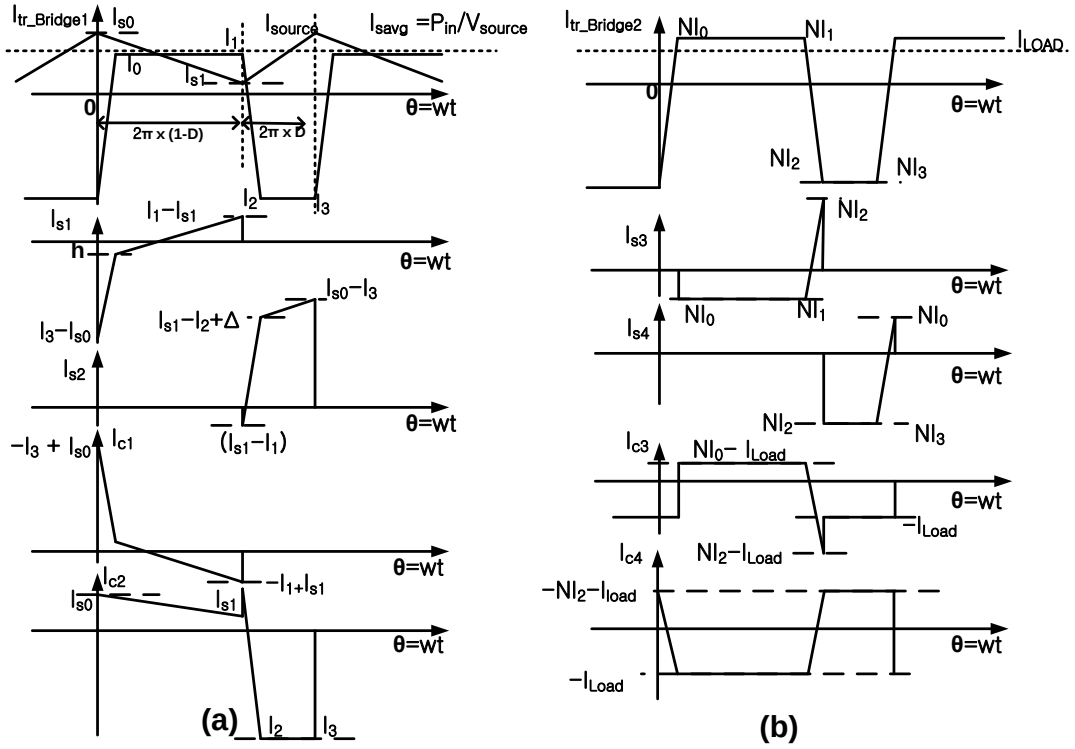


Figure 2.10. Current waveforms of switching devices and capacitors. (a) current waveforms in Bridge 1, (b) current waveforms in Bridge 2.

Table 1. Comparison of topologies in total-device ratings.
(V_{in} = 300-600 and P_o = 20kW, P_{base}=P_o.)

	DAB	Ideal PWM voltage source full-bridge	M-DAB	Bi-directional full-bridge
TDR	44 p.u.	16 p.u.	21.6 p.u.	26 p.u.

2.3. Chapter Summary

This chapter has presented a literature survey on high-power bi-directional dc/dc topologies. The challenges identified in high-power bi-directional dc/dc converters include efficiency, power density, and device ratings.

In resonant topologies, operation at a high frequency is possible with zero-voltage and zero-current switching. Hence, converter design at a high-power density is possible in resonant converters; however, a high total-device rating is a main disadvantage. For high-power applications, the full-bridge, Dual-Active Bridge, and modified Dual-Active Half Bridge converters are presented in the literature survey. Each topology has problems to be resolved.

In summary, the full-bridge converter has problems related to the system's parasitic elements. The Dual-Active Bridge converter has problems in total-device ratings when the source or output voltages vary widely. Although the modified Dual-Active Half Bridge (M-DAB) topology was shown to result in lower total-device ratings for wide voltage ranges, its ratings for dc-energy-storage capacitors are high. These limitations of the conventional topologies require that a novel concept be developed for high-power applications.

CHAPTER 3

DUAL-ACTIVE BRIDGE BUCK-BOOST CONVERTER

3.1. Introduction

Given the attractive attributes of the DAB converter, there have been several attempts [12, 15, 20, 22-25] with DAB and half-bridge converters to achieve low device stresses. One example is the M-DAB converter [20], which uses four active switches and four dc-energy-storage capacitors, using the duty-cycle and the phase-angle control to achieve a bi-directional power flow as well as controlled current stresses.

Other attempts to achieve low-current stresses or extend the ranges of zero-voltage switching, have used switching-signal modulations [12, 15, 25]. However, these efforts still seem to have only a limited effect. Among bi-directional full-bridge topologies, a modified full-bridge converter [17, 18] adopts the dual-active switching but has only duty-ratio control, which results in soft commutation of the primary switches and ZVS in a voltage-source bridge. However, this topology does not use a phase-shift angle as a control variable, which results in high-RMS currents during the shoot-through interval. Another drawback of the modified full-bridge converter is that the peak-current stress is not controllable for wide-load ranges.

This chapter proposes a Dual-Active Bridge Buck-Boost (DAB^3) converter, which achieves minimum-current stresses for a wide input-voltage range, thus realizing minimum TDR. The proposed converter achieves bi-directional power-flow capability by using both the phase-shift angle between two active bridges (H-bridges) and the duty-

cycle control. In the proposed converter, system-parasitic components are effectively utilized, which makes the topology suitable for high-power applications.

3.2. Principle of Operation

The schematic of the DAB[3] converter is shown in Figure 3.1. The topology is similar to the bi-directional full-bridge topology; however, significant differences will be derived from the dual-active switching and the unique-control objectives that enable the control of the device stresses in the topology.

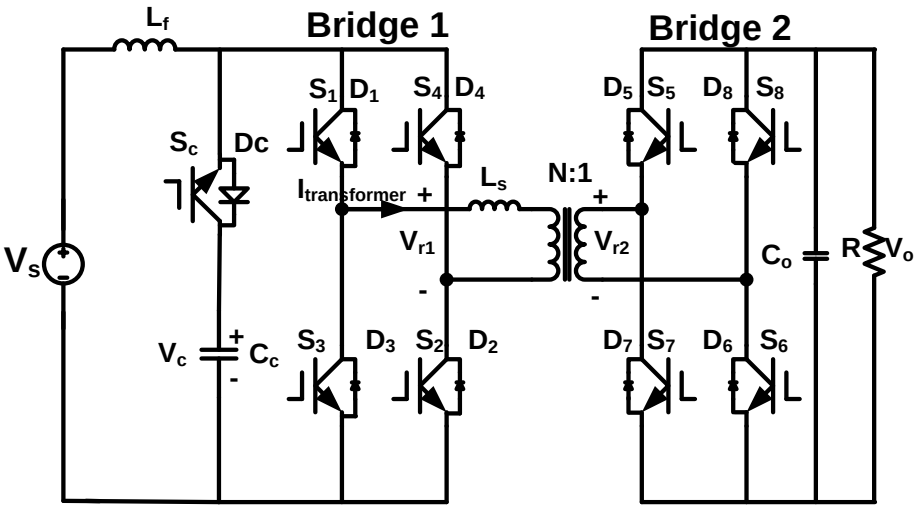
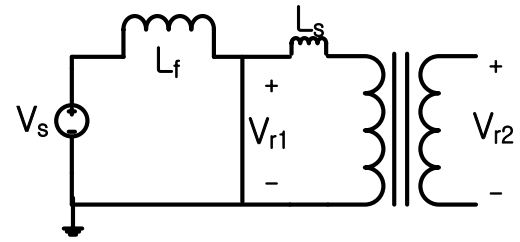


Figure 3.1. Dual-Active Bridge Buck-Boost (DAB[3]) converter.

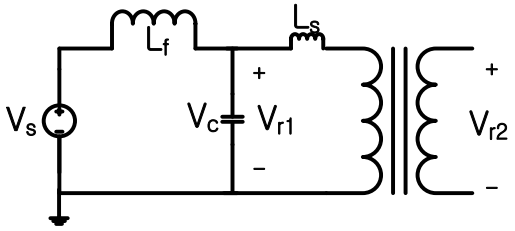
The topology in Figure 3.1 has two H-bridges (Bridge 1 and Bridge 2) along with an active-clamp circuit, which consists of a switch (S_c) and a capacitor (C_c). An input-filter inductor (L_f) is used in the topology to boost the source voltage (V_s). A major-control objective is to have the voltage across the clamp capacitor (V_c) follow the (primary referred) output voltage $N \times V_o$ (with an N:1 isolation transformer) by adjusting the duty ratio (D) and the phase-shift angle (∅). The switches S_c and D_c, the capacitor C_c,

the filter inductor $L_{f,}$ and all the switching devices in Bridge 1, which operate between all switches ON and two switches OFF, can function similarly to a boost converter.

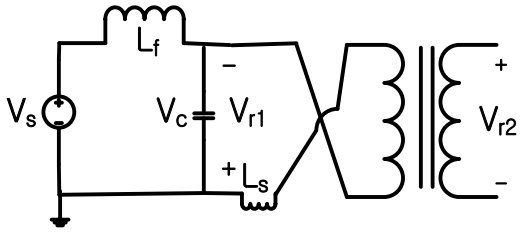
The simplified circuits in Figure 3.2 explain how Bridge 1 operates during a switching period. Bridge 1 has mainly three states, notated as (a), (b) and (c) in Figure 3.2. When all of the switches in Bridge 1 are set to the "on" state as in (a), the slope of the filter-inductor current is positive, and the current increases. This interval is defined as a shoot-through (SH) interval. When either set of switch devices between $\{S_1, S_2, S_c\}$ or $\{S_3, S_4, S_c\}$ is "on," as in (b) and (c), the slope of the filter-inductor current is negative, and the current ramps down, supplying current to the load.



(a) (S_1,S_2,S_3,S_4) are ON state.



(b) (S_1,S_2,S_c) are ON state.



(c) (S_3,S_4,S_c) are ON state.

Figure 3.2. Equivalent circuits for Bridge 1.

By switching the H-bridge to three states, the voltage output of Bridge 1 converts a dc source, V_s, into square ac waves. In Bridge 1, the role of the control signal is to vary the duty ratio (D). During the duty interval, the non-zero part of the square wave is seen in the terminal voltage (V_{r1}) of the transformer as shown in Figure 3.2. The switch set of $\{S_1, S_2, S_c\}$ produces the voltage level V_1, while the set of $\{S_3, S_4, S_c\}$ produces $-V_1$ in the transformer input. The set of $\{S_1, S_2, S_3, S_4\}$ produces the zero level of the voltage in the transformer input.

Transformer-voltage waveforms are plotted against angle in units of radians in Figure 3.3. The relationship between V_s and V_c is given by Equation (8). V_c is controlled by the duty ratio (D) of Bridge 1. During the interval, $\delta(= 2\pi D)$, a clamp switch, S_c remains turned on.

$$\frac{V_s}{2D} = V_c \tag{8}$$

At the same time, the phase-shift angle ($\emptyset$) between Bridge 1and Bridge 2 is varied to control the power flow between Bridge 1 and Bridge 2. The value of the duty ratio (D) that is used for Bridge 2 is the same as the one used for Bridge 1. If the shoot-through (SH) interval is defined in Bridge 1, a zero-voltage (ZV) interval is defined in Bridge 2. In Figure 3.4, equivalent circuits are illustrated for the subintervals during the switching frequency. During the ZV interval, only upper (S_5 and S_8) or lower switching devices (S_6 and S_7) are in the "on" state.

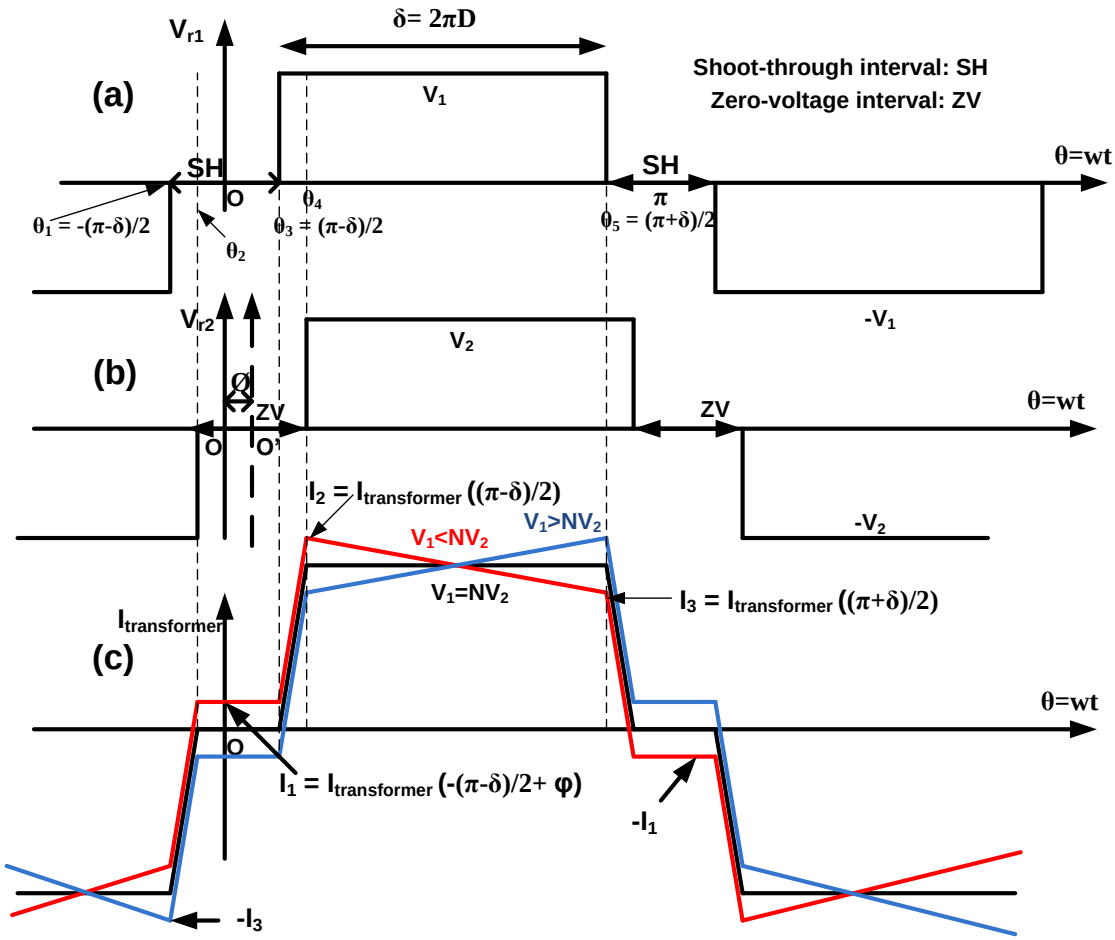
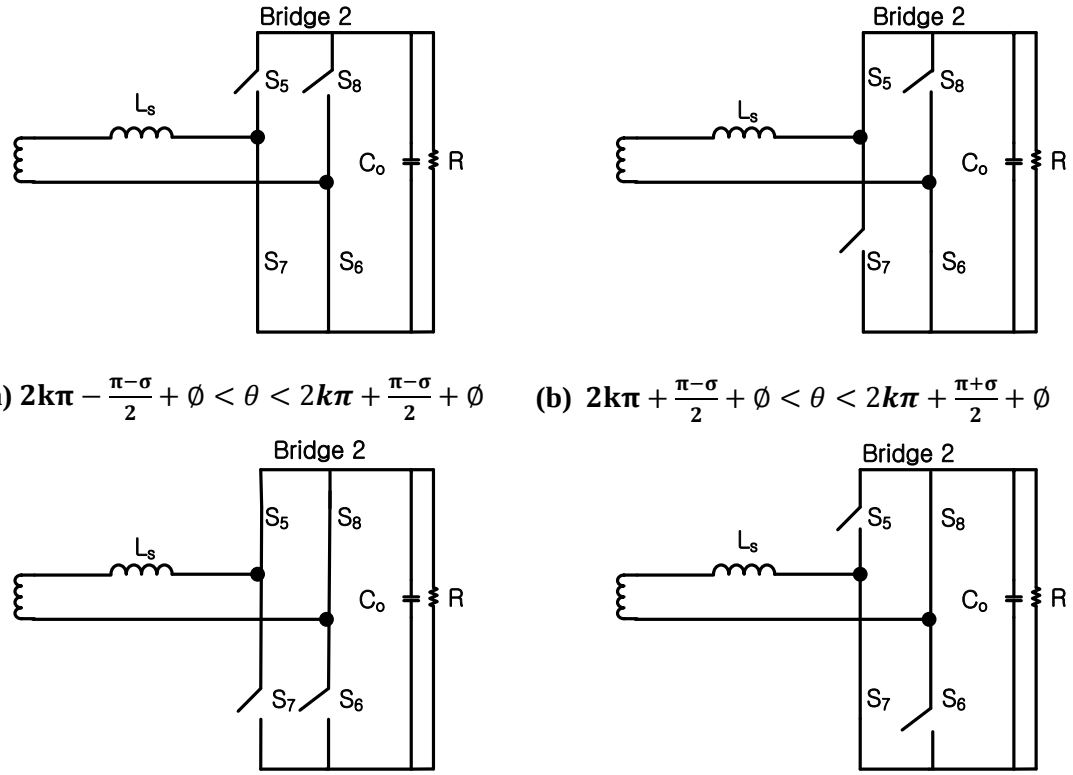


Figure 3.3. Ideal transformer-voltages and -current waveforms. (a) V_{r1}, (b) V_{r2}, (c) transformer current.

The control objective concerning the duty ratio (D) is to make an operating point become "$V_c = N \times V_o$" for a source voltage (V_s). If the condition, "$V_c = N \times V_o$" is maintained over an entire operating point, the transformer current can be controlled to achieve low device stresses. As shown in the black-colored waveform of (c) in Figure 3.3, when the condition of $V_1 = N \times V_2$ is satisfied, the slope of the transformer becomes zero and causes minimum device stress.



(a) $\mathbf{2k\pi} - \frac{\pi-\sigma}{2} + \emptyset < \theta < 2k\pi + \frac{\pi-\sigma}{2} + \emptyset$ **(b)** $\mathbf{2k\pi} + \frac{\pi-\sigma}{2} + \emptyset < \theta < 2k\pi + \frac{\pi+\sigma}{2} + \emptyset$

(c) $\mathbf{2k\pi} + \frac{\pi+\sigma}{2} + \emptyset < \theta < 2k\pi + \frac{3\pi-\sigma}{2} + \emptyset$ **(d)** $\mathbf{2k\pi} + \frac{3\pi-\sigma}{2} + \emptyset < \theta < 2k\pi + \frac{3\pi+\sigma}{2} + \emptyset$

Figure 3.4. Equivalent circuits in Bridge 2 for a switching period. *k*= 0,1,2,…

Piecewise-linear equations for the transformer current can be derived based on the current waveforms. In the derivation, $\omega = 2\pi f_s$ is defined.

$$I(\theta) = \frac{NV_2}{\omega L_s}\left(\theta + \frac{\pi - \delta}{2}\right) - I_3 \qquad \text{for } \theta_1 < \theta < \theta_2 \qquad (9)$$

$$I(\theta) = I_1 \qquad \text{for } \theta_2 < \theta < \theta_3 \qquad (10)$$

$$I(\theta) = \frac{V_1}{\omega L_s}\left(\theta - \frac{\pi - \delta}{2}\right) + I_1 \qquad \text{for } \theta_3 < \theta < \theta_4 \qquad (11)$$

$$I(\theta) = \frac{(V_1 - NV_2)}{\omega L_s}\left(\theta - \frac{\pi - \delta}{2} - \emptyset\right) + I_2 \qquad \text{for } \theta_4 < \theta < \theta_5 \qquad (12)$$

With the initial conditions, I_1, I_2, I_3 can be obtained.

$$I_1 = \frac{-\delta}{2\omega L_s} V_1 + \frac{\delta}{2\omega L_s} NV_2 \qquad (13)$$

$$I_2 = \frac{(2\emptyset - \delta)}{2\omega L_s} V_1 + \frac{\delta}{2\omega L_s} NV_2 \qquad (14)$$

$$I_3 = \frac{\delta}{2\omega L_s} V_1 + \frac{2\emptyset - \delta}{2\omega L_s} NV_2 \qquad (15)$$

When the condition, V_1=NV_2, is satisfied, I_1, I_2, I_3 becomes simple.

$$I_1 = 0,\ I_2 = I_3 = \frac{\emptyset}{\omega L_s} V_1 \qquad (16)$$

When the phase-shift angle ($\emptyset$) is greater than θ_3, the waveform of the transformer current changes its shape. Hence, a new set of equations should be derived. In Figure 3.5, transformer voltages and currents are illustrated for $\emptyset > \theta_3$. Equations (17)-(20) are transformer equations when $\emptyset > \theta_3$.

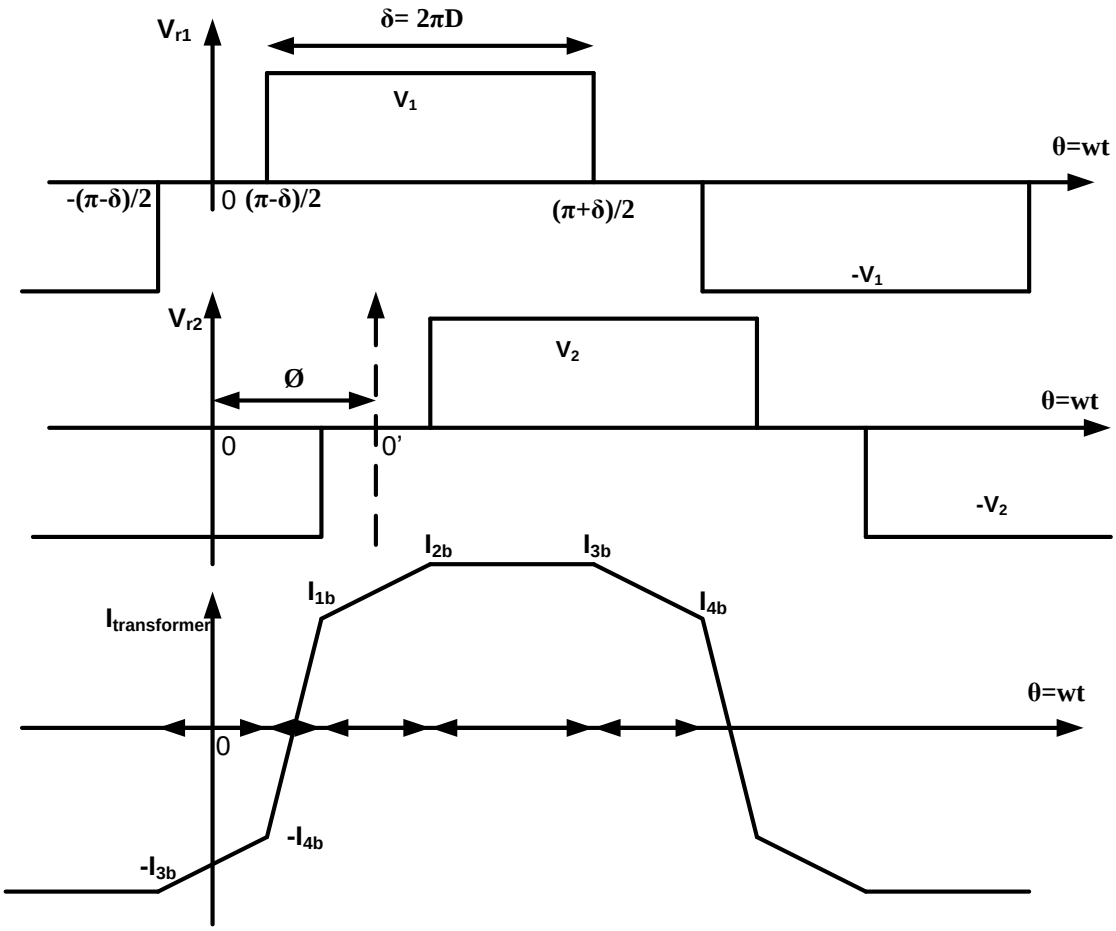


Figure 3.5. Ideal transformer-voltages and-current waveforms for a large phase-shift angle, $\emptyset > \boldsymbol{\theta_3}$ $(= \mathbf{2\pi D})$.

$$I(\theta) = \frac{NV_2}{\omega L_s}\left(\theta + \frac{\pi - \delta}{2}\right) - I_{3b} \qquad \text{for } \theta_1 < \theta < \theta_2 \qquad (17)$$

$$I(\theta) = \frac{NV_2}{\omega L_s}\left(\theta - \frac{\pi - \delta}{2}\right) - I_{4b} \qquad \text{for } \theta_2 < \theta < \theta_3 \qquad (18)$$

$$I(\theta) = \frac{NV_2}{\omega L_s}\left(\theta + \frac{\pi - \delta}{2} - \emptyset\right) - I_{1b} \qquad \text{for } \theta_3 < \theta < \theta_4 \qquad (19)$$

$$I(\theta) = \frac{NV_2}{\omega L_s}\left(\theta - \frac{\pi - \delta}{2} - \emptyset\right) - I_{2b} \qquad \text{for } \theta_4 < \theta < \theta_5 \qquad (20)$$

With the initial conditions, I_{1b}, I_{2b}, I_{3b}, I_{4b} can be obtained.

$$I_{1b} = \frac{\delta+2\emptyset-2\pi}{2\omega L_s} V_1 + \frac{\delta}{2\omega L_s} NV_2 \tag{21}$$

$$I_{2b} = \frac{2\emptyset-\delta}{2\omega L_s} V_1 + \frac{\delta}{2\omega L_s} NV_2 \tag{22}$$

$$I_{3b} = \frac{\delta}{2\omega L_s} V_1 + \frac{2\emptyset-\delta}{2\omega L_s} NV_2 \tag{23}$$

$$I_{4b} = \frac{\delta}{2\omega L_s} V_1 + \frac{\delta+2\emptyset-2\pi}{2\omega L_s} NV_2 \tag{24}$$

3.3. Characteristics of the DAB^3 Converter

The transformer current has been analytically modeled using linear equations as shown in Equations (9)-(24). As can been seen in Figure 3.3 and Figure 3.5, the transformer current changes its form when the phase-shift angle ($\emptyset$) reaches a critical angle ($\emptyset_c = \pi$-2πD). The change of the current equations indicates the change of the output-power characteristics.

In Figure 3.6, output power is plotted for the control variables, D and $\emptyset$. The phase-shifted voltages (V_{r1},V_{r2}) across the leakage inductance (L_s) drive the transformer current. Phase-shift angle, $\emptyset$, controls the direction and the magnitude of the power flow, which is made possible through the active switching in both H-bridges.

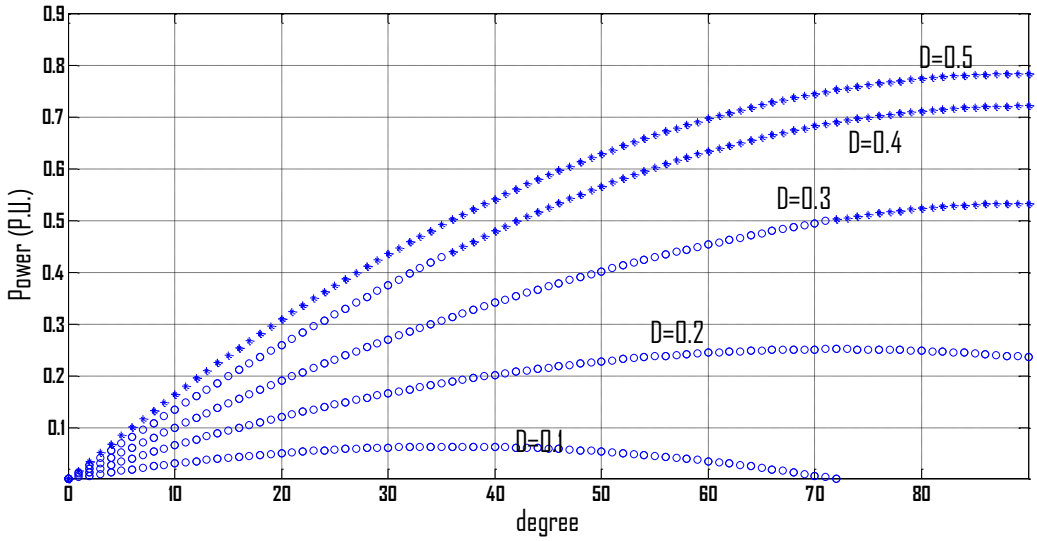


Figure 3.6. Plot of output power (P_o (p.u.)) with the conditions $V_1 = NV_2$ (N=1). D (duty ratio) = $\frac{\delta}{2\pi}$, (o: $0 < \emptyset < \pi - 2\pi D$, $*$: $\pi - 2\pi D < \emptyset < \frac{\pi}{2}$).

$$P_o = P_{in} = \frac{1}{2\pi}\int_0^{2\pi} v_{r1}(\theta) \times i(\theta) d\theta \qquad \text{for } \theta_1 < \theta < \theta_2$$

$$= \frac{V_1 \times NV_2}{2\pi w L_s}(-\emptyset^2 + 4\pi D\emptyset)d\theta \qquad \text{for } 0 < \emptyset < \pi - 2\pi D \qquad (25)$$

$$= \frac{V_1 \times NV_2}{\pi w L_s}(-(\emptyset - \frac{\pi}{2})^2 + \frac{\pi^2}{4} - 2\pi^2(D - \frac{1}{2})^2) \qquad \text{for } \pi - 2\pi D < \emptyset < \pi/2 \qquad (26)$$

The steady-state power equations in (25) and (26) show that the transferred output power is a function of the duty cycle (D) and the phase-shift angle ($\emptyset$). By increasing the phase angle, the output power increases until the phase angle reaches a boundary value ($\pi - 2\pi D$), at which point the trajectory changes to a different equation; however, the two equations, (25) and (26), are continuous in the boundary points. The output power is monotonic with the phase-shift angle ($\emptyset$) and the duty cycle (D). This fact indicates that the output power can be controlled using negative feedback.

From Equations (25) and (26), the operating points which transfer the maximum power from the input to the output can be obtained. The output power reaches a maximum point when one of the conditions, $\frac{\partial P}{\partial \emptyset} = 0$ or $\frac{\partial P}{\partial D} = 0$, is satisfied, in which case the following Equations (27)-(30) are obtained.

$$\frac{\partial p}{\partial D} = \frac{V_1 \times NV_2}{2\pi\omega L_s}(4\pi\emptyset) = 0 \qquad \text{for } 0 \le \emptyset \le \pi - 2\pi D \qquad (27)$$

$$\frac{\partial p}{\partial D} = \frac{V_1 \times NV_2}{\pi\omega L_s}\left(-4\pi^2\left(D - \frac{1}{2}\right)\right) = 0 \qquad \text{for } \pi - 2\pi D < \emptyset \le \frac{\pi}{2} \qquad (28)$$

$$\frac{\partial p}{\partial \emptyset} = \frac{V_1 \times NV_2}{2\pi w L_s}(-2\emptyset + 4\pi D) = 0 \qquad \text{for } 0 \le \emptyset \le \pi - 2\pi D \qquad (29)$$

$$\frac{\partial p}{\partial \emptyset} = \frac{V_1 \times NV_2}{\pi\omega L_s}\left(-2\left(\emptyset - \frac{\pi}{2}\right)\right) = 0 \qquad \text{for } \pi - 2\pi D < \emptyset \le \frac{\pi}{2} \qquad (30)$$

From Equations (27) and (28), the maximum power can be transferred at D = 0.5. In Equations (29) and (30), the phase angle $\emptyset$ gives the maximum output power at $\emptyset = 2\pi D$ if $\emptyset$ is less than π-2πD. When $\emptyset$ is greater than π-2πD but less than $\frac{\pi}{2}$, the maximum power transfers at $\emptyset = \frac{\pi}{2}$.

Equations (13)-(26) can be used to estimate peak currents of the transformer for a wide-power range. In the estimation, the conditions and parameters used are L_s = 8 uH and f_s = 35 kHz. Other parameters are normalized for given base units, $V_b = V_1$ and $Z_b = 2\pi\omega L_s$. In Figure 3.7 and Figure 3.8, the maximum (peak) values of the transformer currents are plotted. The minimum- peak current is obtained at d (= NV_2/V_1) = 1, which is the flat-top condition.

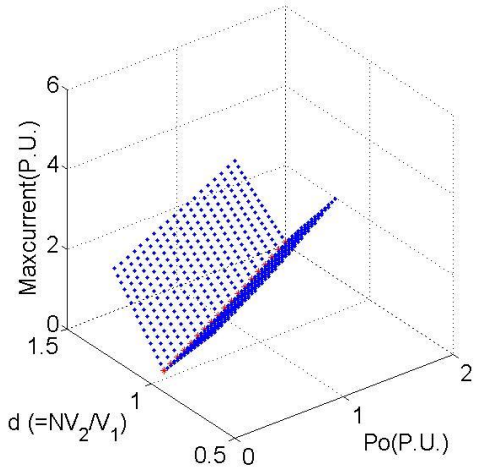


Figure 3.7.Peak-transformer current when D (duty ratio) = 0.4.
$V_b = V_1$, $Z_b = 2\pi\omega L_s$, $P_b = V_b I_b$, $L_s = 8$ uH.

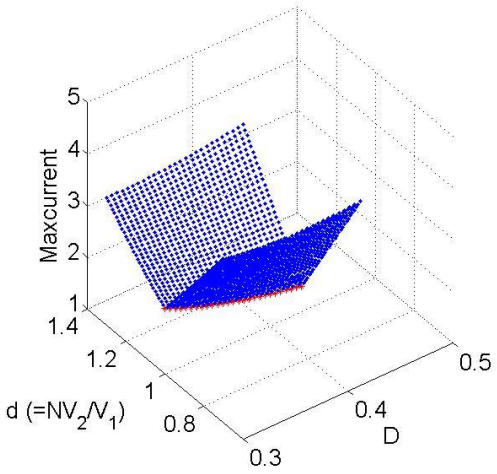


Figure 3.8. Peak-transformer current when P_o=1.2282 (P.U.).
$V_b = V_1$, $Z_b = 2\pi\omega L_s$, L_s =8 uH.

In Figure 3.9, the total-device rating is plotted for a wide range of clamp/output voltages and wide duty-ratio ranges. Figure 3.9 indicates that at the flat-top condition (d=1), the lowest total-device ratings are obtained in the DAB[3] concept.

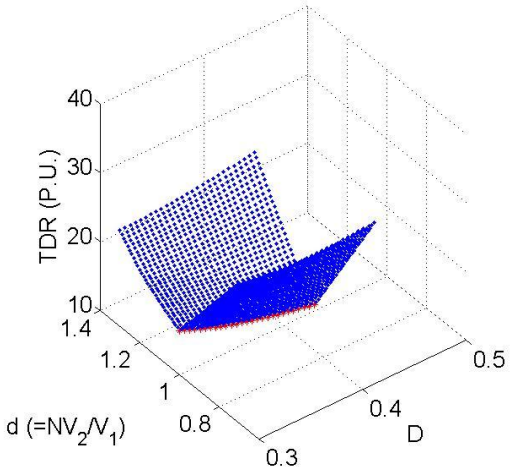


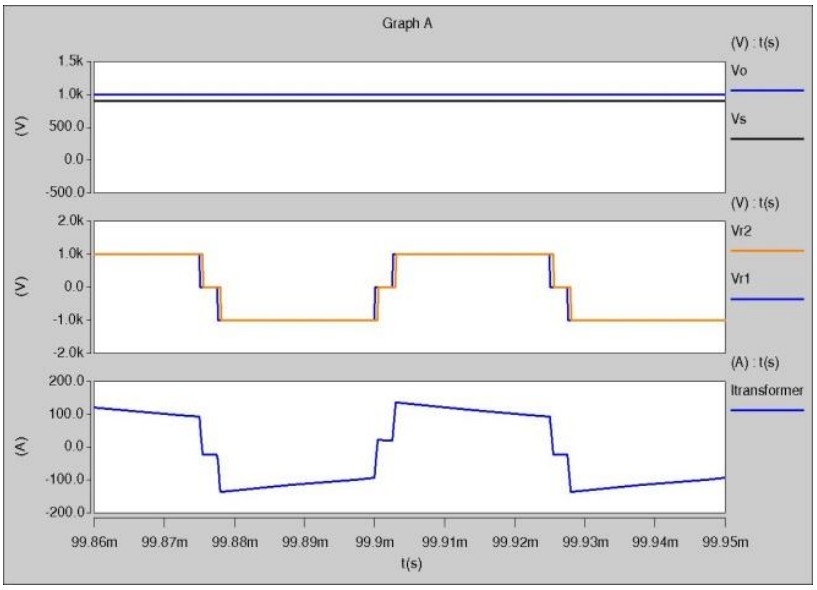
Figure 3.9. TDR for wide ranges of duty ratio (D) and d (=NV_2/V_1) when $P_b = P_o$ = 10 kW.

3.4. Proof of Concept

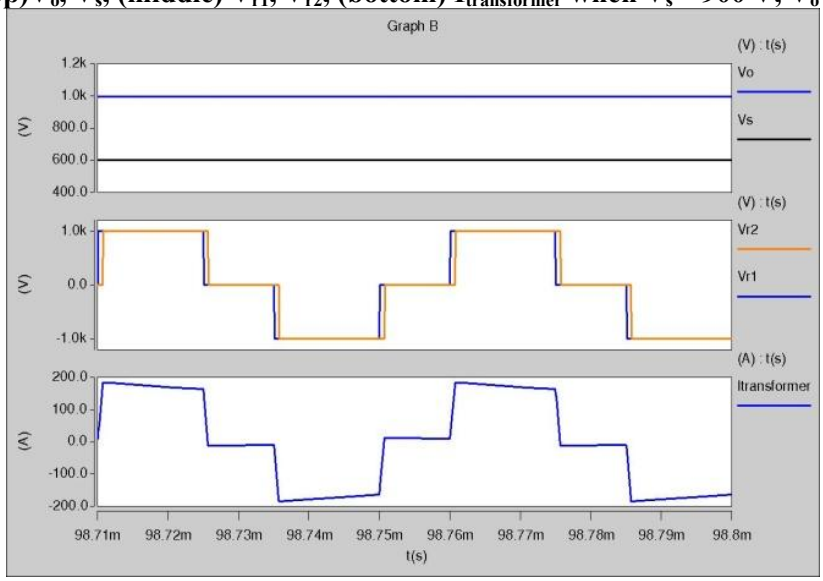
The simulations of the DAB[3] converter, shown in Figure 3.10, prove that the transformer current can be controlled to have a flat top. The conditions and parameters in the simulations are V_s = 900, 600 V, L_s = 4 uH (a series ac inductor), L_f = 100 uH (a dc filter inductor), f_s = 20 kHz (the switching frequency), V_o = 1000 V (the dc-link voltage in Bridge 2), and P_o = 100 kW (the load power). In both cases (V_s = 900 and 600 V), a clamp-capacitor voltage, V_c, is controlled to track NV_o.

A proof of concept was built and tested preliminarily with an output power of 180 W. The results are presented in Figure 3.11. The experimental circuit was operated at 40 kHz. A 100 uH filter inductor (L_f) was used, while the series inductance was kept at 8 uH. The turn ratio of the isolation transformer was 1:1. In Figure 3.11(a) and (b), the pink-colored curve shows the measured current of the transformer in Bridge 1. The green-and red-colored waveforms are the input-and output-terminal voltages of the transformer (V_{r1} and V_{r2}), respectively. Figure 3.11(a) shows the plots when the source

voltage, V_s equals 30 V, and Figure 3.11(b) shows the plots when the source voltage, V_s equals 50 V. In both figures, the output voltages in blue have a constant value of 60 V. The current waveforms in the transformer have flat tops in both cases.

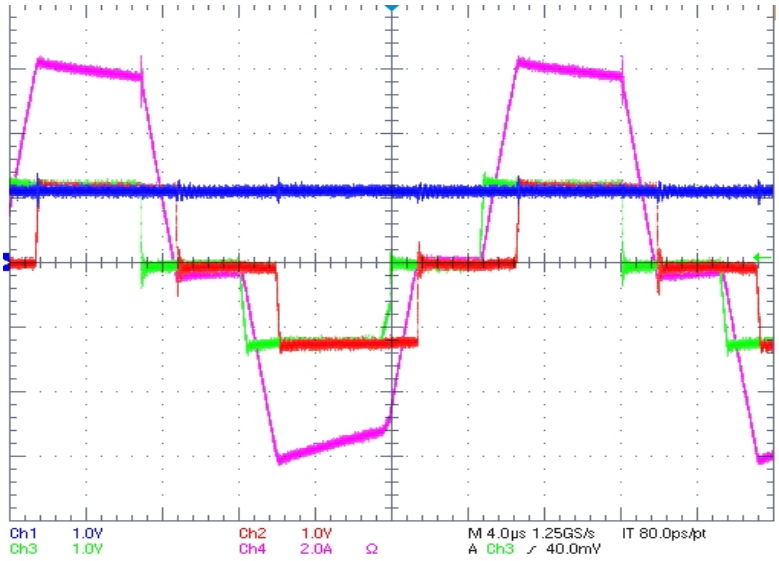


(a) (top)V_o, V_s, (middle) V_{r1}, V_{r2}, (bottom) $I_{transformer}$ when V_s = 900 V, V_o = 1000 V,

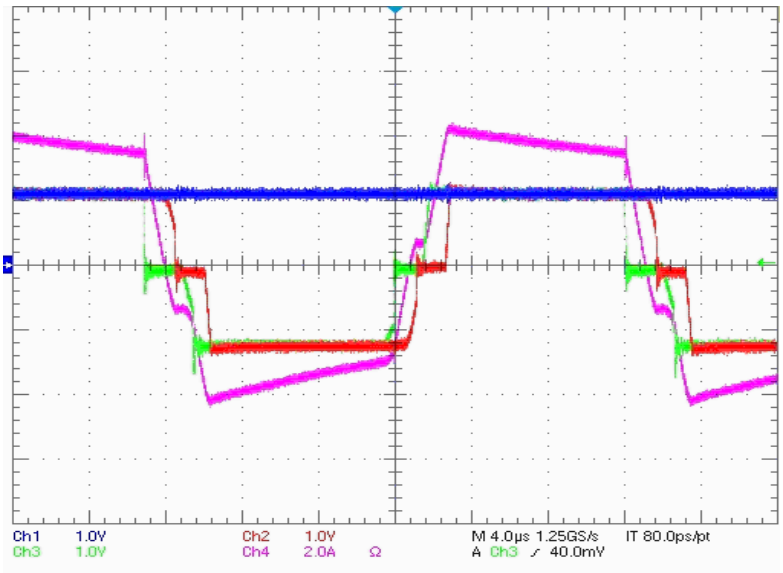


(b) (top) V_o, V_s, (middle) V_{r1}, V_{r2} , (bottom) $I_{transformer}$ when V_s = 600 V, V_o = 1000 V.

Figure 3.10. Simulation results with P_o = 100 kW.



(a) V_s = 30 V,V_{r1}(green),V_{r2}(red) , $I_{transformer}$(pink), and V_o = 60 V (blue),



(b) V_s = 50 V,V_{r1}(green),V_{r2}(red) , $I_{transformer}$(pink), and V_o = 60 V (blue).

Figure 3.11. Experimental result with P_o = 180 W.

3.5. Comparison of Topologies

In this section, the DAB[3] converter is compared with conventional topologies over several metrics, such as the total-device ratings (TDR), the capacitor-current ratings, the

transformer ratings, and the number of devices, etc. Comparisons are based on analytical equations with respect to the peak and RMS values of the device currents. The peak and RMS values are used to obtain the TDR of the switching devices, the current-ripple ratings (A_{RMS}) of the capacitors, and the transformer ratings**.** For the comparison, the conditions and parameters are selected: V_s = 900~600 V, L_s = 4 uH, L_f = 100 uH, F_{sw} = 20 kHz, V_o = 333 V, P_o = 100 kW, transformer turn ratio = 1000 : 333.

For the Dual-Active Bridge converter, analytical expressions of an output power (P_o) and peak-current points (I_{L1} and $I_{L2,}$ as shown in Figure 3.12) are given in Equations (31)-(33).

$$P_o = \frac{NV_1V_2}{\pi\omega L_s}(-\emptyset^2 + \pi\emptyset) \tag{31}$$

$$I_{L1} = \frac{V_1}{\omega L_s}\left(\emptyset - \frac{\pi}{2}\right) + \frac{NV_2}{\omega L_s}\left(\frac{\pi}{2}\right) \tag{32}$$

$$I_{L2} = \frac{1}{2\omega L_s}(\pi V_1 + NV_2(2\emptyset - \pi)) \tag{33}$$

where,

f_s (H_z) = the switching frequency with ω= $2\pi f_s$

$\emptyset$ = the phase shift angle (in radian),

$N = \frac{\text{number of primary turns}}{\text{number of secondary turns}}$

V_1 = dc-link voltage in Bridge 1

V_2 = dc-link voltage in Bridge 2

In Table 2, the current stresses of the transformers are compared. The DAB converter shows a very high current (1050 A) when the condition is V_s = 600 V, and V_o = 333 V (V_o' = 900 V). The fact that the voltage difference, ΔV = V_1-NV_2, across the

inductor (L_s=4 uH) is as large as 300 V over the time interval of 0.5× T_s - $\frac{\emptyset}{2\pi}$ ×T_s causes high current slopes in the DAB converter. Figure 3.12 (a) illustrates the transformer current of the DAB topology when V_1 is not equal to N×V_2. Figure 3.12(a) also indicates that the DAB topology can have the best performance when V_1 = NV_2.

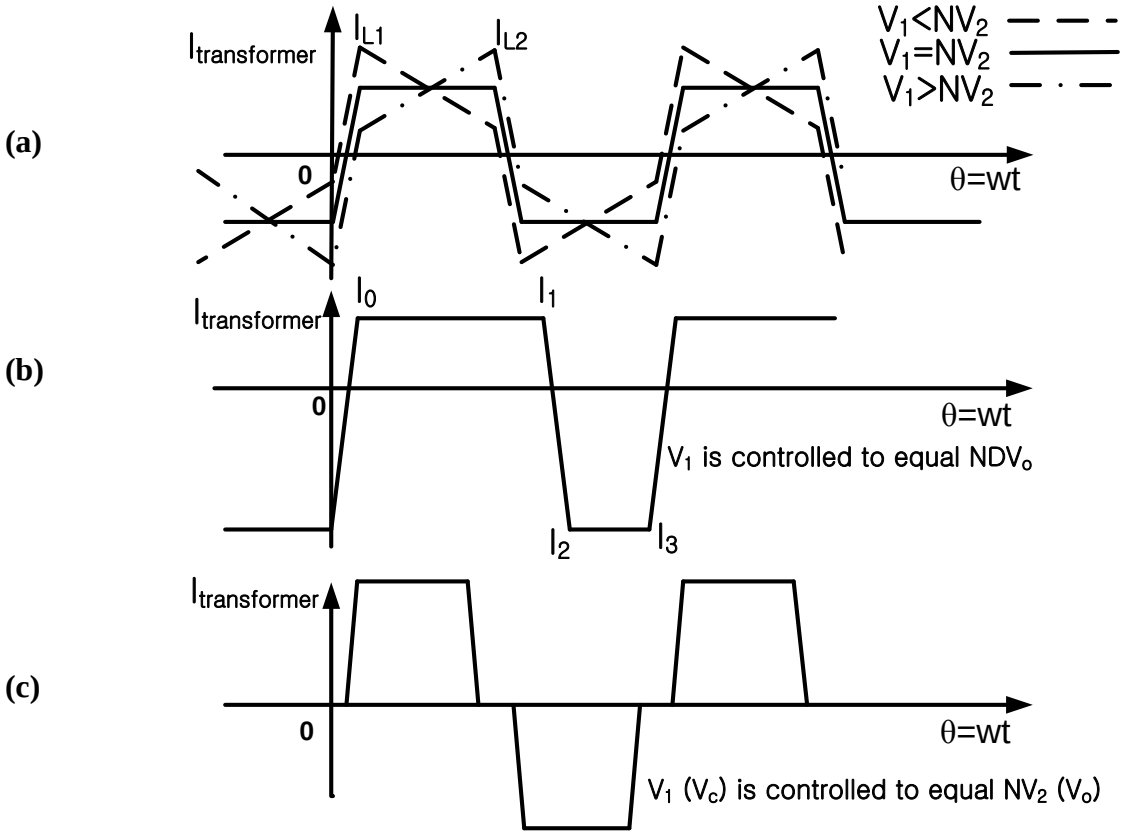


Figure 3.12.Transformer current waveforms.
(a) DAB, (b) M-DAB, (c) DAB[3].

Increasing L_s can decrease the slopes of the transformer currents; however, a higher inductance, L_s requires a higher magnitude of the phase-shift angle, which results in an increase of RMS values of device currents. The peak currents of M-DAB and DAB[3] are relatively low when the flat-top conditions are obtained, as illustrated in Figure 3.12(b) and (c), by controlling the duty ratio and the phase-shift angle. The DAB[3]

converter has only 170.5 Amperes as the peak current of a device for the given condition when the flat-top condition is satisfied ($V_c = 3 \times V_o = 1000$ V). Current stresses in the switching devices of the M-DAB converter are calculated based on analytical derivations in Appendix A. The peak-device current is calculated as 504 A on the primary (Bridge 1) side. The data in Table 3 is used to calculate the TDR for each topology, which is shown in Table 4. DAB^3 has an extremely low TDR in wide-input/output conditions when compared with other topologies. The M-DAB converter has a lower TDR than the DAB converter, but has a greater TDR than the DAB^3 topology.

Table 2.Comparison of transformer current stresses.
L_s = 4 uH, F_{sw} = 20 kHz, P_o = 100 kW.(considered only in Bridge 1.)

	DAB^3(3:1 turn ratio)		M-DAB(3.6:1)		DAB(900:333)	
	V_s(900~600 V)	V_o(333 V)	V_s(=900~600 V)	V_o(333 V)	V_s(900~600 V)	V_o(333 V)
Amps	170.5A (600V, D=0.3)		174A (600V, D=0.5)		1050A (600V, D=0.5)	
	111A (900V, D=0.45)		365A (900V, D=0.25)		113.16A(900V,D=0.5)	

Table 3. Comparison of peak currents of switching devices.

		DAB^3(3:1 turn ratio) V_s(900~600 V), V_o(333 V)	M-DAB(3.6:1) V_s(900~600 V), V_o(333 V)	DAB(900:333) V_s(900~600 V), V_o(333 V)
Amps	Bridge1	170.5 A	504 A	1050 A
	Bridge2	511.5 A	1313 A	2837 A

Table 4. Comparison of total-device ratings (TDR) with P_b=P_o.

TDR	DAB^3(3:1 turns ratio) V_s(900~600 V), V_o(333 V)	M-DAB(3.6:1) V_S(900~600 V), V_o(333 V)	DAB(900:333) V_S(900~600 V), V_o(333 V)
	15 P.U.	20.85 P.U.	75.6 P.U.

Table 5 shows the current-ripple ratings (A_{RMS}) of the capacitors which are used in the topologies. The DAB^3 converter requires a low rated (20 A_{RMS}) active-clamp capacitor, and a high-rated (250 A_{RMS}) output capacitor (C_o) in Bridge 2. The rating of C_o, which is high, is caused by the zero-voltage intervals during which the transformer

current circulates. During this interval, power is not transferred from the source to the load. The output capacitor (C_o) supplies the current required for the load. The DAB converter uses output/input-filter capacitors, which have low current ratings in the flat-top conditions; however, when the difference between the input and output voltages becomes large, the rating of an output capacitor should become very high. Table 5 also shows that the M-DAB converter requires four energy-storage capacitors, which have high-current ratings. This fact is the main limitation of the M-DAB topology.

Table 5. Comparison of capacitor-current ratings.

CONVERTER(capacitors), (turns ratio)	**RATING (A_{RMS})**
DAB(C_o/C_{in}), (3:1)	Very High
M-DAB (C_1/C_2/C_3/C_4), (3.6:1)	High55/200/250/569 A_{RMS}
DAB^3 (C_c/C_o), (900:333)	Low/High (20 A_{RMS}/250 A_{RMS})

In Table 6, transformer [KVA] ratings are estimated and compared between DAB^3 and M-DAB topologies under the same conditions. The transformer [KVA] ratings are defined in Equation (34).

Table 6. Comparison of transformer currents, voltages, and ratings.

	DAB^3(3:1 turn ratio)		**M-DAB(3.6:1 turn ratio)**	
	V_s = 900 V	**V_s = 600 V**	**V_s = 900 V**	**V_s = 600 V**
Ampere in RMS	106	131	204	172
Volt in RMS	948	774	520	600
$[KVA]_T$	2.0134×P_o	2.03×P_o	2.1253×P_o	2.0649×P_o

$$[KVA]_T = \frac{1}{2}\left(V_{RMS\_pri} \times I_{RMS\_pri} + V_{RMS\_sec} \times I_{RMS\_sec}\right) \quad (34)$$

The transformer rating of the DAB^3 topology is almost close to the rating of the M-DAB topology. The transformer-current rating of the M-DAB topology is higher than that of the DAB^3 topology; however, the energy-storage capacitors divide the output

voltage. Hence, the transformer-voltage rating of the M-DAB topology is much smaller than that of the DAB^3 topology.

Table 7 summarizes the number of components that are required. All of the DAB, M-DAB, and DAB^3 converters use leakage or series inductance as an energy-transfer element. The DAB^3 and M-DAB converters require a dc-filter inductor, which is used to boost a voltage source (V_s), whereas the DAB converter does not require any dc-filter inductor, which results in a minimal number of devices; however, extremely high currents can be observed when the DAB converter is operated over a wide-input/output range.

Table 7. Comparisons of required components.

	DAB^3	**M-DAB**	**DAB**
Switching Devices	9	4	8
Capacitor	1/(2)	4/(2)	(2)
Inductor { filter /(leakage)}	1/(1)	1/(1)	(1)

In this section, the DAB^3 and M-DAB topologies have been compared with the DAB topology. All three topologies use system parasitic components effectively. Both M-DAB and DAB^3 have a reasonably low TDR. The DAB^3 topology has shown the main advantages in the TDR (p.u.) and the RMS-current ratings of the capacitors (A_{RMS}) when compared to the M-DAB converter for wide-input/output range conditions.

3.6. Chapter Summary

This chapter proposes a converter concept (the DAB^3 converter) which has controlled device stresses. In the converter, the parasitic elements such as the leakage inductance and parasitic capacitors are effectively used. The leakage inductance is used

to transfer the power. Hence, the converter has very reduced-voltage stresses during the switching transitions. The full-bridge converters require additional circuits such as active- or passive-clamp circuits to deal with the high-voltage stresses that are caused by the system's parasitic elements.

The benefit of the DAB^3 concept is low total-device ratings. In the DAB^3 topology, the capacitor voltage (V_c) in the active-clamp circuit is regulated by the duty-cycle control. The load power or voltage (V_o) is controlled by the phase-shift angle ($\emptyset(t)$) between Bridge1 and Bridge 2. The controller for the clamp-capacitor voltage, V_c can be set so that V_c can track to NV_o. At this operating point, the minimum device rating can be obtained.

Finally in this chapter, the DAB^3 converter is compared with the conventional topologies. Through this comparison, the DAB^3 topology is seen to have advantages in total-device ratings, capacitor ratings, and transformer ratings.

CHAPTER 4

PERFORMANCE CHARACTERIZATION

4.1. Introduction

In the previous chapter, the device-current stresses in the DAB^3 converter were shown to be minimized for a wide operating range. This chapter describes another benefit of the DAB^3 concept. Maintaining the condition, $V_c = NV_o$, achieves not only the minimum total-device rating (TDR), but also zero-voltage switching (ZVS), which reduces switching loss. Sometimes the condition "$V_c = NV_o$" may not be available; however, ZVS is available in non flat-top but in limited conditions with the DAB^3 switching strategy. Hence, the ZVS operating region needs to be analyzed. The slope of the transformer current is determined by the voltage levels of the clamp and output capacitors, C_c and C_o respectively. Hence, ZVS depends on the voltage conditions of the capacitors across the leakage inductance of the transformer. This chapter examines and specifies the conditions for ZVS.

This chapter also discusses power-loss estimation. The power loss in the converter originates mainly from the switching devices, the magnetic devices, and the parasitic resistances of the capacitor banks. Based on simulation results, the minimum switching loss occurs under the flat-top condition. This simulation result supports operation under the flat-top condition. Finally, this chapter analyzes the total power loss for the minimum loss designs and estimates the resulting volumes of the devices.

4.2. Zero-Voltage Switching of the DAB^3 Converter

Figure 4.1 illustrates the ideal current and voltage waveforms of the switching devices when the flat-top condition ($V_1 = NV_2$) is achieved. In Bridge 1, the current (I_{clamp}) in the active-clamp circuit starts to flow in the anti-parallel diode (D_c) and reverses its direction to flow through the IGBT device (S_c). When current starts to flow through the IGBT device, the voltage level across the device is zero if the threshold voltage is neglected. Hence, the turn-on loss for ZVS can be neglected. This process is called zero-voltage switching (ZVS).

ZVS is also available in other switching devices, as well as in Bridges 1 and 2. Over limited operating conditions, all of the switching devices in Bridge 2 can be turned on under ZVS conditions. When V_1 is not equal to NV_2, some of the switching devices may not realize ZVS. However, low-switching loss can be obtained if V_c and V_o are carefully controlled. Figure 4.2 illustrates the current waveforms of the isolation transformer and the switching devices in Bridge 2 in boost mode, with power flowing from Bridge 1 to Bridge 2. This shows that S_6 and S_8 can realize ZVS only when $V_1 \leq NV_2$. However, S_5 and S_7 can realize ZVS over wider operating conditions. The ZVS conditions for the switch devices S_5 and S_7 can be analyzed with respect to the control inputs (D and $\emptyset$) and the voltage ratio ($d= NV_2/V_1$).

Figure 4.3 illustrates the current waveforms in buck mode, with power flowing from Bridge 2 to Bridge 1. The current waveforms in buck mode are different than boost mode. From Figure 4.2 and Figure 4.3, the ZVS conditions can be derived for the switching devices. Table 8 summarizes the ZVS conditions for the switching devices.

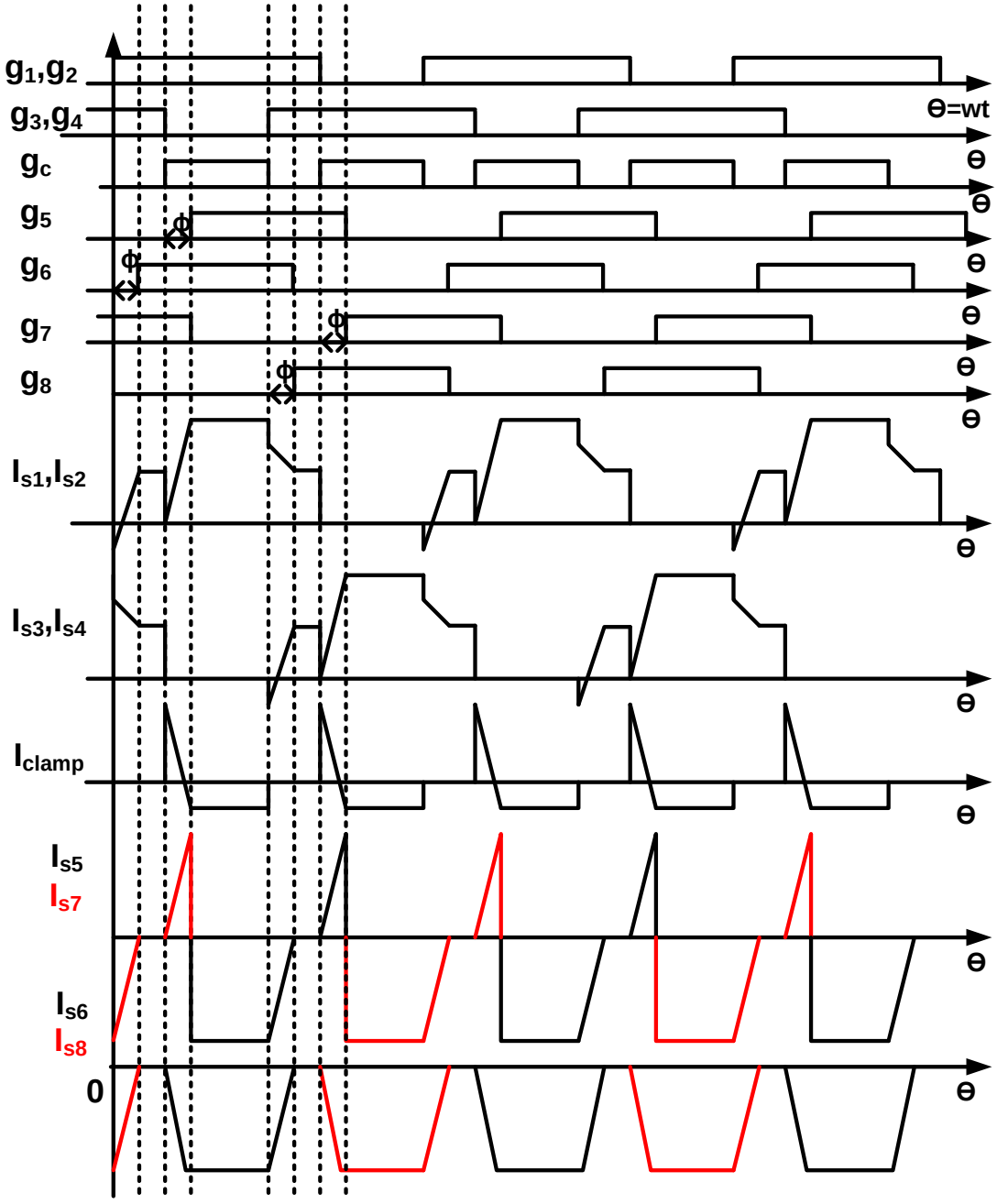


Figure 4.1. Gating signals (g_c, g_1-g_4) and ideal switch currents (I_{clamp}, I_{s1}-I_{s8}) in boost mode when $V_1 = N \times V_2$ is satisfied.

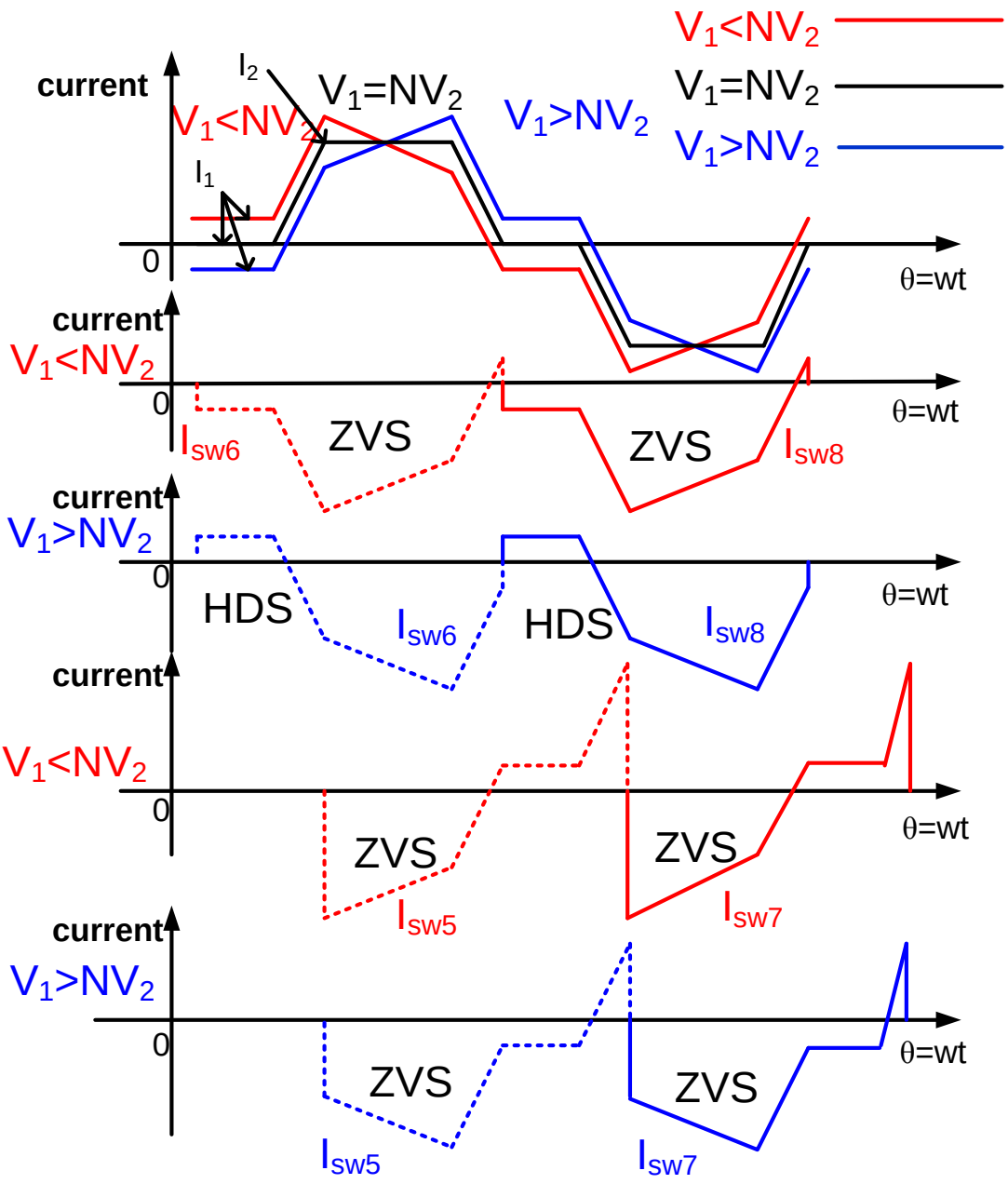


Figure 4.2. Transformer current and switch current waveforms of Bridge 2 in boost mode under three conditions: V_1 less than, equal to, and greater than NV_2

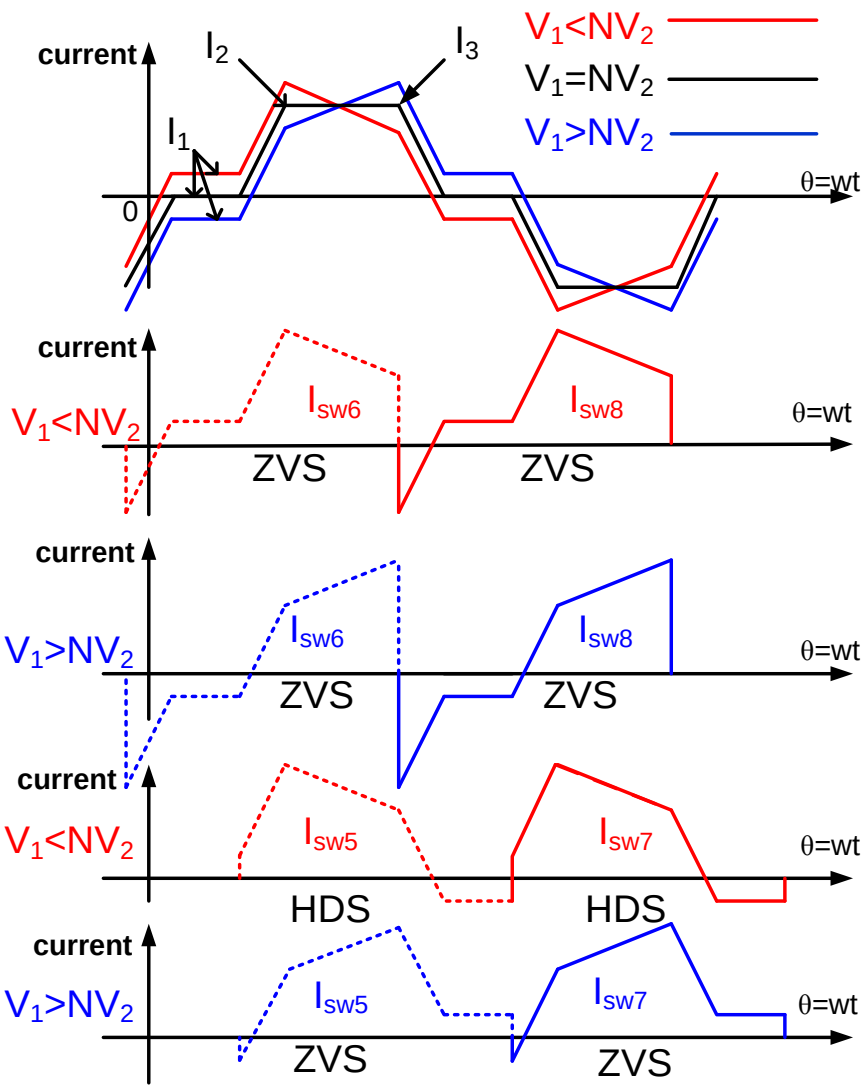


Figure 4.3. Transformer and switch current waveforms of Bridge 2 in buck mode under three conditions: V_1 less than, equal to, and greater than NV_2.

Table 8. ZVS conditions for the switching devices.

Direction of power flow	Phase-angle conditions	$S_{1,2,3,4}$	$S_{5,7}$	$S_{6,8}$
B_1 to B_2	$0 \le \phi < \phi_c$	$\frac{1}{2}\times(I_s-I_3) < 0$	$I_2>0$	$I_1>0$
	$\phi \ge \phi_c$	$\frac{1}{2}\times(I_s-I_{L3b}) < 0$	$I_{2b}>0$	$I_{1b}>0$
B_2 to B_1	$0 \le \phi < \phi_c$	$\frac{1}{2}\times(I_3-I_s) < 0$	$I_1<0$	$I_3>0$
	$\phi \ge \phi_c$	$\frac{1}{2}\times(I_{L1b}-I_s) < 0$	$I_{L4b}>0$	$I_{L3b}>0$

In Figure 4.4, the ZVS regions of the output-power curve are shown for Bridge 1. The blue points are in the hard-switching region whereas the red points are in the ZVS region. The term d is the voltage ratio, d = $\frac{NV_2}{V_1}$. In the simulation, the power curves are plotted for a duty ratio (D) of 0.4.

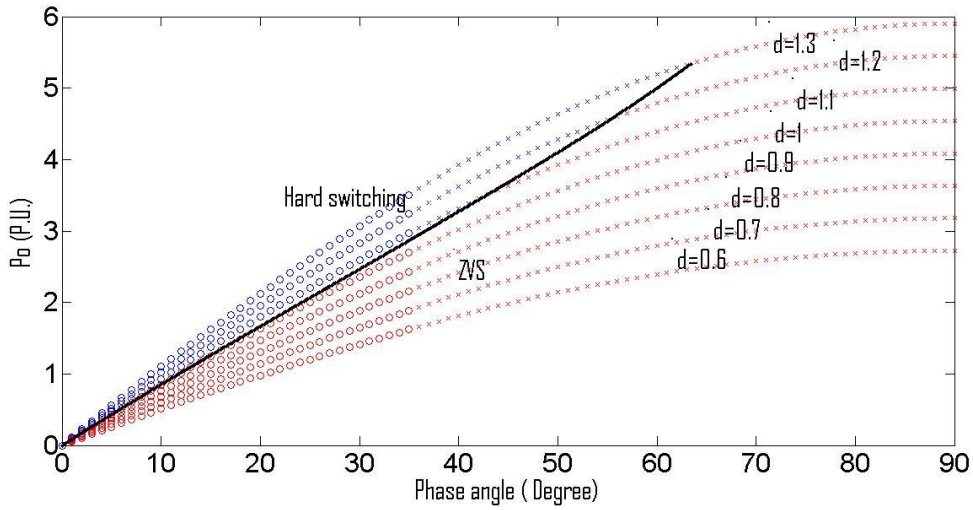


Figure 4.4. Power plots as a function of ∅ for the switches in Bridge 1, with red points in the ZVS region and blue points in the hard-switching region.
(o: $0 < \emptyset < \pi - 2\pi D$, x: $\pi - 2\pi D < \emptyset < \frac{\pi}{2}$), d = NV_2/V_1, $V_b = V_1$, $Z_b = 2\pi wL_s$, D=0.4.

All of the switching devices in Bridge 1 are guaranteed to turn on under ZVS if the flat-top condition is satisfied (d=1). When d is not equal to 1, the slope of the transformer current is not equal to zero, as illustrated in Figure 4.2. For the condition $NV_2 < V_1$ ($d \leq 1$), all switching devices in Bridge 1 can turn on under the ZVS conditions. On the other hand, for the condition $NV_2 > V_1$ ($d>1$), the switching devices in Bridge 1 may turn on under hard-switching. Here, the switching devices in Bridge 1 are represented by S_1-S_4. S_c is neglected since S_c has ZVS for $0.6 < d < 1.3$ in boost mode.

Figure 4.5 and Figure 4.6 show the ZVS regions for Bridge 2 with respect to the power curves. In the figures, the ZVS region for S_5 and S_7 is larger than the ZVS region for S_6 and S_8. As shown in Figure 4.2, S_5 and S_7 turn on with anti-parallel diodes when I_2 is greater than 0. On the other hand, S_6 and S_8 turn on in ZVS when I_1 is greater than 0.

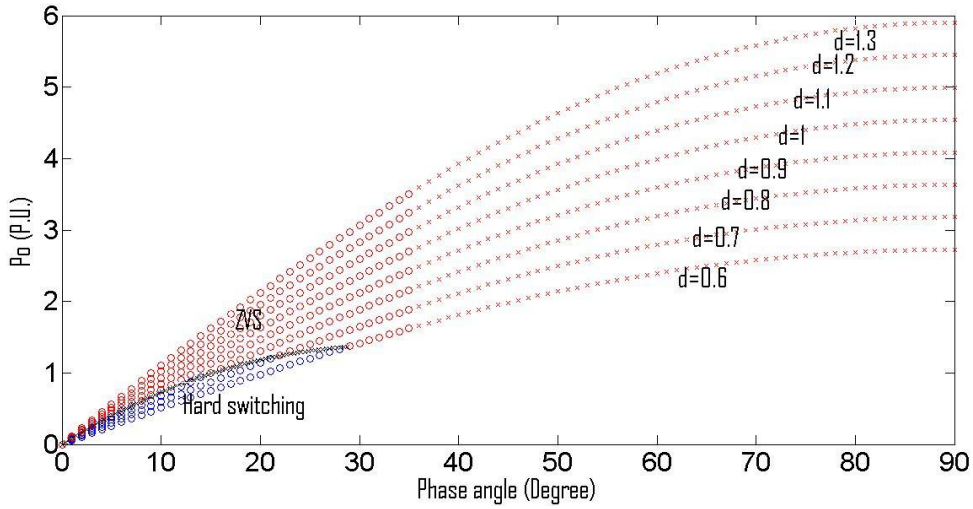


Figure 4.5. Power plots as a function of ∅ (degree) for switches S_5 and S_7, with red points in the ZVS region and blue points in the hard-switching region. (O: $0 < \emptyset < \pi - 2\pi D$, x: $\pi - 2\pi D < \emptyset < \frac{\pi}{2}$), d = NV_2/V_1, $V_b = V_1$, $Z_b = 2\pi wL_s$.

Figure 4.7 and Figure 4.8 specify the ZVS regions of the devices able to realize ZVS. In Figure 4.7, the ZVS regions of the switching devices are plotted on the plane defined by output power and phase-shift angle. In Figure 4.8, the ZVS regions are plotted on the plane defined by the voltage ratio ($d=NV_2/V_1$) and load current (I_o). Region A is the ZVS region common to all switching devices. To operate in region A, the DAB[3] converter must operate with d equal to or slightly greater than one.

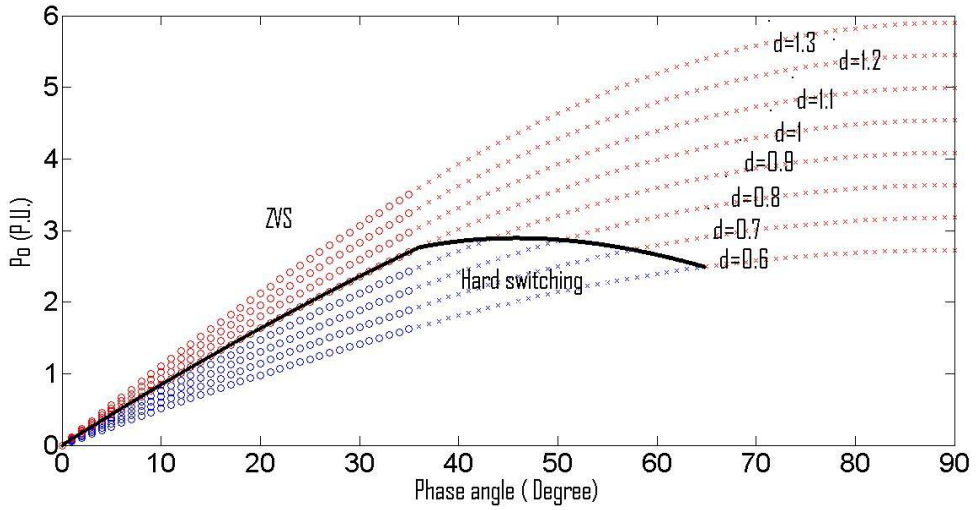


Figure 4.6. Power plots as a function of ∅(degree) for switches S_6 and S_8, with red points in the ZVS region and blue points in the hard-switching region
(O: $0 < \emptyset < \pi - 2\pi D$, x: $\pi - 2\pi D < \emptyset < \frac{\pi}{2}$), d = NV_2/V_1, $V_b = V_1$, $Z_b = 2\pi wL_s$

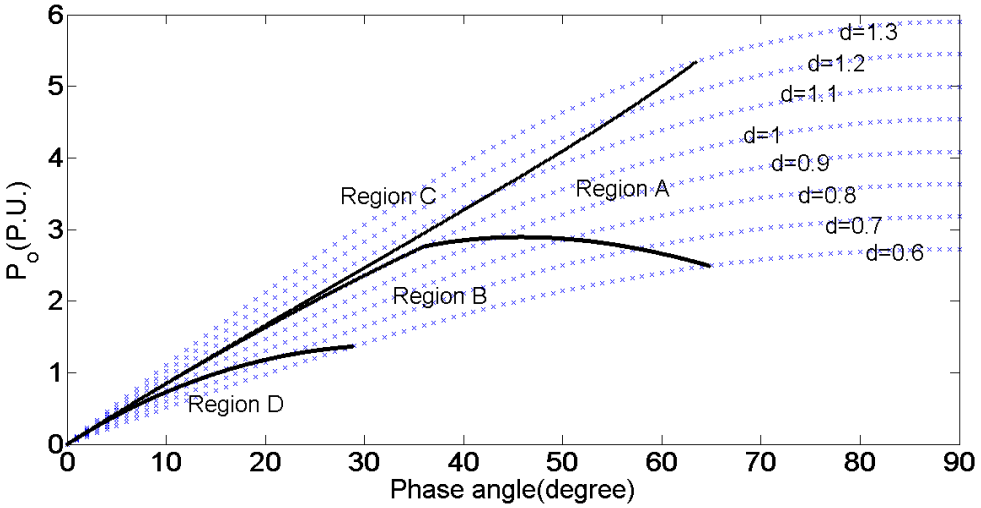


Figure 4.7. The ZVS regions of the DAB[3] converter (P_o v.s. phase angle).
Region A: the ZVS region common to all of the switching devices.
Region B: the ZVS region for the switching devices in Bridge 1 and S_5 and S_7.
Region C: the ZVS region for switching devices S_5-S_8.
Region D: the ZVS region for Bridge 1.
(Blue: $0 < \emptyset < \pi - 2\pi D$, Red: $\pi - 2\pi D < \emptyset < \frac{\pi}{2}$), d = NV_2/V_1, $V_b = V_1$, $Z_b = 2\pi wL_s$

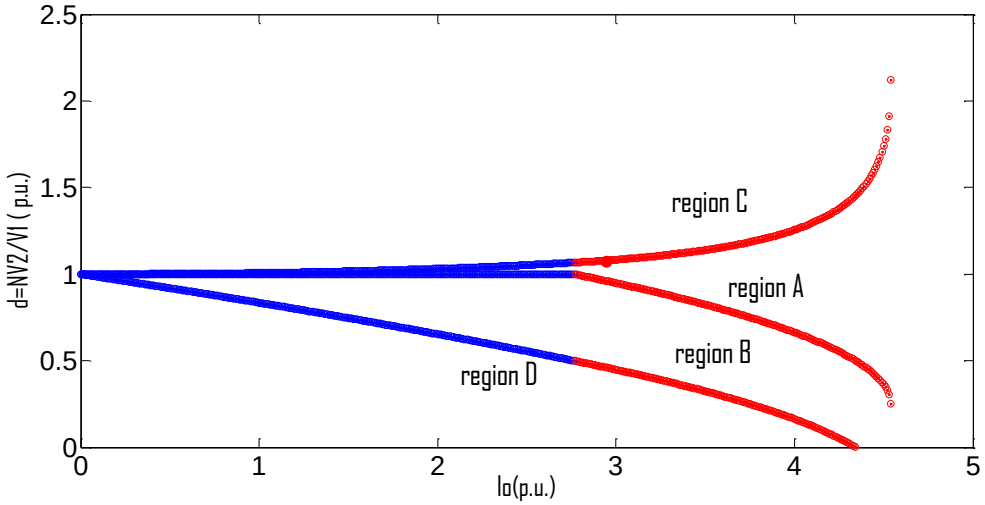
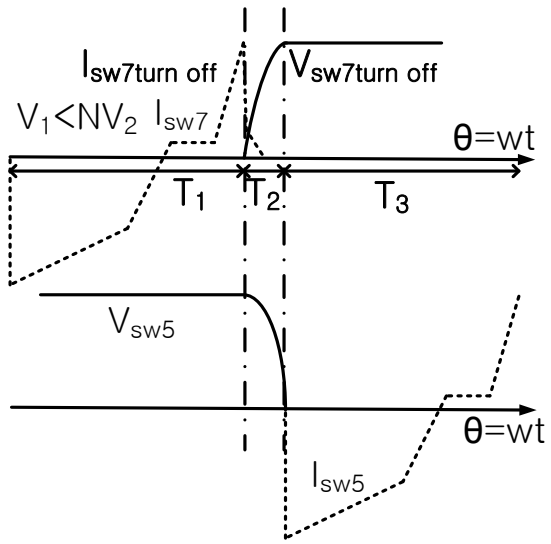


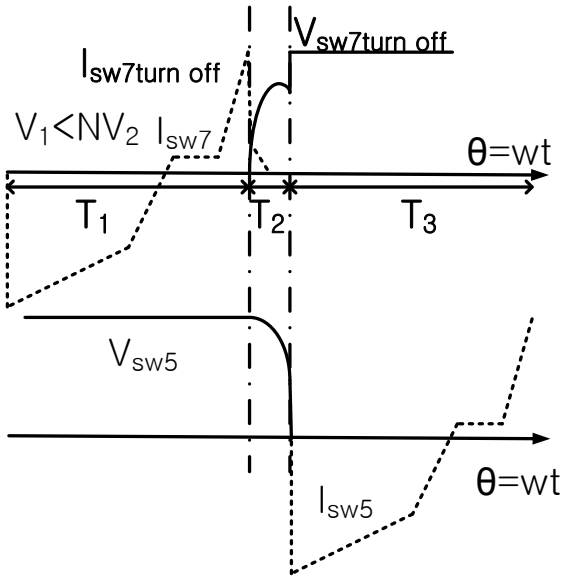
Figure 4.8. The ZVS region of the DAB^3 converter. (d v.s. I_o)
Region A: the ZVS region common for all of the switching devices.
Region B: the ZVS region for the switching devices in Bridge 1 and S_5 and S_7.
Region C: the ZVS region for switching devices S_5-S_8.
Region D: the ZVS region for Bridge 1
(Blue: $0 < \emptyset < \pi - 2\pi D$, Red: $\pi - 2\pi D < \emptyset < \frac{\pi}{2}$), $d = NV_2/V_1$, $V_b = V_1$, $Z_b = 2\pi wL_s$

The completion of ZVS depends on the energy in the reactive components such as inductors and capacitors. Figure 4.9 illustrates the voltages and currents in the switching devices during the switching transitions. The completion of ZVS can be discussed with the resonant pole in Figure 4.10. Figure 4.9(a) shows the waveforms for the completed ZVS, whereas Figure 4.9(b) shows the waveforms for the uncompleted ZVS. When a switching device is under hard switching or uncompleted-ZVS conditions, power loss increases due to the losses of the parasitic or snubber capacitors across the switching device as shown in Figure 4.10. To ensure the completion of ZVS, the energy in the inductor should be sufficient when compared to the energy in the capacitors. In switching intervals, the current from the resonant pole, as shown in Figure 4.9, is calculated to be Equation (35).

$$I_{Ls}=I_p=2C_p\frac{dV_{cp}}{dt} \quad (35)$$



(a) Switching example where the energy in the series inductance is enough to complete the natural ZVS.



(b) Switching example where the energy in the series inductance is not enough to complete the natural ZVS.

Figure 4.9. Switch voltage and current transitions.
(T_1: interval for S_7 conducting, T_2: dead time, T_3: interval for S_5 conducting.)

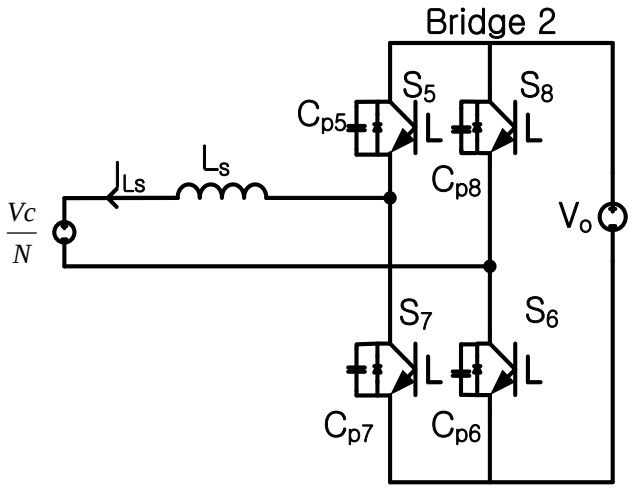


Figure 4.10. A resonant pole in Bridge 2.

The energy stored in the series inductor, $E(L_s)$, is derived in Equation (36). The minimum current required for natural ZVS is derived using Equations (36-38) and shown in Equation (39).

$$E(L_s) = \frac{1}{2} L_s I_{Ls}^2 \tag{36}$$

$$\frac{1}{2} L_s I_{min}^2 = \int_0^{t1} V_i(t) I_{Ls}(t) dt = 2C_p \times \frac{Vc}{N} \times V_o \tag{37}$$

$$I_{L2} = \frac{1}{2\omega L_s} (\pi V_1 + N V_2 (2\emptyset - \pi)) \tag{38}$$

$$I_{min} = 2\sqrt{\frac{C_p}{L_s}} \times \sqrt{\frac{V_c V_o}{N}} \tag{39}$$

Equation (39) shows that the snubber or parasitic capacitance of the switching device, C_p, is related to the minimum current, I_{min} which is required for the completion of ZVS. If I_{min} is normalized by given base uints, $Z_b=\omega L_s$, and $V_b=V_c=V_1$, the minimum

required current in the leakage inductance to complete ZVS in Bridge 2 is given in Equation (40).

$$I_{min}(p.u.)= 2Z_b\sqrt{\frac{C_p}{L_s}} \tag{40}$$

4.3. Parametric Loss Estimation

Since power-electronic converters consist of many non ideal components, power loss occurs in each device. The losses result in heating which can endanger the system's safety and increase the system cost and volume. Hence, designing power converters requires estimating power loss. The power losses are generally classified based on the type of converter component. The main losses in power converters occur from semiconductor switching devices. Power losses also occur in magnetic devices, capacitors, and snubber circuits.

This section estimates the power losses and the volumes of the converter components. The power loss of the devices depends on the operating conditions and parameters, such as the operating frequency and the circuit parameters. The power loss also depends on the design of the components such as volumes of devices and the length of cables. Hence, the converter loss can be examined for various operating conditions and parameters. Component designs for the estimation are based on the conditions in Table 9.

Table 9. Conditions used for the loss estimation. (N=1.5)

V_s	V_c	$d(=NV_2/V_1)$	V_o	Transformer-turns ratio	P_o	R
210 - 270V	300V	0.7~1.3	$V_o = dV_c/N$	3:2(=N:1)	10kW	$(V_o)^2/(P_o)$.

4.3.1. Semiconductor-device loss

In semiconductor switching devices, power loss occurs both as conduction loss and switching loss. The switching loss occurs during the turn-on and-off transitions, which can have a duration of hundreds of nanoseconds to microseconds. The energy loss depends on the voltage and current variations during the turn-on and-off transitions. Since the voltage and current curves of a switching device are dependent on the gate-driving signals, the switching-loss mechanism is generally considered together with the gate-emitter voltage (V_{GE}). Figure 4.11 illustrates the voltages and currents of an IGBT device during the transitions.

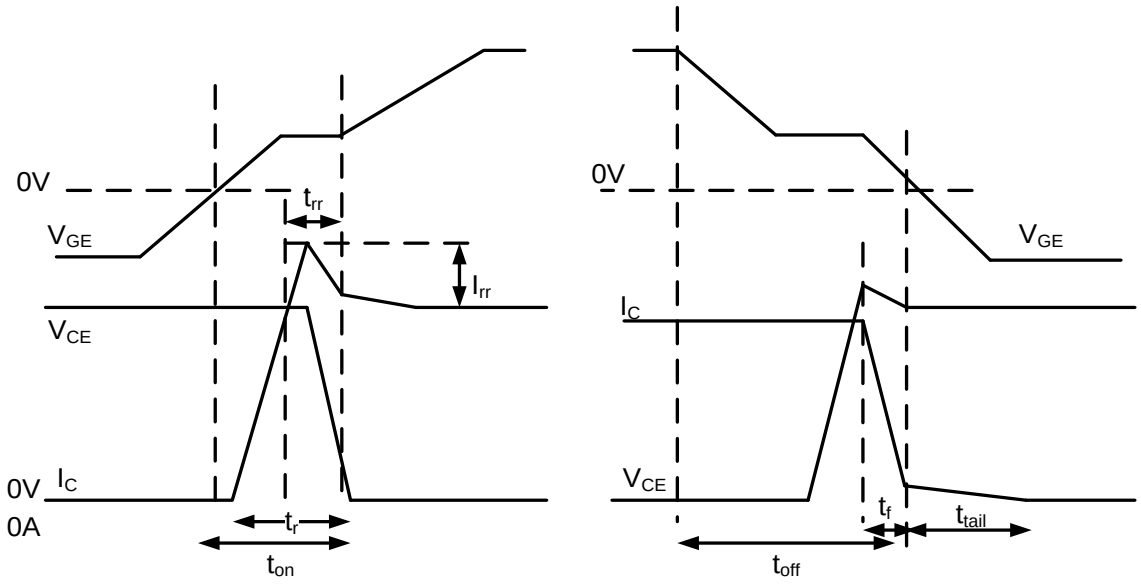


Figure 4.11. Turn on and off transitions of IGBT devices.
(Left) Turn on, (Right) Turn off

The switching loss that occurs in the turn-on transition is represented as $\frac{1}{T_s}\int_{t_s}^{t_s+t_{on}} V_{ce}(t)I_c(t)dt$. As shown in Figure 4.11, the turn-on transition of the switching device is caused by the delay in charging the gate-collector and the gate-emitter

capacitance in the switching process. Switching loss also occurs when the switching device turns off. The illustration on the right of Figure 4.11 shows the turn-off transition of an IGBT device. In the illustration, the slope of the current abruptly decreases during falling time $t_{f.}$ The falling time is required to discharge the gate-to-emitter capacitance to a threshold value. Following the discharge of the gate-to-emitter capacitance, current still flows during the tailing time, t_{tail}, which is caused by a recombination of minority charges in the n- region. The tailing currents cause high turn-off losses in the actual IGBT devices. Reverse-recovery loss of an anti-parallel diode is also categorized as one of the causes of power loss in the IGBT module. The reverse-recovery process is caused by a recombination of excess carriers in the drift region, resulting in significant loss.

In the DAB^3 converter, ZVS is available for the turn-on transition of the switches, whereas the turn-off loss cannot be avoided because of the current-tailing phenomenon for the IGBT devices or reverse-recovery loss for the anti-parallel diodes. Hence, zero turn-on loss is assumed for a soft turn-on of the IGBT device when the anti-parallel diode conducts prior to the IGBT device. The IGBT turn-off is considered hard switching since the snubber capacitors are neglected in the estimation. When d (= NV_2/V_1) does not equal 1, some of the switching devices may turn off with the reverse biasing of anti-parallel diodes.

The classification of an event as a turn-on event or a turn-off event is based on the polarity of the current when the semiconductor device is switching. For example, a positive current in collector to emitter current (I_{ce}) direction at the switching instant is considered IGBT switching. A negative current at the switching instant is considered diode switching. Generally, the manufacturers of power semiconductors provide the data

plots of the switching energy. For the loss estimation, the data from the FUJI 2MBI100TA060A-50 are used. Figure 4.12 shows the turn-on and -off loss (E_{on} and E_{off}) of the IGBT device and the reverse-recovery loss (E_{rr}) of the diode in the FUJI 2MBI100TA060A-50 module.

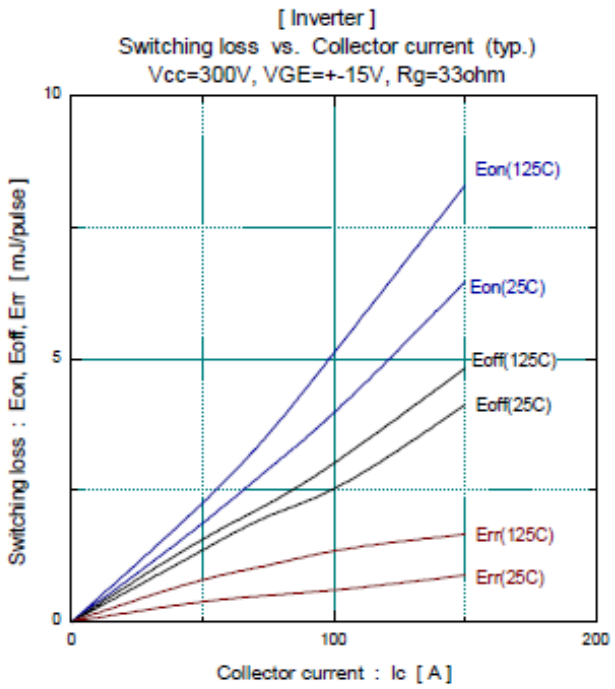


Figure 4.12. Switching loss obtained with 300 V across the device in [26].

The switching loss can be calculated based on the currents and voltages at the switching instant. The analytical values of the switch currents at the switching instant can be derived by the analytical equations of the transformer and filter-inductor currents given in Equations (9)-(24). Figure 4.13 presents the switching-loss estimation process. The energy-loss data in Figure 4.12, is used to proportionally estimate the energy-loss data at other voltage conditions (i.e. E_{on} at 200 V= $2/3E_{on}$ at 300 V). The extended energy-loss data are used to estimate the switching loss at the operating condition of the converter.

Table 10 defines the types of switching loss for current polarities. When the turn-on current is negative, the turn-on loss is neglected. When the turn-on current is positive, the turn-on loss is a non-zero value obtained from the E_{on} data. When the turn-off current is positive, E_{off} data from Figure 4.12 are used. When the turn-off current is negative, E_{rr} data in Figure 4.12 are used.

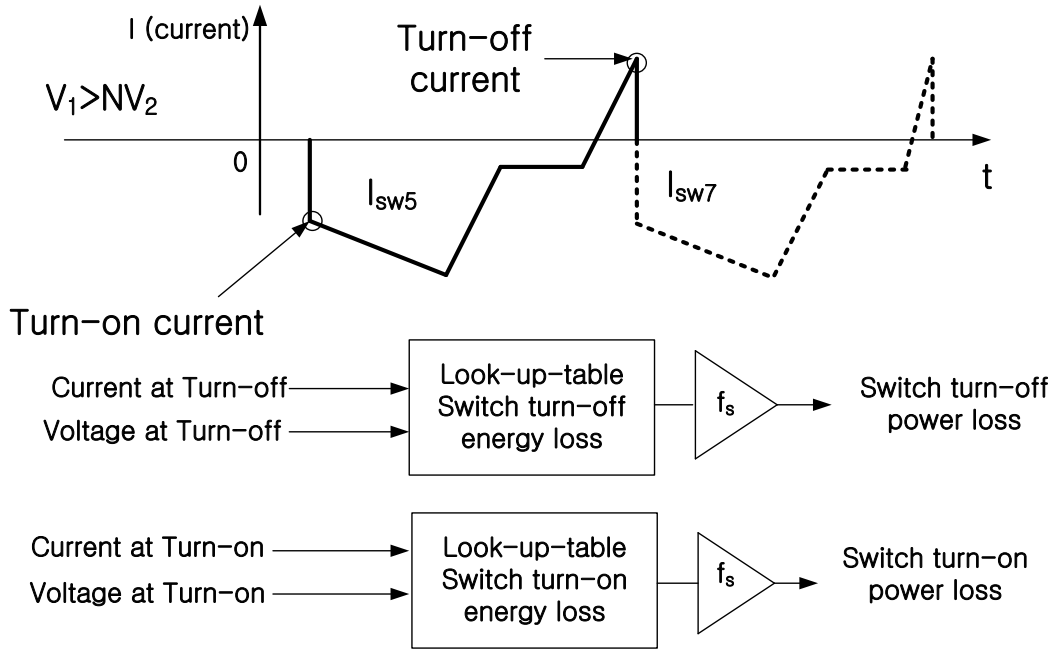


Figure 4.13. Block diagram of the switching-loss estimation process.

Table 10. Definition of switching loss for current polarity.

	At turn-on	**At turn-off**
I > 0	E_{on} by hard switching	E_{off} by hard switching
I < 0	ZVS (energy loss=0)	E_{rr} by reverse biasing of diode

The conduction loss of the semiconductor device is also a significant factor in semiconductor loss. The conduction loss of the IGBT device is caused by effective

channel resistance. The channel resistance of the anti-parallel diode has different characteristics from the IGBT's. Hence, the parameters for both the IGBT and for the anti-parallel diode should be obtained.

The parameters (R_{on}, V_{ce_on}) for the IGBT can be extracted from Figure 4.14, while the parameters (R_D, V_{d_on}) for the anti-parallel diode can be extracted from Figure 4.15. The non-linear curves can be approximated as piecewise-linear equations (41), (42) on the operating point.

$$V_{ce} = R_{on} \times i_{ce} + V_{ce\_on} \tag{41}$$

$$V_F = R_D \times i_{ec} + V_{d\_on} \tag{42}$$

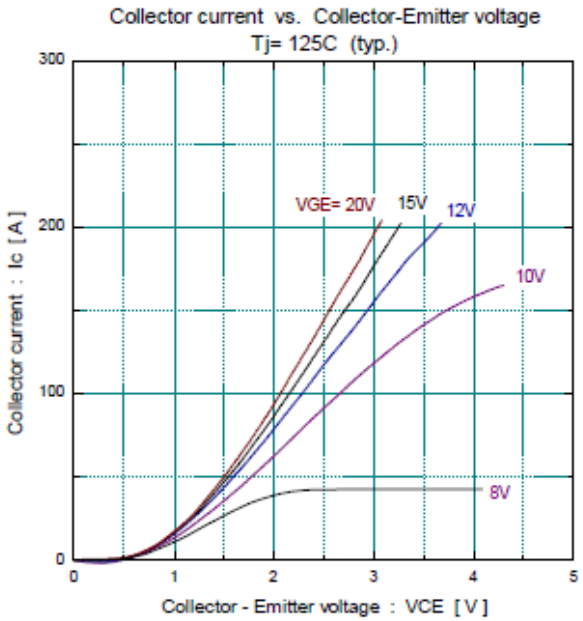


Figure 4.14. Collector current vs. collector-emitter voltage in [26].

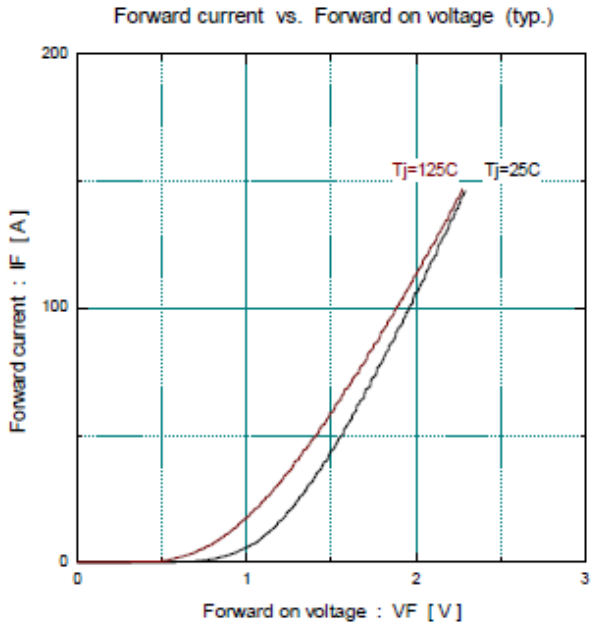


Figure 4.15. Forward current (I_F) vs. forward voltage (V_F) of the anti-parallel diode in [26].

Figure 4.16 illustrates the conduction-loss switch model of an IGBT module. The model uses ideal diodes and an ideal switch. Ideal diodes and switches selectively pass currents so current flows only in the desired direction. Figure 4.17 illustrates a current waveform flowing in the S_5-D_5 IGBT module. When the switching device is turned on under ZVS conditions, the current initially flow in the anti-parallel diode. As the direction of the current is reversed, the current starts to flow in the IGBT device.

The conduction loss of the S_5-D_5 IGBT module can be estimated by Equation (43), which is derived using the conduction-loss switch model of the IGBT module. Since the conduction-loss model consists of the voltage source and resistances, Equation (43) is simplified using Equations (41) and (42) so conduction loss is based on RMS and average currents.

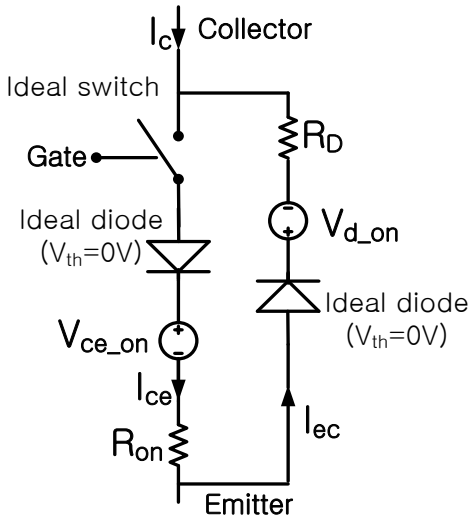


Figure 4.16. Conduction-loss model of an IGBT module.

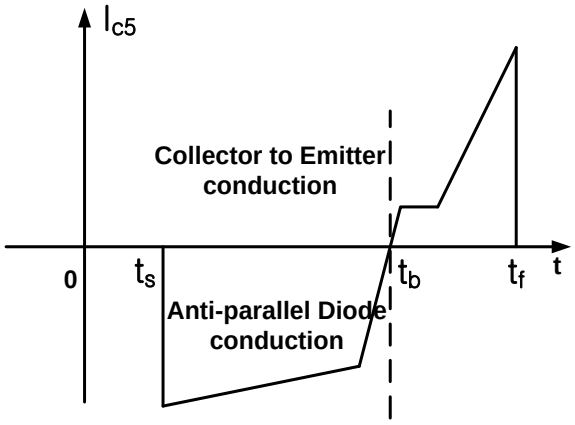


Figure 4.17. Illustration of the current in the S_5-D_5 module of the DAB[3] converter.

$$\text{Conduction loss in } S_5D_5 = \frac{1}{T_s}\int_{nT_s}^{(n+1)T_s}(i_{c5}(t)\times V_{ce5}(t))dt$$

$$= i_{ec5\_RMS}^2 \times R_D + \frac{V_D}{T_s}\int_{nT_s+t_s}^{nT_s+t_b}|i_{ec5}(t)|dt + i_{ce5\_RMS}^2 \times R_{on}$$

$$+ \frac{V_{ce\_on}}{T_s}\int_{nT_s+t_b}^{nT_s+t_f}|(i_{ce5}(t)|)dt \qquad (43)$$

As shown in Chapter 3, the main advantage of maintaining flat-top currents in the transformer is minimization of TDR. Another benefit of flat-top currents is low power loss of the switching devices. Figure 4.18 shows the estimated switching and conduction losses of the switching devices.

The power losses are plotted as a function of a normalized output voltage, d = $\frac{NV_2}{V_1}$. As the value of d deviates from 1, the slope of the transformer current becomes high. Hence, some of the switching devices experience ZVS, while other devices experience hard-switching. When d equals 1, the slope of the transformer current is set to zero and the converter has minimum-device stresses and switching loss in a ZVS condition

The snubber losses are not included in the switch-loss estimation because switching devices are assumed to have no snubber capacitors. For values of d less than 1, the switching devices of S_6 and S_8 turn-on with hard switching. For values of d greater than 1, S_1 - S_4 turn on with hard switching. Hence, in Figure 4.18, the slope of the switching loss curve for d>1 is higher than the slope for d < 1. In summary, keeping the condition, d=1, presents advantages with respect to both the power loss and the total-device ratings.

In Figure 4.19 and Figure 4.20, the switching device losses are plotted as a function of switching frequency, with the flat-top condition satisfied. The plot in Figure 4.19 is for the duty ratio D = 0.35, while the plot in Figure 4.20 is for D = 0.45. As the switching frequency varies from 15 kHz to 45 kHz, the switching loss increases proportionally to the frequency. Since, the conduction loss is independent of the switching frequency, the total-semiconductor-device loss increases as the switching frequency increases.

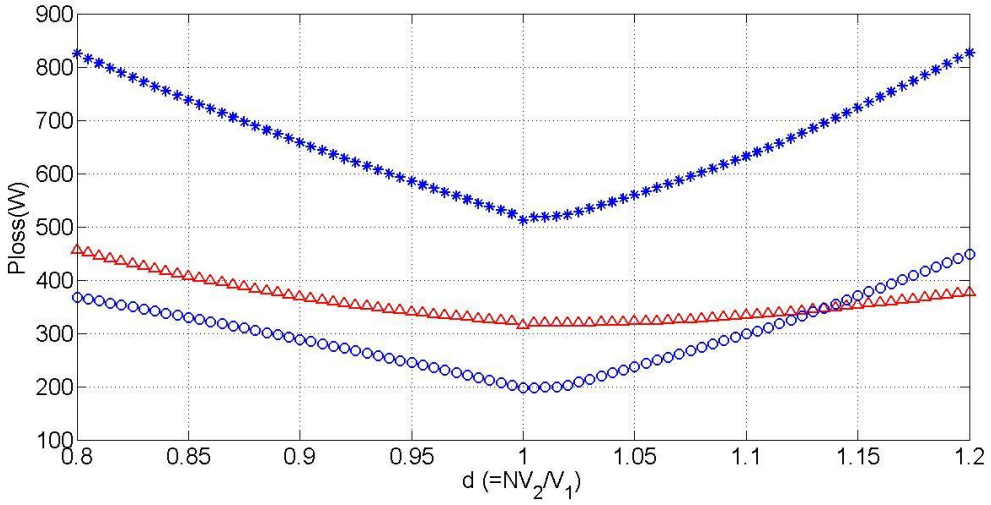


Figure 4.18. Estimated power loss in the switching devices as a function of d, where o represents switching loss. Δ represents conduction loss, and * represents total-semiconductor device loss. P_o=10kW, D(duty ratio)=0.35, (d = $\frac{NV_2}{V_1}$), switching frequency (f_s) = 35 kH_z V_1=300 V, N = 1.5.

The power loss from the switching devices appears as heat. Heat-management devices are generally used to ensure the temperatures of the power semiconductors are below the maximum-temperature ratings. The power stage heatsink occupies a large portion of the overall volume. Therefore, low semiconductor loss is required to reduce volume. Figure 4.19 shows the estimated junction temperature between the semiconductor module and the heatsink. A heatsink thermal resistance of 0.08℃/W with forced convection is assumed for the estimation. The maximum temperature rating of junction of the IGBT device is 150℃. In Figure 4.19, the estimated junction temperature is less than 150℃ for the given frequency ranges. Hence, a smaller heatsink may be used for the optimal design. In this estimation, the volume of the heatsink which is used for the estimation is $4.78 \times 9.5 \times 5.25$ ($inch^3$) (=3906.7 cm^3). Decreasing the switching frequency can reduce the volume of the heatsink, but this would increase the volume of

magnetic devices. Hence, there is a trade-off between the switching frequency and volume of the power converter.

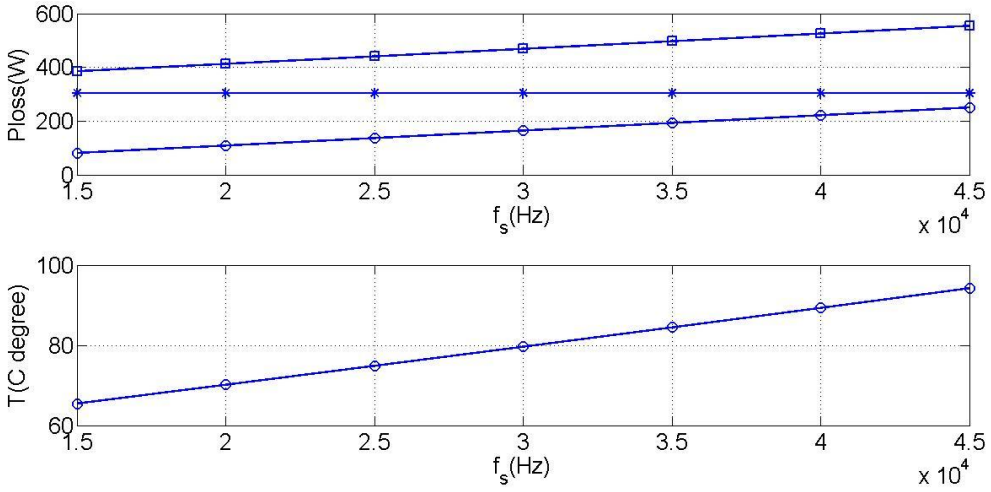


Figure 4.19. Estimated power loss and junction temperature of switching devices when d = NV_1/V_2, D = 0.35, P_o=10 kW, V_1 = 300 V,V_2 = 200 V, N = 1.5.
(upper) *: conduction loss, o:switching loss, □: total-semiconductor device loss , (lower) Estimated-junction temperature.

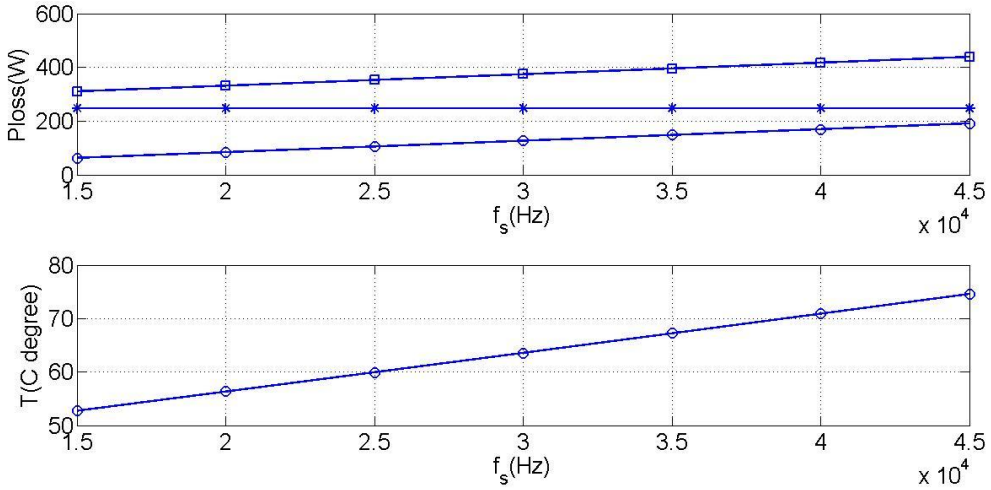
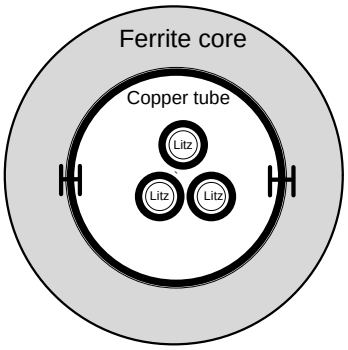


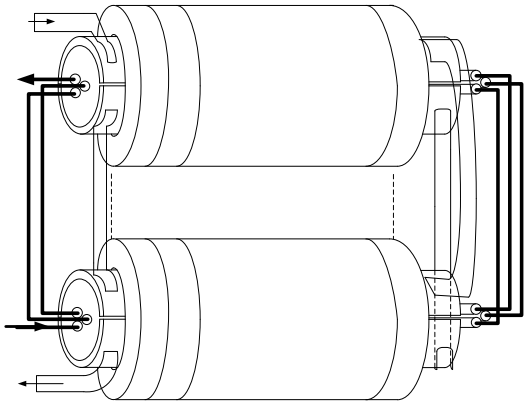
Figure 4.20. Estimated power loss and junction temperature of the switching devices when d = NV_1/V_2 = 1, D = 0.45.
(upper) *: Conduction loss, o: Switching loss, □: total-semiconductor device loss, (lower) Estimated junction temperature

4.3.2. Power-loss estimation of the transformer

A coaxial high-frequency transformer has been proposed for high-frequency power-electronic applications [27-29]. The coaxial transformer is known to have a controllable leakage inductance, a uniform-leakage field, and high efficiency. In the power loss estimation of the DAB^3 converter, the coaxial transformer is considered, and is estimated in efficiency, and its volume is presented. Figure 4.21 shows the coaxial transformer used for the estimation. The transformer is designed to have turns ratio of 3 to 2.



(a) An axial view.



(b) A side view.

Figure 4.21. Coaxial transformer.

The inner windings are realized by three turns of Litz wires. The outer windings for the secondary side are built with copper tubes. The two turns are implemented by splitting the copper tube into two segments. The magnetic core is made by stacking multiple toroidal-ferrite cores to ensure the required cross-sectional area for the operating flux density. The dimensions of the unit core, wire gauge, and dimensions of the copper tube are predetermined in order to decrease the degrees of freedom in the estimation. Table 11 shows the components that are used for the power loss and volume estimation of the coaxial transformer.

Table 11. Components for the coaxial transformer.

Component	Part information	Manufacturer	Description
Core material	44932TC (F-perm)	Mag-Inc	Toroidal ferrite
Inner winding	N32-30E+00003-0 Type 2 Litz	New England Wire Technologies	Litz cable
Outer winding	Copper tube		Width = 1.57×skin depth
Insulation 1	0.020" PFA JACKET TO 0.213"+0.007"/-0.014" OD TRANSLUCENT		PFA
Insulation 2	Polyolefin, 7864K28	N/A	Heat-shrink tube

In the power-loss estimation, the design of the transformer is changed to reflect the effect of switching frequency. For a given switching frequency, multiple designs of the transformer are performed for different values of the maximum-flux density (B_m). The resulting designs have different volumes of the magnetic cores and different core losses. The design which causes the minimum loss at a given frequency is finally chosen for the estimation.

The power losses in the magnetic devices are generally explained by core and copper losses. The core loss occurs in the magnetic-core materials, while the copper loss

occurs in the winding conductors. The core loss is explained by hysteresis loss and eddy-current loss.

In a B-H characteristic of a magnetic material, energy loss is represented as the area inside the B-H loop, which is shown in Figure 4.22.

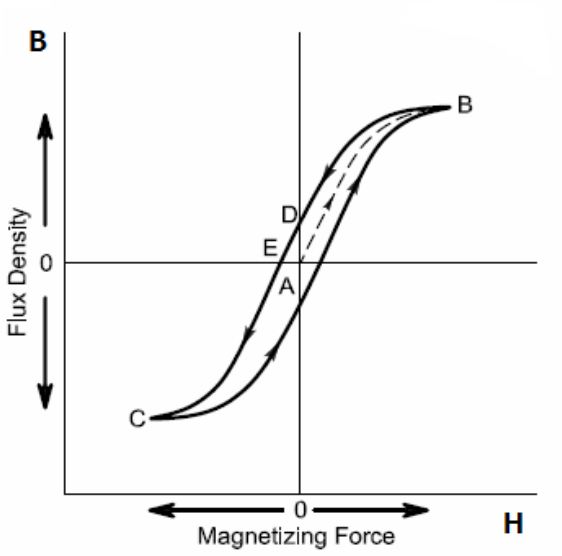


Figure 4.22. B-H characteristics of magnetic-core material.

Let's consider a ferromagnetic core with coil windings, which is excited by an ac source. To reverse the magnetic flux in a ferromagnetic material periodically, energy is required in this process. A fraction of this energy is dissipated as heat, and the rest of the energy is returned to the coil and to the ac source. The resulting power equation can be simplified as shown in Equation (44).

$$P_H = (f)(A_c l_m) \int_{\text{one cycle}} HdB \text{ (W)} \tag{44}$$

where

P_H: Hysteresis loss (W)

B: Magnetic-flux density (Tesla)

f: Operating frequency (H_z)

A_c: Cross sectional area (m)

l_m: Length of the core (m).

Another cause of core loss is eddy-current loss. When an ac magnetic field flows through a magnetic material, electrical-eddy currents flow in the magnetic material. The illustration in Figure 4.23 shows how the eddy current flows in a magnetic material. Eddy currents are induced to oppose the time-varying flux. The eddy currents and the resistance of the magnetic material cause I^2R loss. Hence, a core loss (P_{core}) includes both hysteresis (P_H) and eddy-current loss (P_{eddy}).

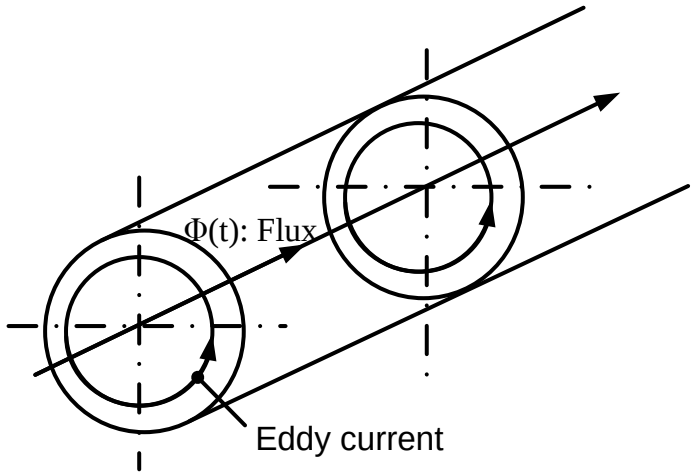


Figure 4.23. Eddy currents in core material.

Core manufacturers provide data sheets quantifying the core loss. Core loss can also be expressed by the Steinmetz's equation, shown in Equation (45). The parameters of the equation can be fitted by the experimental-data plots of manufacturers. For the estimation, Equation (45) is fitted to the core-loss curve of the F-perm material of Mag-Inc., which is described in Appendix A.

$$P_{fe} = K_{fe}(\Delta B)^{\beta} A_c \ell_m \text{ (W)}, \tag{45}$$

where

ΔB: Ripple of magnetic flux density (T)

A_c: Cross sectional area that is linked by flux (m^2)

ℓ_m: Core length (m).

The transformer can be designed by Faraday's law using square-wave excitation, as described in Equation (46). From this equation, it can be known that B_m, A_c and f_s can be free variables for fixed values of V_{rms} and N. In the estimation, the transformer design is optimized at each switching frequency by varying the free variables, B_m and A_c, parametrically.

$$V_{rms}=4NB_mA_cf, \tag{46}$$

where

N: Number of turns

B_m: Maximum value of magnetic-flux density (Tesla)

A_c: Total cross-sectional area that is linked by flux (m^2)

f : Operating frequency (H_z).

Another loss factor in the magnetic device is copper loss. High-frequency currents increase the ac resistance, since the current is redistributed by the skin and proximity effects. Hence, the conductors in which high-frequency currents flow experience significant copper losses. The current distribution in a copper tube can be derived from Equations (47)-(50), which is known as Bessel's differential equation of order of zero and which has been previously solved for the coaxial transformer in [27, 28, 30]. In Equation (47), J_z is the current density in a cylindrical coordinate, and r is the radial distance from the axis of symmetry.

For a copper tube split into N segments, the approximated solution for the power loss is given in Equations (49) and (50).

$$\frac{d^2 J_z}{dr^2} + \frac{1}{r}\frac{dJ_z}{dr} - j\frac{w\mu^2}{\rho} J_z = 0 \tag{47}$$

$$J_z = CI_0\left[\frac{\sqrt{2}r}{\delta} e^{\frac{j\pi}{4}}\right] + DK_0\left[\frac{\sqrt{2}r}{\delta} e^{\frac{j\pi}{4}}\right] \tag{48}$$

$$P_{ave} = \frac{1}{2}\int_{r_i}^{r_o}\int_{0}^{2\pi} |J_z(r)|^2 \rho r d\theta dr [w/m] \tag{49}$$

$$P_{ave} \approx \frac{N^2\rho\pi}{2\mu_0^2\delta}\left[\left(r_i B_i^2 + r_o B_o^2\right)F_1(R) - \left(4B_o B_i\sqrt{r_i r_o}\right)F_2(R)\right][w/m] \quad (50)$$

N= Number of segments

r_i = Tube inner radius, r_o= Tube outer radius

$R = \frac{(r_o - r_i)}{\delta}$, δ= Skin depth= $\sqrt{\frac{\rho}{\mu_0 \pi f_s}}$

ρ = 1.7× 10-7, $\mu_0 = 4\pi \times 10^{-7}$, f_s = Switching frequency (Hz)

$B_i = \frac{\mu_o I_{net\_i}}{2\pi r_i}$, $B_o = \frac{\mu_o I_{net\_o}}{2\pi r_o}$

I_{net_i} = Net RMS current enclosed by the circle at r_i

I_{net_o} = Net RMS current enclosed by the circle at r_o

$F_1(x) = \frac{\sinh(2x)+\sin(2x)}{\cosh(2x)-\cos(2x)}$, $F_2(x) = \frac{\sinh(x)\cos(x)+\cosh(x)\sin(x)}{\cosh(2x)-\cos(2x)}$

The minimum average power loss, P_{ave} in Equation (49) is found by solving $\frac{\partial P_{ave}}{\partial R} = 0$. The solution of the differential equation is found at $R = \frac{\pi}{2}$, which results in the tube thickness, (r_o-r_i)= 1.57δ. When the outer winding is realized by a single tube, the solution shows that the power loss in the copper tube is determined by the thickness. Splitting the tube into two segments does not change the field distribution. Therefore, the power loss increases by N^2 (number of segments) times of the non-split structure, as shown in Equation (50).

The inner windings are implemented by Litz wires. The multiple strands of Litz wires have a negligible impact on the proximity effect. When the current is uniformly distributed in the cables, which have multiple strands, and the strands have a much smaller diameter than skin depth, the current distribution is similar to the distribution in dc currents. The dc-current distribution in the Litz wires will result in greatly reduced ac resistance. The ac resistance of Litz wires is formulated in the manufacturer's datasheet [31]. Equation (51) describes the copper loss in the Litz wires.

$$P_{litz} = R_{ac\_litz}^{2} I_{rms} \tag{51}$$

The power loss in the coaxial transformer has been described and formulated through Equations (47)-(51). The loss estimation is based on these equations. The design that gives the maximum efficiency was chosen for a switching frequency. The power losses and volumes are given in Figure 4.24 over given frequency ranges.

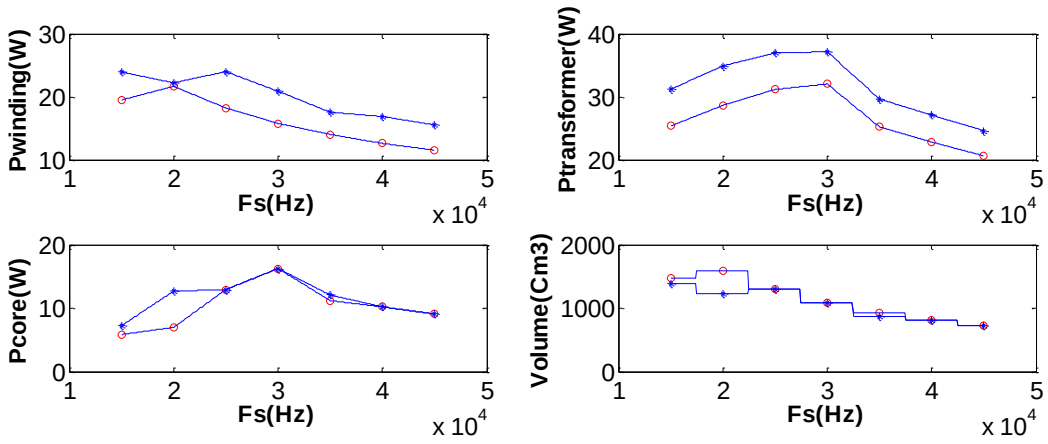


Figure 4.24. Winding losses, core losses, total transformer losses and volume vs. switching frequency for a transformer designed for the minimum power loss. (o) D=0.45, (*) D=0.35.

As the switching frequency increases, the volume of the maximum-efficiency design decreases as the length of the coaxial stack decreases. If the number of winding turns is kept constant, the required winding length also decreases as the switching frequency increases. While the estimation includes the skin and proximity effects, the increased losses of high-frequency excitation are outweighed by the decreased losses due to geometry changes. If the geometry of the transformer is fixed, the copper loss should be monotonic to the operating frequency.

Since the core and copper losses will increase the temperature of the magnetic components, more accurate designs should take into consideration thermal issues, especially if volume-density maximization is to be accounted for. As the temperature increases, the saturation level of the magnetic-flux density (B_{sat}) has a tendency to decrease. Hence, the geometry should be changed, or the heat should be managed by additional equipment. However, a heat analysis is not included.

4.3.3. Power loss of the dc inductor

The loss characteristics in the dc-filter inductor are similar to the loss characteristics in transformer. Losses occur in the core and copper materials. The core loss in the dc inductor is modeled in the same way as the coaxial transformer.

For the dc-inductor design, a ferrite core (EI type, PC40 material) manufactured by TDK is assumed. The wire for the winding is N32-30E+00003-0 Type 2 Litz, which is manufactured by New England Wire Technologies. Figure 4.25 shows the structure of the dc inductor, which is used here for loss and volume estimations.

The dc inductor requires high inductance with many winding turns. Since large (Litz wires in AWG#8) cables are required to meet the current ratings (30-40 A), obtaining sufficient window area is difficult using commercially available products. To reduce the degree of freedom, the geometry of the EI core (EI705019) is selected, and the number of pieces of the core, winding turns, and switching frequency are set as free variables. Furthermore, in this estimation, the dc-current ripple is set to have less than 30 % of the average current. 30 % of the inductor's ripple current is obtained by L_f = 50 uH when the source voltage (V_s) = 270 V.

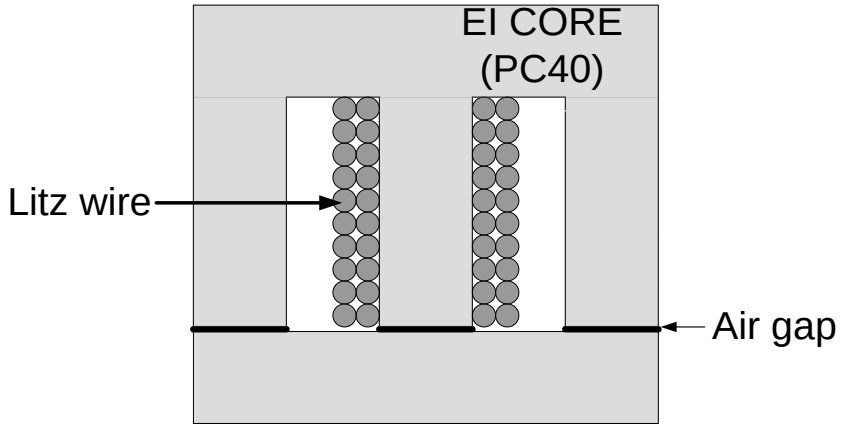


Figure 4.25. A dc-filter inductor.

From Equations (52) and (53), the required cross-sectional area is determined based on the given inductance, voltage, operating frequency, duty ratio, and the ripple of flux density.

$$L_f = \frac{N^2 \mu_0 A_c}{2 l_g} \text{ (H)} \tag{52}$$

$$A_c = \frac{V}{N \Delta B f_{ind} D} \text{ (Cross sectional are : } m^2\text{)}, \tag{53}$$

where

N= Number of winding turns

ΔB= ac flux density (Tesla)

$f_{ind} = 2f_s$= operating frequency on the dc-filter inductor (H_z)

D = Duty ratio

l_g = Air-gap length (m)

In the design, the maximum-flux density, which is represented as $B_{max} = \Delta B + B_{average,}$ should not exceed the saturation level (B_{sat} = 0.4 T, PC40 core). At each switching frequency (f_s = 15k, 20k, 25k, 30k, 35k, 40k Hz), multiple designs were performed, and the design which have minimal loss was searched parametrically. Winding turns (N), cross-sectional areas, and switching frequencies were varied in the design process. Since the core loss has nonlinear characteristics, as depicted in Equation (45), the parameters for Steinmetz' equation, Equation (45) should be fitted for each frequency.

The dc-inductor losses and volumes are plotted in Figure 4.26. The operating frequency of the dc inductor is double the switching frequency of the converter. As the switching frequency increases, the volume of the core can be decreased to achieve minimum losses. As the switching frequency increases, the total loss in the dc inductor decreases.

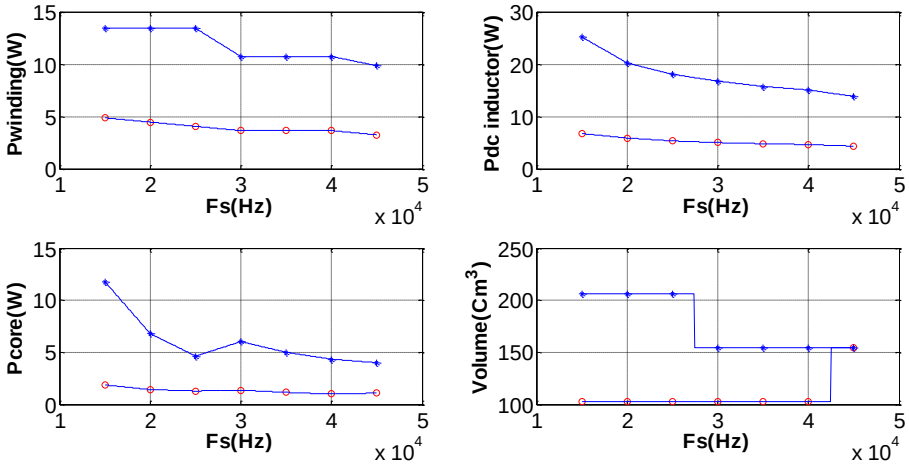


Figure 4.26. Winding loss, core loss, total dc inductor loss, and volume for a dc inductor designed for the minimum loss.

4.3.4. Loss and volume of the power stage

The load voltage is filtered by dc capacitors. In the capacitor banks, power loss occurs due to the equivalent-series resistance (ESR) of the electrolytic capacitors. In the DAB[3] switching, the transformer voltage, V_{r2} which is seen on the Bridge 2 side, is set to zero to vary the duty ratio (D). During the time interval in which the level of V_{r2} is zero, the output capacitors supply the load currents. Hence, the output-filter capacitor (C_o) requires high RMS current-ripple ratings. Electrolytic capacitors can be used to realize current requirements. The required current-ripple rating in the rated condition, which is shown in Table 9, is estimated to be 33 A_{RMS}. Five electrolytic capacitors, which are manufactured by Vishay 26222E3, are used in the estimation. The resulting capacitance is 11mF. Maximum-power loss due to capacitor ESR is estimated to be 13 W. The volume of the capacitor bank is 1742 cm^3 (= 5× 348.4 cm^3).

The power loss in the power stage occurs in the switching devices, transformers, dc inductors, clamp capacitors, and capacitor banks. The system loss and the volume of the power stage are estimated in Figure 4.27. As discussed in this chapter, semiconductor

losses are dominant in the DAB[3] converter. The second dominant cause is from transformer loss. The loss from the DC inductor and the capacitor bank makes the rest of the sources of a power loss.

The volume of the power stage is calculated based on the design for the minimal power loss. However, the volume of some components, such as the heat sink, is not optimized. Hence, the result cannot accurately show the impact of the switching frequency on the volume. The heatsink used in the estimation is large enough to cover all frequencies from 15 kHz to 45 kHz. Hence, the volume of the power stage, as shown in Figure 4.27, decreases as the switching frequency increases. If the switching frequency increases beyond 45 kHz, the heat sink, which is required, must have lower thermal resistance.

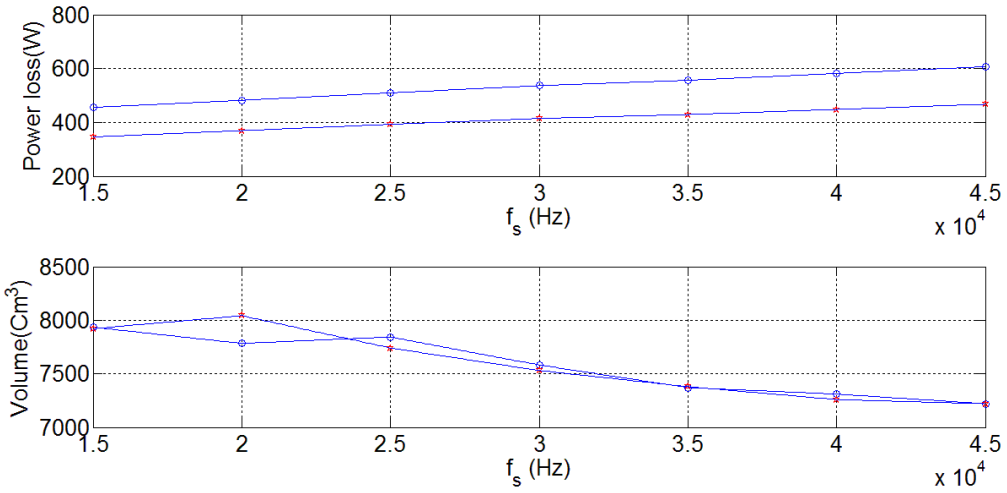


Figure 4.27. Total-power loss and total volumes for a 10kW power stage. (top) Power loss of magnetic devices, (bottom) volume vs. switching frequency in the minimum-loss designs. (* is power loss with D=0.45, o is power loss with D=0.35.)

4.4. Chapter Summary

Section 4.2 analyzed the conditions of ZVS using power-transfer plots. ZVS occurs in limited regions. The ZVS region of switching devices, both in Bridge 1 and Bridge 2, is a subset of the entire power-transfer region. In most of the regions, only a fraction of the switching devices can be turned on under ZVS conditions. This means that the condition, $V_c = NV_{o,}$ is required to be maintained over the operating conditions.

In Section 4.3, the power losses and volumes of the converter are estimated for the selected components. With d = 1, the power loss in the switching device becomes minimal. This result, along with the ZVS regions plotted in Section 4.3, allow us to conclude that the DAB^3 converter should be operated at d = 1.

For future research, optimal design of the heatsink should be considered. If high power density is required for automotive applications, the heat sink should be designed based on an accurate understanding of semiconductor losses since the heat sink occupies more volume than any other component. Also, magnetic components should be designed in consideration of thermal properties if the power density optimization is pursued.

CHAPTER 5

SMALL-SIGNAL MODEL

5.1. Introduction

In this chapter, a small-signal model of the DAB^3 converter is developed. The small-signal model presents information about the poles and zeros of the system at a quiescent operating point. By converting the small-signal model from the time domain to the frequency domain, the stability and dynamic characteristics can be analyzed.

Figure 5.1 shows an inductor-current waveform of a dc/dc converter operated with PWM signals. The current waveform consists of a high-frequency component and a low-frequency component, which are seen as the actual waveform and averaged waveform in the figure. The objective of ac modeling is to predict the low-frequency component.

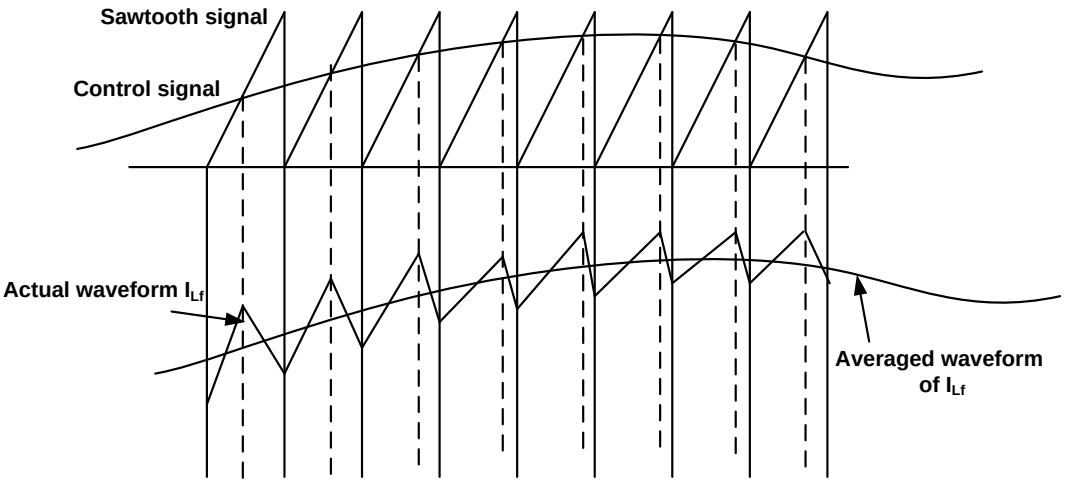


Figure 5.1. AC variations of the converter signals.

Generally, a two-step procedure is required to develop the small-signal model [32]. The first step is to develop state equations by averaging the state variables for a switching cycle. Inductor currents and capacitor voltages are typically selected as state variables. The next step is to linearize the state equations at a quiescent operating point. Averaging over a switching period removes the high-frequency switching ripples. When the moving-average method is applied to the state variables, such as the capacitor voltages and inductor currents, Equations (54) and (55) are be obtained.

$$L\frac{d<i_L(t)>_{T_s}}{dt} = \frac{1}{T_s}\int_t^{t+T_s} V_L(t)dt = < v_L(t) >_{T_s} \tag{54}$$

$$C\frac{d<V_c(t)>_{T_s}}{dt} = \frac{1}{T_s}\int_t^{t+T_s} i_c(t)dt = < i_c(t) >_{T_s} \tag{55}$$

As a first step, the state variables are averaged over a switching period. In Equation (54), $< i_L(t) >_{T_s}$ denotes the average value of $i_L(t)$ over a switching period T_s. The integration of the state variable $i_L(t)$ produces the product of two quantities, the time-varying current ($V_L(t)$) and the time interval (dt). Hence, the output of Equation (54) is a nonlinear quantity. Equation (55) maps $V_c(t)$ to $<V_c(t)>_{T_s}$ with the same procedure that was used to generate Equation (54).

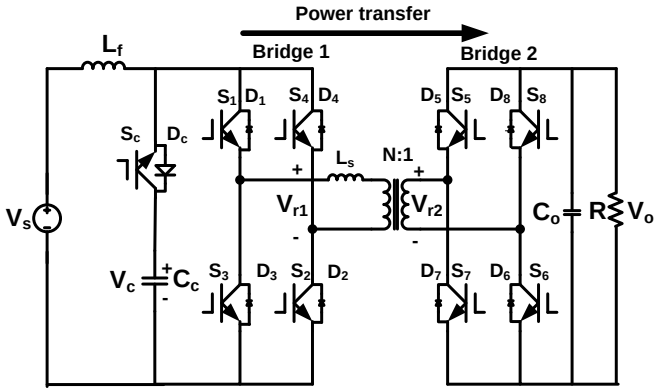
As a second step, the nonlinear quantities are linearized at an operating point using Tailor-series expansion. Linear equations appropriate for small-signal modeling are obtained by neglecting the dc, second-order and higher-order terms.

In this chapter, a small-signal model for the DAB^3 converter is developed for the boost and buck modes. In the boost mode, power flows from Bridge 1 to Bridge 2. In the buck mode, power flows from Bridge 2 to Bridge 1. Since the system dynamics are

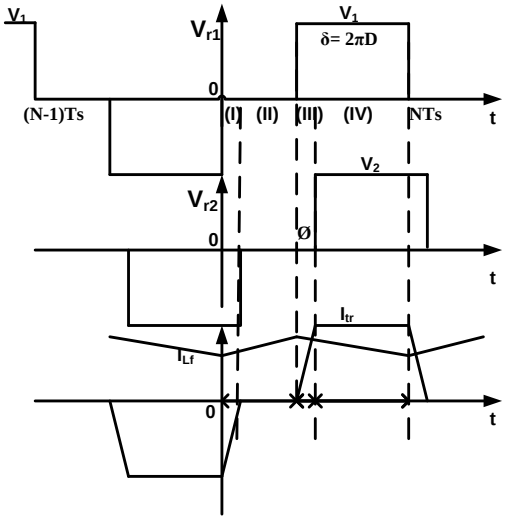
different for each direction of power flow, small-signal models are derived for both the boost and buck modes. Finally, the transfer functions are presented and analyzed in bode plots.

5.2. Small-Signal Model of Boost Mode

The DAB^3 converter has several reactive components as shown in Figure 5.2(a). The power stage can be analyzed with respect to these reactive components using circuit analysis.



(a) Schematic of the DAB^3 converter



(b) Voltages and currents for the subintervals of (I)~(IV).

Figure 5.2. DAB^3 converter and important waveforms in boost mode.

The linear equations related to the reactive components are developed in terms of the selected state variables, i_{Lf}, V_c, $i_{Ls,}$ and $V_{o.}$ Figure 5.2(b) shows the ideal waveform of the transformer voltages and current, and the equations for the transformer current are derived in Section 3.2. For the subintervals from (I) to (IV) shown in Figure 5.2(b), the state equations are described in matrix forms (56)-(59).

(I)
$$\begin{pmatrix} \frac{di_{Lf}}{dt} \\ \frac{dV_c}{dt} \\ \frac{dI_{Ls}}{dt} \\ \frac{dV_o}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{N}{L_s} \\ 0 & 0 & -\frac{1}{C_o} & -\frac{1}{RC_o} \end{bmatrix} \begin{pmatrix} i_{Lf} \\ V_c \\ i_{Ls} \\ V_o \end{pmatrix} + \begin{pmatrix} \frac{1}{L_f} \\ 0 \\ 0 \\ 0 \end{pmatrix} V_s \quad (56)$$

(II)
$$\begin{pmatrix} \frac{di_{Lf}}{dt} \\ \frac{dV_c}{dt} \\ \frac{dI_{Ls}}{dt} \\ \frac{dV_o}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_o} \end{bmatrix} \begin{pmatrix} i_{Lf} \\ V_c \\ i_{Ls} \\ V_o \end{pmatrix} + \begin{pmatrix} \frac{1}{L_f} \\ 0 \\ 0 \\ 0 \end{pmatrix} V_s \quad (57)$$

(III)
$$\begin{pmatrix} \frac{di_{Lf}}{dt} \\ \frac{dV_c}{dt} \\ \frac{dI_{Ls}}{dt} \\ \frac{dV_o}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & -\frac{1}{L_f} & 0 & 0 \\ \frac{1}{Cc} & 0 & -\frac{1}{Cc} & 0 \\ 0 & \frac{1}{Ls} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_o} \end{bmatrix} \begin{pmatrix} i_{Lf} \\ V_c \\ i_{Ls} \\ V_o \end{pmatrix} + \begin{pmatrix} \frac{1}{L_f} \\ 0 \\ 0 \\ 0 \end{pmatrix} V_s \quad (58)$$

(IV)
$$\begin{pmatrix} \frac{di_{Lf}}{dt} \\ \frac{dV_c}{dt} \\ \frac{dI_{Ls}}{dt} \\ \frac{dV_o}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & -\frac{1}{L_f} & 0 & 0 \\ \frac{1}{Cc} & 0 & -\frac{1}{Cc} & 0 \\ 0 & \frac{1}{Ls} & 0 & -\frac{N}{Ls} \\ 0 & 0 & \frac{1}{Co} & -\frac{1}{RC_o} \end{bmatrix} \begin{pmatrix} i_{Lf} \\ V_c \\ i_{Ls} \\ V_o \end{pmatrix} + \begin{pmatrix} \frac{1}{L_f} \\ 0 \\ 0 \\ 0 \end{pmatrix} V_s \quad (59)$$

The series-inductor current $i_{Ls}(t)$ ($=I_{tr}(t)$) varies faster than the other state variables. Therefore, $i_{Ls}(t)$ for the subintervals (I)-(IV) can be replaced by Equations (9)-

(12) which consist of slow state variables, V_c and V_o. The resulting matrices are given in Equations (60)-(63).

$$\text{(I')} \quad \begin{pmatrix} \frac{di_{Lf}}{dt} \\ \frac{dV_c}{dt} \\ \frac{dV_o}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{RC_o} \end{bmatrix} \begin{pmatrix} i_{Lf} \\ V_c \\ V_o \end{pmatrix} + \begin{pmatrix} \frac{1}{L_f} \\ 0 \\ 0 \end{pmatrix} V_s + \begin{pmatrix} 0 \\ 0 \\ -\frac{N}{C_o} \end{pmatrix} I_{tr}(t) \qquad (60)$$

$$\text{(II')} \quad \begin{pmatrix} \frac{di_{Lf}}{dt} \\ \frac{dV_c}{dt} \\ \frac{dV_o}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{RC_o} \end{bmatrix} \begin{pmatrix} i_{Lf} \\ V_c \\ V_o \end{pmatrix} + \begin{pmatrix} \frac{1}{L_f} \\ 0 \\ 0 \end{pmatrix} V_s + \begin{pmatrix} 0 \\ 0 \\ -\frac{N}{C_o} \end{pmatrix} I_{tr}(t) \qquad (61)$$

$$\text{(III')} \quad \begin{pmatrix} \frac{di_{Lf}}{dt} \\ \frac{dV_c}{dt} \\ \frac{dV_o}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & -\frac{1}{L_f} & 0 \\ \frac{1}{C_c} & 0 & 0 \\ 0 & 0 & -\frac{1}{RC_o} \end{bmatrix} \begin{pmatrix} i_{Lf} \\ V_c \\ V_o \end{pmatrix} + \begin{pmatrix} \frac{1}{L_f} \\ 0 \\ 0 \end{pmatrix} V_s + \begin{pmatrix} 0 \\ -\frac{1}{C_c} \\ 0 \end{pmatrix} I_{tr}(t) \qquad (62)$$

$$\text{(IV')} \quad \begin{pmatrix} \frac{di_{Lf}}{dt} \\ \frac{dV_c}{dt} \\ \frac{dV_o}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & -\frac{1}{L_f} & 0 \\ \frac{1}{C_c} & 0 & 0 \\ 0 & 0 & -\frac{1}{RC_o} \end{bmatrix} \begin{pmatrix} i_{Lf} \\ V_c \\ V_o \end{pmatrix} + \begin{pmatrix} \frac{1}{L_f} \\ 0 \\ 0 \end{pmatrix} V_s + \begin{pmatrix} 0 \\ -\frac{1}{C_c} \\ \frac{N}{C_o} \end{pmatrix} I_{tr}(t) \qquad (63)$$

In small-signal modeling, a moving-average method is conventionally used to remove the high-frequency switching ripples. Using this method, state variables are averaged from one switching cycle to the next. As a result, low-frequency variations are modeled [32]. The resulting equations are represented with the state variables i_{Lf}, V_c, and V_o and a line input, V_s. In the derivation, the control inputs are defined as $d(t) = \frac{\delta}{2\pi}$, $d_{\emptyset}(t) = \frac{\emptyset}{2\pi}$ regarding Figure 5.2.

The parameters used in the derivation are L_s, the parasitic resistance of the dc inductor (R_s), load resistance (R), and the transformer's turns-ratio (N) where N =

$\frac{\text{primary winding turns}}{\text{secondary winding truns}}$. The averaged state equations over a half switching period (T_h=0.5T_s) are shown in (64)-(66) in matrix form.

$$\begin{pmatrix} \frac{d<i_{Lf}(t)>_{T_h}}{dt} \\ \frac{d<V_c(t)>_{T_h}}{dt} \\ \frac{d<V_o(t)>_{T_h}}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & -\frac{2d(t)}{L_f} & 0 \\ \frac{2d(t)}{C_c} & 0 & K_1 \\ 0 & K_2 & \frac{-1}{RC_o} \end{bmatrix} \begin{pmatrix} < i_{Lf}(t) >_{T_h} \\ < V_c(t) >_{T_h} \\ < V_o(t) >_{T_h} \end{pmatrix} + \begin{pmatrix} \frac{1}{L_f} \\ 0 \\ 0 \end{pmatrix} <V_s(t)>_{T_h} \quad (64)$$

$$K_1 = \frac{(-2d(t)*d_\emptyset(t)+d_\emptyset^2(t))NT_s}{L_s C_c} \quad (65)$$

$$K_2 = \frac{2d(t)d_\emptyset(t)NTs - d_\emptyset^2(t)NTs}{C_o L_s} \quad (66)$$

The state equations in matrix Equation (64) are nonlinear since the time-varying state variables are multiplied by the duty ratio, d(t), which is also a time-varying quantity. To linearize the equations, a first-order approximation is used. Conventionally, perturbation and linearization methods are widely used for first-order approximation. To construct a small-signal model at a quiescent operating point, the input, state, and control variables are assumed to have dc terms in capital letters such as V_s and D, plus ac variations in lower cases, such as $\hat{v}_s(t)$, $\hat{d}(t)$. Hence, the averaged variables are represented as

$<V_s(t)>_{T_s} = V_s + \hat{v}_s(t)$, $< V_c(t) >_{T_s} = V_c + \hat{v}_c(t)$, $< V_o(t) >_{T_s} = V_o + \hat{v}_o(t)$,

$< i_{Lf}(t) >_{T_s} = I_{Lf} + \hat{i}_{Lf}(t)$, $< d(t)>_{T_s} = D + \hat{d}(t)$, $< d_\emptyset(t) >_{T_s} = D_\emptyset + \hat{d}_\emptyset(t)$.

In the linearization, dc terms, second-order terms, and higher-order terms are neglected. The resulting small-signal models are represented in Equation (67)-(69).

$$\begin{pmatrix} \frac{d\hat{i}_{Lf}(t)}{dt} \\ \frac{d\hat{v}_c(t)}{dt} \\ \frac{d\hat{v}_o(t)}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & -\frac{2D}{L_f} & 0 \\ \frac{2D}{Cc} & 0 & K_3 \\ 0 & K_4 & \frac{-1}{RC_o} \end{bmatrix} \begin{pmatrix} \hat{i}_{Lf}(t) \\ \hat{v}_c(t) \\ \hat{v}_o(t) \end{pmatrix} + \begin{pmatrix} \frac{-2V_c}{L_f} \\ (\frac{2I_{Lf}}{C_c} - \frac{2D_\emptyset NT_s V_o}{C_c L_s}) \\ \frac{2D_\emptyset NT_s V_c}{C_o L_s} \end{pmatrix} \hat{d}(t) +$$

$$+ \begin{pmatrix} 0 \\ (\frac{2D_\emptyset NT_s V_o - 2DNT_s V_o}{C_c L_s}) \\ \frac{2DNT_s V_c}{C_o L_s} - \frac{2D_\emptyset NT_s V_c}{C_o L_s} \end{pmatrix} \hat{d}_\emptyset(t) + \begin{pmatrix} \frac{1}{L_f} \\ 0 \\ 0 \end{pmatrix} \widehat{V}s(t) \quad (67)$$

$$K_3 = \frac{(-2DD_\emptyset NT_s)}{C_c L_s} + \frac{(D_\emptyset^2 NT_s)}{C_c L_s} \quad (68)$$

$$K_4 = \frac{1}{C_o L_s}(2DD_\emptyset NT_s - D_\emptyset^2 NT_s) \quad (69)$$

Matrix Equations (67)-(69) can be organized in the form $\dot{X} = AX + BU$ as shown in Equation (70).

$$X = \begin{pmatrix} \hat{i}_{Lf}(t) \\ \hat{v}_c(t) \\ \hat{v}_o(t) \end{pmatrix}, \quad A = \begin{bmatrix} -\frac{R_s}{L_f} & -\frac{D}{L_f} & 0 \\ \frac{D}{C_c} & 0 & K_3 \\ 0 & K_4 & \frac{-1}{2RC_o} \end{bmatrix}, \quad B = [B_1\ B_2\ B_3], \quad (70)$$

$$B_1 = \begin{pmatrix} \frac{-2V_c}{L_f} \\ (\frac{2I_{Lf}}{C_c} - \frac{2D_\emptyset T_s V_c}{C_c L_s}) \\ \frac{2D_\emptyset NT_s V_c}{C_o L_s} \end{pmatrix}, \quad B_2 = \begin{pmatrix} 0 \\ (\frac{2D_\emptyset NT_s V_o - 2DNT_s V_o}{C_c L_s}) \\ \frac{2DNT_s V_c}{C_o L_s} - \frac{2D_\emptyset NT_s V_c}{C_o L_s} \end{pmatrix} \hat{d},$$

$$B_3 = \begin{pmatrix} \frac{1}{L_f} \\ 0 \\ 0 \end{pmatrix}, \quad U = \begin{pmatrix} \hat{d}(t) \\ \hat{d}_\emptyset(t) \\ \hat{v}_S(t) \end{pmatrix}$$

$$K_3 = \frac{(-2DD_\emptyset NT_s)}{C_c L_s} + \frac{(D_\emptyset^2 NT_s)}{C_c L_s}, \quad K_4 = \frac{1}{C_o L_s}(2DD_\emptyset NT_s - D_\emptyset^2 NT_s)$$

Conversion of matrix Equation (70) using Laplace transform presents the transfer functions of the control input ($\hat{d}(t)$ or $\widehat{\emptyset}(t)$) to the state outputs ($\widehat{V}_c(t)$ or $\widehat{V}_o(t)$). In the following example, the transfer functions are obtained for the specified conditions and set

of parameters. The parameters and conditions are C_c = 3 mF, C_o = 2 mF, L_f = 100 uH, F_{sw} = 35 kHz, V_s = 160 V, V_o = 133 V, N = 3:2, and P_o = 3 kW.

Figure 5.3 shows the transfer function from the control input (d(s)) to the output (V_c(s)), denoted as G_{V_cd}(s). All poles in G_{V_cd}(s) are located in the left-half plane. At the crossover frequency, the phase margin is also higher than -180 degrees. Hence, the transfer function, G_{V_cd}(s), is stable. In the transfer function, G_{V_cd}(s), all zeros are located in the left-half plane. In the DAB[3] topology, the operation of Bridge 1 looks similar to the boost converter. However, there is no feed-forward path in the operation of Bridge 1. This fact explains why there are no right-half plane (RHP) zeros in the system for boost mode.

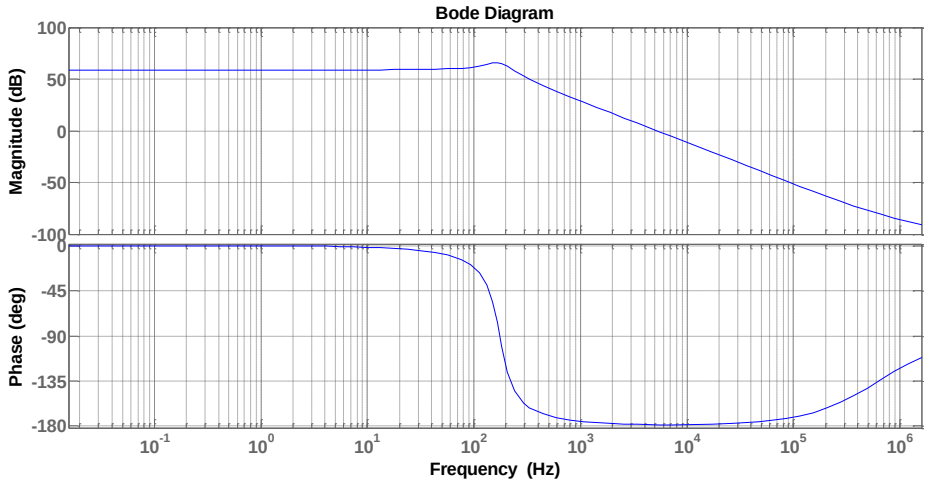


Figure 5.3. Bode plot of the transfer function, $T_{v_cd}(s)$.

Figure 5.4 shows the transfer function of phase angle (Ø) to the output voltage (V_o), denoted as ($G_{V\emptyset}$(s)). The system is stable and has only LHP poles and zeros.

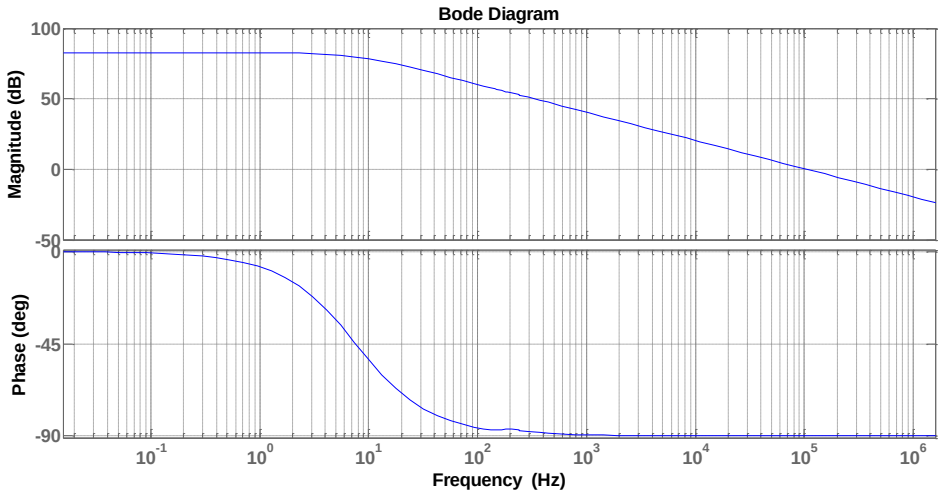


Figure 5.4. Bode plot of the transfer function, $G_{V\emptyset}(s)$.

5.3. Small-Signal Model of Buck Mode

When the power flows from Bridge 2 to Bridge 1, the operation of the DAB^3 converter is defined as the buck mode. Because the power stage in the buck mode has different dynamics from that in the boost mode, a separate small-signal model is developed for the buck mode. As discussed in Section 5.2, the power transfer in the DAB^3 converter is half-wave symmetric. Hence, the state equations over a half switching period can be used as the small-signal model.

Equations (71)-(74) show the state equations for a half-switching period ($0.5T_s$). The state variable, i_{Ls} represents the transformer current (I_{tr}) in Bridge 1.

(I_b)
$$\begin{pmatrix} \frac{diLf}{dt} \\ \frac{dV_C}{dt} \\ \frac{di_{Ls}}{dt} \\ \frac{dV_s}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & \frac{1}{L_f} & 0 & -\frac{1}{L_f} \\ -\frac{1}{C_c} & 0 & -\frac{N}{C_c} & 0 \\ 0 & \frac{1}{L_s} & 0 & 0 \\ \frac{1}{C_s} & 0 & 0 & -\frac{1}{RC_s} \end{bmatrix} \begin{pmatrix} i_{Lf} \\ V_c \\ i_{Ls} \\ V_s \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} V_o \quad (71)$$

(II_b)

$$\begin{pmatrix} \frac{diLf}{dt} \\ \frac{dV_c}{dt} \\ \frac{di_{Ls}}{dt} \\ \frac{dV_s}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & \frac{1}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{C_s} & 0 & 0 & -\frac{1}{RC_s} \end{bmatrix} \begin{pmatrix} i_{Lf} \\ V_c \\ i_{Ls} \\ V_s \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} V_o \quad (72)$$

(III_b)

$$\begin{pmatrix} \frac{diLf}{dt} \\ \frac{dV_c}{dt} \\ \frac{di_{Ls}}{dt} \\ \frac{dV_s}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & 0 & 0 & -\frac{1}{L_f} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{C_s} & 0 & 0 & -\frac{1}{RC_s} \end{bmatrix} \begin{pmatrix} i_{Lf} \\ V_c \\ i_{Ls} \\ V_s \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \\ \frac{1}{L_s} \\ 0 \end{pmatrix} V_o \quad (73)$$

(IV_b)

$$\begin{pmatrix} \frac{diLf}{dt} \\ \frac{dV_c}{dt} \\ \frac{di_{Ls}}{dt} \\ \frac{dV_s}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & \frac{1}{L_f} & 0 & -\frac{1}{L_f} \\ -\frac{1}{C_c} & 0 & \frac{N}{C_c} & 0 \\ 0 & -\frac{1}{L_s} & 0 & 0 \\ \frac{1}{C_s} & 0 & 0 & -\frac{1}{RC_s} \end{bmatrix} \begin{pmatrix} i_{Lf} \\ V_c \\ i_{Ls} \\ V_s \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \\ \frac{N}{L_s} \\ 0 \end{pmatrix} V_o \quad (74)$$

Replacing the faster variable ($i_{Ls}= I_{tr}$) with the slow variables (V_c and V_o), the state matrices in Equations (71)-(74) simplify to Equations (75)-(78).

(I_b')

$$\begin{pmatrix} \frac{di_{Lf}}{dt} \\ \frac{dV_c}{dt} \\ \frac{dV_s}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & \frac{1}{L_f} & -\frac{1}{L_f} \\ -\frac{1}{C_c} & 0 & 0 \\ \frac{1}{C_s} & 0 & -\frac{1}{RC_s} \end{bmatrix} \begin{pmatrix} i_{Lf} \\ V_c \\ V_s \end{pmatrix} + \begin{pmatrix} 0 \\ -\frac{1}{C_c} \\ 0 \end{pmatrix} I_{tr}(t) \quad (75)$$

(II_b')

$$\begin{pmatrix} \frac{di_{Lf}}{dt} \\ \frac{dV_c}{dt} \\ \frac{dV_s}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & 0 & 0 \\ \frac{1}{C_s} & 0 & -\frac{1}{RC_s} \end{bmatrix} \begin{pmatrix} i_{Lf} \\ V_c \\ V_s \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \\ 0 \end{pmatrix} I_{tr}(t) \quad (76)$$

$$(III_b') \qquad \begin{pmatrix} \frac{di_{Lf}}{dt} \\ \frac{dV_c}{dt} \\ \frac{dV_s}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & 0 & 0 \\ \frac{1}{C_s} & 0 & -\frac{1}{RC_s} \end{bmatrix} \begin{pmatrix} i_{Lf} \\ V_c \\ V_s \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \\ 0 \end{pmatrix} I_{tr}(t) \qquad (77)$$

$$(IV_b') \qquad \begin{pmatrix} \frac{di_{Lf}}{dt} \\ \frac{dV_c}{dt} \\ \frac{dV_s}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & \frac{1}{Lf} & -\frac{1}{L_f} \\ -\frac{1}{Cc} & 0 & 0 \\ \frac{1}{C_s} & 0 & -\frac{1}{RC_s} \end{bmatrix} \begin{pmatrix} i_{Lf} \\ V_c \\ V_s \end{pmatrix} + \begin{pmatrix} 0 \\ \frac{1}{C_c} \\ 0 \end{pmatrix} I_{tr}(t) \qquad (78)$$

Using Equations (75)-(78), the averaged models are derived for a half-switching period. Equations (79) and (80) represent a state matrix with variables averaged over a half-switching period ($T_h = 0.5\ T_s$).

$$\begin{pmatrix} \frac{d<i_{Lf}(t)>_{T_h}}{dt} \\ \frac{d<V_c(t)>_{T_h}}{dt} \\ \frac{d<V_s(t)>_{T_h}}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & \frac{2d(t)}{L_f} & -\frac{1}{L_f} \\ -\frac{2d(t)}{C_c} & 0 & 0 \\ \frac{1}{C_s} & 0 & \frac{-1}{RC_s} \end{bmatrix} \begin{pmatrix} < i_{Lf}(t) >_{T_h} \\ < V_c(t) >_{T_h} \\ < V_s(t) >_{T_h} \end{pmatrix} + \begin{pmatrix} 0 \\ K_5 \\ 0 \end{pmatrix} <V_o(t)>_{T_h} \qquad (79)$$

$$K_5 = \frac{(2d(t) * d_\emptyset(t) - d_\emptyset^2(t))NT_s}{L_s C_c} \qquad (80)$$

The small-signal model for the buck mode is obtained using perturbation and linearization methods, as shown in Equation (81).

$$\begin{pmatrix} \frac{d\hat{i}_{Lf}(t)}{dt} \\ \frac{d\hat{v}_c(t)}{dt} \\ \frac{d\hat{v}_s(t)}{dt} \end{pmatrix} = \begin{bmatrix} -\frac{R_s}{L_f} & \frac{2D}{L_f} & -\frac{1}{L_f} \\ \frac{-2D}{C_c} & 0 & 0 \\ \frac{1}{C_s} & 0 & \frac{-1}{RC_s} \end{bmatrix} \begin{pmatrix} \hat{i}_{Lf}(t) \\ \hat{v}_c(t) \\ \hat{v}_s(t) \end{pmatrix} + \begin{pmatrix} \frac{2V_c}{L_f} \\ (-\frac{2I_{Lf}}{C_c} + \frac{2D_\emptyset NT_s V_o}{C_c L_s}) \\ 0 \end{pmatrix} \hat{d}(t) +$$

$$\begin{pmatrix} 0 \\ (\frac{-2D_\emptyset NT_s V_o + 2DNT_s V_o}{C_c L_s}) \\ 0 \end{pmatrix} \hat{d}_\emptyset(t) + \begin{pmatrix} 0 \\ \frac{2DD_\emptyset NT_s - D_\emptyset^2 NT_s}{C_c L_s} \\ 0 \end{pmatrix} \hat{V}_o(t) \qquad (81)$$

Transfer functions of the power stage can be derived using the small-signal model. The set of matrix Equations (82) can be organized in the form of $\dot{X} = AX + BU$.

$$X = \begin{pmatrix} \hat{i}_{Lf}(t) \\ \hat{v}_c(t) \\ \hat{v}_s(t) \end{pmatrix}, \quad A = \begin{bmatrix} -\frac{R_s}{L_f} & \frac{2D}{L_f} & -\frac{1}{Lf} \\ -\frac{2D}{Cc} & 0 & 0 \\ \frac{1}{Cs} & K_4 & \frac{-1}{RC_s} \end{bmatrix}, \quad B = [B_1\ B_2\ B_3], \qquad (82)$$

$$B_1 = \begin{pmatrix} \frac{2V_c}{L_f} \\ (-\frac{2I_{Lf}}{C_c} + \frac{2D_\emptyset NT_s V_c}{C_c L_s}) \\ 0 \end{pmatrix}, \quad B_2 = \begin{pmatrix} 0 \\ (\frac{-2D_\emptyset NT_s V_o + 2DNT_s V_o}{C_c L_s}) \\ 0 \end{pmatrix},$$

$$B_3 = \begin{pmatrix} 0 \\ \frac{2DD_\emptyset NT_s - D_\emptyset^2 NT_s}{C_c L_s} \\ 0 \end{pmatrix}, \quad U = \begin{pmatrix} \hat{d}(t) \\ \hat{d}_\emptyset(t) \\ \hat{v}_s(t) \end{pmatrix}$$

Similar to the boost mode, the phase-shift angle ($\hat{\emptyset}(t)$) and the duty ratio ($\hat{d}(t)$) are the chosen control variables for the buck mode. Figure 5.5 shows the DAB[3] converter in the buck mode. As shown in the figure, the clamp voltage (V_c) and output voltage (V_s) are required to be regulated to achieve power transfer with a flat-top waveforms. If the control scheme is made such that V_c is controlled by $\emptyset(t)$, and V_s is controlled by d(t), then the transfer functions of $G_{v_c\emptyset}(s) = \frac{V_c(s)}{d_\emptyset(s)}$ and $G_{v_s d}(s) = \frac{V_s(s)}{d(s)}$ can be derived.

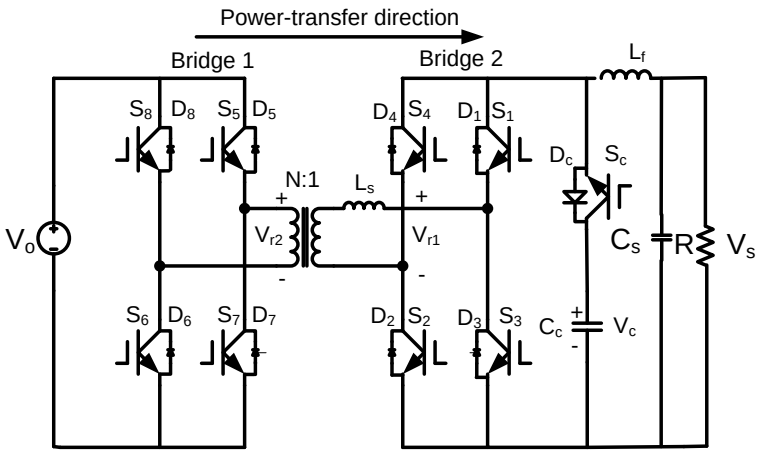


Figure 5.5. DAB^3 converter in buck mode.

The bode plot of the transfer function, $G_{v_c\emptyset}(s)$ is shown in Figure 5.6. The magnitude decreases initially at -20dB/decade from a single low-frequency pole. At approximately 200-300 Hz, a double pole and double zeros make a glitch. The phase makes a high peak and settles to -90 degree. All poles are located in the left-half plane. Hence, the system function is stable.

For the control of $V_s(t)$, the transfer function of the control input (d(s)) to output $V_s(s)$, denoted as , $G_{v_sd}(s) = \frac{V_s(s)}{d(s)}$, is derived using only $i_{Lf}(t)$ and $V_s(t)$ as state variables. In the transfer function shown in Figure 5.7, complex double poles exist in the left-half plane. The system is stable due to the positive phase margin at the crossover frequency.

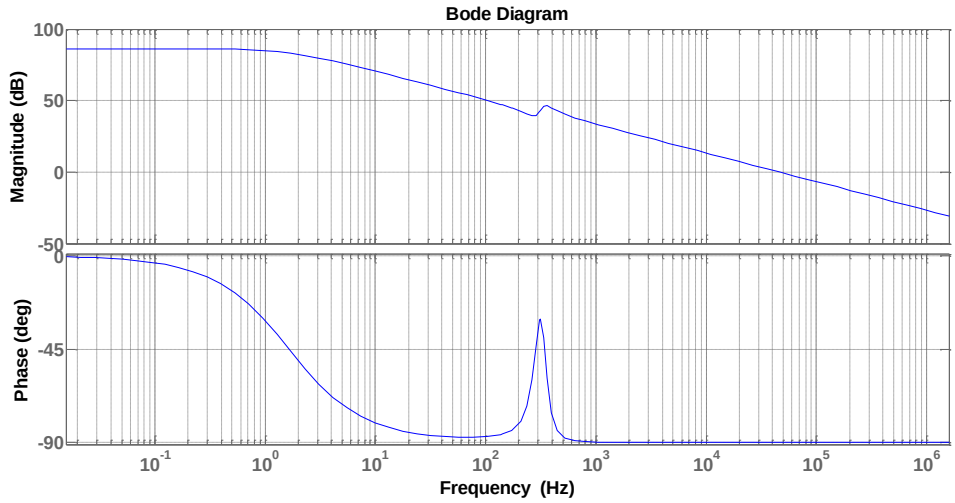


Figure 5.6. Bode plot of the transfer function, $G_{v_c\emptyset}(s) = \frac{V_c(s)}{d_\emptyset(s)}$.

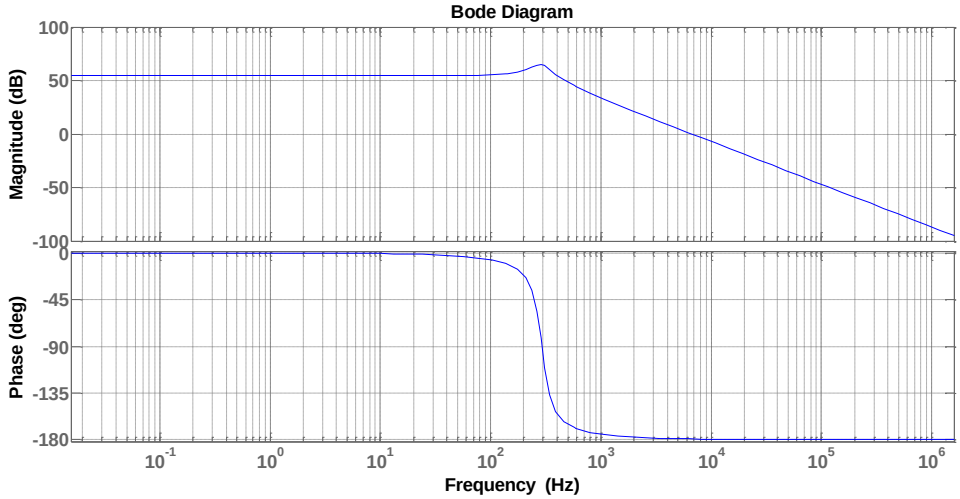


Figure 5.7. Bode plot of the transfer function, $G_{v_s d}(s) = \frac{V_s(s)}{d(s)}$.

5.4. Chapter Summary

In this chapter, small-signal models were developed for the DAB^3 converter topology. The derivation of small-signal models proceeded averaging operation over the switching period and then applying the perturbation, and linearization methods. Since the

output power is half-wave symmetric, the state equations in the half period were used for averaging state variables.

In the DAB^3 converter, the duty ratio and the phase-shift angle can be defined as control variables since the output power and the clamp capacitor voltage (V_c) are the functions of duty ratio and phase-shift angle. Hence, the relations between the state and control variables were analyzed.

From bode plot analyses, the transfer functions of the system are stable for both boost and buck modes. In the next chapter, these transfer functions are used to design the feedback controllers. The stability test of the converter is also performed by designed controllers using the Saber simulator.

CHAPTER 6

DESIGN OF CONTROLLERS AND EXPERIMENTAL REUSLTS

6.1. Introduction

The main task in the control of the DAB^3 converter is to control device currents by regulating the voltage levels of the clamp capacitor (V_c) and the load voltage (V_o or V_s). In this chapter, the voltage controls are implemented using proportional-integral (PI) controllers; however, the PI network is not responsible for all of the issues in the design of the control for the DAB^3 converter. The transformer-saturation problem also needs to be addressed since dual-active switching with the control of the duty ratio and the phase-shift angle causes dc currents in the transformer. Hence, one method to prevent dc saturation of the high-frequency isolation transformer is proposed.

This chapter also focuses on the implementation of the controllers using FPGA (Field-Programmable-Gate Arrays). The discretized PI controls and other functional blocks are designed in detail, in preparation for hardware implementation. The last section provides experimental results. The experimental results show that device stresses are controlled over a range of source voltage and loading conditions.

6.2. Controller Design in the Continuous-Time Domain

6.2.1. Overall control concepts

In Chapter 3, a minimum total-device rating was achieved by controlling the clamp voltage (V_c) to NV_o, where V_o is the voltage level required by the load. The clamp

voltage, V_c is controlled by the duty ratio. The magnitude and direction of the power flow is controlled by the phase-shift angle. The controller is first designed in the continuous-time domain and analyzed using bode analysis. Then, the controllers will be discretized for implementation in a digital control system.

Figure 6.1 illustrates a block diagram with the main controllers and functional blocks. The block diagram has two loops $T_1(s)$ and $T_2(s)$. $T_1(s)$ represents the control loop in Bridge 1, which is realized with duty-ratio control. $T_2(s)$ in Bridge 2 is realized with a phase-shift angle control. In these control loops, H_1 and H_2 are sensor gains, V_c^* and V_o^* are reference values, and C(s) and D(s) represent the compensators in $T_1(s)$ and $T_2(s)$ respectively.

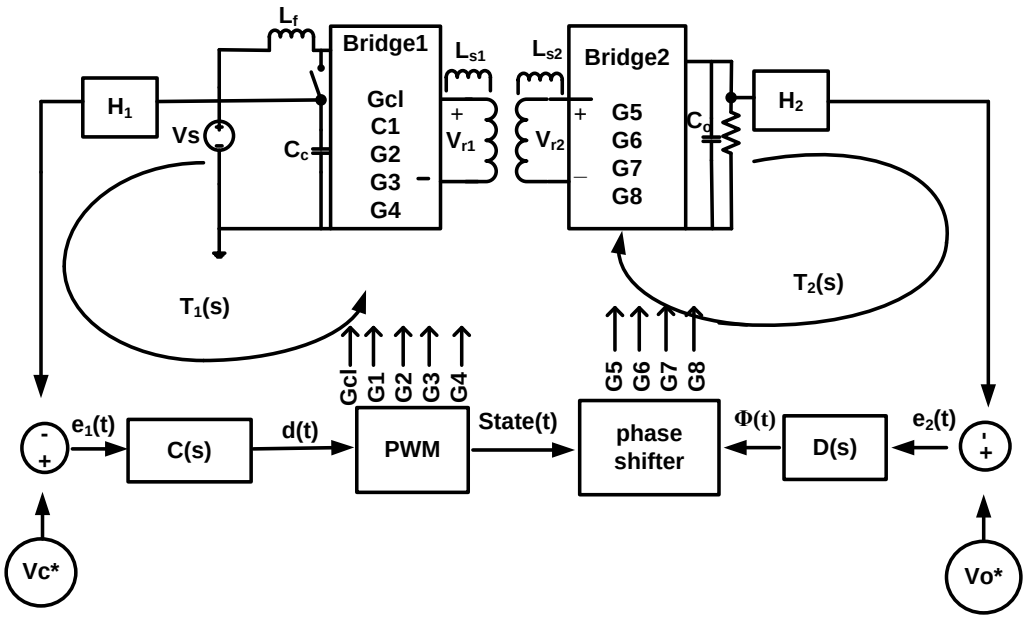


Figure 6.1. Block diagram of the control schemes for the DAB^3 converter.

The switching in Bridge 1 is realized using the PWM (pulse-width modulation) method. The compensator, C(s), in $T_1(s)$ should be designed to ensure the system's stability and to decrease the steady-state errors. A state machine is used to generate

switching signals based on the duty-ratio signal from the PWM units. The phase-shift angle (∅) and the state information (State (t)) generate the switching signals for Bridge 2. The phase-shift angle is controlled by the compensator D(s) in $T_2(s)$, which regulates V_o to match the reference value, V_o^*. The gating signals in Bridge 2 ensure the waveform of V_{r2} has the same duty ratio (D) as V_{r1} but is shifted by the phase angle (∅).

6.2.2. Design of controllers

In this section, the compensators C(s) and D(s) are designed in the continuous-time domain and in the next section, they will be mapped to discretized forms. The small-signal models, which were derived in Chapter 5, are used to derive transfer functions based on the operating conditions shown in Table 12. Since the clamp capacitor voltage is regulated by adjusting the duty ratio, the relationship of the small-signal duty ratio ($\hat{d}$) to small-signal voltage output ($\hat{v}_c$) is considered in the design. The transfer function, $G_{V_c d}(s)$, which was defined and derived in Chapter 5, is the plant. The block diagram of the clamp capacitor voltage regulator is shown in Figure 6.2.

Table 12. Conditions and parameters in the experimental unit.

component	value	component	Value
L_f	50 uH	R	20, 10.3, 7.7 Ω
C_c	6 mF	V_s	155-120 V
C_o	9 mF	V_c^*	189 V
L_s(L_{s1}+L_{s2})	8 uH	V_o^*	125 V
H_1	1.5/189	N_1:N_2	3:2
H_2	1.5/125		

From Figure 6.1 and Figure 6.2, the loop gain, $T_1(s)$, can be represented as $T_1(s) = H_1(s)C(s)G_{Vcd}(s)/V_m$. The loop gain, $T_1(s)$ is analyzed in stability and dynamics of the feedback system.

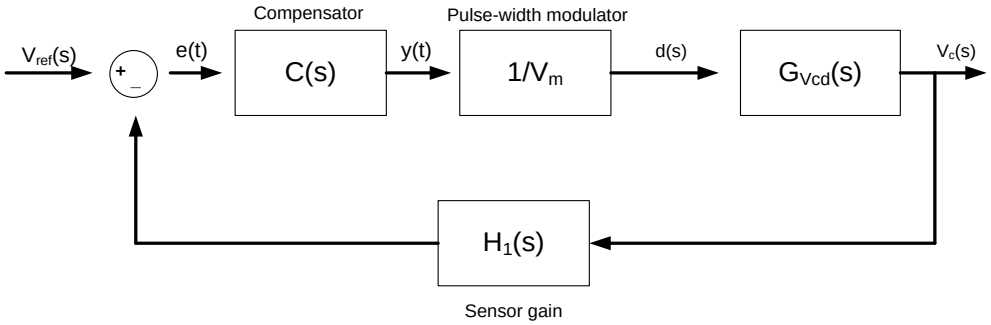


Figure 6.2. Small-signal model of the voltage regulator for $T_1(s)$.

A bode-plot is used to design and analyze the controllers. Figure 6.3 shows the bode plot of the uncompensated loop gain, $T_{1u}(s)$, where $C(s) = 1$. The bode plot of $T_{1u}(s)$ shows the phase margin of 20 degrees at the crossover frequency (f_c =300 Hz). The crossover frequency is low since a high capacitance (6 mF) is used for the clamp capacitor. The clamp capacitor is implemented with electrolytic capacitors, which have low current-ripple ratings. Hence, many capacitors are required to realize a sufficient current rating.

To increase the phase margin at the crossover frequency and decrease the steady-state error, the design uses a PI regulator. When applied to a dc/dc converter, a PI regulator generally provides a large low-frequency loop gain and a well-regulated dc output. The general form of the PI regulator is shown in Equation (83). $G_{c\infty}$ and ω_L can be 0.29 and 100, respectively, and the phase margin and dc gains can be increased.

$$C(s) = C_{\infty}\left(1 + \frac{w_L}{s}\right) \tag{83}$$

Figure 6.4 shows the bode plot of the compensated loop gain. The phase margin and dc gain are increased, while the crossover frequency is smaller than that of the uncompensated loop gain.

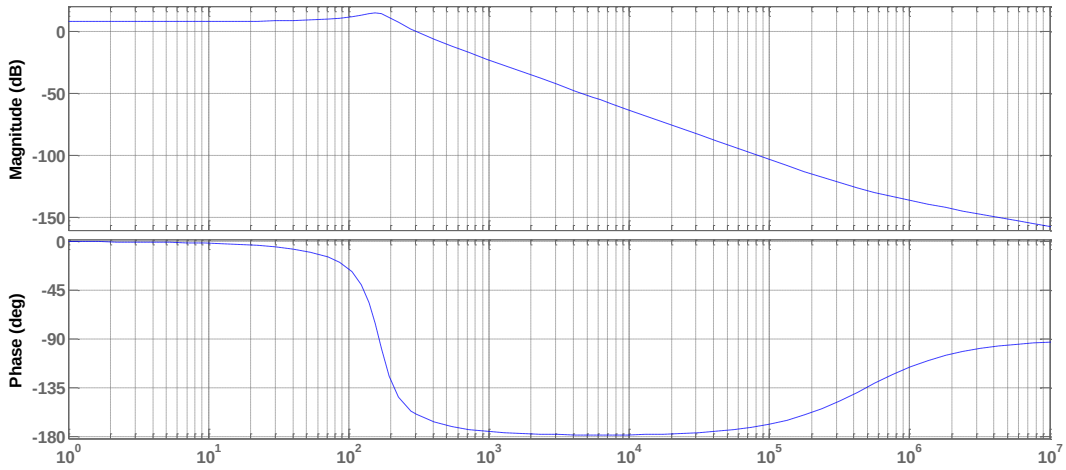


Figure 6.3. Bode plot of the uncompensated loop gain ($T_{u1}(s) = H_1(s)G_{Vcd}(s)/V_m$).

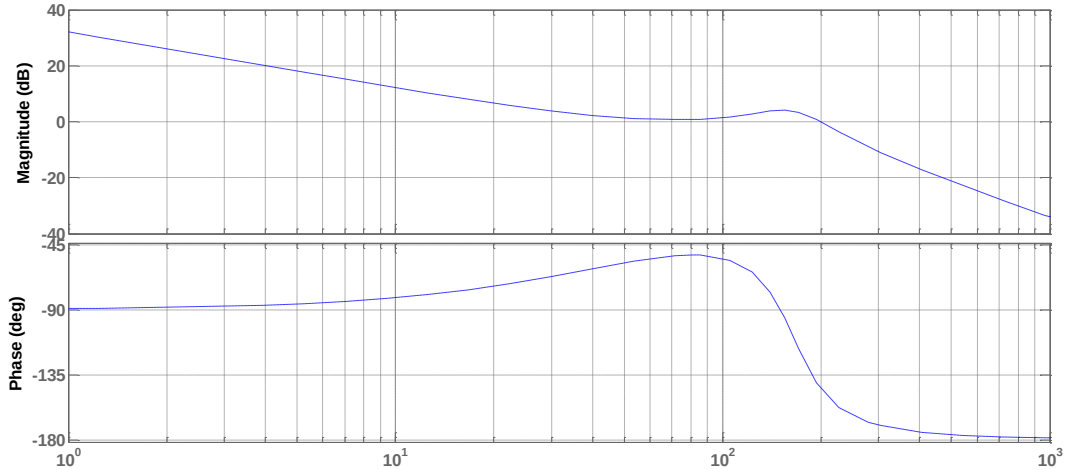


Figure 6.4. Bode plot of the compensated loop gain ($T_1(s) = G_{Vcd}(s)C(S)H_1(s)/V_m$).

The output power is controlled with $T_2(s)$. As depicted in Equations (25) and (26) in Chapter 3, the load voltage (V_o) or output power (P_o) is a function of the phase-shift angle (Ø) and the duty ratio (D). Since the duty ratio (D) of the system is calculated by

the control loop $T_1(s)$, the degree of freedom in designing the loop $T_2(s)$ decreases by importing D from the loop of $T_1(s)$. Hence, the phase-shift angle is calculated as the output of the compensator D(s). The general form of D(s), when it is realized with a PI compensator, is shown in Equation (84).

$$D(s) = D_\infty \left(1 + \frac{w_L}{s}\right) \tag{84}$$

Figure 6.5 illustrates the block diagram for the control of the load voltage (V_o). In this controller design, $G_{V\emptyset}(s)$ is used as a plant transfer function. As described in Chapter 5, $G_{V\emptyset}(s)$ is the transfer function of phase-shift angle ($\hat{d}_\emptyset$) to output voltage ($\hat{v}_o$). The compensator D(s) of $T_2(s)$ should be slower than C(s) of $T_1(s)$, since a similar dynamic response can cause coupling between $T_1(s)$ and $T_2(s)$.

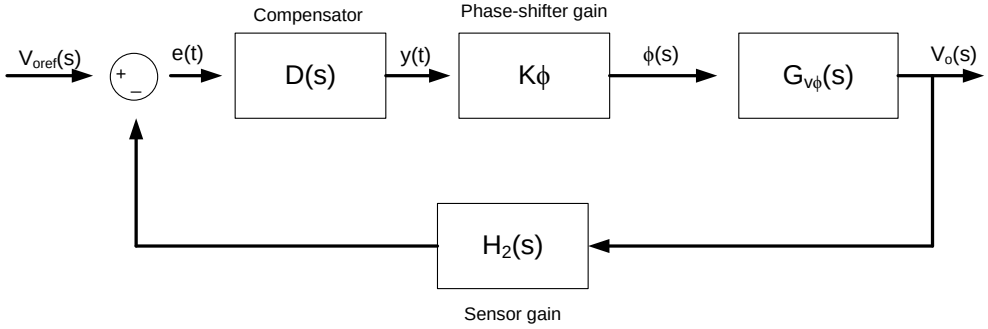


Figure 6.5. Load voltage (V_o) regulator small-signal model.

Figure 6.6 shows the bode plot of the uncompensated loop gain ($T_{u2}(s)=H_2(s)\ G_{v\emptyset}(s)K_\emptyset$). $T_{u2}(s)$ has a sufficient phase margin (>90 degree), and the crossover frequency is 200Hz. In Figure 6.7, the compensated loop gain, $T_2(s)$, is plotted. The plot indicates a high dc gain.

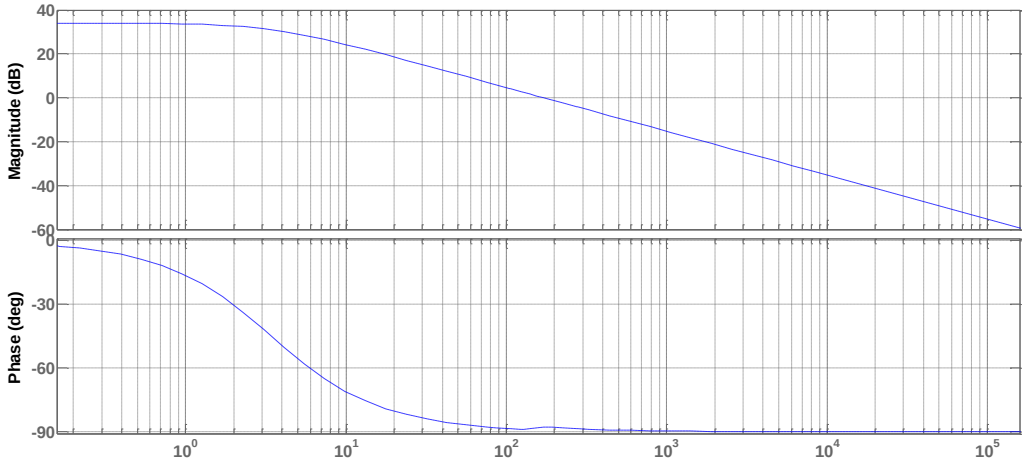


Figure 6.6. Bode plot of the uncompensated loop gain, $T_{u2}(s) = H_2(s)G_{v\emptyset}(s)K_{\emptyset}$.

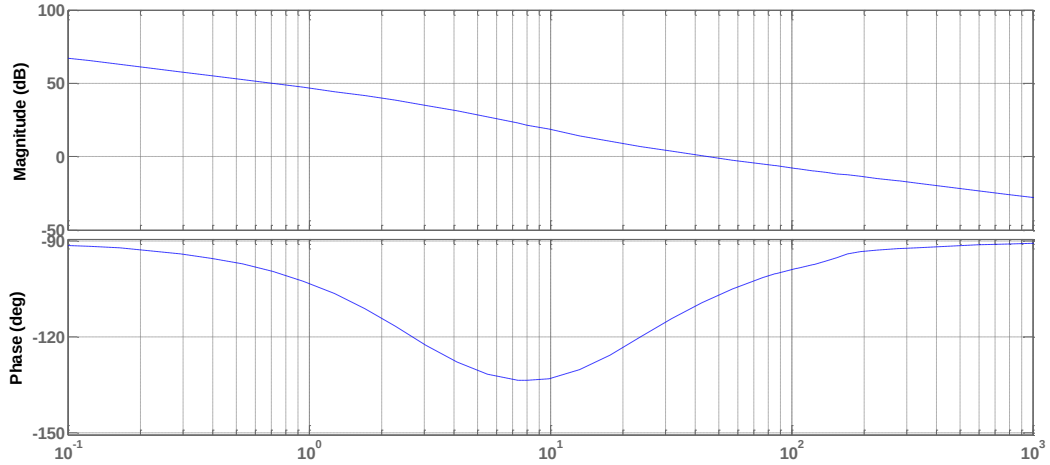
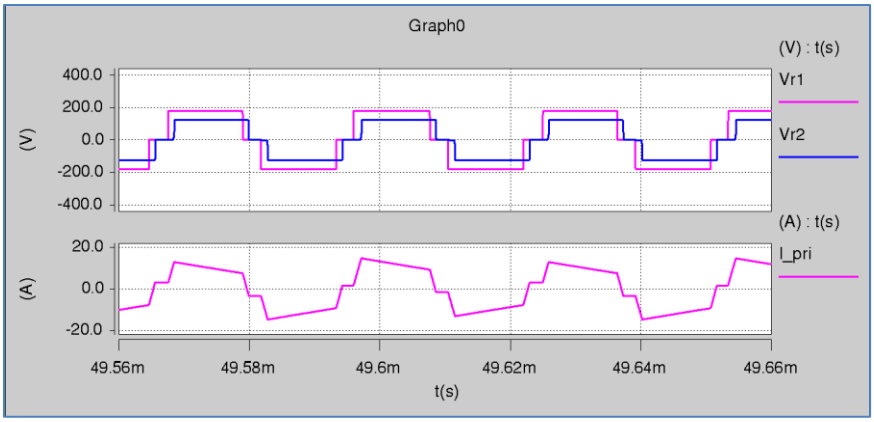
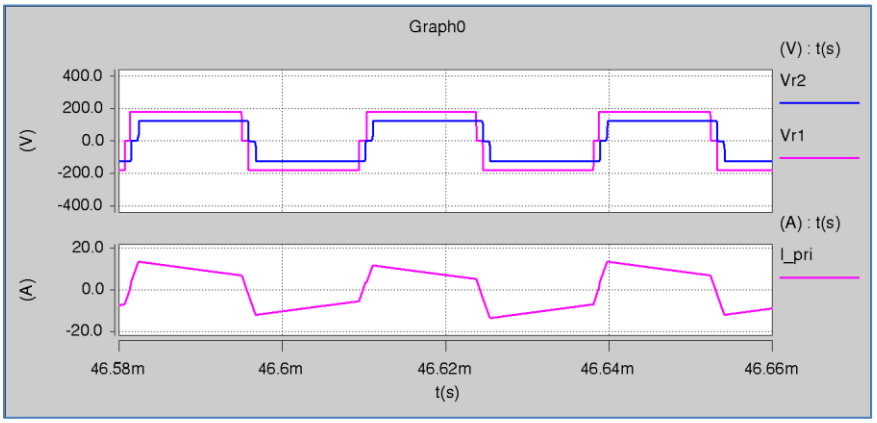


Figure 6.7. Bode plot of the compensated loop gain, $T_2(s) = H_2(s)D(s)G_{v\emptyset}(s)K_{\emptyset}$.

Figure 6.8 shows the simulated results of controlled power stage operation. The conditions of the simulation are V_s = 145~170 V, V_c^* = 180 V, and V_o^* = 125 V. The controller regulates the voltages to follow the reference voltages. The transformer currents are controlled to ensure low device stresses. Figure 6.9 shows the simulated step response due to a load change, which tests the stability of the controller. A step change of the load resistance from R = 20 Ω to R = 10 Ω varies the load current. However, the load voltage level is regulated to follow the reference voltage.



(a) V_s = 145 V, V_c^* = 180 V, V_o^* = 125 V.



(b) V_s = 170 V, V_c^* = 180 V, V_o^* = 125 V.

Figure 6.8. Simulation results of controlled power stage operation.

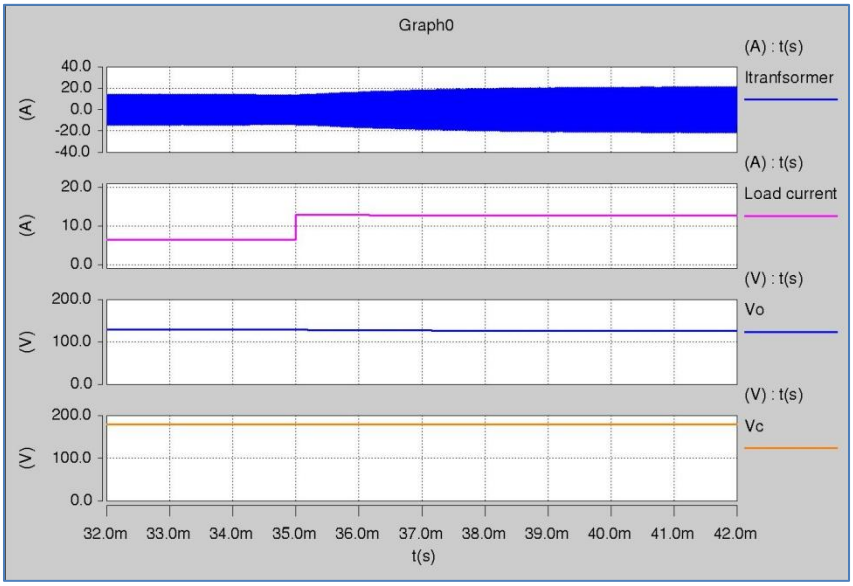


Figure 6.9. A step response by load change for a stability test. V_s = 145 V, V_c^* = 180 V, V_o^* = 125 V.

6.3. Digital-Control Implementations

6.3.1. Sampled-data system

In Section 6.2, the compensators were designed in the continuous-time domain. For digital-control implementation, the compensators should be discretized. Figure 6.10 presents a block diagram of the digital-control system for the DAB[3] converter. The control system consists of a power stage, voltage sensors (H_1 and H_2), analog-to-digital (A/D) converters, and a digital processor, a digital-phase shifter, a digital-pulse-width modulator (DPWM), a state machine, and controllers for the A/D converters [33-37]. An FPGA (Field-Programmable-Gate Array) is used as the digital processor for the experiment, since it has a smaller time delay than a microprocessor or digital-signal processor.

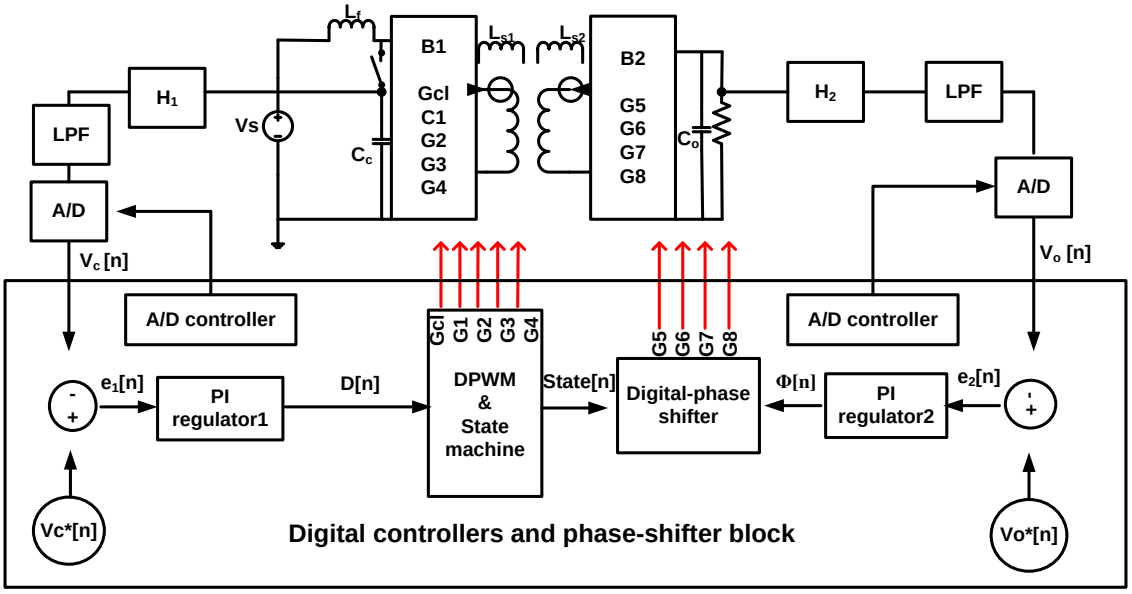


Figure 6.10. Block diagram of the sampled-data system.

As shown in Figure 6.10, the A/D converters, which produce 8-bit serial data, are used for converting the analog signals of $H_1V_c(t)$ and $H_2V_o(t)$ to $V_c[n]$ and $V_o[n]$. The 8-

bit-serial data are converted into an unsigned 8-bit word by a serial-shift register. For the calculation of negative numbers, the number format is converted into a 2's complement word, which is shown in Figure 6.11. For the entire digital implementation, 2's complement binary number is used as the base format, but changes its width for every requirement. For example, an extension of bits is required to prevent an overflow or underflow under the arithmetic operation of two 2's complement words. Summing two numbers such as $011111111_{(2)}$+$011111111_{(2)}$ causes an overflow. Hence, this condition requires the extension of a bit, such as $0011111111_{(2)} + 0011111111_{(2)} = 0111111111_{(2)}$.

If an 8-bit A/D converter which uses unsigned binary number is used for conversion of $H_1V_c^*(t) = 1.5$ V, the least significant bit (LSB) corresponds to 189 V/2^7 = 1.47 V in the power stage. In this case, the analog-to-digital converter gain, $K_{A/D,}$ is 85.3. The reference value of the clamp voltage control, $V_c^*(t) \times H_1 = 1.5$ V, can be implemented as $V_c^*[n] = 010000000_{(2)}$ in an 9bit 2's complement word. However, $V_c^*[n]$ is extended to be $0010000000_{(2)}$ in a 10bit 2's complement word to prevent overflow or underflow.

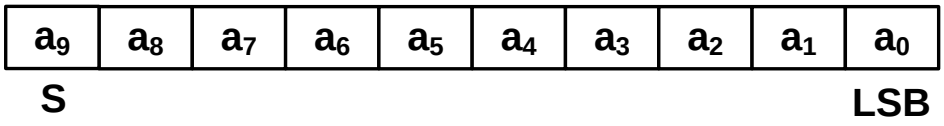


Figure 6.11. A 10bit-2's complement word. (S: sign bit, LSB: least significant bit)

Since the FPGA board has a 40 MHz oscillator, 40 MHz is used as the base clock for the digital system. The control signal of each A/D converter uses a 20 MHz clock. The sampling frequency of each A/D converter is 70 kHz. The block diagram shown in Figure 6.12 is a sampled-data system for the control loop of the clamp capacitor voltage (V_c).

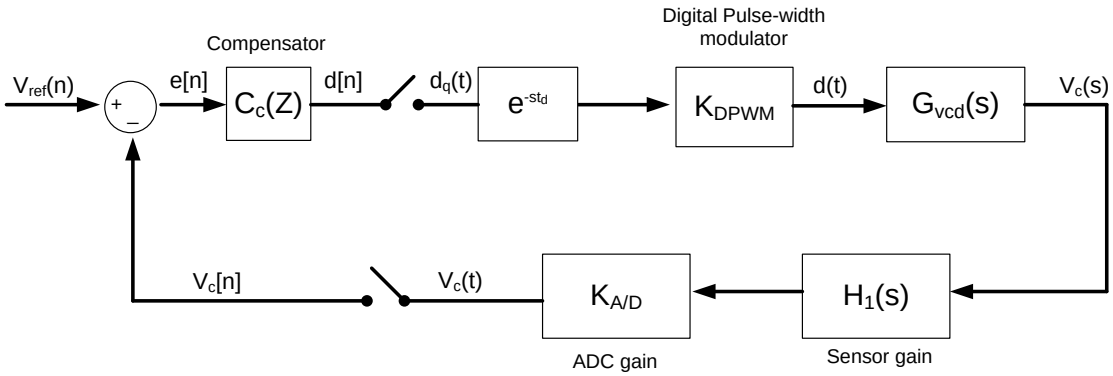


Figure 6.12. Block diagram of the sampled-data system for control of V_c.

For the digital pulse-width modulator (PWM), a signed 10 bit-counter (in a 2's complement format) is implemented to generate a 70-kHz signal using a 40-MHz base clock. In this scheme, the digital-PWM gain, $K_{DPWM,}$ can be selected as 576. However, this selection of K_{DPWM} must avoid the limit-cycling problem [33, 35, 38].

The first condition for avoiding the limit-cycling problem is that the 1 LSB variation (denoted as q_{DPWM}) of the digital-duty cycle should not give a variation of the controlled output (here, $V_c(t)$) in steady state. The quantized output value can be denoted as q_{ADC}. If the transfer function of the duty cycle (D(t)) to the output voltage ($V_c(t)$) is defined as $G_{Vcd}(s)$, the dc gain can be represented as G_{Vcd0}. Hence, the necessary condition for the elimination of limit cycling is presented in Equation (85) and (86). The chosen integrator gains, (K_I), are presented in Table 13. Since these inequalities (85), (86) are satisfied in the selection of the ADC, DPWM resolutions, and the integrator gain (K_I), the limit cycling oscillation can be avoided. In Figure 6.12, $C_c(z)$ is a discrete compensator that corresponds to C(s) in the continuous time domain.

$$q_{DPWM} \times G_{Vcd0} < q_{ADC.} \tag{85}$$

$$K_I \times G_{Vcd0} < 1 \tag{86}$$

The control loop of the output voltage (V_o) is illustrated in Figure 6.13. The sampled-data system consists of the transfer function ($G_{V_c\phi}(s)$), sensor gain (H_2), analog-to-digital converter gain ($K_{A/D}$), compensator gain (D(z)), digital-phase shifter gain ($K_{d\phi}$), and the time delay ($\exp(-sT_d)$).

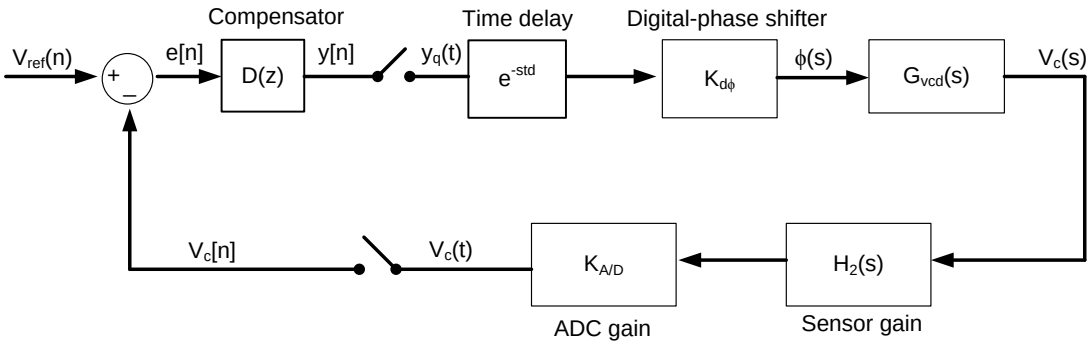


Figure 6.13. Block diagram of the sampled-data system for control of V_o.

In Section 6.2.2, the compensators were designed in the continuous-time domain. For digital-control implementation, the compensators should be discretized. In this design, the Backward-Euler method is used to discretize the integrator. In the sampled-data system of Figure 6.12, $C_c(z)$ corresponds to a discrete-PI compensator of C(s). The discrete PI regulator is formulated using Equations (87)-(89).

$$\text{Integral part: } C_{cI}[n] = K_I T_s \times e[n] + C_{cI}[n-1] \tag{87}$$

$$\text{Proportional part: } C_{cp}[n] = K_p \times e[n] \tag{88}$$

$$\text{Output of PI compensator: } d[n] = C_{cI}[n] + C_{cp}[n] \tag{89}$$

Based on Equations (87)-(89), the detailed structure of the discrete-PI compensator is illustrated in Figure 6.14. The discrete-PI compensator has an error input,

e[n], and an output, d[n]. The parameters K_I and K_P are obtained from the parameters of the continuous compensator.

The compensator D(z) has a similar form to $C_c(z)$. The implementation uses an anti-windup scheme to prevent saturation of the integrator. The anti-windup scheme is not illustrated in the block diagrams. The resulting parameters used in the experiment are given in Table 13.

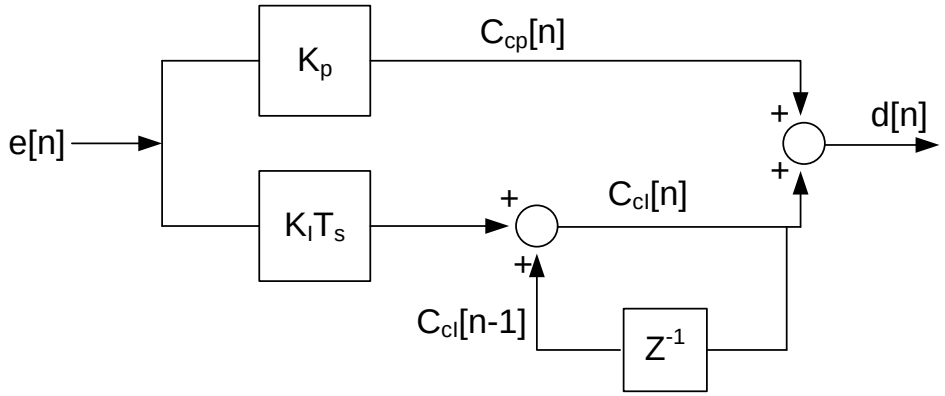


Figure 6.14. Discrete-PI compensator in a Backward-Euler method.

Table 13. Gains of compensators for the voltage loops.

Compensator	Gain	Value
$C_c(z)$ in T_1 loop	K_P	2
	$K_I \times T_s$	0.01
D(z) in T_2 loop	K_P	6
	$K_I \times T_s$	10

6.3.2. Digital-pulse-width modulator (DPWM)

A digital-pulse-width modulator (DPWM) operates under principles similar to those of the continuous PWM method. The DPWM unit consists of a digital comparator with two inputs: an N-bit counter and an N-bit duty cycle from the compensator, $C_c(z)$. Figure 6.15 shows the structure of the DPWM block.

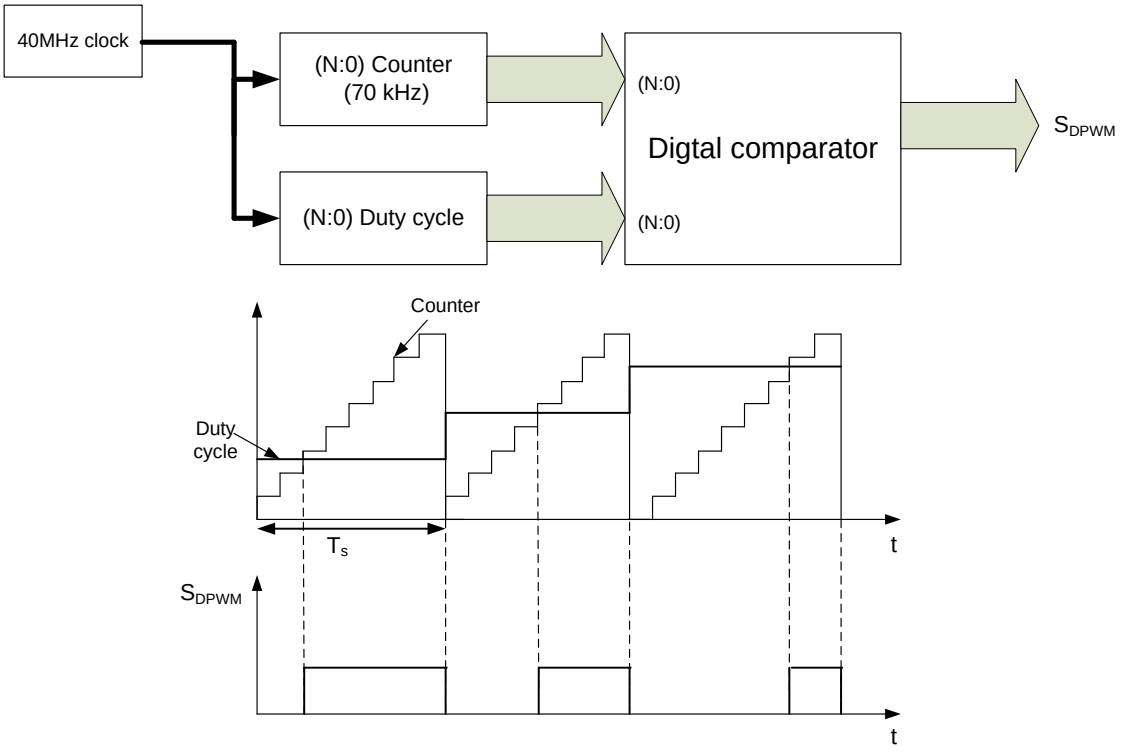


Figure 6.15. Digital-pulse-width modulator (DPWM).

A saw-tooth generation in a DPWM is implemented directly using an N-bit counter. In Figure 6.16, the DPWM block is verified in Modelsim software. The output of the PI regulator, plotted at the top of the figure, shows that the output of the PI regulator increases. This is expected since the integrator is summing the positive-error input, which is predefined for the test. A ramp signal is the output of a 70-kHz counter converted in an analog format. The third row shows the output of the comparator, the DPWM output signal. The fourth row shows the 40-MHz base-clock signal.

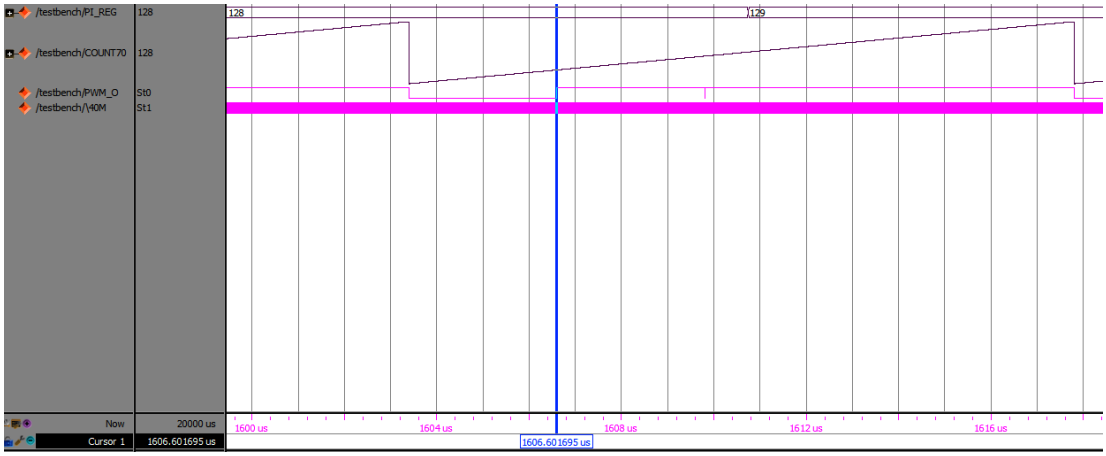


Figure 6.16. Simulation of the DPWM module in Modelsim.

(uppermost plot) PI regulator output (duty ratio),
(second from the top) 70-kHz counter analog output,
(second from the bottom) PWM output, (bottom) 40-MHz clock.

6.3.3. State machine

A state machine is used to generate the switching-signals. As shown in Figure 6.17 the state is based on inputs from the DPWM units and counters. In each state, the switching signals are defined as outputs to make a square wave using the H-Bridge for each switching period. The switching signals corresponding to each state are listed in Table 14.

The outputs of a state are defined as (Q_c,Q_1,Q_2,Q_3,Q_4) for Bridge1, and (Q_5,Q_6,Q_7,Q_8) for Bridge 2. In this definition, Q_x has a 1-bit value, for example, 0 or 1. The x in Q_x represents the device. In the beginning of the state machine, the state machine starts with the initial state S0. S0 has a state output of (01111), which turns on all of the switch devices except for the active-clamp switch. During this state, the dc inductor current increases with a positive slope.

At the rising edge of S_{DPWM}, the state changes to S1. S1 provides dead time is given to the switch devices in the H-Bridge. With the completion of dead time, the switch

devices in the diagonal pair and the clamp circuit are turned on in the S2 state (11100). The S2 state ends with the rising edge of a timer, which has a 70-kHz-clocking signal, and the state changes to the S3 state (01100), in which dead time is given to the switching devices. The S3 state continues until the timer for dead time ends. The S4 state (01111) starts with the completion of dead time. In the S4 state, all of the switch devices in Bridge 1 are turned on, except for the active-clamp switch. After the S4 state, the same procedure repeats.

In Bridge 2, output signals of the time-delayed states are generated by using the phase-shifting block. Applying the switching patterns in Table 14 creates square-wave voltages. Figure 6.18 plots the simulation of the state machine using Modelsim. The top plot shows the counter output at 70 kHz. The second plot shows the output (100) of the PI regulator. The third plot shows the present state. The fourth plot shows the rising edge of the PWM output. The rising edge of a signal can be extracted by a delay line rising-edge detector. The fifth plot shows the DPWM output. The bottom plot shows the 40-MHz-base clock.

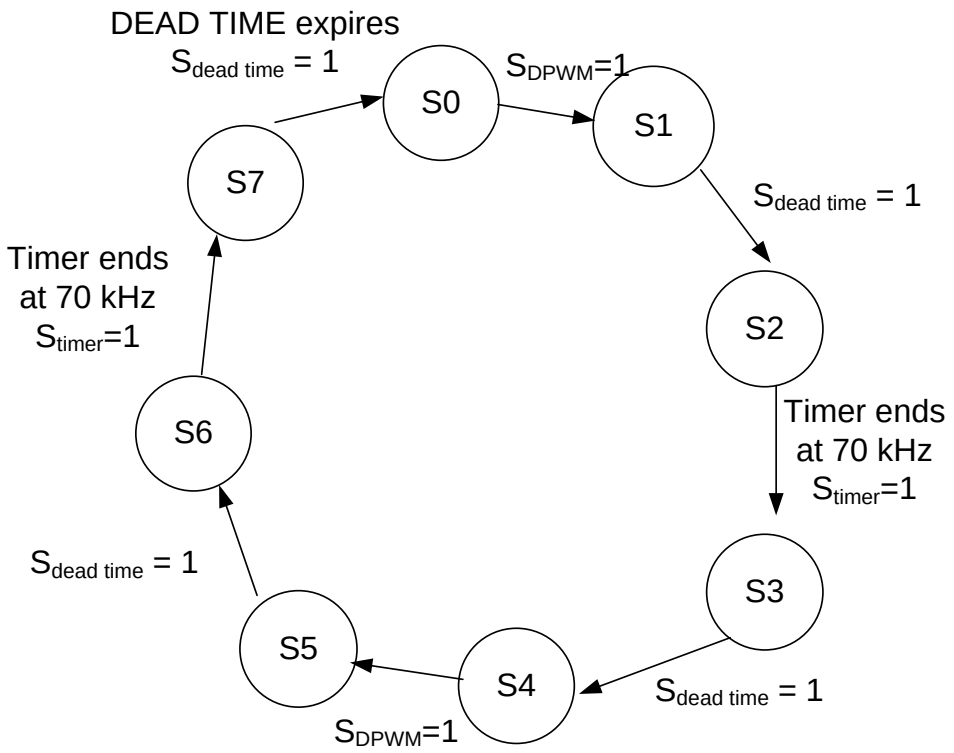


Figure 6.17. Simplified block diagram of the state machine in Bridge 1.

Table 14. The switching state of Bridge 1 and Bridge 2.

State	S0	S1	S2	S3	S4	S5	S6	S7
Bridge1	01111	01100	11100	01100	01111	00011	10011	00011
Bridge2	0110	0100	1100	1000	1001	0001	0011	0010

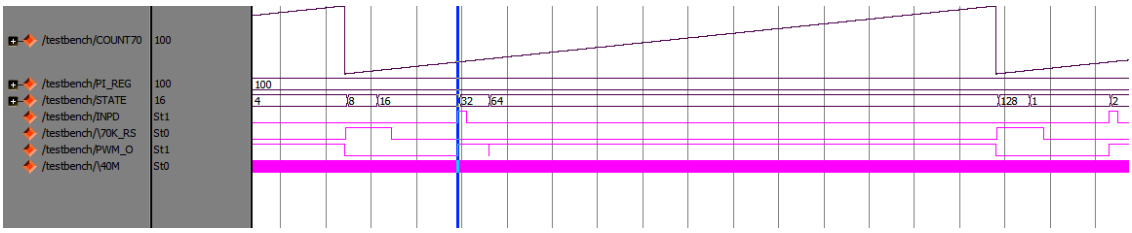


Figure 6.18. Simulation of the state machine.
(uppermost plot) 70-kHz counter, (second from top) PI regulator output, (third from top) state, (third from bottom) rising edge of S_{DPWM} (second from bottom) S_{DPWM} (bottom) 40-MHz clock.

6.3.4. Digital-phase shifter

A phase-shifting function is used to generate the switching signals for Bridge 2. Figure 6.19 illustrates the concept of a digital-phase shifter using a circular buffer. The input is the current state of Bridge 1. Figure 6.19 shows the current state of Bridge 1 being written to S2, as indicated by the writing pointer. As the writing pointer moves to the right at 40 MHz, the next state of Bridge 1 is written to the new location of the writing pointer.

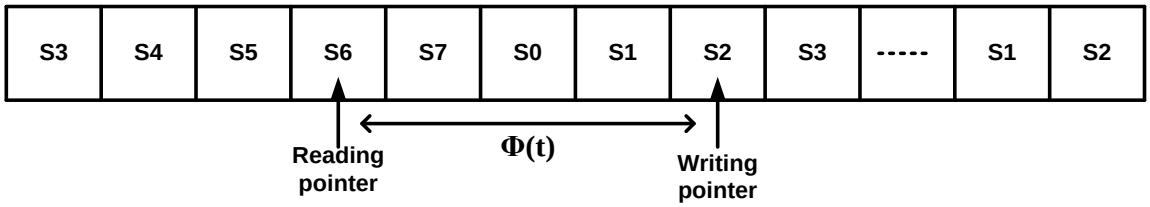


Figure 6.19. Phase shifter using a circular buffer.

The reading pointer indicates the location of the state that has to be applied to the switching devices in Bridge 2. The governing equations between the reading and writing pointers are in Equations (90) and (91).

$$\text{Reading address } (R_{ad}) = \text{Writing address } (W) - \emptyset(t) \quad \text{for } \emptyset(t) < W \tag{90}$$

$$\text{Reading address } (R_{ad}) = \text{Ram depth } (D_{ep}) + \text{Writing address } (W) - \emptyset(t) \quad \text{for } \emptyset(t) > W \tag{91}$$

In Equations (90) and (91), $\emptyset(t)$ is the time shift between the reading address and the writing address. The Ram depth (D_{ep}) is illustrated in Figure 6.20. The phase-shifting algorithm is implemented using a dual-port ram, which is generally used to separate the reading and writing process in the memory. In the phase shifter, the addressing is made with a K_{addr} bit counter. The writing address increases as the K-bit counter increases in

the 40 MHz clock speed. The operation of the dual-port ram follows the concepts of the circular buffer shown in The reading address is calculated using Equations (90) and (91). In the architecture, the outputs of the dual-port ram are the phase-shifted state and the gating signals for Bridge 2.

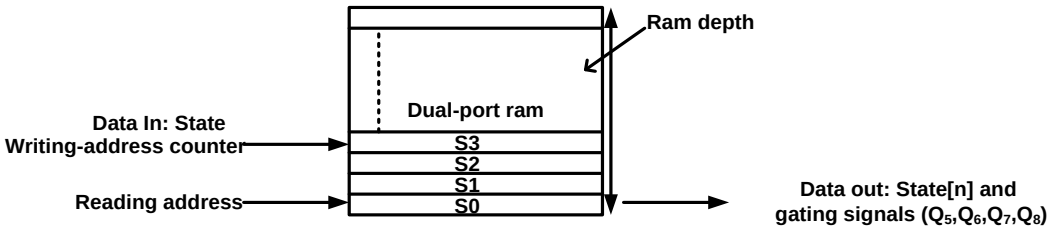


Figure 6.20. Architecture of the phase shifter using dual-port ram.

In Figure 6.21, the simulation results of the phase shifter are plotted using the Modelsim software. In the plot, the value of the phase-shift is shown as 140. This value is converted to 140 * 0.025 μsec= 3.5 μsec in a 40-MHz clock. In the plot, it is observed that a state input (state) is shifted from the state input. The plot at the bottom shows the output of the phase shifter.

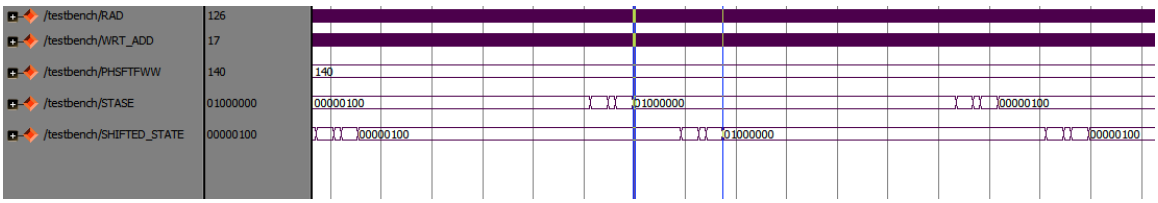


Figure 6.21. Simulation of the digital-phase shifter in Modelsim software. (top plot) RAD: Reading address, (second from top) WRT_ADD: Writing address, (third from top) the amount or the phase-shift, (second form bottom) a state input, (bottom plot) an output of the phase shifter.

6.4. Methods for Preventing Transformer Saturation

6.4.1. The problems of dc currents in high-frequency transformers

Figure 6.22 shows a B-H curve and magnetizing-current waveforms, with and without dc flux, based on sinusoidal excitation. If the average value of the flux is zero, and the magnitude is less than the saturation level, the magnetizing current is sinusoidal, as shown in Figure 6.22(a). If the flux is not balanced, and the flux magnitude is higher than the saturation level, as shown in Figure 6.22(b), the magnetizing current shifts to the nonlinear (saturation) region. This reasoning can be applied to switch-mode power converters with galvanic isolation operating at high-switching frequencies. For switch-mode power-electronic converters consisting of an isolation transformer, high peak currents owing to transformer saturation are often observed.

In self-commutated converter applications, 60 Hz-transformer saturation has been a problem. The converter's transformer experiences dc saturation when inrush currents flow from the power system. A proposed method to reduce or prevent dc components in the transformer by adjusting the gating signals of the converter is presented in [39]. For high-frequency power electronic applications, some methods are proposed using PWM signal-perturbation for single-ended dc/dc converters. These methods modify the PWM signals to balance the dc magnetization of the high-frequency isolation transformer. In [40], the peak–transformer current is limited in order to prevent the saturation of a transformer under heavy-load conditions.

For the dual-active switching converters, transformer saturation is more problematic than single ended converters. Gating signals are simultaneously applied on

both the primary and secondary sides of the Dual-Active Bridge (DAB) converter. Typically in such dual-active-mode converters as the DAB, the gating signals on both sides expose the transformer to more frequent dc currents. However, in the DAB converter, the dc currents have been avoided by strictly requiring 50 % square wave excitation on both the primary and secondary sides.

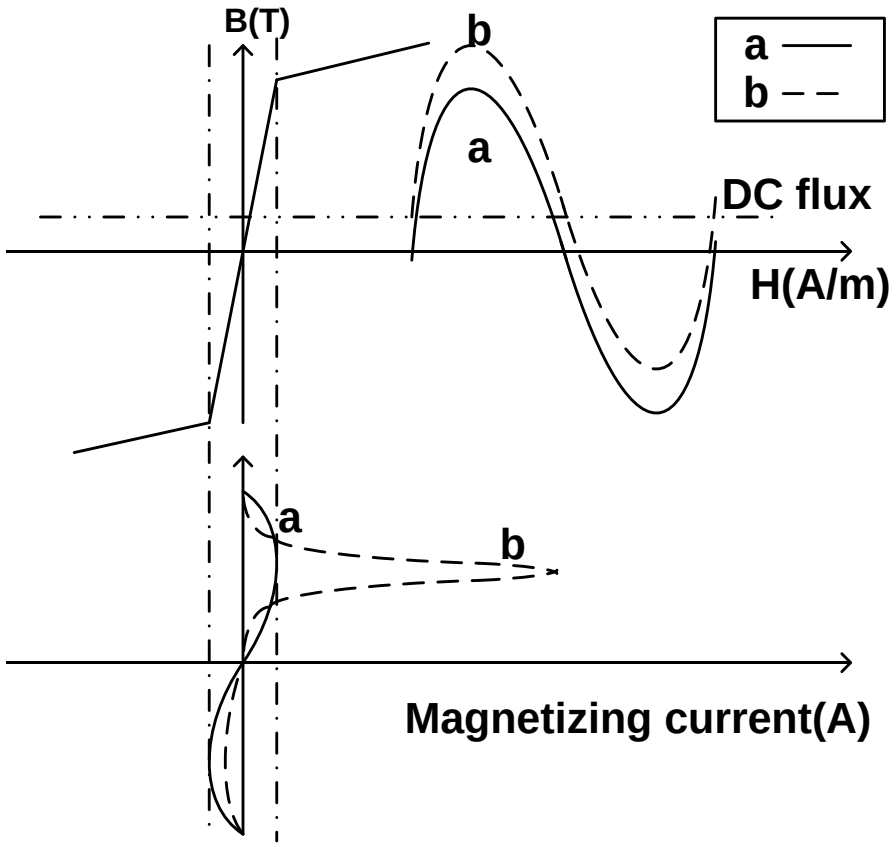


Figure 6.22. B-H curve and magnetizing current.
(Trace a) is for the case without DC bias (trace b) has DC bias.

In the DAB[3] converter, dc currents are problematic because the duty ratio changes on both sides of the transformer, as a result of the active switching of non-ideal-semiconductor devices [41]. Hence, the transformer can be exposed to dc offsets or dc averages in volt-seconds on both sides of the transformer.

The dc average of the volt-seconds can cause high-dc currents since the winding resistance is very small. However, the dc effects are damped rapidly on the other side of the transformer because the induced voltage is proportional to the derivative of the flux linkages. The same reasoning applies when the source voltage is assumed to be located on the other side. Hence, an imbalance of volt-seconds on any side will cause dc magnetization, which causes dc currents, but the dc impacts are not seen on the other side. This fact necessitates the development of a methodology to sense and prevent dc currents on both sides of the transformer.

6.4.2. Methodology

The prevention of dc currents on both sides of the transformer is an important issue for PWM-converter controls. Hence, this work proposes a method that prevents dc currents in the transformer. The block diagram of the control scheme is shown in Figure 6.23.

Since dc currents can flow on any side of the transformer, current sensing should be done on both sides. Each sensed current is converted to a digital signal by an A/D converter operating with a 70 kHz sampling frequency. Hence, the functional-control loops (Controllers 1 and 2 in Figure 6.23) are added to detect and prevent transformer dc currents. In Controllers 1 and 2, the dc-offset currents are extracted. To measure the dc offsets of the transformer currents, the sampled currents are summed at every half cycle. The dc current is measured by Equation (92).

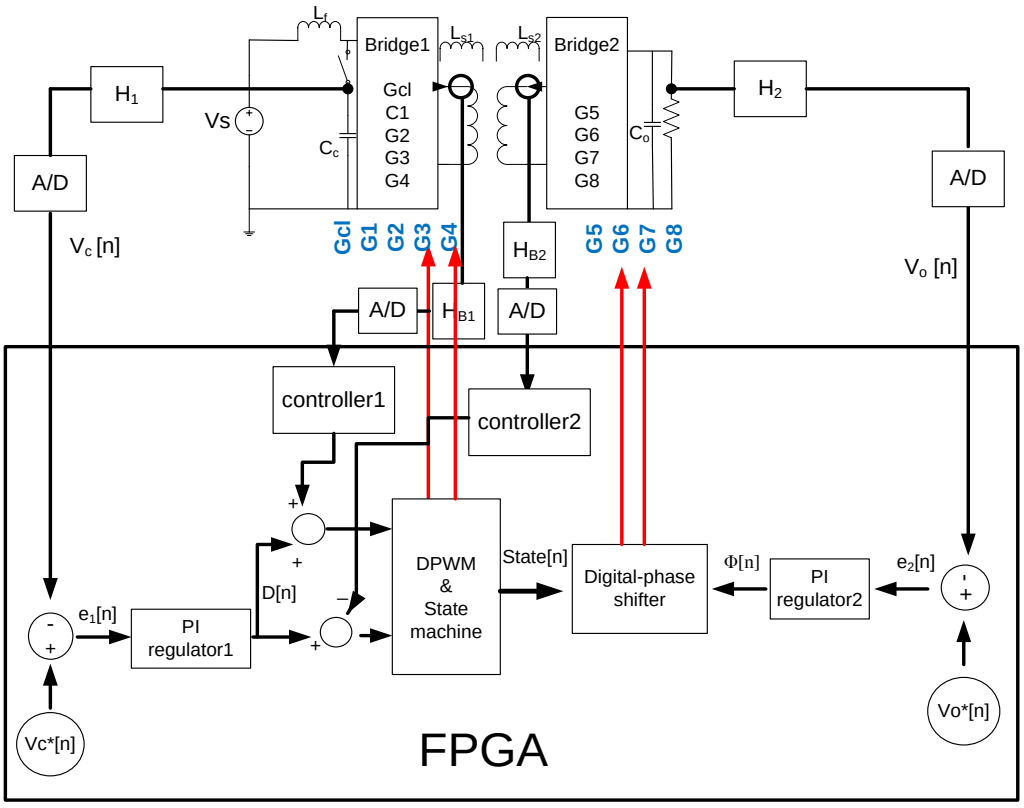


Figure 6.23. Control method to prevent dc-currents.

$$I_{dc}[n] = i[n] + i[n-1] \tag{92}$$

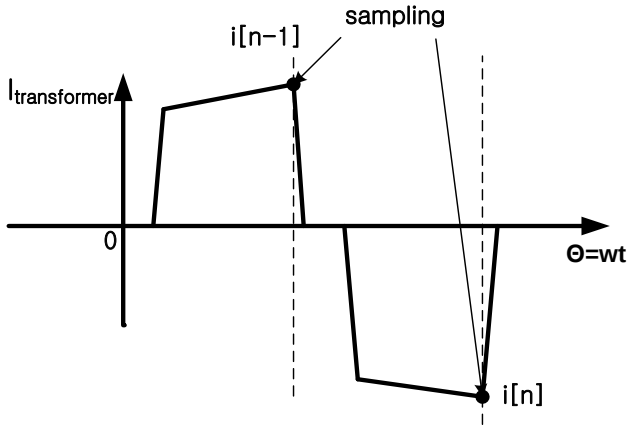


Figure 6.24. Current sampling to measure the dc-offsets.

The extracted dc offsets are processed by a compensator and are finally supposed to be zero. Figure 6.25 illustrates a detailed-block diagram of Controllers 1 & 2, which includes a dc-current extraction function and the PI regulator. Finally, the output of this control loop, P[n], is added to or subtracted from the output signal, D[n], of the clamp-voltage controller to adjust the volt-seconds.

Figure 6.26 shows how the adjustment of the volt-seconds works to remove the dc currents. If a negative dc-offset current is detected in Bridge 1, the duty cycle for the first-half cycle should be increased in Bridge 1 to generate positive volt-seconds.

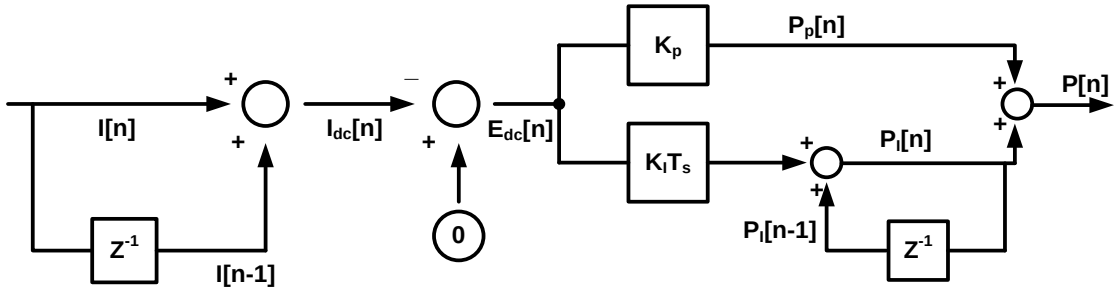


Figure 6.25. Block diagram for Controllers 1 & 2.

As shown in Figure 6.26 (a) & (c), D1[n] originates from D[n], an output of the V_c controller for the interval of the first half cycle ($nT_s < t < 0.5T_s + nT_s$). The perturbed duty ratio D1[n] equals D[n] $-\delta$ (δ>0) and is compared with the sawtooth signal of the counter to move the state to the next state. In contrast to the interval of the first half cycle, D1[n] is not perturbed in the next-half cycle($nT_s + 0.5T_s < t < (n+1)T_s$), in which D1[n] equals to D[n]. As a result of this adjustment, the volt-seconds impressed across the windings have a positive value.

For the positive-dc current flowing in Bridge 2, the adjustment of the duty cycle in Bridge 2 should make the volt-seconds negative. Hence, the positive-dc current will be

reduced. The adjustment of duty signals for Bridge 2 (B_2) is shown in Figure 6.26 (b) & (D). The duty ratio for Bridge 2 is perturbed only for the next-half interval ($0.5T_s+nT_s < t < (n+1)T_s$). Figure 6.26(e) shows the DPWM output of Bridge 2 when there is a phase-shift angle, $\emptyset(t)$.

Simulations in Saber software were performed to verify the proposed dc-current prevention method. The control methods are demonstrated experimentally in the next section. Figure 6.27 shows the circuit used to simulate the injection of an average-dc voltage into the transformer. Figure 6.28 (a) and (b) show the simulation results without and with the dc-current-prevention schemes, respectively. In Figure 6.28(a), dc currents are observed on the primary side of the transformer, whereas no dc current exists in Figure 6.28(b).

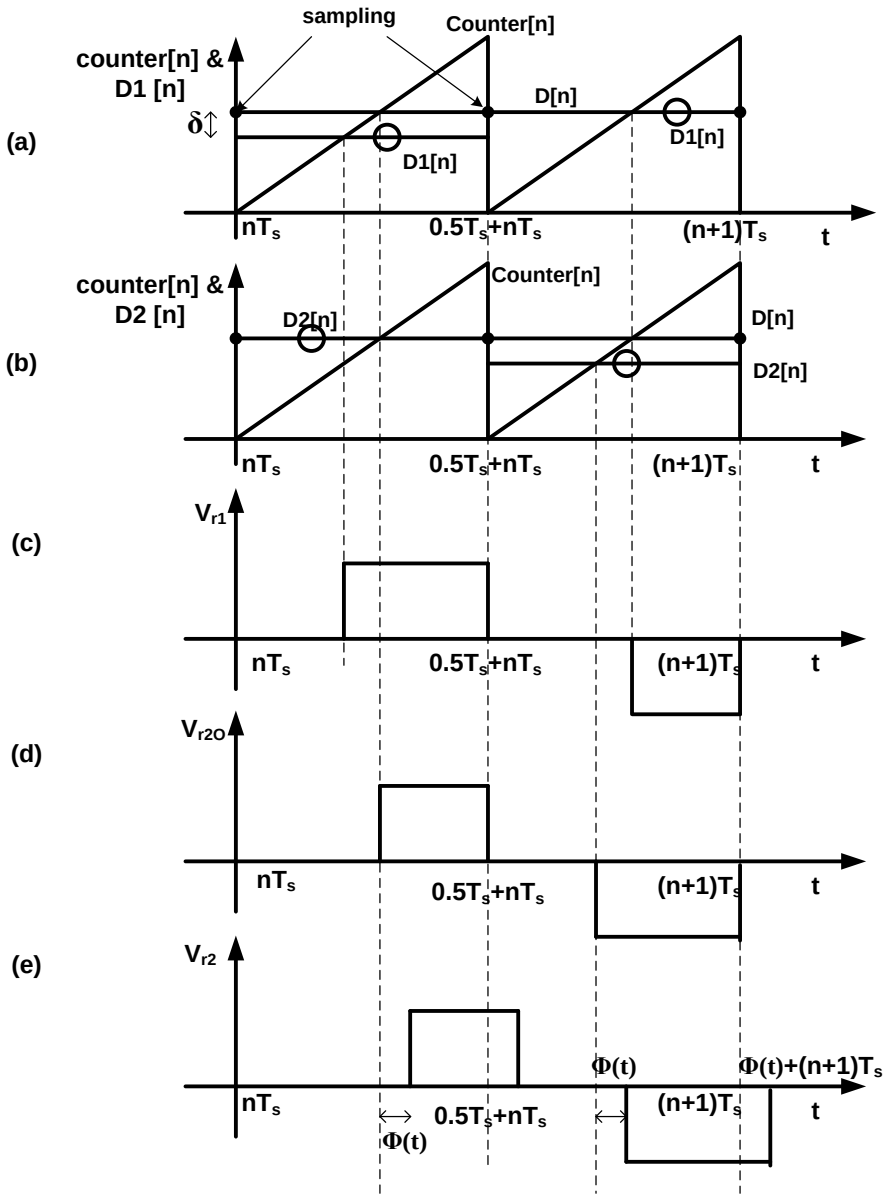


Figure 6.26. Perturbed PWM outputs.

(a) Counter, duty ratio D[n], and adjusted duty ratio, $D_1[n]$.
(b) Counter, duty ratio D[n], and adjusted duty ratio, $D_2[n]$.
(c) Transformer voltage V_{r1}.
(d) Adjusted-transformer voltage, V_{r2o}, which is not phase-shifted.
(e) V_{r2}, adjusted and with a phase-shift angle.

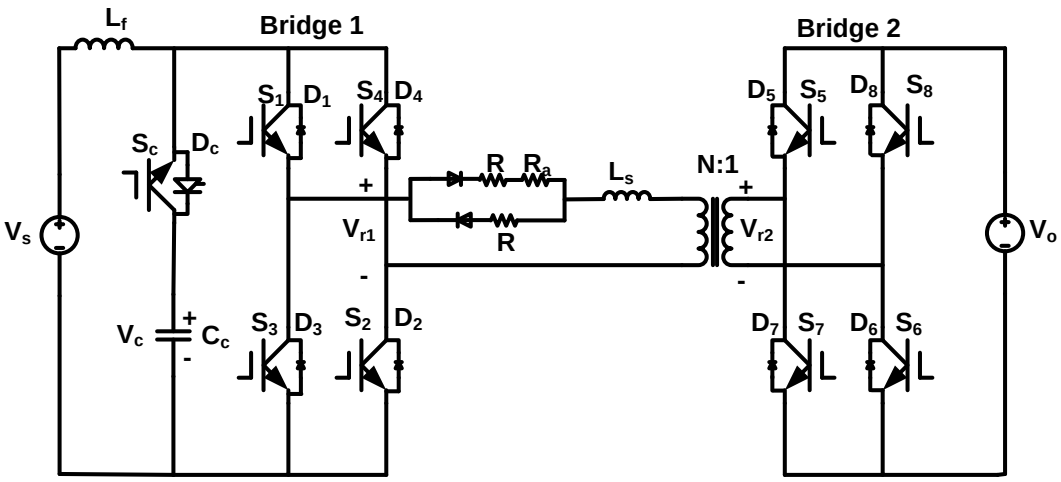
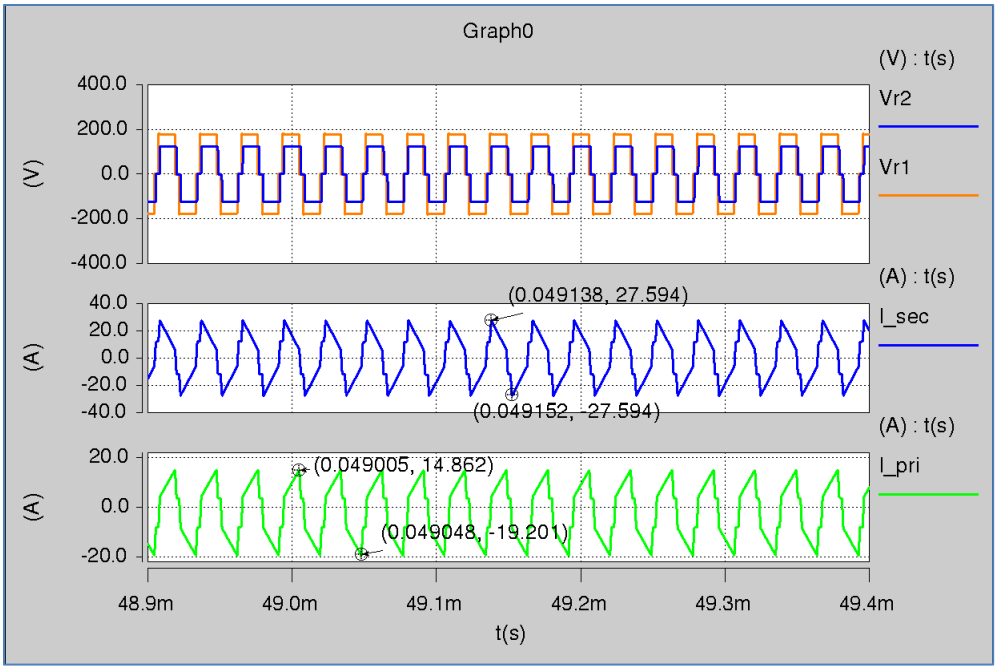


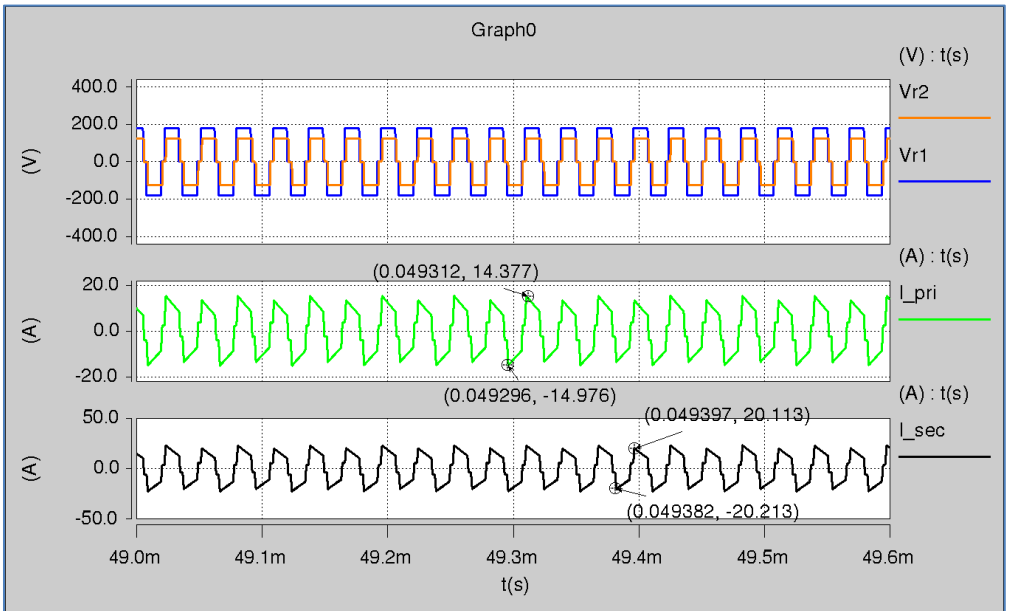
Figure 6.27. Power stage with dc-injected transformer.



(a) without the dc prevention method

Figure 6.28. Plots of the simulation for testing dc prevention method.

"Figure 6.28 . Plots of the simulation for testing dc prevention method." continued



(b) with the dc prevention method.

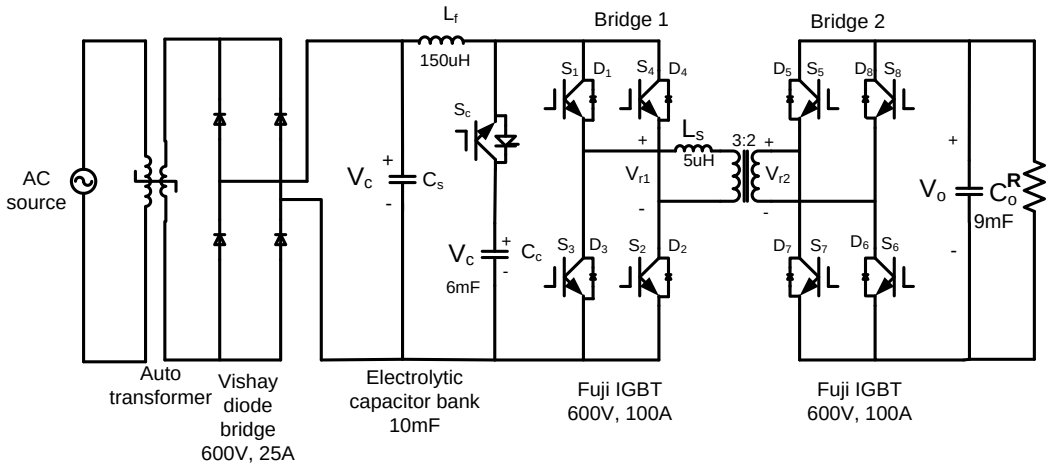
Figure 6.28. Plots of the simulation for testing dc prevention method. (Uppermost) V_{r1} and V_{r2}, (Middle) $I_{\_pri}$, (bottom) $I_{\_sec}$.

6.5. Experimental Validations

6.5.1. Experimental unit

A 10 kW rated unit was built and tested in the lab. Figure 6.29 shows an illustration of the experimental unit and a picture of the power stage. Since the components in the experimental circuit are not optimized for performance, only the parameters of the components are depicted in this chapter. The power stage is designed to operate at a 35 kHz switching frequency. The 220 V AC source is connected by an auto transformer.

(a)



(b)

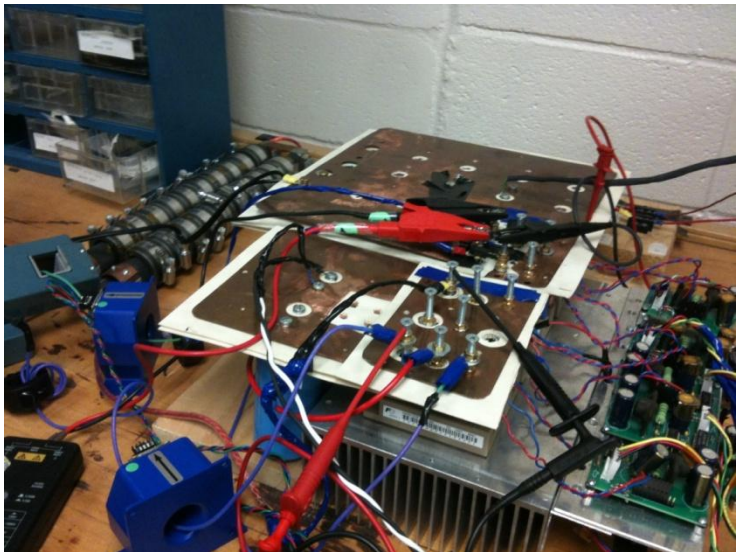


Figure 6.29. Experimental unit.
(a) schematic, (b) picture of the power stage.

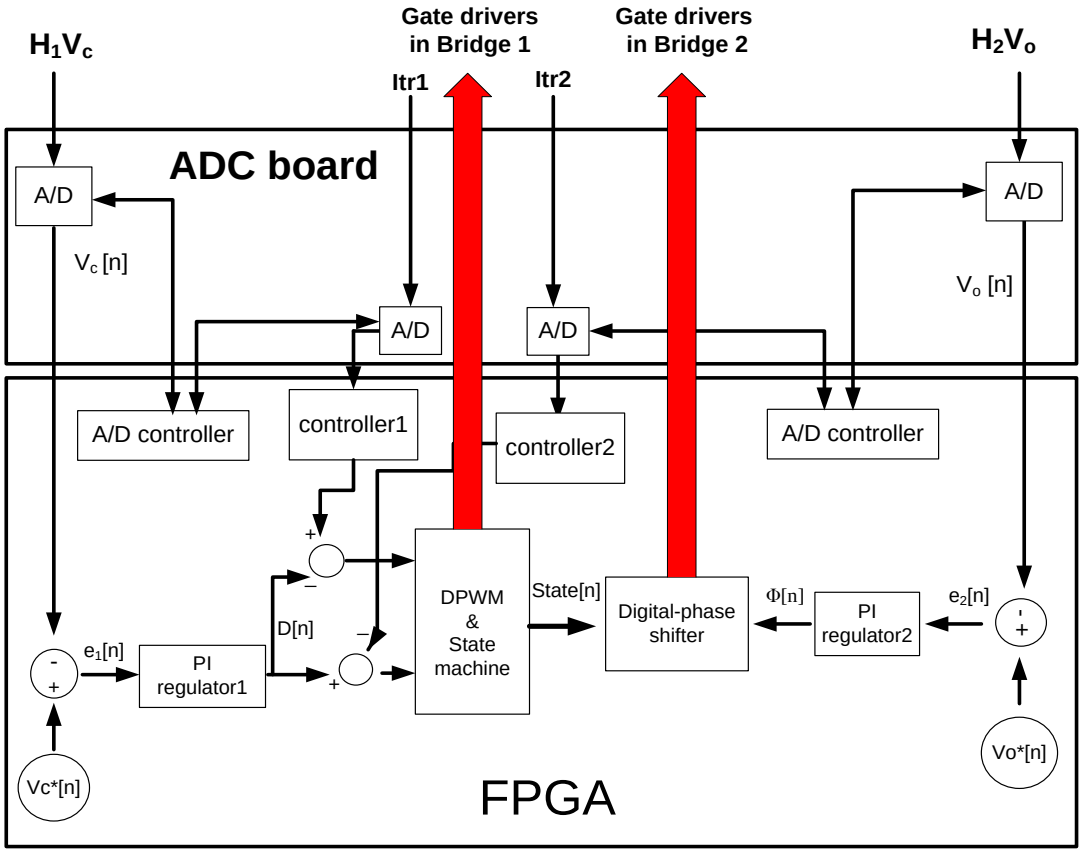
A single-phase diode-bridge is used as a rectifier. Multiple electrolytic capacitors are used to obtain a dc-link capacitor bank with sufficient current rating. The switch devices used in the power stage are Insulated Gate Bipolar Transistor (IGBT) devices. The Fuji 600 V/100 A IGBT, model no. 2MBI100TA060-50, was selected for all switch devices. Table 15 lists the ratings of the components used in the experimental setup.

Table 15. Components in the experiment

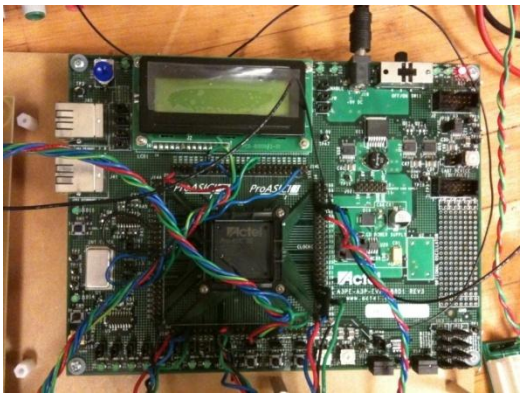
Component	Value	unit	Description
Voltage source (AC)	220	V	Constant ac voltage
Auto transformer	0~220	V	6 kVA
Diode bridge	600/20	V/A	Voltage and current ratings
C_s	10	mF	DC-link capacitor for V_s
C_c	6	mF	Clamp capacitor
C_o	9	mF	Filter capacitor for V_o
L_f	100	uH	Filter inductor
L_{sp}	5	uH	Series ac inductor
L_{ss}	5	uH	Series ac inductor
Transformer	15	KVA	High frequency transformer
R	6.7/10.3/20	ohm	Load resistance
S_c,S_1-S_8	600/100	V/A	Fuji 2MBI100TA060-50 IGBT
Controller	n/a	n/a	FPGA(ACTEL 1500E)

Figure 6.30 shows the controller setup. Figure 6.30 (a) shows an illustration of the control boards, emphasizing the signal conditioning and processor components. The signal-conditioning board primarily provides analog-to-digital conversion (ADC) and signal conditioning. The arrows show the directions of the I/O signals (input/output interface). Figure 6.30 (b) shows a picture of the FPGA board (ACTEL ProAsic1500E) used for control implementation. Figure 6.30 (c) shows a picture of the signal-conditioning board, which has ADCs and signal-conditioning circuits.

(a)



(b)



(c)

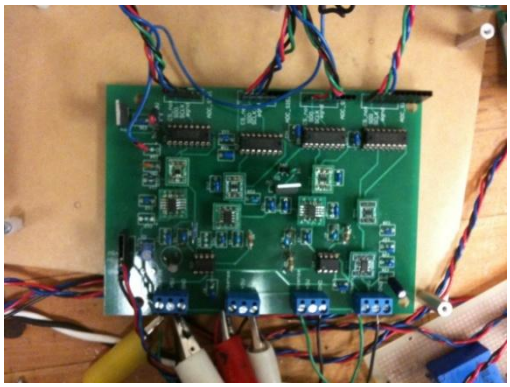


Figure 6.30. Controller setup.
(a) Signal-flow diagram, (b) FPGA board, (c) ADC board.

6.5.2. Multi-modal test schemes

In the experiment, two modes of operation were defined in the controller. One is full-bridge mode. The other is DAB^3 mode. This multi-mode operation focuses on how to

avoid high-peak currents during the transient conditions. If the converter is operated with components that have long transients, such as batteries, the operating mode of the converter should be selected with respect to the voltage levels, V_c and NV_o.

The mode of operation is defined by the voltage levels of the clamp capacitor (C_c) and the output capacitor (C_o). When the level of V_c differs significantly from the level of $N \times V_o$, the converter should not be operated in a dual-active switching mode to avoid high-peak currents, which cause very high losses. Figure 6.31 shows the proposed multi-modal operation scheme.

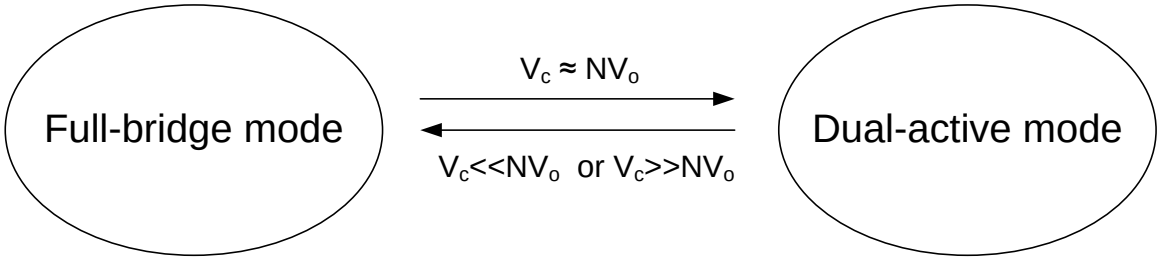


Figure 6.31. Block diagram of multi-modal operation.

Full-bridge mode operates as follows. When the voltage levels of V_c and NV_o differ, the converter should be operated in a full-bridge mode. In full-bridge mode, the switching devices in Bridge 2 are turned off so that they are used as a diode bridge. After the filter capacitor (C_o) is charged to a critical level, at which point the switching devices do not have high currents, the control strategy switches to DAB^3 mode. For transient conditions, the full-bridge mode helps prevention of dc magnetization of the transformer. Under DAB^3 mode, the converter-switching signals are generated using the dual active-switching scheme.

6.5.3. Test results

Table 16 shows the test conditions under which the power circuit was tested. The reference voltages for V_c and V_o were fixed for the entire experiment. The clamp voltage reference was set to 189 V. The output voltage reference was set to 125 V. The switching frequency was set to 35 kHz. In this case, the DPWM frequency should be 70 kHz. The experiment was performed for a range of loads. Figure 6.32 to Figure 6.37 show the waveforms from the experiment, as captured with an oscilloscope.

Table 16. Test conditions for the experiment

	Value	Unit
Source voltage range (V_s)	125- 150	V
Clamp voltage (V_c)	189	V
Output voltage (V_o)	125	V
Load resistance	20,10.3, 6.7	Ω
Switching frequency (f_s)	35	kHz
Turn ratio of transformer	3:2	N_1:N_2

Figure 6.32 and Figure 6.33 were captured with a load of 20 Ω. For both V_s = 125 V and V_s = 150 V, the current waveforms can be controlled to be flat. The flat currents in the transformer result in low device ratings, as discussed in the previous chapters. In Figure 6.34 and Figure 6.35, the converter is operated with a load of 10.3 Ω.

Figure 6.36 and Figure 6.37 show the transformer waveforms with a load of 6.7 Ω. The plots show flat-top currents for both the 10.3 Ω and 6.7 Ω loads. The measured efficiency is 87-89 %. Since the air gap is used in the transformer, the magnetizing inductance becomes very small. Hence, high magnetizing current flows in the system. The increased magnetizing current increases both the conduction and the switching losses

in Bridge 1. As a result, the efficiency is low. Hence, optimization of the component design and selection is required to improve efficiency.

Next, the proposed dc-current prevention method was tested. Figure 6.38 shows the circuit used to inject dc-voltage into the experimental setup. The injection circuit is similar to the one used in simulation, as shown in Figure 6.27. The dc component is injected by unbalancing the voltage inputs to the isolation transformer. In the experiment, an average dc voltage was successfully injected. In the experimental setup, film resistances of R = 0.3 Ω are used to cause an average dc voltage. As a result, dc current flows in Bridge 1 of the transformer. Figure 6.39(a) shows waveforms without the dc-current prevention scheme. Figure 6.39(b) shows waveforms with the dc-current prevention scheme, removing the dc offset currents. Figure 6.39(c) gives more detailed plots of V_{r1},V_{r2} and $I_{transformer}$ with the dc-current prevention scheme when the conditions are V_s = 90 V, V_c = 120 V, V_o = 80 V.

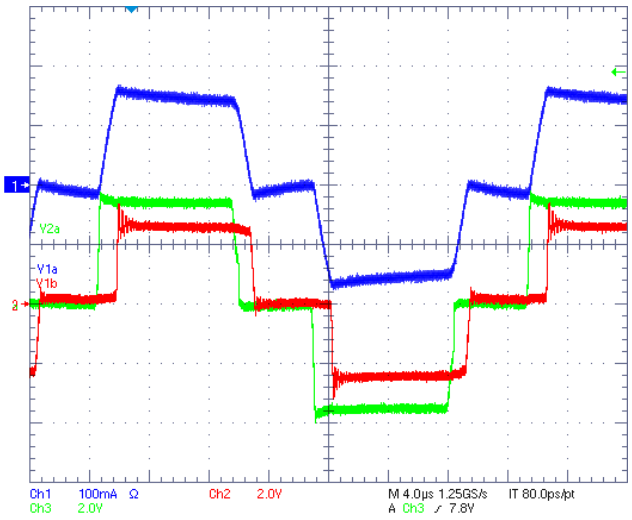


Figure 6.32. Plots of transformer waveforms, with V_s = 125 V and R = 20 Ω. (Blue) transformer current, (Green) transformer voltage (V_{r1}) in Bridge 1, (Red) transformer voltage (V_{r2}) in Bridge 2. Voltage: 100 V/div, current: 5 A/div

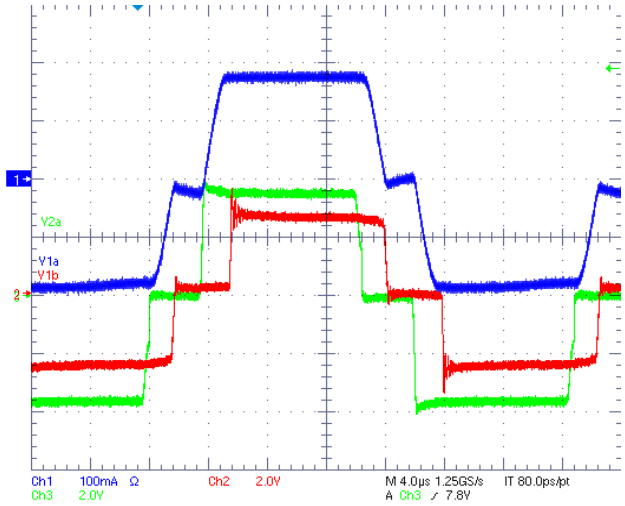


Figure 6.33. Plots of transformer waveforms with V_s = 145 V and R = 20 Ω. (Blue) transformer current, (Green) transformer voltage (V_{r1}) in Bridge 1, (Red) transformer voltage (V_{r2}) in Bridge 2. Voltage: 100 V/div, current: 5 A/div

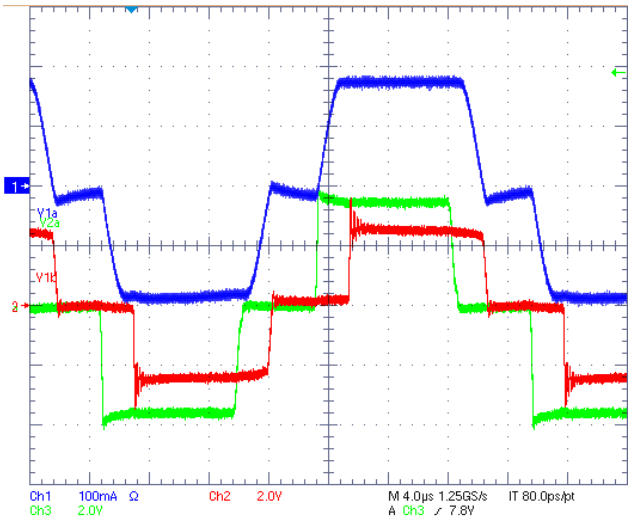


Figure 6.34. Plots of transformer waveforms, with V_s = 125 V, R = 10 Ω. Voltage: 100 V/div Current: 10 A/div

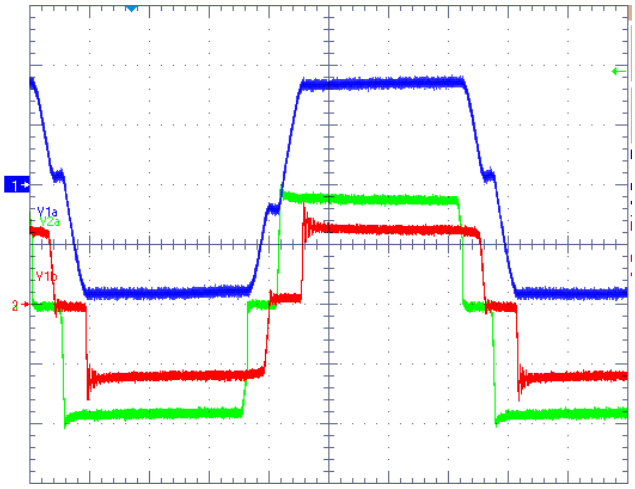


Figure 6.35. Plots of transformer waveforms, with V_s = 150 V and R = 10 Ω. Voltage: 100 V/div Current: 10 A/div

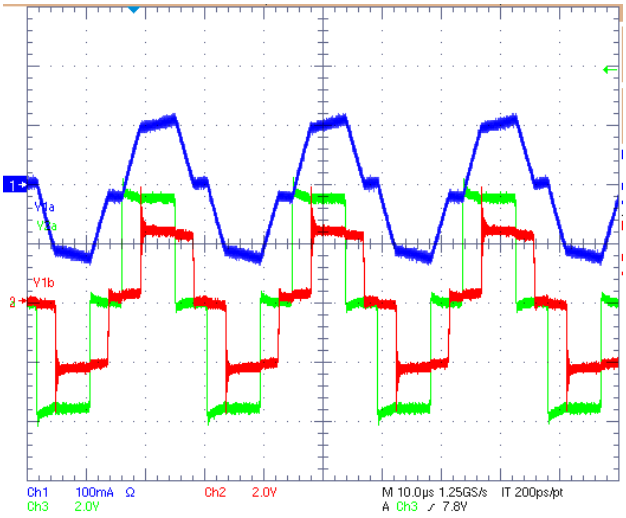


Figure 6.36. Plot of transformer waveforms, with V_s = 125 V, R = 6.7 Ω. Voltage: 100 V/div Current: 20 A/div

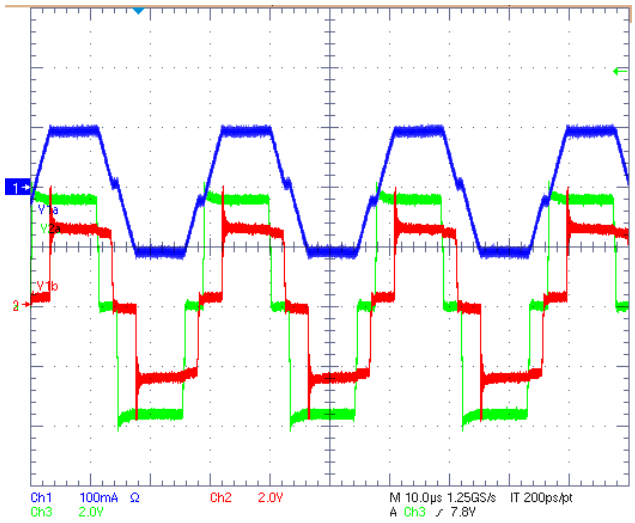


Figure 6.37. Plots of transformer waveforms, with V_s = 150 V and R = 6.7 Ω.
Voltage: 100 V/div Current: 20 A/div

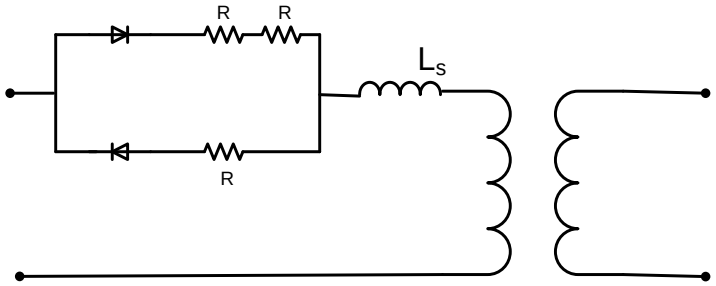
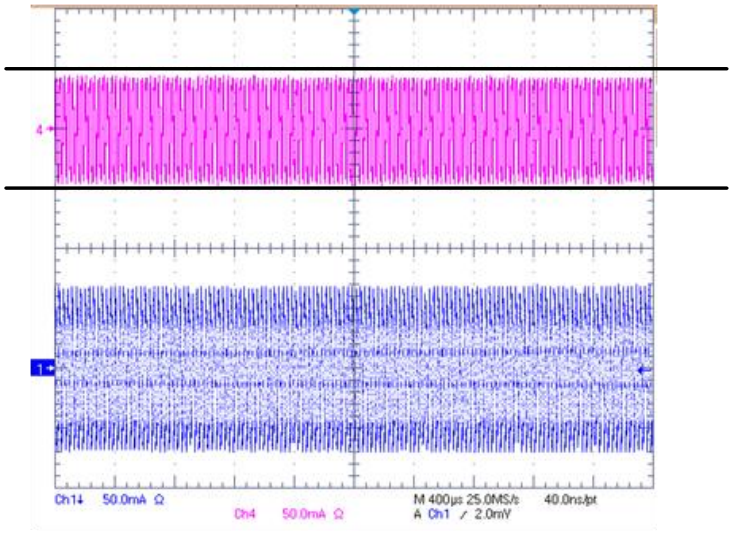
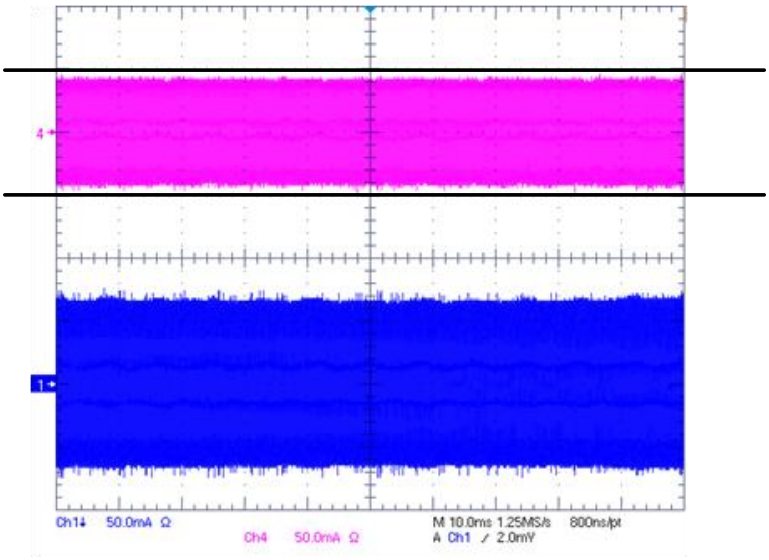


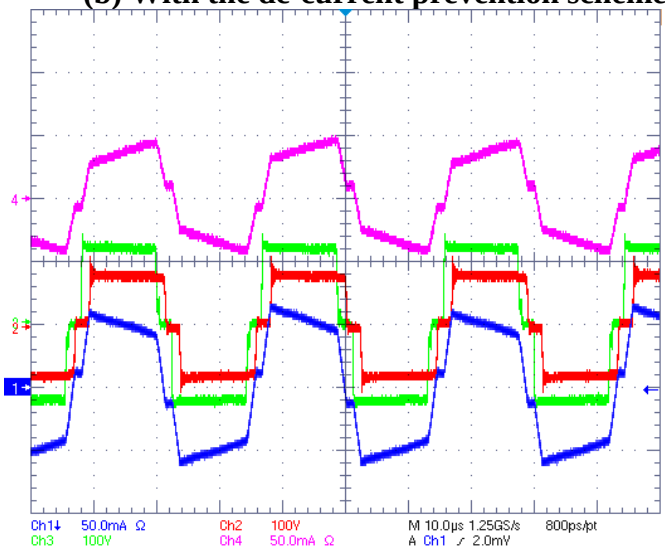
Figure 6.38. Injection of the dc voltage into the isolation transformer.



(a) Without the dc-current prevention scheme.
Pink: Transformer current in Bridge 1, Blue: transformer current in Bridge 2.



(b) With the dc-current prevention scheme.



(c) V_{r1}(green),V_{r2} (red), (pink) $I_{transformer}$ in Bridge 1 with the dc-current prevention scheme, (blue) $I_{transformer}$ in Bridge 2

Figure 6.39. Test results of the dc prevention methods.
Voltage: 100 V/div, current: 10 A/div

6.6. Chapter Summary

This chapter presented the development of the DAB^3 controller, the implementation of the controller using an FPGA, and the experimental validation of DAB^3 functionality.

The control objective is to regulate load power while controlling device currents to have minimum stresses. In the DAB^3 converter, transformer dc saturation is problematic. Hence, a control scheme is also implemented to prevent dc currents on both sides of the transformer.

The second focus of this chapter is the implementation of the controller. The switching frequency of Bridge 1 is relatively high. Thus, a low controller propagation delay is required. Hence, an FPGA was used to realize the fast control loop. The FPGA implementation requires low-level designs using Verilog-HDL. Due to the low-level design, a number of functional blocks were developed, including DPWM, state machines, digital-phase shifter, and PI regulators.

Finally, the experimental results demonstrated the proposed DAB^3 converter and related controller schemes at the multi-kW level. A multi-mode operating procedure was developed and tested to demonstrate black-start capability. Operation of the dc-current prevention scheme was demonstrated.

The main contributions of this chapter include:

1. A controller design and implementation based on digital hardware.
2. The proof of the DAB^3 concept, flat-top currents, by the developed controllers.
3. A proposed dc current prevention method.
4. Experimental validation of the dc current prevention method.

CHAPTER 7

CONCLUSTIONS AND RECOMMENDATIONS

7.1. Summary

In Chapter 1, the thesis began with an introduction to high-power bi-directional dc/dc converters. Applications identified for these converters included energy-storage systems. In energy-storage systems, the terminal voltage of the voltage source varies widely. Hence, the bi-directional dc/dc converter should have capability to regulate the output voltage for wide variations of the source voltage. The challenges in designing high power bi-directional dc/dc converter are reducing parasitic effects, low total-device rating, high efficiency, and high-power density.

Chapter 2 presented a survey of previous work. A resonant dc/dc topology was identified as widely used for high-power conversion. The resonant dc/dc topology has low switching loss in high switching frequencies, but high device ratings. A full-bridge converter is introduced for high-power applications. This topology has problems involving parasitic elements. The Dual-Active Bridge converter was discussed. In the DAB topology, a system's parasitic elements are effectively used in transferring power. Hence, the problems of parasitic elements are resolved. However, the total-device rating (TDR) is high if the converter is operated at wide input/output ranges. Other modifications of full-bridge and DAB topologies were discussed. The other DAB topologies still have problems in terms of device stresses.

In Chapter 3, the concept of a high-power bi-directional dc/dc converter with controlled-device stresses is proposed and researched. The proposed converter, which is

named a DAB^3 converter, is suitable for high-power applications since the system's parasitic elements are used effectively. The idea of effectively using both the leakage inductance of the isolation transformer and the parasitic capacitance of the switch devices originates from the DAB topology. The leakage inductance of the isolation transformer is used as a main power-transfer element. In the DAB^3 converter, the duty ratio and the phase-shift angle are used as control variables. By varying the transformer-input voltages on both sides, the device currents can be controlled to be low. As a result, this converter has low TDR compared with the conventional converters.

In Chapter 4, the ZVS regions are analyzed on the power-transfer curve. ZVS is feasible with the DAB^3 converter. ZVS depends on the voltage conditions of the clamp and output voltages. As the duty ratio and phase shift angle vary, the feasibility of ZVS depends on the duty ratio and phase-shift angle. The estimated switching losses of the DAB^3 converter support the benefits of flat-top operation. When the flat-top condition exists, the loss in the switch device becomes minimal. The minimal loss designs for the magnetic devices are presented and discussed. Finally, total system loss is presented.

Chapter 5 presented small-signal models of the converter. Two steps were used for the derivation of the small-signal models. The first step is time-average modeling. The second step is perturbation and linearization. The average modeling is applied to remove the high-frequency components in the waveforms. The perturbation and linearization methods are used to develop ac small-signal models of the state equations. The transfer functions relating system outputs to control-input variables were developed.

In Chapter 6, controllers were designed and validated experimentally. Based on the control loops which regulate the clamp and output voltages, a method to prevent dc current in the transformers was proposed and validated experimentally.

7.2. Contributions

1. A bi-directional dc/dc converter, DAB^3 converter was developed. In this converter, device stresses are controlled for wide input/output ranges, and parasitic elements are effectively used to transfer power. Hence, the proposed converter has a low TDR for wide input/output ranges.
2. The DAB^3 converter's characteristics were researched. The condition for ZVS is analyzed on the power-transfer curves. This analysis is useful in studying the converter's efficient operating region. Power-loss estimation for minimal loss design is performed.
3. Power-loss estimation for a minimal loss design was performed.
4. A small-signal model of the DAB^3 converter was developed.
5. Digital controllers implemented in FPGA, based on Verilog-HDL, were developed to minimize propagation delays. Controllers to simultaneously minimize device ratings, regulate the output voltage, and prevent dc currents in the transformer were developed.

A number of conference papers related to this research have been published. 2 journal papers are under development.

1. Sangtaek Han; Munuswamy, I.; Divan, D., "Preventing transformer saturation in bi-directional dual active bridge buck-boost DC/DC converters," in Proc. 2010 IEEE Energy Conversion Congress and Exposition (ECCE), Atlanta, GA, USA, Sep 12-16, 2010.

2. Sangtaek Han; Divan, D., "Dual active bridge buck-boost converter," in Proc. 2009 IEEE Energy Conversion Congress and Exposition (ECCE), San Jose, CA, Sept 20-24, 2009.

3. Sangtaek Han; Divan, D., "Bi-directional DC/DC converters for plug-in hybrid electric vehicle (PHEV) applications," in Proc. 2008 IEEE Applied Power Electronics Conference and Exposition (APEC), Feb. 24-28, 2008.

7.3. Recommendations for Future Research

Several topics are possible for future research on the DAB^3 converter.

1. Parametric optimization for volume and efficiency. For the power-density optimization, thermal models are required for the components since thermal constraints impact the converter volume. Furthermore, loss estimation requires a more accurate loss model for switch based on switch-loss characterization.
2. Development of a combination of the series resonant and DAB^3 topologies. If feasible, such a combination would enable higher switching frequency with lower losses and prevention of the saturation of the isolation transformer. This may result in a higher volume density.
3. Design and analysis of heat management devices.

APPENDIX A

DEVICE RATINS OF CONVERTERS

Device-Current Ratings of the M-DAB Converter

With respect to Figure 2.10, the device current ratings of M-DAB topology can be derived.

$I_{C1\_RMS} \cong \frac{1}{3}\{|I_3 - I_{s0}|^2 + |h|^2 + |I_3 - I_{s0}| \times |h|\} \times \frac{\emptyset}{2\pi} + \frac{1}{3} \times h^2 \times D_{x1} + \frac{1}{3}(I_1 - I_{s1})^2 \times D_{x2})\}^{0.5}$.

$I_{C2\_RMS} \cong \{\frac{1}{3} \times \left(I_{s0}{}^2 + I_{s1}{}^2 + |I_{s0}| \times |I_{s1}|\right) \times (1 - D) + \frac{1}{3} \times |I_2|^2 \times \frac{\emptyset}{2\pi} + \frac{1}{3} \times (I_2^2 + I_3^2 + |I_2| \times I3 \times D - \emptyset 2\pi\}0.5$.

$I_{C3\_RMS} \cong \{(|NI_0 - I_{LOAD}|)^2 \times \left((1 - D) - \frac{\emptyset}{2\pi}\right) + (I_{LOAD})^2 \times (D) + |NI_0 - I_{LOAD}|^2 \times \frac{1}{3} D_{x3} + \frac{1}{3} \times |NI_2 - I_{LOAD}|^2 \times D_{x4}\}^{0.5}$.

$I_{C4\_RMS} \cong \{(|I_{LOAD}|)^2 \times (1 - D) + (-|I_{LOAD}| - |NI_2|)^2 (D - \frac{\emptyset}{2\pi}) + \frac{1}{3} \times (|-NI_2 - I_{LOAD}|)^2 \times D_{x5} + \frac{1}{3} \times |I_{LOAD}|^2 \times \left(\frac{\emptyset}{2\pi} - D_{x5}\right)\}^{0.5}$.

$h = I_0 - (I_{s0} - \Delta) = I_0 - I_{s0} + \frac{V_s}{L_{dc}} \times \frac{\emptyset}{2\pi} \times T_s$.

$M = I_1 - I_{s1.}$

$D_{x1} = (1 - D - \frac{\emptyset}{2\pi}) \times \frac{|h|}{(h+M)}$, $D_{x2} = (1 - D - \frac{\emptyset}{2\pi}) \times \frac{|M|}{(h+M)}$.

$D_{x3} = \frac{\emptyset}{2\pi} \times \frac{|NI_0 - I_{LOAD}|}{(|NI_0 - I_{LOAD}| + |I_{LOAD}|)}$, $D_{x4} = \frac{\emptyset}{2\pi} \times \frac{|I_{LOAD}|}{(|NI_0 - I_{LOAD}| + |I_{LOAD}|)}$.

$D_{x5} = \frac{\emptyset}{2\pi} \times \frac{|NI_2 + I_{LOAD}|}{(|NI_2 + I_{LOAD}| + |I_{LOAD}|)}$, $D_{x6} = \frac{\emptyset}{2\pi} \times \frac{|I_{LOAD}|}{(|NI_2 + I_{LOAD}| + |I_{LOAD}|)}$.

Peak current of switch devices of M-DAB converter

Switch device	Voltage stress	$I_{SWpeak}(A)$
SW_1	$\frac{V_{in}}{(1-D)}$	Max($\|I_3- I_{s0}\|$,$\|I_1-I_{s1}\|$)
SW_2	$\frac{V_{in}}{(1-D)}$	Max($\|I_{s1}-I_1\|$, $\|I_{s1}-I_2\|$,$\|I_{s1}-I_3\|$)
SW_3	V_o	Max($\|NI_0\|$, $\|NI_1\|$, $\|NI_2\|$)
SW_4	V_o	Max($\|NI_0\|$, $\|NI_2\|$, $\|NI_3\|$)

Capacitor-Current Ratings of the DAB^3 Converter

$I_{clamp\_RMS} = \{I_s^2 \times d_1 + |I_s - I_{L2}|^2 \times \frac{1}{3} d_2 + |I_s - I_{L2}|^2 \times D\}^{0.5}$

$I_{co\_RMS} = \{|NI_2 - I_L|^2 \times 2D + 2(0.5 - D) \times |I_L|^2\}^{0.5}$

I_s= source current= $\frac{P_o}{V_s}$

I_L= load current= = $\frac{P_o}{V_o}$

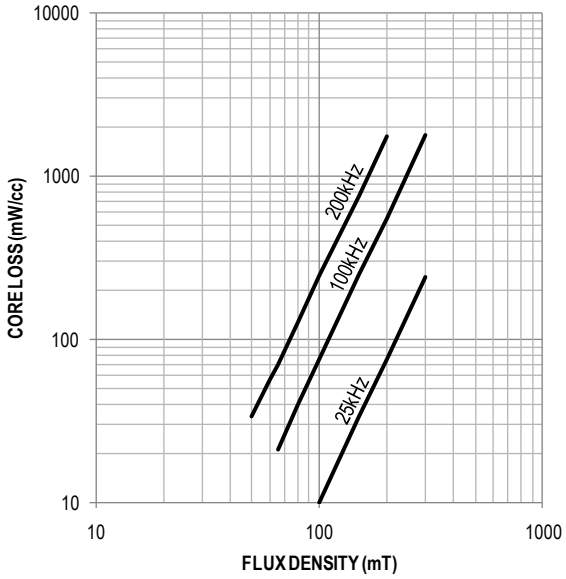
I_{L2}= $I_2 = \frac{(2\emptyset - \delta)}{2\omega L_s} V_1 + \frac{\delta}{2\omega L_s} NV_2$

$d_1 = \frac{|I_s|}{(|I_s| + |I_s - I_{L2}|)} \frac{\emptyset}{2\pi}$

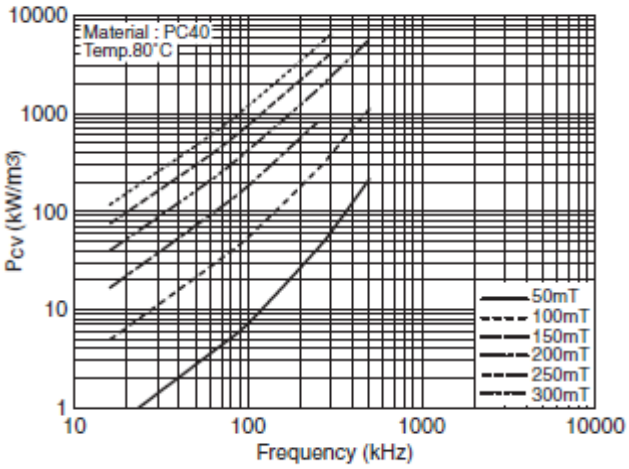
$d_2 = \frac{|I_s - I_{L2}|}{(|I_s| + |I_s - I_{L2}|)} \frac{\emptyset}{2\pi}$

APPENDIX B

CORE LOSS DATA PLOTS



Core-loss plot for F-perm (Mag-Inc).



Core-loss plot for PC 40 (TDK).

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